ISL72813SEH

32-Channel Driver Circuit with an Integrated Decoder

FN8884
Rev 2.00
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The ISL72813SEH is a radiation hardened, high-voltage, high-current, driver circuit fabricated using the Renesas proprietary PR40 silicon-on-insulator process technology to mitigate single-event effects. This device integrates 32 driver circuits that feature high-voltage, common emitter, and open-collector outputs with a 42V breakdown voltage and a peak current rating of 600mA.

To further reduce solution size and increase system power density, the ISL72813SEH integrates a 5-bit to 32-channel decoder (plus enable pin) as well as level shifting circuitry to reference the output of the decoder to a negative voltage. This conveniently allows the user to select 1 of 32 available driver channels. The inputs to the decoder are TTL/CMOS compatible, allowing easy interface to CPUs, FPGAs, or microprocessors.

The ISL72813SEH operates across the military temperature range from -55°C to +125°C and is available in a 44 Ld hermetically sealed Ceramic Lead-Less Chip Carrier (CLCC) package.

Related Literature

For a full list of related documents, visit our website

- ISL72813SEH product page

Features

- Electrically screened to SMD 5962-17208
- Acceptance tested to 100krad(Si) (HDR) and to 50krad(Si) (LDR) wafer-by-wafer
- Integrated 5-bit to 32-channel decoder
- Integrated level shifting circuit
- High collector current outputs
- High voltage outputs
- Grounded metal lid
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Radiation tolerance
  - HDR (50rad(Si)/s to 300rad(Si)/s) . . . . . 100krad(Si)
  - LDR (0.01rad(Si)/s) . . . . . 50krad(Si)
- SEE hardness
  - No SEB/SEL LET_{TH}, V_{CE} = 33V . . . . . 86.4MeV•cm^2/mg

Applications

- Waveguide switches and coaxial switches
- Relays
- Line drivers
- Logic buffers
- Lamp drivers

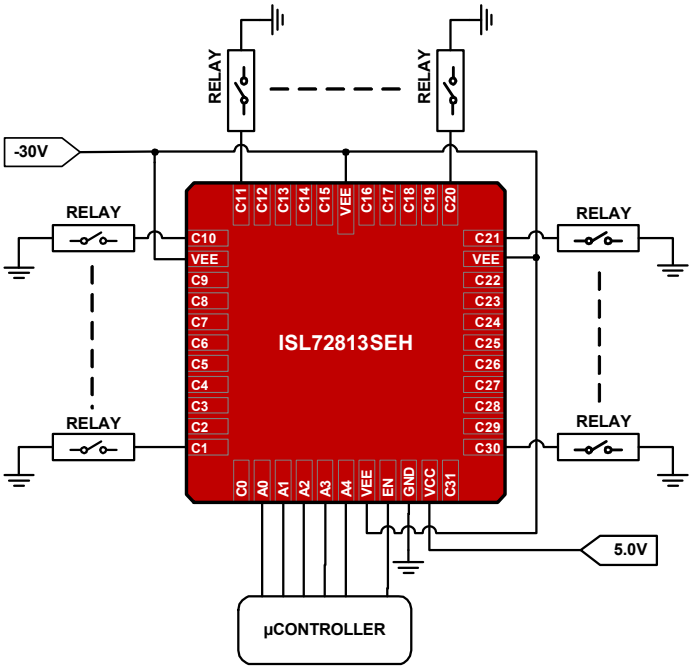


FIGURE 1. TYPICAL APPLICATION

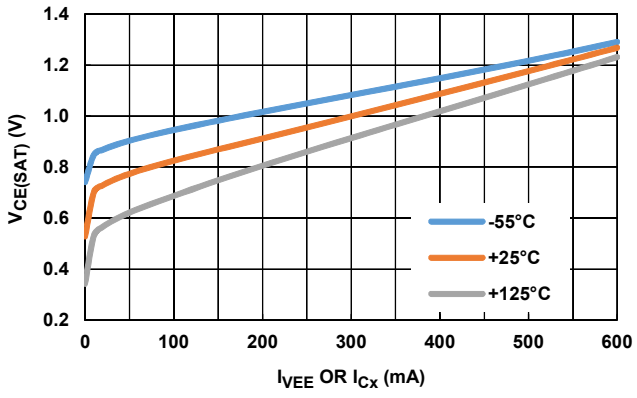


FIGURE 2. $V_{CE(SAT)}$ vs I_{Cx} vs TEMPERATURE

Functional Block Diagram

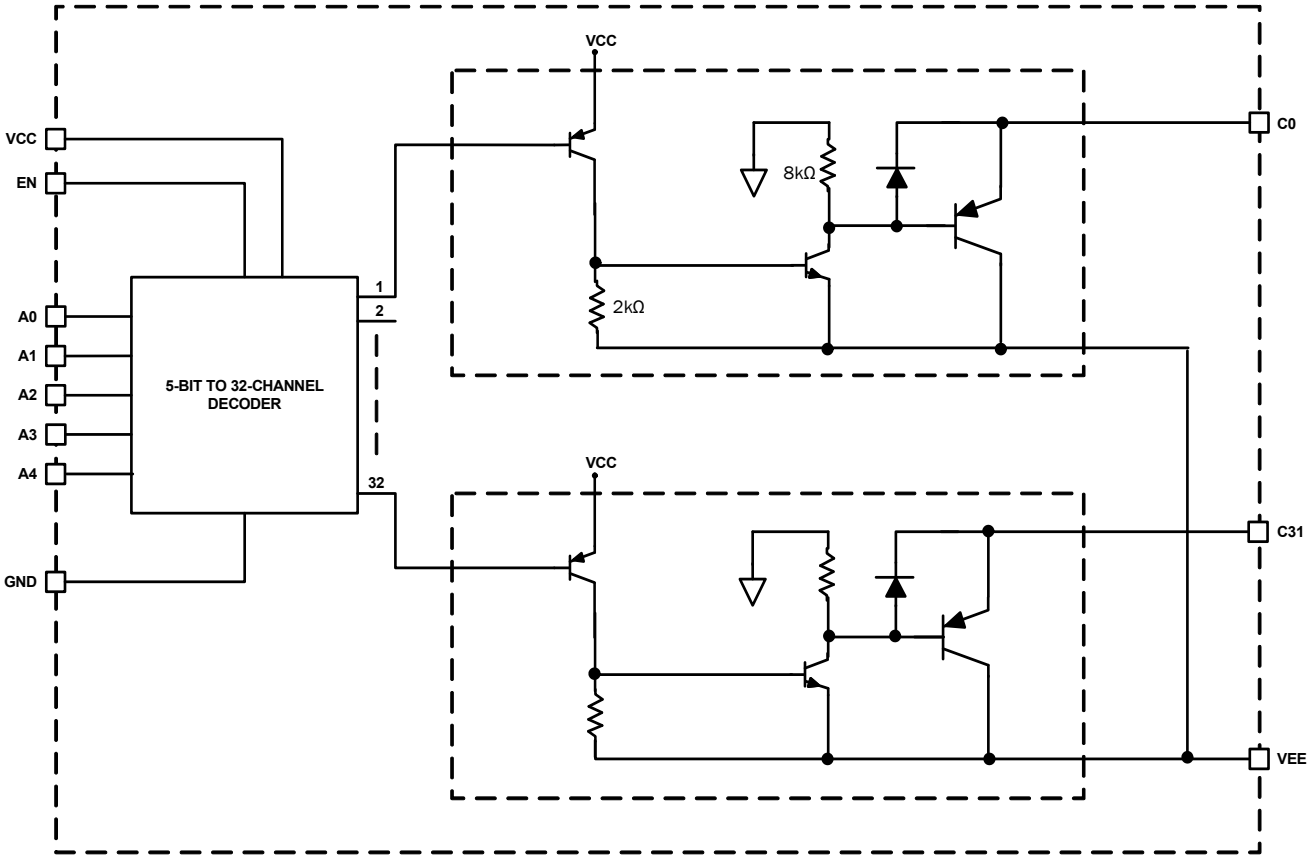


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM (Complementary Darlington)

Ordering Information

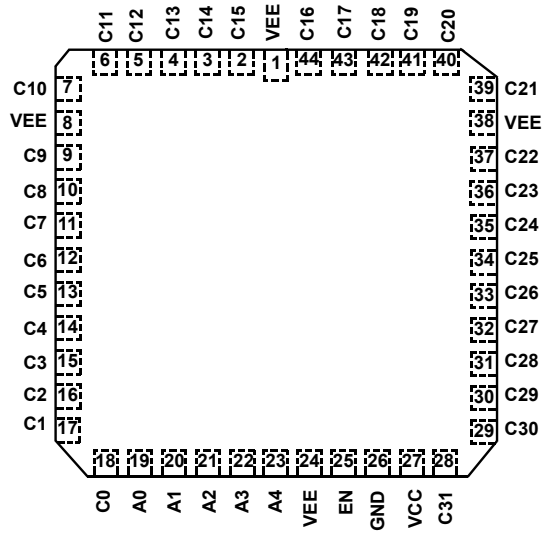
ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PACKAGE DRAWING
5962R1720801VXA	ISL72813SEHVL	-55 to +125	44 Ld CLCC	J44.A
N/A	ISL72813SEHL/PROTO, (Note 3)	-55 to +125	44 Ld CLCC	J44.A
5962R1720801V9A	ISL72813SEHVX	-55 to +125	Die	-
N/A	ISL72813SEHX/SAMPLE, (Note 3)	-55 to +125	Die	-
N/A	ISL72813SEHEV1Z (Note 4)	Evaluation Board		

NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.
4. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

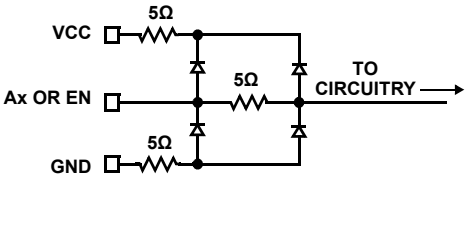
Pin Configuration

ISL72813SEH
(44 LD CLCC)
TOP VIEW

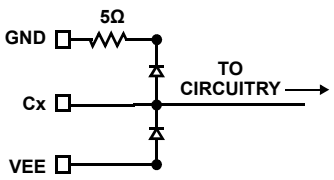


Pin Descriptions

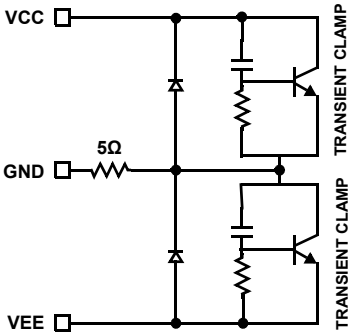
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1, 8, 24, 38	VEE	Circuit 3	Common emitter of all 32 channels.
2-7, 9-18, 28-37, 39-44	Cx	Circuit 2	Channels 0 through 31 collector output.
19-23	Ax	Circuit 1	Address lines for the decoder.
25	EN	Circuit 1	Active high enable input to the decoder.
26	GND	Circuit 3	Supply ground. Connect this pin to the PCB ground plane.
27	VCC	Circuit 3	Bias supply for the decoder and the level shift circuit. Connect to 5V.
LID	N/A	N/A	Package Lid is internally connected to GND.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Typical Application Schematic

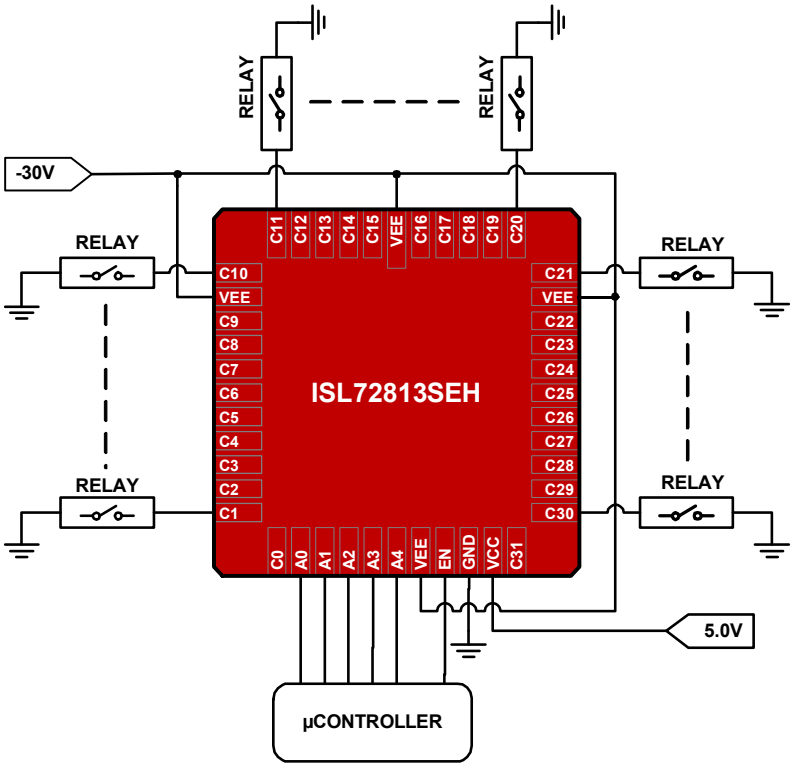
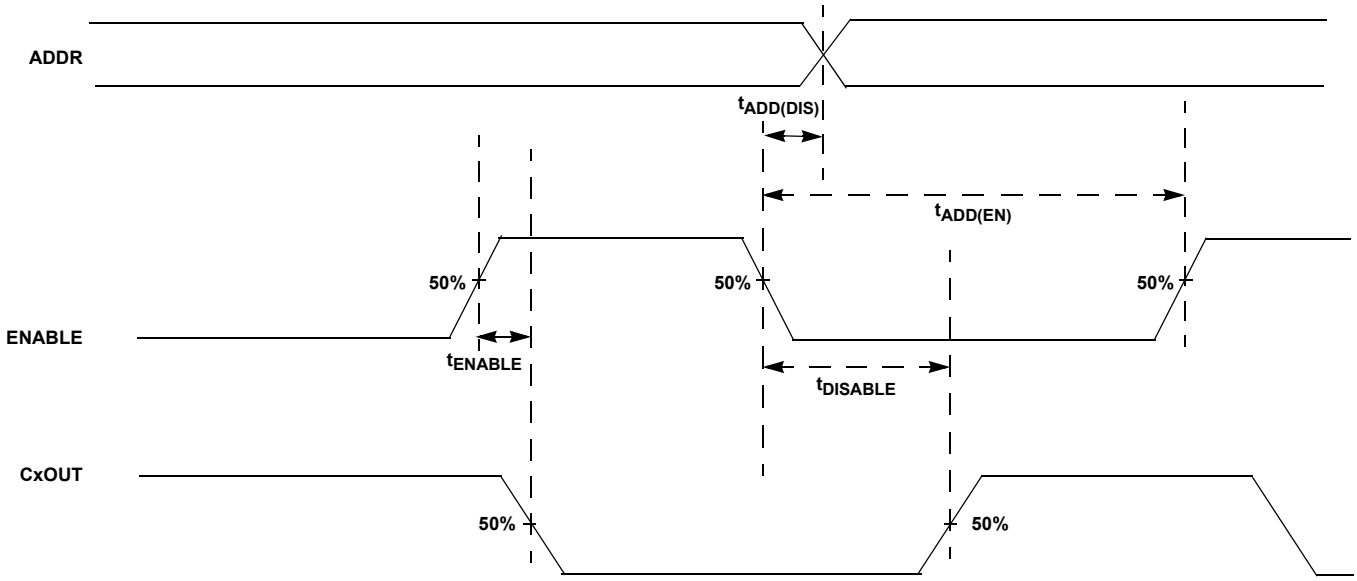


FIGURE 4. TYPICAL APPLICATION DIAGRAM

Timing Diagram



$t_{ADD(DIS)}$ and $t_{ADD(EN)}$ cannot be measured but are provided as a reference.
$t_{ADD(DIS)} = t_{ENABLE} \leq 10\mu s$
$t_{ADD(EN)} = t_{DISABLE} \leq 50\mu s$

FIGURE 5. TIMING DIAGRAM

TABLE 1. TRUTH TABLE

A4	A3	A2	A1	A0	EN	CHANNEL
X	X	X	X	X	0	NONE
0	0	0	0	0	1	0
0	0	0	0	1	1	1
0	0	0	1	0	1	2
0	0	0	1	1	1	3
0	0	1	0	0	1	4
0	0	1	0	1	1	5
0	0	1	1	0	1	6
0	0	1	1	1	1	7
0	1	0	0	0	1	8
0	1	0	0	1	1	9
0	1	0	1	0	1	10
0	1	0	1	1	1	11
0	1	1	0	0	1	12
0	1	1	0	1	1	13
0	1	1	1	0	1	14
0	1	1	1	1	1	15
1	0	0	0	0	1	16
1	0	0	0	1	1	17
1	0	0	1	0	1	18
1	0	0	1	1	1	19
1	0	1	0	0	1	20
1	0	1	0	1	1	21
1	0	1	1	0	1	22
1	0	1	1	1	1	23
1	1	0	0	0	1	24
1	1	0	0	1	1	25
1	1	0	1	0	1	26
1	1	0	1	1	1	27
1	1	1	0	0	1	28
1	1	1	0	1	1	29
1	1	1	1	0	1	30
1	1	1	1	1	1	31

Absolute Maximum Ratings

V_{CC} . . . . . (GND - 0.3V) to GND + 6.5V
GND - VEE. 42V
GND - VEE (Note 8) 33V
V_{Cx} . . . . . (GND + 0.3V) to V_{EE} - 0.3V
Logic Input Voltage (EN, Ax) . . . . . (GND - 0.3V) to V_{CC} + 0.3V
Logic Input Current (EN, Ax) . . . . . ±15mA
Power Dissipation, PD 1.25W
Peak I_{CE}. 600mA
Maximum Supply Turn-On Ramp Rate (V_{EE}). . . . . -1V/µs
Maximum Supply Turn-On Ramp Rate (V_{CC}). . . . . +0.5V/µs
ESD Rating
Human Body Model (Tested per MIL-STD-883 TM 3015) 7kV
Machine Model (Tested per JESD22-A115-C). 300V
Charge Device Model (Tested per JS-002-2014) 1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
44 Ld CLCC (Notes 5, 6).	25	1.2

Maximum Junction Temperature . . . . . +150°C
Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Temperature . . . . . -55°C to +125°C
V_{CC} . . . . . 3.3V ±10% or 5V ±10%
GND - VEE . . . . . 5V to 34V
$|V_{Cx}$ - VEE| . . . . . 5V to 34V
Maximum Lifetime Duty Cycle vs I_{CE} (Note 7)
170mA. 100%
200mA. 73%
300mA. 32%
400mA. 18%
500mA. 12%
530mA. 10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the package underside.
7. Based on assumed 1.6 x 10^5 hours lifetime at +150°C junction temperature to 0.1% failures.
8. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg at +125°C (TC) for SEB. Refer to the Single Event Effects Test Report for more information.

Electrical Specifications

Test Conditions: V_{CC} = 5.0V, V_{EE} = -34V. Logic High = V_{CC} and Logic Low = GND; typicals are at T_A = +25°C unless otherwise noted (Note 9). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) at +25°C with exposure at a high dose rate of 50rad(Si)/s to 300rad(Si)/s; over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP (Note 9)	MAX (Note 10)	UNIT
POWER SUPPLY						
Supply Current	I_{CC}	V_{CC} = 3.6V, 5.5V, V_{EE} = 0V and -34V, Cx = OPEN, EN = V_{CC}	-	7.0	**9.5**	mA
Quiescent Supply Current	I_{CCQ}	V_{CC} = 3.6V, 5.5V, V_{EE} = 0V and -34V, Cx = OPEN, EN = 0V	-	625	**850**	µA
Supply Current	I_{EE}	V_{CC} = 3.6V, 5.5V, V_{EE} = -34V, Cx = OPEN, EN = V_{CC},	-	-9	-	mA
Quiescent Supply Current	I_{EEQ}	V_{CC} = 3.6V, 5.5V, V_{EE} = -34V, Cx = OPEN, EN = 0V	**-100**	-2.5	-	µA
DRIVER CIRCUIT						
Output Collector Leakage Current	I_{CEX}	V_{CC} = 3.6V, 5.5V, V_{Cx} = 0V, V_{EE} = -34V, EN = 0V	-	0.01	**40.00**	nA
Collector - Emitter Saturation Voltage $V_{CE(SAT)} = V_{Cx} - V_{EE}$	$V_{CE(SAT)}$	I_C = 530mA, V_{CC} = 3.0V, 4.5V, V_{EE} = -34, EN = V_{CC}	-	1.098	**1.500**	V
		I_C = 500mA, V_{CC} = 3.0V, 4.5V, V_{EE} = -34, EN = V_{CC}	-	1.077	**1.450**	V
		I_C = 350mA, V_{CC} = 3.0V, 4.5V, V_{EE} = -34, EN = V_{CC}	-	0.974	**1.400**	V
		I_C = 200mA, V_{CC} = 3.0V, 4.5V, V_{EE} = -34, EN = V_{CC}	-	0.874	**1.300**	V

Electrical Specifications Test Conditions: V_{CC} = 5.0V, V_{EE} = -34V. Logic High = V_{CC} and Logic Low = GND; typicals are at T_A = +25°C unless otherwise noted (Note 9). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) at +25°C with exposure at a high dose rate of 50rad(Si)/s to 300rad(Si)/s; over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP (Note 9)	MAX (Note 10)	UNIT
DECODER INPUTS						
High-Level Threshold	V_{IH}	V_{CC} = 3.0V, 5.5V	**2**	-	-	V
Low-Level Threshold	V_{IL}	V_{CC} = 3.0V, 5.5V	-	-	**0.8**	V
Input High Current	I_{IH}	V_{CC} = 5.5V, tested logic input = 2.0V	**-500**	-125	-	nA
Input Low Current	I_{IL}	V_{CC} = 5.5V, tested logic input = 0.8V	**-500**	-190	-	nA
Input High Current	I_{IH}	V_{CC} = 3.0V, tested logic input = 2.0V	**-500**	-10.7	-	nA
Input Low Current	I_{IL}	V_{CC} = 3.0V, tested logic input = 0.8V	**-500**	-70	-	nA
SWITCHING CHARACTERISTICS						
Enable Turn-On Time (Notes 11, 12, 13)	t_{ENABLE}	V_{CC} = 3.0V, 5.5V, R_{LOAD} = 64.4Ω	-	2.3	**10**	µs
Disable Turn-Off Time (Notes 11, 12, 13)	$t_{DISABLE}$	V_{CC} = 3.0V, 5.5V, R_{LOAD} = 64.4Ω	-	3.9	**50**	µs

NOTES:

9. Typical values shown are not guaranteed.
10. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.
11. Addressing should only be changed while EN = GND or VEE is unbiased; otherwise, multiple outputs can be activated. See "Ensuring Break-Before-Make (BBM) Operation" on page 8.
12. After disabling (EN = 0) and changing addresses, you must wait at most 50µs before enabling (EN = 1) the new channel. This prevents multiple outputs from being momentarily ON at the same time. See "Ensuring Break-Before-Make (BBM) Operation" on page 8.
13. Limits established by characterization and are not production tested.

Functional Description

Functional Overview

The ISL72813SEH is a radiation hardened, high-voltage, high-current, driver circuit fabricated using the Renesas proprietary PR40 silicon-on-insulator process technology to mitigate single-event effects. This device integrates 32 driver circuits that feature high-voltage, open-collector outputs with a 42V breakdown voltage. The peak current rating for each driver is 600mA.

The part has a 5-bit to 32-line decoder and an enable pin to select between the 32 driver channels or disable all the channels by driving the EN pin LOW. The logic inputs (A0 - A4) to the decoder and the enable pin (EN) are TTL/CMOS compatible.

VEE Supply Ramp Rate

If the ramp rate of the VEE supply is > |-1V/µs|, it is possible to turn on multiple channels during the ramping of the supply.

The internal capacitance of the part along with a fast VEE dV/dt can momentarily pull up the base voltages of the internal channel transistors high enough to turn on multiple channels. After the VEE supply reaches its steady state, the device will respond properly to its logic inputs.

Keeping the VEE ramp rate ≤ |-1V/µs| will ensure that the channels will remain OFF while the VEE supply is coming up.

Ensuring Break-Before-Make (BBM) Operation

The ISL72813SEH does not have internal circuitry to ensure Break-Before-Make (BBM) operation when switching from one channel to another channel. The design architecture of the part is inherently prone to Make-Before-Break (MBB) operation and the possibility exists that multiple channels can be momentarily ON when switching from one channel to another.

If the part is enabled (EN = 1) and you switch between channels by changing the logic settings at the A0 - A4 address pins, two or more channels can momentarily be ON at the same time. Eventually, only the channel that is being addressed will continue to be ON and the other channels will turn OFF.

During the period when multiple channels are simultaneously ON, these channels will conduct current through their respective switch cells into VEE. Depending on the loading at the channels, this current draw could interfere with proper operation of the application. Care must be taken to prevent MBB operation by properly using the enable pin to implement BBM operation.

Ensuring BBM operation (only one channel ON at any time) will require using the enable pin to completely disable the part before switching between channels. Complete the following steps to implement BBM operation:

1. Before switching from one channel to another channel, take the enable pin (EN) to the LOW state (logic 0). This will signal the internal logic to turn all switches OFF.
2. Wait at least 10µs ($t_{ADD(DIS)}$) to ensure the signal propagated through the internal logic.
3. Change the address to select the channel that you want to turn ON next by applying the appropriate logic to the A0 to A4 address pins.
4. Wait another 40µs to ensure two conditions:
   a. The address change propagated through the internal logic (10µs).
   b. The previous channel's switch is fully turned OFF (pulled up). This completes the 50µs delay required to ensure the previous channel is disabled ($t_{DISABLE}$).
5. Take the enable pin (EN) to the HIGH state (logic 1). This will enable the part. Only the channel that is addressed will be ON.
6. Wait 10µs (t_{ENABLE}) after enabling the part before repeating Steps 1 through 5 above.

Power Supply Sequencing

Starting with the VCC, EN, A0 - A4, and VEE pins all at 0V, the recommended power-on sequencing is:

1. VCC - Ramp the supply up to $5V_{DC}$ with a ramp rate ≤0.5V/µs).
2. A0 - A4 Logic Inputs - Apply the appropriate logic voltages to these pins to select a driver channel.
3. VEE - Ramp the supply to the negative bias voltage for the application at a ramp rate ≤ |-1V/µs|.
4. EN Logic Input - Set to a Logic 1 (High) to enable the part and turn ON the channel that is addressed by the logic levels at the A0 - A4 logic pins.

Note:

- If VCC is left floating, power the part through the logic inputs.
- If there is a bias on the VEE pin, VCC should ramp no faster than 0.5V/µs to avoid turning on unintended channels.

Typical Performance Curves

Unless otherwise noted, V_{CC} = 5V, V_{EE} = -34V

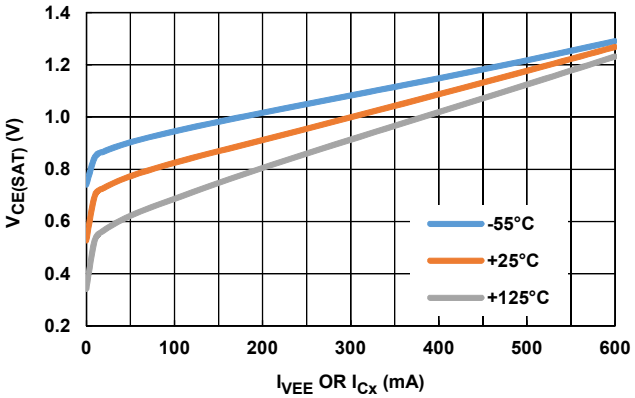


FIGURE 6. $V_{CE(SAT)}$ vs I_{CX} vs TEMPERATURE

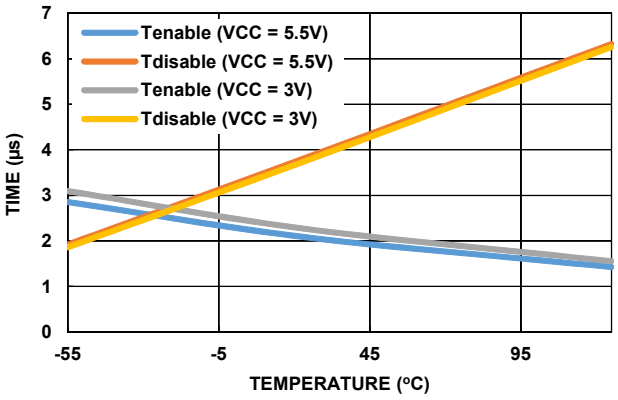


FIGURE 7. $t_{ENABLE}/t_{DISABLE}$ vs V_{CC} vs TEMPERATURE

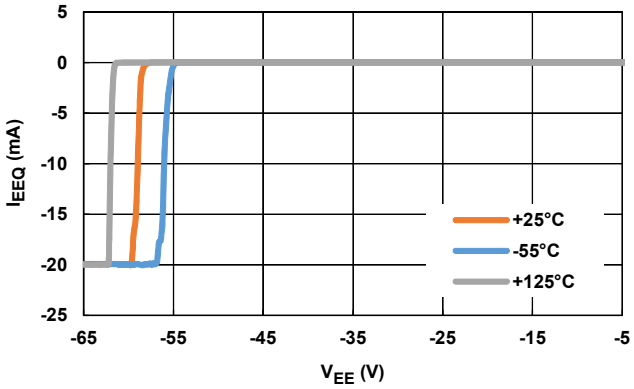


FIGURE 8. I_{EEQ} vs V_{EE} vs TEMPERATURE

Package Characteristics

Weight of Packaged Device

2.02 grams (typical)

Lid Characteristics

Finish: Gold
Lid Potential: GND

Die Characteristics

Die Dimensions

7100µm x 7100µm (280 mils x 280 mils)
Thickness: 305µm ±25µm (12 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

Dielectrically Isolated Advanced Bipolar Technology - PR40

ASSEMBLY RELATED INFORMATION

Substrate Potential

Floating

ADDITIONAL INFORMATION

Worst Case Current Density

$<2 \times 10^5$ A/cm^2

Transistor Count

3940

Metallization Mask Layout

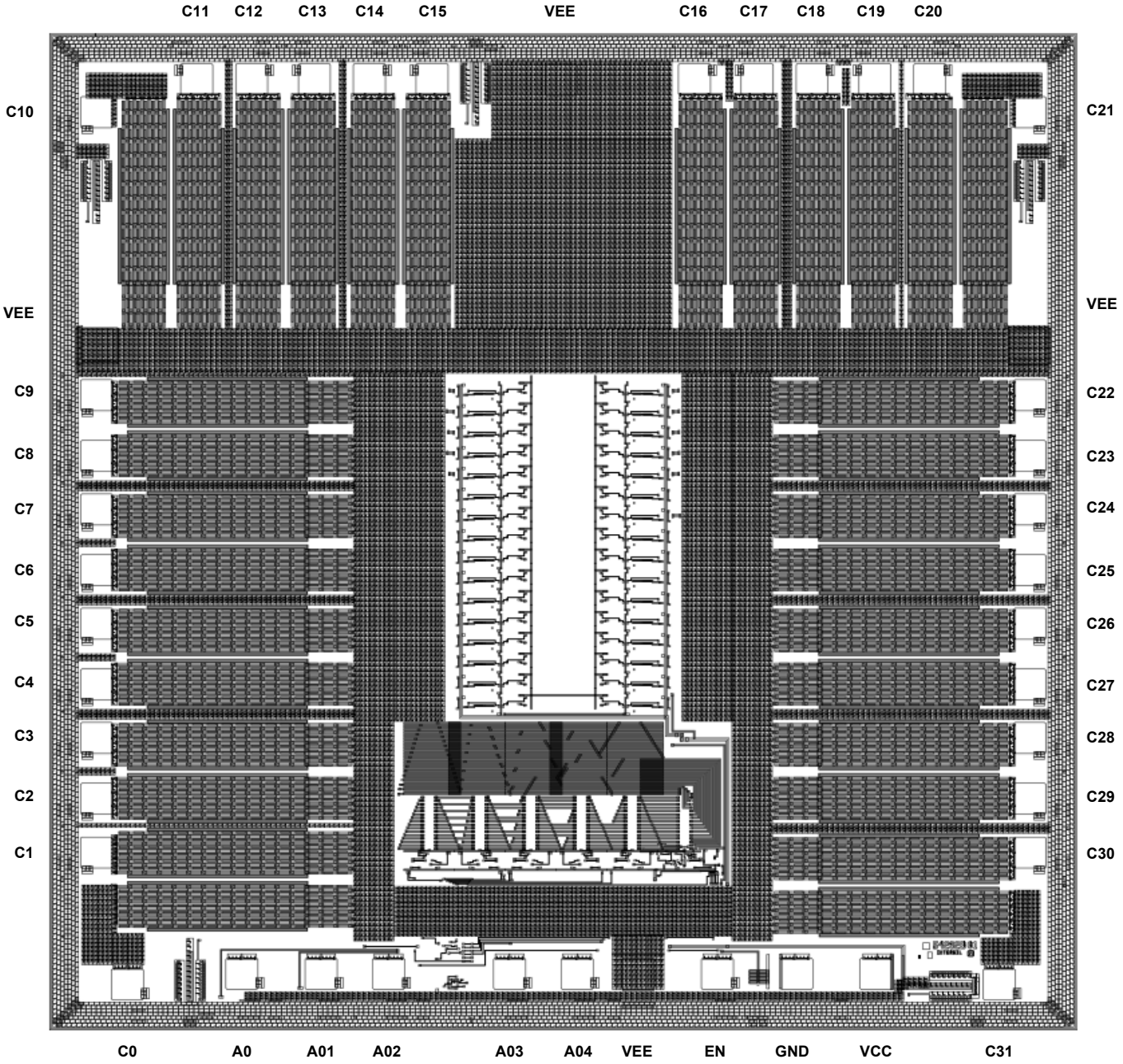


FIGURE 9. ISL72813SEH MASK LAYOUT

TABLE 2. LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)
C0	P18	584.5	376
C1	P17	376	1301
C2	P16	376	1677.5
C3	P15	376	2104.5
C4	P14	376	2478.5

TABLE 2. LAYOUT X-Y COORDINATES (Continued)

PAD NAME	PAD NUMBER	X (µm)	Y (µm)
C5	P13	376	2905.5
C6	P12	376	3279.5
C7	P11	376	3706.5
C8	P10	376	4080.5
C9	P9	376	4507.5
VEE8	P8	379	4863.5
C10	P7	376	6491.5
C11	P6	1056.5	6723.5
C12	P5	1430.5	6723.5
C13	P4	1857.5	6723.5
C14	P3	2230.5	6723.5
C15	P2	2657.5	6723.5
VEE1	P1	3538	6719
C16	P44	4442.5	6723.5
C17	P43	4869.5	6723.5
C18	P42	5242.5	6723.5
C19	P41	5669.5	6723.5
C20	P40	6043.5	6723.5
C21	P39	6724	6491.5
VEE38	P38	6719	4863.5
C22	P37	6724	4507.5
C23	P36	6724	4080.5
C24	P35	6724	3706.5
C25	P34	6724	3279.5
C26	P33	6724	2905.5
C27	P32	6724	2478.5
C28	P31	6724	2104.5
C29	P30	6724	1677.5
C30	P29	6724	1301
C31	P28	6515.5	376
VCC	P27	5676	451
GND	P26	5137	451
EN	P25	4598	451
VEE24	P24	4059	451
A4	P23	3644	451
A3	P22	3185	451
A2	P21	2362	451
A1	P20	1903	451
A0	P19	1364	451

NOTES:

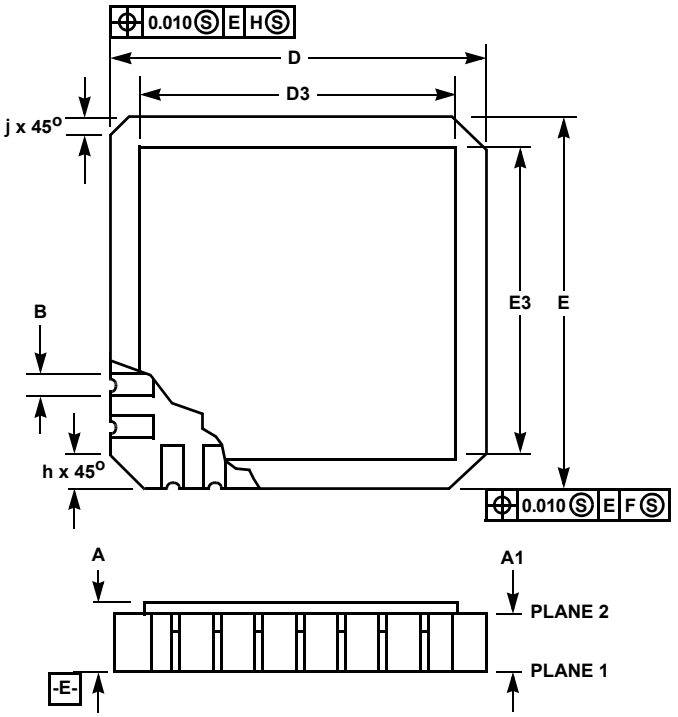
14. Origin of coordinates is the centroid of pad P18.
15. Pad size for all pads: 195µm x 195µm.
16. Bond wire size: 0.002”.

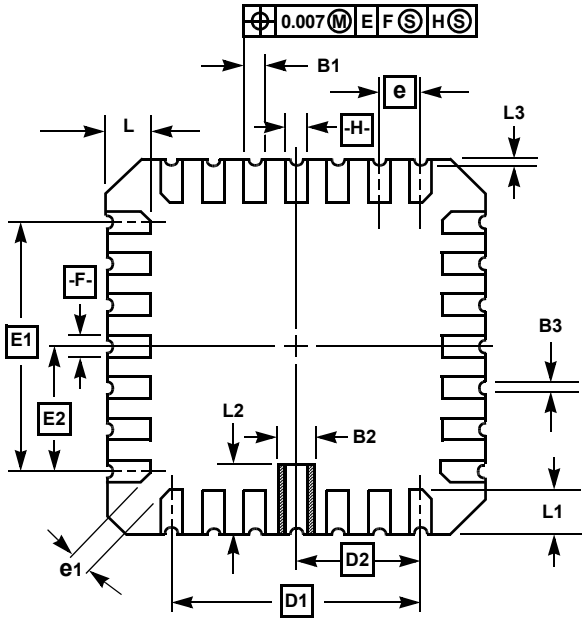
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Mar 30, 2018	FN8884.2	Updated Figure 3 by fixing the lines that were not properly connected. Removed About Intersil section and updated Disclaimer.
Feb 20, 2017	FN8884.1	Changed from “radiation tolerant” to “radiation hardened” throughout document. Page 1: Changed “current driver” in first and second paragraphs to “driver circuit(s)” Added “SMD #” to the Features section. Added “Waveguide switches and coaxial switches” to the Application section. Added “(Complementary Darlington)” to Figure 3 title on page 2. Added the “SMD part numbers” and “Notes 3 and 4” to the Ordering Information table on page 2. Page 3 - Pin Description table Descriptions column: VEE - changed “current drivers” to “channels” Cx - removed “current driver” In Recommended Operating Conditions section on page 6 changed VCC to: 3.3V ±10% or 5V ±10%. For IEE in specification table on page 6, removed minimum limit and changed typical from -33mA to -9mA.
Nov 17, 2016	FN8884.0	Initial Release

Ceramic Leadless Chip Carrier Packages (CLCC)





For the most recent package outline drawing, see J44.A.

J44.A MIL-STD-1835 CQCC1-N44 (C-5)

44 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.120	1.63	3.05	6, 7
A1	0.054	0.088	1.37	2.24	-
B	0.033	0.039	0.84	0.99	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.640	0.662	16.26	16.81	-
D1	0.500 BSC		12.70 BSC		-
D2	0.250 BSC		6.35 BSC		-
D3	-	0.662	-	16.81	2
E	0.640	0.662	16.26	16.81	-
E1	0.500 BSC		12.70 BSC		-
E2	0.250 BSC		6.35 BSC		-
E3	-	0.662	-	16.81	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	11		11		3
NE	11		11		3
N	44		44		3

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NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

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