ISL73041SEH

Radiation Hardened 12V Half-Bridge GaN FET Driver

The ISL73041SEH is a Radiation Hardened PWM input 12V Half Bridge GaN FET Driver designed to drive low $r_{DS(ON)}$ Gallium Nitride FETs for DC/DC switching regulators. An integrated programmable GaN FET gate drive voltage, high-side bootstrap switch, and strong gate drive current provide a compact and robust GaN FET half-bridge driver.

The ISL73041SEH can interface directly to the ISL73847SEH dual-phase PWM buck controller to create a high-efficiency point-of-load regulator to power many of the latest low voltage high current FPGA and DSP digital core rails.

Applications

- High current DC/DC Point-of-Load (POL) for FPGA and DSP supply rails
- 5V or 12V input to 1V output POL regulation
- GaN FET motor driver
- Combine with ISL73847SEH DC/DC PWM controller and Renesas GaN FETs for a complete DC/DC solution

Features

- Qualified to Renesas Rad Hard QML-V Equivalent Screening and QCI Flow (R34TB0001EU)
  - All screening and QCI is in accordance with MIL-PRF-38535L Class-V
- Up to 20V bootstrap voltage half-bridge driver
- Programmable 4.5V to 5.5V gate drive voltage
- Single tri-level PWM input control
- Separate source and sink driver outputs
- High-side peak drive: 2A Sourcing, 4A Sinking
- Low-side peak drive: 4A Sourcing, 8A Sinking
- High and low side programmable dead time control
- Highly matched fast propagation delay: 29ns
- Full military temperature operation T_A = -55°C to 125°C ambient range
- TID Rad Hard Assurance (RHA) testing
  - LDR (≤ 10mrad(Si)/s): 75krad(Si)
- SEE Characterization (see SEE report for details)
  - No DSEE with V_{DD} = 20V or PHS = 13.5V at LET 86MeV·cm^2/mg
  - No DSEE with V_{DD} = 20V or PHS = 16.5V at LET 67MeV·cm^2/mg
  - SEFI <10µm^2 at 86MeV·cm^2/mg
  - No Half-Bridge Shoot-Through SET at LET 86MeV·cm^2/mg

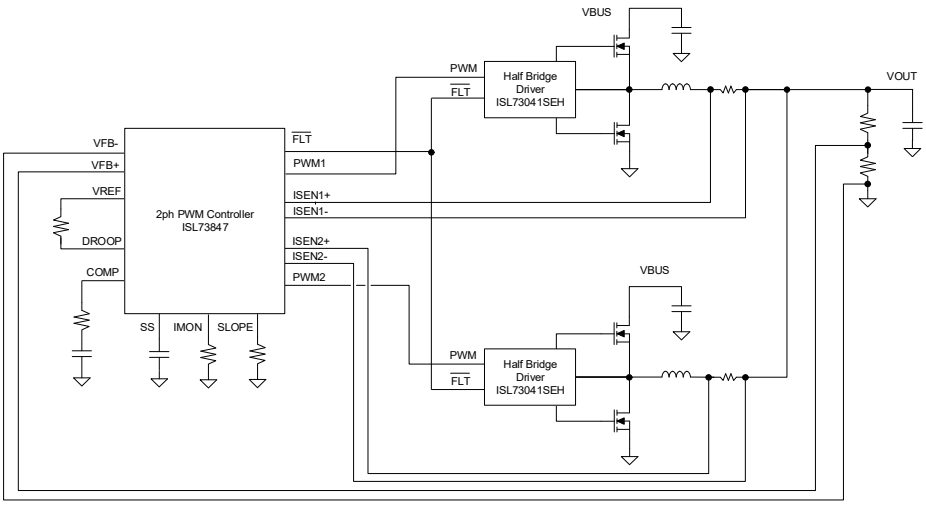

Figure 1. Typical Application Schematic: 2-Phase Controller + Bridge Driver + GaN FETs for 12V Input, 1.0V Output, 50A DC/DC Converter

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1. Overview

1.1 Block Diagram

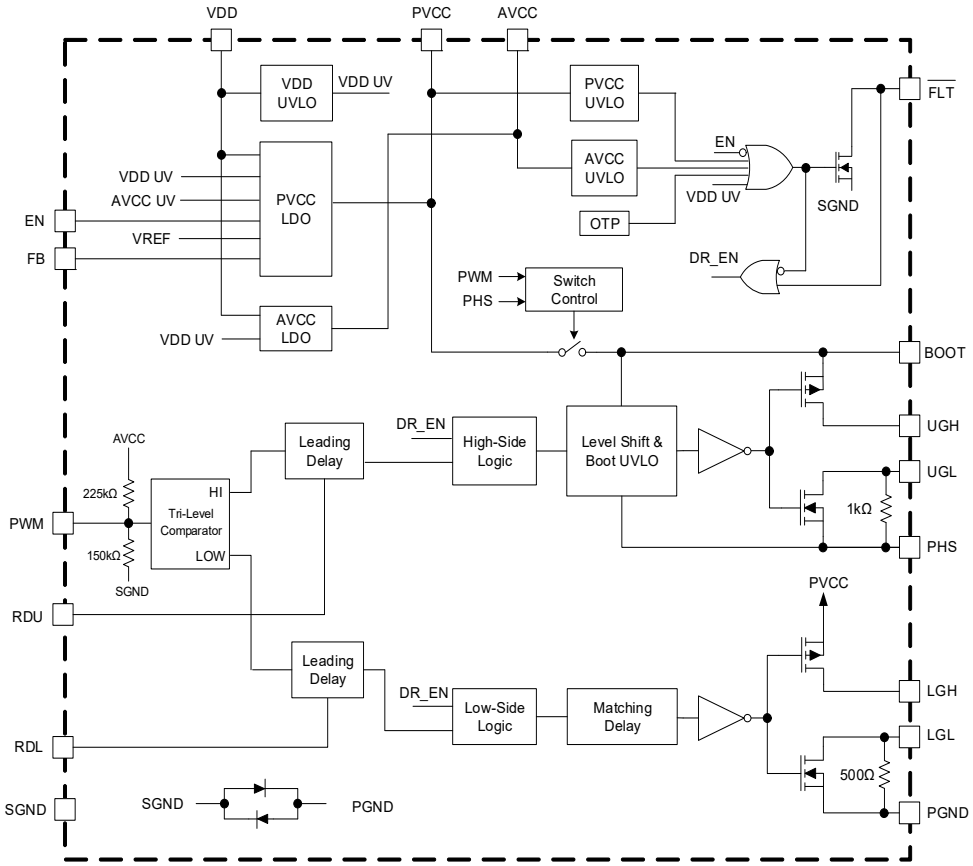


Figure 2. Circuit Block Diagram

2. Pin Information

2.1 Pin Assignments

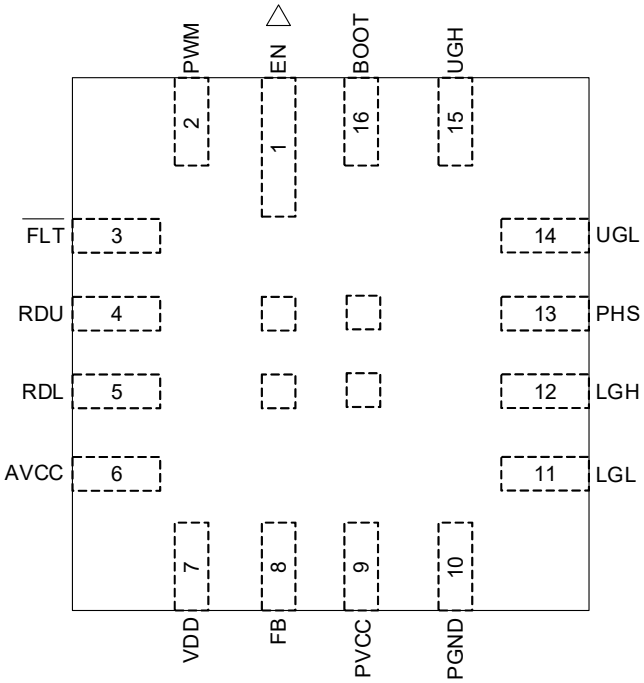


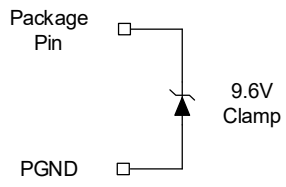
Figure 3. Pin Assignments - Top View

Note: The package lid is branded with a triangular mark that is placed near Pin #1. The Pin #1 bottom pad is approximately twice as long as Pin #2 through #16. The lid seal ring flashing is extended around the castellation of Pin #1 for a visual indicator.

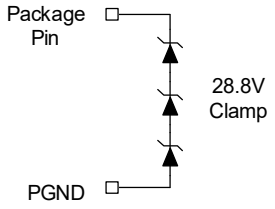
2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	EN	2	Enable input pin. When EN is low, driver outputs are in a high-impedance state and do not respond to PWM inputs. The PVCC LDO is shut down, and the $\overline{FLT}$ pin is internally pulled low. When EN is high, the PVCC LDO is enabled, and the driver outputs respond to PWM inputs. EN pin is VDD voltage compliant.
2	PWM	1	Tri-Level PWM input pin. Logic high turns on the high-side gate driver. Logic low turns on the low-side gate driver. Mid-Level turns off both gate drivers. Internal pull-up and pull-down resistors bias pin to mid-level when not externally driven.
3	$\overline{FLT}$	1	I/O pin. As an open-drain output, $\overline{FLT}$ is an active low indicator for when EN = 0, VDD UVLO, AVCC UVLO, PVCC UVLO, or in an over-temperature fault. As a high-impedance input, $\overline{FLT}$ disables the driver outputs when driven low. Place a pull-up resistor on the $\overline{FLT}$ pin to AVCC. Place a 10pF capacitor from $\overline{FLT}$ to GND for SET mitigation.
4	RDU	1	Dead time delay control for the high-side turn-on. A 1.3kΩ-10kΩ resistor to SGND sets the rising edge delay of Upper Gate High (UGH) to the falling edge of Lower Gate Low (LGL) in the range of 6.5ns to 50ns.
5	RDL	1	Dead time delay control for low-side turn-on. A 1.3kΩ-10kΩ resistor to SGND sets the rising edge delay of Lower Gate High (LGH) to the falling edge of Upper Gate Low (UGL) in the range of 6.5ns-50ns.

Pin Number	Pin Name	ESD Circuit	Description
6	AVCC	1	The output of the internal 5V LDO regulator for chip bias. Input is VDD. A minimum of 1µF ceramic decoupling capacitor is necessary on AVCC to SGND.
7	VDD	2	Input supply to chip. Recommended bias range is 4.75V to 18V.
8	FB	1	PVCC LDO error amplifier inverting input. A resistor divider network from FB to PVCC and SGND sets the PVCC LDO output voltage. If FB is connected to PVCC, PVCC output voltage is 4.5V.
9	PVCC	1	Output of the LDO for the gate drive voltage. Recommended PVCC range is 4.5V to 5.5V. A minimum 1µF ceramic decoupling capacitor is necessary on PVCC to PGND.
10	PGND	-	Low-side driver output reference pin. For typical applications, connect PGND to ground plane and SGND (PAD). Alternatively, connect PGND directly to the low-side transistor's source terminal.
11	LGL	5	Low-side sink driver for gate turn-off. Connect this pin to LGH and the GaN FET gate.
12	LGH	4	Low-side source driver for gate turn-on. Connect this pin to LGL and the GaN FET gate.
13	PHS	3	High-side GaN FET source reference. Connect to the phase switching node of the half-bridge.
14	UGL	7	High-side sink driver for gate turn-off. Connect this pin to UGH and the GaN FET gate.
15	UGH	6	High-side source driver for gate turn-on. Connect this pin to UGL and the GaN FET gate.
16	BOOT	3	High-side bootstrap bias pin. Connect a bootstrap capacitor from this pin to PHS. An internal bootstrap switch connects PVCC to BOOT when PWM = 0V and PHS voltage is within 250mV of PGND.
PAD	SGND	-	Analog signal GND and package bottom thermal pad. The die substrate is electrically connected to PAD. Connect to the ground plane.
LID	SGND	-	The package lid is internally connected to the four bottom pads, die substrate and SGND.



Circuit 1



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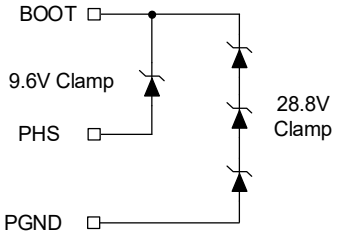
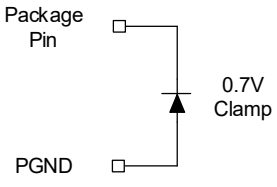


Circuit 3



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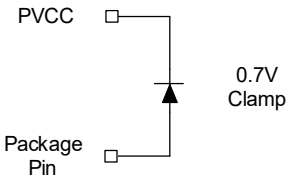

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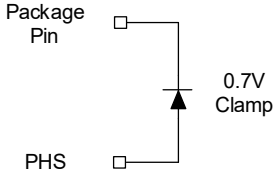
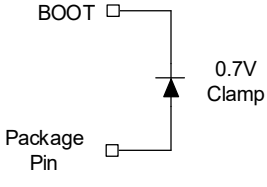


Circuit 6



Circuit 7

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVCC to PGND; BOOT to PHS	-0.3	+6.5	V
VDD to SGND	-0.3	+20	V
SGND to PGND	-0.3	+0.3	V
PHS to PGND	-0.3V DC	+20	V
PHS to PGND[1]	-	+16.5	V
PHS to PGND[2]	-	+13.5	V
PHS to PGND (repetitive transient)	-5V (100ns)	-	V
BOOT to PGND	-0.3	+24	V
BOOT to PGND[1]	-	+21.5	V
BOOT to PGND[2]	-	+18.5	V
EN to SGND	-0.3	VDD+0.3	V
AVCC, FB, PWM, $\overline{FLT}$, RDU, RDL to SGND	-0.3	+6.5	V
UGH, UGL	PHS-0.3	BOOT+0.3	V
LGH, LGL	GND-0.3	PVCC+0.3	V
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	5	kV
Charged Device Model (Tested per JS-002-2018)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

1. Tested in a heavy ion environment at LET = 67MeV•cm^2/mg at 125°C.
2. Tested in a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C.

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	16 Pad CLCC Package	θ_{JA}[1]	Junction to air.	37	°C/W
		θ_{JC}[2]	Junction to case.	6.5	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temp location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-55	+125	°C
VDD Voltage	+4.75	+13.2	V
PVCC	+4.5	+5.5	V
PHS	0	+13.2	V

3.4 Electrical Specifications

3.4.1 DC Electrical Specifications

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
VDD Power Supply							
Shutdown Supply Current	IDD_{SHDN}	EN = 0V	-55 to +125°C	-	850	**1200**	µA
Quiescent Supply Current	I_{DDQ}	PWM = Float; RDU = RDL = 1.3kΩ	-55 to +125°C	-	9	-	mA
		PWM = Float; RDU = RDL = 10kΩ		-	-	**6**	
Unloaded Operating Current	I_{DDO1}	UG and LG unloaded; PWM = 500kHz at 50% 0V to 5V	-55 to +125°C	-	21	**32**	mA
Loaded Operating Current	I_{DDO2}	5nF load on UG; 10nF load on LG; PWM = 500kHz at 50% 0V to 5V	-55 to +125°C	-	55	**70**	mA
Bootstrap Supply							
BOOT Quiescent Current	I_{Q_Boot}	PWM = Float; BOOT-PHS = 4.5V	-55 to +125°C	-	580	**650**	µA
PVCC and AVCC LDOs							
PVCC Feedback Voltage	VFB	Internal reference voltage	-55°C	1.188	1.2	1.212	V
			+25°C	1.188	1.2	1.212	
			+125°C	1.188	1.2	1.212	
			+25°C (Post Rad)	1.188	1.2	1.212	

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
PVCC Gate Drive Voltage	PVCC	PVCC = 4.5V = FB or with external resistors; I_{OUT} from 0mA to 150mA; VDD from 4.85V to 13.2V	-55°C	4.39	4.5	4.6	V
			+25°C	4.4	4.5	4.6	
			+125°C	4.39	4.5	4.6	
			+25°C (Post Rad)	4.39	4.5	4.6	
		PVCC = 5.5V with external FB resistors; I_{OUT} from 0mA to 150mA; VDD from 5.85V to 13.2V	-55°C	5.39	5.5	5.6	V
			+25°C	5.4	5.5	5.6	
			+125°C	5.39	5.5	5.6	
			+25°C (Post Rad)	5.39	5.5	5.6	
PVCC in Pass Mode	-	VDD = 4.75V; FB = PVCC; I_{OUT} = 150mA	-55 to +125°C	**4.34**	4.44	-	V
PVCC Dropout Voltage	-	I_{OUT} = 150mA; VDD voltage where PVCC drops 2% below regulation; PVCC = 4.5V to 5.5V	-55 to +125°C	-	190	**250**	mV
PVCC Output Current Limit	I_{LIMITP}	VDD = 4.75V; FB = PVCC; Force PVCC = 4.2V	-55 to +125°C	**190**	250	**350**	mA
VDD to PVCC Power Supply Rejection Ratio	$PVCC_{PSRR}$	VDD = 6V + 300mVpp AC 1kHz; PVCC = 5.5V; PVCC I_{OUT} = 150mA	-	-	70	-	dB
		VDD = 6V + 300mVpp AC 100kHz; PVCC = 5.5V; PVCC I_{OUT} = 150mA	-	-	30	-	
Internal LDO voltage	AVCC	VDD = 4.97V; I_{OUT} = 20mA	-55 to +125°C	**4.3**	4.6	**4.69**	V
		VDD = 5.25V to 13.2V; I_{OUT} = 0mA to 20mA		**4.7**	5.0	**5.4**	
Dropout Voltage	-	I_{OUT} = 20mA; VDD voltage where AVCC drops 2% below regulation	-55 to +125°C	-	-	**250**	mV
AVCC Output Current Limit	I_{LIMITA}	VDD = 4.75V; Force AVDD = 4.5V	-55 to +125°C	**25**	49	**100**	mA
VDD to AVCC Power Supply Rejection Ratio	$AVCC_{PSRR}$	VDD = 6V + 300mVpp AC 1kHz; AVCC = 5V; AVCC I_{OUT} = 20mA	-	-	70	-	dB
		VDD = 6V + 300mVpp AC 100kHz; AVCC = 5V; AVCC I_{OUT} = 20mA	-	-	30	-	
VDD Undervoltage Lockout (UVLO)							
VDD UVLO Rising Threshold	VR_{VDD}	-	-55 to +125°C	**4.46**	4.6	**4.74**	V
VDD UVLO Falling Threshold	VF_{VDD}	-		**4.41**	4.55	**4.68**	V
VDD UVLO Hysteresis	VH_{VDD}	VR_{VDD} - VF_{VDD}		**25**	50	**90**	mV

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
AVCC Undervoltage Lockout (UVLO)							
AVCC UVLO Rising Threshold	VR_{AVCC}	Test by recovering AVCC from constant current limit	-55 to +125°C	**4.46**	4.6	**4.74**	V
AVCC UVLO Falling Threshold	VF_{AVCC}	Test by putting AVCC into constant current limit		**4.28**	4.41	**4.52**	V
AVCC UVLO Hysteresis	VH_{AVCC}	VR_{AVCC} - VF_{AVCC}		**150**	183	**300**	mV
PVCC Undervoltage Lockout (UVLO)							
PVCC UVLO Rising Threshold	VR_{PVCC}	PVCC = 5.5V with FB resistors[3]	-55 to +125°C	**5.21**	5.34	**5.45**	V
PVCC UVLO Falling Threshold	VF_{PVCC}	PVCC = 5.5V with FB resistors[3]		**5.07**	5.17	**5.27**	V
PVCC UVLO Hysteresis	VH_{PVCC}	VR_{PVCC} - VF_{PVCC}		**100**	150	**300**	mV
BOOT Undervoltage Lockout (UVLO)							
BOOT UVLO Rising Threshold	VR_{BOOT}	-	-55 to +125°C	**3.8**	4.0	**4.2**	V
BOOT UVLO Falling Threshold	VF_{BOOT}	-		**3.6**	3.8	**4.0**	V
BOOT UVLO Hysteresis	VH_{BOOT}	VR_{BOOT} - VF_{BOOT}		**100**	240	**400**	mV
PWM and EN Input Pins							
EN High Level Threshold	VIH_{EN}	PWM = 0V	-55 to +125°C	-	1.8	**2.0**	V
EN Low Level Threshold	VIL_{EN}	PWM = 0V		**1.0**	1.5	-	V
EN Input Hysteresis	$VHYS_{EN}$	VIH_{EN} - VIL_{EN}		**100**	325	**400**	mV
PWM High Threshold	V_{PWMH}	VDD = 4.75V to 13.2V	-55 to +125°C	-	2.7	**2.8**	V
PWM Middle Level Range	V_{PWMM}	VDD = 4.75V to 13.2V		**1.45**	-	**2.4**	V
PWM Low Threshold	V_{PWML}	VDD = 4.75V to 13.2V		**0.95**	1.1	-	V
Mid-High Level Hysteresis	-	VDD = 4.75V to 13.2V		-	100	**200**	mV
Mid-Low Level Hysteresis	-	VDD = 4.75V to 13.2V		-	200	**350**	mV
PWM High Input Current	I_{PWMH}	PWM = 5V		**10**	33	**50**	µA
PWM Low Input Current	I_{PWML}	PWM = 0V		**-50**	-22	**-10**	µA
PWM Pin Pull-Up Resistor	R_{PWMU}	-		**150**	225	**300**	kΩ
PWM Pin Pull-Down Resistor	R_{PWML}	-		**100**	150	**200**	kΩ
PWM Pin Floating Voltage	V_{FLOAT}	-		**1.90**	2.0	**2.135**	V

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
Bootstrap FET Switch							
Low Current Voltage	V_{SWL}	100µA through switch	-55 to +125°C	-	1	**1.6**	mV
High Current Voltage	V_{SWH}	100mA through switch		-	-	**145**	mV
BOOT Switch Resistance	R_{SW}	100mA through switch		-	-	**1.45**	Ω
Positive Window Detect Rising Threshold	-	PWM = 0V		**160**	250	**400**	mV
Positive Window Detect Falling Threshold	-	PWM = 0V		**140**	220	**380**	mV
Negative Window Detect Rising Threshold	-	PWM = 0V		**-380**	-210	**-140**	mV
Negative Window Detect Falling Threshold	-	PWM = 0V		**-400**	-240	**-160**	mV
Positive Window Detect Hysteresis	-	PWM = 0V		**10**	25	**60**	mV
Negative Window Detect Hysteresis	-	PWM = 0V		**10**	20	**60**	mV
$\overline{FLT}$ Open Drain with Internal Detect							
Input High Leakage Current	I_{LEAK}	$\overline{FLT}$ = AVCC; VDD = 13.2V EN = VDD; No fault condition	-55 to +125°C	**-1**	-	**1**	µA
$\overline{FLT}$ Output Low Drive	V_{OL}	I_{SINK} = 10mA; EN = 0V		**-**	0.18	**0.4**	V
Fault Detect Input High Threshold	V_{IH}	VDD = 13.2V; EN = VDD		**2.0**	2.4	**2.8**	V
Fault Detect Input Low Threshold	V_{IL}	VDD = 13.2V; EN = VDD		**1.0**	1.6	**2.0**	V
Upper Gate High Output (UGH)							
UGH Peak Source Current	$IUGH_{SRC}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 5V; 470nF load on UG-PHS	-	-	2	-	A
UGH Output High Voltage	VOH_{UGH}	I_{SOURCE} = 100mA; Voltage drop below BOOT	-55 to +125°C	-	90	**130**	mV
Lower Gate High Output (LGH)							
LGH Peak Source Current	$ILGH_{SRC}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 0V; 1µF load on LG-PGND	-	-	4	-	A
LGH Output High Voltage	VOH_{LGH}	I_{SOURCE} = 100mA; Voltage drop below PVCC	-55 to +125°C	-	56	**90**	mV
Upper Gate Low Output (UGL)							
UGL Peak Sink Current	$IUGL_{SNK}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 0V; 470nF load on UG-PHS	-	-	4	-	A

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
UGL Output Low Voltage	VOL_{UGL}	I_{SINK} = 100mA; Voltage above PHS	-55 to +125°C		50	**80**	mV
UGL Gate Discharge Resistor	RUGL	EN = 0		**800**	1000	**1400**	Ω
Lower Gate Low Output (LGL)							
LGL Peak Sink Current	$ILGL_{SNK}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 5V; 1µF load on LG-PGND	-	-	8	-	A
LGL Output Low Voltage	VOL_{LGL}	I_{SINK} = 100mA; Voltage above GND	-55 to +125°C	-	27	**50**	mV
LGL Gate Discharge Resistor	RLGL	EN = 0		**400**	500	**700**	Ω
Over-Temperature Protection (OTP)							
Rising Thermal Shutdown	OTPR	-	-	-	160	-	°C
Falling Thermal Recovery	OTPF	-	-	-	145	-	°C
Driver Response Time to Thermal Shutdown	-	Design simulation	-	-	45	-	µs

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, +125°C and at +25°C post radiation.
2. Typical values are not guaranteed.
3. UVLO for PVCC is detected on the FB pin. PVCC UVLO thresholds are set at 96.5% rising and 94% falling, typical at +25°C, of the set PVCC voltage. PVCC UVLO thresholds production tested only at PVCC set to 5.5V.

3.4.2 AC Electrical Specifications

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from T_A= -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
Dead Time Delay; RDU and RDL							
Dead Time Delay LG falling to UG rising	t_{DTLU}	VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 1.3kΩ to GND	-55 to +125°C	-	6.5	-	ns
		VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND		**40**	50	**55**	
Dead Time Delay UG falling to LG rising	t_{DTUL}	VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 1.3kΩ to GND		-	6.5	-	ns
		VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND		**40**	50	**55**	
Dead Time Delay Match t_{DTLU} - t_{DTUL}	t_{DTM}	VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 1.3kΩ to GND		-	-0.2	-	ns
		VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND		**-3.5**	-	**3.5**	
PWM Propagation Delay							
UG Turn-Off Propagation Delay PWM Falling to UG Falling	t_{PDUG}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V	-55°C	**20**	27	**32**	ns
			+25°C	**23**	29	**35**	
			+125°C	**27**	33	**39**	
			+25°C (Post Rad)	**20**	29	**39**	
LG Turn-Off Propagation Delay PWM Rising to LG Falling	t_{PDLG}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V	-55°C	**20**	27	**32**	ns
			+25°C	**23**	29	**35**	
			+125°C	**27**	33	**39**	
			+25°C (Post Rad)	**20**	29	**39**	
Propagation Delay Match t_{PDUG} - t_{PDLG}	t_{PDM}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V Over-Temperature and Radiation	-55 to +125°C	**-2.5**	0	**2.5**	ns

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from T_A= -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
PWM Enter Mid-Level to UG Low Delay Time	t_{PDUG1}	PWM [High to Mid] to UG Falling; RDU= RDL = 1.3kΩ	-55 to +125°C	-	80	-	ns
PWM Exit Mid-Level to UG High Delay Time	t_{PDUG2}	PWM [Mid to High] to UG Rising; RDU = RDL = 1.3kΩ		-	65	-	ns
PWM Enter Mid-Level to LG Low Delay Time	t_{PDLG1}	PWM [Low to Mid] to LG Falling; RDU= RDL = 1.3kΩ		-	80	-	ns
PWM Exit Mid-Level to LG Rising Delay Time	t_{PDLG2}	PWM [Mid to Low] to LG Rising; RDU= RDL = 1.3kΩ		-	65	-	ns
UG and LG Transition Times							
UG Rise Time	t_{UGR}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 5nF; 10% to 90%	-55 to +125°C	-	-	**29**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 470nF; 30% to 70%	-55°C	340	470	620	
			+25°C	410	530	680	
			+125°C	480	660	740	
			+25°C (Post Rad)	340	540	740	
UG Fall Time	t_{UGF}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 5nF; 90% to 10%	-55 to +125°C	-	-	**26**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 470nF; 70% to 30%	-55°C	200	260	330	
			+25°C	220	280	360	
			+125°C	260	330	420	
			+25°C (Post Rad)	200	290	420	
LG Rise Time	t_{LGR}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; LG C_{LOAD} = 10nF; 10% to 90%	-55 to +125°C	-	-	**36**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; LG C_{LOAD} = 940nF; 30% to 70%	-55°C	440	550	640	
			+25°C	470	620	800	
			+125°C	600	770	950	
			+25°C (Post Rad)	440	630	950	

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from T_A= -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
LG Fall Time	t_{LGF}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V LG C_{LOAD} = 10nF; 90% to 10%	-55 to +125°C	-	-	**30**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V LG C_{LOAD} = 940nF; 70% to 30%	-55°C	160	240	340	
			+25°C	220	270	380	
			+125°C	260	350	420	
			+25°C (Post Rad)	160	280	420	
Mode Transition Delay							
PVCC Start-Up Delay	-	VDD = 4.75V; PVCC = FB; C_{PVCC} = 1.0µF; EN High to PVCC crossing 0.5V	-	-	115	-	µs
PVCC Start-Up Time	-	VDD = 4.75V; PVCC = FB; C_{PVCC} = 1.0µF; PVCC rise time from 0.45V to 4.05V (10% to 90% of 4.5V)	-	-	15	-	µs
EN High to Driver Output Enabled Delay Time	t_{ENR}	VDD = PVCC = FB = BOOT-PHS = 4.75V	-55 to +125°C	**70**	95	**130**	µs
EN Low to Driver Output Disabled Delay Time	t_{ENF}	EN Low to UG Off; PWM = 5V EN Low to LG Off; PWM = 0V		-	4	**8**	µs
$\overline{FLT}$ Low to LG Output Falling	t_{FLTF}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; EN = VDD; PWM = 0V; $\overline{FLT}$ exercised as an input pin High to Low		-	200	**300**	ns
$\overline{FLT}$ High to LG Output Rising	t_{FLTR}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; EN = VDD; PWM = 0V; $\overline{FLT}$ exercised as an input pin Low to High		-	300	**400**	ns
PVCC Falling Below UVLO to $\overline{FLT}$ Falling Delay	t_{PVCCF}	FB = PVCC	-	-	0.6	-	µs
PVCC Falling Below UVLO to UG Falling Delay		FB = PVCC; PWM = 5V	-	-	0.8	-	µs
PVCC Falling Below UVLO to LG Falling Delay		FB = PVCC; PWM = 0V	-	-	0.5	-	µs

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface specifications apply across the operating temperature range from T_A= -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
PVCC Rising Above UVLO to $\overline{FLT}$ Rising Delay	t_{PVCCR}	FB = PVCC	-	-	0.6	-	µs
PVCC Rising Above UVLO to UG Rising Delay		FB = PVCC; PWM = 5V	-	-	1.0	-	µs
PVCC Rising Above UVLO to LG Rising Delay		FB = PVCC; PWM = 0V	-	-	1.0	-	µs
BOOT Falling Below UVLO to UG Falling Delay	t_{BOOTF}	FB = PVCC; PWM = 5V BOOT-PHS falling 4.5V to 3.5V	-	-	1.5	-	µs
BOOT Rising Above UVLO to UG Rising Delay	t_{BOOTR}	FB = PVCC; PWM = 5V; BOOT-PHS rising 3.5V to 4.5V	-	-	1.8	-	µs

1. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, +125°C and at +25°C post radiation.
2. Typical values are not guaranteed.

Table 1. Burn-In and Operating Life Test Delta Parameters

Parameter	Symbol	Conditions	Delta Limits		Unit
			Min	Max	
VDD Shutdown Current	I_{DD_SHDN}	EN = 0V	-0.12	0.12	mA
VDD Quiescent Current	I_{DDQ_1k}	RDU = RDL = 1kΩ	-1	1	mA
	I_{DDQ_10k}	RDU = RDL = 10kΩ	-0.5	0.5	
BOOT Quiescent Current	I_{BOOTQ}	EN = VDD; PWM = Float; BOOT-PHS = 4.5V	-50	50	µA
PVCC Reference Voltage	V_{FB}	-	-6	6	mV
PVCC Output Voltage	PVCC2	VDD = 4.85V; FB = PVCC	-25	25	mV
	PVCC4	VDD = 13.2V; FB = PVCC	-25	25	mV
PVCC Current Limit	PVCC_I_{LIMIT}	VDD = 4.75V; FB = PVCC	-16	16	mA
PWM High-Level Threshold	V_{PWMH}	VDD = 4.75V; FB = PVCC	-0.28	0.28	V
PWM Mid-Level Upper Threshold	V_{PWMMH}	VDD = 4.75V; FB = PVCC	-0.24	0.24	V
PWM Mid-Level Lower Threshold	V_{PWMML}	VDD = 4.75V; FB = PVCC	-0.145	0.145	V
PWM Low-Level Threshold	V_{PMWL}	VDD = 4.75V; FB = PVCC	-0.095	0.095	V
UG Output High Level	V_{OH_UG}	Source 100mA; Drop below BOOT	-13	13	mV
UG Output Low Level	V_{OL_UG}	Sink 100mA; Rise above PHS	-9	9	mV
LG Output High Level	V_{OH_LG}	Source 100mA; Drop below PVCC	-8	8	mV
LG Output Low Level	V_{OL_LG}	Sink 100mA; Rise above PGND	-5	5	mV

3.5 Timing Diagrams

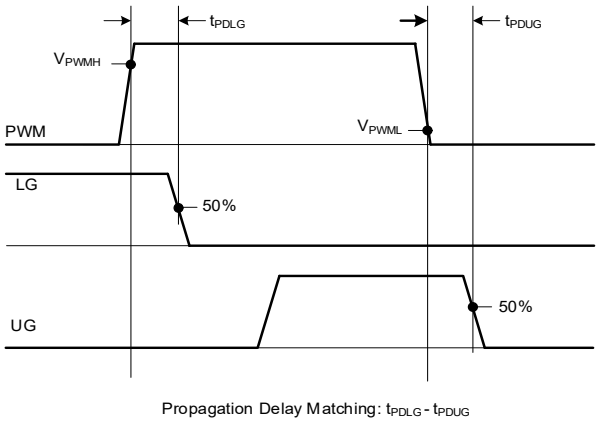


Figure 4. PWM Propagation Delay

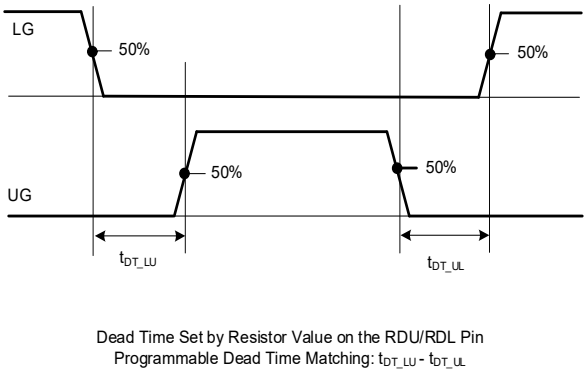


Figure 5. Programmable Dead Time

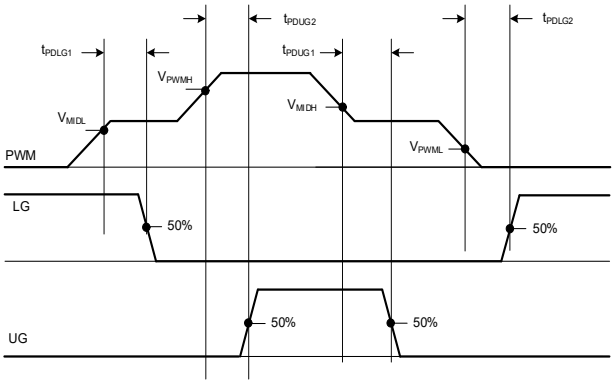


Figure 6. PWM Mid Level Propagation Delay

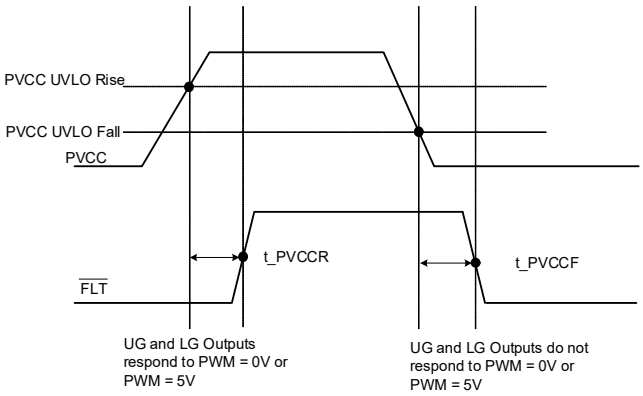


Figure 7. PVCC UVLO to $\overline{FLT}$ Propagation Delay

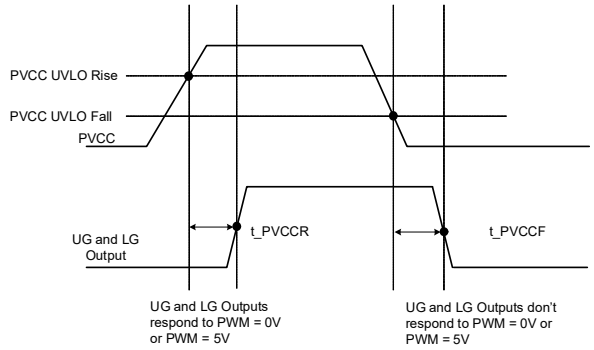


Figure 8. PVCC UVLO to UG & LG Propagation Delay

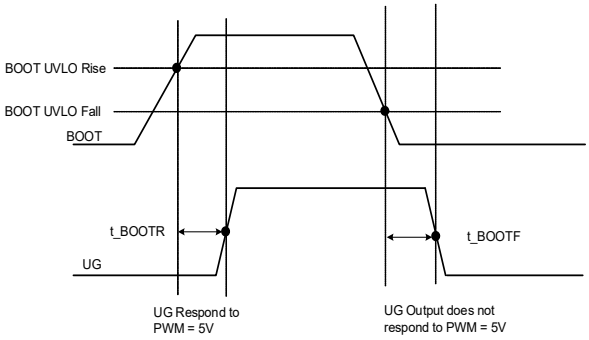


Figure 9. BOOT UVLO to UG Propagation Delay

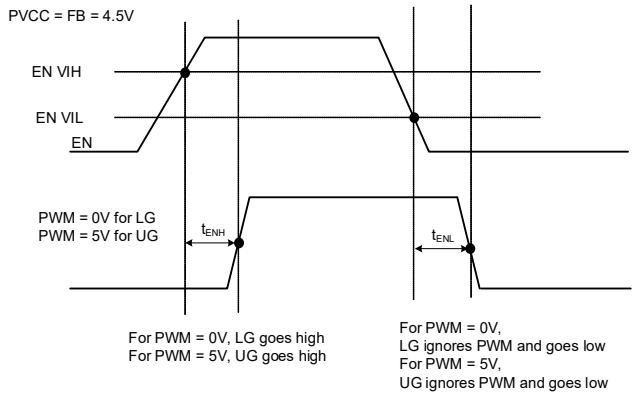


Figure 10. EN Propagation Delay

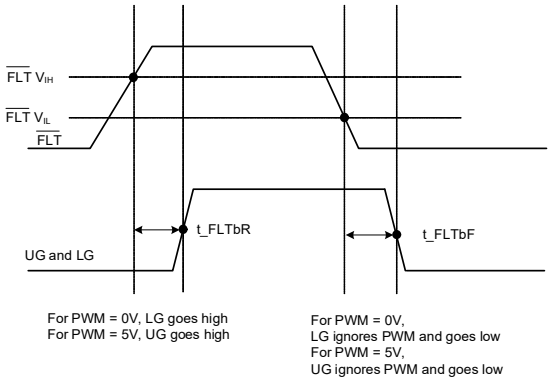


Figure 11. FTLb Propagation Delay (External Driven)

4. Typical Performance Curves

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

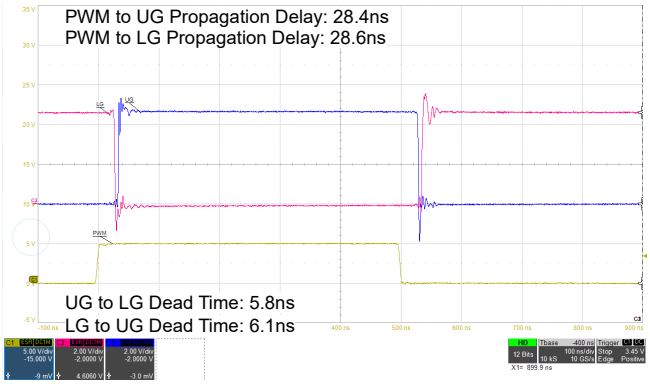


Figure 12. Prop Delay & Dead Time Delay with RDU = RDL = GND or 1.3kΩ

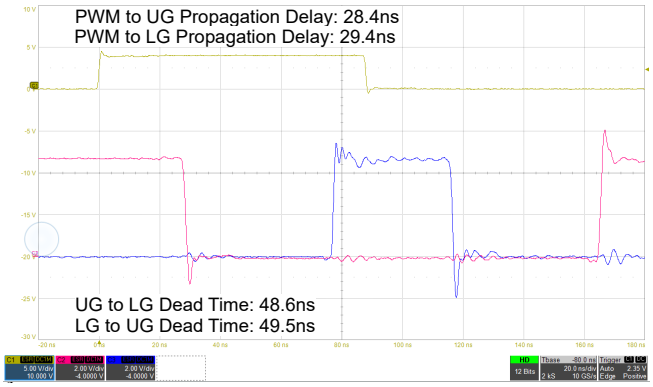


Figure 13. Prop Delay & Dead Time Delay with RDU = RDL = 10kΩ

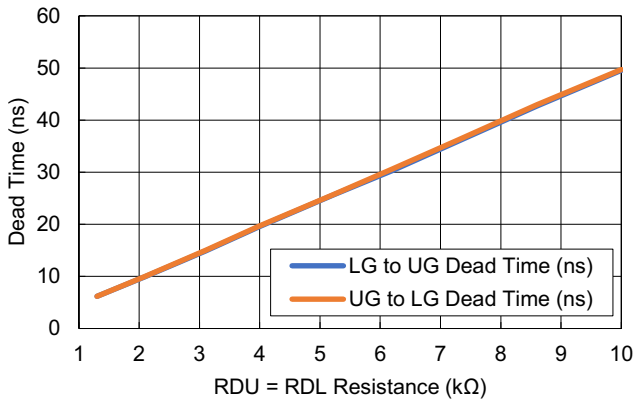


Figure 14. Programmable Dead Time Range 1.3kΩ to 10kΩ

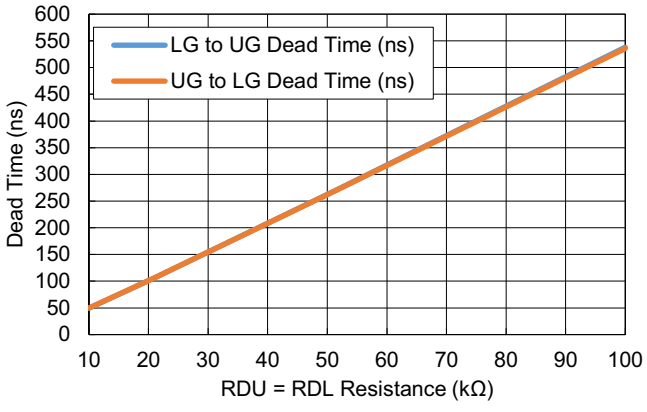


Figure 15. Programmable Dead Time Range 10kΩ to 100kΩ

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

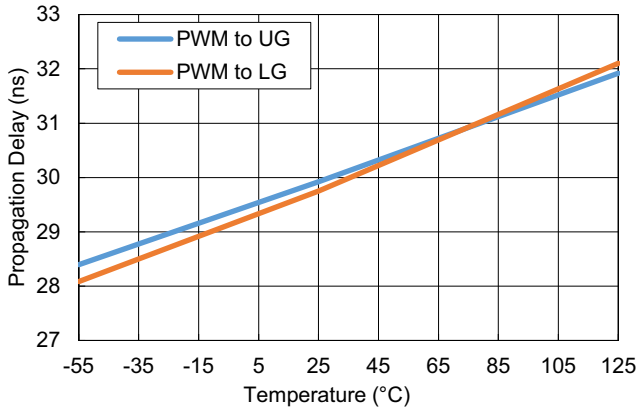


Figure 16. Propagation Delay vs Temperature

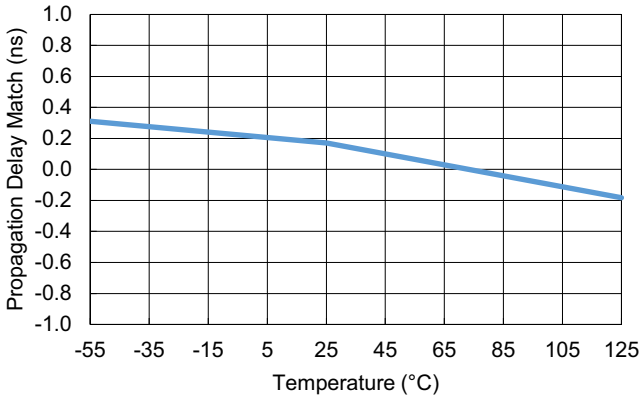


Figure 17. Propagation Delay Matching vs Temperature

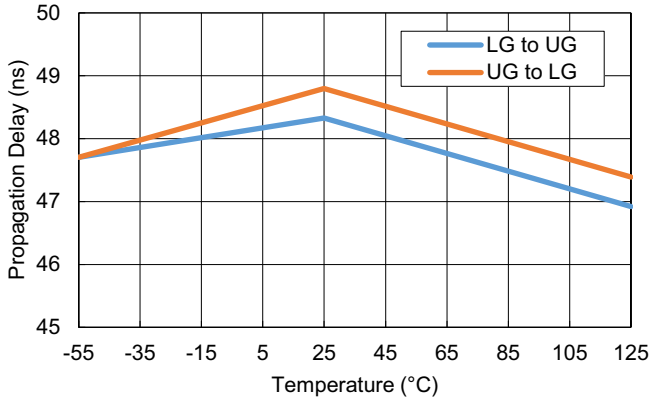


Figure 18. Dead Time Delay vs Temperature; RDU = RDL = 10kΩ

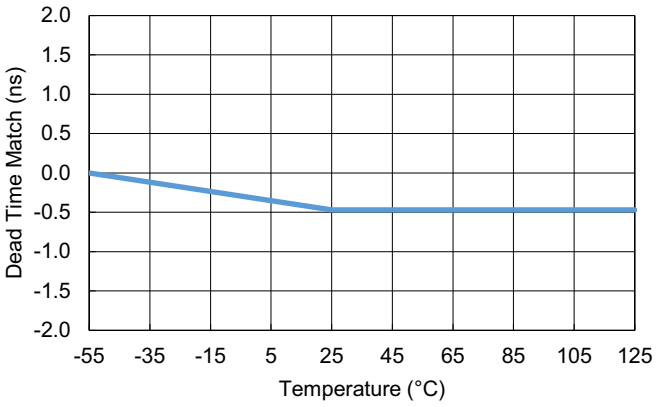


Figure 19. Dead Time Delay Matching vs Temperature; RDU = RDL = 10kΩ

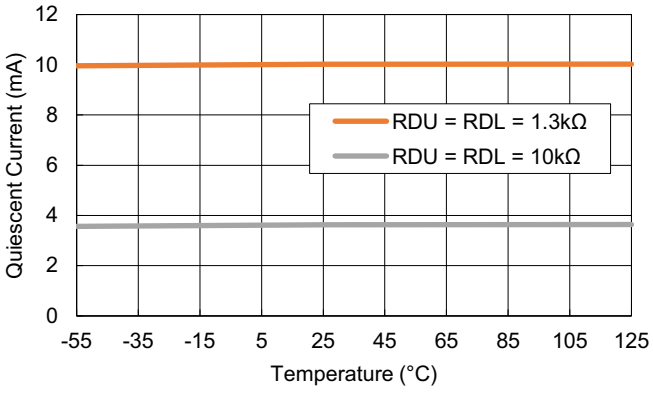


Figure 20. VDD Static Bias Current vs RDU/RDL vs Temperature; Enabled; PWM = Float

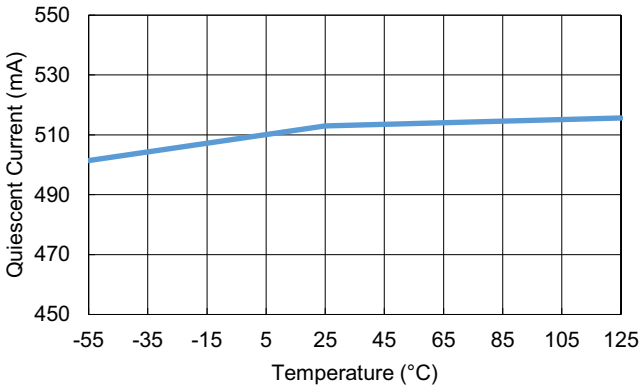


Figure 21. BOOT Static Bias Current vs Temperature; PWM = Float

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

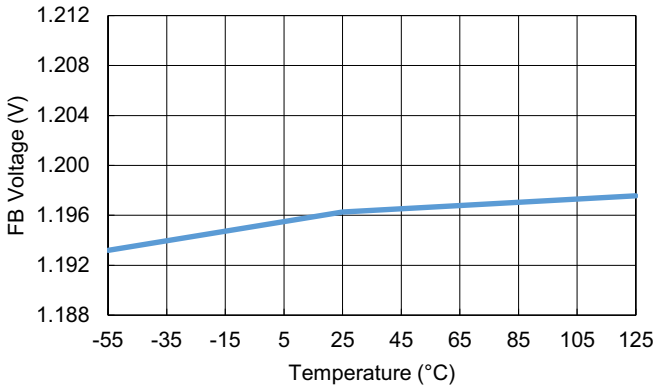


Figure 22. PVCC FB Voltage vs Temperature

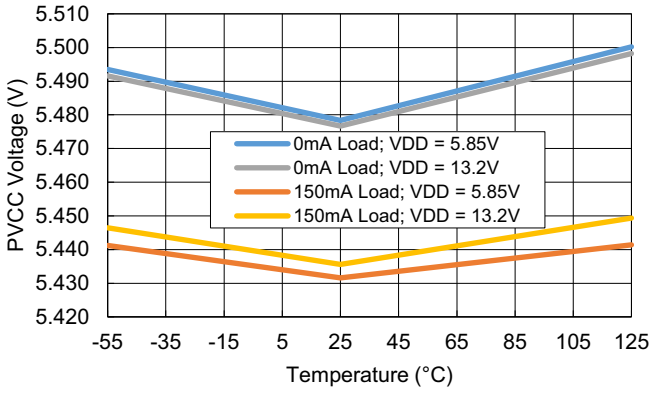


Figure 23. PVCC vs Temperature; PVCC = 5.5V

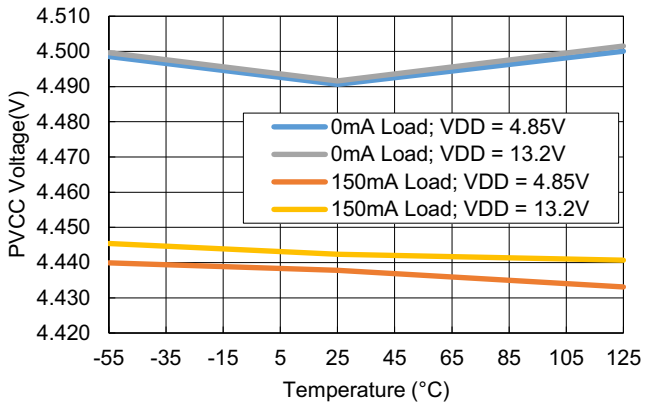


Figure 24. PVCC vs Temperature; PVCC = FB

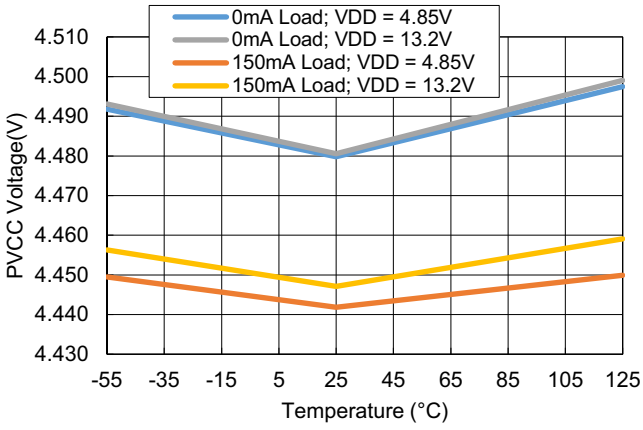


Figure 25. PVCC vs Temperature; PVCC = 4.5V

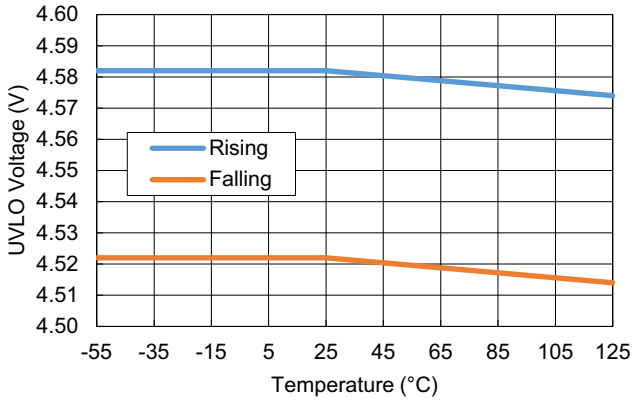


Figure 26. VDD UVLO vs Temperature

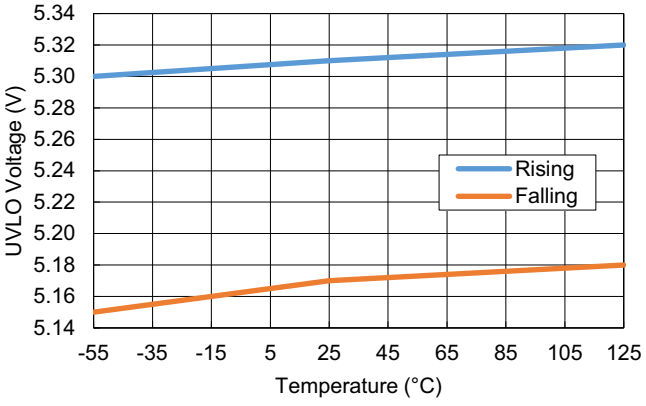


Figure 27. PVCC UVLO vs Temperature

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

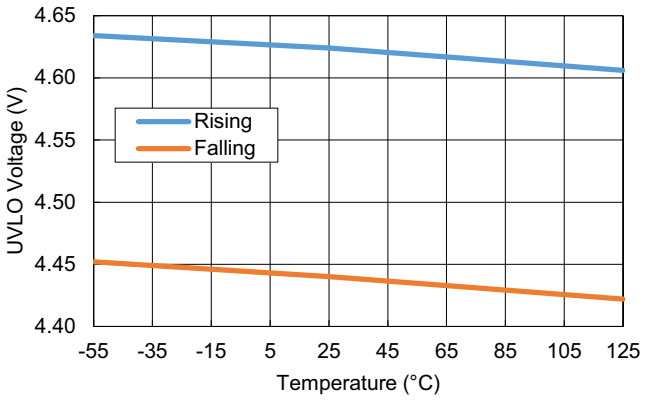


Figure 28. AVCC UVLO vs Temperature

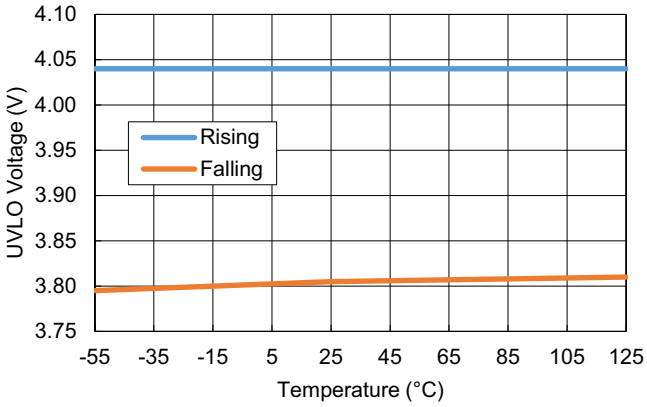


Figure 29. BOOT UVLO vs Temperature

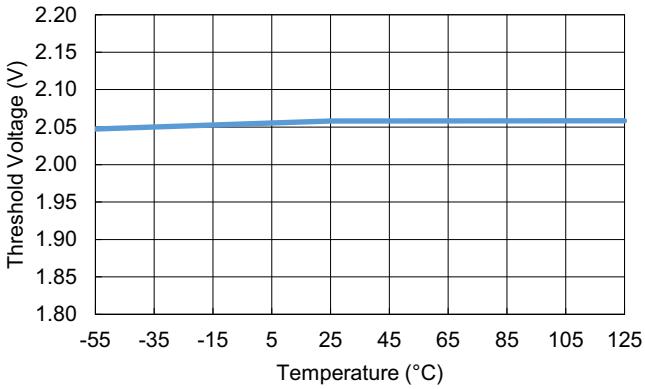


Figure 30. PWM Pin Float Voltage Vs Temperature

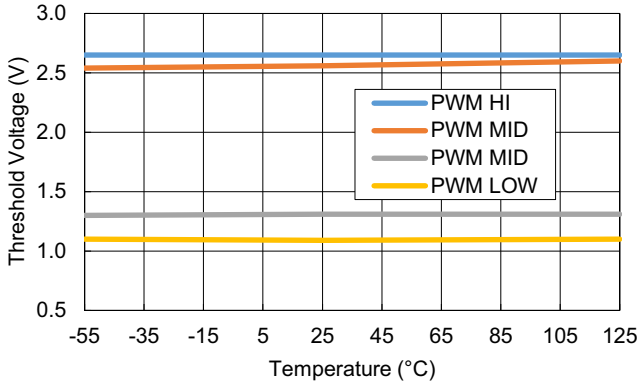


Figure 31. PWM Thresholds vs Temperature

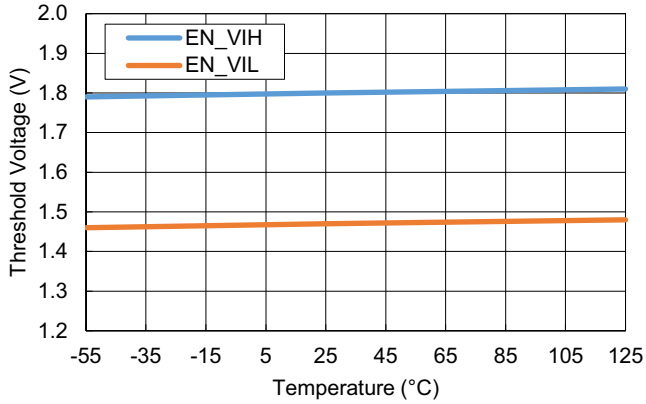


Figure 32. EN Threshold vs Temperature

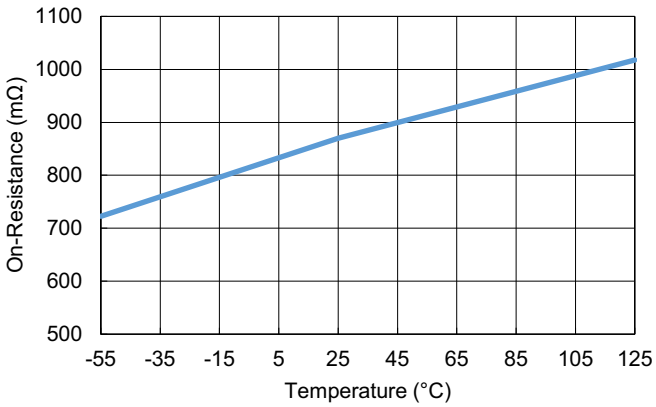


Figure 33. BOOT Switch $r_{DS(ON)}$ vs Temperature

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

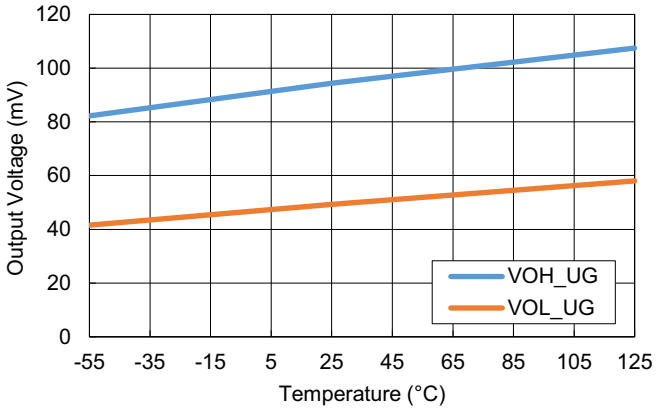


Figure 34. High-Side Driver V_{OL} and V_{OH} vs Temperature; 100mA load

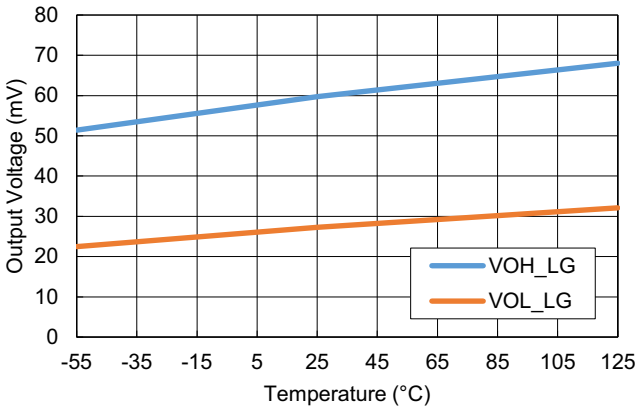


Figure 35. Low-Side Driver V_{OL} and V_{OH} vs Temperature; 100mA load

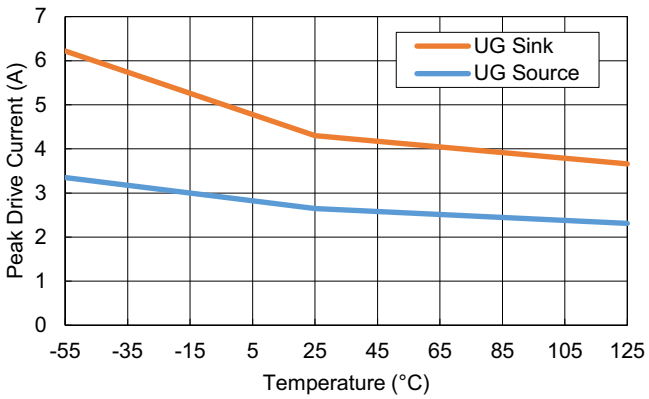


Figure 36. High-Side Driver Peak Source and Sink Current vs Temperature

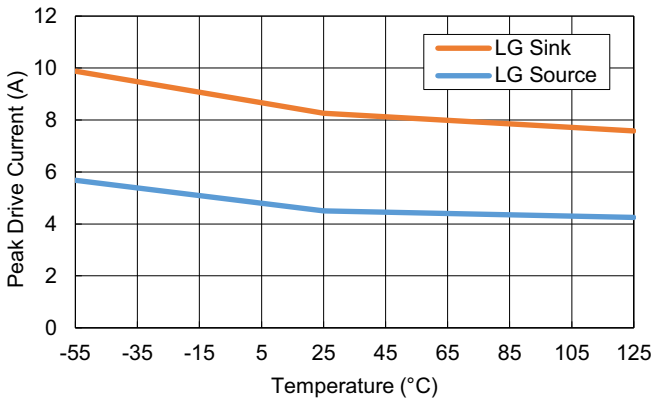


Figure 37. Low-Side Driver Peak Source and Sink Current vs Temperature

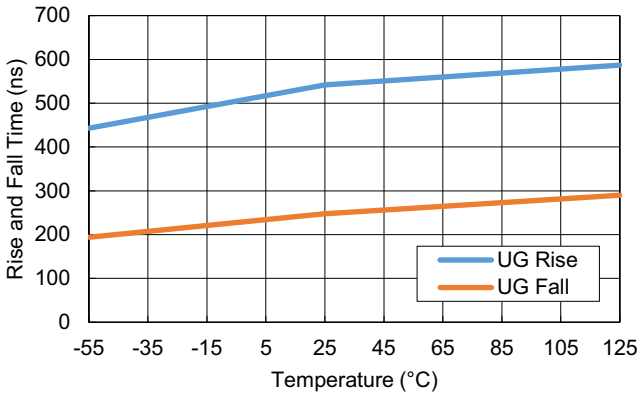


Figure 38. Rise and Fall Times with 470nF on UG and 1000nF on LG vs Temperature; 30% to 70%

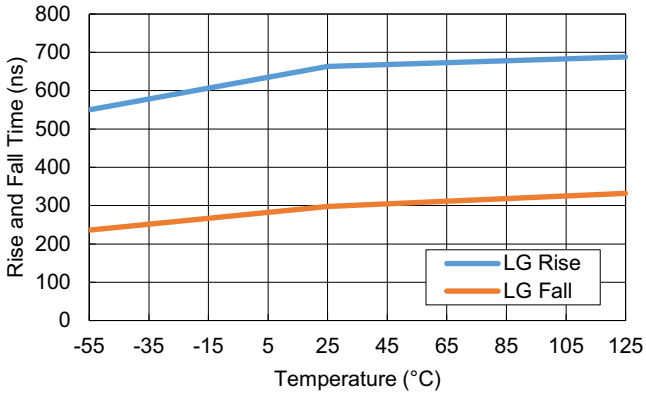


Figure 39. Rise and Fall Times with 470nF on UG and 1000nF on LG vs Temperature; 30% to 70%

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

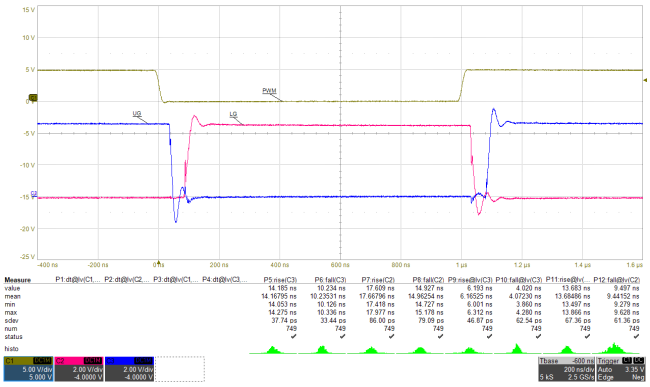


Figure 40. UG and LG Transient Response; 5.1nF on UG and 10nF on LG vs

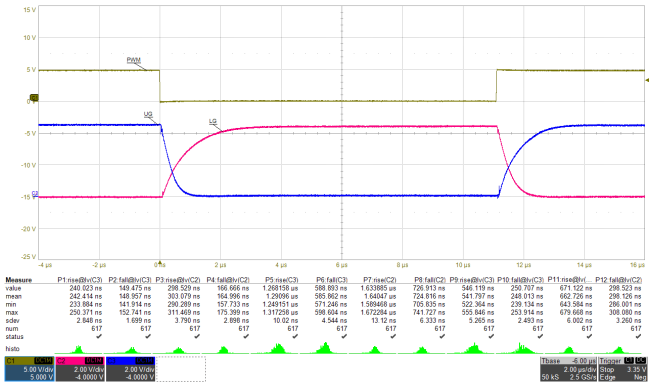


Figure 41. UG and LG Transient Response; 470nF on UG and 1000nF on LG

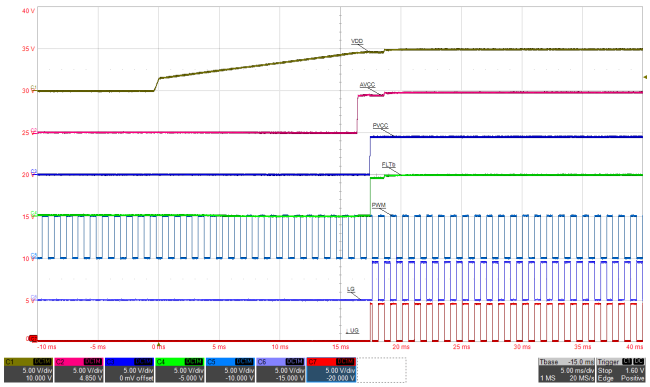


Figure 42. VDD Power-Up Sequence with EN = VDD

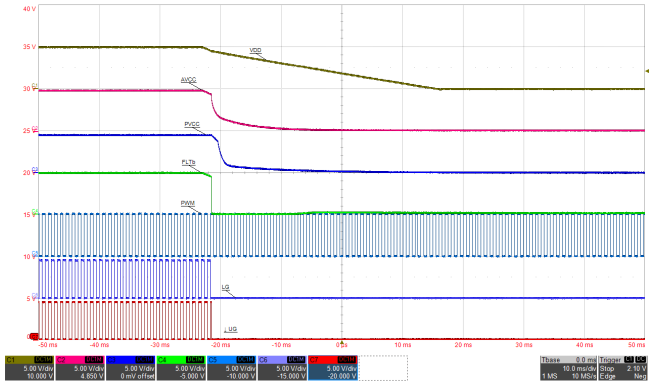


Figure 43. VDD Power-Down Sequence with EN = VDD

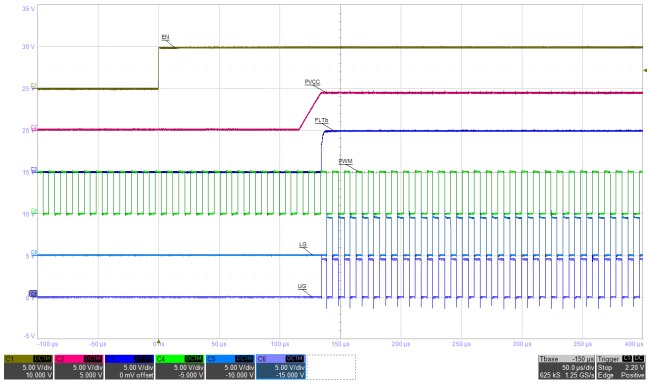


Figure 44. EN Rising Sequence

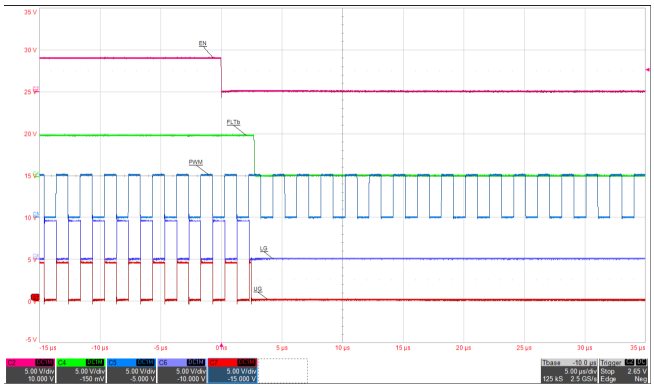


Figure 45. EN Falling Transient Response

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

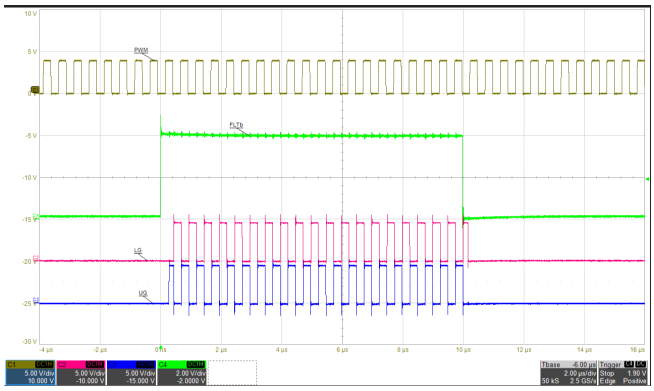


Figure 46. $\overline{FLT}$ Pin Response Time

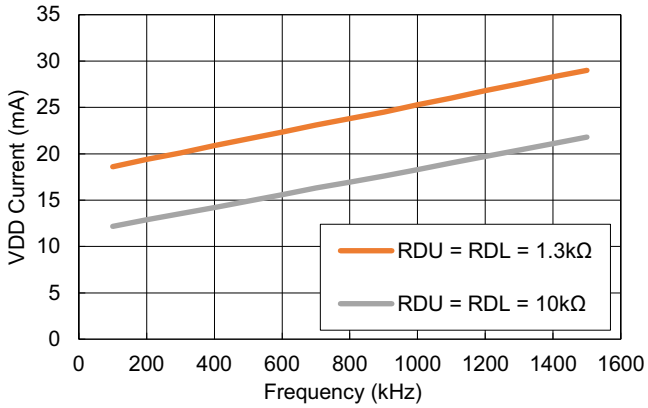


Figure 47. VDD Dynamic Operating Current vs f_{SW}; PVCC = BOOT = 4.5V; PHS = GND; No load on UG and LG

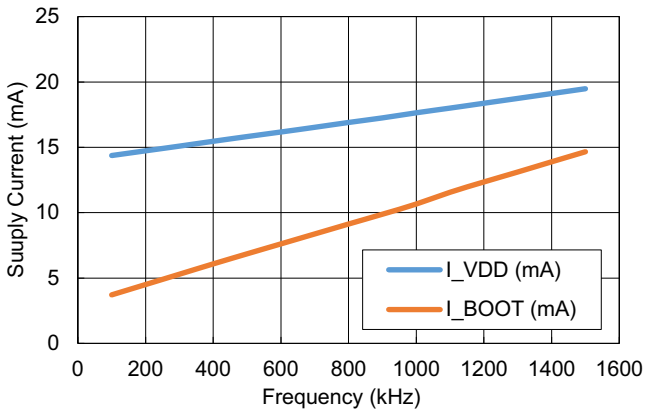


Figure 48. VDD and BOOT Dynamic Operating Current vs f_{SW}; VDD = PHS = 12V; PVCC = BOOT-PHS = 4.5V; No load on UG and LG; RDU = RDL= 0V

5. Functional Description

5.1 Half-Bridge Driver

The ISL73041SEH is a high-frequency 12V Half-bridge driver for enhancement mode N-type GaN FETs or logic level NMOS FETs. High peak drive current and fast propagation delay time with tight matching allow driving low $r_{DS(ON)}$ FETs in high-frequency DC/DC and motor control applications. With an integrated programmable gate drive voltage, high-side level shifter, and bootstrap switch, only a few external components are needed to drive N-type GaN or MOS FETs in a half-bridge configuration.

5.2 GaN/MOS FET Gate Drive Supply

A programmable gate drive supply from 4.5V to 5.5V allows users to optimize the gate voltage for different GaN FETs and logic-level MOSFETs. Renesas GaN FETs recommend a nominal 4.5V gate drive voltage. Other GaN FET vendors can tolerate up to 5.5V. The programmable function allows users to optimize gate drive voltage for low $r_{DS(ON)}$ and GaN FET reliability.

5.3 PWM Input

The PWM pin features a tri-level input for controlling the driver outputs.

- PWM = Low for low-side FET on
- PWM = High for the high-side FET on
- When PWM is at mid-level, both drivers are off.

A PWM input half-bridge driver inherently prevents one type of bridge shoot-through by not allowing the input logic to command both the high-side and low-side drivers simultaneously. The tri-level input allows the half-bridge to be in a high-impedance state during soft-start or hiccup of a PWM controller or for phase dropping in multi-phase regulators. The ISL73041SEH GaN FET Driver is designed to interface with the ISL73847SEH 2-phase PWM Controller.

5.4 Dead Time Control

Because a PWM input driver controls both drivers in a complimentary on/off state, dead time control is needed to prevent shoot-through at the half-bridge FET gates. The ISL73041SEH integrates independent high-side and low-side dead time control on the RDU and RDL pins for delaying the rising edge gate turn-on from the falling edge of gate turn-off. The rising edge dead time delay is programmable from 6.5ns to 50ns with a single resistor on RDU and RDL to ground.

5.5 Driver Output Architecture

The ISL73041SEH half-bridge driver incorporates a 2-stage output for high peak drive currents while minimizing quiescent current. The driver turn-on circuit includes a P-channel transistor and a transient N-channel transistor. When the driver output is low, the N-channel has maximum drive capability to assist in the rise time of the turn-on. As the output reaches near the high level, the N-channel no longer provides drive strength and is only held on by the P-channel. Conversely, the driver turn-off circuit includes an N-channel transistor and a transient P-channel transistor. When the driver output is high, the P-channel has maximum drive capability to assist in the fall time of the turn-off. As the output reaches near the low level, the P-channel no longer provides drive strength and is only held on by the N-channel.

5.6 Integrated BOOT Switch

The ISL73041SEH integrates a boot switch connected between PVCC and BOOT to charge the bootstrap capacitor. A low r_{ON} switch minimizes voltage drop compared to a bootstrap diode while quickly recharging the bootstrap capacitor, which is critical for maintaining the proper V_{gs} gate drive voltage for the high-side GaN FET. The BOOT switch only turns on when the low-side driver is on, and the phase node voltage is between -250mV and +250mV. The ISL73041SEH internally detects the voltage on the PHS pin (connected to the phase node). The purpose of monitoring the PHS pin voltage and requiring the low-side driver to turn on the boot switch is to prevent over-charging the bootstrap capacitor. See Application Information for more information about boot overcharge protection.

6. Application Information

6.1 Power Supply Biasing

ISL73041SEH is biased from the VDD pin and integrates two internal LDOs powered from VDD. The VDD pin bias range is from 4.75V to 18V. A VDD UVLO prevents operation below VDD = 4.75V. Place a 2.2µF or larger ceramic decoupling capacitor near the VDD and SGND pins for input power supply decoupling.

6.2 AVCC LDO

The AVCC LDO is for internal chip biasing. AVCC is internally regulated to 5V nominal. AVCC LDO is enabled when VDD is above the UVLO voltage. The AVCC LDO has an internal overcurrent limiting function. When AVCC LDO crosses the overcurrent limit, the AVCC LDO operates in constant current limit regulation. The current capability on AVCC is 20mA, which includes the current internally consumed by the AVCC pin. When AVCC is below the AVCC UVLO threshold, the $\overline{FLT}$ pin is pulled low to indicate a driver fault condition. Renesas does not recommend using the AVCC LDO for other external biasing; the total current consumption can trigger the constant current limit.

It is necessary to place a 1.0µF or larger decoupling capacitor near the AVCC and SGND pins for stability.

6.3 PVCC LDO

The PVCC LDO is for the low-side gate drive voltage and the high-side bootstrap circuit. PVCC voltage is externally programmable with a resistor divider to the FB pin. The programmable range is from 4.5V to 5.5V. Optionally, FB can be connected directly to PVCC to set PVCC to 4.5V nominal. The PVCC LDO is enabled by EN pin. The PVCC LDO has an internal overcurrent limiting function. When PVCC LDO crosses the overcurrent limit, the PVCC LDO operates in constant current limit regulation. When PVCC is below the UVLO threshold, the $\overline{FLT}$ pin is pulled low to indicate a driver fault condition. The current capability on PVCC is 150mA, which includes the current internally consumed by the PVCC pin. Renesas does not recommend using the PVCC LDO for other external biasing; the total current consumption can trigger the constant current limit.

It is necessary to place a 1.0µF or larger decoupling capacitor near the PVCC and PGND pins for stability. Renesas recommends using a capacitance on PVCC that is 10x larger than the bootstrap capacitor across BOOT-PHS pins.

6.4 Setting PVCC (Gate Drive) Voltage

The voltage on the PVCC LDO to set the gate drive voltage is determined by two resistors connected between PVCC, FB, and SGND. Equation 1 sets the voltage where R_F is connected from PVCC to FB and R_G is connected between FB and SGND.

(EQ. 1) $$PVCC = \left(\frac{R_F}{R_G} + 1\right) \times 1.2V$$

Optionally, short FB to PVCC to set PVCC = 4.5V.

6.5 PVCC and BOOT Undervoltage Lockout (UVLO)

The ISL73041SEH integrates a PVCC UVLO and a BOOT UVLO to prevent undervoltage gate drive to the half-bridge GaN FETs. The PVCC UVLO rising and falling thresholds are relative to the set voltage of PVCC, while the BOOT UVLO is at a fixed threshold.

Under a PVCC UVLO condition, the high-side and low-side driver outputs do not respond to PWM input commands. Under a BOOT UVLO condition, only the high-side driver does not respond to PWM input commands.

6.6 Enable Control

The $\overline{\text{EN}}$ pin controls the start-up of the driver. When EN = 0, the PVCC LDO is disabled. With no PVCC voltage, the $\overline{\text{FLT}}$ pin pulls low to indicate a driver's not-ready condition, and the driver outputs are in a high-impedance state. When EN = 1, the PVCC LDO is enabled, and if no other fault conditions exist, it releases the $\overline{\text{FLT}}$ pin and enables the driver outputs. The delay time between EN logic high and the PVCC LDO start-up is typically 115µs.

The EN pin is VDD voltage compatible and can be tied to VDD for always-enabled applications.

6.7 PWM Operation

Because of the tri-level input thresholds, the PWM pin is designed only for 0V to 5V logic level operation with a high-impedance float or external drive to establish the mid-level. In the high-impedance float state, internal pull-up and pull-down resistors bias the PWM pin at 2V. When PWM is logic high, the high-side driver is on, and the low-side driver is off. When PWM is logic low, the low-side driver is on, and the high-side driver is off. When PWM is at mid-level, both drivers are off.

The PWM operating frequency range is limited on the low end by the boot capacitance on the BOOT to PHS pin to keep the boot circuit biased. As long as sufficient boot bias exists, there is no lower limit on the PWM frequency. The upper PWM frequency is limited by acceptable signal propagation and dead time delays. The typical minimum PWM pulse width for logic high and low to change the driver output state is 20ns.

6.8 Dead Time Control Resistor Setting

The RDU and RDL pins set the rising edge dead time delay for the low-side and high-side drivers. The RDU pin controls UGH rising edge delay respective to the LGL falling edge. The RDL pin controls LGH rising edge delay respective to the UGL falling edge. A resistor to ground on RDU and RDL is required to set the dead time delay. A 1.2V reference voltage on RDU and RDL forces a current through the external resistors. This current is used to program the dead time delay. The dead time delay programmable range is from 6.5ns to 50ns using a 1.3kΩ to 10kΩ resistor. From the Typical Performance Curves Figure 14 and Figure 15, dead times beyond 50ns can be achieved, but the accuracy and dead-time matching performance is not guaranteed per the Electrical Specifications.

Use Equation 2 to calculate the resistor value for a required dead time:

(EQ. 2) $$\text{RDU or RDL}(\text{k}\Omega) = [\text{Dead Time}(\text{ns})]/5.0$$

Although not recommended due to no Electrical Performance testing with using resistance larger than 10kΩ, if using dead time larger than 50ns, use Equation 3 to determine resistor value.

(EQ. 3) $$\text{RDU or RDL}(\text{k}\Omega) = [\text{Dead Time}(\text{ns}) + 6.5]/5.4$$

6.9 Bootstrap Capacitor Design

The high-side bootstrap capacitor provides the bias to the floating high-side circuitry to drive the high-side FET. The bootstrap capacitor recharges to PVCC voltage when the boot switch turns on. Choose the bootstrap capacitor to satisfy two conditions.

- It should be large enough to provide for the high-side driver bias current, the high-side driver DC output current (primarily the 1kΩ resistor on UGL to PHS), the high-side FET gate leakage current, and the instantaneous current to turn on the high-side FET (provide the gate charge) during the high-side on switching period, without discharging the boot voltage significantly.
- It should be small enough such that at initial start-up, the boot-refresh time meets system requirements. The resistance of the boot switch and the bootstrap capacitance determines the initial boot refresh to charge the boot capacitor from 0V to PVCC.

A good starting point is to design for a 5% discharge of the boot voltage during steady-state operation of the high-side drive. To determine the bootstrap capacitor, use Equation 4.

(EQ. 4) $$C_{BOOT} = \frac{Q_{TOT}}{V_{DROP}}$$

where Q_{TOT} is total charge require to operate the high-side driver during high-side on-time. Q_{TOT} includes the following:

- Gate charge for the high-side FET turn-on.
- Charge for the high-side driver boot bias current.
- Charge for the high-side gate-source resistor when driver is sourcing BOOT voltage.
- Charge for the high-side FET gate leakage current.

V_{DROP} is the amount of voltage drop across the boot capacitor. For PVCC = 4.5V: V_{DROP} = 4.5V × 0.05 = 225mV.

The following is a design example of a 12V to 1V DC/DC converter at 500kHz using ISL70023SEH 100V GaN FET as the high-side FET:

- Q_{GS1} = 25nC gate charge
- I_{BOOT} = 600µA; t_{ON} = 1V/12V × 2µs = 167ns; $Q_{BOOT} = I_{BOOT} \times t_{ON}$ = 0.1nC
- For 4.5V gate drive, Q_{GS2} = 4.5V/1kΩ × 167ns = 0.75nC
- ISL70023SEH specifies 9mA gate leakage. Q_{LEAK} = 9mA × 167ns = 1.5nC
- $C_{BOOT} = Q_{TOT}/V_{DROP}$ = 27.4nC / 225mV = 122nF (Use 100nF or 150nF standard value)

This capacitor is the minimum recommended bootstrap capacitor value to meet ripple voltage. Also, it is important to size the capacitor appropriately. During system start-up, the bootstrap capacitor is at 0V. The PWM controller must issue a boot refresh for the high-side driver to clear BOOT UVLO and have sufficient boot bias. Otherwise, the first few high-side commands do not turn on the upper FET, potentially causing system faults. The bootstrap capacitor is charged through PVCC and the internal 1Ω typical boot switch, forming an RC circuit. The boot refresh command from the PWM controller must drive PWM = 0V, and PHS must be within 250mV of PGND to turn on the boot switch and charge the capacitor. The boot refresh command needs to be of long enough duration for the RC circuit to charge above the BOOT UVLO threshold and maintain boot voltage in operation (for example, t = 3×RC would charge the capacitor to 95% of the final voltage). With a 1Ω boot switch impedance and 150nF bootstrap capacitor, this would require a boot refresh time of 450ns.

The ISL73847SEH PWM controller includes a built-in boot refresh command before a soft start-up during initial power-up and recovery from a hiccup. The controller issues 32 pulses of PWM switching between 0V (logic low) and 2V (mid-level). The oscillator of the ISL73847SEH controller sets the boot refresh pulse frequency and has a typical 100ns refresh time (PWM = 0V) to charge the boot capacitor.

6.10 Bootstrap Voltage Overcharge Protection

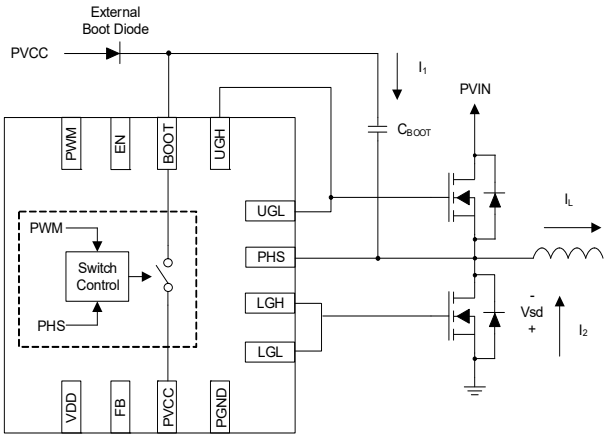
Traditional MOSFET applications drive the gate-source voltage anywhere from 10V-15V while retaining both 1) Low drain-source ON-resistance and 2) reliable operation. GaN FET operation has a much narrower range, usually around 4.5V to 6V, to maintain low ON-resistance and reliable operation.

The ISL73041SEH provides an integrated PVCC LDO to provide bias to the low-side gate driver. The ISL73041SEH also features unique circuitry to prevent overcharging the boot voltage in the bootstrap configuration.

Unlike a MOSFET, there is no body-drain diode in a GaN FET. However, there is still a reverse conduction path from source to drain with zero gate bias. The source-drain voltage is a function of the reverse current and is provided in the GaN FET datasheet as the VSD parameter. During dead time, when both high and low-side GaN FETs are off, the positive current flowing through the inductor is commutated through the low-side FET source-drain channel. The reverse VSD voltage pulls the PHS node of the ISL73041SEH driver below ground. In traditional half-bridge drivers with a boot diode implementation, the boot diode is forward-biased, and the bootstrap capacitor is charged to PVCC + VSD. Depending on the magnitude, this can over-charge the bootstrap capacitor voltage, which provides the upper gate drive voltage.

Important: Operating the GaN FET with higher than recommended gate voltages is unreliable as this can damage the GaN FET. The recommended operating gate voltage for Renesas GaN FETs is 4.5V.

The ISL73041SEH implements bootstrap capacitor overcharge protection by replacing an external boot diode with an internal intelligent boot switch. The boot switch turns on only when PWM = 0V and the PHS voltage is within ±250mV of PGND. This avoids recharging the bootstrap capacitor during dead time, where the PHS voltage can be excessively negative such that it overcharges the bootstrap capacitor. Figure 49 and Figure 50 highlight the bootstrap overcharge protection by replacing the boot diode with a boot switch.



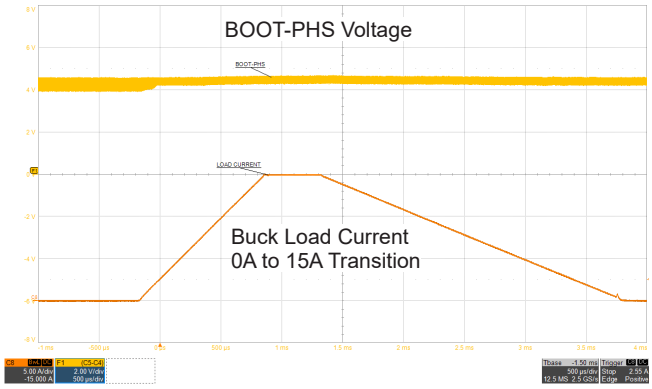


Figure 49. BOOT Switch Only

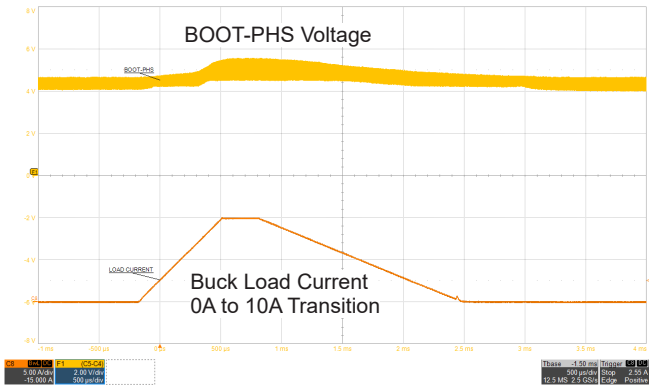


Figure 50. Schottky BOOT Diode Added

6.11 Gate Driver Outputs

The ISL73041SEH features independent source and sink driver outputs for the rise and fall time control. The upper gate driver is the Upper Gate High (UGH) and Upper Gate Low (UGL) pins. The lower gate driver is the Lower Gate High (LGH) and Lower Gate Low (LGL) pin. A series diode is needed on drivers without separate source and sink pins to achieve independent turn-on/off control. This issue can be problematic for GaN FETs as the diode's voltage drop from driver output to the FET gate impacts the FET ON-resistance. If no turn-on or turn-off time reduction is needed, Renesas recommends inserting a 0Ω resistor anyway. In practical layout, the Printed Circuit Board (PCB) trace length connecting the driver output to the FET gate has a parasitic inductance. Combined with the parasitic capacitance of the FET gate, this forms a resonant loop that can cause excessive ringing in the gate drive waveforms during turn-on and turn-off. The ringing overshoot may be large enough to damage a GaN FET gate in a poor layout. A small amount of resistance may be required to dampen the overshoot.

The UGx and LGx output high peak drive currents that turn on and off the FET quickly for high-frequency applications need to minimize switching losses. The high-side driver provides up to 2A source and 4A sink peak drive current. The low-side source and sink driver provides up to 4A source and 8A sink peak drive current.

There is a 1kΩ passive pull-down resistor on UGL to PHS and a 500Ω passive pull-down resistor on LGL to PGND. These passive pull-down resistors prevent charge build-up on the FET gate-source capacitance when the ISL73041SEH driver is not biased. Otherwise, both half-bridge FETs can accumulate enough Vgs from leakage current or stray noise at the capacitive high impedance gate to turn on and cause shoot-through.

In normal operation, driver outputs respond to PWM input commands. Under disabled or fault conditions, the driver outputs do not respond to PWM input, and the driver outputs are in either an active off (the UGL and LGL sink drivers are on) or passive off (1kΩ pull down on UGL to PHS and 500Ω pull down on LGL to PGND) condition. Below is a list of ISL73041SEH states where the driver outputs do not respond to PWM input commands and their associated active or passive states.

Note: A passive off condition supersedes the active off condition.

- EN pin low (driver disabled): Passive Off
- VDD, AVCC or PVCC UVLO: Passive Off
- PWM = Mid level: Active Off
- $\overline{FLT}$ externally driven low: Active Off
- Over-Temperature Fault: Active Off
- BOOT UVLO: Passive off only at the high-side driver. The low-side driver is still active to PWM input commands.

6.12 $\overline{FLT}$ Pin Fault Indication

The ISL73041SEH includes several fault protections to prevent the operation of the half-bridge driver in a faulted condition. The $\overline{FLT}$ pin is an indicator of its fault status. The $\overline{FLT}$ pin is a dual-use open-drain output with external input control. Connect a pull-up resistor from the $\overline{FLT}$ pin to AVCC. The typical value is 10kΩ. $\overline{FLT}$ internally pulls low to indicate a fault condition when one of the following occurs:

- EN = 0 (driver disabled),
- VDD, AVCC or PVCC in UVLO, or
- ISL73041SEH is in an over-temperature fault condition.

Under these fault conditions, the driver outputs do not respond to PWM inputs.

You can also use the ISL73041SEH $\overline{FLT}$ pin for external control input in fault broadcasting applications where all driver $\overline{FLT}$ pins are connected. If one driver or a controller enters a fault condition that pulls its $\overline{FLT}$ pin low, all other ISL73041SEH drivers are disabled to prevent operation when the system detects a fault condition.

For SEE mitigation, Renesas recommends using a 10pF or larger capacitor on the $\overline{FLT}$ pin to SGND. This capacitor prevents false toggling of the $\overline{FLT}$ pin due to SEE transients.

6.13 $\overline{FLT}$ pin Usage with ISL73847SEH and other ISL73041SEH drivers

The ISL73041SEH $\overline{FLT}$ pin works with the ISL73847SEH PWM controller as a system-ready status to initiate soft-start (not in fault) or shutdown (fault encountered) in operation. The ISL73847SEH is a 2-phase controller, so both the $\overline{FLT}$ pin on the ISL73041SEH and the $\overline{FLT}$ pin on the ISL73847SEH are tied with a single pull-up resistor to either the AVCC on ISL73041SEH or VCC on ISL73847SEH.

6.14 $\overline{FLT}$ as Pseudo Enable Pin

The EN pin enables the bandgap before powering up the PVCC LDO and finally enabling the driver outputs. The propagation delay time from the EN rising edge to the driver output's enable is 95µs typical. Alternatively, for faster enable time in applications not using the ISL73847SEH PWM controller, an open-drain NMOS FET can be connected to the $\overline{FLT}$ pin to operate as a faster enable/disable pin. When the gate voltage is logic high, the $\overline{FLT}$ pin is low, and the driver is disabled. When the gate voltage is logic low, the pull-up resistor on the $\overline{FLT}$ pin pulls the $\overline{FLT}$ high. The $\overline{FLT}$ high or low to the driver output's response propagation delay is 100ns typical. When using the $\overline{FLT}$ pin as the driver enable pin, connect EN to VDD.

6.15 Over-Temperature Protection

The ISL73041SEH integrates an Over-Temperature Protection (OTP) circuit. When the junction temperature reaches 160°C typical, the OTP threshold is triggered. In an over-temperature fault condition, the driver stops responding to PWM inputs while the UGL and LGL sink outputs are active to disable the half-bridge. The $\overline{FLT}$ pin pulls low to indicate a fault. The PVCC LDO remains enabled during an over-temperature fault condition. When the junction temperature falls below 145°C typical, the OTP condition clears. The driver automatically resumes normal operation, and the $\overline{FLT}$ pin is released.

6.16 VDD Supply Current

The VDD supply current of ISL73041SEH divides between static bias current and dynamic operating current. The static bias current includes the current needed to bias the dead time delay circuit. The dynamic operating current consists of the operating frequency on PWM, the duty cycle, and the capacitive load of the GaN FET.

The static bias current is approximately:

(EQ. 5) $$I\_VDD\ (static) = 4.5mA + 3 \times \left(\frac{VREF}{RDU}\right) + 3 \times \left(\frac{VREF}{RDL}\right)$$

where VREF = 1.2V; RDU and RDL are the resistors (in kΩ) used for the dead-time delay.

The dynamic operating current is approximately:

(EQ. 6) $$I\_VDD\ (dynamic) = I\_VDD(f_{SW}) + I\_VDD\ (capacitor\ load) + I\_VDD\ (duty\ cycle)$$

The dynamic I_VDD current vs f_{SW} is found in Figure 47.

The dynamic current from the capacitor load is I = C × V × F, where C is the equivalent capacitive load of the GaN FET gate-source capacitance, V is the operating PVCC voltage, and F is the switching frequency (f_{SW}). Determine C by Q_{GS}/V, where Q_{GS} is the total gate charge specified in the GaN FET datasheet. Remember to sum up the low and high sides of GaN FET Q_{GS}.

The dynamic current from the duty cycle is because of the 500Ω pull-down resistor on LGL and 1kΩ resistor on UGL. During one switching cycle, the current through these resistors is Equation 7, where R_1 is 1kΩ, R2 is 500Ω, and D is the duty cycle of the gate drive waveform.

(EQ. 7) $$I\_VDD\ (\text{duty cycle}) = \frac{PVCC}{R_1} \times D + \frac{PVCC}{R_2} \times (1 - D)$$

6.17 Power Dissipation

The power dissipation calculation for the ISL73041SEH half-bridge driver is more complex compared to typical half-bridge drivers where most of the power is dissipated by the dynamic operating current of the driver and in the output driver stage switching the capacitive load of the FET gates. While the dynamic current and output drive dissipation are still significant portions, the ISL73041SEH total power dissipation must also include the two internal LDOs, the current to bias the RDU and RDL dead time circuits, and the internal 1kΩ pull-down resistor on the upper gate driver and the 500Ω pull-down resistor on the lower gate driver as these attributes further increase the power dissipation. Therefore, VDD biasing voltage, PVCC LDO regulated voltage, programmed dead time, and even duty cycle operation become factors in the total power dissipation. Use the spreadsheet calculator tool on the product page to estimate the total power dissipation in the ISL73041SEH driver.

6.18 Dual Complimentary Low-Side GaN FET Driver

The ISL73041SEH can be configured as a dual complementary output low-side driver controlled by the PWM input. Such an application can be used in synchronous low-side drives of transformer-isolated topologies. Connect the PHS pin common to PGND to ground the upper driver. Connect the BOOT pin to the PVCC pin to bypass the boot switch. The upper driver UG is in phase with the PWM input, while the lower driver LG is logically inverted from PWM. The dead time from UG falling to LG rising and LG falling to UG rising is still enforced by the dead time resistors on RDU and RDL in this configuration. Either GaN FET may be omitted in this configuration to use the ISL73041SEH as a single inverting (LG only) or non-inverting (UG only) GaN FET Driver.

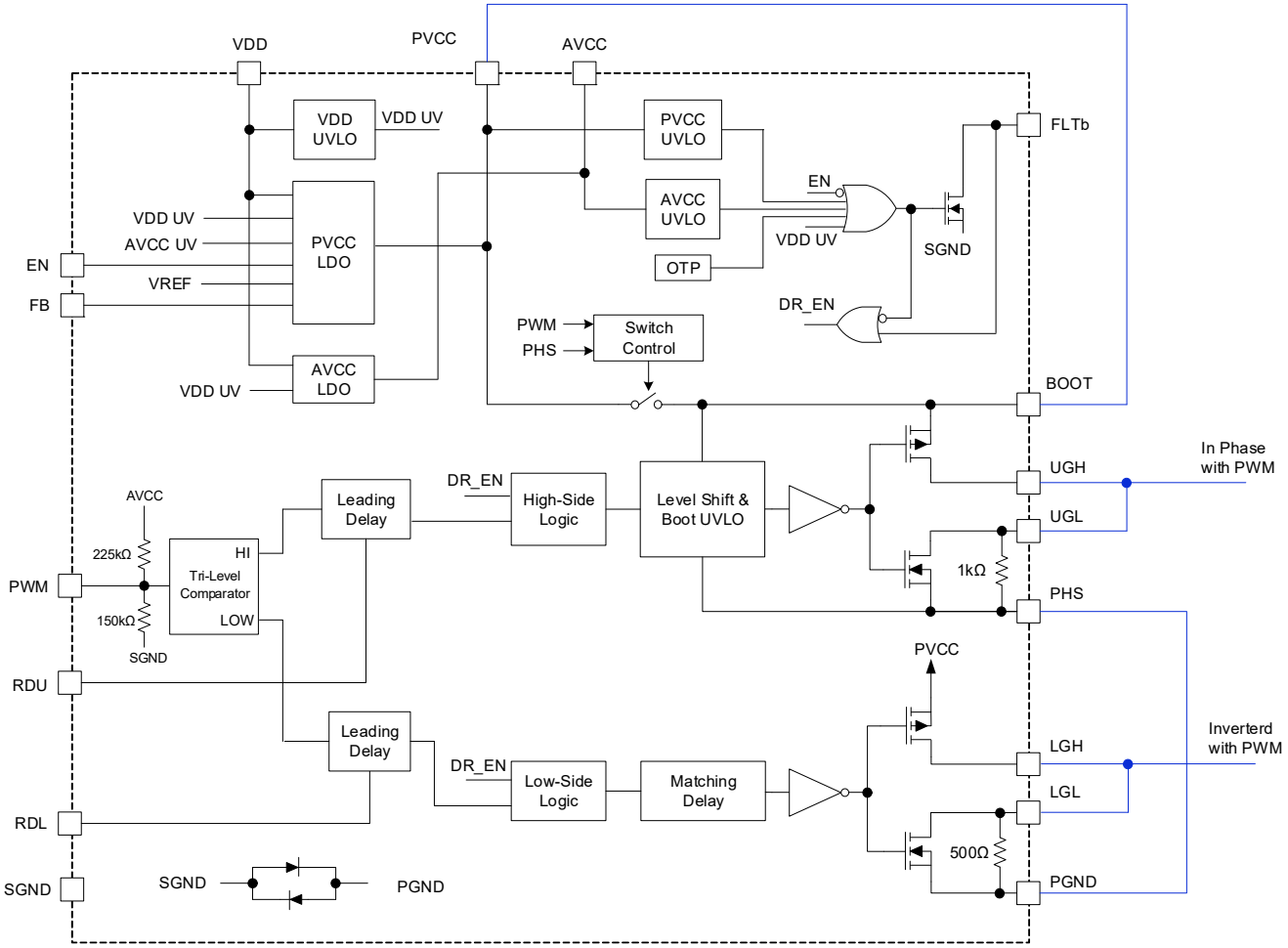


Figure 51. Connection for Dual Low-Side Driver

7. PCB Layout

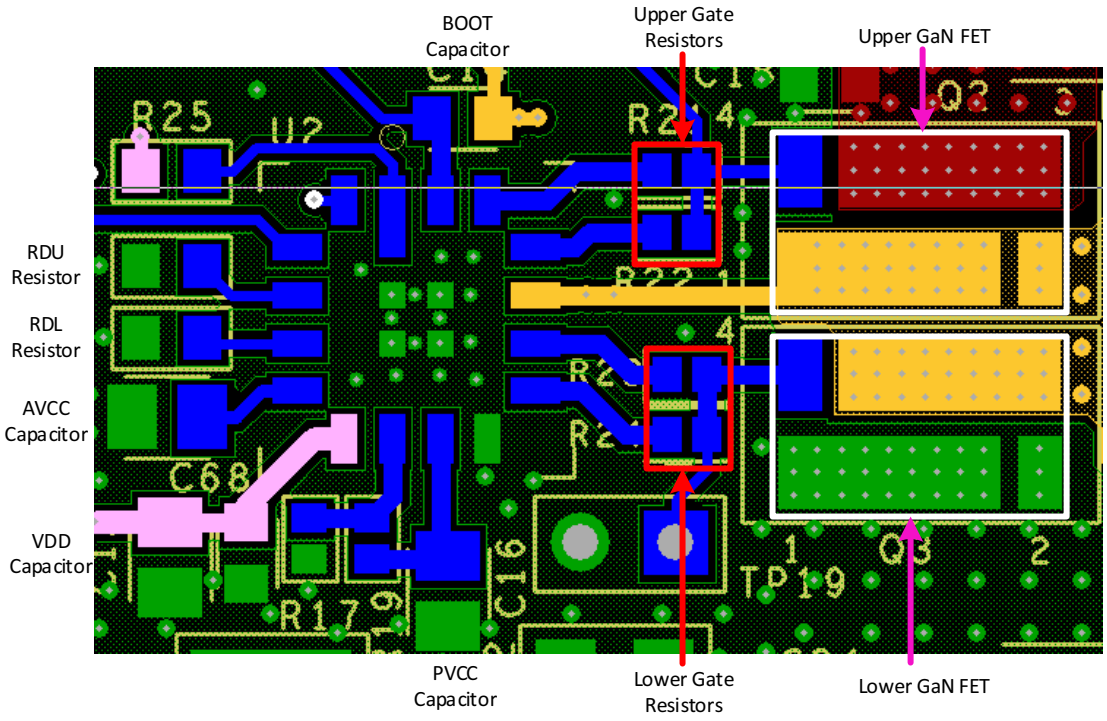
7.1 Layout Guidelines

It is crucial to consider and follow the general printed circuit board layout guidelines to maximize the performance of the ISL73041SEH half-bridge driver and the power GaN FETs it is driving.

- Place low ESR X7R grade or better ceramic capacitors for high-frequency decoupling as close to the package pins as possible. These include the capacitors between VDD-SGND, AVCC-SGND, PVCC-PGND, and BOOT-PHS.
- Place the RDU and RDL dead-time control resistors close to their respective pins and connect them to SGND through the PCB GND plane.
- Connect the four bottom EPAD of the package to the top layer GND plane of the PCB. To further improve thermal performance, place at least four vias in the GND plane under the package EPAD to another internal GND plane to dissipate heat.
- Place the ISL73041SEH close to the half-bridge power GaN FET to minimize trace inductance and high current loop area between the driver output and the GaN FET gate.
- Connect the PGND pin and the low-side FET source commonly through the same PCB ground plane as the SGND PAD. Alternatively, connect the PGND pin to the low-side FET source-sense terminal if it is available. Arrange the components and route the trace to keep this PGND inductance low.

- Route the PHS pin to the switch node of the half-bridge power stage with a short and wide trace to minimize inductance and loop area.
- For the low-side drive, the PVCC capacitor, PVCC and PGND pins, low-side driver gate outputs, low-side FET gate, and GND plane form a current loop during FET turn on and turn off. For the high-side drive, the bootstrap capacitor, the BOOT and PHS pins, the high-side driver gate outputs, the high-side FET gate, and the switch node form a current loop during FET turn-on and turn-off. Keep these loops short and wide, and avoid overlapping with other sensitive signals.
- Size the phase node of the half-bridge (high-side FET source and low-side FET drain) area to handle the current and thermal dissipation from the FETs and switching load. The phase node copper area usually ends up being a significantly large shape. In addition, the phase node is where high voltage and high dv/dt switching occurs. In general, there are two layout practices for handling the phase node. One recommendation is to remove any conductors (including ground) that overlap the phase node on the adjacent layer of the PCB. The other recommendation is to repeat the phase node shape on every layer of the PCB. Both methods minimize the capacitive coupling of noise into the GND plane and prevent any sensitive analog signals from being routed underneath the phase node and causing unintentional common mode noise.

7.2 Layout Example



8. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	2794µm x 2794µm (110 mils x 110 mils) Thickness: 305µm ±25µm (12 mils ±1 mil)
Interface Materials	
Glassivation	Type: Silicon dioxide and silicon nitride Thickness: 18.5kA ±10% dioxide; 6kA ±10% nitride
Top Metalization	Type: Al 99.5%, Cu 0.5% Thickness: 2.85µm ±0.15µm
Backside Finish	Silicon
Process	0.25µm BiCMOS
Assembly Information	
Substrate and Package Lid Potential	Internal connection to the four EPAD (SGND)
Additional Information	
Transistor Count	5737
Weight of Packaged Device	0.36g
Lid Characteristics	Finish: Gold Lid Potential: Connected to SGND pin

8.1 Metalization Mask Layout

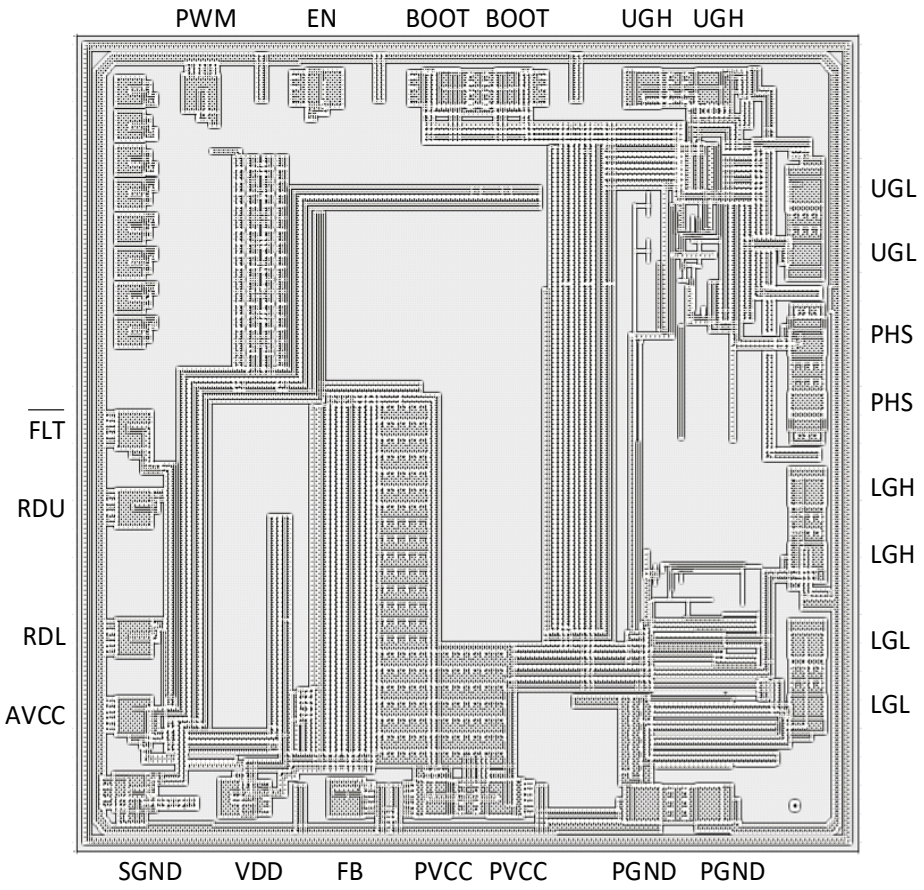


Table 3. Layout X-Y Coordinates (Centroid of Bond Pad)[1]

Pad Name	Pad Number[2]	X Coordinate (µm)	Y Coordinate (µm)	Pad X Dimension (µm)	Pad Y Dimension (µm)	Bond Wire Diameter (0.001")
EN	1	842.5	2529.14	110	110	1.25
PWM	2	413.46	2510.55	110	110	1.25
$\overline{FLT}$	3	177.54	1384.83	110	110	1.25
RDU	4	177.54	1124.81	110	110	1.25
RDL	5	177.54	690.56	110	110	1.25
AVCC	6	177.54	430.56	110	110	1.25
VDD	7	539.75	154.86	110	110	1.25
FB	8	918.37	154.86	110	110	1.25
PVCC	9 (a)	1220.02	154.86	110	110	1.25
PVCC	9 (b)	1475.02	154.86	110	110	1.25
PGND	10 (a)	1954.00	134.50	110	110	1.25
PGND	10 (b)	2204.00	134.50	110	110	1.25
LGL	11 (a)	2529.14	438.13	110	110	1.25

Table 3. Layout X-Y Coordinates (Centroid of Bond Pad)[1] (Cont.)

Pad Name	Pad Number[2]	X Coordinate (µm)	Y Coordinate (µm)	Pad X Dimension (µm)	Pad Y Dimension (µm)	Bond Wire Diameter (0.001”)
LGL	11 (b)	2529.14	688.13	110	110	1.25
LGH	12 (a)	2529.14	943.20	110	110	1.25
LGH	12 (b)	2529.14	1193.42	110	110	1.25
PHS	13 (a)	2529.14	1448.71	110	110	1.25
PHS	13 (b)	2529.14	1698.42	110	110	1.25
UGL	14 (a)	2523.5	1954.00	110	110	1.25
UGL	14 (b)	2523.5	2204.00	110	110	1.25
UGH	15 (a)	2204.00	2529.14	110	110	1.25
UGH	15 (b)	1954.00	2529.14	110	110	1.25
BOOT	16 (a)	1504.48	2529.14	110	110	1.25
BOOT	16 (b)	1254.48	2529.14	110	110	1.25
SGND	PAD	169.99	175.36	110	110	1.25

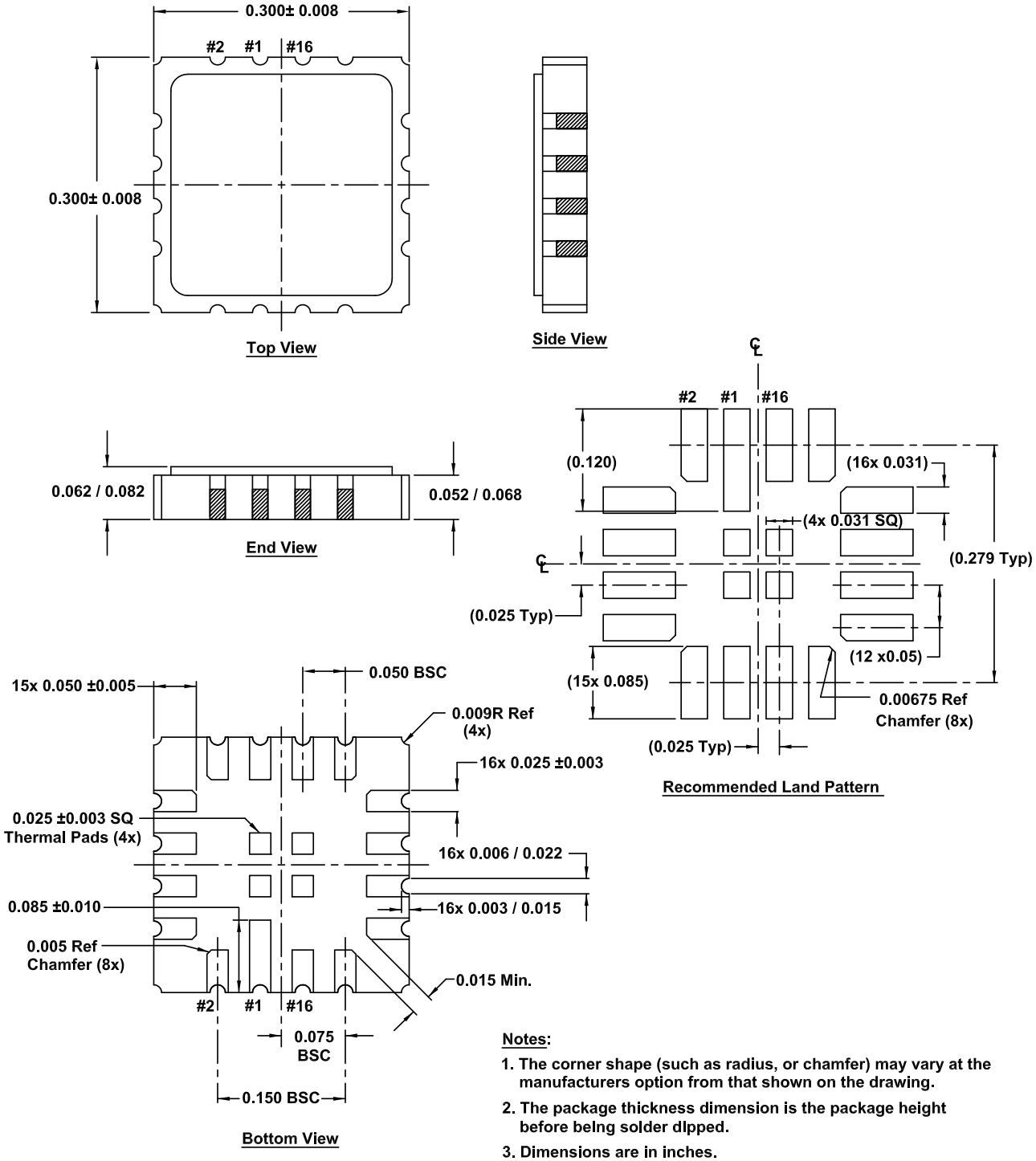
1. Origin of coordinate is the bottom left hand corner of die.
2. Pads 9 through 16 have double bond pads denoted as (a) and (b). Pad number designation intentionally assigned to match package pin number.

9. Package Outline Drawing

For the most recent package outline drawing, see J16.A.

J16.A

16 Pad Ceramic Leadless Chip Carrier (CLCC)
Rev 0, 1/20



Notes:

1. The corner shape (such as radius, or chamfer) may vary at the manufacturers option from that shown on the drawing.
2. The package thickness dimension is the package height before belng solder dlpped.
3. Dimensions are in inches.
   Dimensioning in ( ) for reference only.
4. Package is also compliant to MIL-STD-1835 CQCC1-N16 (C-1).

10. Ordering Information

Part Number[1]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp Range
ISL73041SEHML	LDR to 75krad(Si)	16 Pad CLCC Packaged Device (QML-V Level Screening)	J16.A	Tray	-55 to +125°C
ISL73041SEHMX[2]		Bare Die (QML-V Level Screening)	N/A	N/A	
ISL73041SEHX/SAMPLE[2][3]	N/A	Die	N/A	N/A	
ISL73041SEHL/PROTO[3]		16 Pad CLCC Packaged Device	J16.A	Tray	
ISL73041SEHEV1Z[4]	ISL73041SEH Evaluation Board				
ISL73847SEHEV2Z[4]	ISL73847SEH + ISL73041SEH Evaluation Board				
ISL73847SEHDEMO2Z[4]	ISL73847SEH + ISL73041SEH Business Card Size Demonstration board with Package GaN FETs; V_{IN} = 12V; V_{OUT} = 1V; I_{OUT} = 50A; f_{SW} = 500kHz;				

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications. The die is sourced from wafer lots that have been qualified for Group C and Group E per MIL-PRF-38535 (Refer to R34TB0001: Renesas Radiation Hardened QML-V Equivalent Screening and QCI Flow for more information).
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in this datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
4. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

11. Revision History

Rev.	Date	Description
1.04	Jan 31, 2025	Updated the PGND and SGND pin descriptions. Added SGND to PGND parameter spec to Abs max section. Updated the Layout Guidelines section.
1.03	Jan 4, 2024	Updated Features bullets. Added Dual Complimentary Low-Side GaN FET Driver section.
1.02	Jun 22, 2023	Updated Figure 14. Updated Ordering Information table.

Rev.	Date	Description
1.01	May 30, 2023	Updated Pin Descriptions for pin 4 and 5. Added 86MeV results to Abs max section. For the Quiescent Supply Current spec, updated test conditions, removed the 0V specs, and changed the maximum spec for the 1.3kΩ from 13mA to 9mA and moved the max values to the typical column. For the Dead Time Delay LG Falling to UG Rising spec, updated test conditions, removed the min and max specs for the 1.3kΩ, and updated the typical from 5ns to 6.5ns. For the Dead Time Delay UG Falling to LG Rising spec, updated test conditions, removed the min and max specs for the 1.3kΩ, and updated the typical from 5ns to 6.5ns. For the Dead Time Delay Match spec, updated test conditions, removed min and max limits, and added typical of -0.2ns. Updated test conditions and removed the max limits for the PWM Enter Mid-Level to UG Low Delay Time, PWM Exit Mid-Level to UG High Delay Time, PWM Enter Mid-Level to LG Low Delay Time, and PWM Exit Mid-Level to LG Rising Delay Time specs. For the VDD Quiescent Current spec in Table 1, removed the 0V line. Updated Figures 12, 20, 47. Corrected title for Figures 12, 14, and 38. Removed Figures 18 - 21. Changed 5ns to 6.5ns in the Dead Time Control section. Updated the Dead Time Control Resistor Setting section. Added the Power Dissipation section. Updated the Die and Assembly Characteristics section.
1.00	Mar 23, 2023	Initial release

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