ISL75051ASEH, ISL73051ASEH

3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator

FN8964
Rev.3.00
May 16, 2019

The ISL75051ASEH and ISL73051ASEH are radiation hardened low-voltage, high-current, single-output LDOs specified for up to 3.0A of continuous output current. These devices operate across an input voltage range of 2.2V to 6.0V and can provide output voltages of 0.8V to 5.0V adjustable, based on the resistor divider setting. Dropout voltages as low as 65mV can be achieved using the device.

The OCP pin allows the short-circuit output current limit threshold to be programmed by a resistor from the OCP pin to GND. The OCP setting range is 0.5A minimum to 8.5A maximum. The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value. It subsequently enters an ON/OFF cycle until the fault is removed. The ENABLE feature allows the part to be placed into a low current shutdown mode that typically draws about 10µA.

These devices are optimized for fast transient response and Single Event Effects (SEE). This reduces the magnitude of Single Event Transients (SET) seen on the output. Additional protection diodes and filters are not needed. These devices are stable with tantalum capacitors as low as 47µF and provide excellent regulation all the way from no load to full load. Programmable soft-start allows the user to program the inrush current by using the decoupling capacitor value on the BYP pin.

Applications

- LDO regulator for space applications
- DSP, FPGA, and µP core power supplies
- Post-regulation of switched mode power supplies
- Down-hole drilling

Features

- DLA SMD 5962-11212
- Output current up to 3.0A at T_J = +150°C
- Output accuracy ±1.5% over MIL temperature range
- Ultra low dropout:
  - 65mV (typical) dropout at 1.0A
  - 225mV (typical) dropout at 3.0A
- SET mitigation with no added filtering/diodes
- Input supply range: 2.2V to 6.0V
- Fast load transient response
- Shutdown current of 10µA (typical)
- Output adjustable using external resistors
- PSRR 66dB (typical) at 1kHz
- Enable and PGood features
- Programmable soft-start/inrush current limiting
- Over-temp shutdown and programmable OCP limits
- Stable with 47µF min tantalum capacitor
- Radiation hardness (ISL75051ASEH only)
  - High dose rate (50-300rad(Si)/s): 100krad(Si)
  - Low dose rate (≤0.01rad(Si)/s): 50krad(Si)
- Radiation hardness (ISL73051ASEH only)
  - Low dose rate (≤0.01rad(Si)/s): 50krad(Si)

Related Literature

- For a full list of related documents, visit our website:
  - ISL75051ASEH, ISL73051ASEH device pages

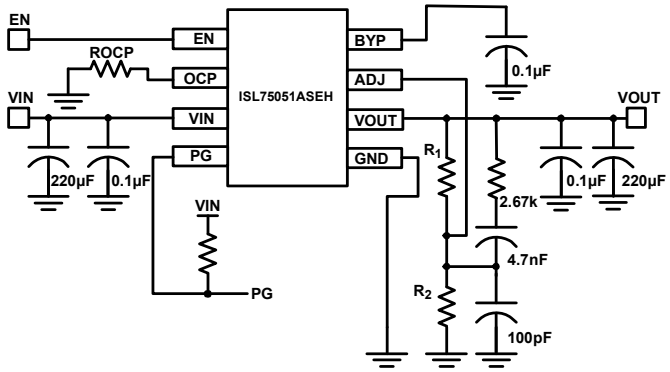

Figure 1. Typical Application

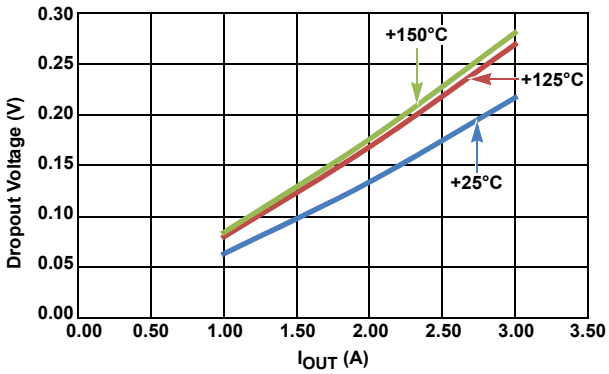

Figure 2. Dropout vs I_{OUT}

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1. Overview

1.1 Block Diagram

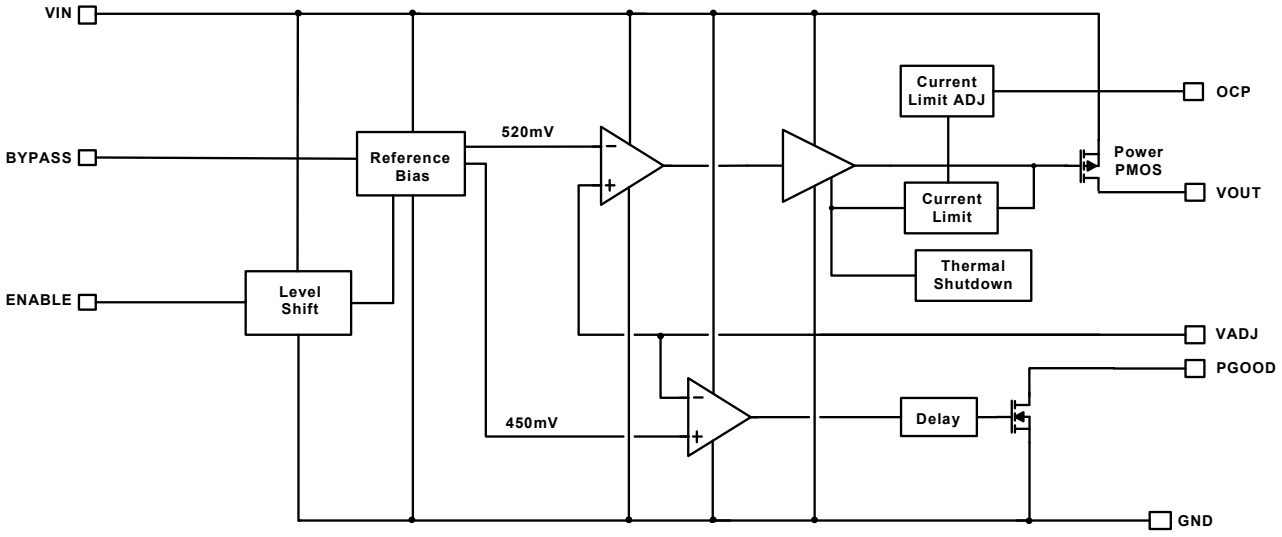


Figure 3. Block Diagram

1.2 Typical Application

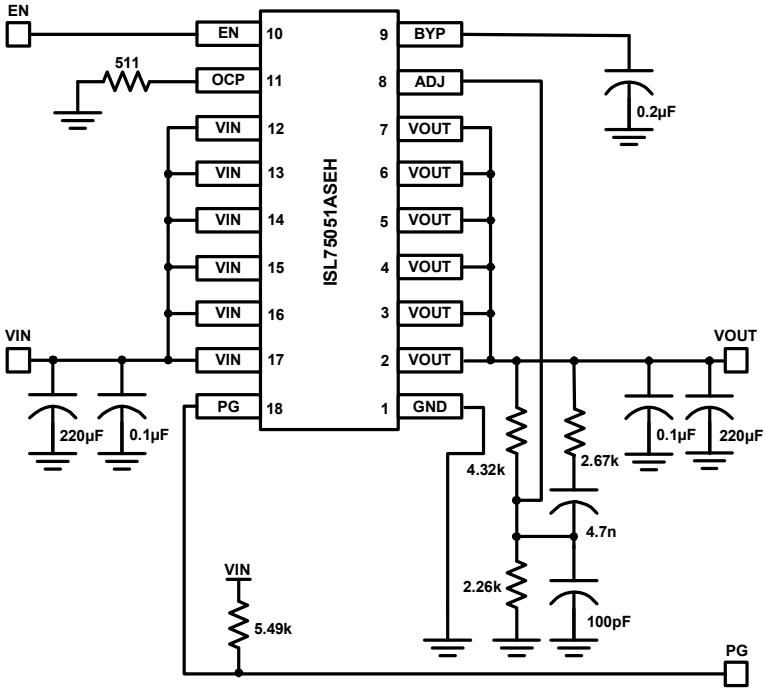


Figure 4. Typical Application

1.3 Ordering Information

Ordering SMD Number (Notes 1, 2)	Part Number	Temp Range (°C)	Package (RoHS Compliant)	Pkg Dwg. #
5962R1121203VXC	ISL75051ASEHVF	-55 to +125	18 Ld CDFP	K18.D
N/A	ISL75051ASEHF/PROTO (Note 3)	-55 to +125	18 Ld CDFP	K18.D
5962R1121203V9A	ISL75051ASEHVX	-55 to +125	Die	
5962R1121203VYC	ISL75051ASEHVFE	-55 to +125	18 Ld CDFP with Bottom METAL	K18.E
N/A	ISL75051ASEHFE/PROTO (Note 3)	-55 to +125	18 Ld CDFP with Bottom Metal	K18.E
N/A	ISL75051ASEHX/SAMPLE (Note 3)	-55 to +125	Die Sample	
5962L1121204VXC	ISL73051ASEHVF	-55 to +125	18 Ld CDFP	K18.D
N/A	ISL73051ASEHF/PROTO (Note 3)	-55 to +125	18 Ld CDFP	K18.D
5962L1121204V9A	ISL73051ASEHVX	-55 to +125	Die	
5962L1121204VYC	ISL73051ASEHVFE	-55 to +125	18 Ld CDFP with Bottom Metal	K18.E
N/A	ISL73051ASEHFE/PROTO (Note 3)	-55 to +125	18 Ld CDFP with Bottom Metal	K18.E
N/A	ISL73051ASEHX/SAMPLE (Note 3)	-55 to +125	Die Sample	
N/A	ISL75051ASEHEV1Z (Note 4)	Evaluation Board		

Notes:

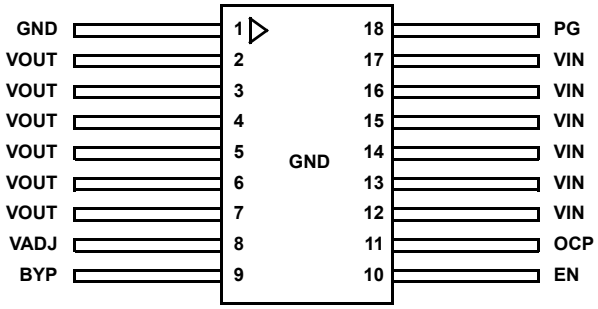
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.
4. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 1. Key Differences Between Family of Parts

Part Numbers	TID Ratings
ISL75051ASEH	HDR to 100krad(Si) RHA Tested LDR to 50krad(Si) RHA Tested
ISL73051ASEH	LDR to 50krad(Si) RHA Tested

1.4 Pin Configuration

18 Ld CDFP
Top View



Note: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.5 Pin Descriptions

Pin Number	Pin Name	Description
1	GND	GND pin.
2, 3, 4, 5, 6, 7	VOUT	Output voltage pins.
8	VADJ	The VADJ pin allows V_{OUT} to be programmed with an external resistor divider.
9	BYP	To filter the internal reference, connect a 0.1µF capacitor from the BYP pin to GND.
10	EN	V_{IN} independent chip enable. TTL and CMOS compatible.
11	OCP	Allows the current limit to be programmed with an external resistor.
12, 13, 14, 15, 16, 17	VIN	Input supply pins.
18	PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Must be grounded if not used.
Top Lid	GND	The top lid is connected to the GND pin of the package.
Bottom Metal	-	The bottom E-pad is only available on the K18.E package and is not electrically connected.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{IN} Relative to GND (Note 5)	-0.3	6.7	V
V_{OUT} Relative to GND (Note 5)	-0.3	6.7	V
PG, EN, OCP/ADJ Relative to GND (Note 5)	-0.3	6.7	V
V_{IN} Relative to GND (Notes 5, 6)	-0.3	6.2	V
V_{OUT} Relative to GND (Notes 5, 6)	-0.3	6.2	V
PG, EN, OCP/ADJ Relative to GND (Notes 5, 6)	-0.3	6.2	V
Junction Temperature (T_J) (Note 5)		+175	°C
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-PRF-883 3015.7)	2.5		kV
Machine Model (Tested per JESD22-A115C)	250		V
Charged Device Model (Tested per JS-002-2014)	1		kV

Notes:

5. Extended operation at these conditions can compromise reliability. Exceeding these limits results in damage. Recommended operating conditions define limits where specifications are established.
6. Tested in a heavy ion environment at LET = 86.3MeV•cm^2/mg at +125°C (T_C).

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
18 Ld CDFP Package (Notes 7, 8)	28	4
18 Ld CDFP Package with Bottom Metal and Solder Mount (Notes 7, 8)	24	3.3

Notes:

7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
8. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter (Note 9)	Minimum	Maximum	Unit
Ambient Temperature Range (T_A)	-55	+125	°C
Junction Temperature (T_J)		+150	°C
V_{IN} Relative to GND	2.2	6.0	V
V_{OUT} Range	0.8	5	V
PG, EN, OCP/ADJ Relative to GND	0	+6.0	V

Note:

9. Refer to “Thermal Guidelines” on page 16.

2.4 Radiation Information

Parameter	Minimum	Maximum	Unit
Maximum Total Dose			
Dose Rate = 50-300rad(Si)/s (ISL75051ASEH only)		100	krad(Si)
Dose Rate = 0.01rad(Si)/s		50	krad(Si)
SEE Performance			
SET (V_{OUT} <±5% During Events) (Note 10)		86.3	MeV•cm^2/mg
SEL/SEB (No Latch-Up/Burnout)		86.3	MeV•cm^2/mg

Note:
10. Refer to this device's Radiation report for more details.

2.5 Electrical Specifications

Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 220\mu F$, 25mΩ, and 0.1µF X7R, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature (see Note 14). **Boldface limits apply across the operating temperature range, -55°C to +125°C.** Pulse load techniques are used by ATE to ensure $T_J = T_A$ defines established limits.

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Unit
DC Characteristics						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} resistor adjust to 0.52V, 1.5V, and 1.8V 2.2V < V_{IN} < 3.6V; 0A < I_{LOAD} < 3.0A	**-1.5**	0.2	**1.5**	%
		V_{OUT} resistor adjust to 5.0V V_{OUT} + 0.4V < V_{IN} < 6.0V; 0A < I_{LOAD} <3.0A	**-1.5**	0.2	**1.5**	%
VADJ Pin Voltage	V_{ADJ}	2.2V < V_{IN} < 6.0V; I_{LOAD} = 0A	**514.8**	520.0	**525.2**	mV
BYP Pin	V_{BYP}	2.2V < V_{IN} < 6.0V; I_{LOAD} = 0A		520		mV
DC Input Line Regulation		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.5V, +25°C and -55°C (Note 12)		1.13	3.50	mV
		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.5V, +125°C (Note 12)		1.13	8.00	mV
		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.8V, +25°C and -55°C (Note 12)		1.62	3.50	mV
		2.2V < V_{IN} < 3.6V, V_{OUT} = 1.8V, +125°C (Note 12)		1.62	10.50	mV
		V_{OUT} + 0.4V < V_{IN} < 6.0V, V_{OUT} = 5.0V (Note 12)		12.50	**20.00**	mV
DC Output Load Regulation		V_{OUT} = 1.5V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V (Note 12)	**-4.00**	-0.8	**-0.1**	mV
		V_{OUT} = 1.8V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V (Note 12)	**-4.80**	-1.20	**-0.05**	mV
		V_{OUT} = 5.0V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V (Note 12)	**-15.00**	-6.00	**-0.05**	mV
VADJ Input Current		V_{ADJ} = 0.5V			**1**	µA
Ground Pin Current	I_Q	V_{OUT} = 1.5V; I_{LOAD} = 0A, V_{IN} = 2.2V		11	**13**	mA
		V_{OUT} = 5.0V; I_{LOAD} = 0A, V_{IN} = 6.0V		16	**19**	mA
		V_{OUT} = 1.5V; I_{LOAD} = 3.0A, V_{IN} = 2.2V		11	**14**	mA
		V_{OUT} = 5.0V; I_{LOAD} = 3.0A, V_{IN} = 6.0V		16	**20**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0V, V_{IN} = 6.0V		10	**30**	µA

Unless otherwise noted, all parameters are established over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 220\mu F$, $25m\Omega$, and $0.1\mu F$ X7R, $T_J = +25°C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature (see Note 14). **Boldface limits apply across the operating temperature range, -55°C to +125°C.** Pulse load techniques are used by ATE to ensure $T_J = T_A$ defines established limits. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Unit
Dropout Voltage	V_{DO}	$I_{LOAD} = 1.0A$, $V_{OUT} = 2.5V$ (Note 13)		65	**100**	mV
		$I_{LOAD} = 2.0A$, $V_{OUT} = 2.5V$ (Note 13)		140	**200**	mV
		$I_{LOAD} = 3.0A$, $V_{OUT} = 2.5V$ (Note 13)		225	**300**	mV
Output Short-Circuit Current	I_{SCL}	$V_{OUT} = 0V$, $V_{IN} = 2.2V$, $R_{SET} = 5.11k$		1.1		A
		$V_{OUT} = 0V$, $V_{IN} = 6.0V$, $R_{SET} = 5.11k$		1.2		A
Output Short-Circuit Current	I_{SCH}	$V_{OUT} = 0V$, $V_{IN} = 2.2V$, $R_{SET} = 511\Omega$		5.7		A
		$V_{OUT} = 0V$, $V_{IN} = 6.0V$, $R_{SET} = 511\Omega$		6.2		A
Thermal Shutdown Temperature	TSD	$V_{OUT} + 0.4V < V_{IN} < 6.0V$		175		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$V_{OUT} + 0.4V < V_{IN} < 6.0V$		25		°C
AC Characteristics						
Input Supply Ripple Rejection	PSRR	$V_{P-P} = 300mV$, $f = 1kHz$, $I_{LOAD} = 3A$; $V_{IN} = 2.5V$, $V_{OUT} = 1.8V$	**42**	66		dB
		$V_{P-P} = 300mV$, $f = 100kHz$, $I_{LOAD} = 3A$; $V_{IN} = 2.5V$, $V_{OUT} = 1.8V$		30		dB
Phase Margin	PM	$V_{OUT} = 1.8V$, $C_L = 220\mu F$ Tantalum		70		dB
Gain Margin	GM	$V_{OUT} = 1.8V$, $C_L = 220\mu F$ Tantalum		16		dB
Output Noise Voltage		$I_{LOAD} = 10mA$, BW = 300Hz < f < 300kHz, BYPASS to GND capacitor = 0.2µF		100		μV_{RMS}
Device Start-Up Characteristics: Enable Pin						
Rising Threshold		$2.2V < V_{IN} < 6.0V$	**0.6**	0.9	**1.2**	V
Falling Threshold		$2.2V < V_{IN} < 6.0V$	**0.47**	0.70	**0.90**	V
Enable Pin Leakage Current		$V_{IN} = 6.0V$, EN = 6.0V			**1**	µA
Enable Pin Propagation Delay		$V_{IN} = 2.2V$, EN rise to I_{OUT} rise	**225**	300	**450**	µs
Hysteresis		Must be independent of V_{IN}; $2.2V < V_{IN} < 6.0V$	**90**	200	**318**	mV
Device Start-Up Characteristics: PG Pin						
PG Rising Threshold		$2.2V < V_{IN} < 6.0V$	**85**	90	**97**	%
PG Falling Threshold		$2.2V < V_{IN} < 6.0V$	**82**	88	**93**	%
PG Hysteresis		$2.2V < V_{IN} < 6.0V$	**2.5**	3.2	**5.0**	$\%V_{OUT}$
PG Low Voltage		$I_{SINK} = 1mA$		35	**100**	mV
		$I_{SINK} = 6mA$		185	**400**	mV
PG Leakage Current		$V_{IN} = 6.0V$, PG = 6.0V		0.01	1.00	µA

Notes:

11. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
12. Line and Load Regulation done under pulsed condition for T <10ms.
13. Dropout is defined as the difference between the supply V_{IN} and V_{OUT}, when the supply produces a 2% drop in V_{OUT} from its nominal value. Data measured within a 3ms period.
14. See"Applications Information" on page 12 and TB379.

3. Typical Operating Performance

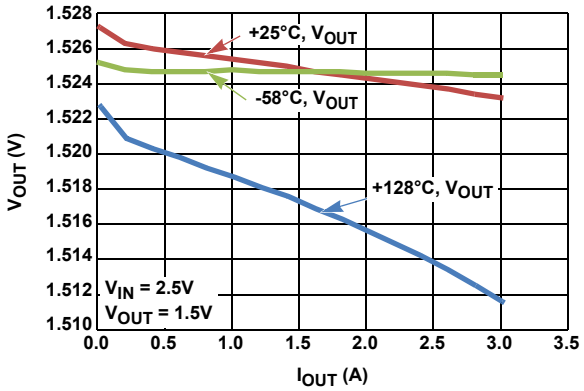


Figure 5. Load Regulation, V_{OUT} vs I_{OUT}

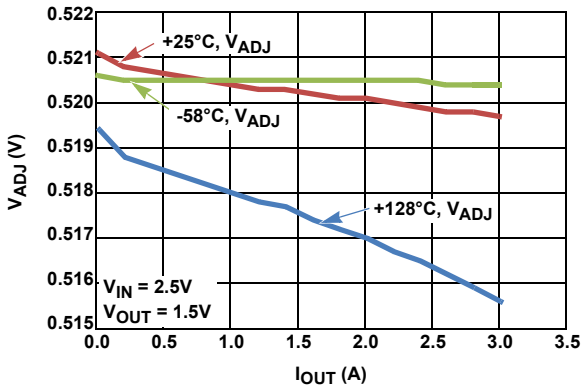


Figure 6. Load Regulation, V_{ADJ} vs I_{OUT}

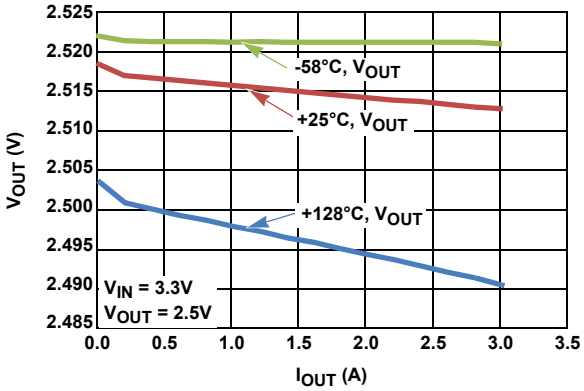


Figure 7. Load Regulation, V_{OUT} vs I_{OUT}

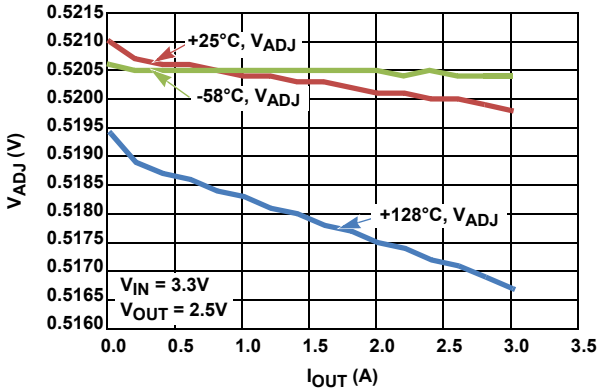


Figure 8. Load Regulation, V_{ADJ} vs I_{OUT}

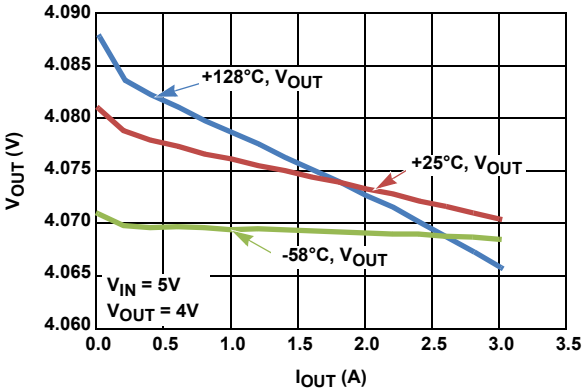


Figure 9. Load Regulation, V_{OUT} vs I_{OUT}

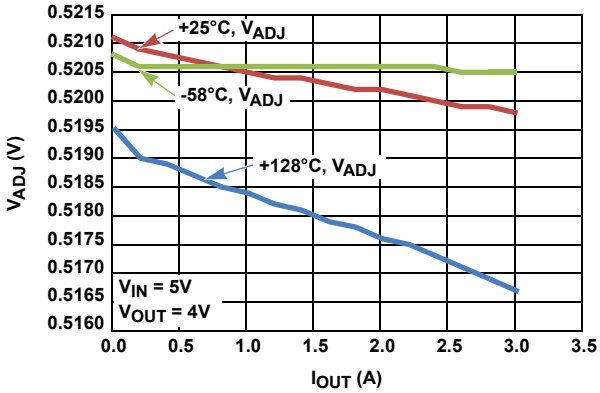


Figure 10. Load Regulation, V_{ADJ} vs I_{OUT}

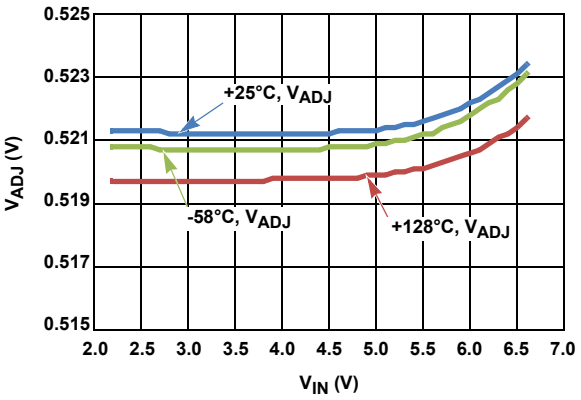


Figure 11. V_{IN} vs V_{ADJ} Over-Temperature

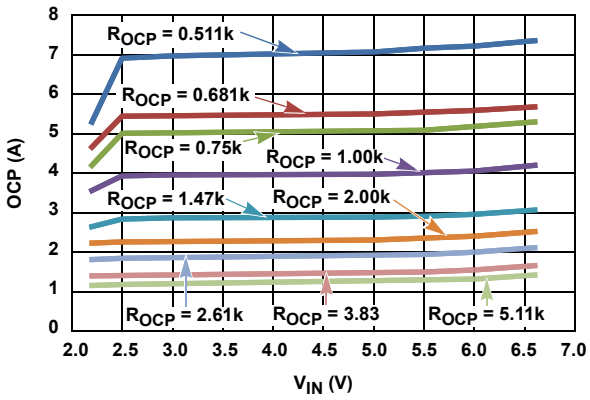


Figure 12. R_{OCP} vs OCP at +25°C, V_{OUT} = 1.5V

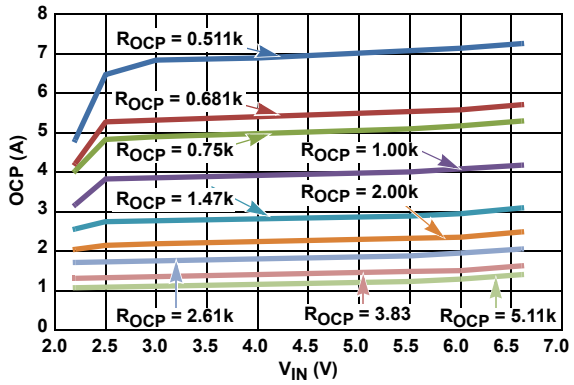


Figure 13. R_{OCP} vs OCP at +128°C, V_{OUT} = 1.5V

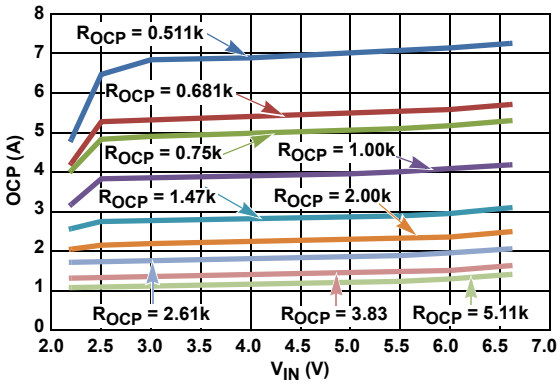


Figure 14. R_{OCP} vs OCP at -58°C, V_{OUT} = 1.5V

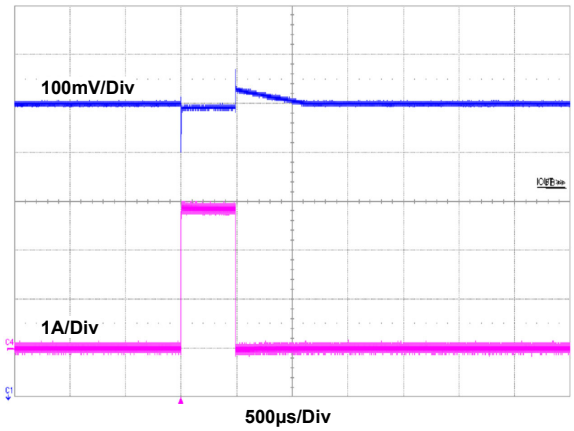


Figure 15. Transient Load Response, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 47µF, 35mΩ

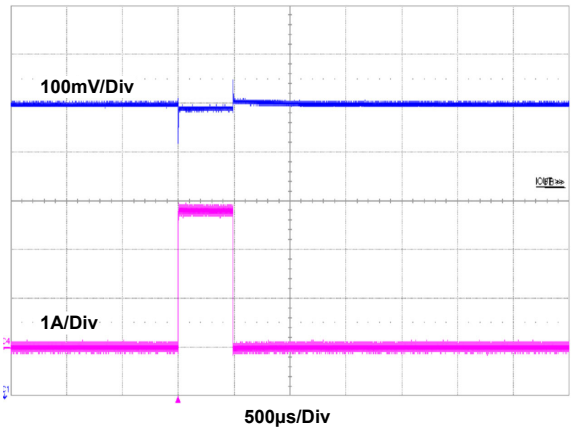


Figure 16. Transient Load Response, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 220µF, 25mΩ

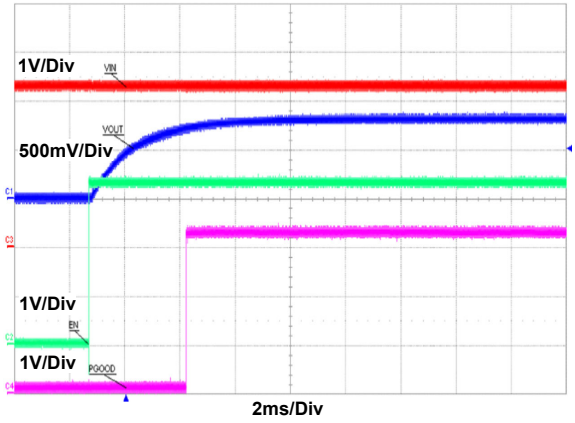


Figure 17. Power-On and Power-Off, EN = 0 to 1, +25°C, V_{IN} = 3.3V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD Turn-On

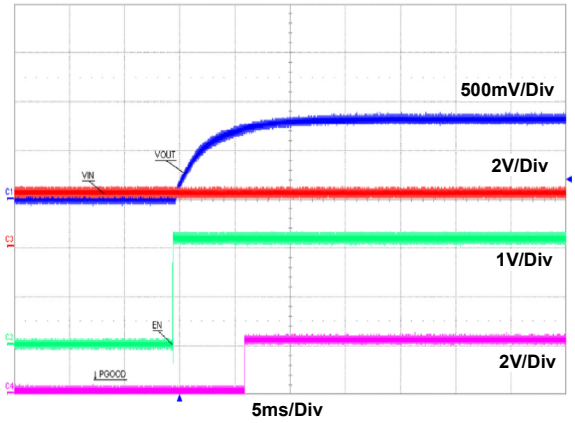


Figure 18. Power-On and Power-Off, EN = 0 to 1, +25°C, V_{IN} = 2.2V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD Turn-On

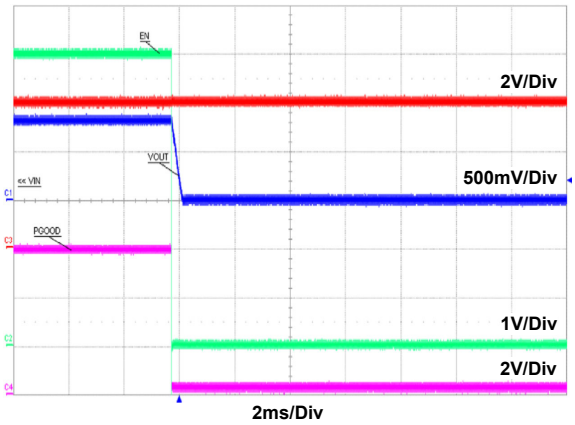


Figure 19. Power-On and Power-Off, EN = 1 to 0, +25°C, V_{IN} = 6V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD Turn-Off

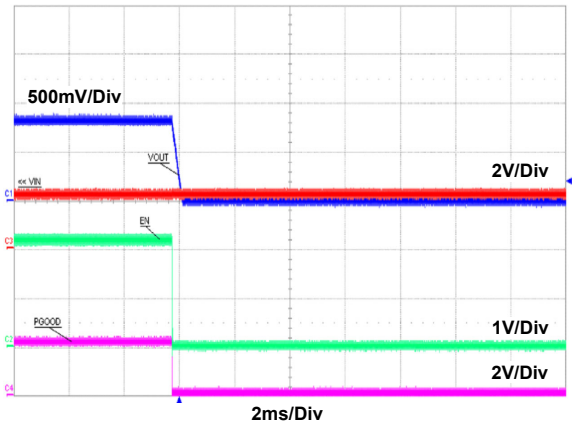


Figure 20. Power-On and Power-Off, EN = 1 to 0, +25°C, V_{IN} = 2.2V, V_{OUT} = 0.8V, I_{OUT} = 0.5A, PGOOD Turn-Off

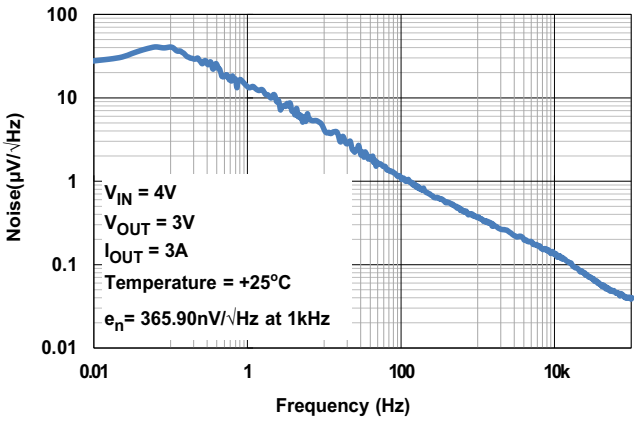


Figure 21. Noise (µV/√Hz)

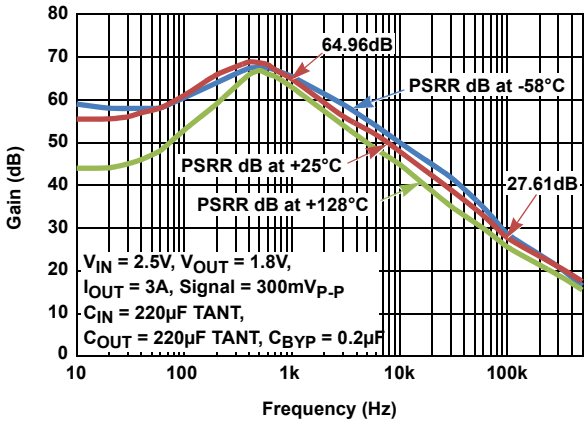


Figure 22. PSRR

4. Applications Information

4.1 Input Voltage Requirements

These radiation hardened LDOs work from a V_{IN} in the range of 2.2V to 6.0V. The input supply can have a tolerance of as much as ±10% for conditions noted in the "Electrical Specifications" on page 7. The minimum input voltage is 2.2V. However, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage, and dropout at the maximum rated current of the application, if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The dropout specification of this family of LDOs has been generously specified to allow applications to design for efficient operation.

4.2 Adjustable Output Voltage

The output voltage of the radiation hardened LDOs can be set to any user-programmable level between 0.8V and 5.0V. This is achieved with a resistor divider connected between the OUT, ADJ, and GND pins. With the internal reference at 0.52V, the divider ratio should be fixed so that when the desired V_{OUT} level is reached, the voltage presented to the ADJ pin is 0.52V. Resistor values for typical voltages are shown in Table 2.

Table 2. Resistor Values for Typical Voltages

V_{OUT} (V)	R_{BOTTOM} (Ω)	R_{TOP} (kΩ)
0.8	7.87k	4.32
1.5	2.26k	4.32
1.8	1.74k	4.32
2.5	1.13k	4.32
4.0	634	4.32
5.0	499	4.32

$$R_{BOTTOM} = \frac{R_{TOP}}{\left(\frac{V_{OUT}}{V_{ADJ}}\right) - 1} \quad \text{(EQ. 1)}$$

4.3 Input and Output Capacitor Selection

The radiation hardened operation requires the use of a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 220µF, 10V, 25mΩ rated DSSC 04051-032 series tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 CDR04 ceramic capacitor that is connected between the VIN to GND pins and the VOUT to GND pins of the LDO, with PCB traces no longer than 0.5cm.

While using the same capacitor for both VIN and VOUT simplifies the design and reduces the BOM count, it is not required to do so. The VIN capacitance provides transient current during start-up and load steps while ensuring that VIN does not drop below the UVLO threshold. The VIN capacitance can be sized appropriately for a given application as long as those two criteria are met.

The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6mΩ to 100mΩ. At the lower limit of ESR = 6mΩ, the phase margin is about 51°. On the high side, an ESR of 100mΩ is found to limit the gain margin at around 10dB. The typical GM/PM seen with capacitors is shown in Table 3.

Table 3. Typical GM/PM with Various Capacitors

Capacitance (µF)	ESR (mΩ)	Gain Margin (dB)	Phase Margin (°)
47	35	14	55
100	25	16	57

Table 3. Typical GM/PM with Various Capacitors (Continued)

Capacitance (µF)	ESR (mΩ)	Gain Margin (dB)	Phase Margin (°)
220	6	19	51
220	25	16	69
100	100	10	62

The type numbers of the KEMET capacitors used in the device are shown in Table 4.

Table 4. KEMET Capacitors Used in Device

KEMET Type Number	Capacitor Details
T525D476M016ATE035	47µF, 10V, 35mΩ
T525D107M010ATE025	100µF, 10V, 25mΩ
T530D227M010ATE006	220µF, 10V, 6mΩ
T525D227M010ATE025	220µF, 10V, 25mΩ
T495X107K016ATE100	100µF, 16V, 100mΩ

A typical gain phase plot measured on the ISL75051ASEHEV1Z evaluation board for V_{IN} = 3.3V, V_{OUT} = 1.8V, and I_{OUT} = 3A with a 220µF, 10V, 25mΩ capacitor is shown in Figure 23 and is measured at GM = 16.3dB and PM = 69.16°.

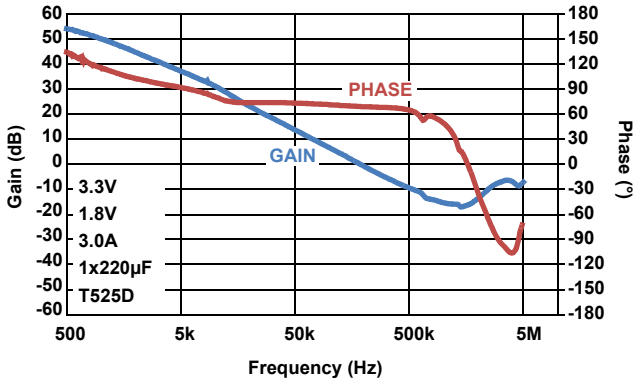


Figure 23. Typical Gain Phase Plot

4.4 Enable

These devices can be enabled by applying a logic high on the EN pin. The enable threshold is typically 0.9V. A soft-start cycle is initiated when the devices are enabled using this pin. Taking this pin to logic low disables the devices.

The EN can be driven from either an open drain or a totem pole logic drive between the EN pin and GND. Assuming an open-drain configuration, M1 actively pulls down the EN line, as shown in Figure 24 on page 14, and thereby discharges the input capacitance, shutting off the devices immediately.

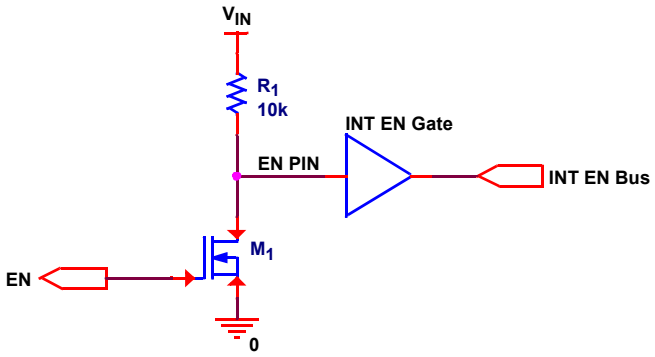


Figure 24. Enable

4.5 Power-Good

The power-good pin is asserted high when the voltage on the ADJ pin crosses the rising threshold of 0.9 x V_{ADJ} (typical). On the falling threshold, power-good is asserted low when the voltage on the ADJ pin crosses the falling threshold of 0.88 x V_{ADJ}. The power-good output is an open-drain output rated for a continuous sink current of 1mA.

4.6 Soft-Start

Soft-start is achieved by the BYP pin charging time constant. The capacitor value on the pin determines the time constant and can be calculated using Equations 2 through 4 based on the V_{IN} range:

If the V_{IN} range is $2.2V \le V_{IN} < 2.7V$:

(EQ. 2) $$t_{SS} = (-4.8376 \bullet V_{IN}) + (0.0254 \bullet T_A) + (0.0522 \bullet C_{BYP}) + 11.8526$$

If the V_{IN} range is $2.7V \le V_{IN} < 4.0V$:

(EQ. 3) $$t_{SS} = (-1.4711 \bullet V_{IN}) + (0.0179 \bullet T_A) + (0.0377 \bullet C_{BYP}) + 4.7430$$

If the V_{IN} range is $4.0V \le V_{IN} < 6.0V$:

(EQ. 4) $$t_{SS} = (-0.4458 \bullet V_{IN}) + (0.0130 \bullet T_A) + (0.0295 \bullet C_{BYP}) + 1.8527$$

where t_{SS} = soft-start time (ms), V_{IN} = input supply (V), T_A = ambient temperature, and C_{BYP} = BYPASS capacitor (nF).

The BYPASS capacitor, C_1, charges with a current source and provides an EA reference, -IN, with an SS ramp. V_{OUT} follows this ramp in turn. The ramp rate can be calculated based on the C_1 value. For conditions in which C_1 is opened, or for small values of C_1, the ramp is provided by C_2 = 50pF, with a source of 0.5µA. Connecting C_1 min = 0.1µF to the BYPASS pin is recommended for normal operation.

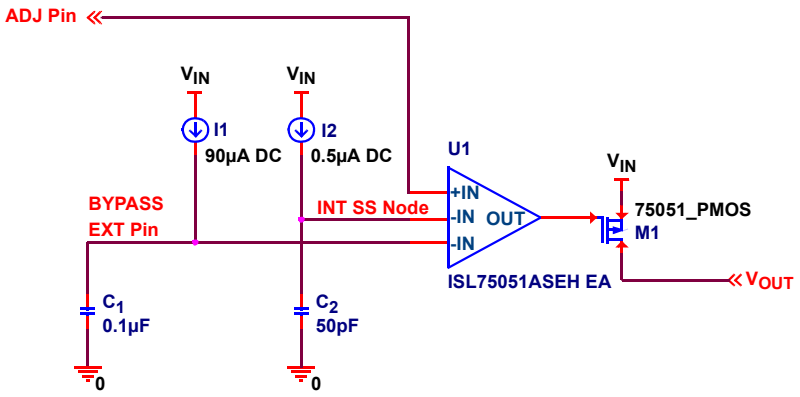


Figure 25. Soft-Start

4.7 Current Limit Protection

The radiation hardened LDOs incorporate protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit becomes a constant current source when the output current exceeds the current limit threshold, which can be adjusted by means of a resistor connected between the OCP pin and GND. If the short or overload condition is removed from V_{OUT}, the output returns to normal voltage mode regulation. The OCP can be calculated with Equation 5:

(EQ. 5)

$2.2V \le V_{IN} < 3.0V$:

$$I_{OCP} = (V_{IN} \cdot 1.2688) + \left(\frac{2.8691}{R_{OCP}}\right) + (T_A \cdot -0.002) - 2.1851$$

$3.0V \le V_{IN} < 6.6V$:

$$I_{OCP} = (V_{IN} \cdot 6.168E-02) + \left(\frac{3.3161}{R_{OCP}}\right) + (T_A \cdot 1.5312E-04) - 0.3176$$

where OCP = Overcurrent Threshold in amps and ROCP = OCP resistor in kΩ. Visit our website for an Excel tool to help calculate the ROCP value needed for a given OCP level.

In the event of an overload condition based on the set OCP limit, the die temperature can exceed the internal over-temperature limit, and the LDOs begin to cycle on and off due to the fault condition (Figure 26). However, thermal cycling may never occur if the heatsink used for the package can keep the die temperature below the limits specified for thermal shutdown.

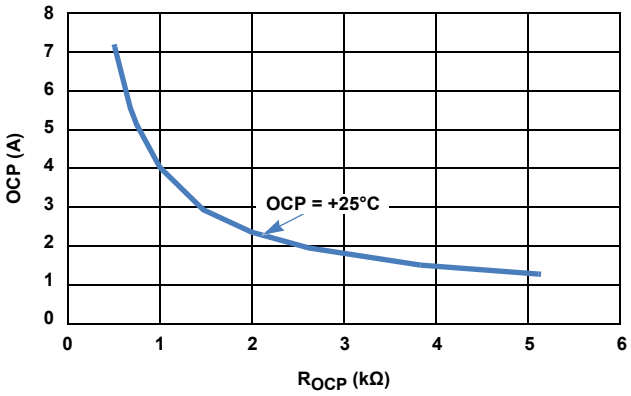


Figure 26. OCP vs R_{OCP}

4.8 Thermal Guidelines

If the die temperature exceeds approximately +175°C, the LDO output shuts down to zero until the die temperature cools to approximately +155°C. The level of power combined with the thermal impedance of the package (θ_{JC} of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the Electrical Specifications table on page 8.

Mount these devices on a high-effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between the package base and the PCB copper plane. The V_{IN} and V_{OUT} ratios should be selected to ensure that dissipation for the selected V_{IN} range keeps T_J within the recommended operating level of +150°C for normal operation.

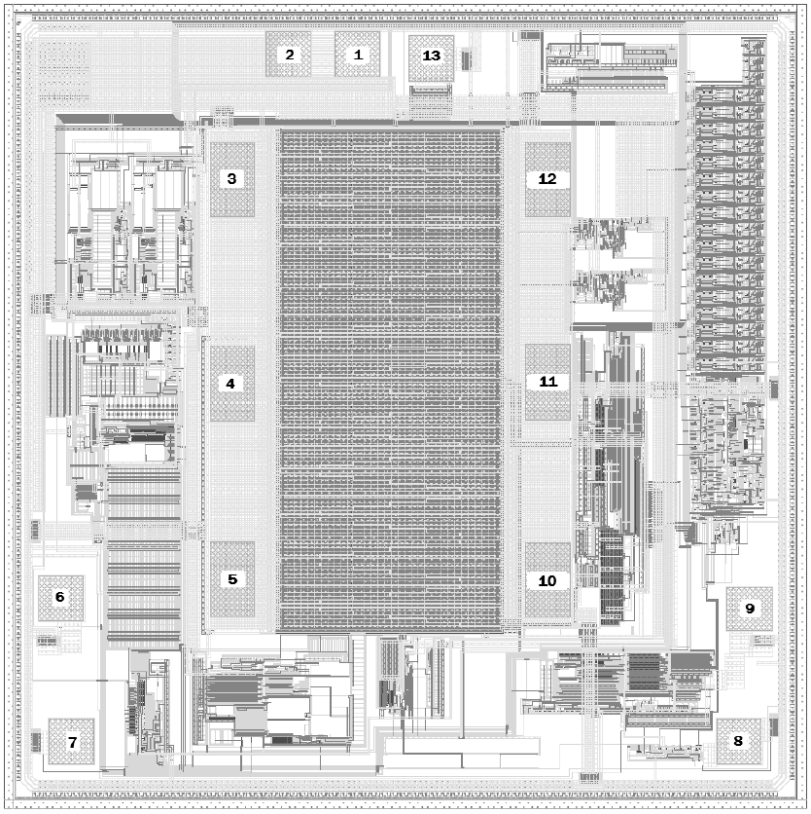
5. Die and Layout Characteristics

Table 5. Die and Assembly Related Information

Die Information	
Dimensions	4555µm x 4555µm (179.3 mils x 179.3 mils) Thickness: 304.8µm ±25.4µm (12.0 mils ±1 mil)
Interface Materials	
Glassivation	Type: Silicon Oxide and Silicon Nitride Thickness: 0.3µm ±0.03µm to 1.2µm ±0.12µm
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 2.7µm ±0.4µm
Backside Metallization	None
Substrate	Type: Silicon
Backside Finish	Silicon
Process	0.6µM BiCMOS Junction Isolated
Assembly Information	
Substrate Potential	Unbiased
Additional Information	
Worst Case Current Density	$<2 \times 10^5 A/cm^2$
Transistor Count	2932
Weight of Packaged Device	K18.D: 1.07g typical with leads clipped K18.E: 1.07g typical with leads clipped
Layout Characteristics	
Step and Repeat	4555µmx4555µm

6. Metallization Mask Layout

Pad X Y Coordinates					
Pad	Name	X (µm)	Y (µm)	DX (µm)	DY (µm)
1	GND	0	0	254	254
2	GND	-393	0	254	254
3	VOUT	-711	-710	254	422
4	VOUT	-711	-1858	254	422
5	VOUT	-711	-2964	254	422
6	ADJ	-1680	-3070	254	254
7	BYP	-1621	-3879	254	254
8	EN	2164	-3879	254	254
9	OCP	2222	-3131	254	246
10	VIN	1078	-2965	254	422
11	VIN	1078	-1853	254	422
12	VIN	1078	-711	254	422
13	PG	420	-25	254	254



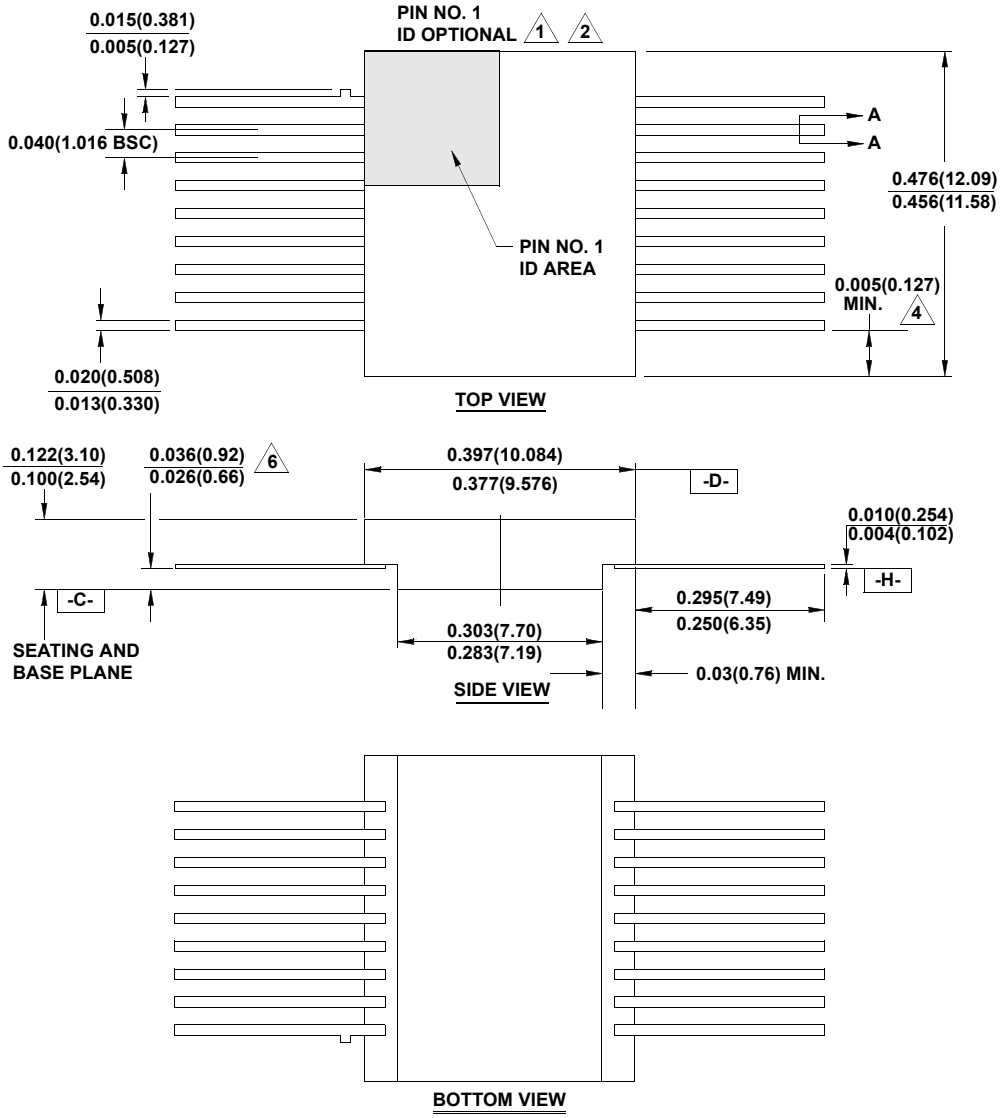
7. Revision History

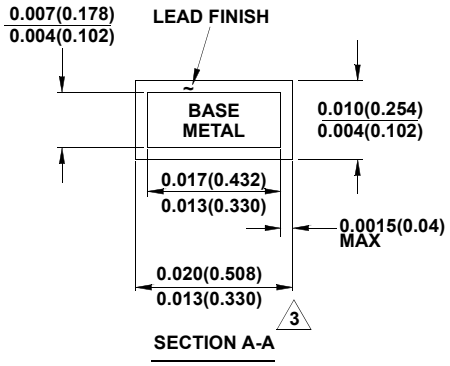
Rev.	Date	Description
3.00	May 16, 2019	Updated links throughout document. Added second paragraph in “Input and Output Capacitor Selection” on page 12. Updated disclaimer.
2.00	Mar 2, 2018	Updated Figure 3 on page 3. Changed Maximum Total Dose Rate at 0.01rad(Si)/s from 100krad(Si) to 50krad(Si) on page 7. Changed Maximum SEE Performance from 86MeV•cm^2/mg to 86.3MeV•cm^2/mg on page 7. Updated Note 10 to link to the device’s test report for SET and SEL/SEB on page 7. Removed Radiation Characteristics section (multiple pages). Updated Renesas disclaimer. Removed About Intersil section.
1.00	Nov 14, 2017	Added ISL75051ASEHF/PROTO and ISL73051ASEHF/PROTO to the Ordering Information table on page 4. Updated Pin descriptions adding bottom metal information. Updated Absolute Maximum Ratings table and added Note 6. Updated Radiation Information table and removed Note 10 on page 7. Updated DC Output Regulation (V_{OUT} = 1.8V) minimum spec from “”-4.0” to “-4.80”. Updated PG Rising Threshold maximum spec from “96” to “97”. Updated PG Hysteresis maximum spec from “4.0” to “5.0”. Updated heading for the tables in sections 3.1, 3.2, and 3.3.
0.00	Sept 25, 2017	Initial release

8. Package Outline Drawings

For the most recent package outline drawing, see K18.D.

K18.D 18 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 5, 3/13



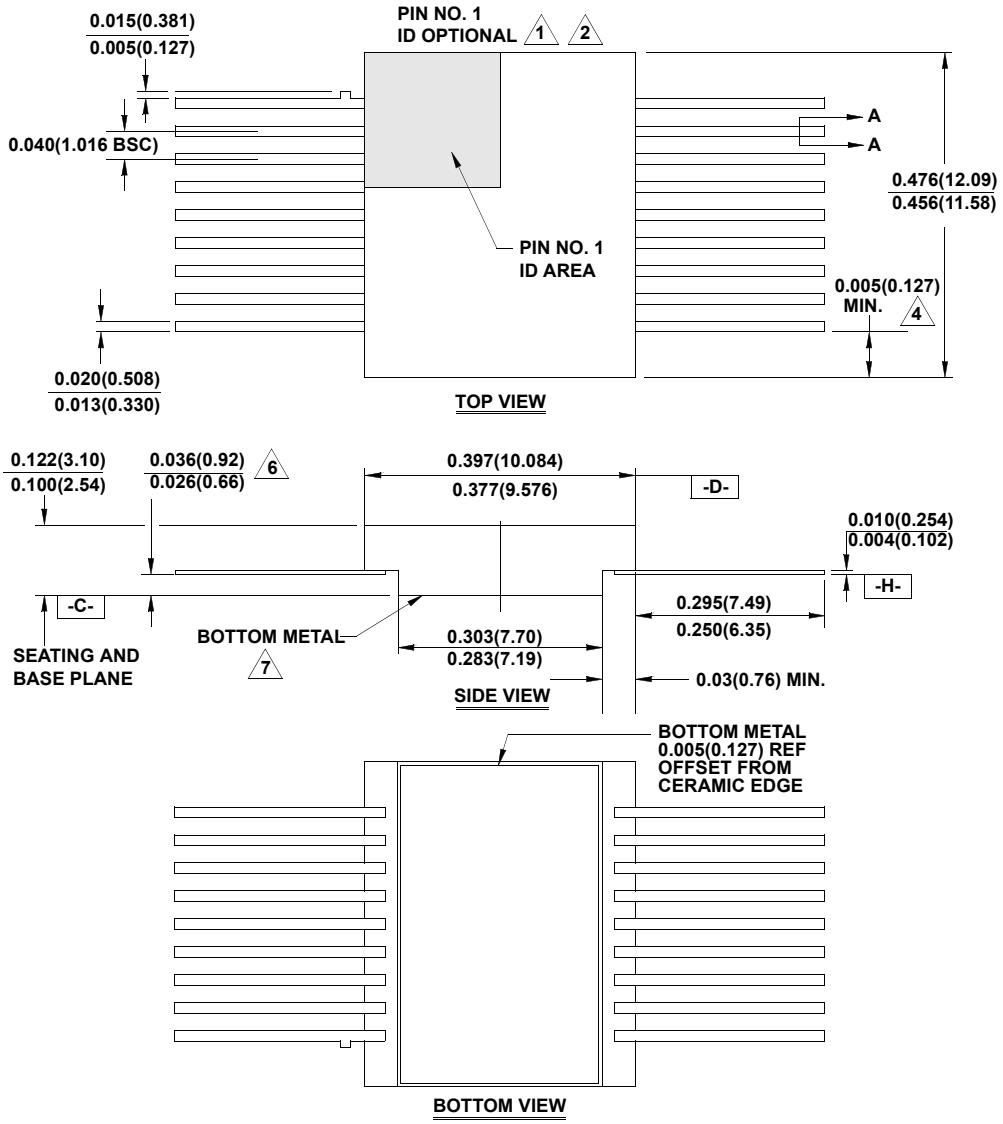


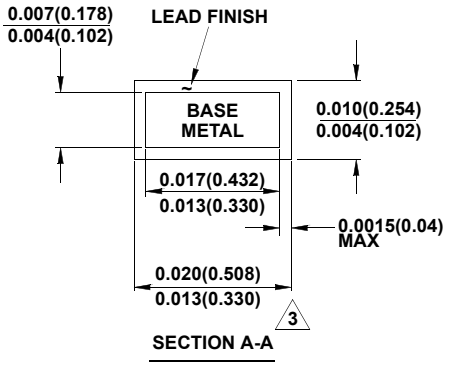
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions = INCH (mm). Controlling dimension: INCH.

K18.E
18 Lead Ceramic Metal Seal Flatpack Package with Bottom Metal
Rev 1, 3/13

For the most recent package outline drawing, see K18.E.





NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. The bottom of the package is a solderable metal surface.
8. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
9. Dimensions = INCH (mm). Controlling dimension: INCH.

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