**NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc**

ISL9000AM

Dual LDO with Low Noise, Very High PSRR and Low I_Q

FN6620
Rev 1.00
November 11, 2011

ISL9000AMRNCP is a high performance dual LDO capable of sourcing 100mA current from each output. It has a low standby current and very high PSRR and is stable with output capacitance of 1µF to 10µF with ESR of up to 200mΩ.

The device integrates an individual Power-On-Reset (POR) function for each output. The POR delay for VO2 can be externally programmed by connecting a timing capacitor to the CPOR pin. The POR delay for VO1 is internally fixed at approximately 2ms. A reference bypass pin is also provided for connecting a noise filtering capacitor for low noise and high-PSRR applications.

The quiescent current is typically only 42µA with both LDO's enabled and active. Separate enable pins control each individual LDO output. When both enable pins are low, the device is in shutdown, typically drawing less than 0.1µA.

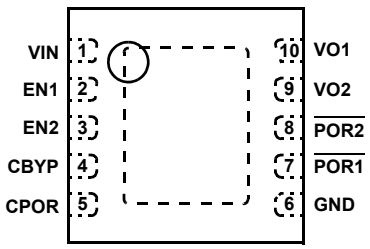
Output voltage for the LDO are VOUT1 = 3.3V and VOUT2 = 1.8V.

Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Logistics Agency (DLA). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

Pinout

ISL9000AMNCEP
(10 LD 3X3 DFN)
TOP VIEW



Features

- Integrates Two 100mA High Performance LDO's
- I_{OUT} per Channel is 50mA at T_J = +150°C
- Excellent Transient Response to Large Current Steps
- ±1.8% Accuracy Over all Operating Conditions
- Excellent Load Regulation:
  < 0.1% Voltage Change Across Full Range of Load Current
- Low Output Noise: Typically 30µV_{rms} @ 100µA (1.5V)
- Very High PSRR: 90dB @ 1kHz
- Extremely Low Quiescent Current: 42µA (both LDOs active)
- Wide Input Voltage Capability: 2.3V to 5.5V
- Low Dropout Voltage: Typically 200mV @ 100mA
- Stable with 1µF to 10µF Ceramic Capacitors
- Separate Enable and POR Pins for Each LDO
- Soft-Start and Staged Turn-On to Limit Input Current Surge During Enable
- Current Limit and Overheat Protection
- Tiny 10 Ld 3x3mm DFN Package
- -55°C to +125°C Operating Temperature Range

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices including Medical Handheld

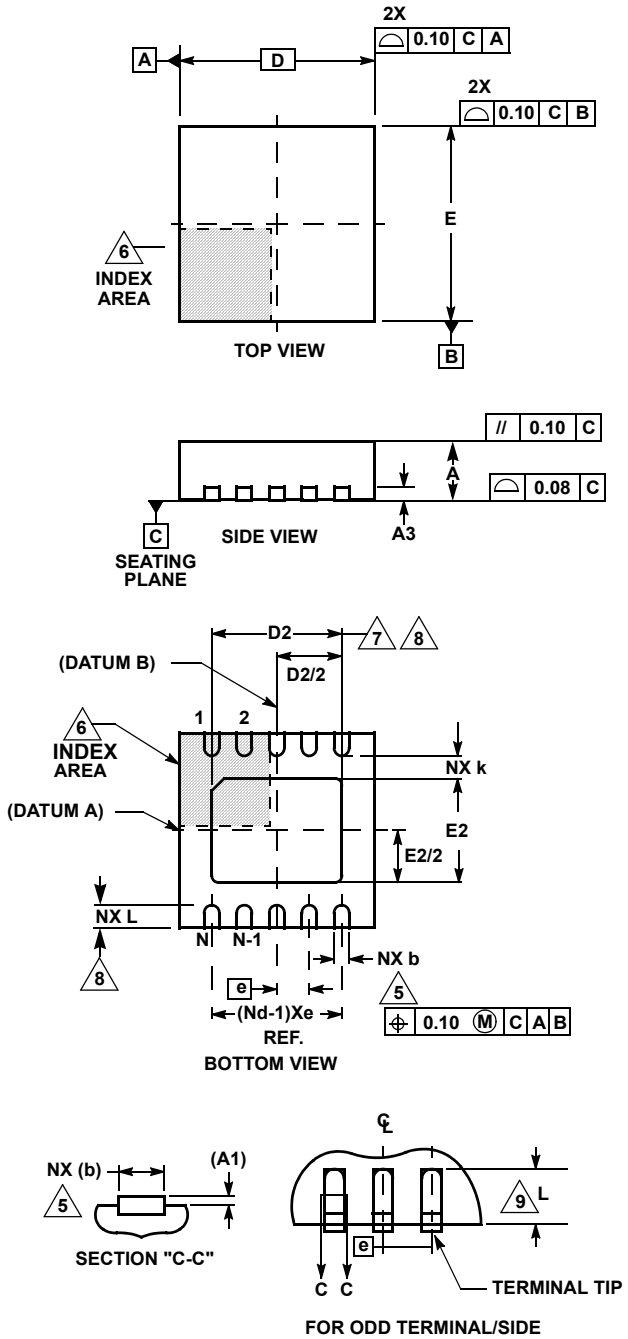
Ordering Information

VENDOR PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	VO1 VOLTAGE (V)	VO2 VOLTAGE (V)	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
ISL9000AMRNCEP	V62/08609-01XB	DKTA	3.3	1.8	-55 to +125	10 Ld 3x3 DFN	L10.3x3C

NOTES:

1. Add -T to part number for tape and reel.
2. Devices must be procured to the VENDOR PART NUMBER.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D		3.00 BSC		-
D2	2.33	2.38	2.43	7, 8
E		3.00 BSC		-
E2	1.59	1.64	1.69	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N		10		2
Nd		5		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.