RENESAS Low Latency High Bandwidth Memory(Low Latency DRAM family Gen.5th)

18 / 9Gb Common I/O x72 Burst Length of 2/4

3D-stacked DRAM for Networking & High-Performance Computing.

R10DS0281EJ0001
Rev.0.01
Jan 13,2019

The Low Latency – Dynamic random-access memory of 5th generation (RENESAS Low Latency DRAM V memory) is suited to networking & High-performance computing system solution that requires reduced random-access cycle (t_{RC}) memory which is, in general, called Low Latency High Bandwidth Memory (RENESAS Low Latency HBM). Low Latency HBM consists of multiple Low Latency DRAM memory (called slice) dies in 3D DRAM stack and base die at the bottom. Utilizing on those technology, Low Latency HBM achieves high random access and high bandwidth access and low power consumption with low input voltage.

In the case of 18Gbits capacity configuration1, Low Latency HBM consists of 8 memory dies and 1 base die, which is divided into 16 independent channels. Each channel is completely independent from other channels, and doesn't need to be synchronized with any of them. It has 72bits wide interface architecture with burst length of 2 operating at DDR data rate and reduced random access cycle t_{RC} operation architecture consisting of 16x2banks which compensates the number of t_{RC}/t_{CK}. Low Latency HBM also supports burst length of 4 operating (configuration2) and interface function like standard DRAM.

The Low Latency HBM provides two different configurations as for different types of Networking / High Performance Computing resource memory application. While configuration 1 supports 16Bytes/cycle data transfer rate as a maximum, configuration 2 can achieve up to 16x2Bytes/cycle data transfer rate.

Specification

- Configuration1:16-channel x72bits DDR architecture.
  8K WLs x144bits xCA [4:0] per a bank
- Configuration2: Pseudo 16-channel x72bits DDR
  8K WLs x288bits xCA [4:1] per a bank
  (1-channel has 2 pseudo channels)
- Density:18Gbits w/8 slice dies,16x2banks /a channel
  9Gbits w/8 slice dies, 8x2banks /a channel
  9Gbits w/4 slice dies,16x1banks /a channel
- Operating frequency
  1.0GHz
- Random Cycle t_{RC}
  12.0 ns / 16.0 ns t
- Command / Address bus 1/2 cycle DDR input.
- Differential clock inputs (CK_t/CK_c)
- One cycle command like SRAM command input.
- Burst Length: 2/4
- Power supply 2.5 V V_{pp}
  1.0 V V_{DDC}
  1.0 V / 1.2V V_{DDQ}
- Refresh command
  - Auto Refresh: 8192 cycles / 2 ms for each bank
- 10-year lifetime with 115° C junction temperature.

Table 1 Main features

Speed	tRC	Operating	Data Rate	Note
Configuration1 Burst Length2	12cycles (12.0ns)	1.0GHz (1.00ns)	2.0Gbps/pin	V_{DDQ} 1.0V
				V_{DDQ} 1.2V
Configuration2 Burst Length 4	16cycles (16.0ns)	1.0GHz (1.00ns)	2.0Gbps/pin	V_{DDQ} 1.0V
				V_{DDQ} 1.2V

Notes. Configuration 1/2 are categorized from difference of μBUMP footprint assignment (transfer data size).
Notes. Do not stop CK* toggling after power-up in all channels. And Keep frequency at 1GHz.
Notes. There are two products for V_{DDQ} 1.0 V nominal product and V_{DDQ} 1.2 V nominal product

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1. Overview

Low Latency DRAM of 5th generation (Low Latency DRAM V) is, like as Low Latency DRAM II / III / IV (product family), a high-performance DRAM chip targeting on such applications that require high bandwidth and moderately small burst length of random accesses onto a high capacity DRAM memory. The primary design emphasis is on high command access rate and small granularity data size with high random accesses and low power, and the secondary emphasis is on high bandwidth for network / compute resource and work memory. Especially, “random accesses “is defined as t_{RC} in specifications. Low Latency HBM is stacked with multiple dies made of Low Latency DRAM technologies archiving short t_{RC} DRAM array core architecture.

Low Latency HBM has two type interface footprints defined in two configurations. Configuration1 mainly focuses on Control/Table/Cache memory application (BL2/16Bytes data size), having 16 channels. And, Configuration 2 focuses on Buffer memory application (BL4/32Bytes data size) in network system, having 16 pseudo channels. Low Latency HBM would cover variable next generation applications, and adapt suitable functions to networking / High performance computing system.

Features Configuration 1 and 2

- BL = 2 / 4 with 72bits DQ width (16Bytes data size) per a channel (a Pseudo channel).
- 8192 words, 144I/O (x72bits, DDR), 32 pages per a bank (=36M).
- The Low Latency HBM consists of 8/4 memory (slice) dies and one logic (base) die.
- Differential clock inputs (CK_t/CK_c) toggling after power-up in all channels (Keep frequency at 1GHz).
- DDR commands entered on each positive CK_t, CK_c edge. Main commands are single cycle input.
- Semi-independent Row & Column Command Interfaces allowing Activates / Precharges function to be issued in parallel with Reads/Writes.
- Data referenced to strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c.
- Up to 16 channels per stack in case of configuration1. Pseudo 16 channels per stack in case of configuration2.
- 16x2banks per channel w/8 slice dies (upper 16banks and lower 16banks are selected by SID) in 18Gbits product case.
  8x2banks per channel w/8 slice dies or 16banks per channel w/4 slice dies in 9Gbits product case.
- DBIac support configurable via MRS
- IO voltage 1.0 V / 1.2V
- DRAM core voltage 1.0 V, independent of IO voltage 1.0V / 1.2V
- Unterminated data/address/cmd/clk interfaces
- Temperature sensor

Table 2 Features configuration 1 and 2

	Configuration1			Configuration2		
Density / Die [Gb]	2.3	1.1	2.3	2.3	1.1	2.3
Memory Stack	8		4	8		4
Total Memory[Gb]	18	9	9	18	9	9
Clock Freq.[GHz]	1.0		1.0	1.0		1.0
tRC[ns]	12.0		12.0	16.0		16.0
Activation command [Cyc.]	1		1	1		1
Burst Length	2		2	4		4
# Ch.	16		16	Pseudo 16		Pseudo 16
#Bank / Ch.	16x2	8x2	16	16x2	8x2	16
#I/O / Ch. Data size	72bits DDR 16Bytes x(BL/2).		72bits DDR 16Bytes x(BL/2).	72bits DDR 16Bytes x(BL/2)		72bits DDR 16Bytes x(BL/2)
Total #I/O	1,152		1,152	1,152		1,152
Peak B/W [Gbps]	2,304		2,304	2,304		2,304
Access Rate [Maps]	16,000		16,000	8,000		8,000

Notes. 8slice dies product has upper 16banks and lower 16banks selected by SID.4slice dies product has only lower 16banks.
Notes. There are two products for V_{DDQ} 1.0 V nominal product and V_{DDQ} 1.2 V nominal product
Notes. In case of 18Gbits product, a bank is selected by bank address of BA [3:0] and SID. In case of 9Gbits product, BA3 or SID do not be used depending on 8 slice dies stack or 4 slice dies stack.

2. Electrical Specifications

Power supplies and DC Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{PP}	2.5 V nominal	–0.3 to +2.8	V
Supply voltage	V_{DDC}	1.0 V nominal	–0.3 to +1.26	V
Output supply voltage, Input voltage, Input / Output voltage	V_{DDQ}	V_{DDQ} 1.0 V nominal V_{DDQ} 1.2 V nominal	–0.3 to +1.26 –0.3 to +1.50	V V
Input / Output voltage	V_{IH} / V_{IL}	V_{DDQ} 1.0 V V_{DDQ} 1.2 V	–0.3 to +1.26 –0.3 to +1.50	V
Junction temperature	T_J		0 to +125	°C
Storage temperature	T_{STG}		–55 to +125	°C

Notes. There are two products for V_{DDQ} 1.0 V nominal product and V_{DDQ} 1.2 V nominal product

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 4 Recommended DC Operating Conditions 0°C ≤ T_J ≤ 115°C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Comments	Note
Supply voltage	V_{PP}	2.375	2.5	2.625	V		1,2
Supply voltage	V_{DDC}	0.950	1.0	1.050	V		1,2
Output supply voltage	V_{DDQ}	0.950 1.140	1.0 1.2	1.050 1.260	V	V_{DDQ} 1.0 V nominal V_{DDQ} 1.2 V nominal	1,2
High level output voltage	$V_{OH\ (DC)}$	V_{DDQ}*0.7			V		1,2
Low level output voltage	$V_{OL\ (DC)}$			V_{DDQ}*0.3	V		1,2
High level input voltage	$V_{IH\ (DC)}$	V_{DDQ}*0.7			V		1,2
Low level input voltage	$V_{IL\ (DC)}$			V_{DDQ}*0.3	V		1,2
Differential input crossing voltage	V_{IX}	V_{DDQ}*0.5-0.1		V_{DDQ}*0.5+0.1	V		1,2
Driver strength Forcing VDDQ/2 voltage.	I_{OH}, I_{OL}				mA mA mA mA mA		1,2

Notes. There are two products for V_{DDQ} 1.0 V nominal product and V_{DDQ} 1.2 V nominal product

Notes. All voltage referenced to V_{SS} (GND) at μBUMP

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3. Package pins.

Table 5 Signals in Identification

Symbol	Direction	I/O Type	Freq [MHz]	Description
CK[a:*]_t CK[a:*]_c	Input	1.0V / 1.2V	1000	Clock inputs: CK_t and CK_c are differential clock inputs. This input clock pair registers address and control inputs on the rising edge of CK_t. CK_c is ideally 180 degrees out of phase with CK_t. Don't stop CK* toggling and change frequency after power-up in all channels (Stable CK* toggling must start at power on sequence).
CKE[a:*]	Input	1.0V / 1.2V	-	**Always CKE HIGH activates after Power UP.** CKE must be maintained HIGH throughout read and write accesses, because of adapting I/O control. Refer to CKE session in detail about CKE usage for LOOP BACK.
RESET_n	Input	1.0V / 1.2V	-	Master reset:
C[a:*]0-C[a:*]7	Input	1.0V / 1.2V	1000	Column Command and Address inputs for each command. Address inputs, including bank select bits and parity bits.
R[a:*]0-R[a:*]8	Input	1.0V / 1.2V	1000	Row Command and Address inputs for each command. Address inputs, including bank select bits and parity bits.
WDQS[a:*]0_t -WDQS[a:*]1_t, WDQS[a:*]0_c -WDQS[a:*]1_c	Input	1.0V / 1.2V	1000	Write data strobe for DQ and DBI inputs: WDQSx0 => DQx0-DQx31,DQx64-DQx67,DBIx0-DBIx3 WDQSx1 => DQx32-DQx63,DQx68-DQx71,DBIx4-DBIx7
RDQS[a:*]0_t -RDQS[a:*]1_t, RDQS[a:*]0_c -RDQS[a:*]1_c	Output	1.0V / 1.2V	1000	Read data strobe for DQ and DBI outputs: RDQSx0 => DQx0-DQx31,DQx64-DQx67,DBIx0-DBIx3 RDQSx1 => DQx32-DQx63,DQx68-DQx71,DBIx4-DBIx7
DQ[a:*]0 -DQ[a:*]71	Input /Output	1.0V / 1.2V	1000	Data input/output: Data size 16Bytes configuration on x72 parts The DQ signals form the 72bits data bus for 16channel or pseudo 16channel mode. During READ commands, the data is referenced to both edges of RDQSx. During WRITE commands, the data is sampled at both edges of WDQSx.
DBI[a:*]0 -DBI[a:*]7	Input /Output	1.0V / 1.2V	1000	Data inversion state for DQ inputs: EVEN Byte DQ group DBIx0 => DQx0-DQx7 ,DQx64 DBIx4=>DQx32-DQx39 ,DQx68 DBIx2 => DQx16-DQx23,DQx66 DBIx6=>DQx48-DQx55 ,DQx70 ODD Byte DQ group DBIx1 => DQx8-DQx15 ,DQx65 DBIx5=>DQx40-DQx47 ,DQx69 DBIx3 => DQx24-DQx31,DQx67 DBIx7=>DQx56-DQx63 ,DQx71

Notes. Input pin has no on-die termination.

Notes. DWORD of Pseudo 16Ch. [a0:h0, a1:h1] (configuration2) / 16Ch. [a: p] (configuration1).

Notes. AWORD of 8Ch. [a; h] (configuration2), / 16Ch. [a; p] (configuration1)
[a:*] = [a0:h0, a1:h1] (configuration2) , [a:*] = [a: p] (configuration1)

Notes. There are two products for V_{DDQ} 1.0 V nominal product and V_{DDQ} 1.2 V nominal product

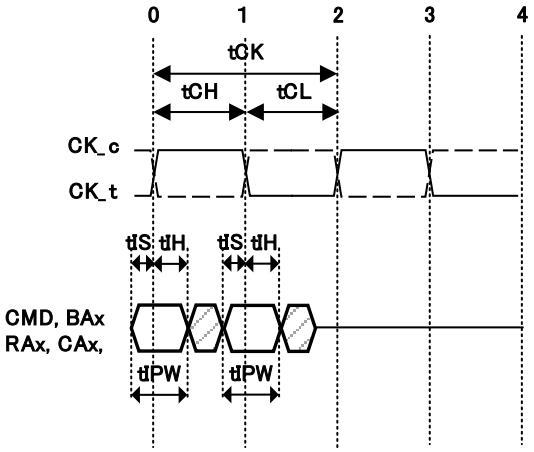
Notes. "x" means some suffix of channel. In this datasheet, this "x" is often omitted.

4. Interface AC Characteristics

Normal bus timing

Standard bus timing waveforms and values for command and data are shown in Figure 1 and Interface AC Parameters in Table 6. All timing is measured to/from the crossing point on differential clocks and to/from the half voltage crossing point on single-ended signals.

(1) Command /Address bus timing



Notes 1. tIS/tIH is defined in each CK_t/c edge (Rise) / CK_c/t edge (Fall).

Figure 1 DDR Command / Address (R[x], C[x] including BAx, RAx, CAx) Input Timing Waveforms

Table 6 Interface AC Parameters; command inputs

Parameter	Symbol f_{CK}	– (1.0GHz)		Unit	Note
		MIN.	MAX.		
CK clock period (maximum 1000 MHz clock frequency, minimum 500MHz)	t_{CK}			ns	
CK_t/_c LOW time	t_{CL}			t_{CK}	
CK_t/_c HIGH time	t_{CH}			t_{CK}	
Clock period jitter	t_{JIT}(per)			ns	1
Cycle-to-cycle clock jitter	t_{JIT}(cc)			ns	
CK_t/_c to Input signal pin setup	t_{IS}			ns	2
CK_t/_c to Input signal pin hold	t_{IH}			ns	2
Input signal pin pulse width	t_{IPW}			ns	

Notes 1. Frequency drift is not allowed.
Notes 2. Total t_{IS} / t_{IH} for V_{DDQ}/2 crosspoint need to add Δt_{IS} /Δt_{IH} derating value in **Table 10** to this t_{IS} / t_{IH} value.

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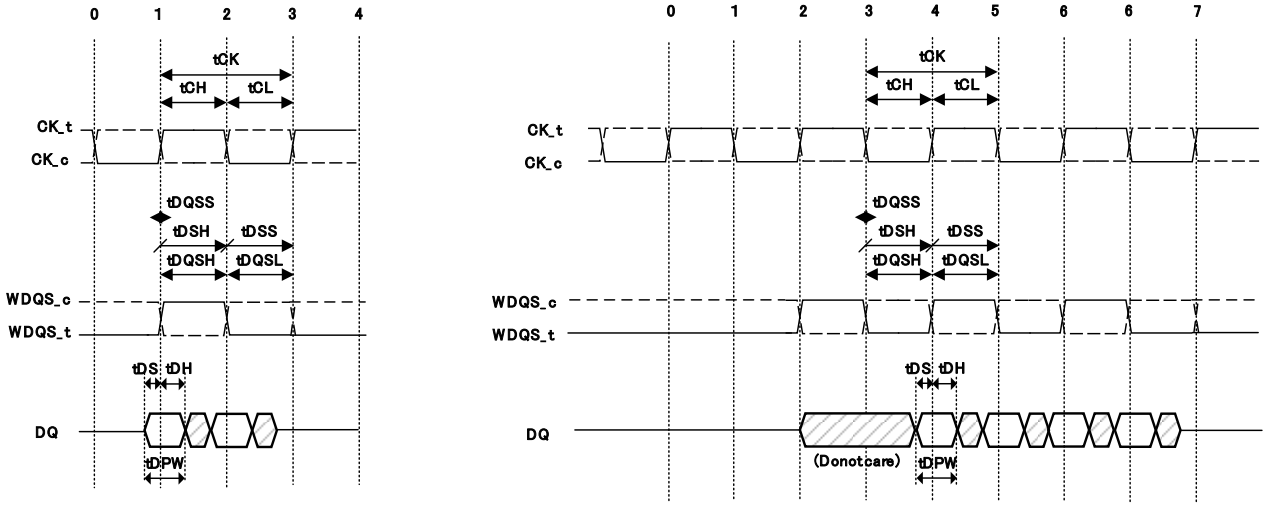
(2) Definition of Data Input / output Timing Waveforms

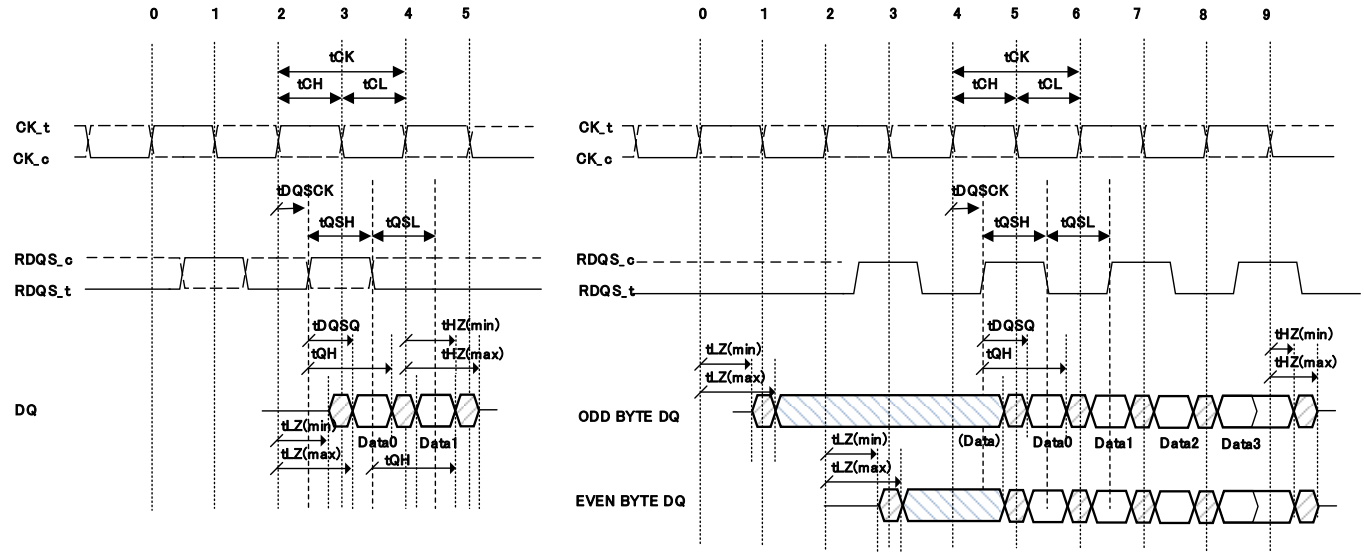
Figure 2 shows “Data Input Timing Waveforms”. Figure 3 shows “Data Output Timing Waveforms”. Low Latency HBM has 2 modes [mode1 , mode2] for preamble setting and postamble setting(Table 7). Table 8 shows DQ Byte group assignment.

Unless necessary, this DATASHEET is described in using configuration1 mode1.



(a) Configuration1 BL2 [mode1] **(b) Configuration2 BL4 [mode2]**

Figure 2 Data Input Timing Waveforms



(a) Configuration1 BL2 [mode1] **(b) Configuration2 BL4 [mode2]**

Notes. (Data) output is data of previous read command or low data in the case of first read command.
Notes. Data3 output is half cycle longer in the configuration2 BL4 [mode2]
Notes. Refer to Table 5 or Table 8 about Byte DQ assignment

Figure 3 Data Output Timing Waveforms

Table 7 Preamble setting and Postamble setting abut cycle number# [tCK].

	Configuration 1 [mode1]		Configuration 2[mode2]	
[tCK]	**Preamble**	**Postamble**	**Preamble**	**Postamble**
WRITE (WDQS)	0	0	1	0
READ (RDQS)	1	0	1	1

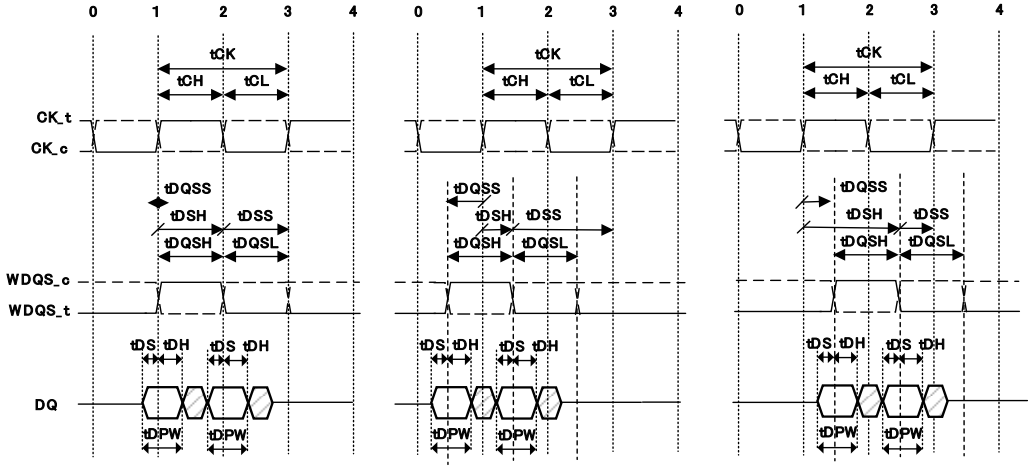
Table 8 DQ group assignment.

DQ	Byte Group
DQx [7:0], DQx64	Even Byte
DQx [15:8], DQx65	Odd Byte
DQx [23:16], DQx66	Even Byte
DQx [31:24], DQx67	Odd Byte
DQx [39:32], DQx68	Even Byte
DQx [47:40], DQx69	Odd Byte
DQx [55:48], DQx70	Even Byte
DQx [63:56], DQx71	Odd Byte

Notes. DWORD of Pseudo 16Ch. [a:p]=[a0:h0, a1:h1] (configuration2) / 16Ch. [a:p](configuration1).

(3) Definition of Data Input / output Timing Specification

Standard bus timing waveforms and values for data are shown in Figure 4 and Figure 5. Figure 4 shows three cases of Data Input Timing Waveforms for tDQSS (0/-/+). Figure 5 shows Data Output Timing Waveforms.



Notes. tDS/tDH is defined in each WDQS_t/c edge (Rise) / WDQS_c/t(Fall).

Figure 4 Data Input Timing Specification for tDQSS (0/-/+)

Table 9 Interface AC Parameters; Data input

Parameter	Symbol f_{CK}	– (1.0GHz)		Unit	Note
		MIN.	MAX.		
WDQS_t (rising edge) to CK_t skew (rising edge)	t_{DQSS}			t_{CK}	
WDQS_t/_c LOW time	t_{DQSL}			t_{CK}	
WDQS_t/_c HIGH time	t_{DQSH}			t_{CK}	
WDQS_t (falling edge) to CK_t (rising edge) setup time	t_{DSS}			t_{CK}	
WDQS_t (falling edge) from CK_t (rising edge) hold time	t_{DSH}			t_{CK}	
DQ, DBI to WDQS_t/WDQS_c(rising or falling edge) setup time	t_{DS}			ns	1
WDQS_t/WDQS_c(rising or falling edge) to DQ, DBI hold time	t_{DH}			ns	1
DQ, DBI input pulse width	t_{DPW}			ns	

Notes. Total t_{DS} / t_{DH} for V_{DDQ}/2 crosspoint need to add Δt_{DS} /Δt_{DH} derating value in **Table 10** to this t_{DS} / t_{DH} value.

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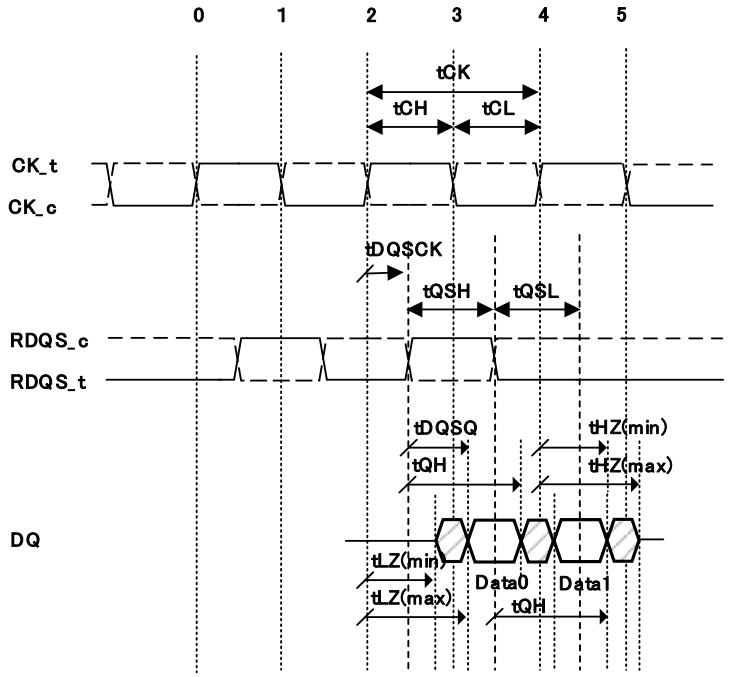
Table 10 Delating value for Δt_{IS} /Δt_{IH} or Δt_{DS} /Δt_{DH}

Slew rate [V/ns]	Setup	Hold	Unit
2			ps
3			ps
4			ps
5			ps
6			ps
7			ps
8			ps
9			ps
10			ps



Notes. RDQS_t/_c need clocking of 1cycle as preamble term before output of DQ data.

Figure 5 Data Output Timing Specification

Table 11 Interface AC Parameters; Data output

Parameter	Symbol f_{CK}	– (1.0GHz)		Unit	Note
		MIN.	MAX.		
RDQS_t/_c LOW time	t_{QSL}			t_{CK}	
RDQS_t/_c HIGH time	t_{QSH}			t_{CK}	
CK to RDQS_t/_c skew	t_{DQSCK}			ns	
RDQS_t/_c to DQ, DBI skew	t_{DQSQ}			ns	
DQ, DBI hold time from RDQS_t/_c	t_{QH}			t_{CK}	
CK_t/_c to DQ output driver turn-on time	t_{LZ}			ns	
CK_t/_c to DQ output driver turn-off time	t_{HZ}			ns	

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Table 12 Interface AC Parameters; chip specifications

Parameter		Symbol f_{CK}	– (1.0GHz)		Unit	Note
			MIN.	MAX.		
ACTIVATE command to same bank Activate command. Row Cycle time. Single bank refresh Cycle time.	BL2 BL4	t_{RC}	12 16		t_{CK} t_{CK}	1
ACTIVATE command (w/ Read command; ACT w/RD) to Precharge command (PRE), Same bank	BL2 BL4	t_{RAS}			t_{CK} / µs t_{CK} / µs	2
Precharge command (PRE) to ACTIVATE command Same bank	BL2 BL4	t_{RP}			t_{CK} t_{CK}	
ACTIVATE command to different bank Activate command Single Bank refresh command is same definition.	BL2 BL4	t_{RRD}			t_{CK} t_{CK}	4
Read w/o AP command to different bank Read command	BL2 BL4	t_{CCD1}			t_{CK} t_{CK}	3
Read w/o AP command to same bank Read command	BL2 BL4	t_{CCD2}			t_{CK} t_{CK}	3
Read w/o AP command to Precharge command(PRE)	BL2 BL4	t_{RTP}			t_{CK} t_{CK}	3
Read command Latency (data output delay) V_{DDQ} 1.0 V nominal product	BL2 BL4	t_{RL}			t_{CK} t_{CK}	9
Write command Latency (data input delay) V_{DDQ} 1.0 V nominal product	BL2 BL4	t_{WL}			t_{CK} t_{CK}	9
Read command to Write Command Delay V_{DDQ} 1.0 V nominal product	BL2 BL4	t_{RWD}			t_{CK} t_{CK}	
Write command to Read Command Delay V_{DDQ} 1.0 V nominal product	BL2 BL4	t_{WRD}			t_{CK} t_{CK}	
REFRESH command to same bank REFRESH command. tRFC=tRC	BL2 BL4	t_{RFC}			t_{CK} t_{CK}	5
Read command to different SID Read command	BL2 BL4	t_{CCDR}			t_{CK} t_{CK}	6
Max Activate Count w/ Read	-	MACR			-	7
Read command Latency (data output delay) V_{DDQ} 1.2 V nominal product	BL2 BL4	t_{RL}			t_{CK} t_{CK}	8,9
Write command Latency (data input delay) V_{DDQ} 1.2 V nominal product	BL2 BL4	t_{WL}			t_{CK} t_{CK}	8,9
Read command to Write Command Delay V_{DDQ} 1.2 V nominal product	BL2 BL4	t_{RWD}			t_{CK} t_{CK}	8
Write command to Read Command Delay V_{DDQ} 1.2 V nominal product	BL2 BL4	t_{WRD}			t_{CK} t_{CK}	8

Notes 1. This command is SRAM like command that operates row activate command w/ Read/Write command (tRCD=0). So, activate command w/o Read/Write command is not supported. And, activate command w/ another bank Read/Write command is not supported.
tRC is minimum value in the case of Write/Read command w/ Auto precharge (w/AP).

Notes 2. Do not use Precharge command after Activate command with Auto precharge Read command / Write command (ACT w/RDA, ACT w/WRA) for any bank. These commands reserve precharge command(PRE), automatically.

Notes 3. Write w/o AP command is not supported.

Notes 4. Single Bank refresh at each bank. Command to Command delay definition is as same as tRRD.

Notes 5. There are some limitations regarding optional refresh modes. Refer to those sessions.

Notes 6. Including Activate command w/ Read command. tCCDR=tCCD1+1tCK.

Notes 7. Maximum bank numbers of open bank by ACT w/RD command.

Notes 8. These specifications of V_{DDQ} 1.2 V nominal product are different from those of V_{DDQ} 1.0 V nominal product.

Notes 9. The specification of Read/Write Latency is constant value (t_{CK}) depending on configuration and V_{DDQ}.

5. Operation

5.1. Interface Overview

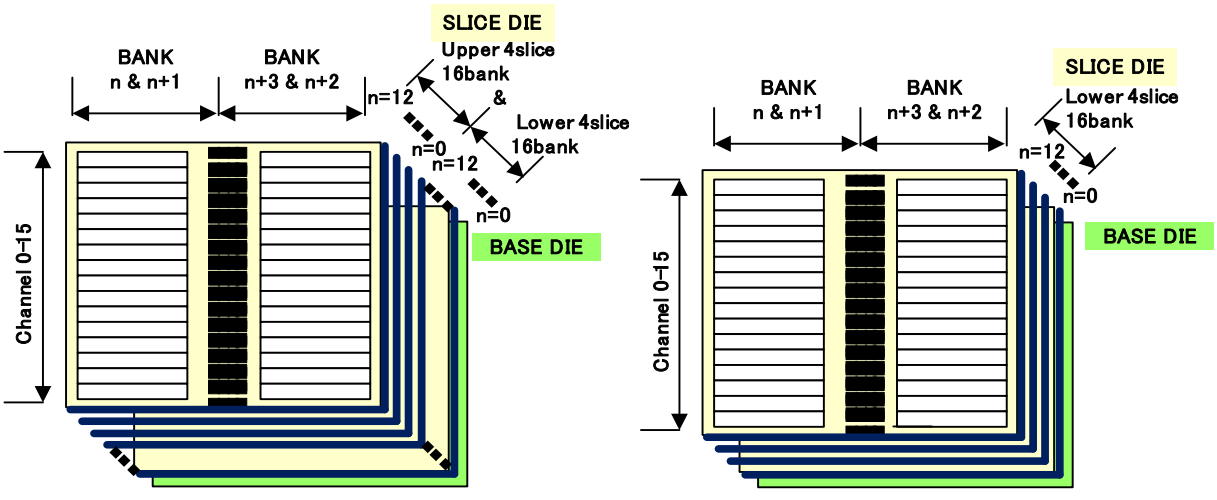
The primary Low Latency HBM interface consists of a unidirectional command and address bus and a bidirectional data bus. This type of data bus is often referred to as common I/O or CIO. Pin Identification contains the list of pins on the Low Latency HBM.

The command and address bus are a double data rate (DDR) bus consisting of R[x], C[x]. Both the command bus and address bus are clocked by the differential clock pair CK_t and CK_c. READ and WRITE commands can be issued at a rate of every single cycles of CK in burst length 2 and 4 mode.

The data interface is a double-rate (DDR) interface that transfers 72bits of data [Note] on each clock edge for 72bits parts and 144bits of data (Pseudo 2channels x 72bits) on each clock edge for 144 bits parts. The data interface also includes 4 data inversion pins. The Low Latency HBM outputs one differential clock pairs, RDQS_t and RDQS_c that are associated with read data. Because the data bus is bidirectional, idle cycles are required to implement data bus turn-around as described in 5.10. Data bus turn-around.

This interface is called a channel. Low Latency HBM has 16 / Pseudo16 channels (8 channels) independently in each configartion1/2. Those channels consist of multiple DRAM dies called as SLICE die and BASE die. For example, 18Gbits Low Latency HBM is containing 8DRAM SLICE dies and 1 BASE die. 4Gbits one has 4DRAM SLICE dies. One SLICE die has 16channels w/ 2banks or 4banks for each case. Figure 6 shows those.

Note For parts with 72bits data bus (configuration1), all references in this section should refer to DQ0-DQ71 and DBI0-7 unless otherwise noted in each channel. And, configuration2 uses 2channle parts of configuration1. So, for parts with 144bits data bus, all references in this section should refer to DQ0-DQ71 and DBI0-7 through 2channels unless otherwise noted in each channel.



(a) 8 slices dies stacked (b) 4 slice dies stacked

Notes. The assignment of channels and banks can physically change in the product revision. This figure is just image.

Notes. Channel0-15 are indicated by suffix [a:p] in the case of configuration1.

Notes. 18/9Gbits with 8slice dies product has upper and lower banks (16/8) selected by SID.4slice dies product has only lower 16banks.

Figure 6 over view of DRAM dies stacked with slice dies and base die

5.2. Clocking

There are three groups of clock signals: CK_t/CK_c, WDQS_t/WDQS_c, and RDQS_t /RDQS_c.

The CK_t/CK_c clock is associated with the address and command pins: R[x], C[x]. At the Low Latency HBM pins, the CK_t/CK_c transitions are nominally centered with respect to address and command signal transitions.

The WDQS_t/WDQS_c clocks are associated with write data. WDQS_t/WDQS_c clocks are used as a source-centered clock for the double data rate DQ0-DQ71, DBI0-DBI7.

The WDQS_t/WDQS_c clocks must meet the specified t_{DQSS} skew with respect to the CK_t/CK_c clock to ensure proper timing relationship between command and data cycles and to enable proper data bus turn-around.

The RDQS_t/RDQS_c clocks are associated with read data. At the Low Latency HBM pins, and for x72 devices, RDQS_t/RDQS_c clocks must be source-synchronous with the read data DQ0-DQ71, DBI0-DBI7 pins.

The RDQS_t/RDQS_c clocks must meet the specified t_{DQSCK} skew with respect to the CK_t/CK_c clock to ensure proper timing relationship between command and data cycles and to enable proper data bus turn-around.

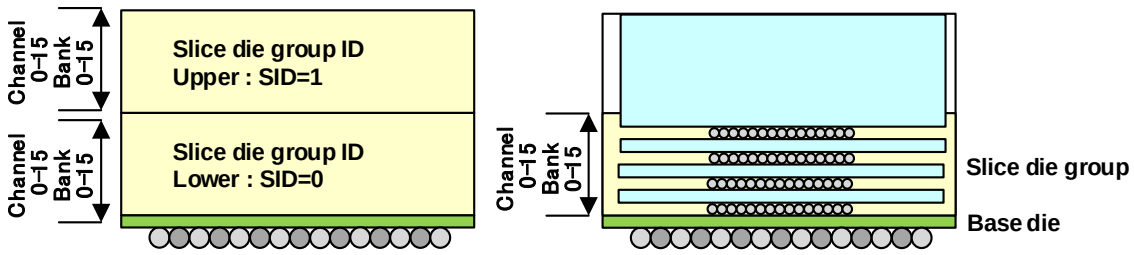
5.3. Addressing

Table 13 channel addressing

	Configuration1			Configuration2		
Product density	18Gbits	9Gbits	9Gbits	18Gbits	9Gbits	9Gbits
Memory Stack	8		4	8		4
Configuration	1			2		
# Ch.	16			Pseudo 16		
Access data size	72bits x BL2			72bits x BL4		
Row address Size	RA[12:0] 8K			RA[12:0] 8K		
Col address Size	CA[4:0] 32			CA[4:1] 16		
Bank address	BA[3:0],	BA[2:0] (BA3=0)	BA[3:0]	BA[3:0]	BA[2:0] (BA3=0)	BA[3:0]
	SID		(SID=0)	SID		(SID=0)
Size	16x2	8x2	16	16x2	8x2	16
Page size	4608 144IOx32		4608 144IOx32	4608 288IOx16		4608 288IOx16
Refresh / a bank	8K/2ms			8K/2ms		

Notes. 10-year lifetime with 115°C junction temperature.

Notes. SID means “Slice die group ID” showed by following figure.



(a) 8slice dies product. SID=0/1 **(b) 4slice dies product.** (SID=0)

Notes. 18/9Gbits with 8slice dies product has upper and lower banks (16/8) selected by SID.4slice dies product has only lower 16banks.

5.4. Command and Address bus

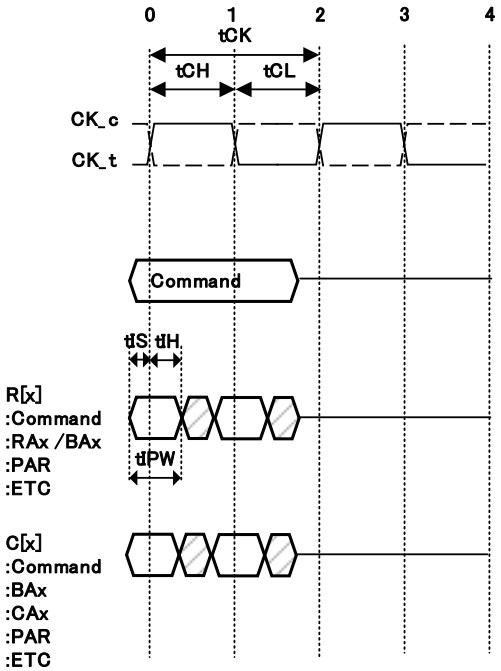
In Burst of 2/4 mode one clock cycle is required to load the multiplexed command and address. In DDR Command and Address mode command and address inputs are captured by the RAM in two beats per cycle. Two of the bits in the command and address field select which of the banks in the RAM will be accessed. The bit functions as an ordinary command and address bits in the devices described in this data sheet.

Table 14 single cycle row/col command and address assignment example (bit encoding; BT0-1).

Row command/address (CMD/BAx, RAx)		
Activate	Rising (BT0)	Falling(BT1)
R[8]	L	RA13/L
R[7]	RA12	RA6
R[6]	RA11	RA5
R[5]	RA10	RA4
R[4]	RA9	RA3
R[3]	RA8	RA2
R[2]	RA7	PAR
R[1]	Command	RA1
R[0]	Command	RA0

Col command/address (CMD/BAx, CAx)		
Read / Write	Rising (BT0)	Falling(BT1)
C[7]	PCS/V	V
C[6]	SID/V	Command
C[5]	BA3/V	CA4
C[4]	BA2	CA3
C[3]	BA1	CA2
C[2]	BA0	PAR
C[1]	Command	CA1
C[0]	Command	CA0/V

Notes. CA0 for BL2. CA0 don't care at BL4.
Notes. V means Valid Signal (either H or L, but not floating)
Notes. Following session exactly shows command encoding table in detail.



Notes. Edge of BT0 is rising edge of command clock (CK). Edge of BT1 is falling edge of command clock (CK).
Notes. tIS/tIH is defined in each CK_t/c edge (Rise/Fall) / CK_t/c(Fall/Rise).

Figure 7 DDR Command / Address (R[x], C[x] including BAx, RAx, CAx) Input Timing Waveforms

5.5. Command encoding

The Low Latency HBM supports standard 9 types of command. The 4 types of command are Row commands as shown in Table 15 and Figure 8. The 5 types of command are Col commands as shown in Table 16 and Figure 9**.**

Table 15 Over view of Row commands

Function	Sym.	Clock Edge	R[0]	R[1]	R[2]	R[3]	R[4]	R[5]	R[6]	R[7]	R[8]
Row NO operation	RNOP	Rising	H	H	V	V	V	V	V	V	L
		Falling	V	V	PAR	V	V	V	V	V	L
Activate w/RD, RDA,or WRA.	ACT	Rising	L	H	RA7	RA8	RA9	RA10	RA11	RA12	L
		Falling	RA0	RA1	PAR	RA2	RA3	RA4	RA5	RA6	RA13/L
Precharge	PRE	Rising	H	L	BA0	BA1	BA2	BA3/V	SID/V	PCS/V	L
		Falling	V	V	PAR	V	V	V	V	V	L
Refresh Single Bank	REF	Rising	L	L	BA0	BA1	BA2	BA3/V	SID/V	PCS/V	L
		Falling	V	V	PAR	V	V	V	V	V	L

Notes. CKE = H (CKE should be LOW preventing for illegal commands at initialization.)

Notes. Active command needs col commands (write / read commands) referring to BA [0:3], SID, PCS of Col commands

Notes. RA13 is only used at 36Gbits configuration in future. And R [8] bit can be reserved pin and must be set 0.

Notes. Bank open for COL operation needs “ACT commands”

Notes. Use PCS at pseudo channel mode (Burst length 4).

Notes. Configuration2 is double data size of Configuration1 divided by PCS.

Notes. Use SID at 8slice dies product due to choose lower or upper four slice dies. (SID=0 recommended when 4slice dies product. BA3=0 recommended when BA3 do not be used).

Notes. Parity is calculated on all pins of each command when the parity function is enabled in the mode register.

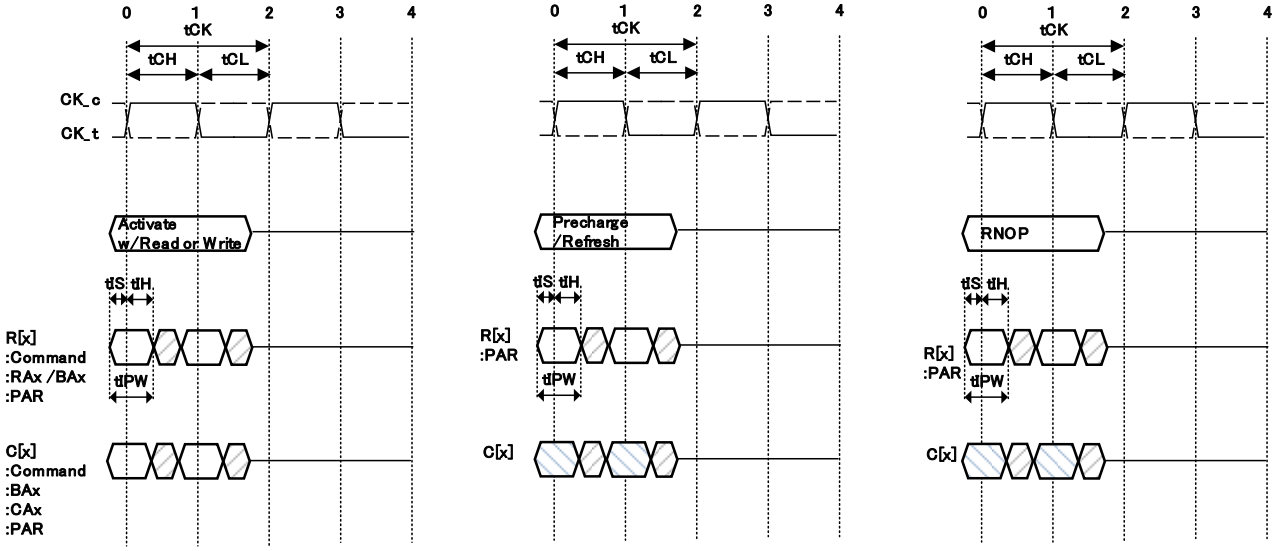


Figure 8 DDR Command / Address (R[x], C[x] including BAx, RAx, CAx) Input Timing Waveforms

- ✓ The two types of NO OPERATION (NOP) command (RNOP, CNOP) must be used on any cycle where no other commands are requested.
- ✓ The ACTIVATE (ACT) command is used to initiate an activate operation of a single bank, but this command needs read command or write command as same timing.
- ✓ The PRECHARGE (PRE) command is used to initiate a precharge operation on a particular bank of the memory.
- ✓ The REF command is used to initiate a refresh operation on a particular bank of the memory.

Table 16 Over view of Col commands

Function	Sym.	Clock Edge	C[0]	C[1]	C[2]	C[3]	C[4]	C[5]	C[6]	C[7]
Column NO Operation	CNOP	Rising	H	H	V	V	V	V	V	V
		Falling	V	V	PAR	V	V	V	V	V
Read	RD	Rising	H	L	BA0	BA1	BA2	BA3/V	SID/V	PCS/V
		Falling	CA0/V	CA1	PAR	CA2	CA3	CA4	L	V
Read w/ AP	RDA	Rising	H	L	BA0	BA1	BA2	BA3/V	SID/V	PCS/V
		Falling	CA0/V	CA1	PAR	CA2	CA3	CA4	H	V
Write w/ AP	WRA	Rising	L	H	BA0	BA1	BA2	BA3/V	SID/V	PCS/V
		Falling	CA0/V	CA1	PAR	CA2	CA3	CA4	H	L
Mode Register set	MRS	Rising	L	L	H	OP6	OP7	MRA0	MRA1	V
		Falling	OP0	OP1	PAR	OP2	OP3	OP4	OP5	V

Notes. CKE = H (CKE should be LOW preventing for illegal commands at initialization.)
Notes. Use PCS at pseudo channel mode (Burst length 4).
Notes. MRA [1:0] and OP [7:0] are showed in detail by Configuration session.
Notes. CA0 for BL2 (Burst length2). CA0 don't care BL4 (Burst length 4).
Notes. 18/9Gbits with 8slice dies product has upper and lower banks (16/8) selected by SID.4slice dies product has only lower 16banks. SID/BA3=0 fixed is each recommended when not to use.
Notes. Parity is calculated on all pins of each command when the parity function is enabled in the mode register.
Notes. The WRITE (WR) command is not used to initiate a burst write. This command is not permitted.

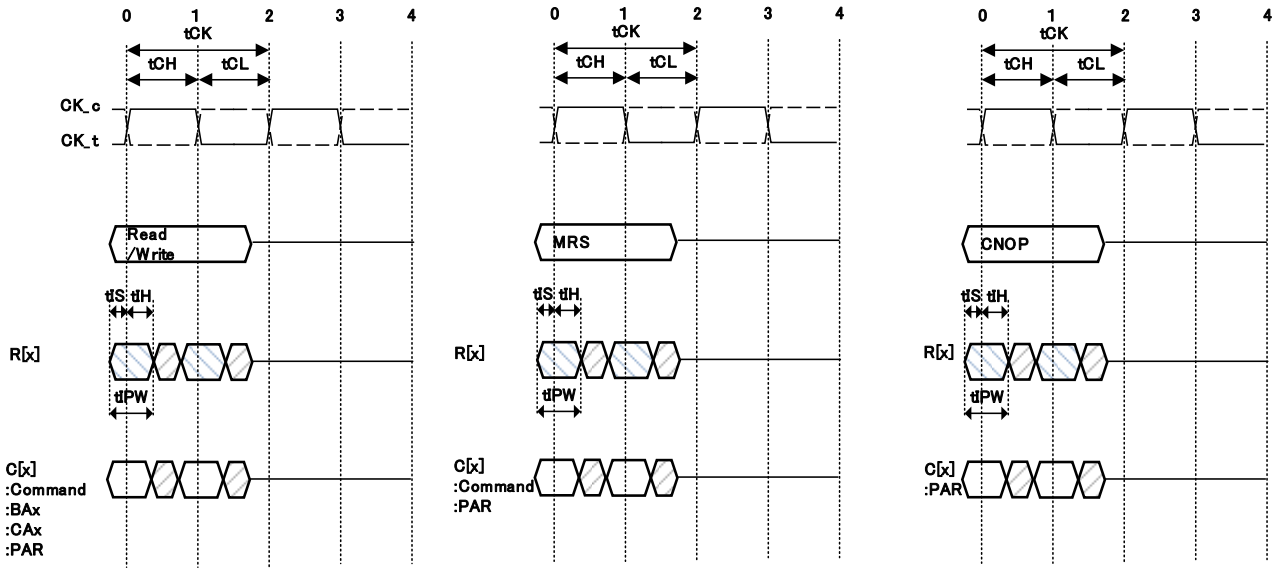


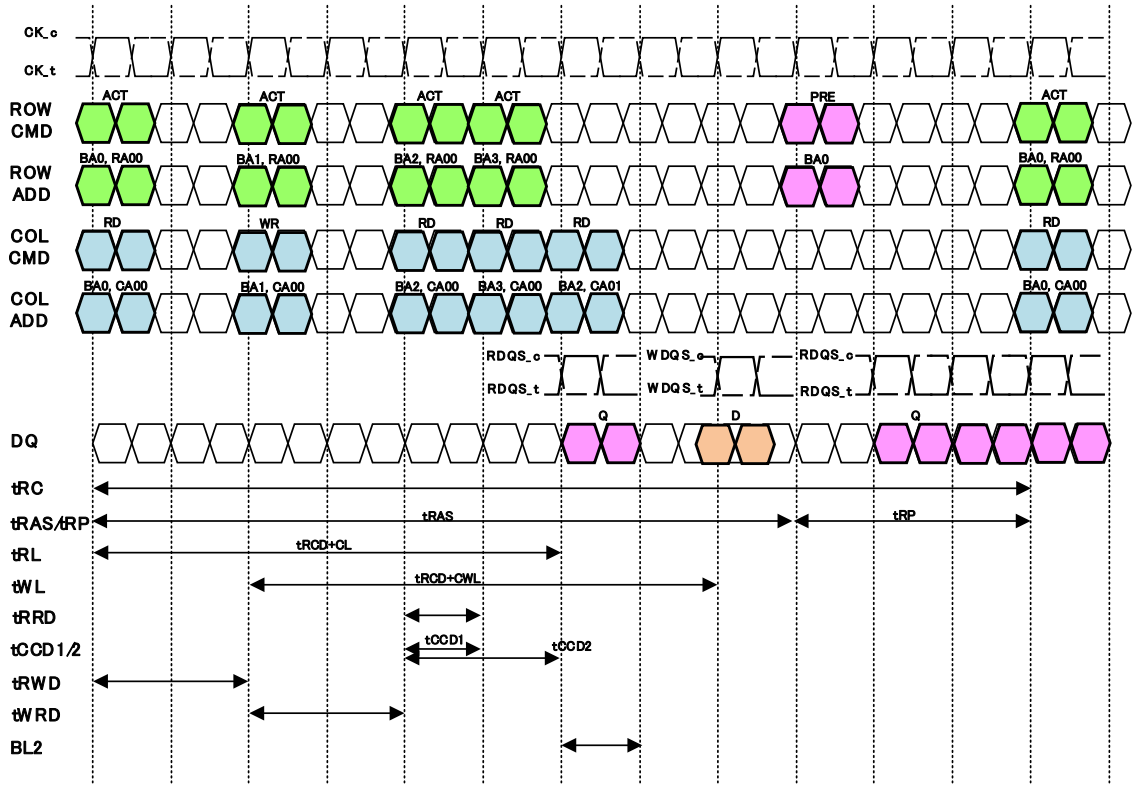
Figure 9 DDR Command / Address (R[x], C[x] including BAx, RAx, CAx) Input Timing Waveforms

- ✓ The two types of NO OPERATION (NOP) command (RNOP, CNOP) must be used on any cycle where no other commands are requested.
- ✓ The READ (RD) command is used to initiate a burst read from the Low Latency HBM.
- ✓ The READ with PRECHARGE (RDA) command is used to initiate a burst read and automatic PRECHARGE (PRE) operation.
- ✓ The WRITE with PRECHARGE (WRA) command is used to initiate a burst write and automatic PRECHARGE (PRE) operation.
- ✓ WRA command needs ACT command.
- ✓ The Mode Register set (MRS) command is used to configure the Low Latency HBM following a reset. Because READ and WRITE commands require one cycle to fully transfer their associated address in burst length 2/4 mode.

5.7. Command Functional Description

Configuration 1 BL2 OVERVIEW

Configuration 1 has 16channels [a:p] (16 command and address controllers (AWORD [a:p])).



Notes. tRWD/tWRD here is the value specified by Low Latency HBM device internal bus turnaround time and it is strongly recommended to add extra NOP to keep the system bus turnaround time

Notes. The two types of NO OPERATION (NOP) command (RNOP, CNOP) must be used on any cycle where no other commands are requested.

Notes. CL is Cas Latency (READ). CWL is Cas Write Latency(Write)

Notes. This figure is a conceptual diagram. For example, RDQS / WDQS preamble and postamble cycle are omitted.

Figure 10 Single cycle activate command description of burst length2 (Configuration1)

Table 17 AC timing parameters ; Configuration1 (example)

	Configuration1		comment
	BL2		
	Cyc	ns	Minimum spec example.
tCK	1GHz	1.00	
tRC	12	12.00	Fast Random ROW Cycle
tRCD	0	0.00	
tRAS			tRAS+tRP=tRC
tRP			tRAS+tRP=tRC
tRL			Read command To Data
tWL			Write command To Data
tRRD			ROW to ROW
tCCD1			COL to COL
tCCD2			COL to COL(same bank)
tRWD			Read to Write
tWRD			Write to Read

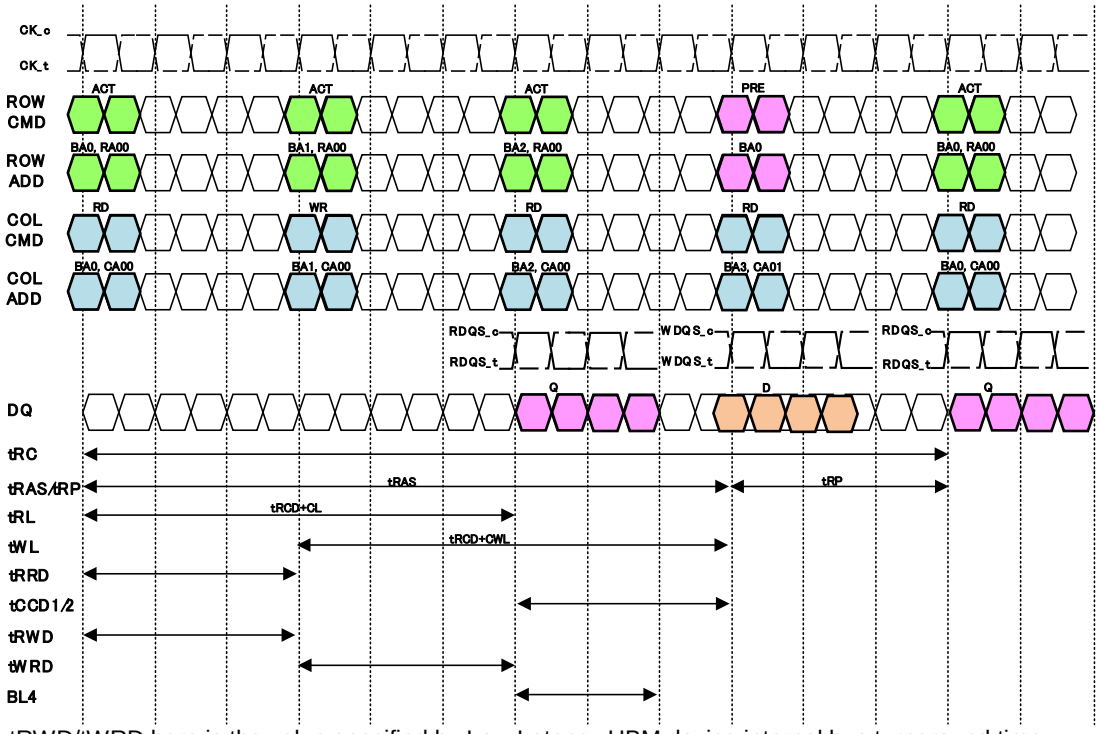
Notes. tCCD1 is the case of another banks access / tCCD2 is the same of same bank access.

Notes. tRAS means tRTP at ACT with READ. Refer to tRTP in burst access case.

This figure is a conceptual diagram. This datasheet is digest edition. Please contact Mail Inquires for more information. Mail Inquiries : LowLatencyHBM@lm.renesas.com

Configuration 2 BL4 OVERVIEW

Configuration 1 has 16channels [a:p] (16 command and address controllers (AWORD[a:p])). Configuration 2 has 8channels [a:h](8 command and address controllers (AWORD [a:h])). Channel size of configuration2 is half of configuration1.This figure is just simple image for understanding. Configuration 2 is based on pseudo channel mode shown in following page.



Notes. tRWD/tWRD here is the value specified by Low Latency HBM device internal bus turnaround time and it is strongly recommended to add extra NOP to keep the system bus turnaround time

Notes. The two types of NO OPERATION (NOP) command (RNOP, CNOP) must be used on any cycle where no other commands are requested.

Notes. CL is Cas Latency (READ). CWL is Cas Write Latency (Write)

Notes. This figure is a conceptual diagram. For example, RDQS / WDQS preamble and postamble cycle are omitted.

Figure 11 Single cycle activate command description of burst length4 (Configuration2)

Table 18 AC timing parameters ; Configuration2 (example)

	Configuration2		comment
	BL4		
	Cyc	ns	Minimum spec example.
tCK	1GHz	1.00	
tRC	16	16.00	Fast Random ROW Cycle
tRCD	0	0.00	
tRAS			tRAS+tRP=tRC
tRP			tRAS+tRP=tRC
tRL			Read command To Data
tWL			Write command To Data
tRRD			ROW to ROW
tCCD1			COL to COL
tCCD2			COL to COL(same bank)
tRWD			Read to Write
tWRD			Write to Read

Notes. tCCD1 is the case of another banks access / tCCD2 is the same of same bank access.

Notes. tRAS means tRTP at ACT with READ. Burst access refers to tRTP.

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5.8. Data mask

This function is not supported.

5.9. Data inversion

To reduce simultaneous switch noise, I/O current and average I/O power, the Low Latency HBM provides the ability to invert all data pins. Because the nominal design for Low Latency HBM I/O signals is not termination.

5.10. Data bus turn-around

Because the DQn-DQ0 and DBIm-DBI0 pins are bidirectional, care must be taken to ensure that the Low Latency HBM and the system chip connected to it do not drive these pins simultaneously. To guarantee this, a rapid DQ and DBI turn-off time is required. The actual bus turn-around time is dependent on many system parameters, including BL, RL, WL, pre-amble, post-amble, controller I/O timing, DRAM I/O timing, PCB delays; and the system must ensure that neither Low Latency HBM, nor the system chip is driving the bus during that time. This is accomplished by inserting a sufficient number of NOP commands between each READ-to-WRITE command transition and between each WRITE-to-READ transition. Additional NOP commands may be required to allow settling of the bus to insure no adverse effect on I/O timing.

5.11. Command cycles

A command to the Low Latency HBM is initiated by driving the R[x], C[x] pin low at the rising edge of CK the appropriate state corresponding to the command.

READ and WRITE commands each require 1 clock to send the full command in burst length 2/4 mode, due to the multiplexed nature of Address loading. The ACT, PRE, NOP and AUTO REFRESH commands are each a single cycle in length.

5.12. Write data cycles

DQ0-DQn, DBI0-DBIm associated with a WRITE command are received by the Low Latency HBM in a DDR burst, starting on a rising edge of WDQS_t that is offset WL clock cycles from rising edge of the CK signal corresponding to the first cycle that the WRITE command was initiated. This delay of WL cycles is intended to ensure that the write data are not driven at the same time that data from a previous READ command are being driven from the Low Latency HBM.

5.13. Read data cycles

DQ0-DQn and DBI0-DBIm associated with a READ command are driven by the Low Latency HBM in a DDR burst, RL clock cycles from the rising edge of the CK signal corresponding to the first cycle that the READ command was initiated. This delay of RL cycles is equal to the delay required for the internal logic and memory within the Low latency HBM to read data and make it available on the bus.

5.14. Automatic Refresh

Refresh cycles of the internal memory are initiated via the Automatic “Refresh command”. Each refresh command causes a single refresh cycle to occur on the bank specified in the command.The minimum data retention time is 2ms over the temperature range specified in “**1. Electrical Specifications”**, and there are 8192 words in each bank. Therefore, each bank must receive 8192 refresh commands every 2ms in order to ensure proper data retention.

6. Initialization

Prior to functional use, Low Latency HBM must be initialized and configured. The steps described in this chapter will ensure that the internal logic of Low Latency HBM has been properly reset and that the functional timing parameters of the chip have been configured.

7. Test Specification

Low Latency HBM supports direct access test mode (DA) as for product qualifications and specifications, and a limited set of test functions as in test mode via command pin.

8. APPENDIX

Revision History	RENESAS Low Latency High Bandwidth Memory (Low Latency DRAM family Gen.5th)

Rev.	Date	Description	
		Page	Summary
Rev.0.001	’19.1.13	-	New Preliminary Datasheet Digest Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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