To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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M62055FP

3 V Power Supply with Watchdog Timer

REJ03D0808-0200
Rev.2.00
Mar 10, 2006

Description

M62055FP is a 3 V power supply featuring a watchdog timer function for a microcontroller system.

It can be a power source of 3 V ± 5% by utilizing the reference voltage and amplifier.

It can also generate a reset pulse for the applied systems during power-on, moreover it includes the watchdog timer for a self diagnostics of the system, which can prevent system erroneous functions.

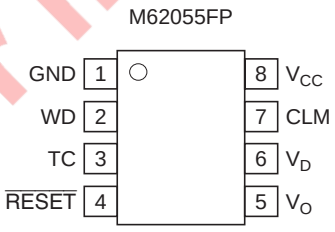
Features

- Power-on reset
- Watchdog timer
- High accuracy voltage source of 3 V ± 5% (Max)
- Over current protection circuit
- The voltage detection accuracy of ±5% (Max)
- Output power (V_O) cutoff function at erroneous conditions
- Backward voltage protection circuits for inputs and outputs

Application

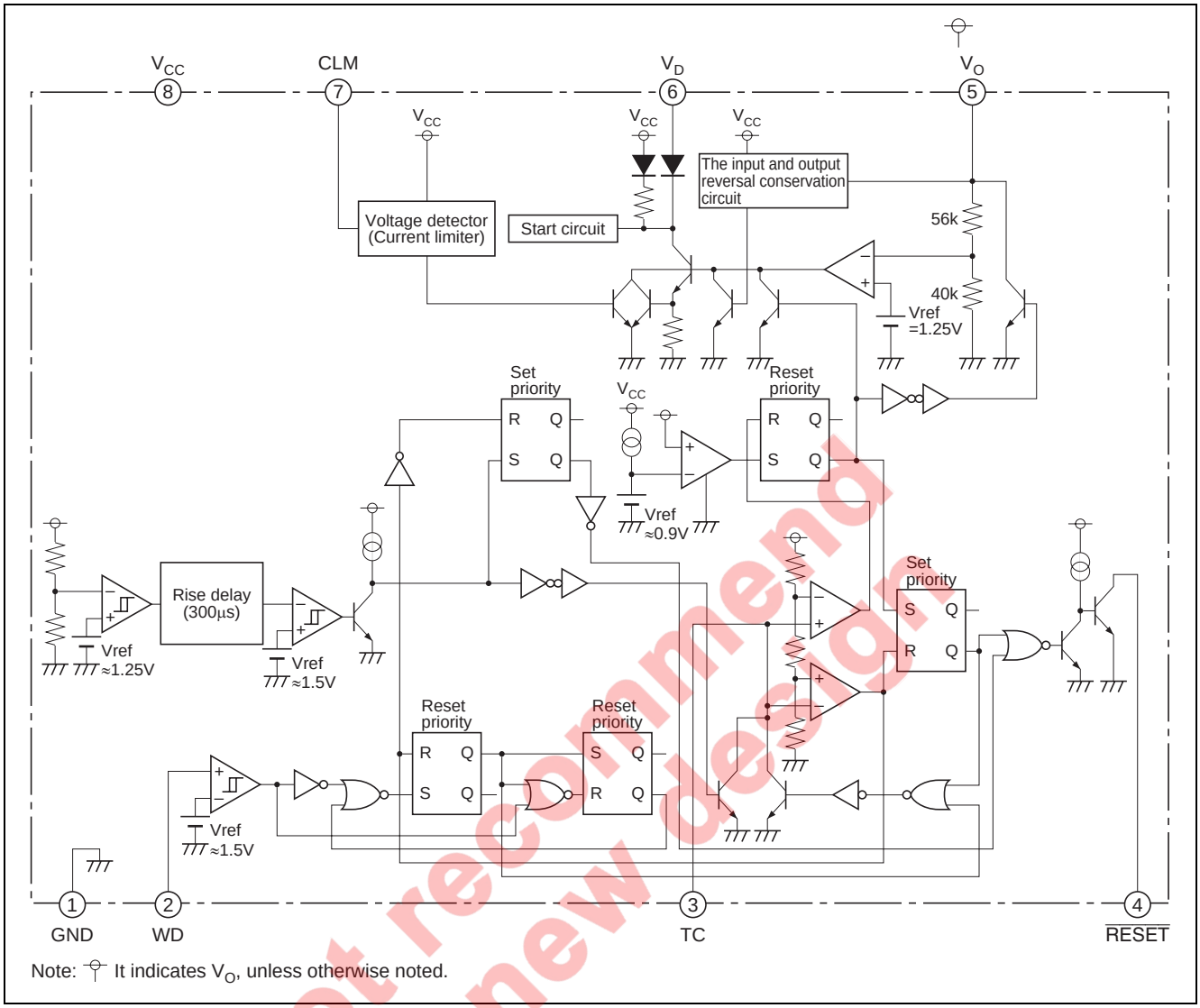
- Handy information terminal equipment, CD-ROM, Portable audio equipment

Pin Arrangement



(Top view)
Package: PRSP0008DA-A (8P2S-A)

Block Diagram



Note: ⏚ It indicates V_O, unless otherwise noted.

Pin Functional Description

Pin No.	Symbol	Functional Description
1	GND	Ground
2	WD	Input for watchdog timer
3	TC	Setting up reset timer and watchdog timer
4	$\overline{\text{RESET}}$	Reset signal output
5	V_O	Feedback to a power supply for a MCU
6	V_D	Controlling the stability of an output voltage with a PNP transistor connected externally
7	CLM	Current limiting
8	V_{CC}	Power supply voltage

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item		Symbol	Ratings	Unit	Conditions
Supply voltage		V_{CC}	13	V	
Reset pin	Output voltage	V_{RM}	10	V	
	Output current	I_{RM}	10	mA	
Watchdog pin input voltage		V_{WDM}	3	V	
Thermal derating		Kθ	4.0	mV/°C	Ta ≥ 25°C
Operating temperature		Topr	–20 to +75	°C	
Storage temperature		Tstg	–55 to +150	°C	

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

DC Characteristics

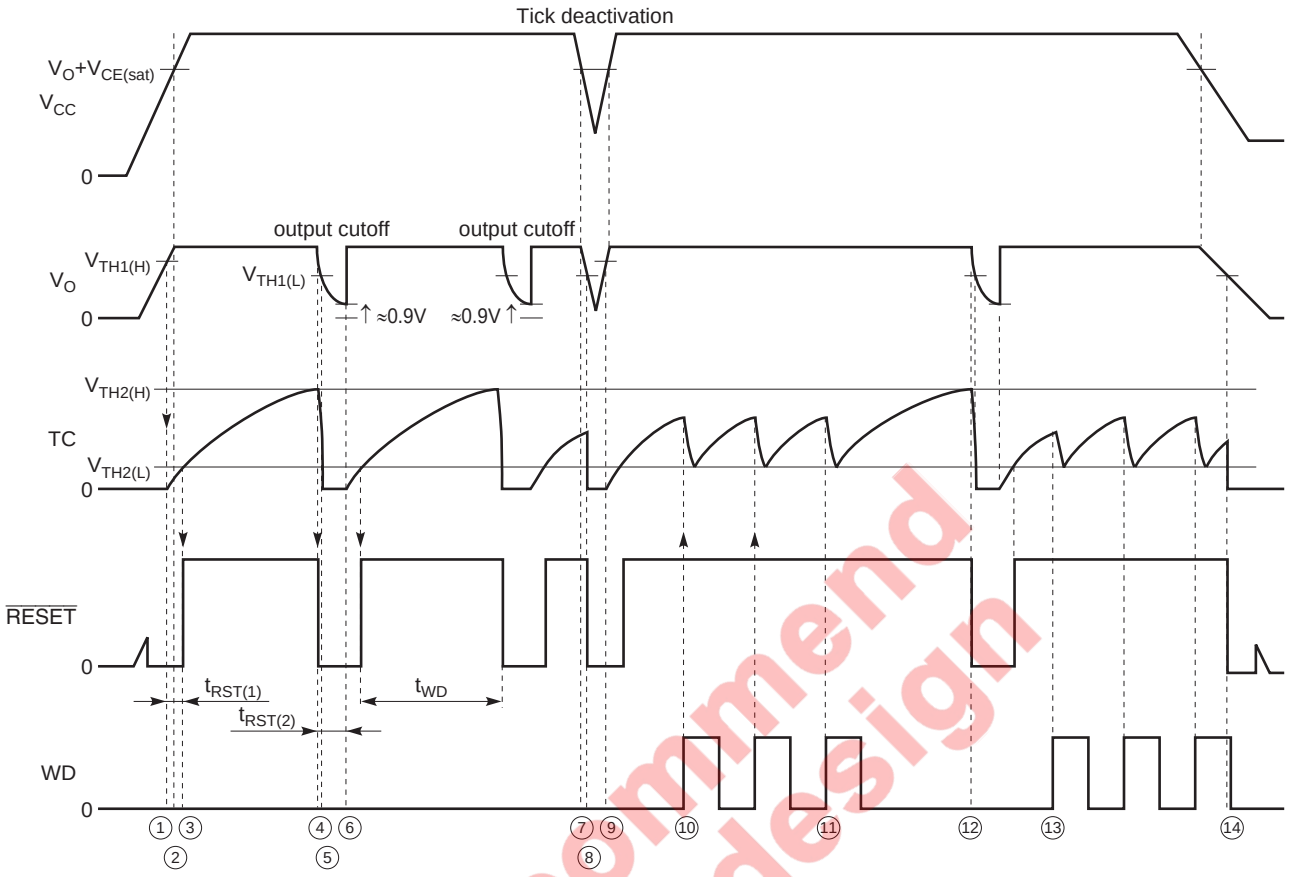
Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Battery backup regulator	Supply voltage		V_{CC}	3.5	—	13	V	
	Circuitry current		I_{CC}	—	500	900	µA	
	Output voltage		V_O	2.85	3.00	3.15	V	
	Bias current		I_{Bmax}	—	10	—	mA	
	Listing short-circuit bias current		IBSC	—	1	—	mA	
	Input voltage regulation		Reg-in	—	0.02	—	%/V	V_{CC} = 3.5V to 13V
	Loading voltage regulation		Reg-lo	—	20	—	mV	I_O = 10mA to 100mA
	Output voltage thermal coefficient		$\Delta V_O/\Delta T$	—	0.02	—	%/T	
	CLM threshold voltage		V_{THCLM}	—	200	—	mV	
Reset, watchdog timer	V_O detection voltage		$V_{TH1(H)}$	2.68	2.82	2.96	V	
			$V_{TH1(L)}$	2.58	2.72	2.86	V	
			ΔV_{TH1}	—	0.1	—	V	
	Output voltage	Reset pin	$V_{OL(RST)}$	—	0.2	0.4	V	Isink = 4mA
	Output leakage current		Ileak	—	—	5	µA	
	Watchdog timer threshold voltage		$V_{TH2(H)}$	2.28	2.40	2.52	V	
			$V_{TH2(L)}$	0.95	1.00	1.05	V	
	WD input current		I_{WD}	—	—	1	µA	V_{IN} = 3V
	WD input threshold voltage		$V_{TH(WD)}$	—	1.5	—	V	
	TC output current		Itco	—	—	–1	µA	V_{IN} = 0.8V
	TC input current		Itc1	—	2.0	—	mA	V_{IN} = 2.4V
			Itc2	8.0	—	—	mA	In the output cutoff transmission mode
	V_{CC} min operating voltage		V_{CCMIN}	—	—	2.0	V	*1

Note: 1. The V_{CC} minimum operating voltage at which the RESET output is low.

AC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Watchdog timer	t_{WD}	0.5	1.2	1.7	ms	C = 0.1µF, R_1 = 10kΩ
Reset timer (1)	$t_{RST(1)}$	0.2	0.5	1.1	ms	C = 0.1µF, R_1 = 10kΩ
Reset timer (2)	$t_{RST(2)}$	—	—	10	ms	C_O = 10µF, R_1 = 10kΩ, I_L = 0
Input pulse width	t_{WDIN}	3	—	—	µs	
Transmission delay time	t_d	—	20	—	µs	

Timing Chart



①: When V_O rises to 0.5 V, $\overline{RESET}$ becomes low. Then, charging to a capacitor C connected to TC will be started at the V_O of 2.82 V ($V_{TH1(H)}$).

②: When V_{CC} rises to 3 V + $V_{CE(sat)}$, V_O becomes stable.

③,④: When TC voltage rises to 1 V ($V_{TH2(L)}$), $\overline{RESET}$ becomes high. When it rises to 2.4 V ($V_{TH2(H)}$) further, the capacitor C is switched to discharge and $\overline{RESET}$ becomes low.

⑤: At the same tome of a change-over to the discharge from the capacitor C, V_O is intercepted.
Then, TC will be discharged completely at V_O of 2.72 V ($V_{TH1(L)}$).

⑥: V_O returns to 3 V right after it has fallen down to 0.9 V. $\overline{RESET}$ repeats above operation till a normal clock signal is input to WD pin.

⑦,⑧,⑨: In the case of a sudden power interruption, V_O falls down according to a decrease of V_{CC}.
When it falls down to 2.72 V, the capcitor C is discharged and $\overline{RESET}$ will be low.
In the case of a reversion from the power interruption, V_O rises according to a increase of V_{CC}. When it rises to 2.82 V, the charging to the capacitor C is started and $\overline{RESET}$ will be high right after TC voltage reaches 1 V.

⑩,⑪: In the case of a clock signal for discharging the capacitor C is applied to pin WD before TC voltage reaches to 2.4 V, a reset signal to $\overline{RESET}$ is canceled.

⑫,⑬: In the case of an abnormal clock signal is input, TC repeats charging / discharging alternately between 1 V and 2.4 V, so that $\overline{RESET}$ also repeats high / low till a normal clock signal is input.

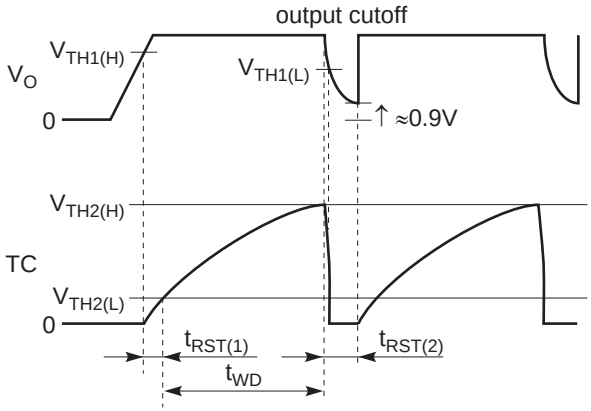
⑭: When V_O falls down to 2.72 V, $\overline{RESET}$ becomes low.

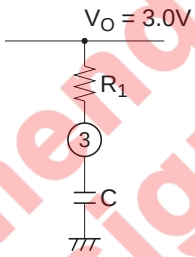
Description of Terms

$t_{RST(1)}$: Time from when TC begins to charge until it reaches to $V_{TH2(L)}$.
t_{WD} : Time from when TC is $V_{TH2(L)}$ until it reaches to $V_{TH2(H)}$.
$t_{RST(2)}$: Time from when TC is $V_{TH2(H)}$ until TC starts charging.

1. Pin (3) (TC pin) Charging and Discharging Time

When an error is occurred in RD input, TC waveform is as shown in figure 1.





$t_{RST(1)} = 0.406 \cdot C \cdot R_1 + 300\mu s^{*1}$

$t_{WD} = 1.2 \cdot C \cdot R_1$ (Charging time)

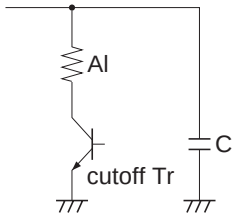
Note: 1. Inside delay time (Typ)

Figure 1

The following formula can be obtained because $t_{RST(2)}$ is equal to the duration of V_O cutoff.

$$t_{RST(2)} = C \cdot R^{*2} \cdot \ln\left(\frac{3}{0.9}\right) + 300\mu s^{*3}$$

$$= 40 \cdot C + 300\mu s^{*3}$$

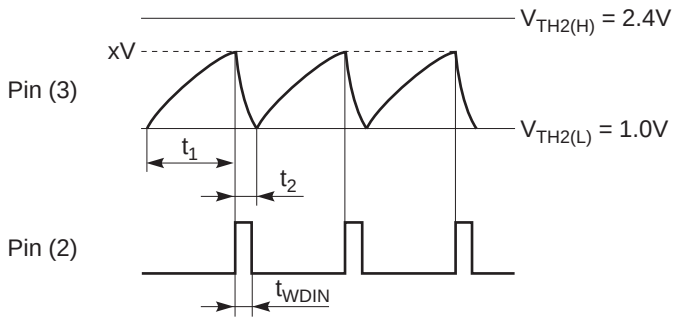


Note: 2. R = Internal resistance
3. Inside delay time (Typ)

Figure 2

2. Pin (2) (WD pin) Input Frequency, Input Pulse Width, Charge/Discharge Time

When input of (2) WD is normal, TC waveform (3) is as shown in figure 3.



$$t_1 = C \cdot R_1 \cdot \ln \frac{2}{3 - X}$$

$$t_2 = 1000 \cdot C \cdot R_1 \cdot \ln \frac{X\left(\frac{R_1}{1000} + 1\right) - 3}{\frac{R_1}{1000} - 2}$$

Figure 3

- Conditions of an input to pin (2) (WD pin)
  (1) Input period should be t_{WD} or less. (Pin discharge is completed before the arrival of $V_{TH2(H)}$ = 2.4 V)

  $$\frac{1}{1.2 \cdot C \cdot R_1} < f$$

  (2) Input pulse width t_{WDIN} should be t_2 or less.

3. Relationship between the Input Pulse Width and the Low Pass Filter

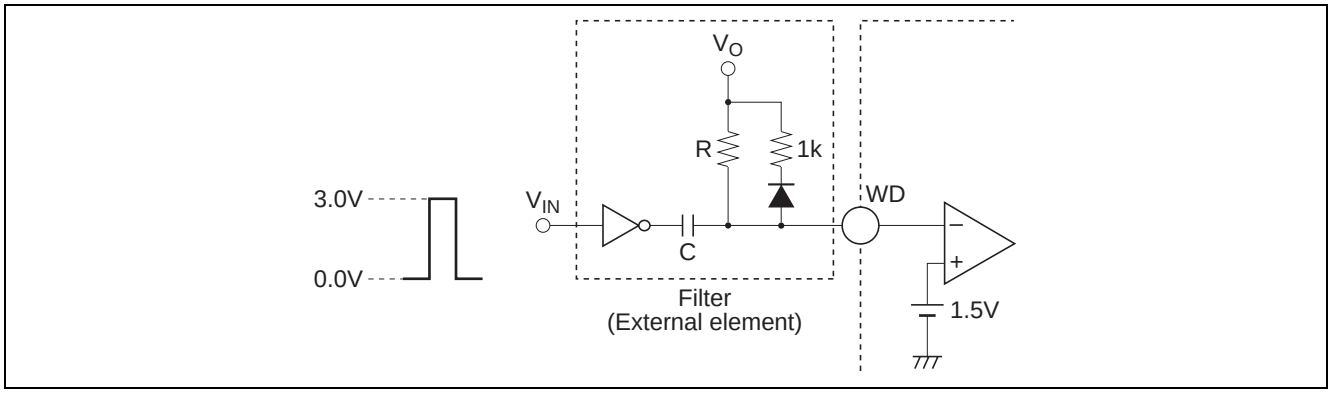


Figure 4

Addition of a low pass filter makes input waveform dull. An input pulse width and CR of a low pass filter is determined referring to the figure 5.

$$t_3 = -C \cdot R \cdot \ln \frac{1.5V}{V_{IN}}$$

$\overline{\text{RESET}}$ is output in the case of $t_4 > t_{WD}$.

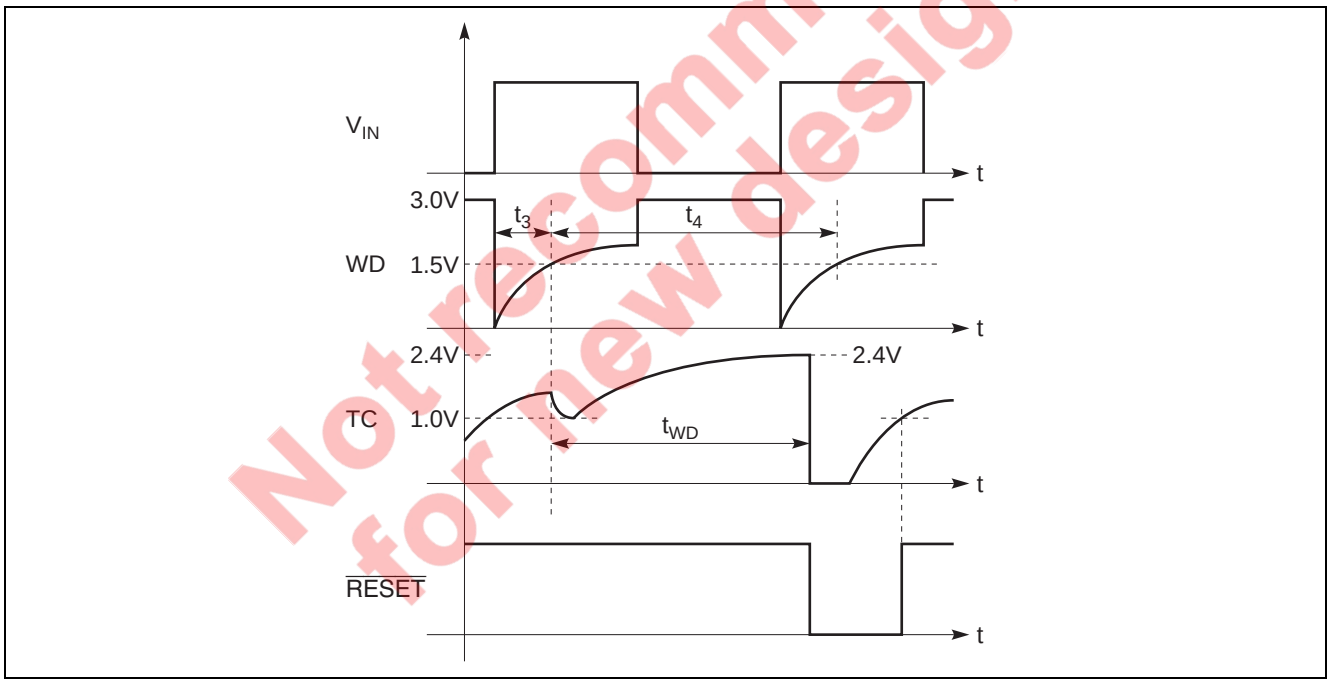


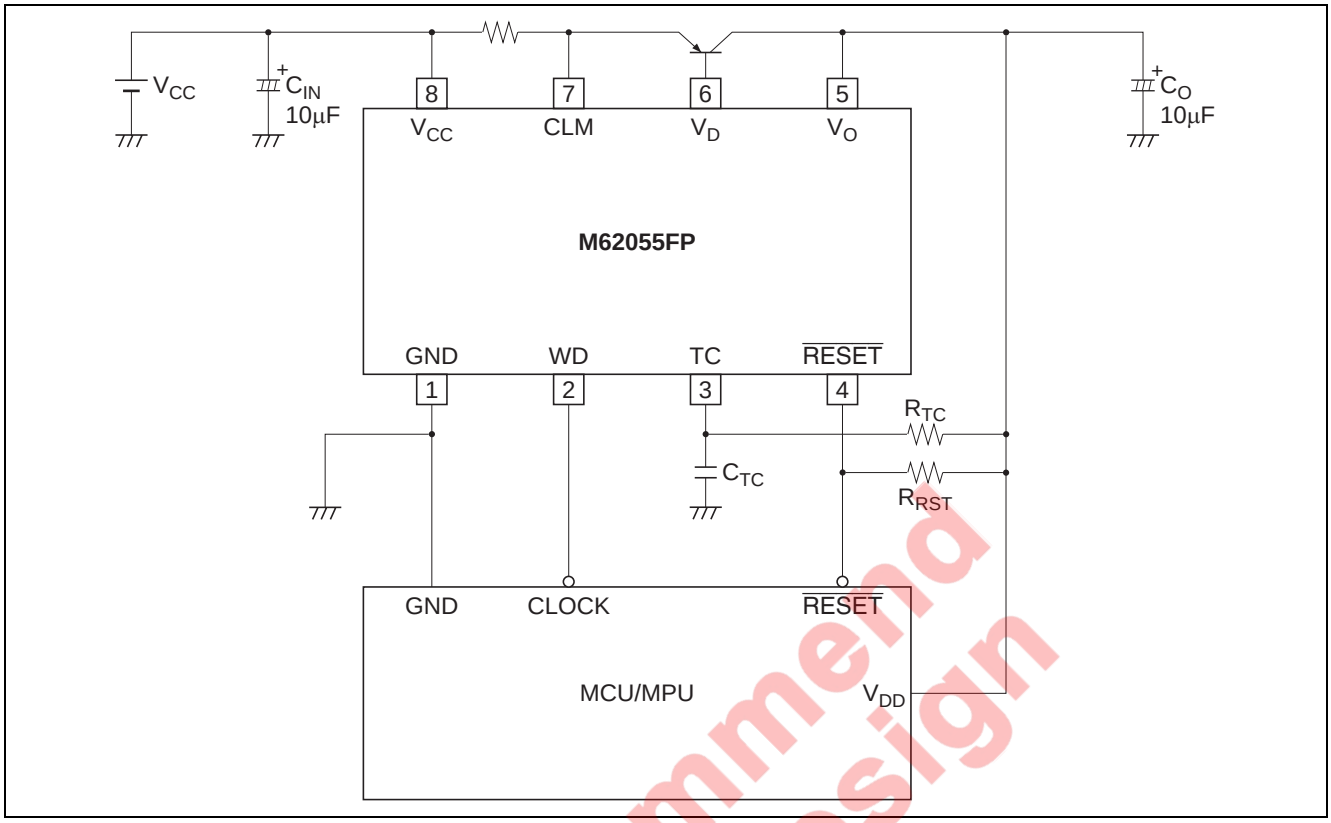
Figure 5

If t_3 is too long, the TC waveform changes as shown in figure5.

t_3 is set as follows:

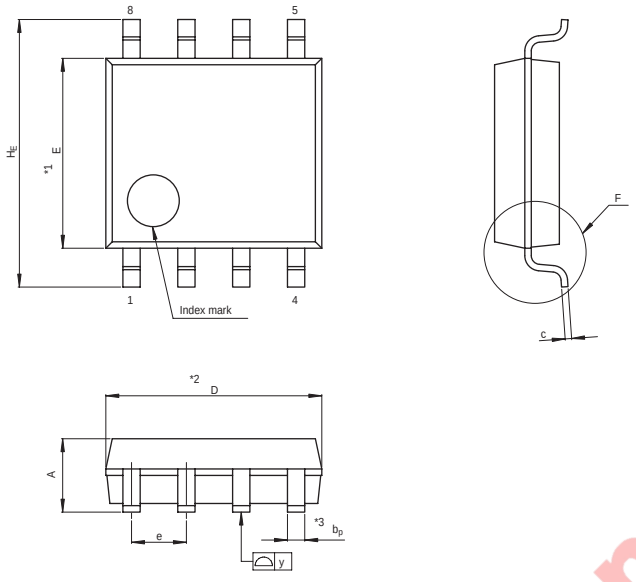
t_{WDIN} (3 µs) or more and t_2 (charging time) or less. (t_2 is a discharge time while an input is normal)

Application Circuit Example



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A_1	0.05	—	—
A	—	—	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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