PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

MC-24212361-X

MCP (MULTI-CHIP PACKAGE) FLASH MEMORY AND MOBILE SPECIFIED RAM
64M-BIT FLASH MEMORY AND 16M-BIT MOBILE SPECIFIED RAM

Description

The MC-24212361-X is a stacked type MCP (Multi-Chip Package) of 67,108,864 bits (4,194,304 words by 16 bits) flash memory and 16,777,216 bits (1,048,576 words by 16 bits) Mobile specified RAM.

The MC-24212361-X is packaged in 85-pin TAPE FBGA.

Features

General Features

- Fast access time : t_{ACC} = 90 ns (MAX.) (Flash memory)
  t_{AA} = 80, 90, 100 ns (MAX.) (Mobile specified RAM)
- Supply voltage : $V_{CC}f$ / $V_{CC}m$ = 2.6 to 3.1 V
- Wide operating temperature : T_A = –25 to +85 °C

Flash Memory Features

- Corresponded page read operation
- Four bank organization enabling simultaneous execution of erase / program and read
- Bank organization : 4 banks (8M bits + 24M bits + 24M bits + 8M bits)
- Memory organization : 4,194,304 words × 16 bits
- Sector organization : 142 sectors (4K words × 16 sectors, 32K words × 126 sectors)
- Boot sector allocated to the highest address (sector) and lowest address (sector)
- 3-state output
- Automatic program
  - Program suspend / resume
- Unlock bypass program
- Automatic erase
  - Chip erase
  - Sector erase (sectors can be combined freely)
  - Erase suspend / resume
- Program / Erase completion detection
  - Detection through data polling and toggle bits
  - Detection through RY (/BY) pin

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- Sector group protection
  - Any sector can be protected
  - Any protected sector can be temporary unprotected
  - Any sector group can be unprotected
- Sectors can be used for boot application
- Hardware reset and standby using /RESET pin
- Automatic sleep mode
- Boot block sector protect by /WP (ACC) pin
- Extra One Time Protect Sector provided
- Program / erase time
  - Program : 11.0 μs / word (TYP.)
  - Sector erase :

    Erase / program cycle : 100,000 cycle

    0.3 s (TYP.) (4K words sector), 0.5 s (TYP.) (32K words sector)

    Erase / program cycle : 1,000,000 cycle

    0.5 s (TYP.) (4K words sector), 0.7 s (TYP.) (32K words sector)
- Erase / program cycle : 100,000 cycle (MIN.)

Mobile specified RAM Features

- Memory organization : 1,048,576 words by 16 bits
- Supply current : At operating : 35 mA (MAX.)

  At Standby Mode 1 : 70 μA (MAX.)

  At Standby Mode 2 : 10 μA (MAX.) (Memory cell data hold invalid)
- Chip Enable inputs : /CEm
- Byte data control : /LB, /UB
- Standby Mode input : MODE
- Standby Mode 1 : Normal standby (Memory cell data hold valid)
- Standby Mode 2 : Memory cell data hold invalid

Ordering Information

Part number	Flash memory access time ns (MAX.)	Mobile specified RAM Access time ns (MAX.)	Operating supply voltage V		Package	Mounted Flash memory
			Chip	I/O		
MC-24212361F9-E90X-CDx	90	80	1.8 ± 0.15 (Flash memory) 2.6 to 3.1 (Mobile specified RAM)	2.6 to 3.1 (Flash memory)	85-pin TAPE FBGA (11 x 8)	μPD29F064115-Y
MC-24212361F9-E95X-CDx		90				
MC-24212361F9-E10X-CDx		100				

Remark "CDx" of part number is package specifications. However, this is not available.

COMMANDS, HARDWARE SEQUENCE FLASGS, HARD WARE DATA PROTECTION, READ MODE REGISTER SETTINGS, TIMING CHARTS and FLOW CHARTS for Flash memory, refer to PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E).

Timing charts for Mobile specified RAM, refer to SRAM AND MOBILE SPECIFIED RAM TAIMING CHARTS FOR MCP (IBB-EB-0291).

Pin Configuration (Marking side)

/xxx indicates active low signal.

85-pin TAPE FBGA (11 × 8)

[MC-24212361F9-ExxX-CDx]

Top View

	A	B	C	D	E	F	G	H	J	K	L	M
10	NC	NC				NC	NC				NC	NC
9	NC	NC		A15	A21	IC	A16	NC	Vss		NC	NC
8		NC	A11	A12	A13	A14	NC	I/O15	I/O7	I/O14	NC	
7			A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5		
6		NC	/WE	MODE	A20			I/O4	Vccm	VccQf	NC	
5		NC	/WP(ACC)	/RESET	RY(/BY)			I/O3	Vccf	I/O11	NC	
4			/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2		
3		NC	A7	A6	A5	A4	Vss	/OE	I/O0	I/O8	NC	
2	NC	NC		A3	A2	A1	A0	/CEf	/CEm		NC	NC
1	NC	NC	NC			NC	NC				NC	NC

Common Pins

A0 - A19	:	Address Inputs
I/O0 - I/O15	:	Data Inputs / Outputs
/OE	:	Output Enable
/WE	:	Write Enable
Vss	:	Ground
NC Note1	:	No Connection
IC Note2	:	Internal Connection

Flash memory Pins

A20, A21	:	Address Inputs
/CEf	:	Chip Enable
RY (/BY)	:	Ready (Busy) Output
/RESET	:	Hardware Reset Input
/WP(ACC)	:	Hardware Write Protect (Acceleration)
Vccf	:	Supply Voltage
VccQf	:	Input / Output Supply Voltage

Mobile specified RAM Pins

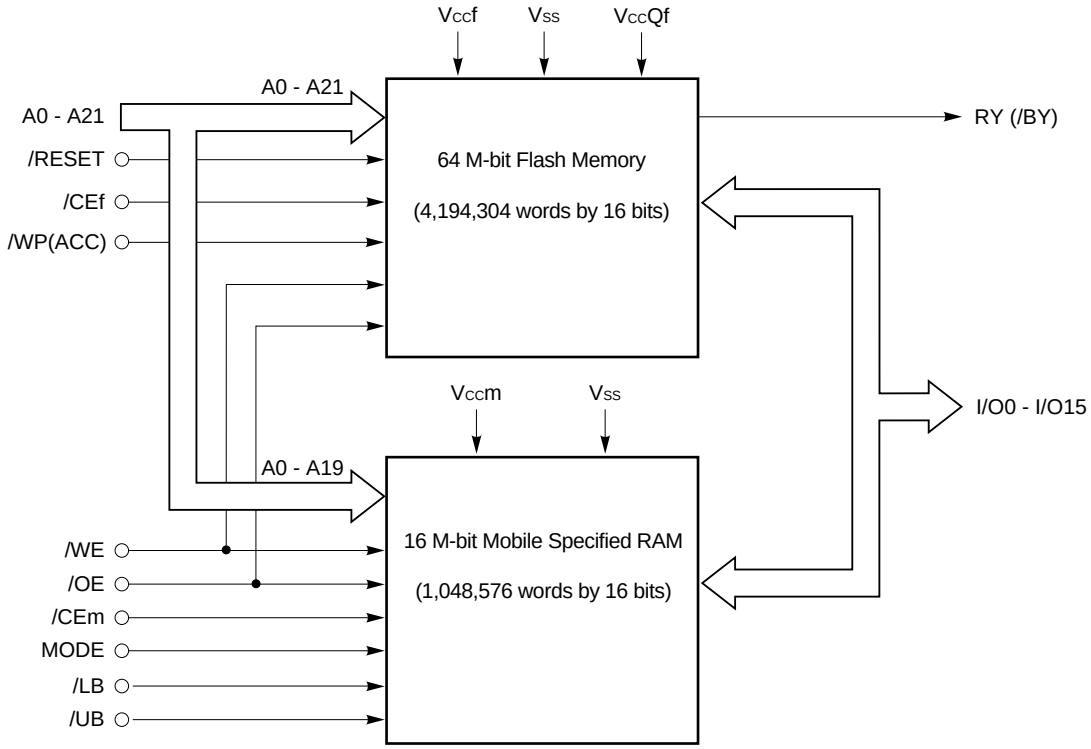
/CEm	:	Chip Enable
MODE	:	Standby Mode Select
/LB, /UB	:	Byte Data Select
Vccm	:	Supply Voltage

Notes 1. Some signals can be applied because this pin is not internally connected.

2. Leave this pin connected to Vss or unconnected (Recommended to connected to Vss).

Remark Refer to **8. Package Drawing** for the index mark.

Block Diagram



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1. Bus Operations

Table 1-1. Bus Operations

Operation		Flash memory			Mobile specified RAM				Common			
		/RESET	/CEf	/WP(ACC)	/CEm	MODE	/LB	/UB	/OE	/WE	I/O0 - I/O7	I/O8 - I/O15
Full standby	Standby Mode 1	H	H	×	H	H	×	×	×	×	Hi-Z	Hi-Z
	Standby Mode 2				H	L						
Output disable		H	L	×	L	H	×	×	H	H	Hi-Z	Hi-Z
Read (Flash memory [Note 1])		H	L	×	**Note 2**				L	H	Data Out	Data Out
Write (Flash memory)		H	L	×	**Note 2**				H	L	Data In	Data In
Temporary sector group unprotect		V_{ID}	×	×	**Note 2**				×	×	Hi-Z or Data Out / In	Hi-Z or Data Out / In
Boot block sector protect		×	×	L	×	×	×	×	×	×	Hi-Z or Data Out / In	Hi-Z or Data Out / In
Flash memory hardware reset		L	×	×	×	×	×	×	×	×	Hi-Z	Hi-Z
Read (Mobile specified RAM)		**Note 3**			L	H	L	L	L	H	Data Out	Data Out
								H				Hi-Z
							H	L			Hi-Z	Data Out
Write (Mobile specified RAM)		**Note 3**			L	H	L	L	×	L	Data In	Data In
								H				Hi-Z
							H	L			Hi-Z	Data In

Caution Other operations except for indicated in this table are inhibited.

Notes 1. When /OE = V_{IL}, V_{IL} can be applied to /WE. When /OE = V_{IH}, a write operation is started.

2. Mobile specified RAM should be Standby.

3. Flash memory should be Standby or Hardware reset.

Remarks 1. H : V_{IH}, L : V_{IL}, × : V_{IH} or V_{IL}

2. Sector group protection and read the product ID are using a command.

3. MODE pin must be fixed to H during active operation.

2. Sector Organization / Sector Address Table (Flash memory)

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank D	4	3FFFFFH 3FF000H	SA141	1	1	1	1	1	1	1	1	1	1
	4	3FEFFFH 3FE000H	SA140	1	1	1	1	1	1	1	1	1	0
	4	3FDFFFH 3FD000H	SA139	1	1	1	1	1	1	1	1	0	1
	4	3FCFFFH 3FC000H	SA138	1	1	1	1	1	1	1	1	0	0
	4	3FBFFFH 3FB000H	SA137	1	1	1	1	1	1	1	0	1	1
	4	3FAFFFH 3FA000H	SA136	1	1	1	1	1	1	1	0	1	0
	4	3F9FFFH 3F9000H	SA135	1	1	1	1	1	1	1	0	0	1
	4	3F8FFFH 3F8000H	SA134	1	1	1	1	1	1	1	0	0	0
	32	3F7FFFH 3F0000H	SA133	1	1	1	1	1	1	0	x	x	x
	32	3EFFFFH 3E8000H	SA132	1	1	1	1	1	0	1	x	x	x
	32	3E7FFFH 3E0000H	SA131	1	1	1	1	1	0	0	x	x	x
	32	3DFFFFH 3D8000H	SA130	1	1	1	1	0	1	1	x	x	x
	32	3D7FFFH 3D0000H	SA129	1	1	1	1	0	1	0	x	x	x
	32	3CFFFFH 3C8000H	SA128	1	1	1	1	0	0	1	x	x	x
	32	3C7FFFH 3C0000H	SA127	1	1	1	1	0	0	0	x	x	x
	32	3B7FFFH 3B8000H	SA126	1	1	1	0	1	1	1	x	x	x
	32	3B7FFFH 3B0000H	SA125	1	1	1	0	1	1	0	x	x	x
	32	3AFFFFH 3A8000H	SA124	1	1	1	0	1	0	1	x	x	x
	32	3A7FFFH 3A0000H	SA123	1	1	1	0	1	0	0	x	x	x
	32	39FFFFH 3980000H	SA122	1	1	1	0	0	1	1	x	x	x
	32	397FFFH 390000H	SA121	1	1	1	0	0	1	0	x	x	x
	32	38FFFFH 388000H	SA120	1	1	1	0	0	0	1	x	x	x
	32	387FFFH 380000H	SA119	1	1	1	0	0	0	0	x	x	x
Bank C	32	37FFFFH 378000H	SA118	1	1	0	1	1	1	1	x	x	x
	32	377FFFH 370000H	SA117	1	1	0	1	1	1	0	x	x	x
	32	36FFFFH 368000H	SA116	1	1	0	1	1	0	1	x	x	x
	32	367FFFH 360000H	SA115	1	1	0	1	1	0	0	x	x	x
	32	35FFFFH 358000H	SA114	1	1	0	1	0	1	1	x	x	x
	32	357FFFH 350000H	SA113	1	1	0	1	0	1	0	x	x	x
	32	34FFFFH 3480000H	SA112	1	1	0	1	0	0	1	x	x	x
	32	347FFFH 340000H	SA111	1	1	0	1	0	0	0	x	x	x
	32	33FFFFH 338000H	SA110	1	1	0	0	1	1	1	x	x	x
	32	337FFFH 330000H	SA109	1	1	0	0	1	1	0	x	x	x
	32	32FFFFH 328000H	SA108	1	1	0	0	1	0	1	x	x	x
	32	327FFFH 320000H	SA107	1	1	0	0	1	0	0	x	x	x
	32	31FFFFH 318000H	SA106	1	1	0	0	0	1	1	x	x	x

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank C	32	317FFFH 310000H	SA105	1	1	0	0	0	1	0	x	x	x
	32	30FFFFH 308000H	SA104	1	1	0	0	0	0	1	x	x	x
	32	307FFFH 300000H	SA103	1	1	0	0	0	0	0	x	x	x
	32	2FFFFFH 2F8000H	SA102	1	0	1	1	1	1	1	x	x	x
	32	2F7FFFH 2F0000H	SA101	1	0	1	1	1	1	0	x	x	x
	32	2EFFFFH 2E8000H	SA100	1	0	1	1	1	0	1	x	x	x
	32	2E7FFFH 2E0000H	SA99	1	0	1	1	1	0	0	x	x	x
	32	2DFFFFH 2D8000H	SA98	1	0	1	1	0	1	1	x	x	x
	32	2D7FFFH 2D0000H	SA97	1	0	1	1	0	1	0	x	x	x
	32	2CFFFFH 2C8000H	SA96	1	0	1	1	0	0	1	x	x	x
	32	2C7FFFH 2C0000H	SA95	1	0	1	1	0	0	0	x	x	x
	32	2BFFFFH 2B8000H	SA94	1	0	1	0	1	1	1	x	x	x
	32	2B7FFFH 2B0000H	SA93	1	0	1	0	1	1	0	x	x	x
	32	2AFFFFH 2A8000H	SA92	1	0	1	0	1	0	1	x	x	x
	32	2A7FFFH 2A0000H	SA91	1	0	1	0	1	0	0	x	x	x
	32	29FFFFH 298000H	SA90	1	0	1	0	0	1	1	x	x	x
	32	297FFFH 290000H	SA89	1	0	1	0	0	1	0	x	x	x
	32	28FFFFH 288000H	SA88	1	0	1	0	0	0	1	x	x	x
	32	287FFFH 280000H	SA87	1	0	1	0	0	0	0	x	x	x
	32	27FFFFH 278000H	SA86	1	0	0	1	1	1	1	x	x	x
	32	277FFFH 270000H	SA85	1	0	0	1	1	1	0	x	x	x
	32	26FFFFH 268000H	SA84	1	0	0	1	1	0	1	x	x	x
	32	267FFFH 260000H	SA83	1	0	0	1	1	0	0	x	x	x
	32	25FFFFH 258000H	SA82	1	0	0	1	0	1	1	x	x	x
	32	257FFFH 250000H	SA81	1	0	0	1	0	1	0	x	x	x
	32	24FFFFH 248000H	SA80	1	0	0	1	0	0	1	x	x	x
	32	247FFFH 240000H	SA79	1	0	0	1	0	0	0	x	x	x
	32	23FFFFH 238000H	SA78	1	0	0	0	1	1	1	x	x	x
	32	237FFFH 230000H	SA77	1	0	0	0	1	1	0	x	x	x
	32	22FFFFH 228000H	SA76	1	0	0	0	1	0	1	x	x	x
	32	227FFFH 220000H	SA75	1	0	0	0	1	0	0	x	x	x
	32	21FFFFH 218000H	SA74	1	0	0	0	0	1	1	x	x	x
	32	217FFFH 210000H	SA73	1	0	0	0	0	1	0	x	x	x
	32	20FFFFH 208000H	SA72	1	0	0	0	0	0	1	x	x	x
	32	207FFFH 200000H	SA71	1	0	0	0	0	0	0	x	x	x

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank B	32	1FFFFFH 1F8000H	SA70	0	1	1	1	1	1	1	x	x	x
	32	1F7FFFH 1F0000H	SA69	0	1	1	1	1	1	0	x	x	x
	32	1EFFFFH 1E8000H	SA68	0	1	1	1	1	0	1	x	x	x
	32	1E7FFFH 1E0000H	SA67	0	1	1	1	1	0	0	x	x	x
	32	1DFFFFH 1D8000H	SA66	0	1	1	1	0	1	1	x	x	x
	32	1D7FFFH 1D0000H	SA65	0	1	1	1	0	1	0	x	x	x
	32	1CFFFFH 1C8000H	SA64	0	1	1	1	0	0	1	x	x	x
	32	1C7FFFH 1C0000H	SA63	0	1	1	1	0	0	0	x	x	x
	32	1BFFFFH 1B8000H	SA62	0	1	1	0	1	1	1	x	x	x
	32	1B7FFFH 1B0000H	SA61	0	1	1	0	1	1	0	x	x	x
	32	1AFFFFH 1A8000H	SA60	0	1	1	0	1	0	1	x	x	x
	32	1A7FFFH 1A0000H	SA59	0	1	1	0	1	0	0	x	x	x
	32	19FFFFH 198000H	SA58	0	1	1	0	0	1	1	x	x	x
	32	197FFFH 190000H	SA57	0	1	1	0	0	1	0	x	x	x
	32	18FFFFH 188000H	SA56	0	1	1	0	0	0	1	x	x	x
	32	187FFFH 180000H	SA55	0	1	1	0	0	0	0	x	x	x
	32	17FFFFH 178000H	SA54	0	1	0	1	1	1	1	x	x	x
	32	177FFFH 170000H	SA53	0	1	0	1	1	1	0	x	x	x
	32	16FFFFH 168000H	SA52	0	1	0	1	1	0	1	x	x	x
	32	167FFFH 160000H	SA51	0	1	0	1	1	0	0	x	x	x
	32	15FFFFH 158000H	SA50	0	1	0	1	0	1	1	x	x	x
	32	157FFFH 150000H	SA49	0	1	0	1	0	1	0	x	x	x
	32	14FFFFH 148000H	SA48	0	1	0	1	0	0	1	x	x	x
	32	147FFFH 140000H	SA47	0	1	0	1	0	0	0	x	x	x
	32	13FFFFH 138000H	SA46	0	1	0	0	1	1	1	x	x	x
	32	137FFFH 130000H	SA45	0	1	0	0	1	1	0	x	x	x
	32	12FFFFH 128000H	SA44	0	1	0	0	1	0	1	x	x	x
	32	127FFFH 120000H	SA43	0	1	0	0	1	0	0	x	x	x
	32	11FFFFH 118000H	SA42	0	1	0	0	0	1	1	x	x	x
	32	117FFFH 110000H	SA41	0	1	0	0	0	1	0	x	x	x
	32	10FFFFH 108000H	SA40	0	1	0	0	0	0	1	x	x	x
	32	107FFFH 100000H	SA39	0	1	0	0	0	0	0	x	x	x
	32	0FFFFFH 0F8000H	SA38	0	0	1	1	1	1	1	x	x	x
	32	0F7FFFH 0F0000H	SA37	0	0	1	1	1	1	0	x	x	x
	32	0EFFFFH 0E8000H	SA36	0	0	1	1	1	0	1	x	x	x
	32	0E7FFFH 0E0000H	SA35	0	0	1	1	1	0	0	x	x	x

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank B	32	0DFFFFH 0D8000H	SA34	0	0	1	1	0	1	1	x	x	x
	32	0D7FFFH 0D0000H	SA33	0	0	1	1	0	1	0	x	x	x
	32	0CFFFFH 0C8000H	SA32	0	0	1	1	0	0	1	x	x	x
	32	0C7FFFH 0C0000H	SA31	0	0	1	1	0	0	0	x	x	x
	32	0BFFFFH 0B8000H	SA30	0	0	1	0	1	1	1	x	x	x
	32	0B7FFFH 0B0000H	SA29	0	0	1	0	1	1	0	x	x	x
	32	0AFFFFH 0A8000H	SA28	0	0	1	0	1	0	1	x	x	x
	32	0A7FFFH 0A0000H	SA27	0	0	1	0	1	0	0	x	x	x
	32	09FFFFH 098000H	SA26	0	0	1	0	0	1	1	x	x	x
	32	097FFFH 090000H	SA25	0	0	1	0	0	1	0	x	x	x
	32	08FFFFH 088000H	SA24	0	0	1	0	0	0	1	x	x	x
	32	087FFFH 080000H	SA23	0	0	1	0	0	0	0	x	x	x
Bank A	32	07FFFFH 078000H	SA22	0	0	0	1	1	1	1	x	x	x
	32	077FFFH 070000H	SA21	0	0	0	1	1	1	0	x	x	x
	32	06FFFFH 068000H	SA20	0	0	0	1	1	0	1	x	x	x
	32	067FFFH 060000H	SA19	0	0	0	1	1	0	0	x	x	x
	32	05FFFFH 058000H	SA18	0	0	0	1	0	1	1	x	x	x
	32	057FFFH 050000H	SA17	0	0	0	1	0	1	0	x	x	x
	32	04FFFFH 048000H	SA16	0	0	0	1	0	0	1	x	x	x
	32	047FFFH 040000H	SA15	0	0	0	1	0	0	0	x	x	x
	32	03FFFFH 038000H	SA14	0	0	0	0	1	1	1	x	x	x
	32	037FFFH 030000H	SA13	0	0	0	0	1	1	0	x	x	x
	32	02FFFFH 028000H	SA12	0	0	0	0	1	0	1	x	x	x
	32	027FFFH 020000H	SA11	0	0	0	0	1	0	0	x	x	x
	32	01FFFFH 018000H	SA10	0	0	0	0	0	1	1	x	x	x
	32	017FFFH 010000H	SA9	0	0	0	0	0	1	0	x	x	x
	32	00FFFFH 008000H	SA8	0	0	0	0	0	0	1	x	x	x
	4	007FFFH 007000H	SA7	0	0	0	0	0	0	0	1	1	1
	4	006FFFH 006000H	SA6	0	0	0	0	0	0	0	1	1	0
	4	005FFFH 005000H	SA5	0	0	0	0	0	0	0	1	0	1
	4	004FFFH 004000H	SA4	0	0	0	0	0	0	0	1	0	0
	4	003FFFH 003000H	SA3	0	0	0	0	0	0	0	0	1	1
	4	002FFFH 002000H	SA2	0	0	0	0	0	0	0	0	1	0
	4	001FFFH 001000H	SA1	0	0	0	0	0	0	0	0	0	1
	4	000FFFH 000000H	SA0	0	0	0	0	0	0	0	0	0	0

3. Sector Group Address Table (Flash memory)

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Sector group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA0	0	0	0	0	0	0	0	0	0	0	4 Kwords (1 Sector)	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	4 Kwords (1 Sector)	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	4 Kwords (1 Sector)	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	4 Kwords (1 Sector)	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	4 Kwords (1 Sector)	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	4 Kwords (1 Sector)	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	4 Kwords (1 Sector)	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	4 Kwords (1 Sector)	SA7
SGA8	0	0	0	0	0	0	1	×	×	×	96 Kwords (3 Sectors)	SA8 – SA10
						1	0					
						1	1					
SGA9	0	0	0	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA11 – SA14
SGA10	0	0	0	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA15 – SA18
SGA11	0	0	0	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA19 – SA22
SGA12	0	0	1	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA23 – SA26
SGA13	0	0	1	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA27 – SA30
SGA14	0	0	1	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA31 – SA34
SGA15	0	0	1	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA35 – SA38
SGA16	0	1	0	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA39 – SA42
SGA17	0	1	0	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA43 – SA46
SGA18	0	1	0	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA47 – SA50
SGA19	0	1	0	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA51 – SA54
SGA20	0	1	1	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA55 – SA58
SGA21	0	1	1	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA59 – SA62
SGA22	0	1	1	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA63 – SA66
SGA23	0	1	1	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA67 – SA70

Remark × : V_{IH} or V_{IL}

(2/2)

Sector group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA24	1	0	0	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA71 – SA74
SGA25	1	0	0	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA75 – SA78
SGA26	1	0	0	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA79 – SA82
SGA27	1	0	0	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA83 – SA86
SGA28	1	0	1	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA87 – SA90
SGA29	1	0	1	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA91 – SA94
SGA30	1	0	1	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA95 – SA98
SGA31	1	0	1	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA99 – SA102
SGA32	1	1	0	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA103 – SA106
SGA33	1	1	0	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA107 – SA110
SGA34	1	1	0	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA111 – SA114
SGA35	1	1	0	1	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA115 – SA118
SGA36	1	1	1	0	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA119 – SA122
SGA37	1	1	1	0	1	×	×	×	×	×	128 Kwords (4 Sectors)	SA123 – SA126
SGA38	1	1	1	1	0	×	×	×	×	×	128 Kwords (4 Sectors)	SA127 – SA130
SGA39	1	1	1	1	1	0	0	×	×	×	96 Kwords (3 Sectors)	SA131 – SA133
						0	1					
						1	0					
SGA40	1	1	1	1	1	1	1	0	0	0	4 Kwords (1 Sector)	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	4 Kwords (1 Sector)	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	4 Kwords (1 Sector)	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	4 Kwords (1 Sector)	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	4 Kwords (1 Sector)	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	4 Kwords (1 Sector)	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	4 Kwords (1 Sector)	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	4 Kwords (1 Sector)	SA141

Remark × : V_{IH} or V_{IL}

Product ID Code (Manufacturer Code / Device Code) (Flash memory)

Product ID code	Output																
	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	HEX
Manufacturer code	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	2210H
Device code																	TBD
Sector group protection	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	01H[Note]

Note If 01H is output, the sector group is protected. If 00H is output, the sector group is unprotected.

Remark H : V_{IH}, L : V_{IL}, x : V_{IH} or V_{IL}

4. Commands (Flash memory)

This sector explains the commands of the flash memory.

Table 4-1. Command Sequence

Command sequence	Bus	1st bus Cycle		2nd bus Cycle		3rd bus Cycle		4th bus Cycle		5th bus Cycle		6th bus Cycle	
	Cycle	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset [Note1]	1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset [Note1]	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	–	–	–	–
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	–	–	–	–
Program Suspend [Note 2]	1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Program Resume [Note 3]	1	BA	30H	–	–	–	–	–	–	–	–	–	–
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend [Note 4, 5]	1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume [Note 5, 6]	1	BA	30H	–	–	–	–	–	–	–	–	–	–
Unlock Bypass Set	3	555H	AAH	2AAH	55H	555H	20H	–	–	–	–	–	–
Unlock Bypass Program [Note 7]	2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock Bypass Chip Erase [Note 7]	2	×××H	80H	×××H	10H	–	–	–	–	–	–	–	–
Unlock Bypass Sector Erase [Note 7]	2	×××H	80H	SA	30H	–	–	–	–	–	–	–	–
Unlock Bypass Reset [Note 7]	2	×××H	90H	×××H	00H[Note11]	–	–	–	–	–	–	–	–
Product ID / Sector Group Protection Information / Read Mode Register Information	3	555H	AAH	2AAH	55H	(BA) 555H	90H	IA	ID	–	–	–	–
Sector Group Protection [Note 8]	4	×××H	60H	SPA	60H	SPA	40H	SPA	SD	–	–	–	–
Sector Group Unprotect [Note 9]	4	×××H	60H	SUA	60H	SUA	40H	SUA	SD	–	–	–	–
Extra One Time Protect Sector Entry	3	555H	AAH	2AAH	55H	555H	88H	–	–	–	–	–	–
Extra One Time Protect Sector Program [Note 10]	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	–	–	–	–
Extra One Time Protect Sector Erase [Note 10]	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	EOTPSA	30H
Extra One Time Protect Sector Reset [Note 10]	4	555H	AAH	2AAH	55H	555H	90H	×××H	00H	–	–	–	–
Extra One Time Protect Sector Protection [Note 10]	4	×××H	60H	EOTPSA	60H	EOTPSA	40H	EOTPSA	SD	–	–	–	–
Read Mode Register Set	3	555H	AAH	2AAH	55H	REGD	C0H	–	–	–	–	–	–

Notes 1. Both these read / reset commands reset the device to the read mode.

2. Programming is suspended if B0H is input to the bank address being programmed to in a program operation.

3. Programming is resumed if 30H is input to the bank address being suspended to in a program-suspend operation.

4. Erasure is suspended if B0H is input to the bank address being erased in a sector erase operation.

5. Erasure is resumed if 30H is input to the bank address being suspended in a sector-erase-suspend operation.

6. If automatic erase resume and suspend are repeated at intervals of less than 100 μs, the erasure operation may not be correctly completed.

7. Valid only in the unlock bypass mode.

8. Valid only when /RESET = V_{ID} (except in the Extra One Time Protect Sector mode).

9. The command sequence that protects a sector group is excluded.

10. Valid only in the Extra One Time Protect Sector mode.

11. This command can be used even if this data is F0H.

Remarks 1. Specify address 555H or 2AAH (A10 to A0).

2. RA : Read address

RD : Read data

IA : Address input as follows

Information	A21 to A12	A11 to A3	A2 to A0
Manufacturer code	Bank address	Don't care	000
Device code	Bank address	Don't care	001
Sector group protection information	Sector group address	Don't care	010
Read mode register information	Bank address	Don't care	011

ID : Code output. Manufacturer code, device code, sector group information, refer to the **Product ID Code (Manufacturer Code / Device Code)**, read mode register information, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

PA : Program address

PD : Program data

SA : Erase sector address. The sector to be erased is selected by the combination of this address. Refer to **2. Sector Organization / Sector Address Table (Flash memory)**.

BA : Bank address. Refer to **2. Sector Organization / Sector Address Table (Flash memory).**

SPA : Sector group address to be protected. Set sector group address (SGA) and (A6, A2, A1, A0) = (V_{IL}, V_{IL}, V_{IH}, V_{IL}).

SUA : Unprotect sector group address. Set sector group address (SGA) and (A6, A2, A1, A0) = (V_{IH}, V_{IL}, V_{IH}, V_{IL}).

EOTPSA : Extra One Time Protect Sector area addresses. These addresses are 000000H to 007FFFH.

SD : Data for verifying whether sector groups read from the address specified by SPA, SUA, and EOTPSA are protected or unprotected

REGD : Read mode register information. Description for setting, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

3. The sector group address is don't care except when a program / erase address or read address are selected.

4. For the operation of the bus, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

5. × of address bit indicates V_{IH} or V_{IL}.

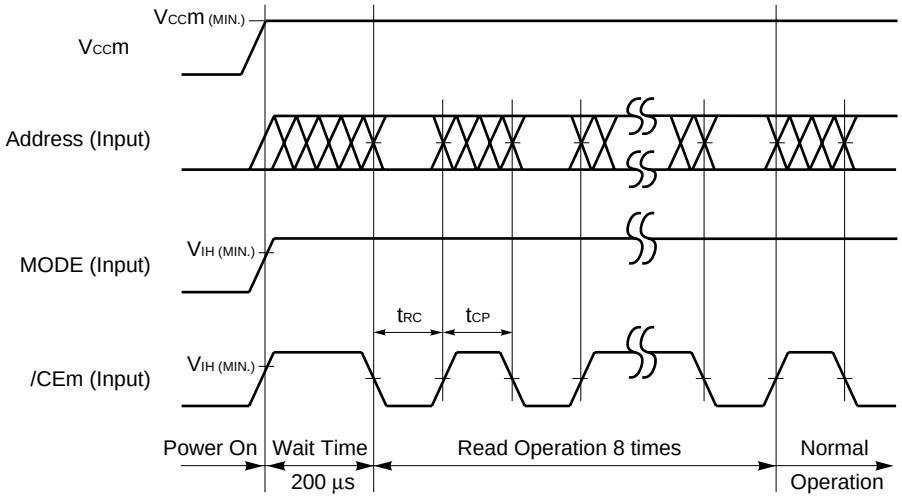
5. Initialization (Mobile specified RAM)

This device is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, before turning on the power, a 200 μs or longer wait must precede any signal toggling.

(2) After the wait time, read operation must be performed at least 8 times. After that, it can be normal operation.

Figure 5-1. Initialization Timing Chart



Cautions 1. Following power application, make MODE and /CEm high level during the wait time interval.

2. Following power application, make MODE high level during the wait time and eight read operations.

3. The read operation must satisfy the specs (Read Cycle (Mobile specified RAM)).

4. The address is don't care (V_{IH} or V_{IL}) during read operation.

5. Read operation must be executed with toggled the /CEm pin.

6. To prevent bus contention, it is recommended to set /OE to high level. However, do not input data to the I/O pins if /OE is low level during a read operation.

6. Standby Mode (Mobile specified RAM)

Standby Mode 1 and Standby Mode 2 differ as shown below.

Table 6-1. Standby Mode Characteristics

Standby Mode	Memory Cell Data Hold	Standby Supply Current (μA)
Mode 1	Valid	70 (I_{SB1})
Mode 2	Invalid	10 (I_{SB2})

6.1 Standby Mode State Machine

(1) From Active

To shift from this state to Standby Mode 1, change /CEm from V_{IL} to V_{IH}.

To shift from this state to Standby Mode 2, change /CEm from V_{IL} to V_{IH} and change MODE from V_{IH} to V_{IL}.

(2) From Standby Mode 1

To shift from this state to Active, change /CEm from V_{IH} to V_{IL}.

To shift from this state to Standby Mode 2, change MODE from V_{IH} to V_{IL}.

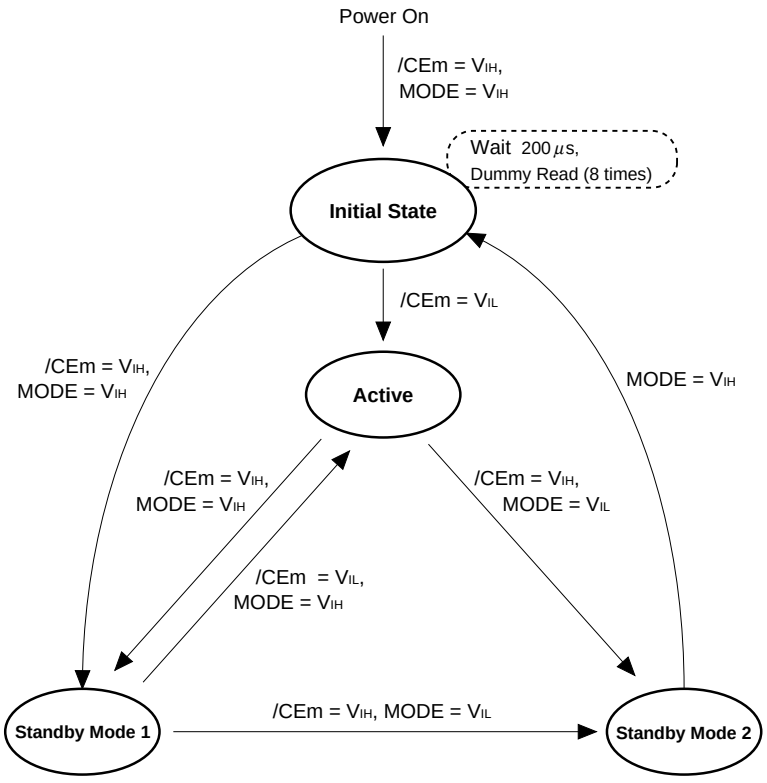
(3) From Standby Mode 2

When shifting from this state to the Active state or to Standby Mode 1, it is necessary to set MODE to V_{IH} and perform a Dummy Read operation 8 times after waiting for 200 μs, in the same way as at power application.

After shifting to Active state, change /CEm to V_{IL}.

After shifting to Standby Mode 1, do not change either MODE or /CEm.

Figure 6-1. Standby Mode State Machine



7. Electrical Specifications

Before turning on power, input $V_{SS} \pm 0.2$ V to the /RESET pin until $V_{CCf} \geq V_{CCf}$ (MIN.) and keep that state for 200 μs.

Absolute Maximum Ratings

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{CCf}	with respect to Vss		–0.5 to +2.4	V
	V_{CCm}			–0.5 to +3.3	
Input / Output supply voltage	V_{CCQf}	with respect to Vss		–0.5 to +4.0	V
Input / Output voltage	V_T	with respect to Vss	Except /WP(ACC), /RESET	–0.5 [Note 1] to V_{CCQf}, Vccm + 0.4 [Note 2] (3.3 V MAX.)	V
			/WP(ACC), /RESET	–0.5 [Note 1] to +13.0	
Ambient operation temperature	T_A			–25 to +85	°C
Storage temperature	T_{stg}			–55 to +125	°C
	T_{bias}	at bias		–25 to +85	

Notes 1. –1.0 V (MIN.) (pulse width ≤ 20 ns)

2. V_{CCQf} + 2.0 V (MAX.) (pulse width ≤ 20 ns) (Except Mobile specified RAM pins)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CCf}		1.65		1.95	V
	V_{CCm}		2.6		3.1	
Input / Output supply voltage	V_{CCQf}		2.6		3.1	V
High level input voltage	V_{IH}	Flash memory	2.0		VccQf+0.3[Note1]	V
		Mobile specified RAM	Vccmx0.8		Vccm+0.3	
	V_{ID}	/RESET	9.0		11.0	
Low level input voltage	V_{IL}	Flash memory	–0.5[Note2]		+0.8	V
		Mobile specified RAM	–0.3[Note3]		Vccmx0.2	
Accelerated programming voltage	V_{ACC}	Flash memory	8.5		9.5	V
Ambient operating temperature	T_A		–25		+85	°C

Notes 1. V_{CCQf} + 0.6 V (MAX.) (pulse width ≤ 20 ns)

2. –0.6 V (MIN.) (pulse width ≤ 20 ns)

3. –0.5 V (MIN.) (pulse width ≤ 30 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Flash memory

Parameter		Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level output voltage		V_{OH}	I_{OH} = –1.5 mA, V_{CCf} = V_{CCf} (MIN.), V_{CCQf} = V_{CCQf} (MIN.)	V_{CCQf}x0.8			V
Low level output voltage		V_{OL}	I_{OL} = 1.0 mA, V_{CCQf} = V_{CCQf} (MIN.)			V_{CCQf}x0.8	V
Input leakage current		I_{LI1}	V_I = Vss to V_{CCQf}, V_{CCQf} = V_{CCQf} (MAX.)			1.0	μA
	High voltage is applied	I_{LI2}	/RESET = 11.0 V			35	
Output leakage current		I_{LO}	V_O = Vss to V_{CCQf}, V_{CCQf} = V_{CCQf} (MAX.)			1.0	μA
Power supply current	Read	I_{CC1}	/CEf = V_{IL}, /OE = V_{IH}, Cycle = 5 MHz, I_{OUT} = 0 mA		8	15	mA
	Program, Erase	I_{CC2}	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming / read			25	mA
	Standby	I_{CC3}	V_{CCf} = V_{CCf} (MAX.), /CEf = /RESET = /WP(ACC) = V_{CCQf} ± 0.3 V, /OE = V_{IL}		15	25	μA
	Standby / Reset	I_{CC4}	V_{CCf} = V_{CCf} (MAX.), /RESET = Vss ± 0.2 V		15	25	μA
	Automatic sleep mode	I_{CC5}	V_{IH} = V_{CCQf} ± 0.2 V, V_{IL} = Vss ± 0.2 V		15	25	μA
	Read during programming	I_{CC6}	V_{IH} = V_{CCQf} ± 0.2 V, V_{IL} = Vss ± 0.2 V			40	mA
	Read during erasing	I_{CC7}	V_{IH} = V_{CCQf} ± 0.2 V, V_{IL} = Vss ± 0.2 V			40	mA
	Programming during suspend	I_{CC8}	/CEf = V_{IL}, /OEf = V_{IH}, Automatic programming during suspend			25	mA
	Accelerated programming	I_{ACC}	/WP (ACC) pin		5	10	mA
			V_{CCf}		12	25	
Low V_{CCf} lock-out voltage[Note]		V_{LKO}		1.0			V

Note When V_{CCf} is equal to or lower than V_{LKO}, the device ignores all write cycles. Refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

Mobile specified RAM

Parameter	Symbol	Test condition	Density of data hold	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}m		–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}m, /CEm = V_{IH} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
Operating supply current	I_{CCA}	/CEm = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA				35	mA
Standby supply current	I_{SB1}	/CEm ≥ V_{CC}m – 0.2 V, MODE ≥ V_{CC}m – 0.2 V	16 Mbits			70	μA
	I_{SB2}	/CEm ≥ V_{CC}m – 0.2 V, MODE ≤ 0.2 V	0 Mbit			10	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		V_{CC}m×0.8			V
Low level output voltage	V_{OL}	I_{OL} = 1 mA				V_{CC}m×0.2	V

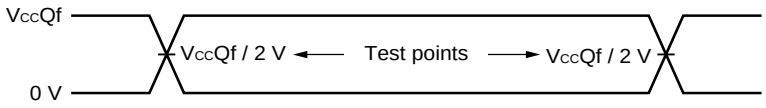
Remark V_{IN} : Input voltage, $V_{I/O}$: Input / Output voltage

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

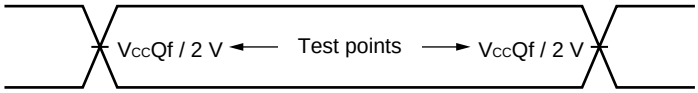
AC Test Conditions

Flash memory

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

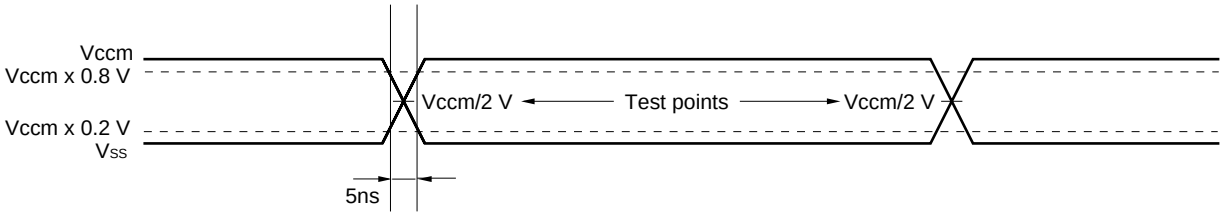


Output Load

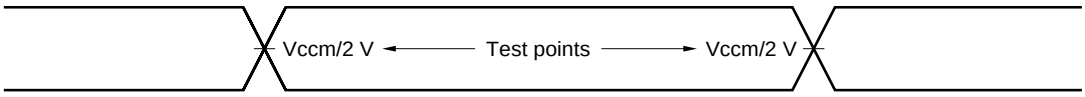
1TTL + 30 pF

Mobile specified RAM

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

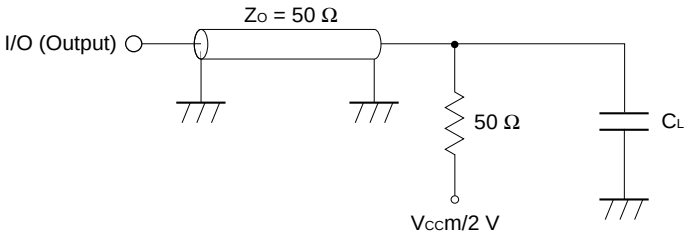


Output Load

AC characteristics directed with the note should be measured with the output load shown in Figure.

C_L: 50 pF

5 pF (t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})



/CEf, /CEm Timing

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Notes
/CEf, /CEm recover time	t_{CCR}		0			ns	

Read Cycle (Flash memory)

Parameter		Symbol	MIN.	MAX.	Unit	Notes
Read cycle time		t_{RC}	90		ns	
Address access time		t_{ACC}		90	ns	1
Page read cycle		t_{PRC}	30		ns	
Page address access time		t_{PACC}		30	ns	1
/CEf access time		t_{CEf}		90	ns	2
/OE access time		t_{OE}		25	ns	
Output disable time		t_{DF}		25	ns	
Output hold time		t_{OH}	0		ns	
/RESET pulse width		t_{RP}	500		ns	
/RESET hold time before read		t_{RH}	50		ns	
/RESET low	At automatic mode	t_{READY}		20	μs	
to read mode	Except automatic mode			500	ns	

Notes 1. /CEf = /OE = V_{IL}

2. /OE = V_{IL}

Remark t_{DF} is the time from inactivation of /CEf or /OE to Hi-Z state output.

Write Cycle (Program / Erase) (Flash memory) **(1/2)**

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Note
Write cycle time		t_{WC}	90			ns	
Address setup time (/WE to address)		t_{AS}	0			ns	
Address setup time (/CEf to address)		t_{AS}	0			ns	
Address hold time (/WE to address)		t_{AH}	45			ns	
Address hold time (/CEf to address)		t_{AH}	45			ns	
Input data setup time		t_{DS}	45			ns	
Input data hold time		t_{DH}	0			ns	
/OE hold time	Read	t_{OEH}	0			ns	
	Toggle bit, Data polling		10				
Read recovery time before write (/OE to /CEf)		t_{GHEL}	0			ns	
Read recovery time before write (/OE to /WE)		t_{GHWL}	0			ns	
/WE setup time (/CEf to /WE)		t_{WS}	0			ns	
/CEf setup time (/WE to /CEf)		t_{CS}	0			ns	
/WE hold time (/CEf to /WE)		t_{WH}	0			ns	
/CEf hold time (/WE to /CEf)		t_{CH}	0			ns	
Write pulse width		t_{WP}	35			ns	
/CEf pulse width		t_{CP}	35			ns	
Write pulse width high		t_{WPH}	30			ns	
/CEf pulse width high		t_{CPH}	30			ns	
Word programming operation time		t_{WPG}		11	TBD	μs	
Chip programming operation time		t_{CPG}		47	TBD	s	
Sector erase operation time	4K words sector	t_{SER}		0.3	1.0	s	1,2
	32K words sector			0.5	1.5		
	4K words sector			0.5	3.0		1,3
	32K words sector			0.7	5.0		
Chip erase operation time		t_{CER}		67.8	205	s	1,2
				96.2	678		1,3
Accelerated programming time		t_{ACCPG}		7	TBD	μs	
Erase / Program cycle			100,000	1,000,000		cycles	
V_{CC}f setup time		t_{VCS}	200			μs	
RY (/BY) recovery time		t_{RB}	0			ns	
/RESET pulse width		t_{RP}	500			ns	
/RESET high-voltage (V_{ID}) hold time from high of RY(/BY) when sector group is temporarily unprotect		t_{RRB}	20			μs	
/RESET hold time		t_{RH}	50			ns	
From completion of automatic program / erase to data output time		t_{EOE}			70	ns	

Notes 1. The preprogramming time prior to the erase operation is not included.

2. Erase / program cycle : 100,000 cycle

3. Erase / program cycle : 1,000,000 cycle

Write Cycle (Program / Erase) (Flash memory) (2/2)

Parameter		MIN.	TYP.	MAX.	Unit	Note
RY (/BY) delay time from valid program or erase operation	t_{BUSY}	90			ns	
Address setup time to /OE low in toggle bit	t_{ASO}	15			ns	
Address hold time to /CEf or /OE high in toggle bit	t_{AHT}	0			ns	
/CEf pulse width high for toggle bit	t_{CEPH}	20			ns	
/OE pulse width high for toggle bit	t_{OEPH}	20			ns	
Voltage transition time	t_{VLHT}	4			μs	1
Rise time to V_{ID} (/RESET)	t_{VIDR}	500			ns	
Rise time to V_{ACC} (/WP(ACC))	t_{VACCR}	500			ns	
Erase timeout time	t_{TOW}	50			μs	2
Erase suspend transition time	t_{SPD}			20	μs	2

Notes 1. Sector group protection only.

2. Table only.

Write operation (Erase / Program) Performance

Parameter	Description		MIN.	TYP.	MAX.	Unit	Note
Sector erase time	Excludes programming time prior to erasure	4K words sector		0.3	1.0	s	1
		32K words sector		0.5	1.5		
		4K words sector		0.5	3.0		2
		32K words sector		0.7	5.0		
Chip erase time	Excludes programming time prior to erasure			67.8	205	s	1
				96.2	678		2
Word programming time	Excludes system-level overhead			11	TBD	μs	
Chip programming time	Excludes system-level overhead			47	TBD	s	
Accelerated programming time	Excludes system-level overhead			7	TBD	μs	
Erase / Program cycle			100,000	1,000,000		cycles	

Notes 1. Erase / program cycle : 100,000 cycle

2. Erase / program cycle : 1,000,000 cycle

Read Cycle (Mobile specified RAM)

Parameter	Symbol	MC-24212361-E90X		MC-24212361-E95X		MC-24212361-E10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	80	10,000	90	10,000	110	10,000	ns	1
Identical address read cycle time	t_{RC1}	80	10,000	90	10,000	110	10,000	ns	2
Address skew time	t_{SKEW}		10		15		20	ns	3
/CEm pulse width	t_{CP}	10		10		10		ns	
Address access time	t_{AA}		80		90		100	ns	4
/CEm access time	t_{ACS}		80		90		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	5
/LB, /UB to output valid	t_{BA}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CEm to output in low impedance	t_{CLZ}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	5		5		5		ns	
/CEm to output in high impedance	t_{CHZ}		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		25		25	ns	

Notes 1. One read cycle (t_{RC}) must satisfy the minimum value ($t_{RC(MIN.)}$) and maximum value ($t_{RC(MAX.)}$ = 10 μs). t_{RC} indicates the time from the /CEm low level input point or address determination point, whichever is later, to the /CEm high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{RC}.

1) Time from address determination point to /CEm high level input point (address access)
2) Time from address determination point to next address change start point (address access)
3) Time from /CEm low level input point to next address change start point (/CEm access)
4) Time from /CEm low level input point to /CEm high level input point (/CEm access)

2. The identical address read cycle time (t_{RC1}) is the cycle time of one read operation when performing continuous read operations toggling /OE , /LB, and /UB with the address fixed and /CEm low level. Perform settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CEm from high level to low level, t_{SKEW} is the time from the /CEm low level input point until the next address is determined.
2) When switching /CEm from low level to high level, t_{SKEW} is the time from the address change start point to the /CEm high level input point.
3) When /CEm is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CEm is active, t_{SKEW} is not subject to limitations when /CEm is switched from high level to low level following address determination, or when the address is changed after /CEm is switched from low level to high level.

4. Regarding t_{AA} and t_{ACS}, only t_{AA} is satisfied during address access (refer to 1) and 2) of **Note 1**), and only t_{ACS} is satisfied during /CEm access (refer to 3) of **Note 1**).

5. Regarding t_{BA} and t_{OE}, only t_{BA} is satisfied if /OE becomes active later than /UB and /LB, and only t_{OE} is satisfied if /UB and /LB become active before /OE.

Write Cycle (Mobile specified RAM)

Parameter	Symbol	MC-24212361-E90X		MC-24212361-E95X		MC-24212361-E10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	80	10,000	90	10,000	110	10,000	ns	1
Identical address write cycle time	t_{WC1}	80	10,000	90	10,000	110	10,000	ns	2
Address skew time	t_{SKEW}		10		15		20	ns	3
/CEm to end of write	t_{CW}	40		50		60		ns	4
/LB, /UB to end of write	t_{BW}	30		35		40		ns	
Address valid to end of write	t_{AW}	35		45		55		ns	
Write pulse width	t_{WP}	30		35		40		ns	
Write recovery time	t_{WR}	20		20		20		ns	5
/CEm pulse width	t_{CP}	10		10		10		ns	
Address setup time	t_{AS}	0		0		0		ns	
Byte write hold time	t_{BWH}	20		20		20		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/WE to output in high impedance	t_{WHZ}		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25	ns	
Output active from end of write	t_{OW}	5		5		5		ns	

Notes 1. One write cycle (t_{WC}) must satisfy the minimum value ($t_{WC(MIN.)}$) and the maximum value ($t_{WC(MAX.)}$ = 10 μs). t_{WC} indicates the time from the /CEm low level input point or address determination point, whichever is after, to the /CEm high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{WC}.

1) Time from address determination point to /CEm high level input point
2) Time from address determination point to next address change start point
3) Time from /CEm low level input point to next address change start point
4) Time from /CEm low level input point to /CEm high level input point

2. The identical address read cycle time (t_{WC1}) is the cycle time of one write cycle when performing continuous write operations with the address fixed and /CEm low level, changing /LB and /UB at the same time, and toggling /WE, as well as when performing a continuous write toggling /LB and /UB. Make settings so that the sum (t_{WC}) of the identical address write cycle times (t_{WC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CEm from high level to low level, t_{SKEW} is the time from the /CEm low level input point until the next address is determined.
2) When switching /CEm from low level to high level, t_{SKEW} is the time from the address change start point to the /CEm high level input point.
3) When /CEm is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CEm is active, t_{SKEW} is not subject to limitations when /CEm is switched from high level to low level following address determination, or when the address is changed after /CEm is switched from low level to high level.

4. Definition of write start and write end

	/CEm	/WE	/LB, /UB	Status
Write start pattern 1	H to L	L	L	If /WE, /LB, /UB are low level, time when /CEm changes from high level to low level
Write start pattern 2	L	H to L	L	If /CEm, /LB, /UB are low level, time when /WE changes from high level to low level
Write start pattern 3	L	L	H to L	If /CEm, /WE are low level, time when /LB or /UB changes from high level to low level
Write end pattern 1	L	L to H	L	If /CEm, /WE, /LB, /UB are low level, time when /WE changes from low level to high level
Write end pattern 2	L	L	L to H	When /CEm, /WE, /LB, /UB are low level, time when /LB or /UB changes from low level to high level

5. Definition of write end recovery time (t_{WR})

1) Time from write end to address change start point, or from write end to /CEm high level input point
2) When /CEm, /LB, /UB are low level and continuously written to the identical address, time from /WE high level input point to /WE low level input point
3) When /CEm, /WE are low level and continuously written to the identical address, time from /LB or /UB high level input point, whichever is later, to /LB or /UB low level input point, whichever is earlier.
4) When /CEm is low level and continuously written to the identical address, time from write end to point at which /WE , /LB, or /UB starts to change from high level to low level, whichever is earliest.

Read Write Cycle (Mobile specified RAM)

Parameter	Symbol	MC-24212361-E90X		MC-24212361-E95X		MC-24212361-E10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read write cycle time	t_{RWC}		10,000		10,000		10,000	ns	1, 2
Byte write setup time	t_{BWS}	20		20		20		ns	
Byte read setup time	t_{BRS}	20		20		20		ns	

Notes 1. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

2. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a read is performed at the identical address using /UB following a write using /LB with /CEm low level, or when a read is performed using /LB following a write using /UB.

Standby Mode Entry / Exit (Mobile specified RAM)

Parameter	Symbol	MC-24212361-E90X		MC-24212361-E95X		MC-24212361-E10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
/CEm High to MODE Low	t_{CM}	0		0		0		ns	

Cautions 1. Make MODE and /CEm high level during the wait time.

2. Make MODE high level during the wait time and three read operations.

3. The read operation must satisfy the read cycle specs.

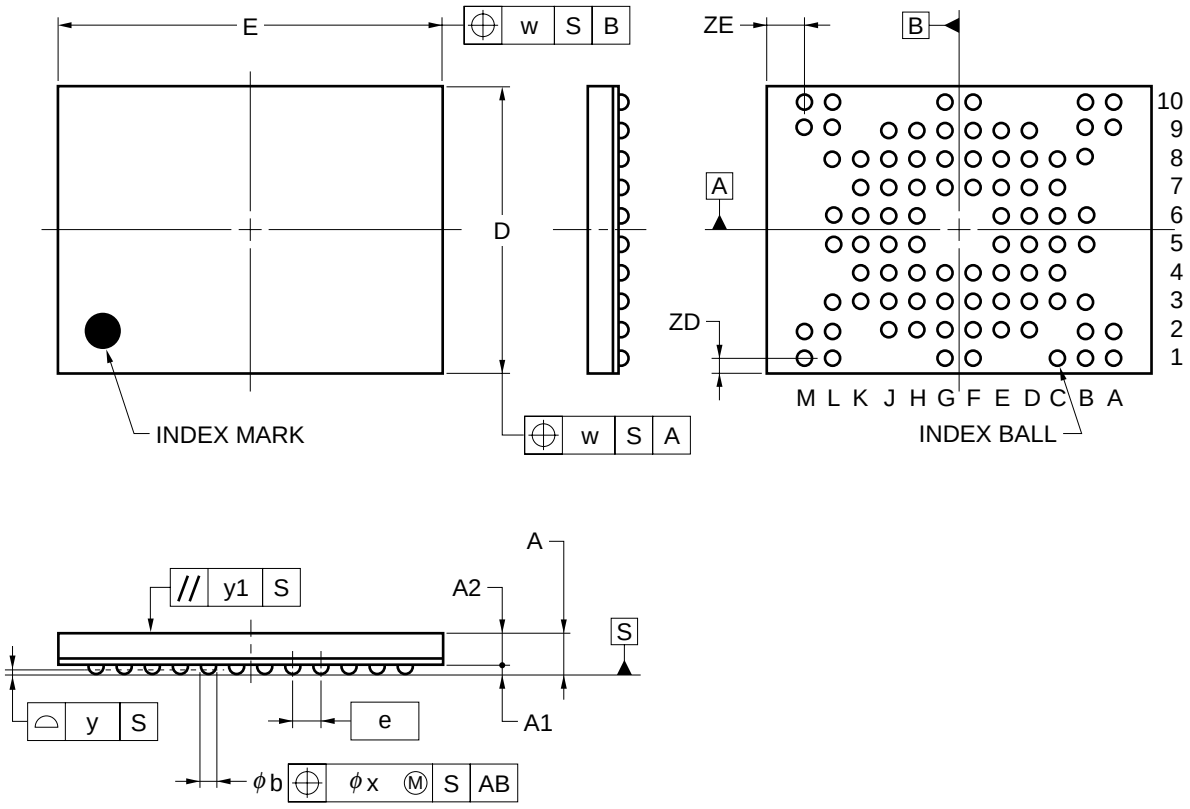
4. The read operation address can be either V_{IH} or V_{IL}.

5. Perform reading by toggling /CEm.

6. To prevent bus contention, it is recommended to set /OE to high level. However, do not input data to the I/O pins if /OE is low level during a read operation.

8. Package Drawing

85-PIN TAPE FBGA (11x8)



This package drawing is a preliminary version. It may be changed in the future.

ITEM	MILLIMETERS
D	8.0
E	11.0
w	0.2
e	0.8
A	1.12
A1	0.27
A2	0.85
b	0.45
x	0.08
y	0.1
y1	0.1
ZD	0.4
ZE	1.1

9. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the MC-24212361-X.

Types of Surface Mount Device

MC-24212361F9-E90X-CDx : 85-pin TAPE FBGA (11 × 8)
MC-24212361F9-E95X-CDx : 85-pin TAPE FBGA (11 × 8)
MC-24212361F9-E10X-CDx : 85-pin TAPE FBGA (11 × 8)

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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