EMBEDDED IOT SOLUTIONS | NEURON PROCESSORS

Neuron 6050 Processor

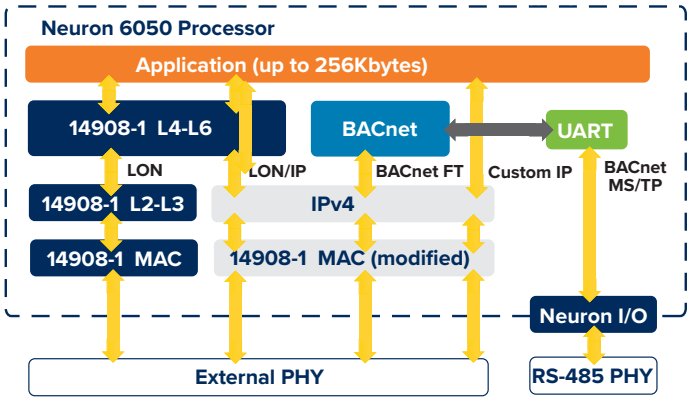


Figure 1. Neuron 6050 Firmware Protocol Stacks

Product Description

The Neuron® 6050 Processor is a single chip control and IP communication processor for modernizing and consolidating smart control networks. It is a key product in Adesto's IzoT® platform — the most comprehensive and open control networking platform for the Industrial Internet of Things (IIoT). It offers compatibility with the large installed base of LON and BACnet MS/TP devices while adding support for LON/IP and BACnet/IP communication. It is designed to bring unprecedented flexibility and openness while lowering development and device costs.

The Neuron 6050 features a high-performance Neuron core. Using an inexpensive flash memory and external communication transceiver, the Neuron 6050 Processor provide a very flexible, low-cost, feature-enhanced LON, BACnet MS/TP, LON/IP, and BACnet/IP solution all within the same device with a single application.

A rich set of LonMark and IoT standard profiles and data types is included that you can use to further reduce application development time.

The Neuron 6050 includes four independent 8-bit logical processors to manage the physical MAC layer, the communication protocol stacks, the user application, and interrupts (see Figure 2, on page 2).

The Neuron 6050 interfaces with an external communication transceiver using a 5-pin network communications port with 3.3V drive and 5V-tolerant pins. A variety of external transceivers can be used including an RS-485 transceiver, ISM-RF wireless transceiver,

Features

- Built-in LON, LON/IP, BACnet/IP, and BACnet MS/TP stacks provide compatibility with millions of LON and BACnet devices and enabling IP access to every Neuron 6050 based device
- Low-cost and royalty-free IzoT FT 6000 EVK available for rapid application development and testing
- Free and royalty-free IzoT SDKs available for simple integration with other processors
- 5-pin network communications port with 3.3V drive and 5V-tolerant pins
- Integrated quad core processor supports applications up to 256KB for a 5x increase over previous generations
- Supports up to 254 network variables (NVs), 127 aliases and 254 address table entries (16x increase)
- Neuron core supports easy migration of existing applications written for previous generation Neuron chips and smart transceivers
- Up to 80MHz system clock provides up to a 16x performance improvement over previous generations
- On-chip 64KB RAM and 16KB ROM

PRODUCT DESCRIPTION

HD-PLC high-speed power line transceiver, Adesto TPT/XF- 1250 1.25Mbps twisted pair transceiver, or Adesto LPT-11 78kbps link power transceiver.

Multi-Protocol Operation

The Neuron 6050 simultaneously supports up to four different communication protocols, as shown in Figure 1 (on page 1), allowing device makers unprecedented flexibility in creating control devices for a wide variety of applications using one application. Backward compatibility and future proofing can both be met using a common platform based on the Neuron 6050.

For LON communication, the Neuron 6050 implements the complete LON stack as defined by ISO/IEC 14908-1 and is fully backward compatible with devices running the LON stack, including devices based on the Neuron 3120, Neuron 3150, or the FT 3120, FT 3150, or FT 5000 Smart Transceiver.

For LON/IP communication, the Neuron 6050 implements layers 4 through 7 of the ISO/IEC 14908-1 LON stack running on top of layers 2 and 3 of a UDP/IP stack. This allows the implementation of devices that are fully compatible with classic LON applications while supporting native IP addressing at the device level. This allows LON compatible applications to run unmodified while gaining IP addressing at the device level.

For BACnet/IP communication, the Neuron 6050 implements a BACnet/IP standard stack running on top of layers 2 and 3 of a UDP/IP stack. This enables BACnet/IP-compliant applications to run on the attached communication channel, pushing BACnet/IP all the way down to the simplest of devices, while leveraging the ease-of-installation provided by LON commissioning tools. Devices thus provisioned are fully compatible and discoverable using industry standard, BTL certified, BACnet management clients.

For BACnet MS/TP communication, the Neuron 6050 implements a BACnet MS/ TP stack that uses one of the Neuron 6050 USARTS to communicate with an external RS-485 transceiver using the BACnet MS/ TP protocol. This enables BACnet MS/TP-compliant applications to be implemented in parallel with LON, LON/IP, and BACnet/ IP applications running on the Neuron 6050.

For other IP applications, the Neuron 6050 implements a UDP/IP stack that an application can use to create any type of IP interface that communicates with the attached channel.

Compatibility

The Neuron 6050 is fully compliant with LON devices implementing the ISO/IEC 14908-1 protocol.

The Neuron core in the Neuron 6050 uses the same instruction set and architecture as the previous- generation Neuron core, including instructions for hardware multiplication and division. The Neuron core is source code compatible with applications written for the Series 5000 and 3100 Neuron core.

Features, continued

- 3.3V operation
- User-programmable interrupts, hardware USART, and 12 GPIO pins with 35 configurable I/O drivers
- Supports a rich set of LonMark® and IoT standard profiles and data types to reduce application development time
- Flash file system for data logging and other applications requiring persistent storage
- Unique 48-bit IEEE MAC ID
- 7mm x 7mm 48-pin QFN package
- -40°C to 85°C industrial temperature range

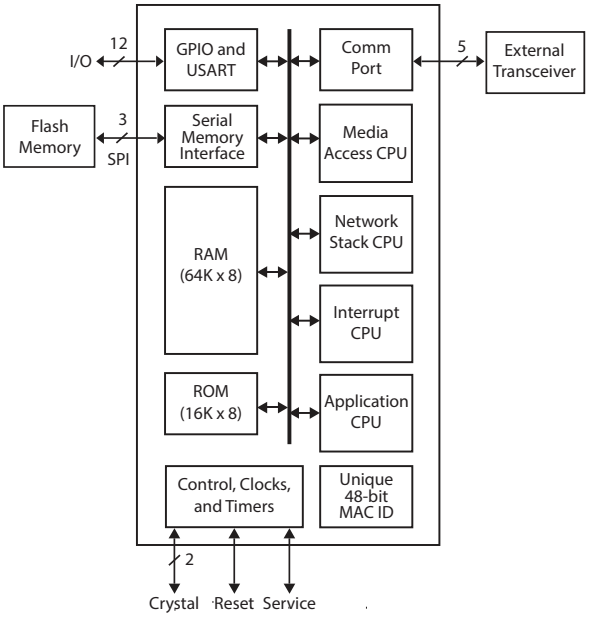


Figure 2. Neuron 6050 Processor

Enhanced Performance

Neuron Core Speed

The internal system clock for the Neuron 6050 can be configured to run from 5MHz to 80MHz. The required external crystal provides a 10MHz clock frequency, and an internal PLL boosts the frequency to a maximum of 80MHz as the internal system clock speed. The Neuron 3120/3150 core divided the external

oscillator frequency by two to create the internal system clock. An Neuron 6050 running with an 80MHz internal system clock is thus 16 times faster than a 10MHz Neuron 3120 or Neuron 3150 core.

The Neuron core inside the Neuron 6050 includes a built-in hardware multiplier and divider to increase the performance of arithmetic operations.

Higher Protocol Limits

The Neuron 6050 Processor supports up to 254 network variables per application, up to 127 aliases, and up to 254 address table entries. This is a significant increase over the previous limits of 62 network variables, 62 aliases, and 15 address table entries which simplifies network installation and supports more complex applications.

Interrupts

The Neuron 6050 lets developers define application interrupts to handle asynchronous events triggered by selected state changes on any of the 12 GPIO pins, by on-chip hardware timer-counter units, or by an on-chip high-performance hardware system timer.

MAC Layer Enhancements

The Neuron 6050 has an enhanced MAC layer that allows frame sizes up to 1280 bytes. This allows large IP frames to be carried over the communication channel without fragmenting the packet to provide better bandwidth utilization of the channel.

The dedicated processor cores for the MAC and network protocol support allows the application to have the same performance independent of the network traffic. Traditional uni-processor designs running popular transceivers such as RS-485 must be interrupted repeatedly to receive every packet on the network, even when the packet turns out to not be addressed to the device. This increases the demands on the application processor and makes the amount of processing available to the application difficult to predict as it becomes a function of the network load.

JTAG Interface

The Neuron 6050 provides an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG) to allow an Neuron 6050 chip to be included in the boundary-scan chain for device production tests.

GPIO

The Neuron 6050 provides 12 bidirectional GPIO pins that are 5V-tolerant and can be configured to operate in one or more of 35 predefined standard input/output modes. The chip also has two 16-bit timer/counters and a hardware USART that reduce the need for external logic and software development.

Memory Architecture

The Neuron 6050 eliminates the need for external serial EEPROM that the previous generation Neuron 5000 required and instead relies only on inexpensive external flash memories for non-volatile application and data storage, and for Neuron firmware upgrades. It has 16KB of ROM and 64KB (44KB user-accessible) of RAM on the chip. Each chip, contains a unique identifier (IEEE MAC ID) in an on-chip, non-volatile, read-only memory. Typical external flash memory configuration is 1MB of which 256KB is available for application code. This is a five-fold increase in application size that can be hosted on the Neuron 6050 compared to previous generations.

The application code and configuration data are stored in the external non-volatile memory (NVM) and copied into the internal RAM during device reset; the instructions then execute from internal RAM. Writes to NVM are shadowed in the internal RAM and pushed out to external NVM by the Neuron firmware.

The Neuron 6050 supports serial peripheral interface (SPI) for accessing off-chip, non-volatile memory.

The Neuron 6050 Processor supports a variety of flash devices; we recommend:

Adesto AT25SF041 or Adesto AT25SF081

Adesto has also qualified the following SPI flash memory devices for use with the FT 6050 Smart Transceiver: Macronix MX25L8035E, Micron M25PX80, ON Semiconductor LE25U40CM, Winbond W25X40CL, Winbond W25Q80BV.

Noise Immunity

A LON device based on the Neuron 6050 is composed of two components: the Neuron 6050 and an external communications transceiver such as an RS-485 transceiver, ISM-RF wireless transceiver, HD-PLC high-speed power line transceiver, Adesto TPT/ XF-1250 1.25Mbps twisted pair transceiver, or Adesto LPT-11 78kbps link power transceiver.

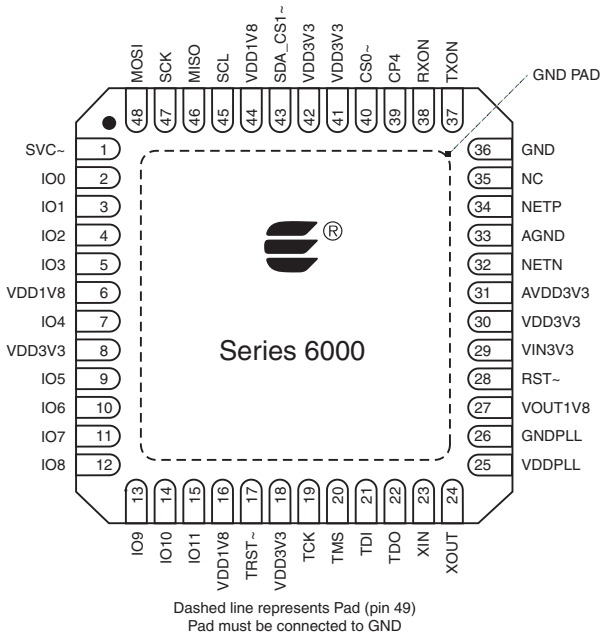


Figure 3. 6K IC Pin Configuration

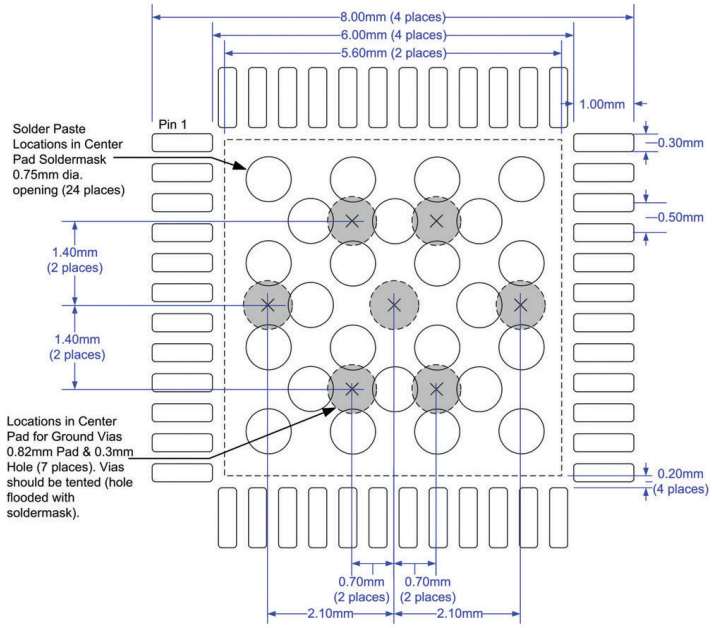
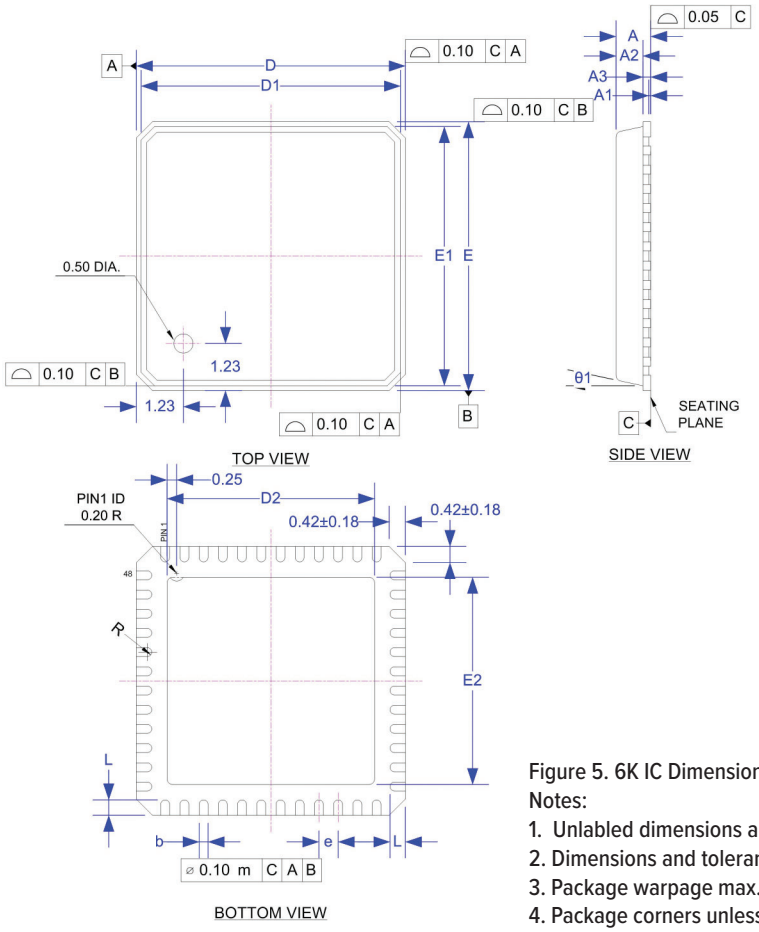


Figure 4. Recommended 6K Pad Layout

6K IC MECHANICAL SPECIFICATIONS



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00 bsc			0.276 bsc		
D1	6.75 bsc			0.266 bsc		
D2	5.20	5.40	5.60	0.205	0.213	0.220
E	7.00 bsc			0.276 bsc		
E1	6.75 bsc			0.266 bsc		
E2	5.20	5.40	5.60	0.205	0.213	0.220
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure 5. 6K IC Dimensions

Notes:

1. Unlabled dimensions are in millimeters.
2. Dimensions and tolerances conform to ASME Y14.5M.-1994.
3. Package warpage max. 0.08 mm.
4. Package corners unless otherwise specified are R0.175±0.025 mm.

6K TAPE AND REEL INFORMATION

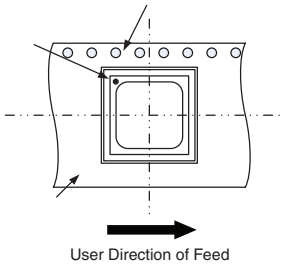


Figure 6. 6K Tape and Reel Orientation

Note: 6K ICs are uniformly loaded in the carrier tape such that pin 1 is oriented in quadrant 1 toward the side of the tape having round sprocket holes.

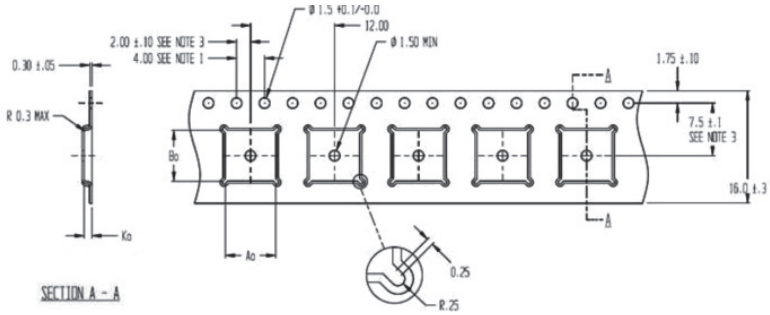
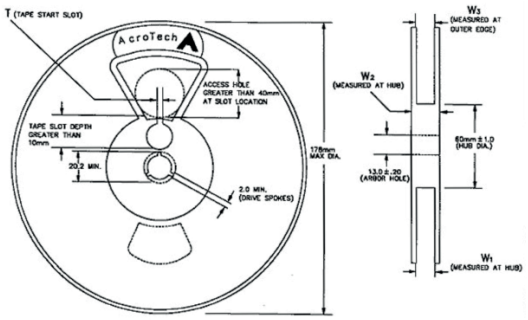


Figure 7. 6K Carrier Tape Outline

Notes:
1. All dimensions in mm
2. Tolerances unless noted: 1PL + 0.2. 2PL + 0.1
3. 10 Sprocket hole pitch cumulative tolerance +0.2
4. Camber compliant with EIA 481
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

For more information, refer to EIA-481-B, “Taping of Surface Mount Components for Automatic Placement”



TAPE SIZE	T	W1	W2	W3
8mm	4.0 ±0.25	+1.5 8.4–0.0	14.4 MAX.	7.9 MIN. 10.9 MAX.
12mm	5.0 ±0.50	+2.0 12.4–0.0	18.4 MAX.	11.9 MIN. 15.4 MAX.
16mm	7.0 ±0.50	+2.0 16.4–0.0	22.4 MAX.	15.9 MIN. 19.4 MAX.
24mm	11.0 ±0.50	+2.0 24.4–0.0	30.4 MAX.	23.9 MIN. 27.4 MAX.
32mm	11.0 ±0.50	+2.0 32.4–0.0	38.4 MAX.	31.9 MIN. 35.4 MAX.
44mm	11.0 ±0.50	+2.0 44.4–0.0	50.4 MAX.	43.9 MIN. 47.4 MAX.

Figure 8. 6K 7” Reel and Hub Dimensions

APPLICATION DEVELOPMENT

A typical Neuron 6050-based device requires a power source, crystal, external memory, external transceiver, and an I/O interface to the device being controlled (see Figure 9).

Adesto provides all of the building blocks required to successfully design and field cost-effective, robust products based on the Neuron 6050. Adesto's end-to-end solutions include a comprehensive set of development tools (described below), network interfaces, routers, and network tools. In addition, pre-production design review services, training, and worldwide technical support (including onsite support) are available through Adesto's technical assistance program.

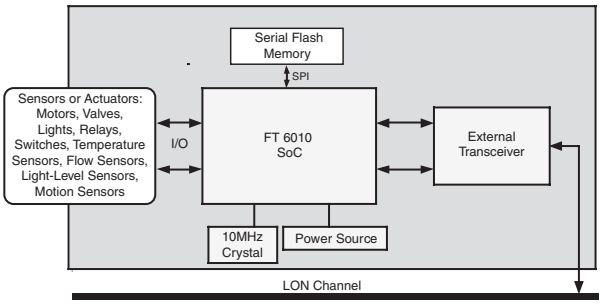


Figure 9. Typical Neuron 6050-based Device

IzoT FT 6000 EVK — a complete hardware and software platform for creating or evaluating LON, LON/IP, BACnet FT, and BACnet MS/TP devices based on an Adesto Neuron chip or smart transceiver. Using the FT 6000 EVK, developers can create applications that run on the Neuron 6050 using the highly productive Neuron C programming language.

IzoT SDK Premium Edition — a software development kit that enables developers to build communicating devices using any processor that runs Linux for the application and Layers 3 through 7 of the LON/IP and LON protocol stacks. The IzoT SDK Premium Edition includes royalty-free firmware for the Neuron 6050 that enables the Neuron 6050 to be used as a PHY chip to interface to a network communications channel.

IzoT ShortStack SDK — a free software development kit, available at github.com/izot/shortstack, that enables developers to build communicating devices using any processor that can run the application plus a tiny IzoT ShortStack driver. The IzoT ShortStack SDK includes royalty-free firmware for the Neuron 6050 that enables the Neuron 6050 to be used as a Layer 2 to 6 LON and LON/IP protocol processor with external transceiver interface to a network communications channel.

PRODUCT SPECIFICATIONS

EMI
Compliant with FCC Part 15 Subpart B and EN55022 Level B

ESD
Compliant with EN 61000-4-2, Level 4

Radiated Electromagnetic Susceptibility
Compliant with EN 61000-4-3, Level 3

Fast Transient/Burst Immunity
Compliant with EN 61000-4-4, Level 4

Surge Immunity
Compliant with EN 61000-4-5, Level 3

Conducted RF Immunity
Compliant with EN 61000-4-6, Level 3

Operating Temperature
-40° to 85°C

Reflow Soldering Temperature Profile
Refer to *Joint Industry Standard IPC/JEDEC J-STD-020D.1* (March 2008)

Peak Reflow Soldering Temperature
260°C

Model #	Product Name	Product Description
14550R-500	Neuron 6050 Processor	Tape and reel package, quantity 500
10070R-43-54	IzoT FT 6000 EVK	Hardware and software development kit
23360-10	IzoT SDK Premium Edition	Software development kit
23400-FV	IzoT Short Stack SDK	Software development kit available at www.github.com/izot/shortstack

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