To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

NP100N04MDH, NP100N04NDH, NP100N04PDH

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP100N04MDH, NP100N04NDH, NP100N04PDH are N-channel MOS Field Effect Transistors designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP100N04MDH-S18-AY Note	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K) typ. 1.9 g
NP100N04NDH-S18-AY Note			TO-262 (MP-25SK) typ. 1.8 g
NP100N04PDH-E1-AY Note		Tape 800 p/reel	TO-263 (MP-25ZP) typ. 1.5 g
NP100N04PDH-E2-AY Note			

Note Pb-free (This product does not contain Pb in the external electrode.)

FEATURES

- Enhancing $T_{ch(MAX.)}$ to 200°C (Operation time until 250 Hr)
- Super low on-state resistance
  - NP100N04MDH, NP100N04NDH
    $R_{DS(on)1}$ = 3.3 mΩ MAX. (V_{GS} = 10 V, I_D = 50 A)
    $R_{DS(on)2}$ = 4.7 mΩ MAX. (V_{GS} = 4.5 V, I_D = 50 A)
  - NP100N04PDH
    $R_{DS(on)1}$ = 2.9 mΩ MAX. (V_{GS} = 10 V, I_D = 50 A)
    $R_{DS(on)2}$ = 4.3 mΩ MAX. (V_{GS} = 4.5 V, I_D = 50 A)
- High avalanche energy, High avalanche current
- Logic level drive Type
- Low input capacitance
  C_{iss} = 8700 pF TYP. (V_{DS} = 25 V)

(TO-220)

(TO-262)

(TO-263)

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Date Published December 2007 NS
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±100	A
Drain Current (pulse) (T_C = 25°C) Note1	$I_{D(pulse)}$	±400	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	288	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch1}	175	°C
Channel Temperature Note2	T_{ch2}	200	°C
Storage Temperature	T_{stg}	−55 to +175	°C
Repetitive Avalanche Current Note3	I_{AR1}	80	A
Repetitive Avalanche Current Note4	I_{AR2}	90	A
Repetitive Avalanche Energy Note5	E_{AR}	1000	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Reliability test condition

High temperature bias condition (V_{DS} = V_{DSS}, V_{GS} = 0 V, 250 Hr)

High temperature gate bias condition (V_{DS} = 0 V, V_{GS} = 12 V, 250 Hr)

<R> **3.** L = 100 μH, T_{ch} ≤ 200°C

<R> **4.** L = 10 μH, T_{ch} ≤ 200°C

5. T_{ch} ≤ 200°C, R_G = 25 Ω, V_{GS} = 12 → 0 V

THERMAL RESISTANCE

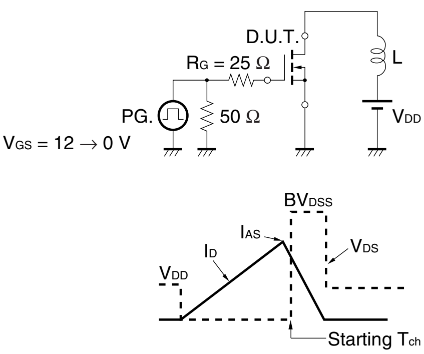
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.52	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

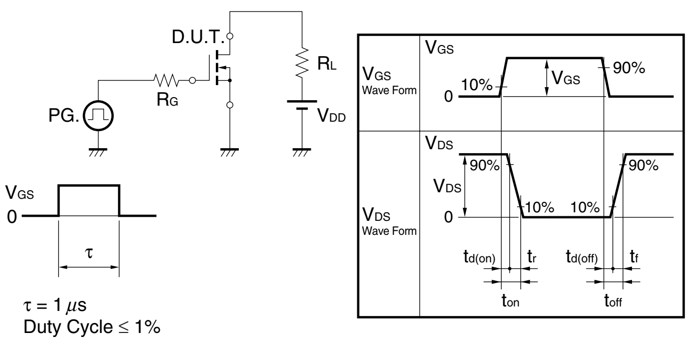
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 50 A	45	100		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 50 A NP100N04MDH, NP100N04NDH		2.6	3.3	mΩ
		V_{GS} = 10 V, I_D = 50 A NP100N04PDH		2.3	2.9	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 50 A NP100N04MDH, NP100N04NDH		3.3	4.7	mΩ
		V_{GS} = 4.5 V, I_D = 50 A NP100N04PDH		3.0	4.3	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V,		8700	13000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		1400	2100	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		410	740	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 50 A,		24	53	ns
Rise Time	t_r	V_{GS} = 10 V,		12	30	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		150	300	ns
Fall Time	t_f			16	40	ns
Total Gate Charge	Q_G	V_{DD} = 32 V,		165	250	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		27		nC
Gate to Drain Charge	Q_{GD}	I_D = 100 A		39		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 100 A, V_{GS} = 0 V		0.92	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 100 A, V_{GS} = 0 V,		65		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		100		nC

Note Pulsed

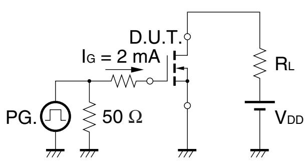
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

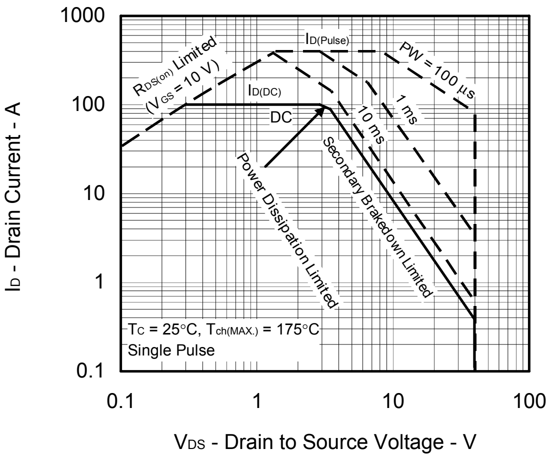


TEST CIRCUIT 3 GATE CHARGE

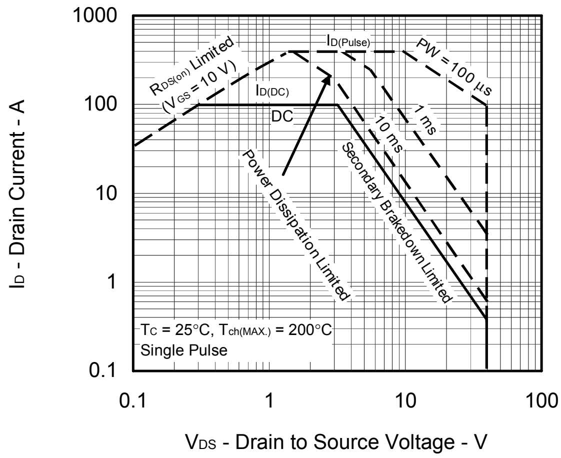


TYPICAL CHARACTERISTICS (T_A = 25°C) (NP100N04MDH)

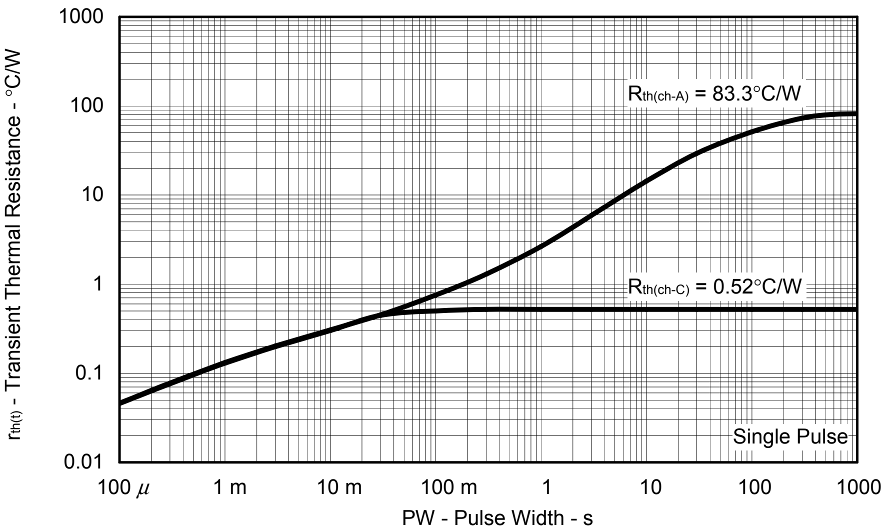
<R> FORWARD BIAS SAFE OPERATING AREA



<R> FORWARD BIAS SAFE OPERATING AREA

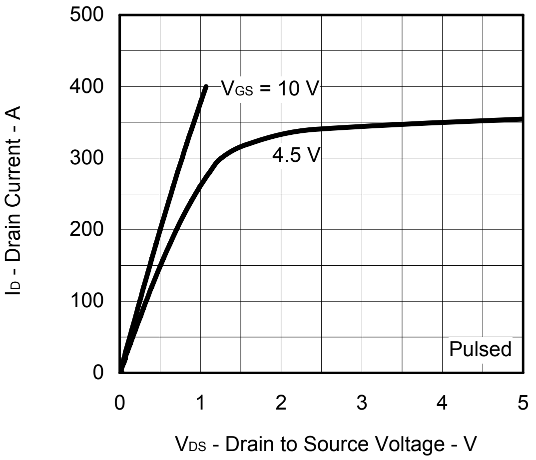


<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

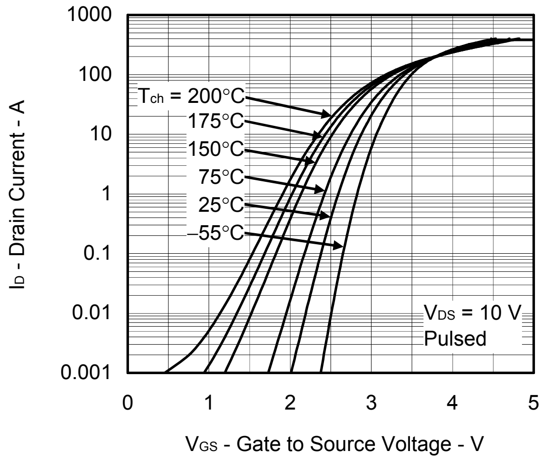


Note Confirm the operation tracks are in Safe Operating Area.

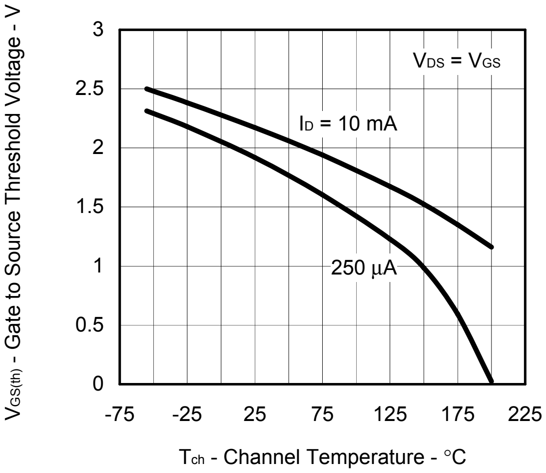
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



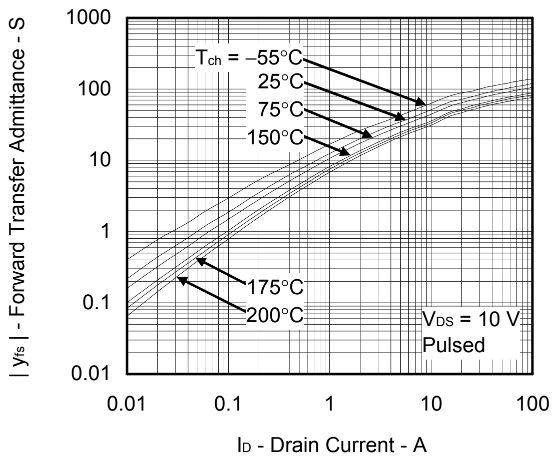
FORWARD TRANSFER CHARACTERISTICS



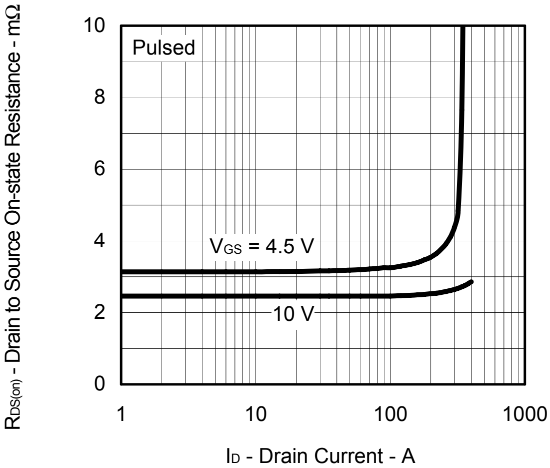
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



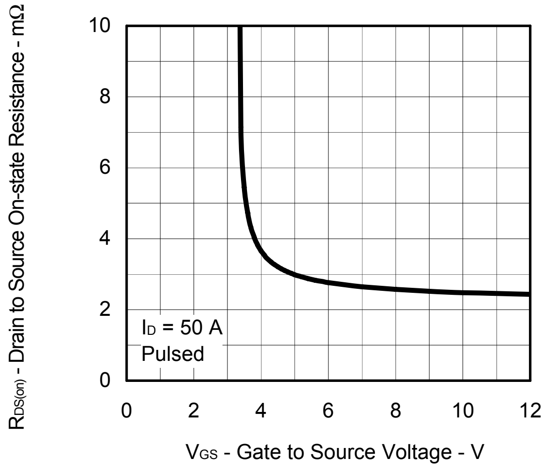
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



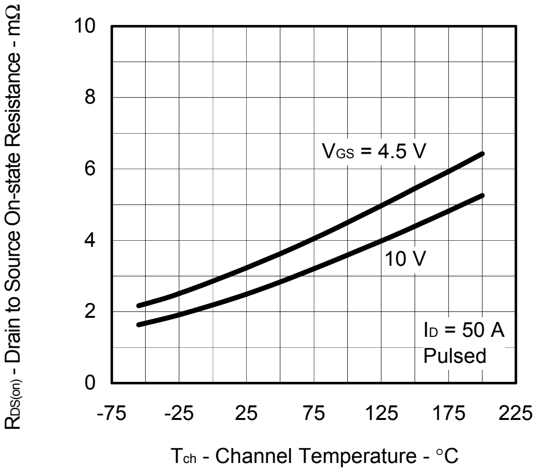
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



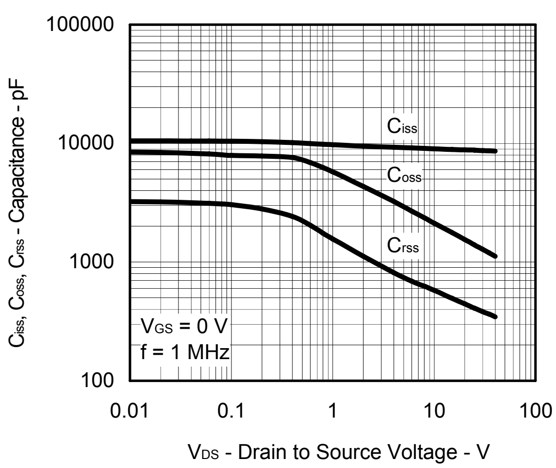
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



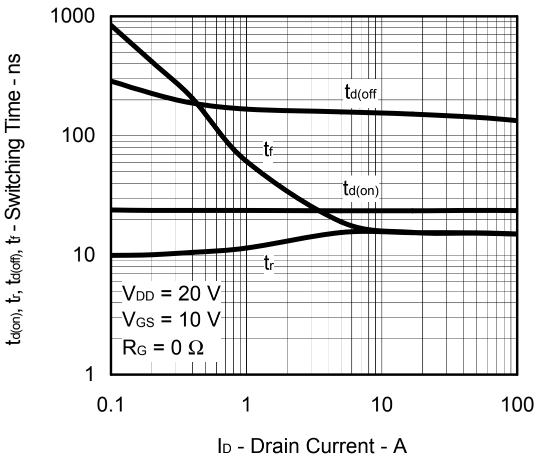
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



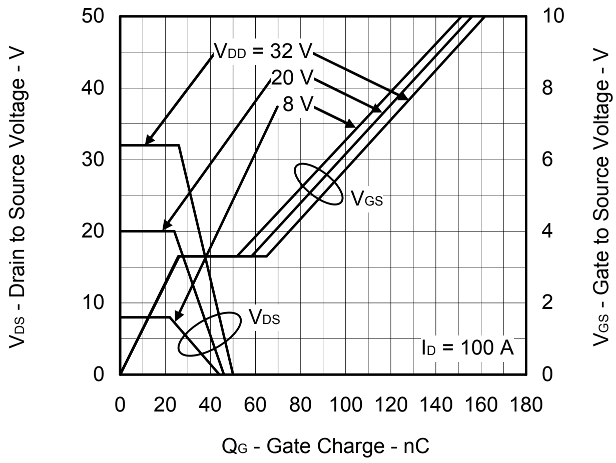
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



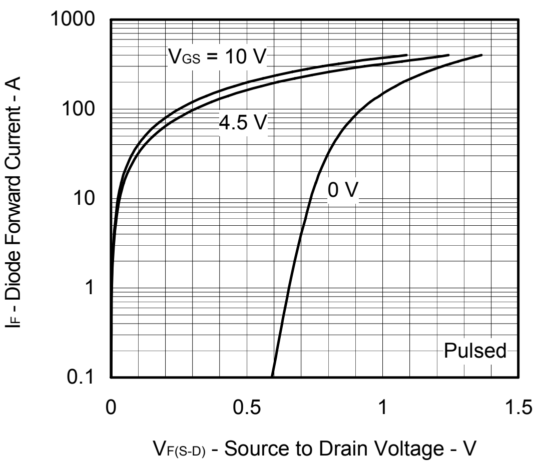
SWITCHING CHARACTERISTICS



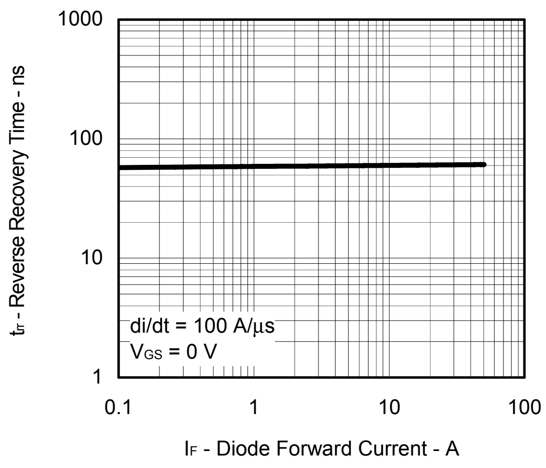
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

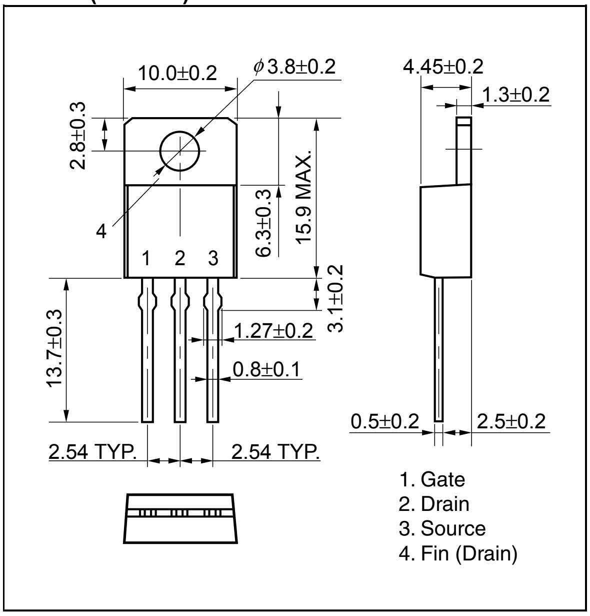


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

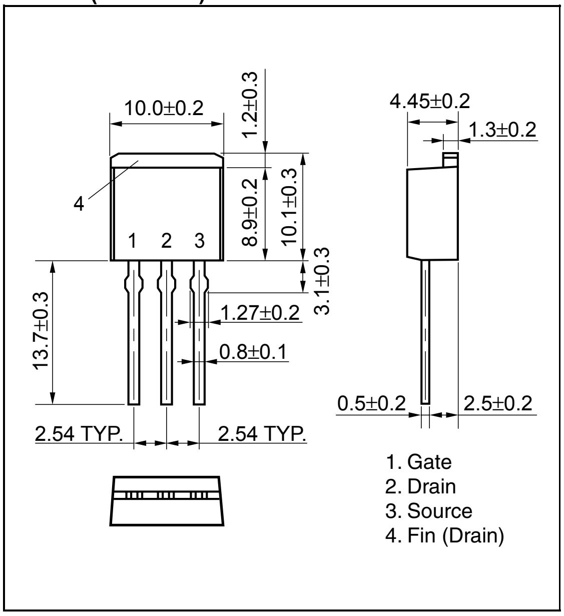


PACKAGE DRAWINGS (Unit: mm)

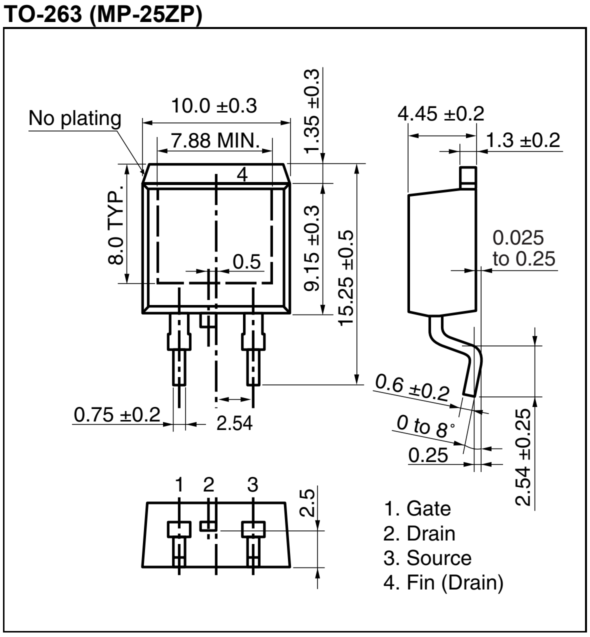
TO-220 (MP-25K)



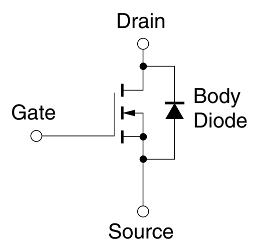
TO-262 (MP-25SK)



TO-263 (MP-25ZP)



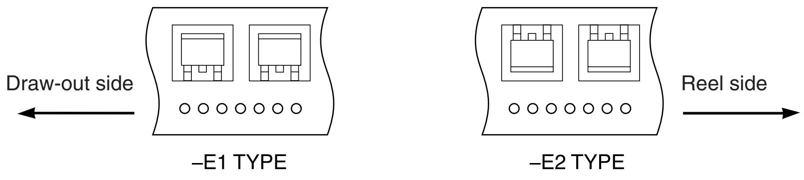
EQUIVALENT CIRCUIT



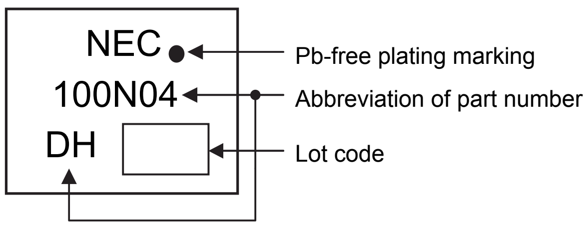
Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

TAPE INFORMATION (NP100N04PDH)

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow NP100N04PDH	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Wave soldering NP100N04MDH, NP100N04NDH	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating NP100N04MDH, NP100N04NDH, NP100N04PDH	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).