

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# DATA SHEET



## MOS FIELD EFFECT TRANSISTOR NP100N055MUH, NP100N055NUH, NP100N055PUH

### SWITCHING N-CHANNEL POWER MOS FET

#### DESCRIPTION

The NP100N055MUH, NP100N055NUH, NP100N055PUH are N-channel MOS Field Effect Transistors designed for high current switching applications.

#### ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP100N055MUH-S18-AY <sup>Note</sup>	Pure Sn (Tin)	Tube	TO-220 (MP-25K) typ. 1.9 g
NP100N055NUH-S18-AY <sup>Note</sup>		50 p/tube	TO-262 (MP-25SK) typ. 1.8 g
NP100N055PUH-E1-AY <sup>Note</sup>		Tape	TO-263 (MP-25ZP) typ. 1.5 g
NP100N055PUH-E2-AY <sup>Note</sup>		800 p/reel	

**Note** Pb-free (This product does not contain Pb in the external electrode.)

#### FEATURES

- Enhancing  $T_{ch(MAX.)}$  to 200°C (Operation time until 250 Hr)
- Super low on-state resistance
  - NP100N055MUH, NP100N055NUH  
 $R_{DS(on)} = 4.9 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 50 \text{ A)}$
  - NP100N055PUH  
 $R_{DS(on)} = 4.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 50 \text{ A)}$
- High avalanche energy, High avalanche current
- Low input capacitance  
 $C_{iss} = 7000 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$

(TO-220)



(TO-262)



(TO-263)



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**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	55	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±100	A
Drain Current (pulse) (T <sub>C</sub> = 25°C) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±400	A
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	288	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch1</sub>	175	°C
Channel Temperature <sup>Note2</sup>	T <sub>ch2</sub>	200	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current <sup>Note3</sup>	I <sub>AR1</sub>	80	A
Repetitive Avalanche Current <sup>Note4</sup>	I <sub>AR2</sub>	90	A
Repetitive Avalanche Energy <sup>Note5</sup>	E <sub>AR</sub>	1000	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Reliability test condition

High temperature bias condition (V<sub>DS</sub> = V<sub>DSS</sub>, V<sub>GS</sub> = 0 V, 250 Hr)

High temperature gate bias condition (V<sub>DS</sub> = 0 V, V<sub>GS</sub> = 20 V, 250 Hr)

**3.** L = 100 μH, T<sub>ch</sub> ≤ 200°C

**4.** L = 10 μH, T<sub>ch</sub> ≤ 200°C

**5.** T<sub>ch</sub> ≤ 200°C, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V

**THERMAL RESISTANCE**

Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	0.52	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	83.3	°C/W

<R>

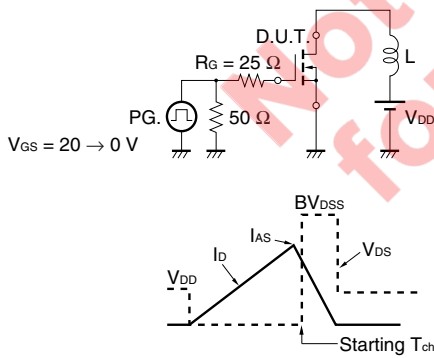
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**ELECTRICAL CHARACTERISTICS (TA = 25°C)**

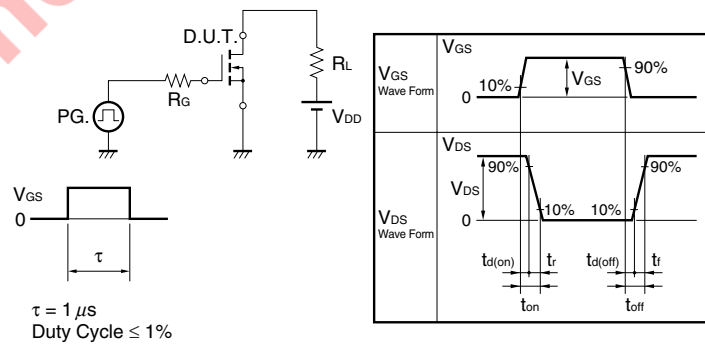
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
Forward Transfer Admittance <sup>Note</sup>	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 50\text{ A}$	30	63		S
Drain to Source On-state Resistance <sup>Note</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ NP100N055MUH, NP100N055NUH		3.9	4.9	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ NP100N055PUH		3.6	4.5	$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{DS} = 25\text{ V},$		7000	11000	pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V},$		1000	1500	pF
Reverse Transfer Capacitance	$C_{rss}$	$f = 1\text{ MHz}$		270	490	pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 28\text{ V}, I_D = 50\text{ A},$		28	62	ns
Rise Time	$t_r$	$V_{GS} = 10\text{ V},$		15	30	ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 0\ \Omega$		90	180	ns
Fall Time	$t_f$			12	30	ns
Total Gate Charge	$Q_G$	$V_{DD} = 44\text{ V},$		115	175	nC
Gate to Source Charge	$Q_{GS}$	$V_{GS} = 10\text{ V},$		34		nC
Gate to Drain Charge	$Q_{GD}$	$I_D = 100\text{ A}$		34		nC
Body Diode Forward Voltage <sup>Note</sup>	$V_{F(S-D)}$	$I_F = 100\text{ A}, V_{GS} = 0\text{ V}$		0.93	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 100\text{ A}, V_{GS} = 0\text{ V},$		60		ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100\text{ A}/\mu\text{s}$		120		nC

**Note** Pulsed

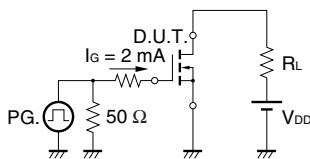
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

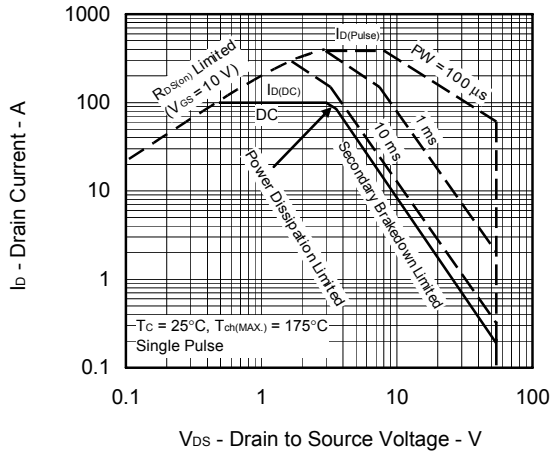


**TEST CIRCUIT 3 GATE CHARGE**

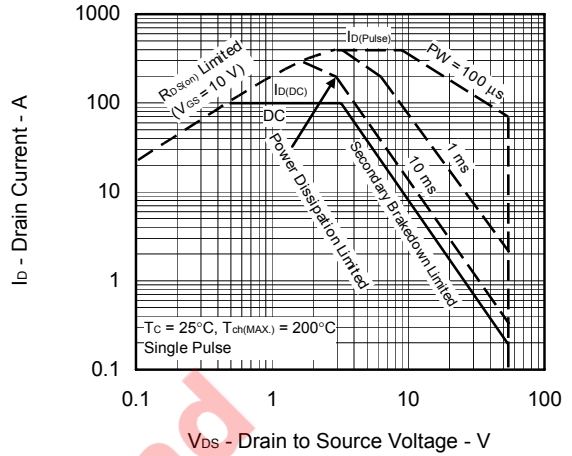


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C) (NP100N055MUH)

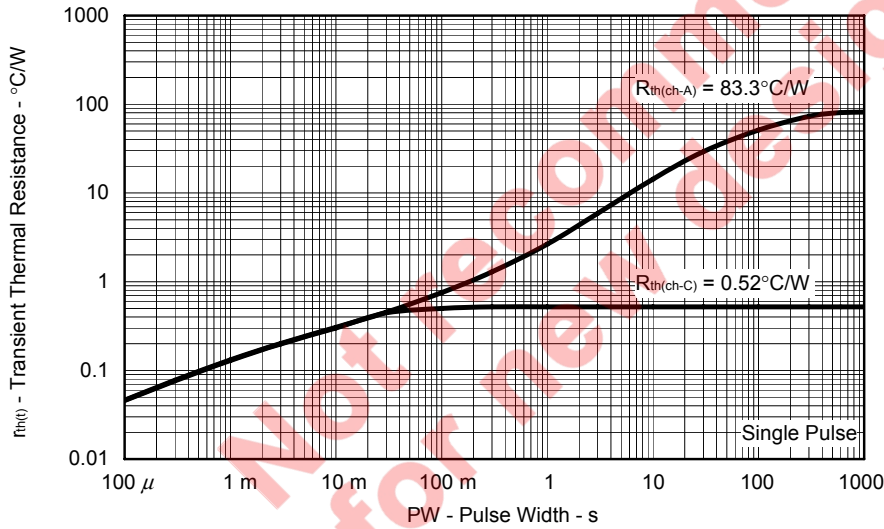
<R> FORWARD BIAS SAFE OPERATING AREA



<R> FORWARD BIAS SAFE OPERATING AREA

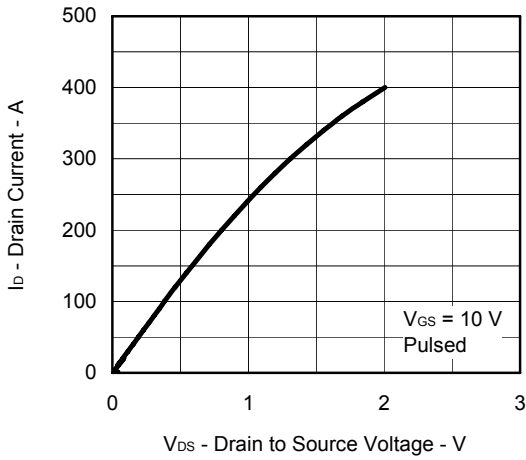


<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

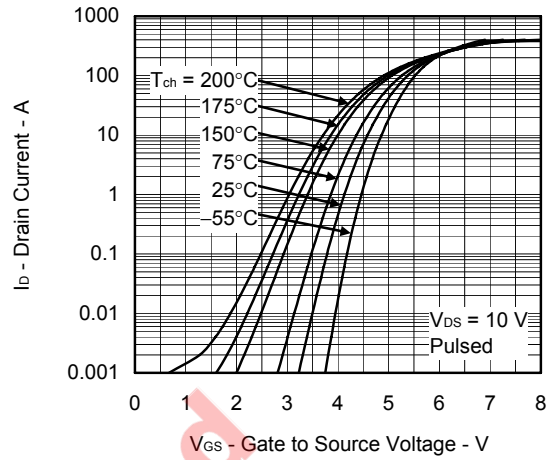


**Note** Confirm the operation tracks are in Safe Operating Area.

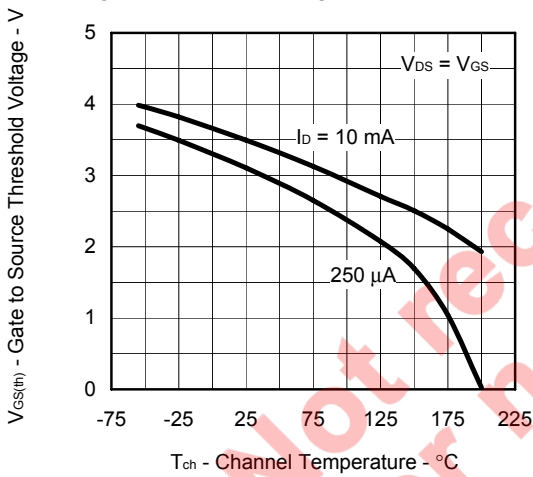
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



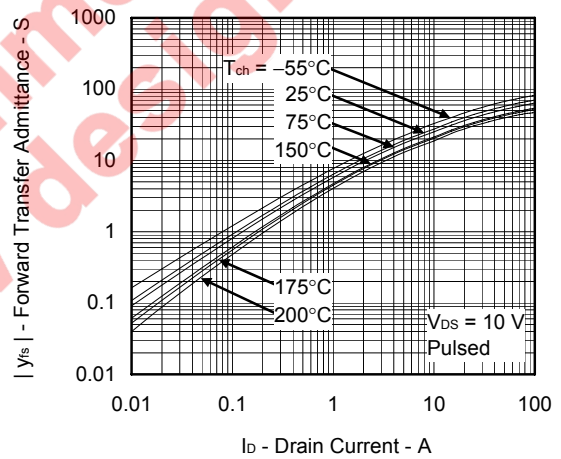
FORWARD TRANSFER CHARACTERISTICS



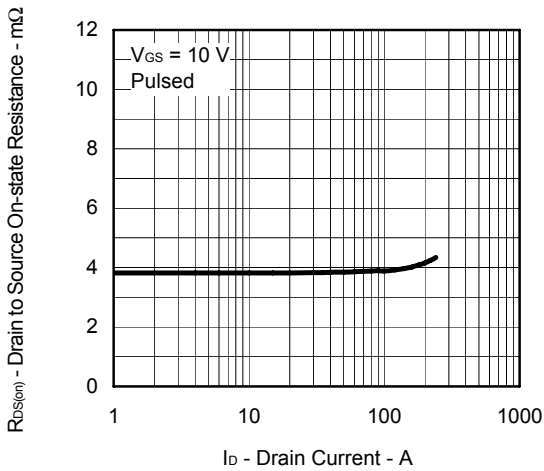
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



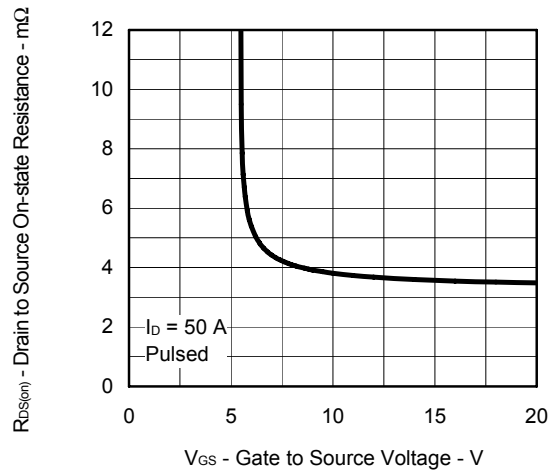
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



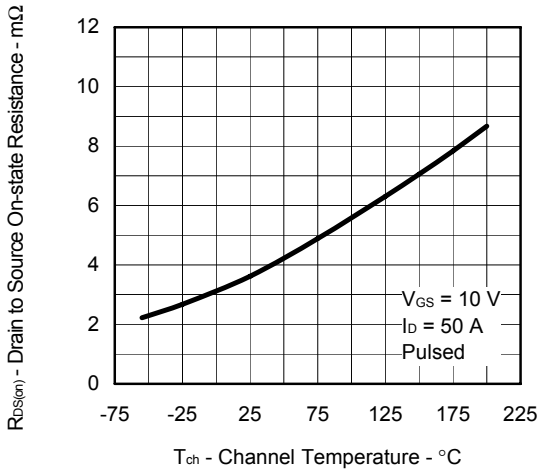
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



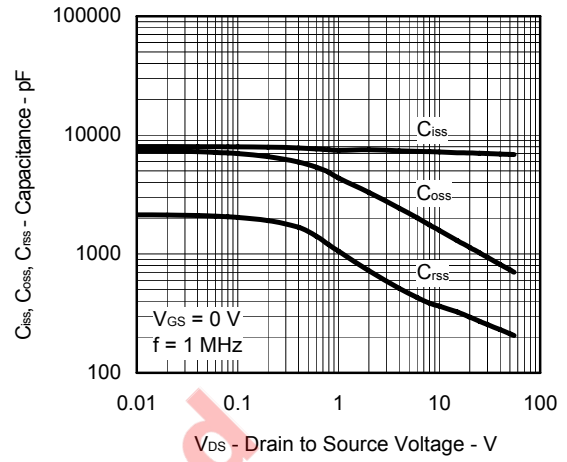
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



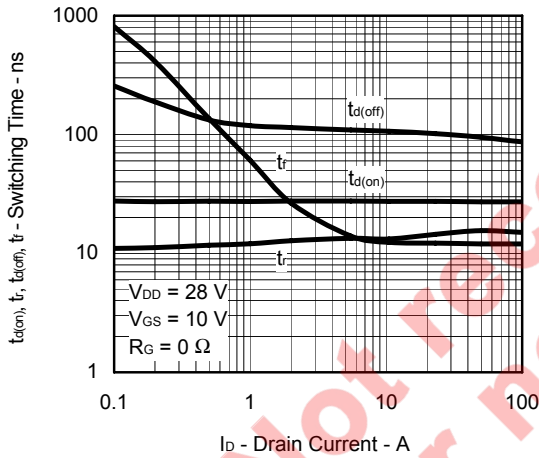
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



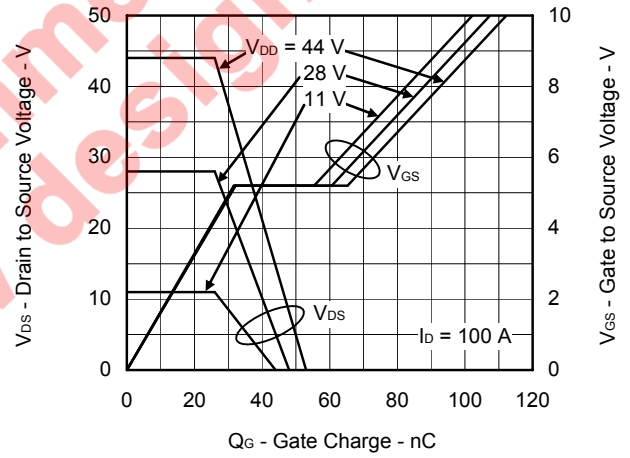
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



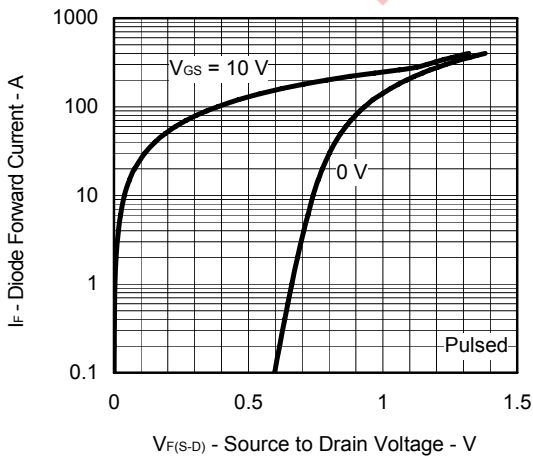
SWITCHING CHARACTERISTICS



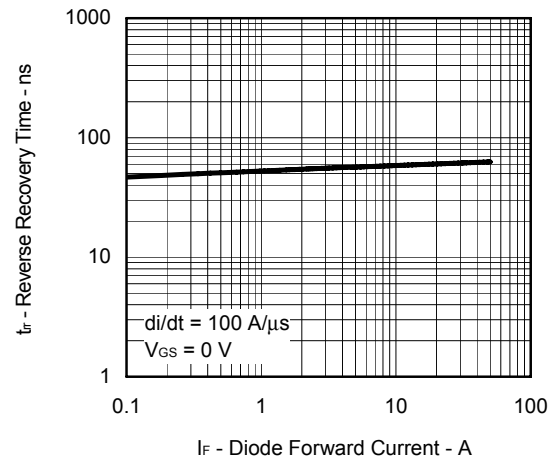
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



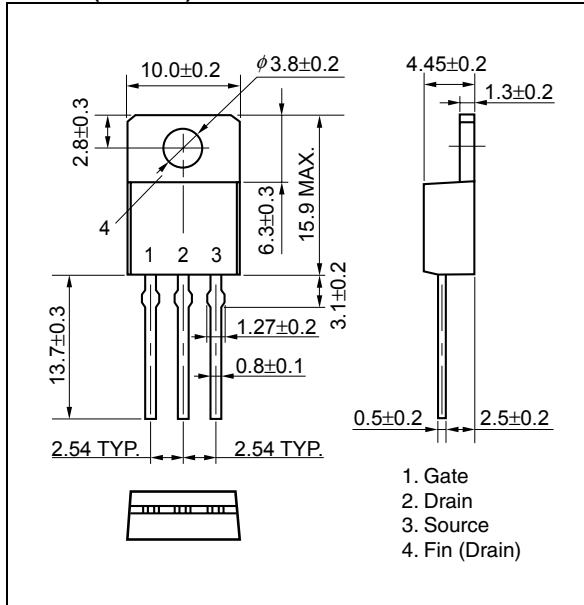
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



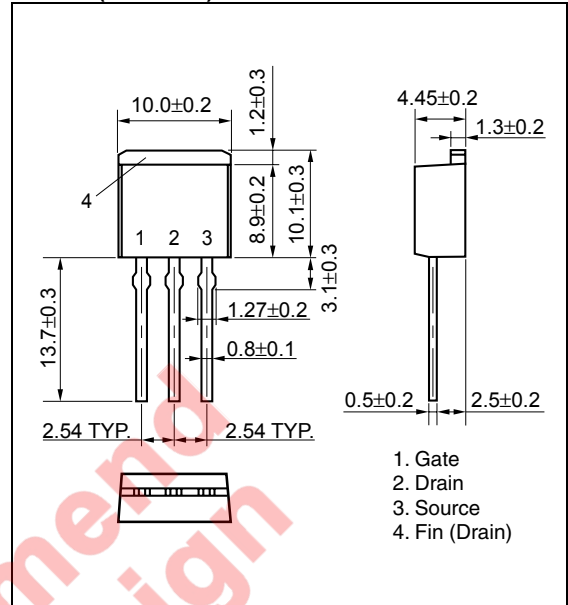


PACKAGE DRAWINGS (Unit: mm)

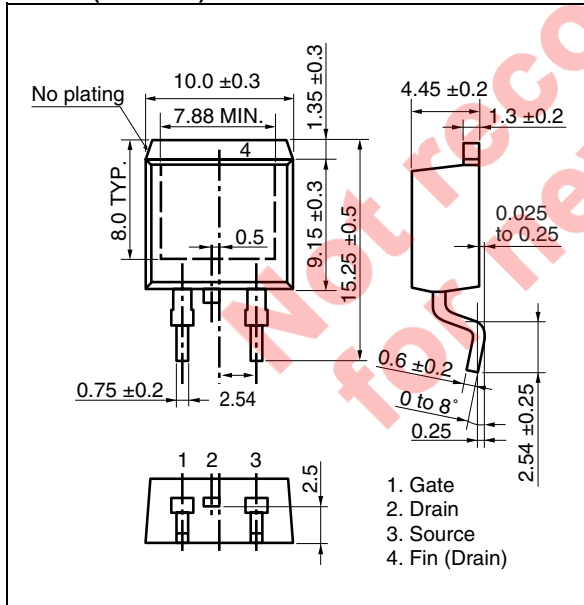
TO-220 (MP-25K)



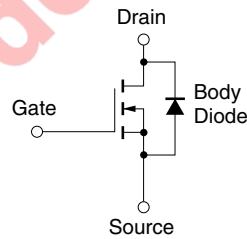
TO-262 (MP-25SK)



TO-263 (MP-25ZP)



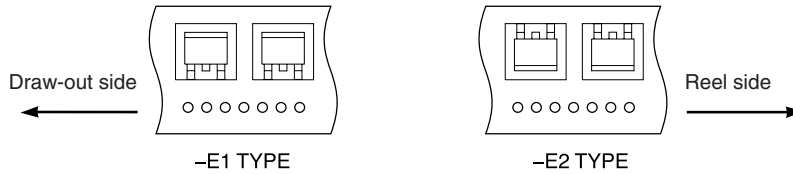
EQUIVALENT CIRCUIT



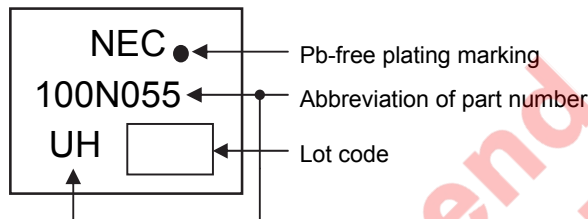
**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

**TAPE INFORMATION (NP100N055PUH)**

There are two types (-E1, -E2) of taping depending on the direction of the device.



**MARKING INFORMATION**



**RECOMMENDED SOLDERING CONDITIONS**

These products should be soldered and mounted under the following recommended conditions.

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Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow NP100N055PUH	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Wave soldering NP100N055MUH, NP100N055NUH	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating NP100N055MUH, NP100N055NUH, NP100N055PUH	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

**Caution Do not use different soldering methods together (except for partial heating).**

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