To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR
NP70N04MUG

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP70N04MUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP70N04MUG-S18-AY [Note]	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K) typ. 1.9 g

Note Pb-free (This product does not contain Pb in the external electrode).

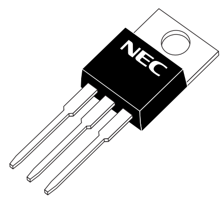
FEATURES

- Super low on-state resistance

  $R_{DS(on)}$ = 5.0 mΩ MAX. (V_{GS} = 10 V, I_D = 35 A)

- Channel temperature 175 degree rated

(TO-220)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±70	A
Drain Current (pulse) [Note1]	$I_{D(pulse)}$	±280	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	115	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current [Note2]	I_{AR}	37	A
Repetitive Avalanche Energy [Note2]	E_{AR}	137	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. T_{ch} ≤ 150°C, V_{DD} = 20 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.30	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

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Date Published April 2009 NS
Printed in Japan

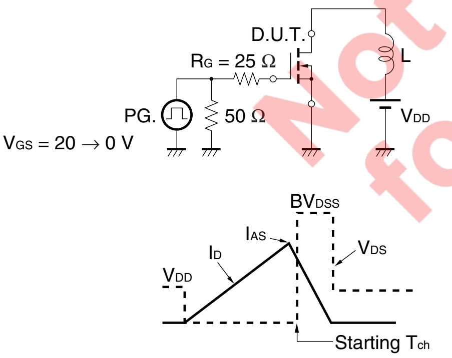
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

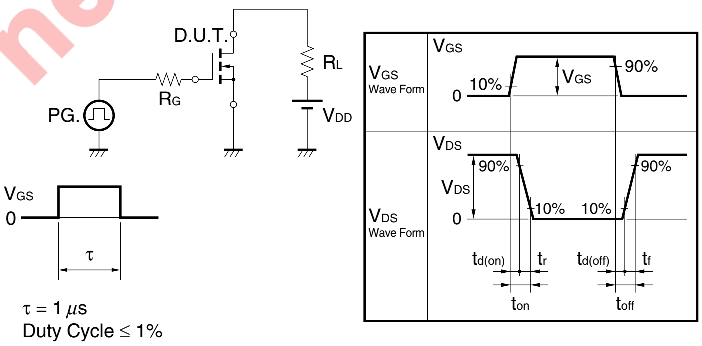
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0		4.0	V
Forward Transfer Admittance Note	$\mid y_{fs} \mid$	V_{DS} = 5 V, I_D = 35 A	25	49		S
Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 35 A		4.0	5.0	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V,		4900		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		480		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		310		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 35 A,		25		ns
Rise Time	t_r	V_{GS} = 10 V,		18		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		63		ns
Fall Time	t_f			12		ns
Total Gate Charge	Q_G	V_{DD} = 32 V,		90		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		21		nC
Gate to Drain Charge	Q_{GD}	I_D = 70 A		31		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 70 A, V_{GS} = 0 V		0.96	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 70 A, V_{GS} = 0 V,		37		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		42		nC

Note Pulsed

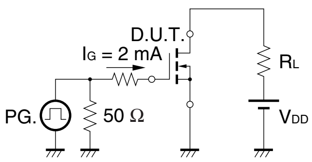
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

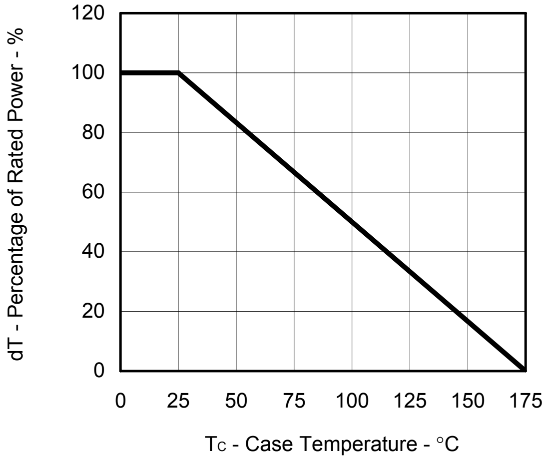


TEST CIRCUIT 3 GATE CHARGE

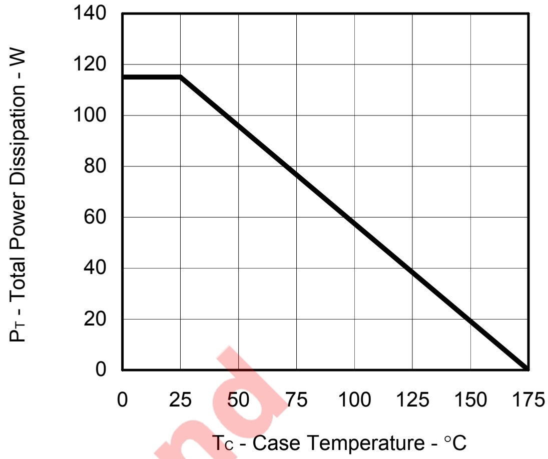


TYPICAL CHARACTERISTICS (T_A = 25°C)

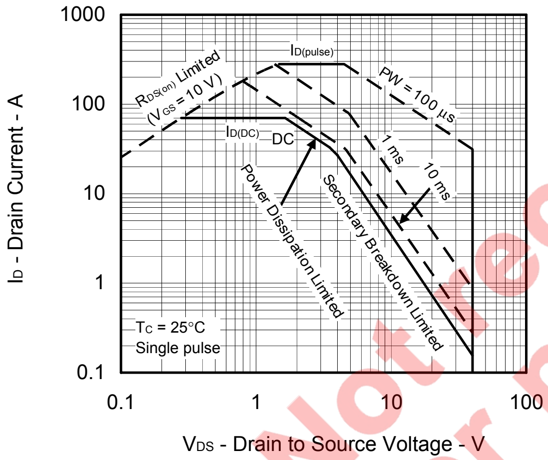
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



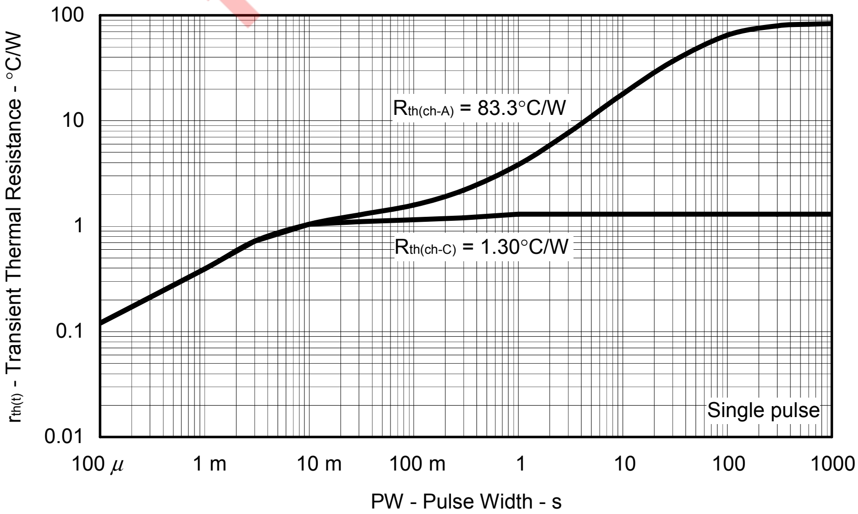
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



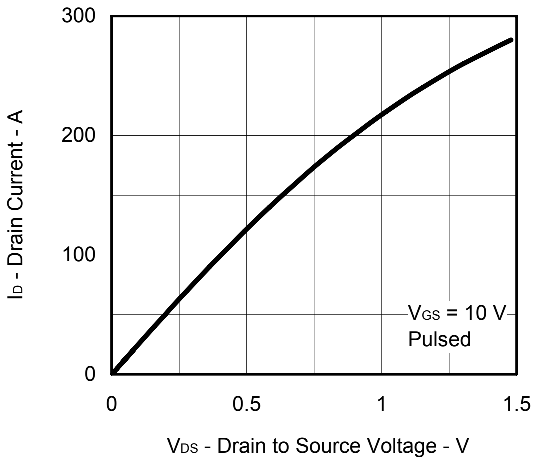
FORWARD BIAS SAFE OPERATING AREA



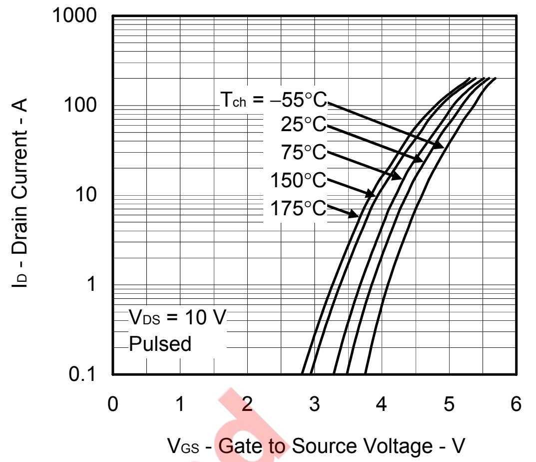
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



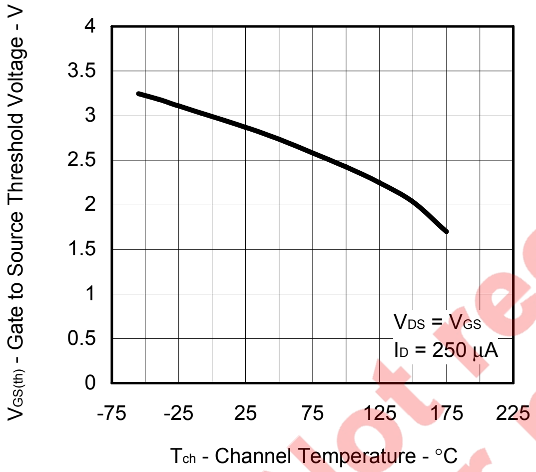
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



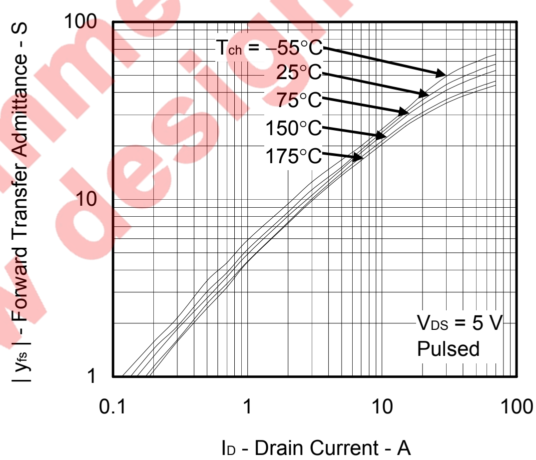
FORWARD TRANSFER CHARACTERISTICS



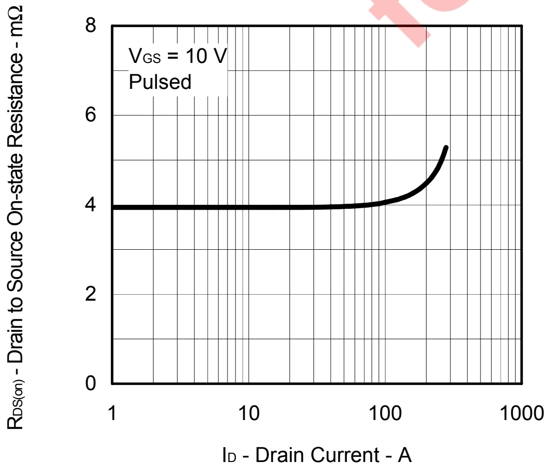
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



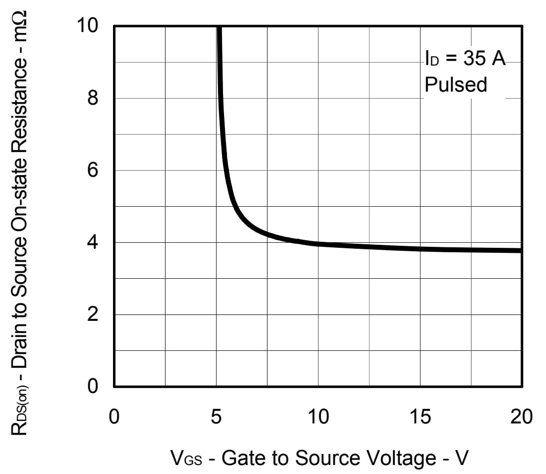
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



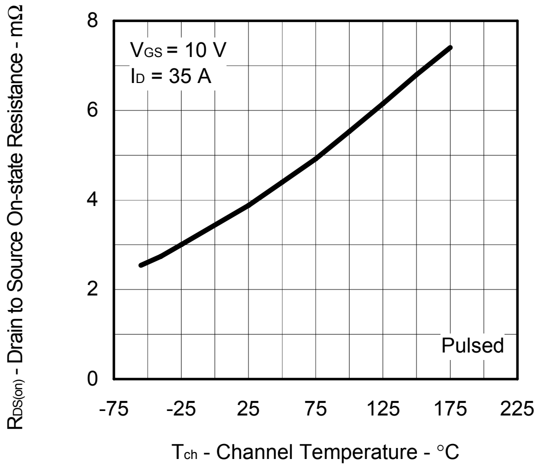
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



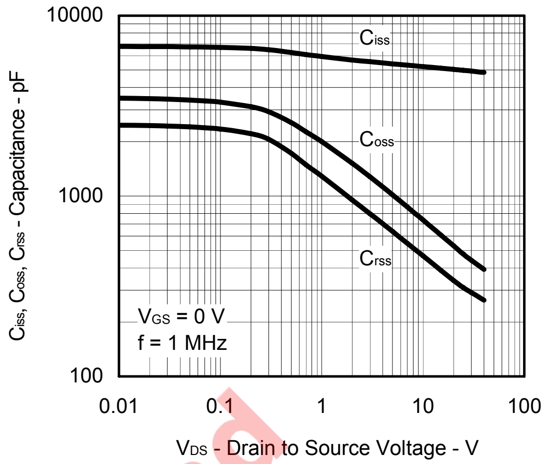
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



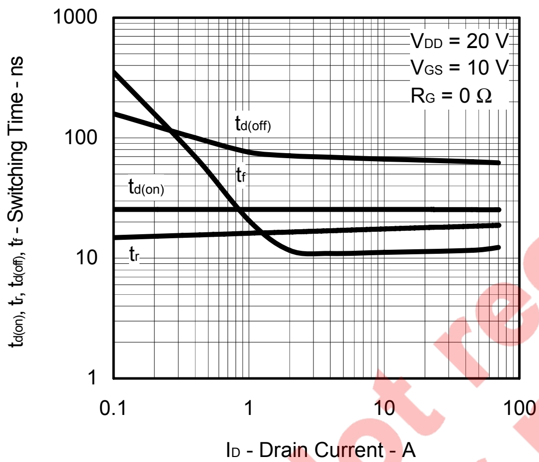
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



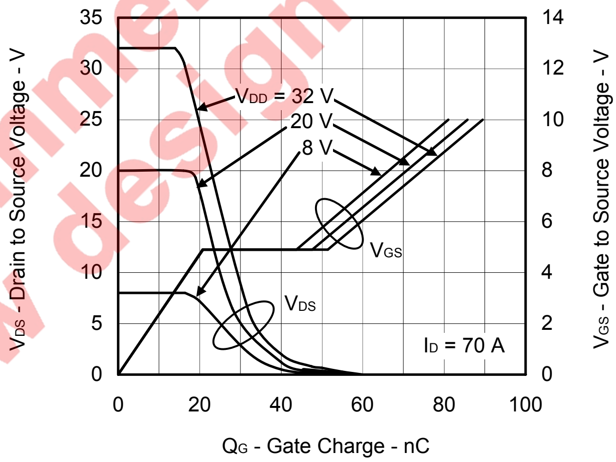
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



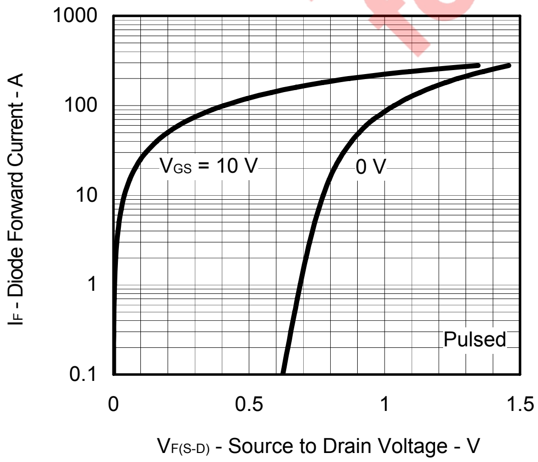
SWITCHING CHARACTERISTICS



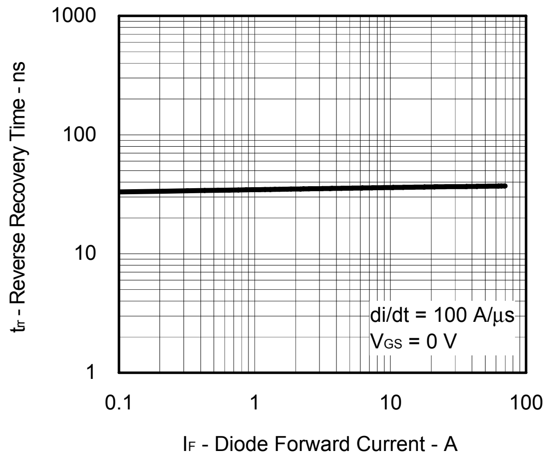
<R> DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE
FORWARD VOLTAGE

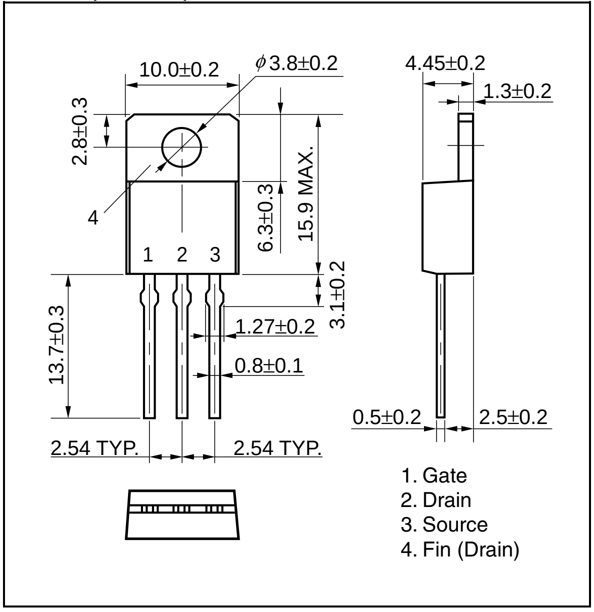


REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT

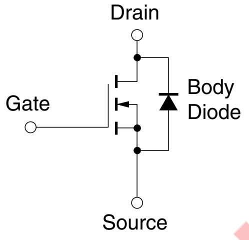


PACKAGE DRAWING (Unit: mm)

TO-220 (MP-25K)

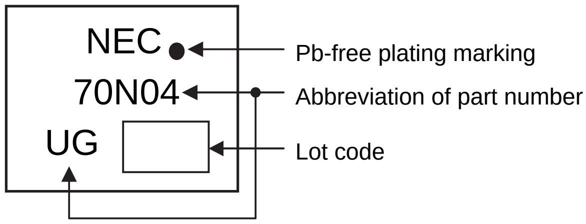


EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The NP70N04MUG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave soldering MP-25K	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating MP-25K	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

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