EMBEDDED IOT SOLUTIONS | SMART TRANSCEIVERS

PL 3120 Power Line Smart Transceiver

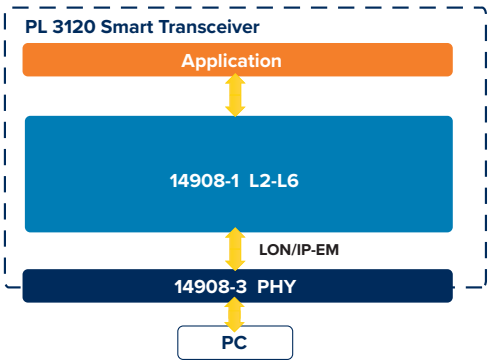


Figure 1. PL 3120 Firmware Protocol Stack

Introduction

The PL 3120 Power Line Smart Transceiver integrates a Neuron processor core with a power line transceiver, making it ideal for appliance, audio/video, lighting, heating/cooling, security, metering, and irrigation applications. A complete system-on-a-chip, the PL 3120 features a highly reliable narrow-band power line transceiver, an 8-bit Neuron processor core for running applications and managing network communications, on-board memory, and an extremely small form factor – all at a price that is compelling for even the most cost-sensitive consumer product applications.

A Global Product

Compliant with FCC, Industry Canada, Japan MPT, and European CENELEC EN50065-1 regulations, the PL 3120 Power Line Smart Transceiver can be used in applications worldwide.

The PL 3120 implements the CENELEC access protocol, which can be enabled or disabled by the user. This eliminates the need for users to develop the complex timing and access algorithms mandated under CENELEC EN50065-1.

Unmatched Performance

Intermittent noise sources, impedance changes, and attenuation make the power line a hostile signaling environment. The PL 3120 Power Line Smart Transceiver incorporates a variety of technical innovations to insure reliable operation:

- Unique dual carrier frequency feature automatically selects an alternate secondary communication frequency should the primary frequency be blocked by noise;

Features

- Combines an ISO/IEC 14908-3 ANSI-709.2-compliant power line transceiver with an ISO/IEC 14908-1 Neuron 3120 processor core
- Designed to comply with FCC, Industry Canada, Japan MPT, and European CENELEC EN 50065-1 power line communications regulations
- Supports CENELEC A-band and C-band operation
- Dual carrier frequency mode and digital signal processing
- 4K bytes of embedded EEPROM for application code and configuration data
- 2K bytes of embedded RAM for buffering network data and network variables
- Full duplex hardware UART and SPI serial interfaces
- 12 I/O pins with 38 programmable standard I/O modes to minimize external interface circuitry
- -40°C to +85°C operating temperature range
- RoHS-compliant

- Highly efficient, patented, low-overhead forward error correction (FEC) algorithm to overcome errors induced by noise;
- Sophisticated digital signal processing, noise cancellation, and distortion correction algorithms. These features correct for a wide variety of signaling impediments, including impulsive noise, continuous tone noise, and phase distortion;
- High output, low distortion external amplifier design that can deliver 1Ap-p into low impedance loads, eliminating the need for expensive phase couplers in typical residential applications.

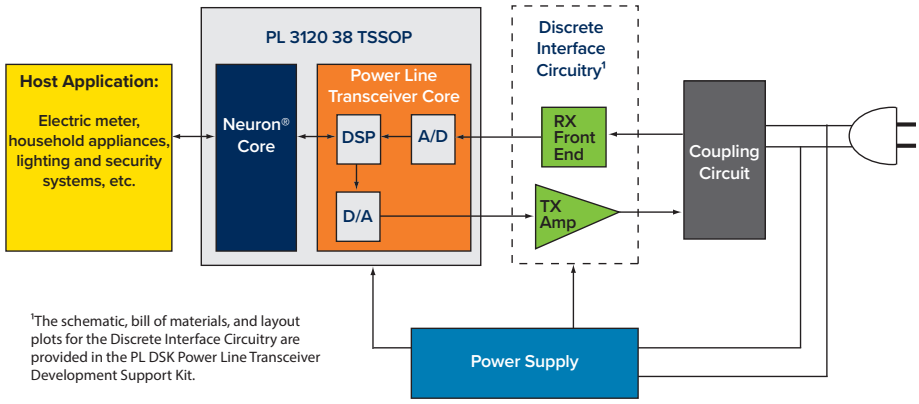


Figure 2. PL 3120 Power Line Transceiver Block Diagram

The combination of these special features enable the PL 3120 to operate reliably in the presence of consumer electronics, power line intercoms, motor noise, electronic ballasts, dimmers, and other typical sources of interference. The PL 3120 can communicate over virtually any AC or DC power mains, as well as unpowered twisted pair, by way of a low-cost, external coupling circuit.

The PL 3120 is targeted at very low cost designs that require up to 4K bytes of application code, and an ultra-compact 38 TSSOP package. The chip includes 4K bytes of EEPROM and 2K bytes of RAM. The Neuron system firmware and software application libraries are contained in on-chip ROM.

The PL 3120 operates at either 6.5536MHz or 10.0MHz. The 6.5536MHz clock frequency enables the transceiver to communicate in the CENELEC A-band, which is used for metering and utility applications. The 10MHz clock frequency supports the CENELEC C-band, which is used for general purpose signaling and all non-utility related applications.

Application programs stored in the embedded EEPROM may be updated over the power line network. This valuable feature enables products to be updated without physically accessing them, i.e., from a local PC with a power line interface or from a remote service center through a SmartServer IoT Edge Server. The embedded EEPROM may be written up to 10,000 times with no data loss. Data stored in the EEPROM will be retained for at least ten years.

Inexpensive Power Supply

The PL 3120 uses +8.5 to +18VDC and +5VDC power supplies and supports very low receive mode current consumption. The wide power supply range and very low receive power requirements allow the use of inexpensive power supplies.

Additionally, the transceiver incorporates a power management feature that constantly monitors the status of the device's power supply. If during transmission the power supply voltage falls to a level that is insufficient to ensure reliable signaling, the transceiver stops transmitting until the power supply voltage rises to an acceptable level. This unique feature allows the use of a power supply with one-third the current capacity otherwise required. The net result is a reduction in the size, cost, and thermal dissipation of the power supply. Power management is especially useful for high volume, low-cost consumer products such as electrical switches, motion detectors, outlets, light sensors, and dim.

Flexible I/O, Simple Configuration

The PL 3120 provides 12 I/O pins which can be configured to operate in one or more of 38 predefined standard input/output modes. Combining a wide range of I/O models with two on-board timer/counters enables the PL 3120 to interface with application circuits using minimal external logic or software development. The transceiver also features a full duplex hardware UART supporting baud rates of up to 115kbps, and an SPI interface that operates up to 625kbps.

External Components

Only a small number of inexpensive external components are required to create a complete PL 3120-based device (see the PL 3120 Power Line Smart Transceiver Block Diagram). These components include:

- Discrete interface circuitry comprised of roughly 50 components, primarily resistors and capacitors. This circuitry provides “front-end” filtering for the on-chip A/D, and implements the power amplifier that drives the on-chip D/A transmit signal onto the power line. Adesto offers a comprehensive Power Line Development Support Kit* (DSK) with which customers can implement this interface circuitry. Contact your salesperson for details about purchasing a PL DSK.
- Coupling circuit consisting of approximately ten components, mainly capacitors and inductors, which acts as a simple high-pass filter located between the PL 3120 and the power mains. This circuitry provides surge and line transient protection in addition to blocking the low frequency, 50Hz/60Hz AC mains signal. Detailed schematics are provided in the PL 3120 / PL 3150 Power Line Smart Transceiver Data Book.
- The RoHS compliant Revision B PL 3120 eliminates the need for an external inverter, thereby reducing the cost of external components. Circuits without an external inverter can only be used with Revision B parts (15311R-1000 PL 3120 Power Line Smart Transceiver).

PRODUCT SPECIFICATIONS

Function	Description
Emissions compliance	Designed to be compliant with FCC, Industry Canada, Japan MPT, and CENELEC EN50065 specification for low-voltage signaling
Bit rate	5.4kbps raw bit rate in CENELEC C-band and 3.6kbps in CENELEC A-band
Communication technique	Dual Frequency BPSK with DSP-enhanced receiver
Data Integrity	Forward error correction of up to 2 bit errors per packet; 18 bit packet CRC
Carrier frequencies	132kHz (primary) and 115kHz (secondary) in CENELEC C-band and 86kHz (primary) and 75kHz (secondary) in CENELEC A-band
RoHS Compliance	Compliant with European Directive2002/95/EC on Restriction of Hazardous Substances (RoHS) in electrical and electronic equipment

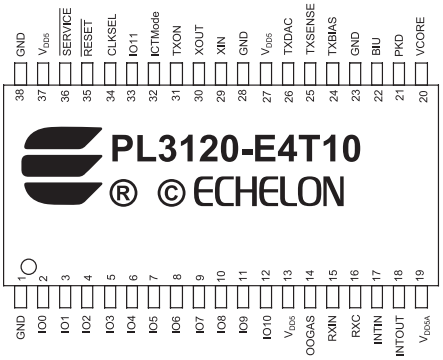


Figure 3. PL 3120 Power Line Smart Transceiver Pinout

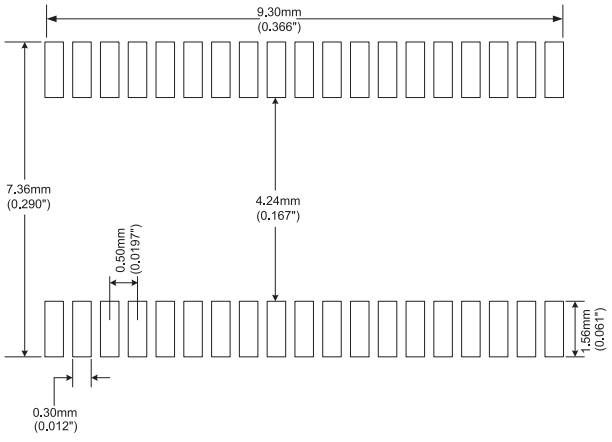


Figure 4. Recommended Footprint

Power Line Smart Transceiver Pin Descriptions

Name	Pin Number	Type	Pin Functions
XIN	29	Input	Oscillator connection or external clock input
XOUT	30	Output	Oscillator connection
RESET	35	Digital I/O (Built-in Pull-up)	Reset pin (active LOW) Note: The maximum external capacitance is 1000pF
SERVICE	36	Digital I/O (Built-in Configurable Pull-up)	Service Pin (active LOW)
CLKSEL	34	Digital Input	Tie to V_{DD5}
IO0-IO3	2, 3, 4 ,5	Digital I/O	Large current-sink capacity (20mA); General purpose I/O; The output of timer/counter 1 may be routed to IO0; The output of timer/counter 2 may be routed to IO1
IO4-107, IO11	6, 7, 8, 9, 33	Digital I/O	General purpose I/O; The input of timer/counter 1 may be one of IO4-IO7; The input of timer/counter 2 is IO4
IO8	10	Digital I/O	General purpose I/O; UART RX; SPI slave clock input; SPI master clock input
IO9	11	Digital I/O	General purpose I/O; SPI slave data output; SPI master data input
IO10	12	Digital I/O	General purpose I/O; SPI slave data input; SPI master data output
V_{DD5}	13, 27, 37	Power	Power input (5V nom); All V_{DD5} pins must be connected together externally
V_{DD5A}	19	Power	Power input (5V nom); Supplies on-chip analog circuitry
GND	1, 23, 28, 38	Power	Power input (0V, GND); All GND pins must be connected together externally
ICTMode	32	Digital Input	In-circuit test mode control; Driving ICTMode high and RESET low will place all outputs in high impedance mode for in-circuit test. Tie to GND for normal operation.
PKD	21	Digital Output	Packet Detect LED driver
BIU	22	Digital Output	Band in Use LED driver
RXIN	15	Analog Input	Receiver input
INTIN, INTOUT	17, 18	Analog I/O	Integrator input and output
RXC	16	Analog Input	Receive signal
OOGAS	14	Analog Input	Comparator to detect when energy storage power supply lacks sufficient energy to transmit a packet; Tie to VCORE if not used
VCORE	20	Power	Output of internal 1.8V regulator. Requires 0.1µF external capacitator
TXON	31	Digital Output	High when transmitting; Used to drive LED to show packet transmission
TXDAC	26	Analog Output	Transmit waveform DAC output
TXSENSE	25	Analog Input	Transmit amplifier sense feedback
TXBIAS	24	Analog Output	Transmit amplifier bias generator

Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
V_{DD5}	V_{DD5} Supply Voltage	4.75	5.00	5.25	V
V_{DD5A}	V_{DD5} Supply Voltage	4.60	5.00	5.25	V
T_A	Ambient Temperature	-40	25	85	°C
$F_{A\text{-band}}$	XIN Frequency for A-band Operation (6.5536MHz±200ppm)	6.55232	6.5536	6.5549	MHz
$F_{C\text{-band}}$	XIN Frequency for C-band Operation (10.0000MHz±200ppm)	9.9980	10.0000	10.0020	MHZ

Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	Min	Typ.	Max	Unit
V_{IL}	Digital Input Low-level Voltage			0.8	V
V_{IH}	Digital Input High-level Voltage	2.0			V
V_{OL}	Digital Output Low-level Voltage I_{out}<20µA IO4-IO11, A0-A14, D0-D7, R/W, E (I_{OL} = 1.4mA) IO0-IO3, SERVICE, RESET (I_{OL}= 20mA) IO0-IO3, SERVICE, RESET (I_{OL}= 10mA) PKD, BIU, TXON (I_{OL}= 12mA)			 0.1 0.4 0.8 0.4 0.5	V
V_{OH}	Digital Output High-level Voltage I_{out}<20µA IO4-IO11, A0-A14, D0-D7, R/W, E (I_{OH} = -1.4mA) IO0-IO3, SERVICE, RESET (I_{OH} = -1.4mA) PKD, BIU, TXON (I_{OH}= -12mA)	 V_{DD5} -0.1 V_{DD5}-0.5 V_{DD5}-0.4 V_{DD5}-0.5			V
V_{hys}	Digital Input Hysteresis	175			mV
I_{in}	Input Current (Excluding Pull-ups)[1]	-10		10	µA
I_{pu}	Pull-up Source Current (V_{out}=0, Output=High-Z)[1]	30		300	µA
I_{DD}	V_{DD5} + V_{DD5A} Supply Current (not including I/O or internal pull-up current)		9	13	mA
V_{LV1}	V_{DD5} LV1 Trip Point	4.0		4.45	V

Notes:
1. IO4-IO7 and SERVICE pins have configurable pull ups; The RESET pin has a permanent pull-up

Recommended Operating Conditions for Power Line Smart Transceiver Discrete Interface Circuitry*

Symbol	Parameter	Min	Typ.	Max	Unit
V_{ARX}	V_A Supply Voltage - Receive Mode [2]	8.5	12.0	18.0	V
V_{ATX}	V_S Supply Voltage - Transmit Mode [2]	10.8	12.0	18.0	V
T_A	Ambient Temperature	-40	25	85	°C

Notes:
2. Minimum value can be 8.5V under certain conditions (refer to Data Book for details).
Maximum value must also satisfy the following: VATXAVE < (150-TAMAX)/(8*DMAX);
Where: VATXAVE = Average VA supply voltage while transmitting
TAMAX = Maximum ambient temperature (°C)
DMAX = Maximum transmit duty cycle of the device (expressed as decimal number)

Electrical Characteristics of Power Line Smart Transceiver Discrete Interface Circuitry* (over recommended operating conditions)

Symbol	Parameter	Min	Typ.	Max	Unit
I_{ARX}	V_A Supply Current - Receive Mode		350	500	µA
I_{ATX}	V_S Supply Current - Transmit Mode		120	250	mA
V_{OTX}	Transmit Output Voltage		7		Vp-p
I_{TXLIM}	Transmit Output Current Limit		1.0		Ap-p
Z_{INRX}	Input Impedance - Receive Mode (with recommended RXCOMP inductor)		500		Ω
Z_{OTX}	Output Impedance - Transmit Mode		0.9		Ω
V_{PMU}	Power Management - Upper V_A Threshold	11.2	12.1	13.0	V
V_{PML}	Power Management - Lower V_A Threshold	7.3	7.9	8.6	V

*NOTE: The schematic, bill of materials, and layout plots for the Discrete Interface Circuitry are provided in the PL DSK Power Line Smart Transceiver Development Support Kit.

SPECIFICATIONS AND ORDERING

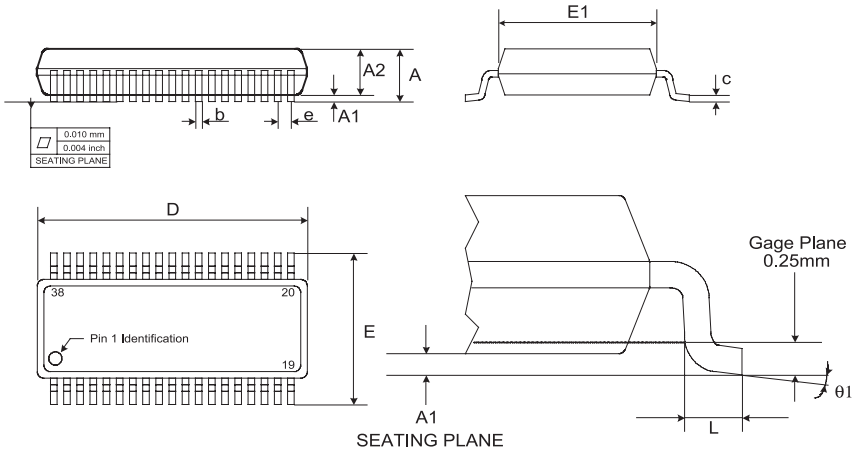
Absolute Maximum Ratings

Stresses beyond these values may cause eermanent damage to the device; functional operation under these conditions is not implied

Ambient operating temperature	-40° to +85°C
Storage temperature	-55° to +125°C
Voltage on V_{DD5} and V_{DD5A} pins with respect to GND	-0.3 to 6.0V
Voltage on each pin with respect to GND[3]	-0.3 to (V_{DD5} + 0.3V)
Voltage on TXBIAS, TXSENSE, OOGAS pins	-0.3 to 1.89V
Maximum voltage on VCORE pin with respect to GND	1.89V
V_{DD5}, V_{DD5A}, or GND current per pin	±50mA
Input clamp current, I_{IK} (V_1<0 or V_1>V_{DD5})[3]	±10mA
Output clamp current, I_{OK} (V_1<0 or V_1>V_{DD5})[3]	±10mA
Output current per pin[3]	±25mA
Power dissipation	250MW
Reflow soldering temperature profile	Refer to Joint Industry Standard document *IPC/JEDED J-STD-020C* (July 2004)
Reflow soldering temperature	235°C

Notes:
3. Applies to all pins except VDD5, VDD5A, VCORE, TXBIAS, TXSENSE and OOGAS

DIMENSIONS



	mm (prevailing dimensions)			inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	1.00	1.05	.0.31	0.039	0.041
b	0.17	-	0.27	0.0067	-	0.011
c	0.09	-	0.20	0.0035	-	0.0079
D	9.60	9.70	9.80	0.378	0.381	0.385
E	6.40 BSC			0.252 BSC		
e	0.50 BSC			0.0197 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
L	0.45	0.60	0.75	0.0711	0.023	0.030
01	0°	-	8°	0°	-	8°

Figure 5. PL 3120 Power Line Smart Transceiver Package Diagram

Model #	Product Name	Product Description
15310R-1000	PL 3120 Smart Transceiver	Tubes of 100, total quantity 1000

003-0378-01H rev 12/2019

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