PTX100R

NFC Reader IC

Product Description

The PTX100R is a highly integrated NFC reader IC for contactless communication with increased key performance parameters such as output power (transmitter current up to 650mA) and RX sensitivity (-80dBc [1]). While eliminating EMC filter and matching components, the PTX100R enables simple integration and compact design without the complexity associated with existing solutions (dual resonating circuits composed by EMC filter and antenna).

Due to its modular Soft Controller architecture, the NFC functionalities are integrated into a split stack solution where time-critical operations are running on the on-chip HW accelerator, and the rest of the NFC logic is in the host controller to carry out applications such as POS and IOT readers.

Features

The architecture enables:

- Efficient power transmission with accurate digital programmability of RF carrier and modulation shape
- EMC filter removal due to sinewave output driver and Direct Antenna Connection (DiRAC)
- -80dBc RX sensitivity with full dynamic range due to DiRAC
- SDK composed of FW and SW integrated in a Split Stack architecture with PTX100R firmware update capability over the host processor:
  - Modular SW stack running on the Host architecture
  - Integrated FW running on the on-chip MCU for time-critical operations
- Fractional-N PLL to support any reference input clock frequency from 13.15MHz to 52MHz
- EMVCo® 3.0/3.1 PCD L1 compliancy[2]
- ISO/IEC14443-A reader/writer mode up to 848kBit/s
- ISO/IEC14443-B reader/writer mode up to 848kBit/s
- NFC Forum Reader/Writer mode
- Supports reading/writing of NFC Tag Type 2, 3, 4A/4B and 5
- FeliCa™ reader/writer mode 212&424kBit/s
- ISO/IEC 15693 reader/writer mode
- Support reading/writing of Mifare® card family including Mifare Classic® (without crypto)[3]
- Support Apple ECP “Enhanced Contactless Polling” (feature only available for customers with valid Apple MFi license)
- Transparent mode allowing implementation of customer protocols based on low-level commands
- NFC Forum P2P Passive Initiator
- NFC Card Emulation Mode for Tag Type 4A (106kBit/s)
- Low Power Card Detection (LPCD)
- Low Power Field Detection (LPFD)
- Programmable GPIOs
- Supported host interfaces: I2C, SPI, UART

PTX100R reader IC enables key improvements in customer care-about such as:

RF performance: Patented groundbreaking architecture enables efficient power transmission and -80dBc RX sensitivity, state of the art reader performance even in challenging and complex integration environments.

Interoperability:

- Digitized architecture enables accurate shape control of the modulated signal.
- Elimination of the EMC filter results in well-behaved signal shape avoiding overshoot and

[1] Receiver input dynamic range and sensitivity are defined in Table 5.

[2] Depending on the Software Stack, EMVCo® L1 or full NFC Forum Reader functionality is supported by PTX100R.

[3] MIFARE is a registered trademark of NXP B.V

undershoot (especially important for compliance with EMVCo® 3.0/3.1)
- DiRAC allows high output power and high input sensitivity which translates to substantially larger operating volume.

Manufacturability:
- No need for bulky and performance-limiting external components of the EMC filter (no tolerances issue introduced) minimizing the performance variation between final devices.
- Reduced number of matching components allow lower antenna matching impedance, resulting in higher output power.
- Accurate adjustment of transmitter and receiver parameters due to digital architecture enabling tighter production control giving more margin for new use cases.

PTX100R is optimized for applications such as Point-Of-Sales (POS), Mobile POS, Access Control, Wearables, etc.

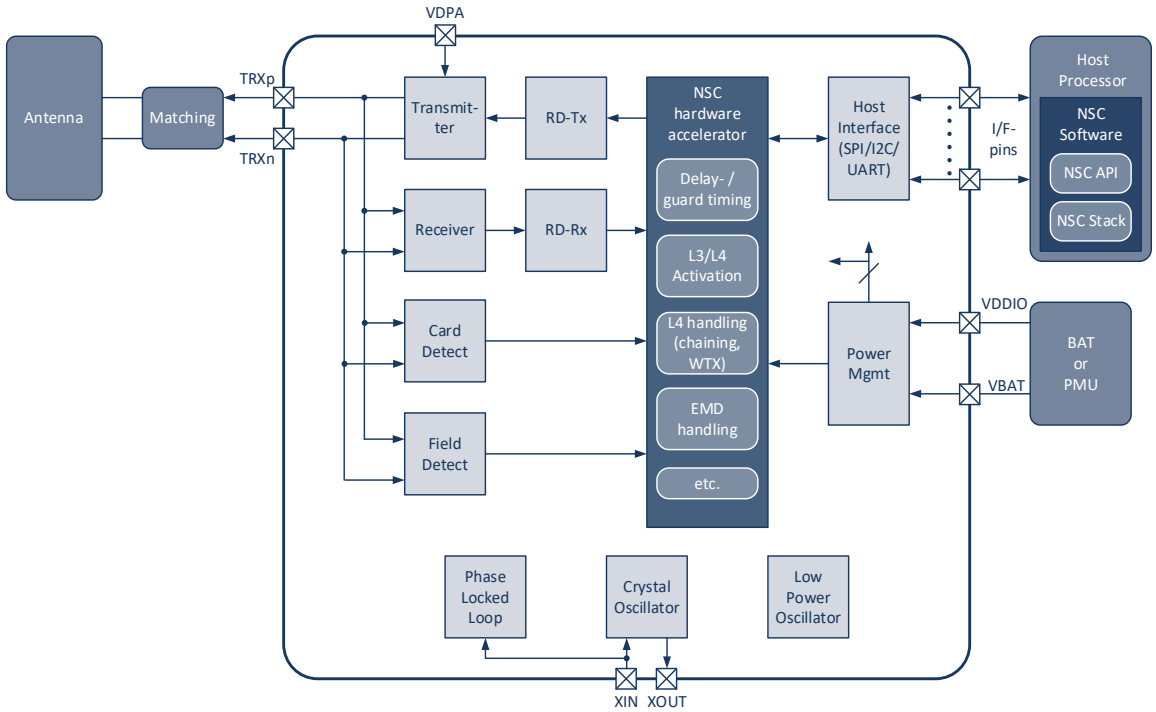

Figure 1: Block Diagram

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1.1 Pin Diagram

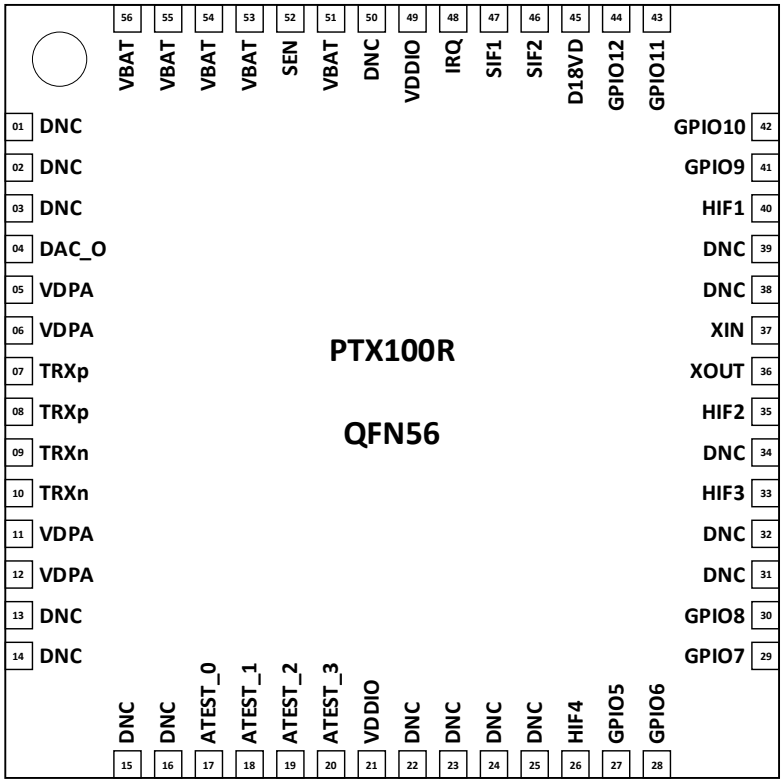


Figure 2: Pin Diagram

1.2 Pin Description

Signal Name	Signal Type	QFN56 Pin	Description
DNC	-	1	Do not connect
DNC	-	2	Do not connect
DNC	-	3	Do not connect
DAC_O	Analog out	4	AUX-DAC voltage output
VDPA	Supply	5	TX-PA supply
VDPA	Supply	6	TX-PA supply
TRXp	Analog inout	7	Transmitter/Receiver pin p
TRXp	Analog inout	8	Transmitter/Receiver pin p
TRXn	Analog inout	9	Transmitter/Receiver pin n
TRXn	Analog inout	10	Transmitter/Receiver pin n
VDPA	Supply	11	TX-PA supply
VDPA	Supply	12	TX-PA supply
DNC	-	13	Do not connect
DNC	-	14	Do not connect
DNC	-	15	Do not connect
DNC	-	16	Do not connect
ATEST_0	Analog out	17	Analog test mux
ATEST_1	Analog out	18	Analog test mux
ATEST_2	Analog out	19	Analog test mux
ATEST_3	Analog out	20	Analog test mux

Signal Name	Signal Type	QFN56 Pin	Description
VDDIO	Supply	21	IO Pad supply
DNC	-	22	Do not connect
DNC	-	23	Do not connect
DNC	-	24	Do not connect
DNC	-	25	Do not connect
HIF4	Digital inout	26	SPI: MISO, I2C: SCL, UART: TXD
GPIO5	Digital inout	27	General purpose digital IO pin
GPIO6	Digital inout	28	General purpose digital IO pin
GPIO7	Digital inout	29	General purpose digital IO pin
GPIO8	Digital inout	30	General purpose digital IO pin
DNC	-	31	Do not connect
DNC	-	32	Do not connect
HIF3	Digital inout	33	SPI: MOSI, I2C: SDA, UART: RXD
DNC	-	34	Do not connect
HIF2	Digital inout	35	SPI: SCK, I2C: ADDR1, UART: RTS
XOUT	Analog out	36	Xtal oscillator output
XIN	Analog in	37	Xtal oscillator input / Reference clock input
DNC	-	38	Do not connect
DNC	-	39	Do not connect
HIF1	Digital inout	40	SPI: NSS, I2C: ADDR0, UART: CTS
GPIO9	Digital inout	41	General purpose digital IO pin
GPIO10	Digital inout	42	General purpose digital IO pin
GPIO11	Digital inout	43	General purpose digital IO pin
GPIO12	Digital inout	44	General purpose digital IO pin
D18VD	Supply	45	Decoupling of core supply
SIF2	Digital in	46	Select interface type bit 2
SIF1	Digital in	47	Select interface type bit 1
IRQ	Digital out	48	Interrupt request to host
VDDIO	Supply	49	IO Pad supply
DNC	-	50	Do not connect
VBAT	Supply	51	Battery supply
SEN	Analog in	52	System enable input
VBAT	Supply	53	Battery supply
VBAT	Supply	54	Battery supply
VBAT	Supply	55	Battery supply
VBAT	Supply	56	Battery supply
GND	Supply	-	The exposed pad at the back of QFN is used as GND Requires good thermal connection to ensure low thermal resistance for power dissipation

Table 1: Pin Description

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
V_{BAT}	Supply voltage at VBAT pin		-0.5		5.5	V	
V_{VDPA}	Supply voltage at VDPA pin		-0.5		5.5	V	
T_J	Junction temperature		-40		125	°C	
T_S	Storage temperature		-40		150	°C	
$R_{th(ja)}$	Thermal resistance junction to air				29	K/W	Based on JESD-51
P_{TOT}	Total power dissipation allowed in the chip				1.8	W	
$V_{ESD(HBM)}$	electrostatic discharge voltage; Human Body Model (HBM)	1500 Ohm, 100 pF; JEDEC JS-001-2017 Table 2A			1500	V	All pins except TRXp/n
$V_{ESD(HBM), TRX}$	electrostatic discharge voltage; Human Body Model (HBM)	1500 Ohm, 100 pF; JEDEC JS-001-2017 Table 2A			750	V	ESD-sensitive pins: TRXp/n
$V_{ESD(CDM)}$	electrostatic discharge voltage (Charge Device model)	Field induced model; JEDEC JS-002-2018			1000	V	
I_{LU}	Latch up	AEC-Q100 (Transient current)	100			mA	
V_{inmax}	Maximum input voltage at digital IO pins		-0.3		V_{DDIO}+0.3	V	
I_{iomax}	Maximum current into digital IO pins				4	mA	

Table 2: Absolute Maximum Ratings

2.2 Electrical Characteristics

Unless noted otherwise, typical condition T_A=25°C, V_{BAT}= 5.4V, V_{VDPA}= 5V, F_{ref_clk} = 27.12MHz, V_{ref_clk}=1.8Vpp.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
T_A	Ambient temperature		-40		70	°C	
T_J	Junction temperature		-40		120	°C	
V_{BAT}	Supply voltage		2.7		5.5	V	
V_{DDIO}	Pad supply voltage		1.62		5.5	V	
V_{VDPA}	Transmitter supply		2.5		V_{BAT}	V	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
V_{SEN_H}	System Enable (SEN) pin high-level voltage range		1.62		V_{BAT}	V	
V_{IH}	GPIO pins high level input voltage		0.75*V_{DDIO}		V_{DDIO}	V	
V_{IL}	GPIO pins low level input voltage		0		0.15*V_{DDIO}	V	
V_{OH}	GPIO pins high level output voltage[4]		V_{DDIO}-0.5		V_{DDIO}	V	
V_{OL}	GPIO pins low level output voltage		0		0.45	V	

Table 3: Operating Range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
I_{PD}	Power down current consumption	V_{BAT} = 3.6V SEN=0		3		uA	
I_{STBY}	Standby current consumption	V_{BAT} = 3.6V		15		uA	
I_{CD_rd}	Low power card detection current consumption	V_{BAT} = 5.5V		100		uA	2Hz polling frequency with optimized reading distance
I_{VDPA}	Transmitter input current				650	mA	

Table 4: DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
$V_{in\_rx\_rd}$	RX carrier signal reader		100m		50	Vpp	differential
$S_{in\_RX\_rd}$	RX sensitivity AM			-80[5]		dBc	$V_{in\_rx\_rd}$ ≥25Vpp
$H_{out\_tx\_rd}$	Transmitter output harmonics			-60		dBc	
C_{out_tx}	Transmitter serial output capacitance			640		pF	

Table 5: Receiver / Transmitter Characteristics

[4] *VOH measurement condition: Iload=2.8mA with VDDIO=4.5V; Iload=0.4mA with VDDIO=1.62V.*
VOL measurement condition: Iload=2.1mA with VDDIO=4.5V; Iload=0.6mA with VDDIO=1.62V.

[5] *To achieve -80dBc RX sensitivity, V_{VDPA} shall not have voltage ripple higher than 500uVrms (V_{VDPA} = 5V) around the carrier frequency (±1MHz).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
F_{ref_clk}	Reference clock input frequency		13.15	27.12	52	MHz	
$V_{ref\_clk\_low}$	Reference clock input voltage low		0		400	mV	
$V_{ref\_clk\_high}$	Reference clock input voltage high		1.4		1.95	V	
Δf_{ref_clk}	Reference clock frequency tolerance		-50		+50	ppm	
$DC\_f_{ref\_clk}$	Reference clock duty cycle		40	50	60	%	

Table 6: Reference Input Frequency Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Remarks
F_{xtal_clk}	Reference clock input frequency			27.12		MHz	
Δf_{xtal_clk}	Reference clock frequency tolerance		-50		+50	ppm	
ESR	Equivalent serial resistance				150	Ohm	
C_L	Load capacitance			6		pF	On chip available

Table 7: Crystal Requirements

3. Functional Description

3.1 System Architecture

PTX100R is a highly integrated reader IC using a split-stack SW architecture, allowing flexible adaptation of SW to the needs of the application system such as POS, IoT/NFC Reader etc. This flexibility is achieved by an optimized software interface and ready to use SW-stack for the host-controller. The portable SW stack written in C, implements high level NFC functionality and provides easy to use APIs for integration into the Host system.

As shown in Figure 3, on the Host Controller, the EMVCo® main application (typically EMV L2 Stack) makes use of the EMVCo® L1 stack; this one abstracts the interaction to the NFC Hardware through a very intuitive L1 API.

The PTX solution is modular and runs on different platforms, providing additional facilities for custom features in case needed.

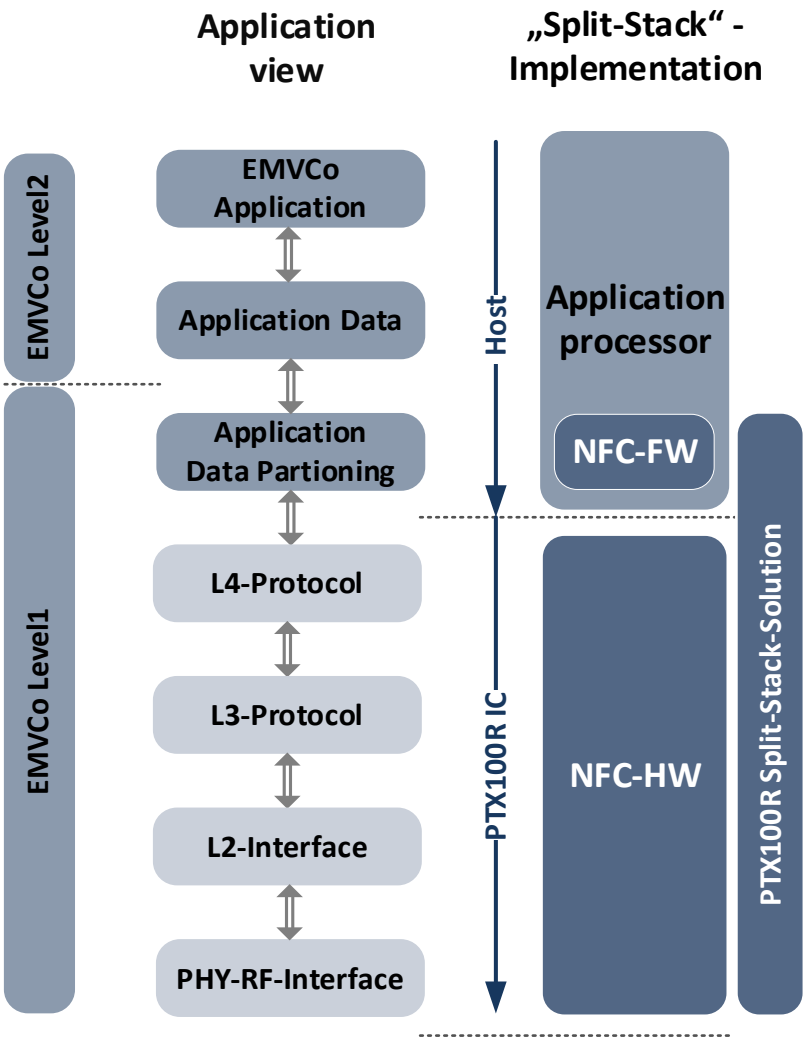


Figure 3: System Architecture to show Interface with PTX100R for EMVCo® Application

3.2 Power Management

The power management unit is the central circuit of the PTX100R responsible for providing all necessary reference voltages and currents, generating the internal supply domains, implementing the power-up sequence, and controlling the transitions between different energy states.

3.2.1. Power Supply Concept

PTX100R has 4 externally accessible supply domains which are described as follows:

3.2.1.1. VBAT

VBAT is the main supply domain from which all functional blocks are supplied. To operate PTX100R this supply must always be present.

3.2.1.2. D18VD

The internally generated core supply is routed to pin D18VD for external supply blocking. Hence external supplies are not allowed to be connected. For recommended blocking components please refer to the relevant application note.

3.2.1.3. VDDIO

Pad supply for all GPIO- and HIF/SIF-pins. It must be present during start-up for proper host-interface selection and afterward for host interface communication. In power-down mode, the voltage may be removed from this domain, but the pin shall not be pulled to VS (i.e. to be put to HiZ).

If for power saving reasons at any point in time the VBAT domain is switched off, then VDDIO must also be removed.

3.2.1.4. VDPA

The VDPA is the power supply for transmitter block, it can be connected to the same supply as V_{BAT}. The voltage on this pin has a direct impact on the maximum available power to be transmitted by PTX100R. The voltage on VDPA should be equal or lower than V_{BAT}.

3.2.2. SEN-Pin

The SEN-pin is used to boot up the PTX100R (logic-high level) or to bring the IC into power-down state (logic-low level). Detailed ranges for the logic-levels are given in Table 3.

Note that SEN-input voltage must never exceed V_{BAT}. For safe operation, SEN shall change to a logic low before V_{BAT} drops below V_{BAT_min} (value defined in Table 3).

Logic-low level pulses with smaller than 3.4 us pulse width on SEN-pin will not change the current energy state of the IC. Negative pulses that are slightly longer will first reset the internal state and for even longer negative pulses the IC changes the energy state to power-down mode. The exact pulse width below which a reset is triggered, and above which power-down mode is entered depends on the blocking capacitor value on D18VD-pin.

3.2.3. Supply Ramp-Up Sequence

For the supply ramp-up two sequences are proposed: a default sequence with SEN pin at logic-low for relaxed timing constraints between V_{BAT} and V_{DDIO}, and a sequence with SEN pin connected to V_{BAT} for simpler configuration and faster start-up (VDPA can be ramped up same time as VBAT or later).

Ramp-up sequence with SEN at logic-low (transition into power-down mode):

- First, the battery supply V_{BAT} shall be ramped up – the IC remains in power-down mode
- V_{DDIO} shall be ramped up. V_{DDIO} may ramp concurrently to V_{BAT}.
- V_{DDIO} supply and a stable state of SIF1/SIF2 pins shall latest be available when the SEN pin voltage reaches a valid logic-high level. These timings also apply when leaving power-down mode with disabled V_{DDIO}.

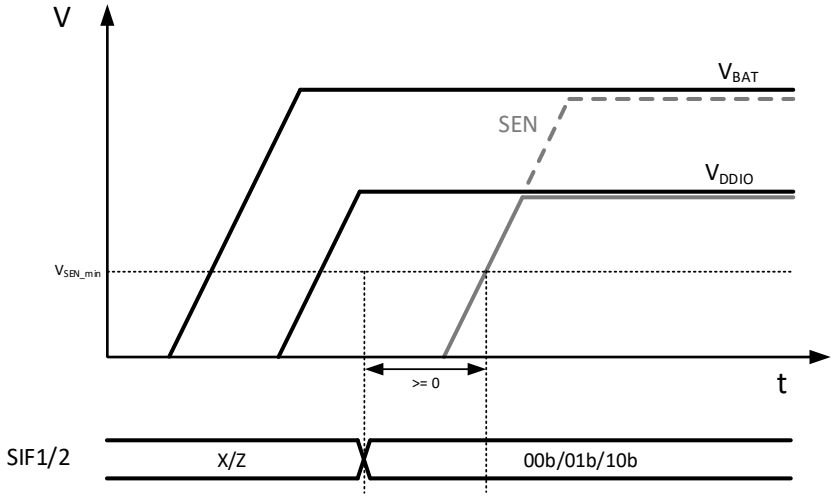


Figure 4: Supply Ramping Up (SEN at logic-low)

Ramp-up sequence with SEN at logic-high (transition into full-power mode):

- First, the battery supply V_{BAT} together with SEN pin voltage shall be ramped up.
- V_{DDIO} shall be ramped and shall be at V_{DDIO_min} latest 100 us after V_{BAT} exceeds V_{BAT_min} (i.e. 2.7 V). Latest at this point also the state of the SIF1/SIF2 pins shall be stable.

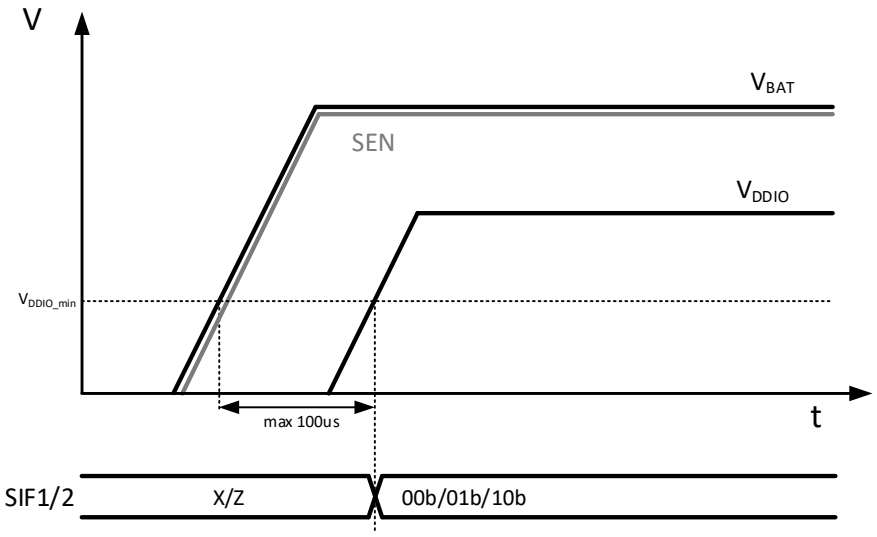


Figure 5: Supply Ramp Up (SEN==VBAT)

In typical applications, after SEN, V_{DDIO} and SIF pins reach their stable level, PTX100R is ready for operation in less than 1ms.

As SIF pins select the interface to be used and are only captured at boot time, it is important that the logic level of SIF pins is set at the right time during the power-up process.

3.2.4. Energy States

To support the implementation of flexible system power consumption profiles, PTX100R offers different energy states, each being a trade-off between functionality and power consumption.

3.2.4.1. Full-Power Mode

This is the main operating mode of PTX100R, in which all internal supply domains are ramped up and all internal clocks are running. This mode is activated by applying a logic-high level at SEN-pin.

In this mode, PTX100R is fully active and can communicate with the host controller via the host interface.

3.2.4.2. Power-Down (PD) mode

For maximum power saving, PTX100R can be set to power-down mode by applying a logic-low level at SEN-pin. In this mode PTX100R consumes its lowest power and does not react to any external events. All GPIO-pins and the SIF1/SIF2-pins are switched to HiZ-state.

After leaving this mode the internal state of PTX100R is reset.

3.2.4.3. Standby (STBY) Mode

PTX100R supports Standby Mode for low power applications, with the possibility to wake up in response to selected events such as Low Power Card Detection or Host-interface activities. In this mode, a logic-high level shall be maintained on SEN-pin and the internal state of PTX100R is fully maintained.

Depending on the application, different wake-up sources (e.g. execution of Polling loop, LPCD/LPFD procedure) can be defined by the customer. Once configured, it runs autonomously and no interaction with the Host is required.

Events triggering the wakeup of the IC from standby mode include:

- Activity on Host-interface
- Execution of Polling
- LPCD/LPFD procedure

3.3 Clock Concept

In PTX100R a low-power oscillator (LPO), a crystal oscillator (XO) and a phase-locked loop (PLL) are the main blocks responsible for generating the necessary internal clocks in the various modes.

The reference clock for PTX100R can either be provided from an external clock source or the internal crystal oscillator can be employed. Out of this clock, the PLL subsequently derives the system frequency of 13.56MHz.

3.3.1. Low Power Oscillator (LPO)

The low-power oscillator is the lifeline of PTX100R, and its 125kHz-clock is particularly employed during IC ramp-up and in standby mode, when the internal PLL is powered down to save energy.

3.3.2. Crystal Oscillator (XTAL)

The internal crystal oscillator is designed for crystal types with a resonant frequency of 27.12MHz, which shall be externally connected between XIN- and XOUT pins. The oscillator will also work with other crystals around this frequency - please contact Renesas for support.

The PTX100R features internal caps of 6pF each from XIN- and XOUT-pins to GND to act as crystal load capacitors.

3.3.3. External Reference Clock

An external reference clock with frequency between 13.15MHz and 52MHz can be applied to XIN pin. Detailed requirement on the external reference clock is specified in Table 6.

3.3.4. Phase Lock Loop (PLL)

A fractional-N PLL produces the core clock that is used to derive all the needed internal clocks.

A Delta-Sigma Modulator (DSM) is used to program the N division word of the fractional-N PLL. This allows very fine frequency resolution of all clocks and output frequencies.

3.4 Contactless Interface

Lower-level functionality up to communication framing is available through the Contactless Frontend, higher level functionality is implemented via the RF-Subsystem of the on-chip MCU (see chapter 3.6.1)

Figure 6 gives a block level overview of the Contactless Interface. At TRXp/TRXn pins the device is connected via a matching network to the antenna of the system.

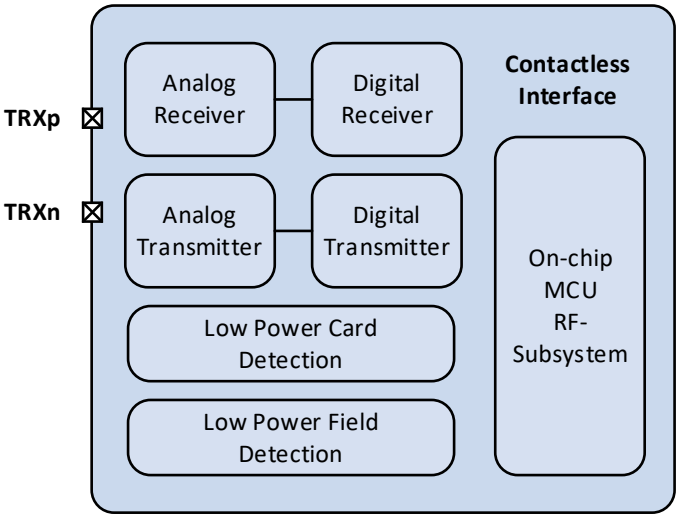


Figure 6: Contactless Interface

3.4.1. Analog/Digital Transmitter

In PCD mode, the transmitter generates the RF-field and consequently amplitude-modulates the PCD commands on the RF-carrier according to the selected communication type.

The analog transmitter itself consists of a digital-like topology, which allows to directly output sinusoidal carriers with high spectral purity and high efficiency. Therefore, EMC-filters, which are required in conventional products in the matching network of Reader-antennas, can be omitted. Additionally, direct antenna connection allows to shape the modulation in a very fine granularity. PTX100R offers dynamic wave-shaping feature, which optimizes the modulation shapes to fulfill the requirements of the final application – see chapter 3.4.6 for details.

The digital transmitter is responsible for encoding the command/data to be sent, applying the respective modulation according to the selected communication type and synchronization of the modulation with the carrier.

The output power of the transmitter can be adapted directly by adjusting the sinusoidal amplitude based on the Received Signal Strength Indicator (RSSI). The RSSI level to trigger the switch of output power

can be simply defined as parameter and used as input for the software API. More details on Digital Dynamic Power Control (DDPC) are explained in chapter 3.4.7.

3.4.2. Analog/Digital Receiver

The receiver, consisting of an analog and a digital part, is responsible for reception, demodulation and signal processing of incoming commands and data from the communication counterpart of PTX100R.

The analog receiver is based on an I/Q-architecture in the RF-domain, which is followed by a baseband chain with programmable gain amplifiers and filters to properly adjust the received signal from varied sized antennas to the full-scale range of the ADC.

The digital receiver provides means to configure the digital detection threshold on a fine granularity to optimize sensitivity while ensuring good noise immunity. The received information is then extracted on a bit- and frame-level to finally obtain the transmitted command/data.

For easy integration into the customer application, parameters such as PGA gain and digital RX-threshold can be adapted based on the target applications, while RF-protocol related parameters such as filter frequency settings stay pre-defined and unmodified.

3.4.3. Polling Loop

Polling loop is the center of all NFC-applications. In a loop PTX100R executes polling sequences through the defined RF-protocol following well-defined timing specifications. Depending on the use-case and SDK variant, PTX100R can be configured to execute one of the three different scenarios:

- EMVCo payment polling loop which permanently polls for TypeA and TypeB RF-technology; optionally Felica can be included as preliminary protocol
- Standard NFC applications, which polls for selected technologies in defined intervals. Between the polling cycles PTX100R either stays idle or enters standby to reduce power consumption
- Low-Power application. For Reader applications, the Low Power Card Detection mechanism is used to significantly reduce power consumption (see chapter 3.4.4 for more information).

  For applications where Host-Card-Emulation functionality is required, Low Power Field Detection can be enabled during Standby mode to detect the existence of an external RF field (see Chapter 3.4.5 for more information).

Polling interval together with the above-mentioned RF-protocol configurations can configured by the customer based on the target application and used as input parameters of the SW API.

3.4.4. Low Power Card Detection (LPCD)

To optimize the power consumption for low power applications, PTX100R supports Low Power Card Detection (LPCD) feature. LPCD is used to check if a PICC is within the communication range without immediately starting a power-hungry communication. Only when a PICC is present, normal polling will be initiated, otherwise PTX100R goes back to standby. The interval for LPCD is a configurable parameter which can be optimized for different applications.

To check the amplitude and phase of the antenna and determine if a PICC is present, only a reduced set of the hardware blocks are enabled in LPCD mode. Additionally, the active time of Transmitter, the most power consuming block, is kept to minimum. Comparing with normal polling mode which executes communication commands according to standard and requires Transmitter to be active for at least several milliseconds, in LPCD mode the transmitter is only active for less than 100us.

The power consumption in LPCD mode can be further optimized by adjusting the output amplitude.

Thanks to the split-stack architecture, the Low Power Card Detection is performed by PTX100R autonomously. Once LPCD mode is configured, the Host MCU is not required anymore, thus can go to lower power mode. In case a PICC is discovered, the host will be notified by PTX100R.

3.4.5. Low Power Field Detection (LPFD)

To enable low power applications in Card Emulation mode, PTX100R supports Low Power Field Detection (LPFD) feature. A dedicated Wake Up Receiver (WURX) block is used to sense the presence of an RF-field. The WURX block is enabled periodically and only when an RF-Field is detected, a system wakeup from standby is triggered.

The detection threshold as well as the interval for LPFD is customer configurable. In this way the performance and power consumption can be optimized based on the individual application.

3.4.6. Wave-Shaping

One of the great features enabled by the sine-wave transmitter is an advanced wave-shaping capability for the modulation on the RF-Field. As the change of sine-wave amplitude is directly fed to the antenna without being influenced by external matching components such as the EMI filter, the shape of the modulation edges can be adjusted directly if needed.

To achieve this, PTX100R offers the possibility to add up to 8 cycles with different sine-waves amplitude between the unmodulated carriers and the carriers with modulation applied. This can be independently done for the falling and the rising modulation edge.

3.4.7. Digital Dynamic Power Control (DDPC)

To maintain a stable output power within a given volume (e.g. EMVCo compliance requirement), the output of PTX100R can be switched between different levels based on the measured RSSI value. The RSSI value indicates the amplitude of the RF-Field generated by the PTX100R, which changes under the influence of load depending on the distance.

When a load on the antenna is detected at a close distance, which is indicated by a lower RSSI value, PTX100R automatically reduces the output power to a predefined low-power level. Conversely when the load is further away it switches back to the high-power mode.

Figure 7 below illustrates the principle behind the DDPC: for a given antenna system an upper and a lower RSSI threshold can be defined. When the PTX100R operates in high-power mode and the measured RSSI value drops below the upper threshold, the transmitter is switched to the low-power mode. Similarly, when in low-power mode and the RSSI exceeds the lower threshold a switch back to high-power mode is performed. Enough hysteresis between upper and lower switching level ensures a stable performance.

DDPC algorithm is executed on PTX100R directly, which means no host-interaction is needed.

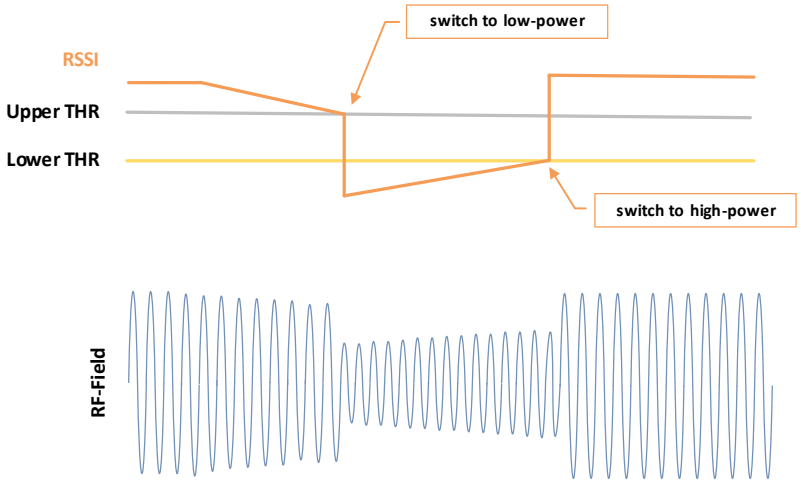


Figure 7: Dynamic Digital Power Control (DDPC)

3.5 Other Supported Features

3.5.1. Temperature Sensor and Over-Temperature Protection

PTX100R features an on-chip temperature sensor that continuously monitors the die temperature. In case the temperature exceeds a configurable threshold, the transmitter is automatically disabled.

3.5.2. Auxiliary Digital-to-Analog Converter (AUX-DAC)

PTX100R comprises a 5-bit general-purpose digital-to-analog converter (DAC), which operates from the V_{BAT} domain and whose output is available at the DAC_O pin.

3.5.3. GPIO Customer Usage

PTX100R provides customer access to 8 GPIOs. These GPIOs can be configured as input or output separately, depending on the customer application. Specially for system with small MCU, this feature releases the load on the Host greatly.

3.6 Programmable Control Logic

PTX100R is a highly integrated NFC device greatly unloading the host device in respect to contactless communication effort. This is achieved by handling major parts of the contactless protocols up to NFC-Forum ISO-DEP protocol or EMVCo Block Transmission Protocol directly on the IC using the Renesas NSC (NFC Soft Controller) interface. On top the Renesas SW stacks takes care of data aggregation and management, providing easy to use APIs to the user.

Time-critical high-level functions, such as ISO-DEP frame de-/composition, automatic frame re-transmission, WTX handling, EMD handling, etc, are implemented by a programmable control logic circuit – the on-chip MCU – guaranteeing great execution speed.

3.6.1. On-chip MCU

The on-chip MCU executes the program downloaded to the PTX100R code-memory. It has access to all internal status information as well as the configuration mechanisms.

After downloading the micro-code (uCode) the on-chip MCU can be enabled. Subsequently, it accepts NSC commands for handling all tasks.

3.6.2. PTX100R Device Control Firmware

3.6.2.1. uCode Download Mechanism

Before enabling the on-chip MCU, the devices uCode must be downloaded. This is done via the host-interface by utilizing the Write-Instruction functionality.

3.6.2.2. Accelerator Enable

Activating the on-chip MCU is achieved by writing the corresponding command to the device.

3.6.2.3. Soft-Reset

PTX100R provides a Soft-Reset functionality that resets all digital blocks and disables all analog blocks (same condition as after boot).

3.7 Host Interface

PTX100R supports the most used industry standard host interfaces, namely SPI up to 10Mbps, I2C up to 3.4Mbps and UART with data-rates from 9.6kbps up to 3.4Mbps.

The host interface is designed for typical interface supply voltages used by micro-controllers in the range of 1.8V to 5V which must be supplied by the host via the VDDIO pin.

3.7.1. Host-Interface Selection

Only one interface type is available at a time and the configuration can only be changed when PTX100R is in power-down state. Host interface selection is done via the configuration pins SIF1 and SIF2 at startup. A change of the pin state after boot does not have any effect on the selected interface type.

The following table describes the selection of host interface with respect to the value at the SIF pins:

{SIF2, SIF1}	HIF
2'b00	SPI
2'b01	I2C
2'b10	UART
2'b11	Reserved for test

Table 8: Host Interface Selection

3.7.2. Host-Interface Lines

4 pins (HIF1-HIF4) are utilized for the host interface communication, depending on the selection, configuration, and application at least 2 HIF pins and up to all 4 are used.

Table 9 specifies the pin assignment for the chosen interface type. For SPI, all HIF-interface pins are used during the communication. In contrast, for I2C HIF1 and HIF2 (corresponding to the ADDR0 and ADDR1 pins) are only needed at startup to define the last two bits of the I2C-address. For UART mode HIF1 and HIF2 (CTS and RTS) are used for flow control.

PIN	SPI	I2C	UART
HIF1	NSS	ADDR0 [1)]	CTS [2)]
HIF2	SCK	ADDR1 [1)]	RTS [2)]
HIF3	MOSI	SDA	RXD
HIF4	MISO	SCL	TXD

Table 9: Pin Assignment for HIF Selection

1) LSBs of I2C address, evaluated at boot
2) Flow-control pins

3.7.3. IRQ Line

PTX100R has an exclusive IRQ line used to signal the host a communication request.

For SPI and I2C interface asserting an IRQ is the only possibility to initialize a transmission from PTX100R to the host.

The UART interface in contrast, provides a special "push" mode, allowing PTX100R to initiate a transfer and transmit notifications to the host directly without the host starting the transfer. This mode is only usable with hardware flow-control enabled. In this mode, no IRQ line is needed.

3.7.4. SPI

PTX100R implements a standard SPI interface supporting the SPI mode 0 (CPOL = 0, CPHA = 0), i.e. the clock must be low when data changes and data is captured at the leading clock edge after NSS is de-asserted.

It uses 4 signal lines for communication:

- Not-Slave-Select (NSS): Active low input to select the device. A communication is initiated by pulling NSS low. When NSS is high the data output MISO is disabled
- Serial Clock (SCK): Clock input for the SPI interface.
- Master-Out-Slave-In (MOSI): Serial data line from host (master) to PTX100R. Data is registered at positive edge of the clock
- Master-In-Slave-Out (MISO): Serial data line from PTX100R to host (master). Data is shifted on negative edge of the clock

Figure 8 below illustrates a standard SPI transfer with mode 0. The communication starts on pulling NSS line low.

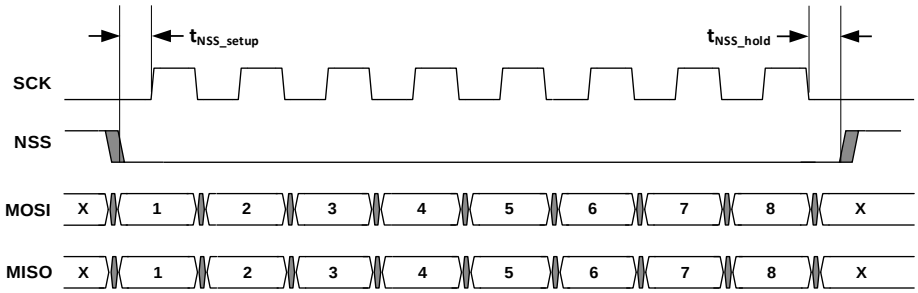


Figure 8: SPI mode 0 (CPOL, CPHA = 0)

Data transfers must always be byte aligned, i.e. the number of bits transmitted is a multiple of 8. Furthermore, the minimum numbers of bytes per frame are 2 (1 header byte + 1 data byte) and frames must be transmitted at once – without pulling NSS high in between.

Further timing characteristics for SPI interface are specified in Table 10.

Symbol	Parameter	Min	Typ	Max	Unit	Remarks
f_{SCK}	SPI clock frequency			10	MHz	
DC_{SCK}	SPI clock input duty cycle	40	50	60	%	
t_{NSS_setup}	Setup time from NSS low to rising edge of SCK	25			ns	
t_{NSS_hold}	Hold time from falling edge of SCK to NSS high	25			ns	

Table 10: SPI Timing Characteristics

3.7.5. I2C

The I2C interface provided by PTX100R is according to the revision 6 of NXP I2C-bus specification. Following modes are supported by the device:

- Standard-mode (Sm), with a bit rate up to 100 kbps
- Fast-mode (Fm), with a bit rate up to 400 kbps
- Fast-mode Plus (Fm+), with a bit rate up to 1 Mbps
- High-speed mode (Hs-mode), with a bit rate up to 3.4 Mbps

PTX100R supports 7-bit addressing, where the 2 LSBs of the devices I2C-address can be configured via the pins HIF1 and HIF2 at start-up. In contrast, the upper 5 bits are fixed to 10011(b), resulting in an address between 0x4C and 0x4F (see Table 11).

7bit I2C Address	HIF2 pin	HIF1 pin
0x4C	0	0
0x4D	0	1
0x4E	1	0
0x4F	1	1

Table 11: I2C Address Selection depending on HIF Pin Setting

Clock-stretching is not used by the PTX100R, i.e. no delaying of the communication is necessary.

3.7.6. UART

PTX100R supports serial communication UART communication mode with flow-control up to a data-rates of 3.4 Mbps. As there is no common clock reference for the UART interface the data-rate reference must be very accurate.

A transaction starts with a Start-of-Frame (SOF) symbol, i.e. one byte with value 0x55, followed by a byte indicating the length of transmission payload (TXL). The TXL specifies the number of payload bytes following. A TXL == 0x00 specifies a length of 256 byte.

Every response from PTX100R starts with the length of reception payload (RXL). As for the transmission, the RXL specifies the number of bytes to follow, but only values from 1 to 255 are possible. In case no response is expected (write only transactions) the device sends a one byte acknowledge putting RXL to 0x00.

After boot, baud-rate detection is enabled and accepts data rates of 9.6kbps or 115.2kbps. Once the clock system is configured correctly, data rates up to 3.4Mbps can be used.

As mentioned above, hardware flow control (RTS/CTS – both polarities are possible) must be enabled as TX-push mode is used for communicating with PTX100R.

To further improve communication stability, stop bit can be extended to 2 bits instead of 1 bit.

3.8 FW/SW Functionality

3.8.1. NSC-Interface

To access PTX100R, an optimized high-level software interface is implemented providing functions for device configuration as well as all data communications.

The interface is based on messages which carry commands, responses, and notifications. Commands are always sent by the host; responses are generated by the PTX100R as reactions to commands. Notifications are transmitted by the PTX100R to indicate the host an event has occurred and is usually asynchronous to commands.

Data packages between PTX100R and the host are called NSC Data messages, and the RF/NFC specific protocol related header bytes are managed by the on-chip MCU automatically.

3.8.2. SW Split Stack

Renesas provides additional SW-stacks on top of the NSC interface to further ease the integration of the PTX100R into the target application. The SW stacks manage all interactions with the PTX100R on

NSC level, by setting up and configuring the device, consolidating status information, handling error messages, and establishing a data channel between the host and the NFC controller.

Two versions of SW stacks are available for PTX100R:

- POS stack is intended for EMVCo® payment applications, providing a full, ready to use Level 1 layer.
- IoT stack is suitable for standard NFC reader use-cases, easing the creation of full NFC applications.

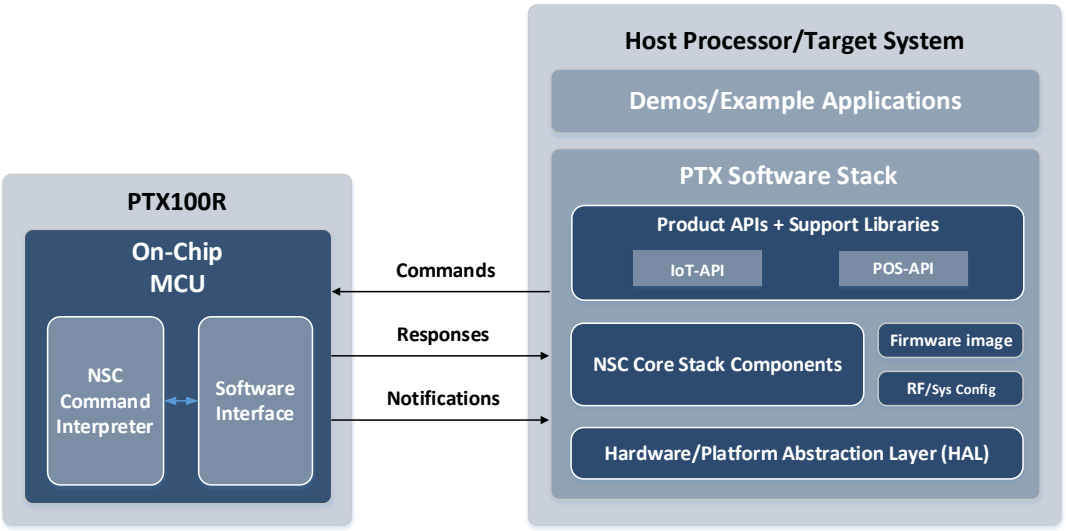


Figure 9: PTX100R SW Stack Integration View

For more details on the PTX100R SW integration, please refer to the integration manual accordingly.

4. Reference Schematic

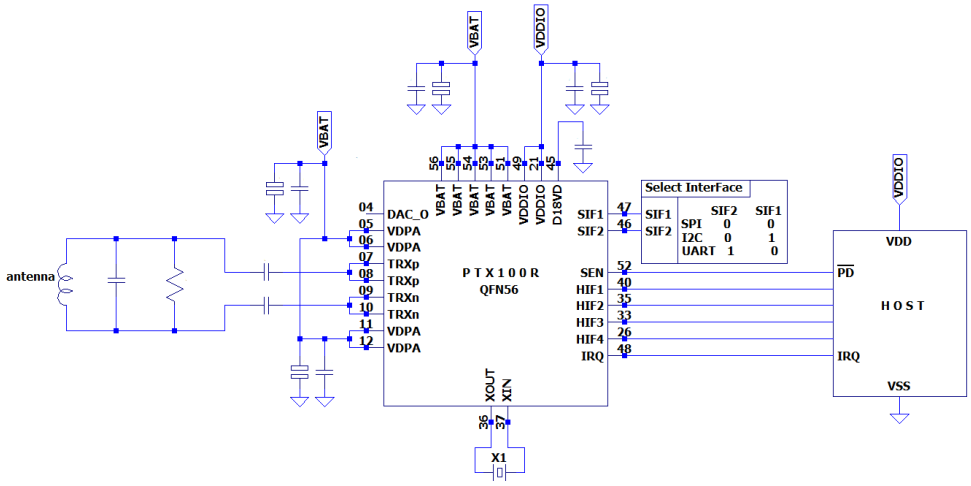


Figure 10: Exemplary Reference Schematic

5. Ordering and Package Information

5.1 Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
PTX100RDQ56D13	HVQFN56	7x7	Tape & Reel	3000

Table 12: Ordering Information

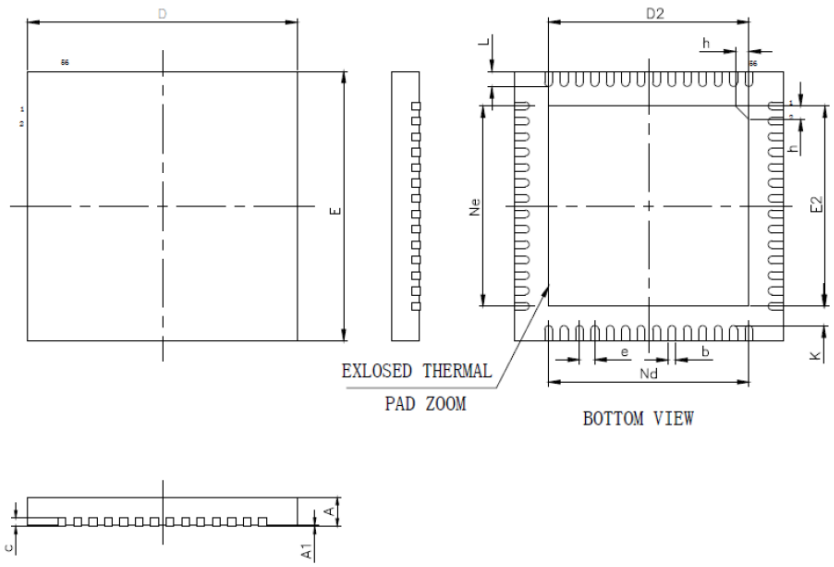
5.2 Package Marking

Figure 11: Package Marking

Symbol	Description
PTX100R	Device Name
XXXXXX.X	Wafer Lot No.
YYWW	Production year/week

Table 13: Marking code HVQFN56

5.3 Package Drawing and Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.10	5.20	5.30
e	0.40BSC		
Nd	5.20BSC		
Ne	5.20BSC		
E	6.90	7.00	7.10
E2	5.10	5.20	5.30
K	0.20	—	—
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	217*217		

Figure 12: Package Drawings and Dimensions