

R1RW0416DI Series

Wide Temperature Range Version
4M High Speed SRAM (256-kword × 16-bit)

R10DS0283EJ0100
Rev.1.00
Nov.18.19

Description

The R1RW0416DI is a 4-Mbit high speed static RAM organized 256-kword × 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The R1RW0416DI is packaged in 400-mil 44-pin SOJ and 400-mil 44-pin plastic TSOPII for high density surface mounting.

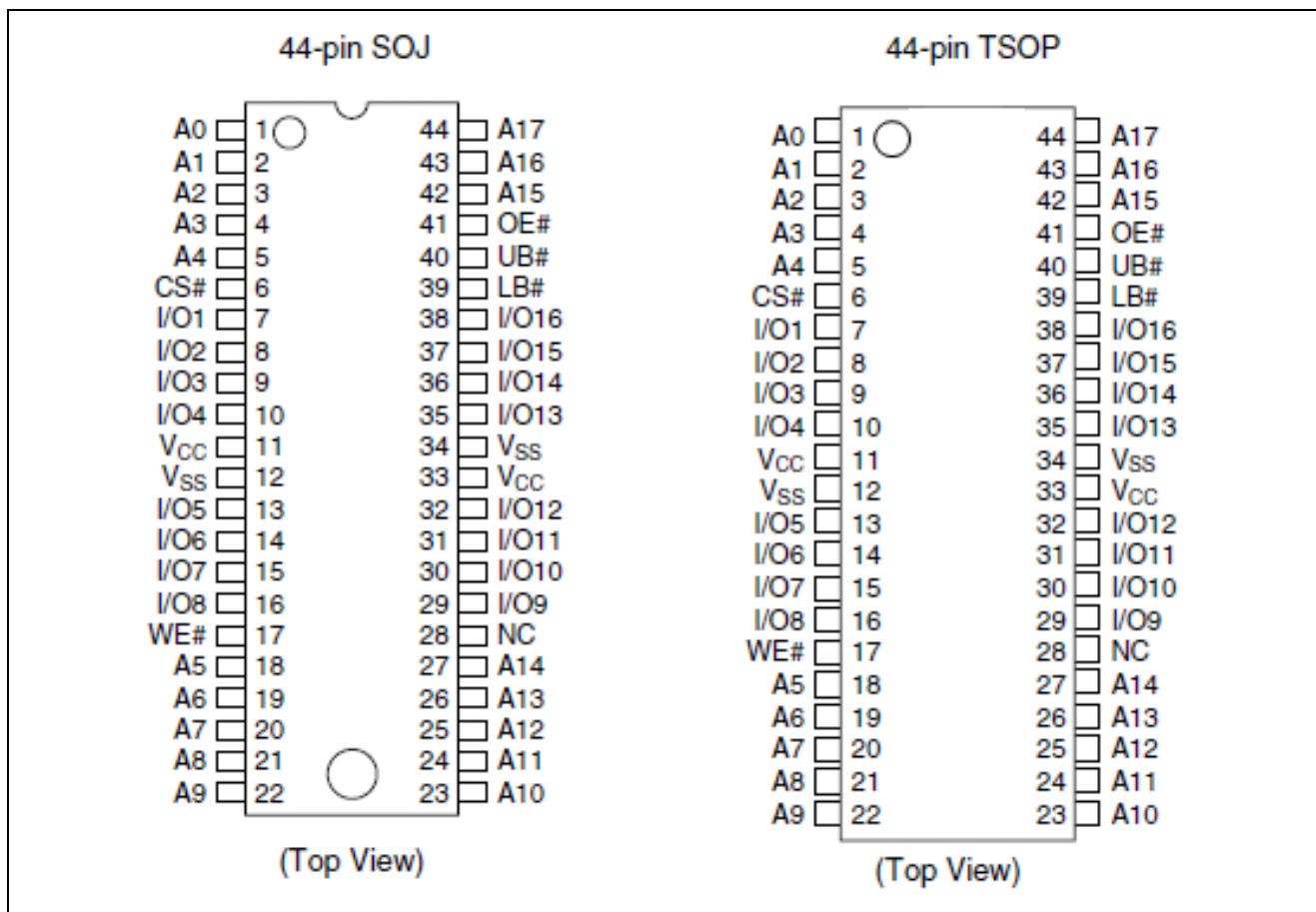
Features

- Single 3.3V supply: 3.3V ± 0.3V
- Access time: 10ns / 12ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current: 145mA / 130mA (max)
- TTL standby current: 40mA (max)
- CMOS standby current : 5mA (max)
- Center V_{CC} and V_{SS} type pin out
- Temperature range: -40 to +85°C

Ordering Information

| Type No. | Access time | Package |
|-----------------|-------------|-------------------------------|
| R1RW0416DGE-2PI | 12ns | 400-mil 44-pin plastic SOJ |
| R1RW0416DSB-0PI | 10ns | 400-mil 44-pin plastic TSOPII |
| R1RW0416DSB-2PI | 12ns | |

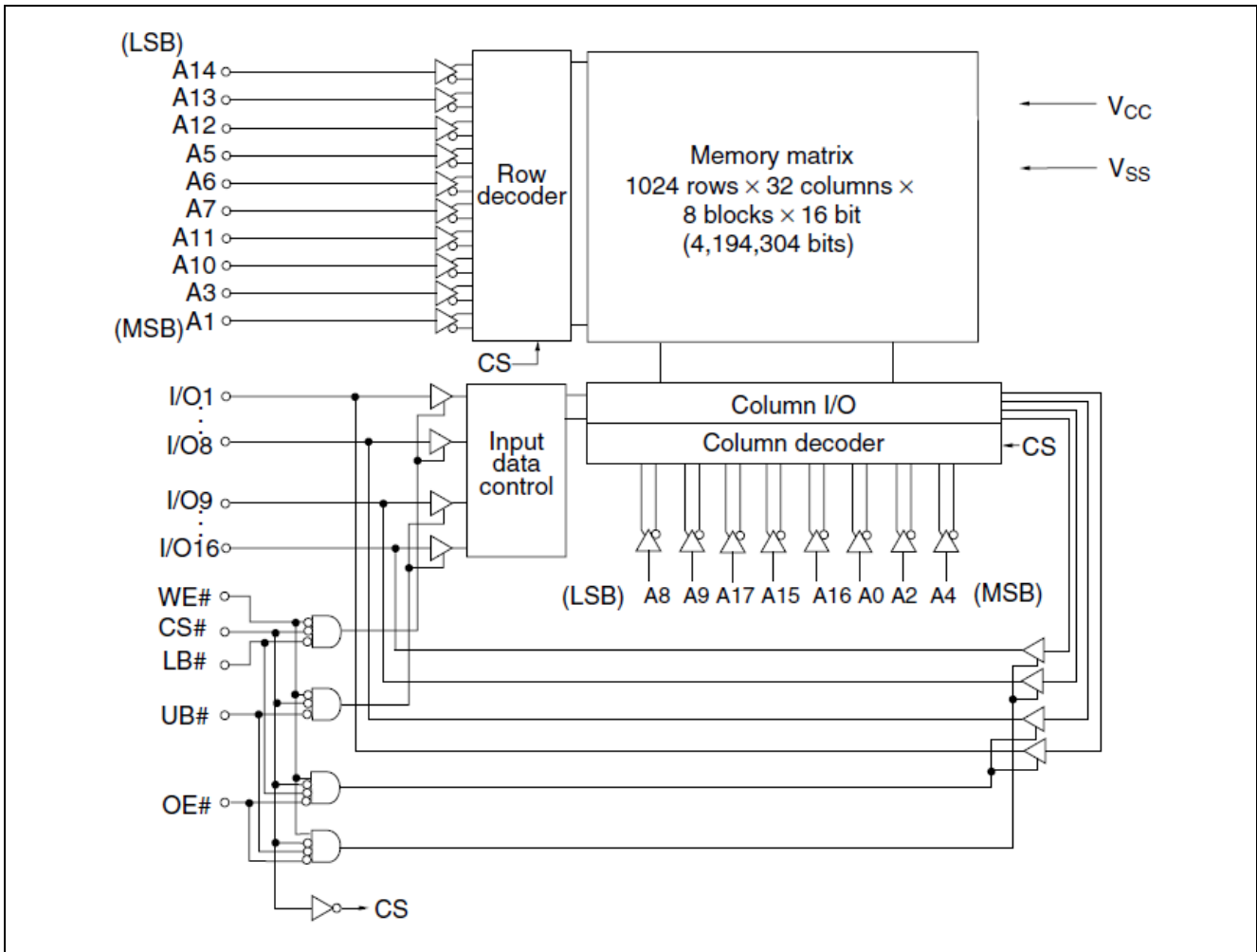
Pin Arrangement



Pin Description

| Pin name | Function |
|-----------------|-------------------|
| A0 to A17 | Address input |
| I/O1 to I/O16 | Data input/output |
| CS# | Chip select |
| OE# | Output enable |
| WE# | Write enable |
| UB# | Upper byte select |
| LB# | Lower byte select |
| V _{CC} | Power supply |
| V _{SS} | Ground |
| NC | No connection |

Block Diagram



Operation Table

| CS# | OE# | WE# | LB# | UB# | Mode | V _{CC} current | I/O1–I/O8 | I/O9–I/O16 | Ref. cycle |
|-----|-----|-----|-----|-----|------------------|------------------------------------|-----------|------------|-------------|
| H | × | × | × | × | Standby | I _{SB} , I _{SB1} | High-Z | High-Z | — |
| L | H | H | × | × | Output disable | I _{CC} | High-Z | High-Z | — |
| L | L | H | L | L | Read | I _{CC} | Output | Output | Read cycle |
| L | L | H | L | H | Lower byte read | I _{CC} | Output | High-Z | Read cycle |
| L | L | H | H | L | Upper byte read | I _{CC} | High-Z | Output | Read cycle |
| L | L | H | H | H | — | I _{CC} | High-Z | High-Z | — |
| L | × | L | L | L | Write | I _{CC} | Input | Input | Write cycle |
| L | × | L | L | H | Lower byte write | I _{CC} | Input | High-Z | Write cycle |
| L | × | L | H | L | Upper byte write | I _{CC} | High-Z | Input | Write cycle |
| L | × | L | H | H | — | I _{CC} | High-Z | High-Z | — |

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------------|-----------------------------------|------|
| Supply voltage relative to V _{SS} | V _{CC} | –0.5 to +4.6 | V |
| Voltage on any pin relative to V _{SS} | V _T | –0.5*1 to V _{CC} + 0.5*2 | V |
| Power dissipation | P _T | 1.0 | W |
| Operating temperature | Topr | –40 to +85 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –40 to +85 | °C |

- Notes: 1. V_T (min) = –2.0V for pulse width (under shoot) ≤ 6ns.
2. V_T (max) = V_{CC} + 2.0V for pulse width (over shoot) ≤ 6ns.

Recommended DC Operating Conditions

(T_a = –40 to +85°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|--------------------|--------|-----|-------------------------|------|
| Supply voltage | V _{CC} *3 | 3.0 | 3.3 | 3.6 | V |
| | V _{SS} *4 | 0 | 0 | 0 | V |
| Input voltage | V _{IH} | 2.0 | — | V _{CC} + 0.5*2 | V |
| | V _{IL} | –0.5*1 | — | 0.8 | V |

- Notes: 1. V_{IL} (min) = –2.0V for pulse width (under shoot) ≤ 6ns.
2. V_{IH} (max) = V_{CC} + 2.0V for pulse width (over shoot) ≤ 6ns.
3. The supply voltage with all V_{CC} pins must be on the same level.
4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics(Ta = -40 to +85°C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V)

| Parameter | Symbol | Min | Max | Unit | Test conditions | |
|--------------------------------|------------------|-----------------|-----|------|---|--|
| Input leakage current | I _{LI} | — | 2 | μA | V _{IN} = V _{SS} to V _{CC} | |
| Output leakage current | I _{LO} | — | 2 | μA | V _{IN} = V _{SS} to V _{CC} | |
| Operating power supply current | 10ns cycle | I _{CC} | — | 145 | mA | Min cycle CS# = V _{IL} , I _{OUT} = 0mA Other inputs = V _{IH} /V _{IL} |
| | 12ns cycle | I _{CC} | — | 130 | mA | |
| Standby power supply current | I _{SB} | — | 40 | mA | Min cycle, CS# = V _{IH} , Other inputs = V _{IH} /V _{IL} | |
| | I _{SB1} | — | 5 | mA | f = 0MHz V _{CC} ≥ CS# ≥ V _{CC} - 0.2V, (1) 0V ≤ V _{IN} ≤ 0.2V or (2) V _{CC} ≥ V _{IN} ≥ V _{CC} - 0.2V | |
| Output voltage | V _{OL} | — | 0.4 | V | I _{OL} = 8mA | |
| | V _{OH} | 2.4 | — | V | I _{OH} = -4mA | |

Capacitance

(Ta = +25°C, f = 1.0MHz)

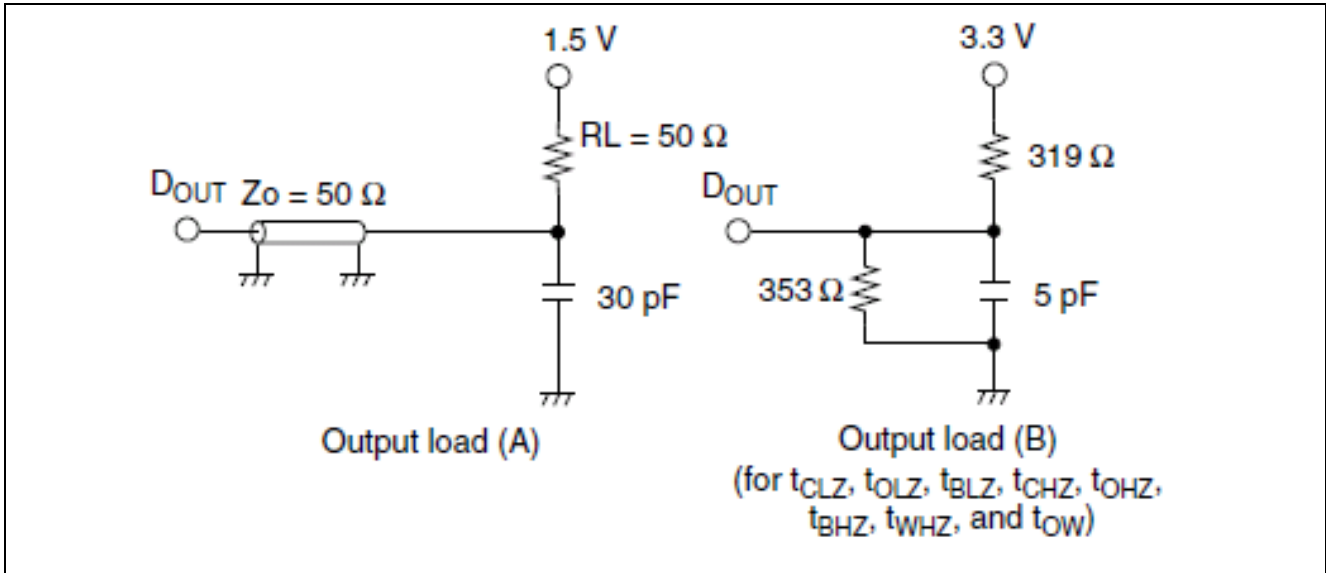
| Parameter | Symbol | Min | Max | Unit | Test conditions |
|----------------------------|------------------|-----|-----|------|-----------------------|
| Input capacitance*1 | C _{IN} | — | 6 | pF | V _{IN} = 0V |
| Input/output capacitance*1 | C _{I/O} | — | 8 | pF | V _{I/O} = 0V |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, unless otherwise noted.)

- Input pulse levels: 3.0V/0.0V
- Input rise and fall time: 3ns
- Input and output timing reference levels: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

| Parameter | Symbol | R1RW0416DI | | | | Unit | Notes |
|------------------------------------|-----------|--------------|-----|--------------|-----|------|-------|
| | | 10ns Version | | 12ns Version | | | |
| | | Min | Max | Min | Max | | |
| Read cycle time | t_{RC} | 10 | — | 12 | — | ns | |
| Address access time | t_{AA} | — | 10 | — | 12 | ns | |
| Chip select access time | t_{ACS} | — | 10 | — | 12 | ns | |
| Output enable to output valid | t_{OE} | — | 5 | — | 6 | ns | |
| Byte select to output valid | t_{BA} | — | 5 | — | 6 | ns | |
| Output hold from address change | t_{OH} | 3 | — | 3 | — | ns | |
| Chip select to output in low-Z | t_{CLZ} | 3 | — | 3 | — | ns | 1 |
| Output enable to output in low-Z | t_{OLZ} | 0 | — | 0 | — | ns | 1 |
| Byte select to output in low-Z | t_{BLZ} | 0 | — | 0 | — | ns | 1 |
| Chip deselect to output in high-Z | t_{CHZ} | — | 5 | — | 6 | ns | 1 |
| Output disable to output in high-Z | t_{OHZ} | — | 5 | — | 6 | ns | 1 |
| Byte deselect to output in high-Z | t_{BHZ} | — | 5 | — | 6 | ns | 1 |

Write Cycle

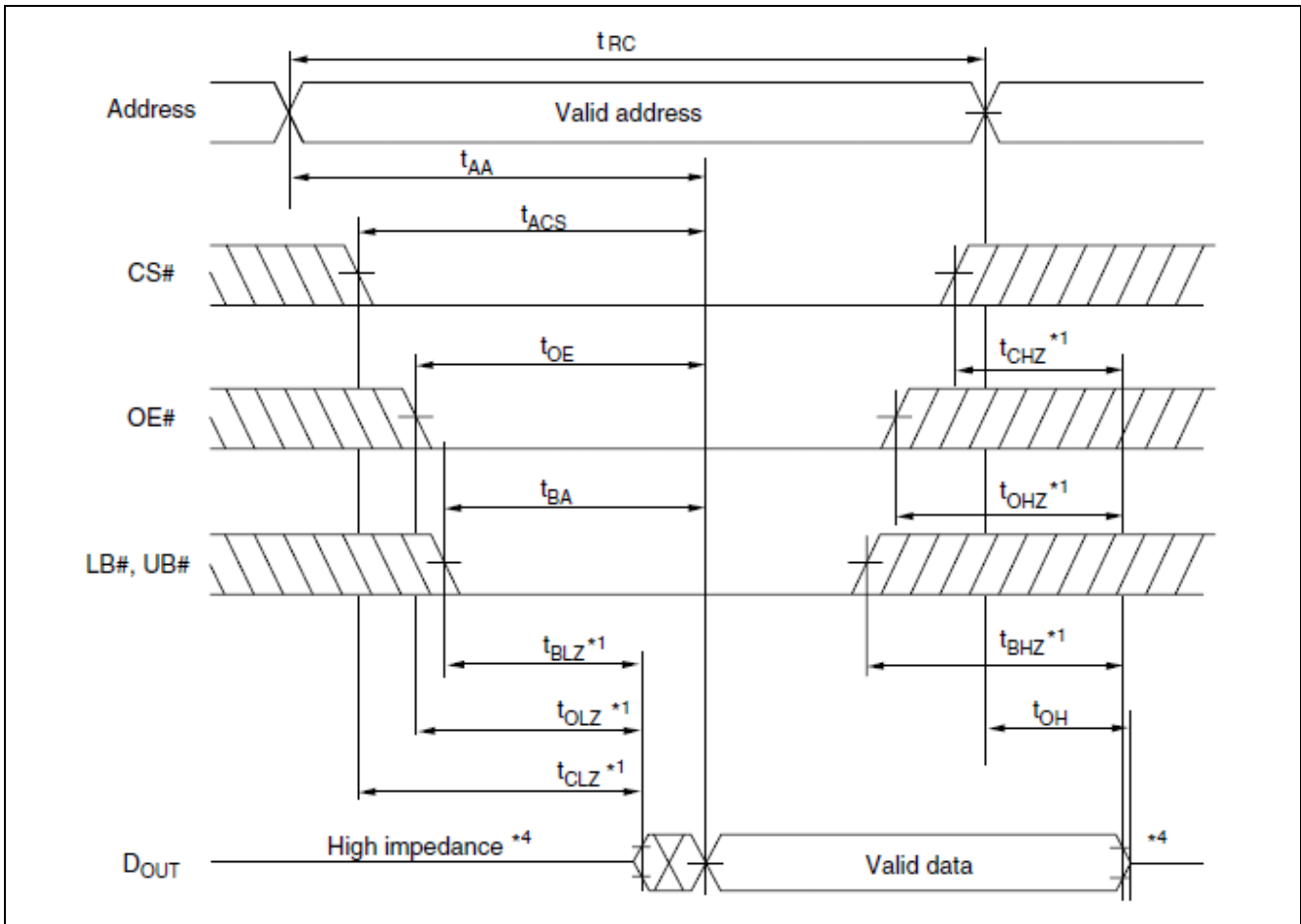
| Parameter | Symbol | R1RW0416DI | | | | Unit | Notes |
|------------------------------------|-----------|--------------|-----|--------------|-----|------|-------|
| | | 10ns Version | | 12ns Version | | | |
| | | Min | Max | Min | Max | | |
| Write cycle time | t_{WC} | 10 | — | 12 | — | ns | |
| Address valid to end of write | t_{AW} | 7 | — | 8 | — | ns | |
| Chip select to end of write | t_{CW} | 7 | — | 8 | — | ns | 8 |
| Write pulse width | t_{WP} | 7 | — | 8 | — | ns | 7 |
| Byte select to end of write | t_{BW} | 7 | — | 8 | — | ns | |
| Address setup time | t_{AS} | 0 | — | 0 | — | ns | 5 |
| Write recovery time | t_{WR} | 0 | — | 0 | — | ns | 6 |
| Data to write time overlap | t_{DW} | 5 | — | 6 | — | ns | |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | ns | |
| Write disable to output in low-Z | t_{OW} | 3 | — | 3 | — | ns | 1 |
| Output disable to output in high-Z | t_{OHZ} | — | 5 | — | 6 | ns | 1 |
| Write enable to output in high-Z | t_{WHZ} | — | 5 | — | 6 | ns | 1 |

Notes: 1. Transition is measured $\pm 200\text{mV}$ from steady voltage with output load (B). This parameter is sampled and not 100% tested.

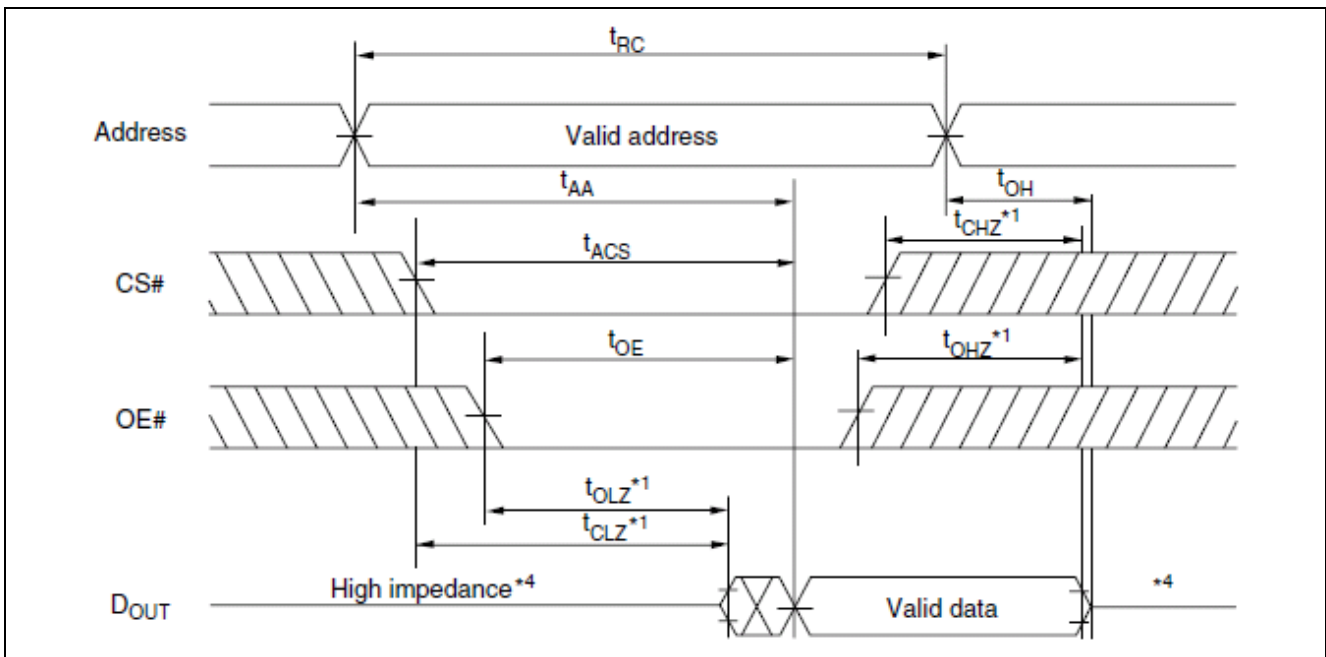
2. If the CS# or LB# or UB# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
3. WE# and/or CS# must be high during address transition time.
4. If CS#, OE#, LB# and UB# are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. t_{AS} is measured from the latest address transition to the latest of CS#, WE#, LB# or UB# going low.
6. t_{WR} is measured from the earliest of CS#, WE#, LB# or UB# going high to the first address transition.
7. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB# (t_{WP}). A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.
8. t_{CW} is measured from the later of CS# going low to the end of write.

Timing Waveforms

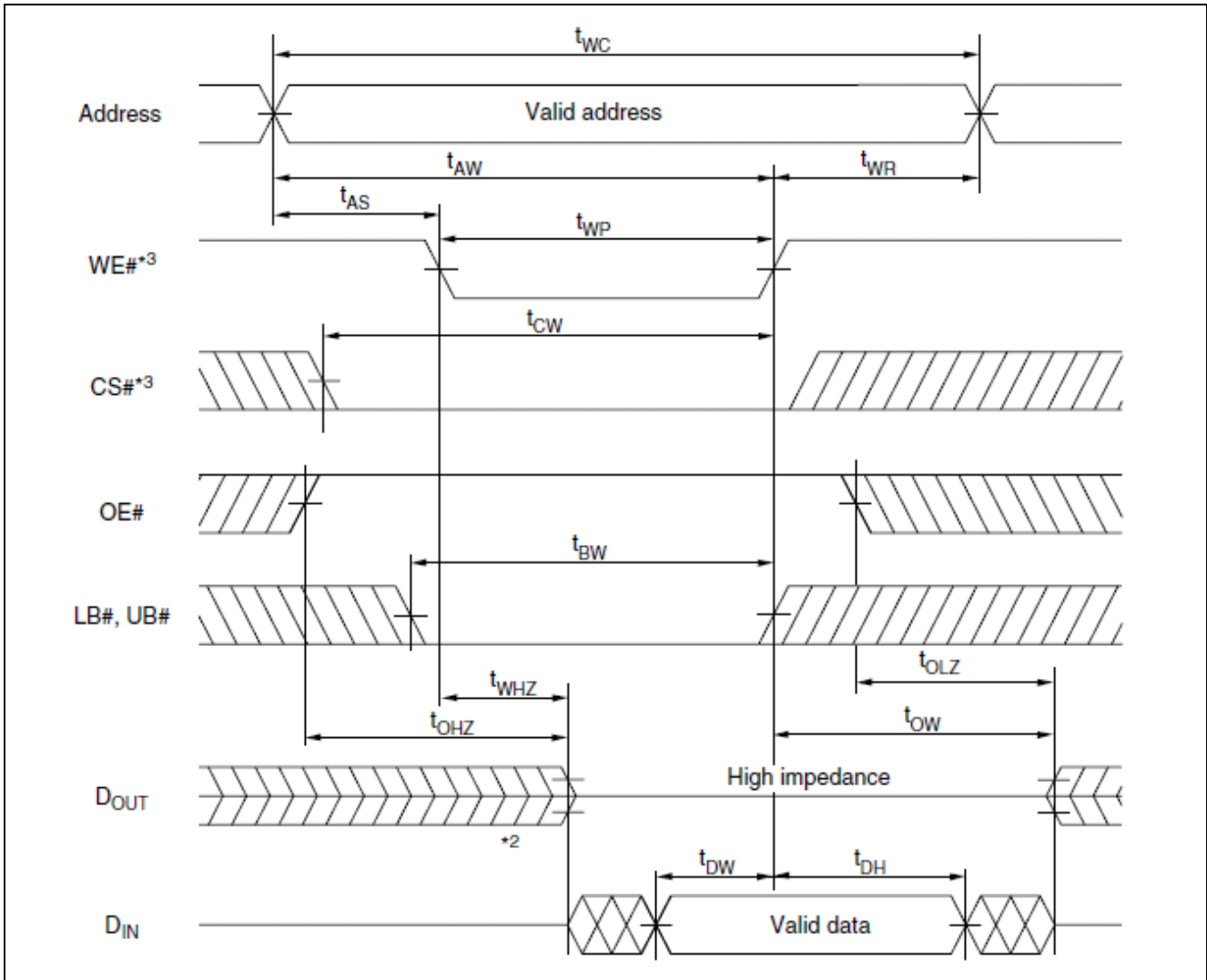
Read Timing Waveform (1) (WE# = V_{IH})



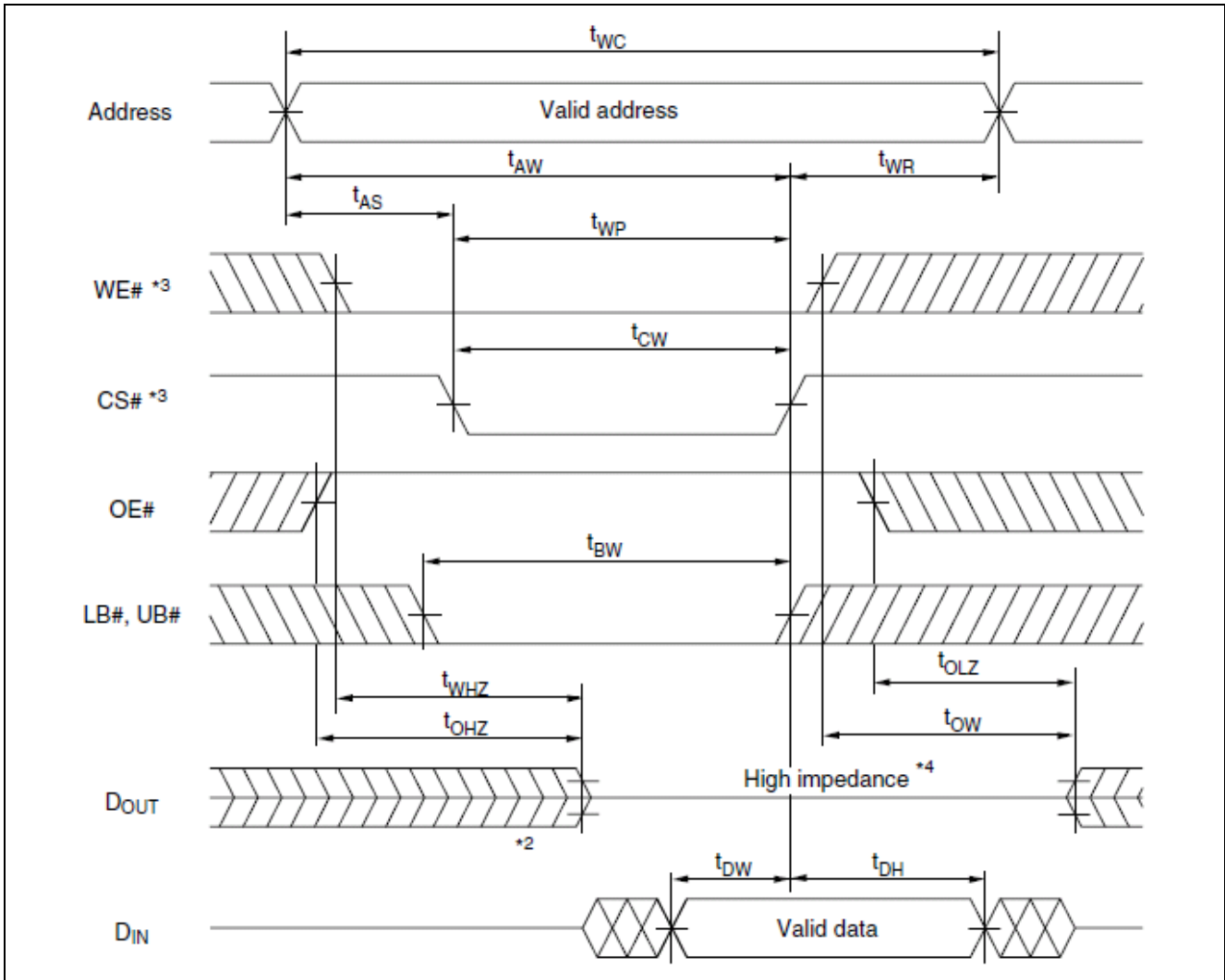
Read Timing Waveform (2) (WE# = V_{IH}, LB# = V_{IL}, UB# = V_{IL})



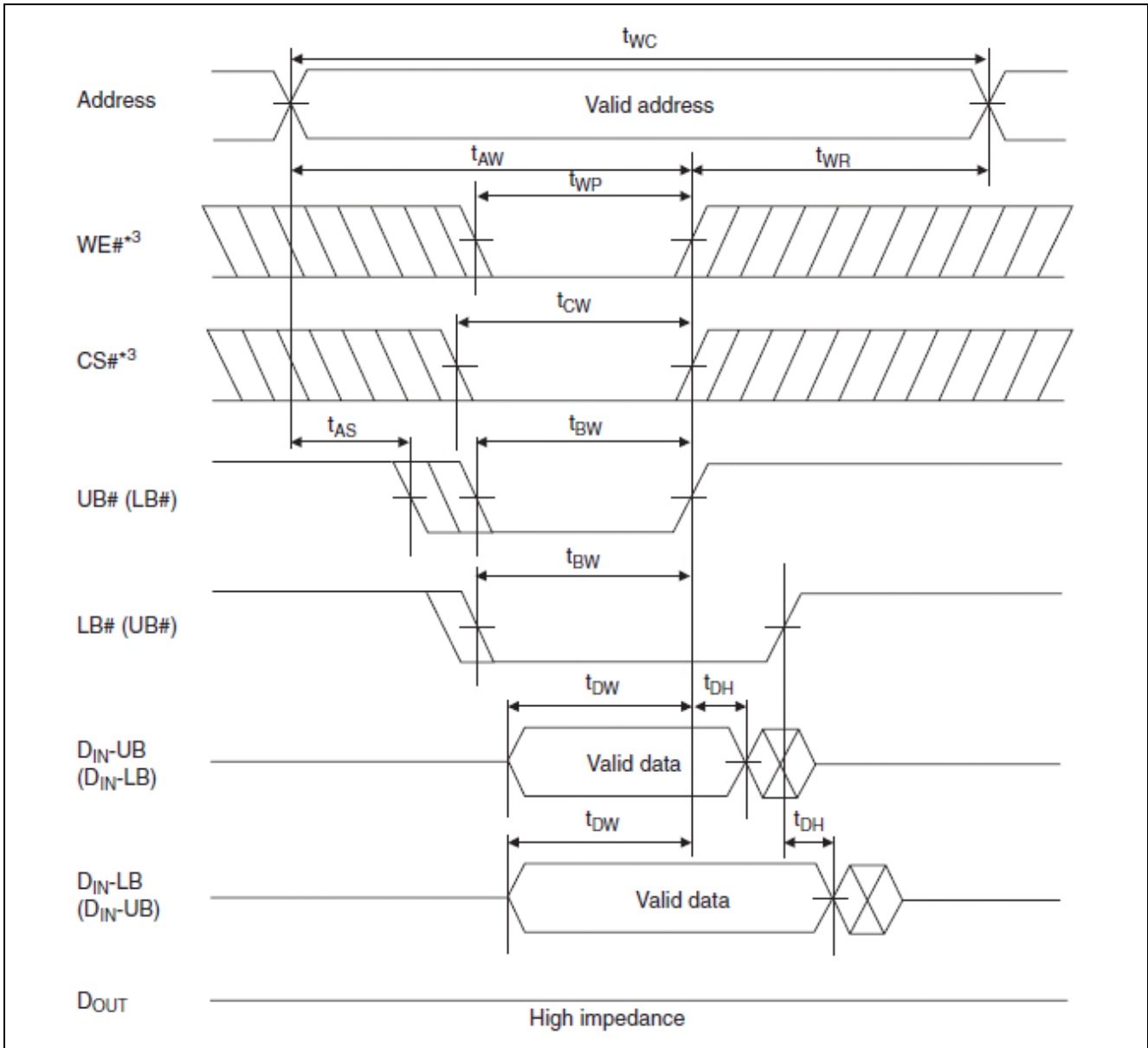
Write Timing Waveform (1) (WE# Controlled)



Write Timing Waveform (2) (CS# Controlled)



Write Timing Waveform (3) (LB#, UB# Controlled, OE# = V_{IH})



Revision History

| Rev. | Date | Description | |
|------|-----------|-------------|----------------------|
| | | Page | Summary |
| 1.00 | Nov.18.19 | - | First Edition issued |

All documents should contain the following section break and paragraph as the last item. The footers of this document refer to the paragraph in order to reference the last page of the document.

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