R2A20150NP/SA

8-bit I/O Expander for I²C BUS (Corresponds to Fast mode)

R03DS0012EJ0100
Rev.1.00
2011.09.05

Description

The R2A20150NP/SA is a CMOS 8-bit I/O expander, which has serial to parallel and parallel to serial data converting functions.

It can communicate with a microcontroller via few wiring thanks to the adoption of the 2-wire I²C BUS.

Maximum 8 ICs can be connected to a bus by using 3-chip select pins, so that it is possible to handle up to 64 bits data.

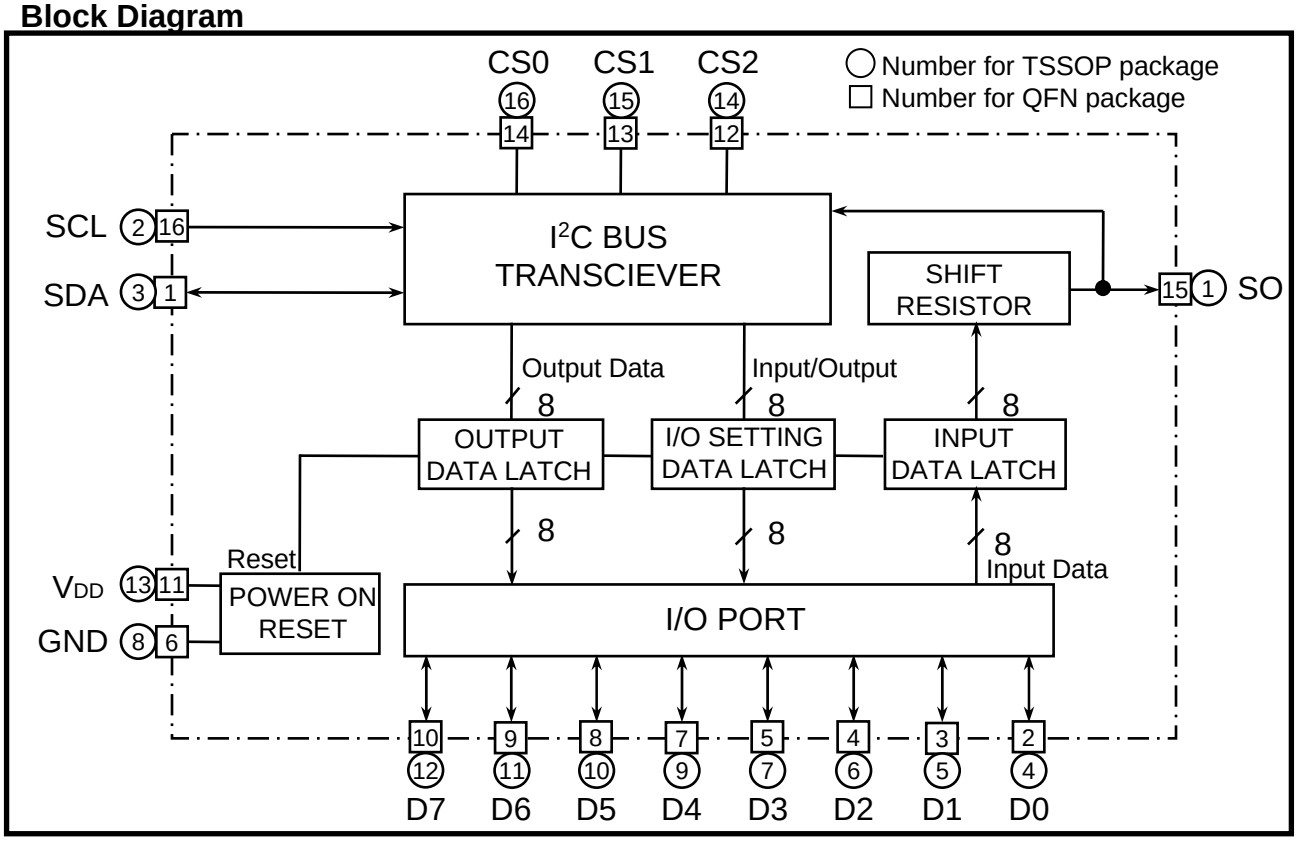
Features

- Simple 2-wire (SCL and SDA) communication with a microcontroller.
- 8-bit data conversion between serial and parallel by I²C BUS.
- Corresponds to Fast mode (400kHz) of I²C BUS specification.
- Possible to set input and output each bit separately.
- By using three chip select pins (CS0,CS1,CS2), R2A20150 can connect with the same BUS line to maximum 8 pieces.
- Very small package line-up QFN-16 and TSSOP-16.

Application

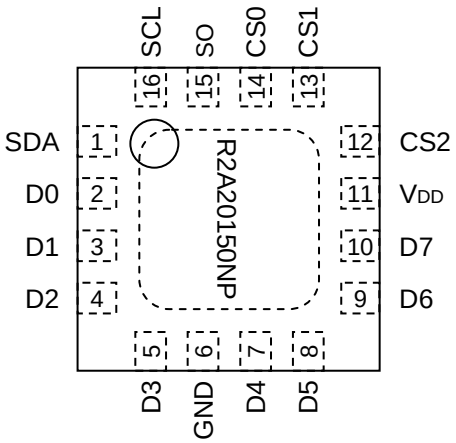
- I/O port expansion of Microcomputer.
- Data conversion from serial to parallel and from parallel to serial in peripheral of Microcomputer.

Block Diagram



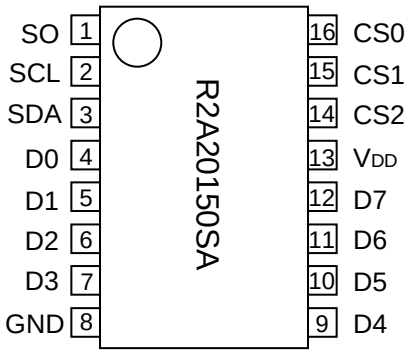
Pin Arrangement

R2A20150NP (Top view)



Package: PWQN0016KB-A [NP]

R2A20150SA (Top view)



Package: PTSP0016JB-A [SA]

EXPLANATION OF TERMINALS The pin No. of ( ) are for QFN package

Pin No.		Symbol	I/O	Function
TSSOP	QFN			
1	15	SO	Output	Serial data output terminal
2	16	SCL	Input	Serial clock input terminal
3	1	SDA	Input/Output	Serial data input/output terminal
4	2	D0	Input/Output	Parallel data input/output terminal (Initial state after power on is input mode.)
5	3	D1		
6	4	D2		
7	5	D3		
9	6	D4		
10	7	D5		
11	8	D6		
12	9	D7		
14	10	CS2	Input	Chip select data input terminal This IC accessed only when the lower 3bits data from Slave address coincide with the data of CS0 to CS2.
15	12	CS1		
16	13	CS0		
13	14	VDD	-	Power supply terminal
8	11	GND	-	GND terminal

Absolute Maximum Ratings

(Ta= 25 deg unless otherwise noted)

Symbol	Item	Conditions		Ratings	Unit
V_{DD}	Supply voltage			-0.3 to +6.5	V
V_I	Input voltage			-0.3 to V_{DD}+0.3 (<6.5)	V
V_O	Output voltage			-0.3 to V_{DD}+0.3 (<6.5)	V
I_{OH}	Output current “High”	D0 ~ D7		-5 to 0	mA
I_{OL}	Output current “Low” *1	D0 ~ D7	Continuous	0 to +4	mA
			Peak	0 to +30	mA
Pd	Power dissipation	Ta= +85deg		290(NP) / 150(SA)	mW
K theta	Thermal derating factor	Ta> +25deg		7.25(NP) / 3.75(SA)	mW/deg
Topr	Operating temperature range			-30 to +85	deg
Tstg	Storage temperature			-40 to +125	deg

*1 : The maximum ratings of Output current “Low” is 4mA when using continuously for each port, but peak current is 30mA (13% duty) when considering duty cycle including power off period.

Recommended Operating conditions

Symbol	Item	Conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		2.7	5.0	5.5	V
V_{IH}	Input high voltage		0.8V_{DD}	-	V_{DD}	V
V_{IL}	Input low voltage		0	-	0.2V_{DD}	V

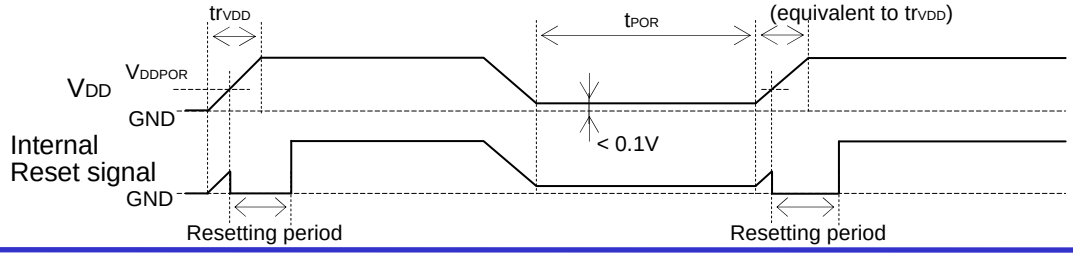
Electrical Characteristics

(V_{DD} = +5V +/-10%, GND=0V, Ta= -30 to +85deg unless otherwise noted)

Symbol	Item	Conditions	Limits			Unit
			Min	Typ	Max	
I_{DD}	Circuit current	V_{IH}=V_{DD}, V_{IL}=GND, f_{SCL}=400kHz	-	0.05	0.5	mA
		V_{IH}=V_{DD}, V_{IL}=GND, f_{SCL}=STOP	-	0.1	10	µA
I_{ILK}	Input leak current		-10	0	10	µA
V_{OL}	Output low voltage (SDA)	Isink=3mA	-	-	0.4	V
V_{IH}	Input high voltage		0.8V_{DD}	-	V_{DD}	V
V_{IL}	Input low voltage		0	-	0.2V_{DD}	V
Vhys	Hysteresis of Schmitt trigger input (SDA, SCL)		0.5	0.8	-	V
V_{OH}	Output high voltage (D0 ~ D7)	I_{OH}=-1mA, V_{DD}=5V	V_{DD} – 0.4	-	V_{DD}	V
		I_{OH}=-500µA, V_{DD}=3V	V_{DD} – 0.4	-	V_{DD}	
V_{OL}	Output low voltage (D0 ~ D7)	I_{OL}=5mA, V_{DD}=5V	0	-	0.4	V
		I_{OL}=2.5mA, V_{DD}=3V	0	-	0.4	
I_{OL}	Output current “Low” *2 (D0 ~ D7)	V_{OL}=0.4V, V_{DD}=5V	5	10	-	mA
		V_{OL}=0.4V, V_{DD}=3V	2.5	5	-	
		V_{OL}=1.0V, V_{DD}=5V	15	25	-	
		V_{OL}=1.0V, V_{DD}=3V	5	10	-	
tr_{VDD}	Supply voltage rise-up time *3	V_{DD}=0 to 2.7V	100	-	-	µs
V_{DDPOR}	Operating voltage of internal reset *3	V_{DD}=0 to 2.7V	-	1.5	1.9	V
t_{POR}	Time period of re-power on (Power supply OFF → ON) *3	V_{DD} < 0.1V	1	-	-	ms

*2 : Output low current should be set; average current of summary of D0 to D3 or D4 to D7 < 16mA.
Average current is calculate by below equation;
Average current = I_{OL} X duty duty : The period of flow I_{OL} (Include power off period)

*3 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (t_{POR}).

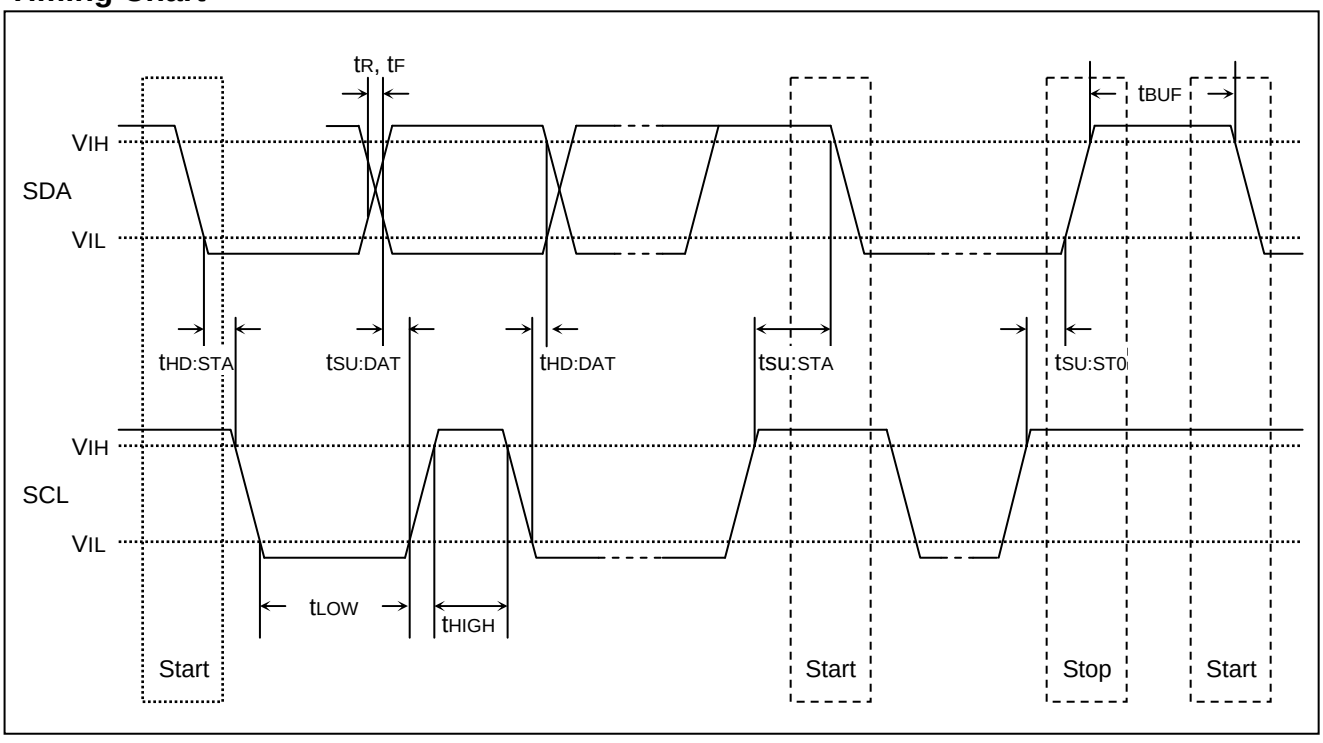


I²C BUS Characteristics

Item	Symbol	Normal mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Free time: the bus must be free before a new transmission can start	t_{BUF}	4.7	-	1.3	-	µs
Hold time START condition after this period, the first Clock pulse is generated	$t_{HD:STA}$	4.0	-	0.6	-	µs
Low period of the clock	t_{LOW}	4.7	-	1.3	-	µs
High period of the clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for START condition. Only relevant for a repeated START condition.	$t_{SU:STA}$	4.7	-	0.6	-	µs
Data Hold time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data Set-up time	$t_{SU:DAT}$	250	-	100	-	ns
Rise time of SDA and SCL signals	t_R	-	1000	-	300	ns
Fall time of SDA and SCL signals	t_F	-	300	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	0.6	-	µs
Capacitive load of bus line	C_b	-	400	-	400	pF

All of above value are corresponds to V_{IH}min and V_{IL}max.

Timing Chart



Functional Blocks

● I^2C BUS Interface

The I^2C BUS interface recognizes start/stop conditions, a slave address and a write/read mode selection by receiving SDA,SCL,CS0,CS1 and CS2 signals and then the latch pulse, dedicated to each data latch are generated.

● Data Latch

This IC has 3 types of data latch: the I/O setting data latch, the input data latch and the output data latch and each latch is controlled by the I^2C BUS interface.

• I/O setting data latch

These latches set input-state or output-state of each parallel data terminals (D0 to D7). They are set at the next byte after receiving the slave address byte in the write mode from the master.

In case this latch is set to high, the data is transferred from the I^2C BUS interface to the parallel data terminals. In the opposite transmission: from the parallel data terminals to the I^2C BUS, it is set to low.

• Output data latch

In the write mode, the data from the I^2C BUS to the parallel data terminals is latched.

When the master transmits output data after a setting in write mode, the output data is taken into the latch.

• Input data latch

In the read mode, the data of parallel data terminals is latched in the input data latches. The input data is taken into the latches from the parallel data terminals on every 8th negative edge of SCL clock.

The latched data is output to the master through the sift resistor. On the output terminal assigned by the I/O setting latch, the input data latch takes the state of the output terminal.

● Parallel Input/Output Port

In case I/O setting latch is set to low (the input mode), each parallel terminal becomes hi-impedance and is able to accept an input. In another case I/O setting latch is set to high (output mode), each parallel terminal output a data according to the state of the output data latch.

● Serial Output Port

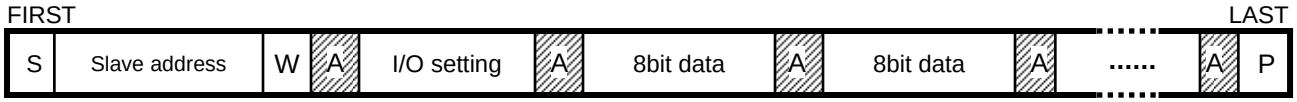
The parallel data from each parallel terminal are conversion to 8bit serial data and output to SO terminal. Without serial output mode, SO terminal goes to low output.

● Power on Reset

When the power is turned on, each latch is reset (initialize) and then the parallel data I/O terminals become hi-impedance (input mode).

Digital Data Format

1.Write mode: I²C BUS data input to parallel data output
(The data transmits continuously each 8bits after setting slave address and I/O.)



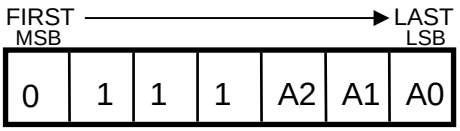
2.Read mode: Parallel data input to I²C BUS data output)
(The data transmits continuously each 8bits after setting slave address. When final data transmitted, do not return the acknowledge, then input the stop condition.)

Transmission from Master (MCU etc.) to Slave (R2A20150)

Transmission from Slave (R2A20150) to Master (MCU etc.)

- S: Start condition
  While SCL level is high, SDA line level should be changed from high to low.

- Slave address



Note: Lower three bits (A0, A1, A2) are a programmable address.
This IC is accessed only when the lower 3 bits data of slave address coincide with the data of CSO to CS2. (refer to the right table)

Chip select data

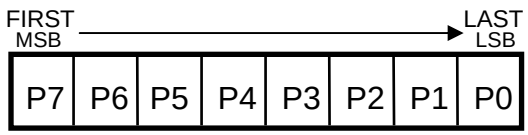
MSB		LSB			
A2	A1	A0	CS2	CS1	CS0
0	0	0	L	L	L
0	0	1	L	L	H
0	1	0	L	H	L
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	H	H	H

(L=Low,H=High)

- W: Write (SDA = Low), R: Read (SDA = High)

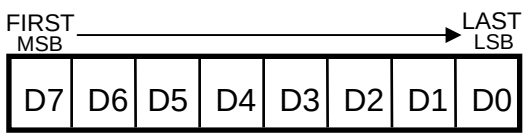
- A: Acknowledge bit
  (Slave side confirm the data receive, change to Low in the SDA line)
  *$\overline{A}$: IN a read mode; after final data transmitted, do not return acknowledge. Change to High.)

- I/O setting data (I/O setting of parallel data I/O terminals.)



Note: DATA INPUT from parallel data terminals = Low
DATA OUTPUT to parallel data terminals = High
Each bit data corresponds to the I/O state of the parallel data terminals.

- 8-bit data

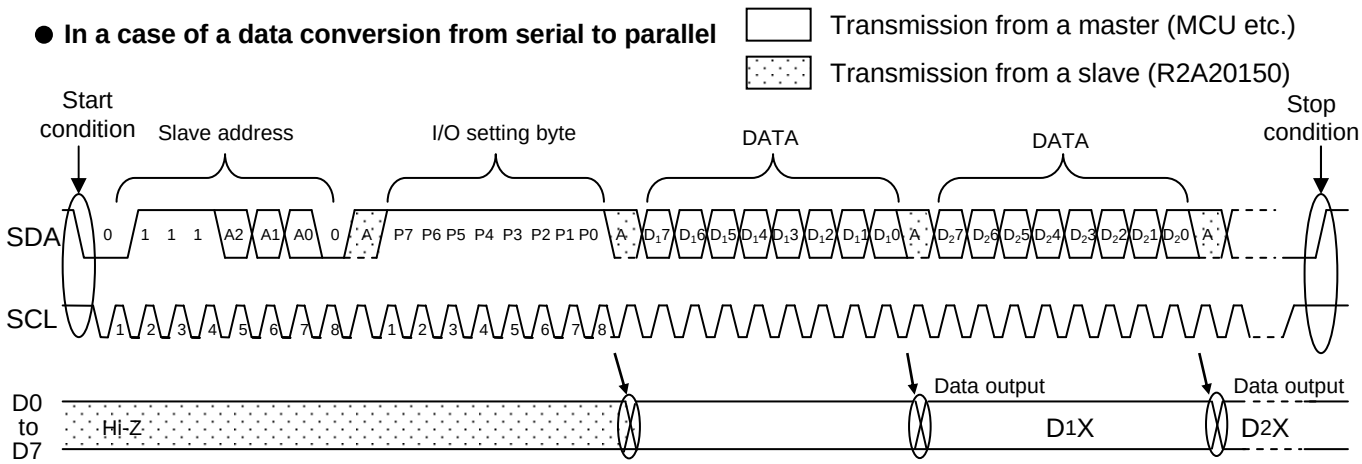


- P: Stop condition
  While SCL level is high, SDA level should be changed from low to high.

FUNCTIONAL DESCRIPTION

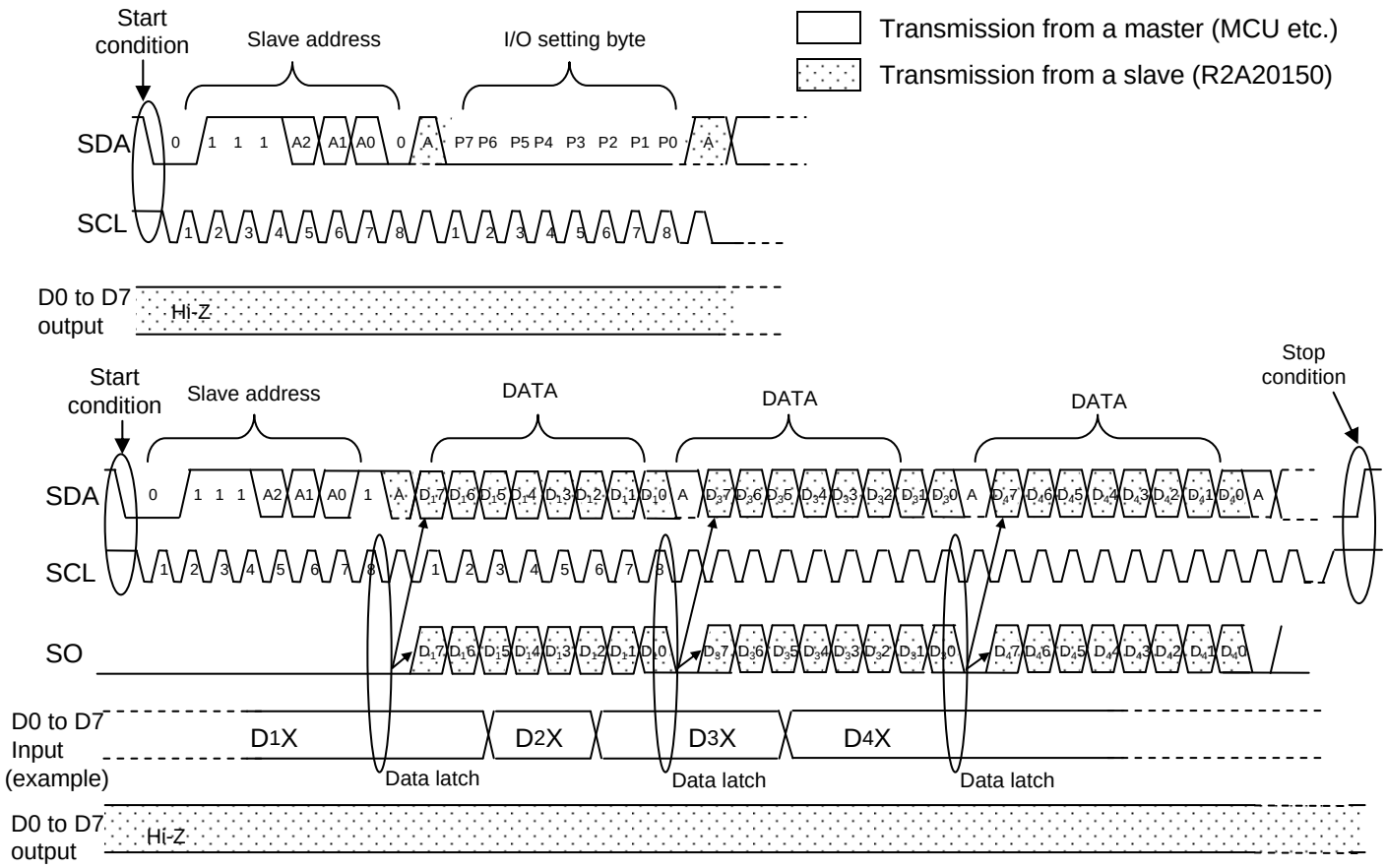
All parallel data I/O terminals are set to the input-state after power-on. In case any terminals need to be set to the output state, the corresponding terminals should be set during the write mode.
This setting is hold until a next setting.
In the write mode, 8 bits data can be transmitted from the I²C BUS interface to the parallel ports continually After the slave address and I/O setting.
In the read mode, 8 bits data can be transmitted from the parallel ports to the I2C BUS interface continually After the slave address setting. This 8 bits serial data is output from the SO terminal. SO terminal sets to “L” state without read mode.
In the case of a changing between the write- and read-mode, the data must be transmitted again from the Starting condition.

● **In a case of a data conversion from serial to parallel**



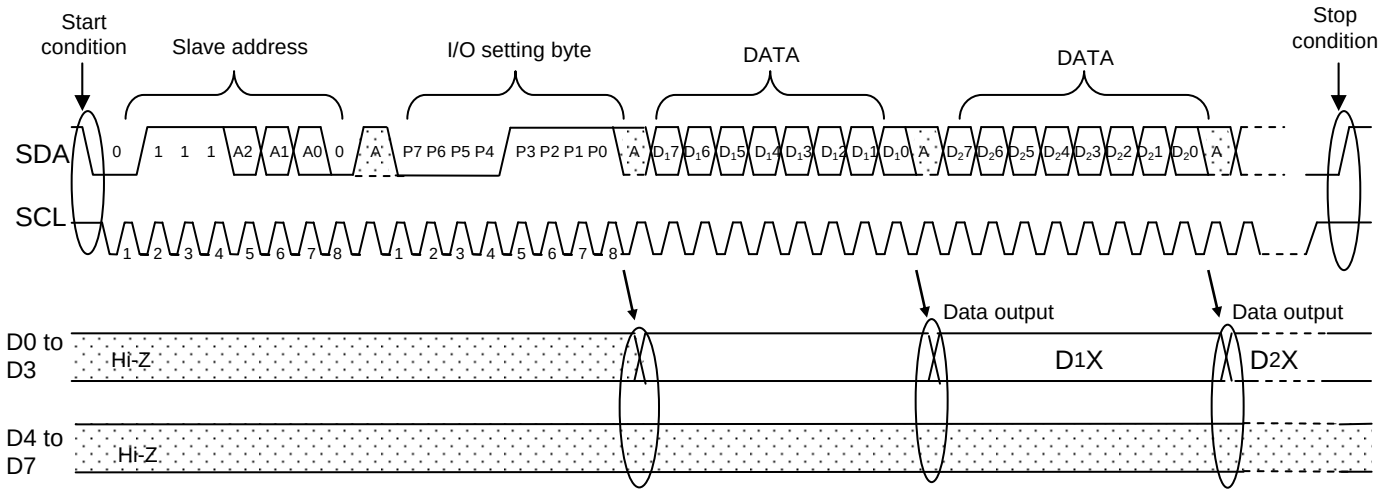
● **In a case of a data conversion from parallel to serial**

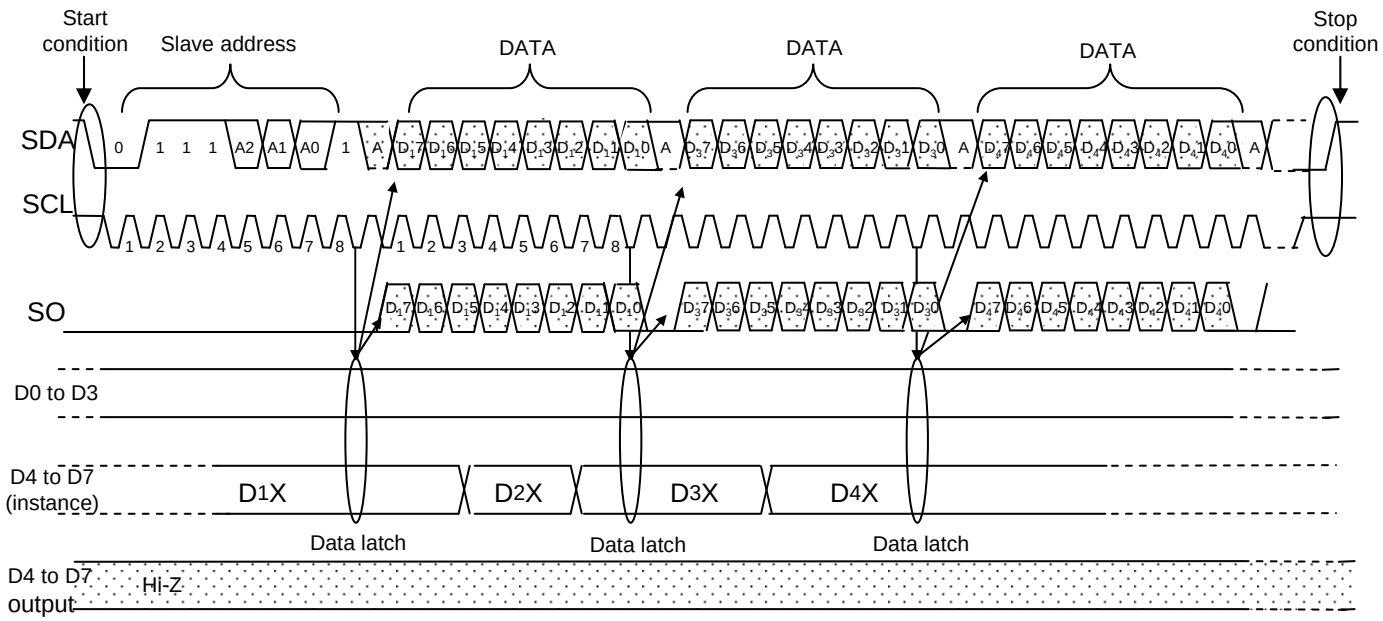
All I/O setting resistors are set to low (input) in the write mode, before a parallel data is read.
(All I/O setting resistors are set to the input mode after power-on.)



● **In case the I/O setting is different between each terminals.**

An example : the parallel port terminals of D0 to D3 and D4 to D7 are assigned as output and input terminals, respectively.





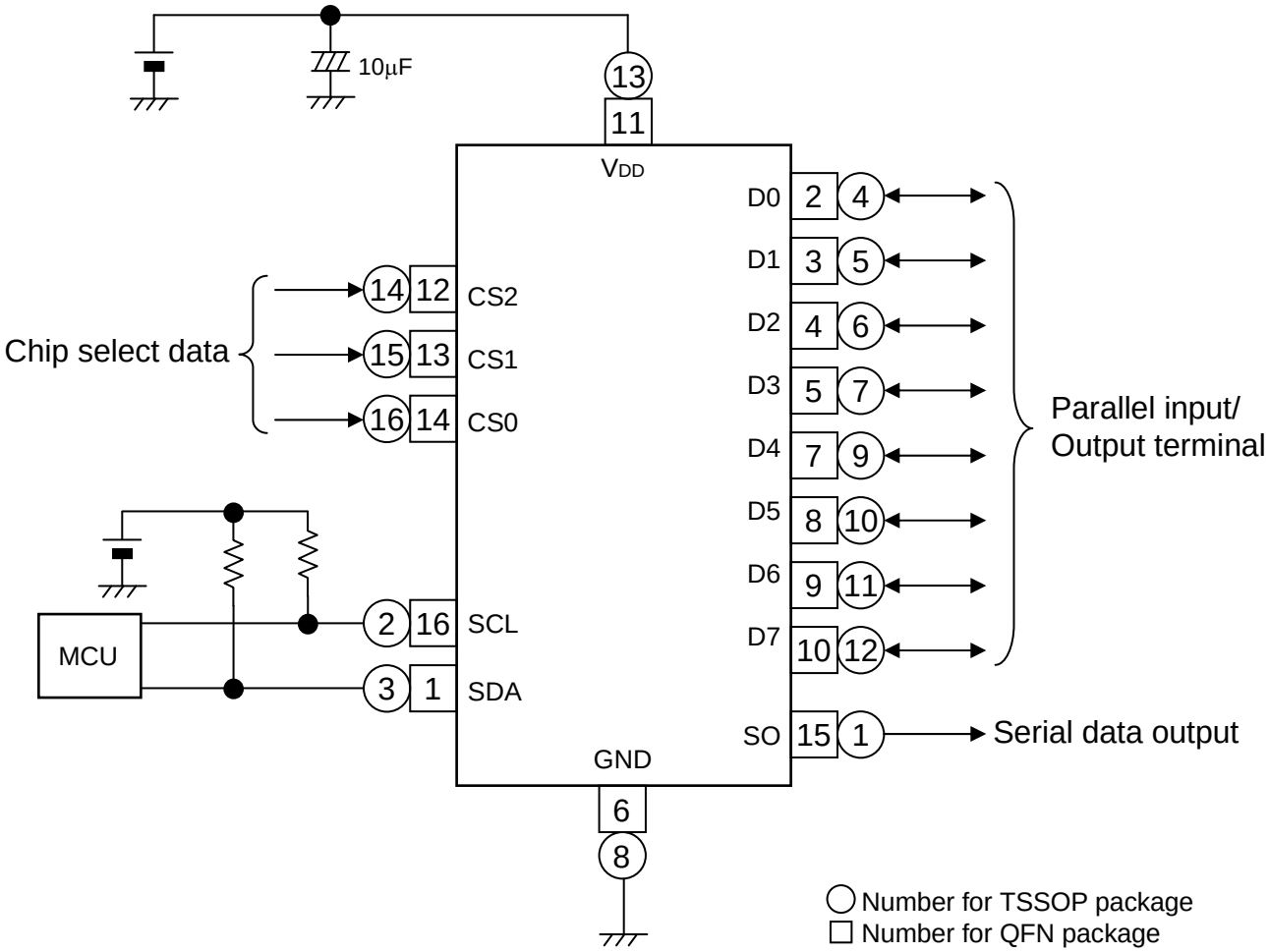
***** Write mode

The terminal assigned as an output provides the data written in the output data latch.
After power-on, all terminals are reset to the input-state. Then an initial data low of the output latch are output after the I/O setting has been done. Finally the assigned output are provided after the 8-bit data transmission.
Then terminal assigned as an input keeps the input condition (High-impedance) regardless of 8-bit data setting.

***** Read mode

The input data is taken into input latch on every 8th negative-going edge of the SCL clock through the terminal assigned as an input, and then the latched data is output via the SDA line.
The data of the output assigned terminal is also handled in the same procedures as above.

TYPICAL APPLICATION



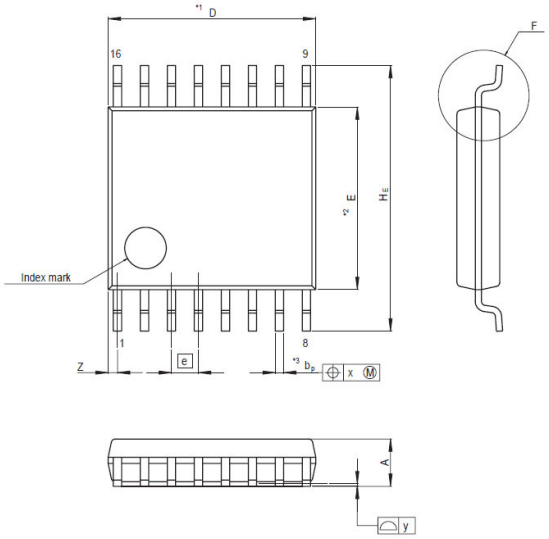
Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20150SA	TSSOP-16	PTSP0016JB-A	SA	Embossed Taping/2,000 pcs.
R2A20150NP	QFN-16	PWQN0016KB-A	NP	Embossed Taping/3,000 pcs.

Package outline

SA: PTSP0016JB-A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP16-4.4x5-0.65	PTSP0016JB-A	TTP-16DAV	0.05g

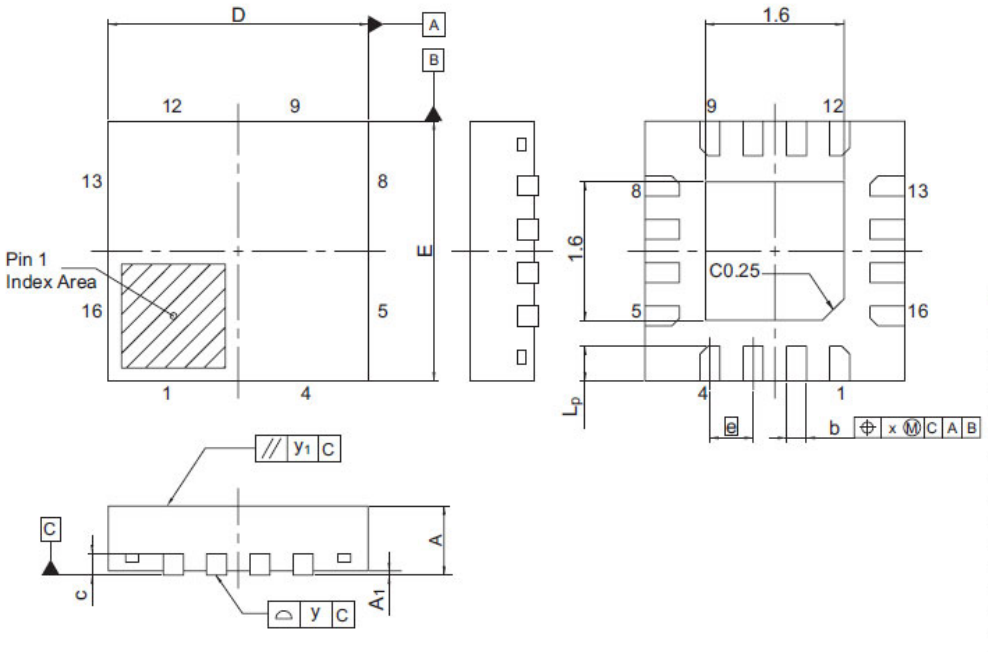


NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.0	5.3
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L_1	—	1.0	—

NP: PWQN0016KB-A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN16-3x3-0.50	PWQN0016KB-A	—	0.020g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	2.90	3.00	3.10
E	2.90	3.00	3.10
A_2	—	—	—
A	—	—	0.80
A_1	0	—	0.05
b	0.18	0.23	0.28
b_1	—	—	—
e	—	0.5	—
L_p	0.30	0.40	0.50
x	—	—	0.1
y	—	—	0.08
y_1	—	—	0.1
t	—	—	—
H_D	—	—	—
H_E	—	—	—
Z_D	—	—	—
Z_E	—	—	—
c	—	0.20	—
c_1	—	—	—

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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