Preliminary Datasheet

R2A25110KSP

Intelligent Power Device for IGBT Drive with Micro Isolator

1. Description

The R2A25110KSP device is an intelligent power device for IGBT gate-drive in the high voltage inverter application. The Micro Isolator with the coreless transformer structure is adopted for data transfer with high voltage isolation between the primary circuit (MCU side) and the secondary circuit (IGBT side). This device contains IGBT gate drive circuit, Miller clamp circuit, soft turn-off circuit as well as several types of protection circuits such as IGBT temperature detection. This device also supports driving parallel IGBTs.

1.1. Features

- On-chip Micro Isolator (isolated circuit)
  High voltage isolation: 2500V_{RMS}
  - High Common Mode Rejection (CMR): over 35kV/us
- High output gate drive circuit
  - Gate drive output resistance: 1.0 ohm max (IGBT parallel connection supported)
  - On-chip active Miller clamp function
  - On-chip soft turn-off function
- Various on-chip protection circuits
  - IGBT emitter current detection circuit: 2 channels
    Over current detection (threshold voltage: 0.25 V typ.), short circuit detection (threshold voltage: 0.5 V typ.)
    Over current detection function can be enabled/disabled (SEL pin)
  - IGBT temperature detection circuit: 2 channels
  - On-chip under voltage lockout circuit
    VCC1 (5 V system): 4.1 V typ.
    VCC2 (15 V system): 10 V typ.
  - On-chip over temperature protection circuit (200 degC)
  - FAULT feedback
    Adjustable FAULT hold time with the external capacitor
- Operating temperature: - 40 to 125 degC (junction temperature: 150 degC max)
- On-chip 5 V regulator

1.2. Applications

- Main inverters for EV/HEV in automotive applications
- Converters for EV/HEV in automotive applications
- Inverters and converters for industrial instruments, etc.

Note: The information contained in this document is the one that was obtained when the document was issued, and may be subject to change.

2. Block Diagram

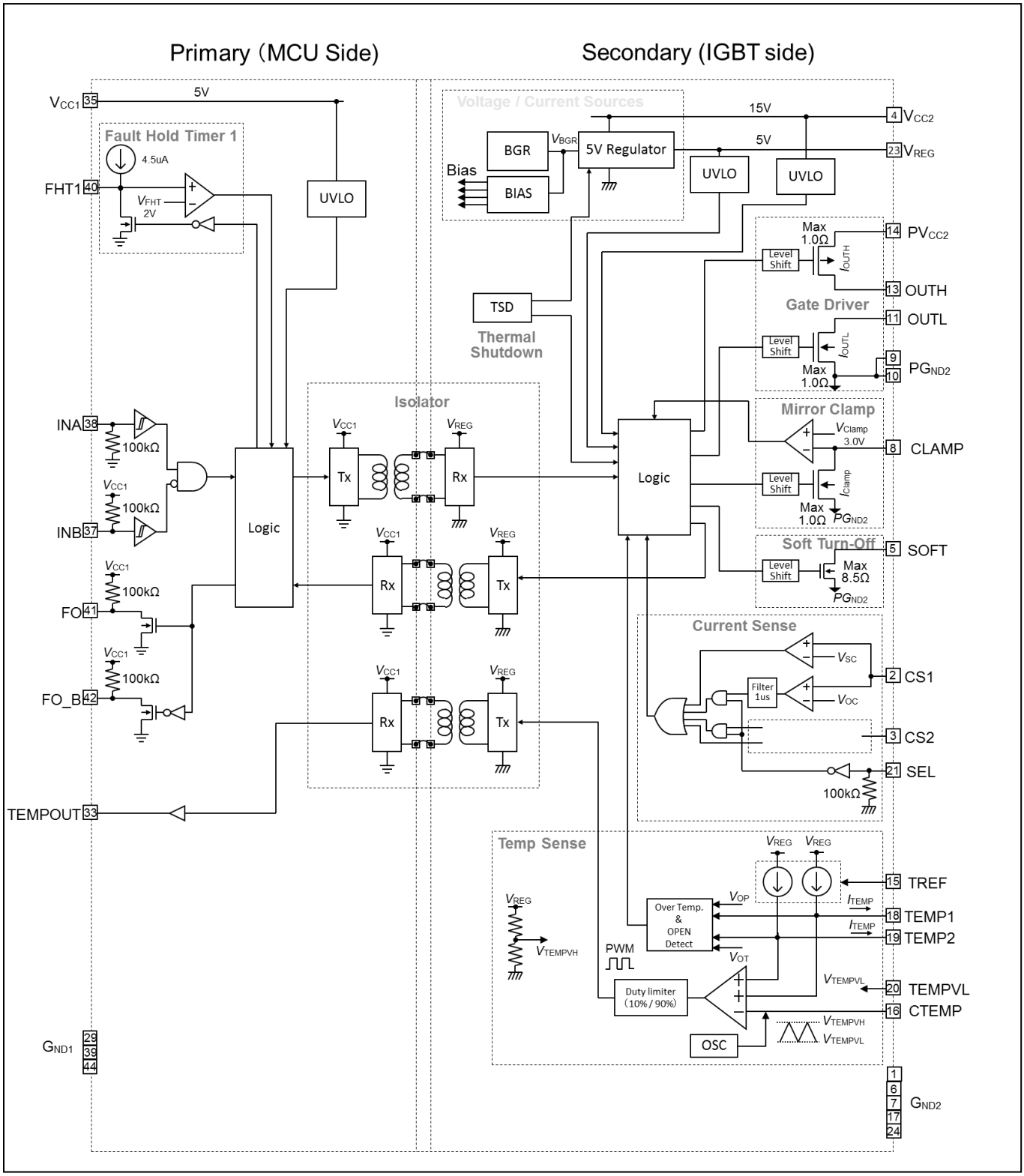


Figure 1: Block Diagram

3. Pin Arrangement

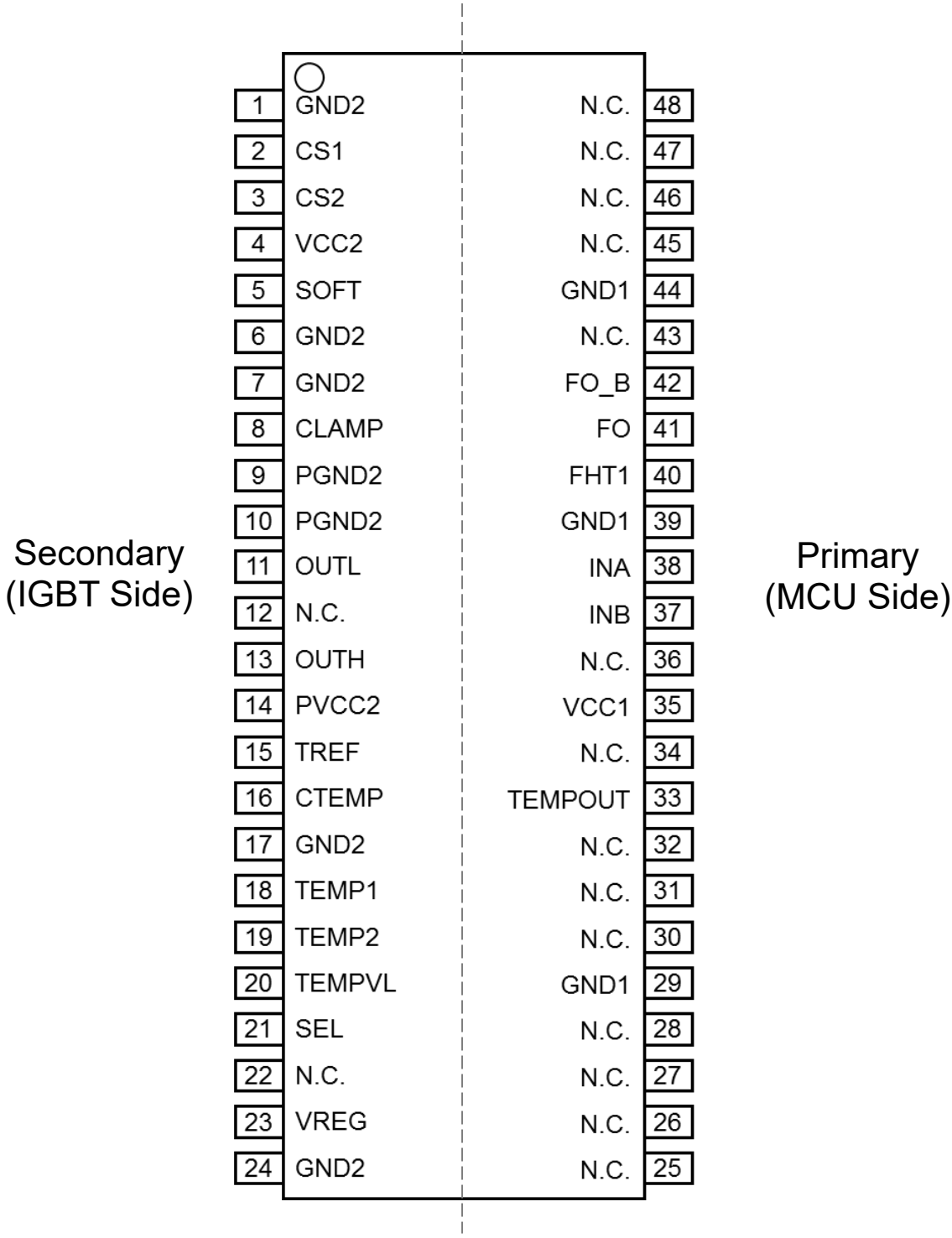


Figure 2: SSOP48 (Top View)

Table 1: Pin List (1/2)

PIN No.	PIN NAME	Reference pin	PU/PD	Functions
1	GND2	–	–	Secondary GND
2	CS1	GND2	–	Emitter current detection input (ch1)
3	CS2	GND2	–	Emitter current detection input (ch2)
4	VCC2	GND2	–	Secondary power supply input (15 V typ.)
5	SOFT	PGND2	–	Soft turn-off output
6	GND2	–	–	Secondary GND
7	GND2	–	–	Secondary GND
8	CLAMP	PGND2	–	Active Miller clamp output
9	PGND2	–	–	Secondary power GND
10	PGND2	–	–	Secondary power GND
11	OUTL	PGND2	–	Low side gate drive output
12	N.C.	–	–	Non Connection
13	OUTH	PGND2	–	High side gate drive output
14	PVCC2	PGND2	–	Secondary power supply input (15 V typ.)
15	TREF	GND2	–	Constant current setting pin connected to resistor for IGBT temp detection
16	CTEMP	GND2	–	IGBT temp detection period setting pin connected to capacitor
17	GND2	–	–	Secondary GND
18	TEMP1	GND2	–	IGBT temp detection input (ch1)
19	TEMP2	GND2	–	IGBT temp detection input (ch2)
20	TEMPVL	GND2	–	IGBT temp voltage detection threshold value input (lower limit)
21	SEL	GND2	PD	Selection of over current detection function (GND2: Enabled, VREG: Disabled)
22	N.C.	–	–	Non Connection
23	VREG	GND2	–	5 V regulator output
24	GND2	–	–	Secondary GND
25	N.C.	–	–	Non Connection
26	N.C.	–	–	Non Connection
27	N.C.	–	–	Non Connection
28	N.C.	–	–	Non Connection
29	GND1	–	–	Primary GND
30	N.C.	–	–	Non Connection
31	N.C.	–	–	Non Connection
32	N.C.	–	–	Non Connection
33	TEMPOUT	GND1	–	IGBT temp detection output
34	N.C.	–	–	Non Connection
35	VCC1	GND1	–	Primary power supply input (5 V typ.)
36	N.C.	–	–	Non Connection
37	INB	GND1	PU	Inverted gate drive input
38	INA	GND1	PD	Non-inverted gate drive input
39	GND1	–	–	Primary GND
40	FHT1	GND1	–	Fault hold time setting pin connected to capacitor
41	FO	GND1	PU	Non-inverted fault output (H level output at error)
42	FO_B	GND1	PU	Inverted fault output (L level output at error)

Remark: PD - Pull down resistor / PU- Pull up resistor

N.C. pins in open state is recommended.

Table 1: Pin List (2/2)

PIN No.	PIN NAME	Reference pin	PU/PD	Functions
43	N.C.	–	–	Non Connection
44	GND1	–	–	Primary GND
45	N.C.	–	–	Non Connection
46	N.C.	–	–	Non Connection
47	N.C.	–	–	Non Connection
48	N.C.	–	–	Non Connection

Remark: PD - Pull down resistor / PU- Pull up resistor

N.C. pins in open state is recommended.

4. Functional Description

4.1 Power Supply

The primary circuit has the power supply pin (VCC1) which supplies 5 V power reference to GND1.

The secondary circuit has two types of power supply pins VCC2 and PVCC2, and two types of GND pins GND2 and PGND2. VCC2 supplies 15 V power reference to GND2 to the control circuit of the secondary side, and PVCC2 supplies 15 V power reference to PGND2 to the gate drive circuit. The IGBT gate voltage is applied from PVCC2 at the ON state and from PGND2 at the OFF state. VCC2 and PVCC2 should be externally short-circuited and GND2 and PGND2 should also be externally short-circuited.

The IC incorporates a 5-V output regulator, and outputs 5 V from the VREG pin. This regulator is capable of supplying a maximum of 5-mA current to the external circuits, thus being useful for setting the IGBT temperature detection circuit and other circuits. Even when the 5-V power is not necessary for external circuits, the 0.022-uF capacitor should be connected to the VREG pin to stabilize the internal voltage.

4.2 Inverted input/Non-inverted input

The IGBT gate can be turned on or off by either non-inverted logic (active high) input or inverted logic (active low) input. The IGBT gate is turned on only when the INA= high (H) and INB= low (L) (refer to table 2).

When the non-inverted logic is used, the input signal should be applied to the INA pin with the INB pin fixed to the low level.

When the inverted logic is used, the input signal should be applied to the INB pin with the INA pin fixed to the high level.

The INA and INB pins are internally pulled down and pulled up, respectively. Therefore, the IGBT is turned off when one of the INA and INB pins are open.

4.3 Gate Driver

The gate driver charges or discharges the IGBT gate pins. Figure 3 shows a block diagram of the circuit.

To turn on the IGBT, the OUTH pin is short-circuited to the PVCC2 pin via a 1.0 Ohm or smaller transistor; and the OUTL pin is driven to the high-impedance state.

To turn off the IGBT, the OUTL pin is short-circuited to the PGND2 pin via a 1.0 Ohm or smaller transistor; and the OUTH pin is driven to the high-impedance state.

Since the high-side gate drive output pin OUTH and the low-side gate drive output pin OUTL are independent of each other, the slew rates of the rise and fall of the gate voltage can be separately adjusted using the external resistors (RGH and RGL). The OUTH and OUTL pins should be provided with individual gate resistors and connected to the IGBT. The external resistor values (RGH and RGL) should be determined so that the peak current does not exceed the absolute maximum ratings (IOUTH and IOUTL) while the IGBT is being charged or discharged.

Table 2: I/O Truth Table

INA	INB	OUTH	OUTL	IGBT State
L	X	Hi-Z	L	OFF
X	H	Hi-Z	L	OFF
H	L	H	Hi-Z	ON

4.4 Active Miller Clamp

The active Miller clamp is the feature to prevent the self-turn-on of the IGBT due to the coupling capacitance between the IGBT gate and collector. Figure 3 shows a block diagram of the circuit.

The CLAMP pin also serves as the input pin to detect the IGBT gate voltage. If the CLAMP pin voltage falls below V_{CLAMP} (3.0 V typ.) while the input signal to turn off the IGBT is applied to the INA or INB pin, the IGBT gate is short-circuited to the PGND2 pin with 1.0 Ohm or lower.

With the CLAMP pin, the gate can be connected to the PGND2 pin with the lower impedance than the OUTL pin to which the gate resistor (R_{GL}) is connected. Therefore, self-turn-on of the IGBT can be prevented more effectively, compared to the case in which only the OUTL pin is used to ground the gate.

The active Miller clamp not only works at normal turn-off operation of the IGBT as shown in the timing chart in figure 12 but also works at soft turn-off operation as shown in figures 13 to 17.

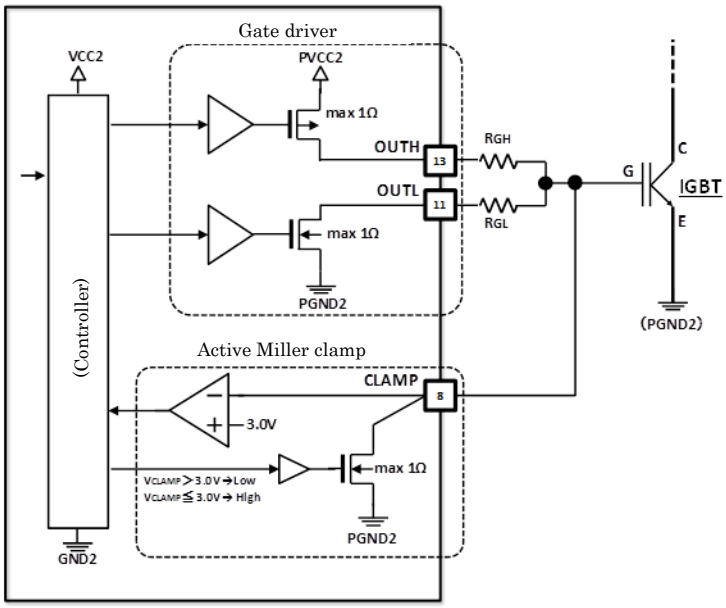


Figure 3: Gate Driver and Active Miller Clamp Circuit

4.5 Soft Turn-off

The soft turn-off is the feature to lower the gate voltage of the IGBT gradually and turn it off when any of the following abnormal states is detected on the secondary circuit: low voltage, over current, short circuit, over temperature (IGBT and IC), TEMP1 or TEMP2 open, and timeout (communication error). Figure 4 shows a block diagram of the soft turn-off circuit.

If a fault such as over current occurs and the IGBT is turned off immediately, the IGBT may be destroyed due to the excessive voltage applied between the collector and emitter of the IGBT. To prevent this, the IGBT gate is discharged slowly using the soft turn-off pin instead of using a high current gate driver or active Miller clamp. The turn-off time can be adjusted by the resistor (R_{SOFT}) connected between the SOFT pin and the IGBT gate pin.

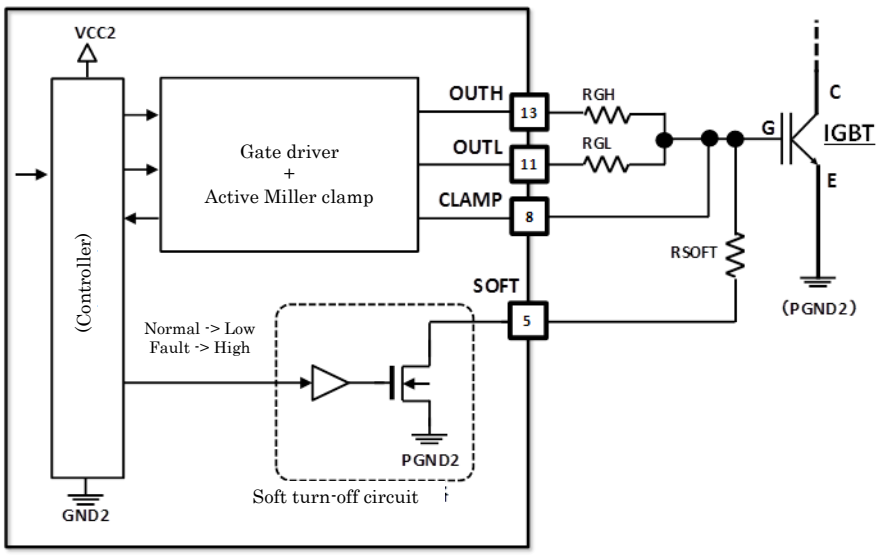


Figure 4: Soft Turn-off Circuit

4.6 Abnormal State Detection

This product can detect various abnormal states (faults) and externally output the associated fault signals. The following types of abnormal states can be detected:

1. IGBT over current and short circuit
2. IGBT over temperature and temperature sense diode open
3. Low voltage (UVLO)
4. Timeout
5. Over temperature of the product (TSD)

Sections 4.6.1 to 4.6.6 describe the above functions.

4.6.1 IGBT Over Current and Load Short Circuit Detection

This feature turns off the output from the gate driver if the over current or short-circuit current in the IGBT is detected. Figure 5 shows a block diagram of the circuit. Since two CS pins (CS1 and CS2) are provided, it is possible to separately detect the emitter current of the two IGBTs connected in parallel.
By applying the pin voltage of the shunt resistor connected to the IGBT emitter pin to the CS1 or CS2 pin, it is possible to detect whether the IGBT emitter is in the over current state or load short circuit state. The over current detection threshold can be set through the shunt resistor value.
The IGBT is soft turned-off if the voltage applied to the CS1 or CS2 pin rises beyond the threshold voltage* when the IGBT is in the on-state. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

*Over current detection voltage (Voc): 0.25 V typ.; filtering time 1 us typ.
* Short circuit current detection voltage (Vsc): 0.5 V typ.

The over current detection function is enabled when the SEL pin is open or connected to the GND2 pin; to disable the function, connect the SEL pin to the VREG pin (5 V typ.).

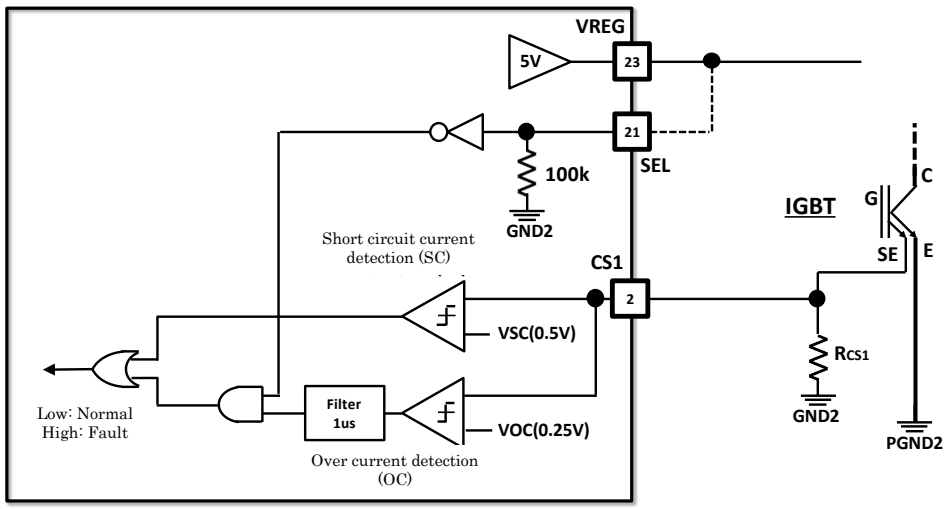


Figure 5: Over Current and Short Circuit Current Detection Circuit

4.6.2 IGBT Temperature Detection

Figure 6 shows the IGBT temperature detection circuit. This circuit outputs the constant current ($I_{TEMP} = 4/R_{TREF}$) from the TEMP pin to the temperature sense diode incorporated in the IGBT. The forward voltage of the temperature sense diode (IGBT chip temperature voltage) is input to the IGBT temperature detection circuit via the TEMP pin, converted to the PWM signal having the duty cycle proportional to the voltage, and finally output from the TEMPOUT pin via the Micro Isolator.

Since two TEMP pins (TEMP1 and TEMP2) are provided, it is possible to separately monitor the temperature of the two IGBTs connected in parallel. In this case, the lower TEMP pin voltage (the higher IGBT chip temperature) of the two is selected and output.

When the temperature of only one IGBT is to be monitored, connect the TEMP1 and TEMP2 pins in parallel. In this case, the sum of the TEMP1 and TEMP2 pin current flows in the IGBT temperature sense diode connected to the TEMP pins. Therefore, appropriately adjust the current value using the external R_{TREF}.

The CTEMP pin is used to set the frequency of the PWM signal output from the TEMPOUT pin. Connect the capacitor Ctemp to the CTEMP pin. The frequency of the PWM signal $f_{TEMPOUT}$ can be

determined by the equation shown in figure 7.

Figure 8 shows the relationship between the temperature sense voltage input to the TEMP pin and the duty cycle of the PWM signal output from the TEMPOUT pin. Based on the VL and VH determined by the equation below, the duty cycle linearly changes from 10% to 90% when the TEMP pin voltage is in a range from VL to VH. When the TEMP pin voltage is lower than VL, the duty cycle is limited to 10% and when the TEMP pin voltage is higher than VH, the duty cycle is limited to 10%.

$V_L = 0.1 \times V_{TEMPVH} + 0.9 \times V_{TEMPVL}$

$V_H = 0.9 \times V_{TEMPVH} + 0.1 \times V_{TEMPVL}$

(V_{TEMPVH} = 3.8 V; V_{TEMPVL} is set using the TEMPVL pin.)

The TEMPOUT pin output is fixed to the low level (GND1) if the voltage for under-voltage lock out (VCC1, VCC2) is detected.

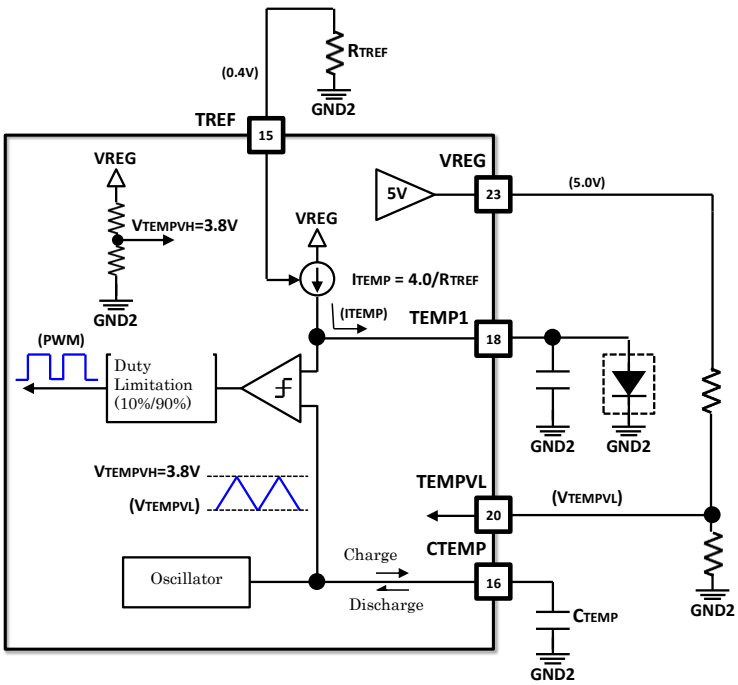


Figure 6: IGBT Temperature Detection Circuit

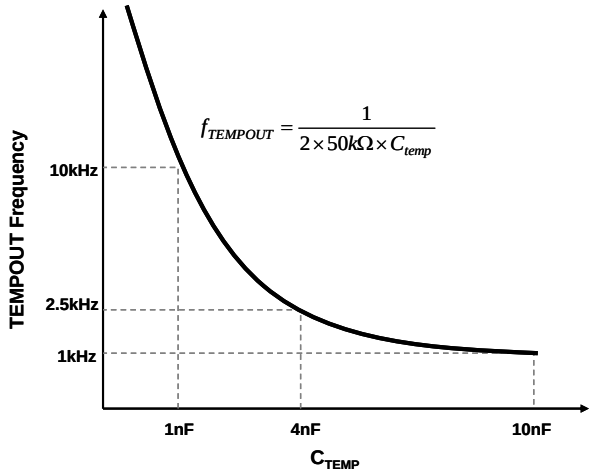


Figure 7: CTEMP-TEMPOUT Frequency

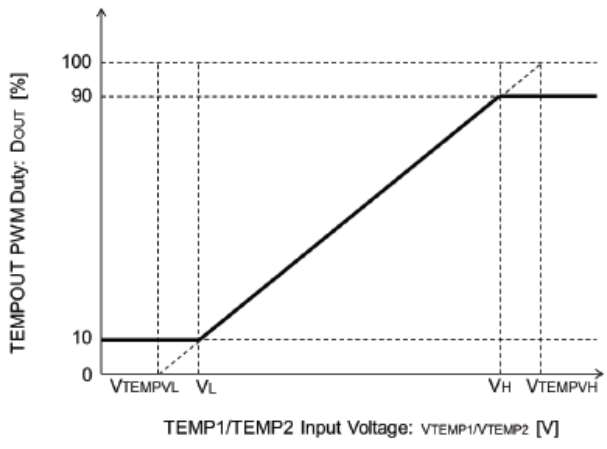


Figure 8: Relation between TEMP1 and TEMP2 Voltages and PWM Output Duty Cycle

4.6.3 IGBT Over Temperature Detection and Detection of Temperature Sense Diode Open

This feature turns off the IGBT if over temperature of the IGBT is detected. This feature is included in

the IGBT temperature detection circuit shown in figure 6.

If the TEMP1 or TEMP2 pin voltage falls below the over temperature detection threshold (V_{OT} = V_{TEMPVL} - 0.1 V typ.), the IGBT is soft turned off. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

In addition, if the TEMP1 or TEMP2 pin voltage rises beyond the open detection threshold (V_{OP} = 4.25 V typ.), the temperature sense diode is determined to be open. At this time, the IGBT is soft turned off and the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

4.6.4 Under Voltage Lock Out (UVLO) Circuit

This feature turns off the IGBT to prevent the damage on the IGBT due to malfunctioning of the IC when the supply voltage goes low.

The primary circuit is equipped with a UVLO that detects a voltage drop of VCC1, and the UVLO turns off the IGBT (this is a normal turn-off operation different from a soft turn-off) when the VCC1 voltage drops below 4.1 V. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

The secondary circuit is equipped with a UVLO that detects the voltage drop of VCC2 and a UVLO that detects the voltage drop of VREG (output from 5 V regulator). The IGBT is soft turned off if the VCC2 voltage drops below 10 V or the VREG voltage drops below 4.1 V. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

4.6.5 Timeout Detection

The timeout detection is a feature that outputs a fault status when the data transfer via Micro Isolator is not correctly performed.

For example, a timeout is detected at the secondary circuit when a signal transferred from the primary circuit to the secondary circuit via Micro Isolator is not detected in a certain period of time. The IGBT is soft turned off if a timeout is detected at the secondary circuit. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

Also, a timeout is detected at the primary circuit when a signal transferred from the secondary circuit to the primary circuit via Micro Isolator is not detected in a certain period of time. When a timeout is detected at the primary circuit, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit. The IGBT is not forcibly turned off in this condition.

4.6.6 Internal Over Temperature Detection (TSD)

This feature turns off the IGBT to prevent the damage on the IGBT due to malfunctioning of the IC when an extraordinary over heat (200 degC) is detected in the IC (thermal shut down: TSD). The operation is resumed when the IC temperature is decreased by the TSD hysteresis temperature (30 degC).

Temperature sense diodes are placed at the three positions that tend to be heated in the IC (near the OUTH, OUTL and CLAMP pins). The IGBT is soft turned off if the temperature of the driver transistor in the IC exceeds a threshold value due to the over load or the increased ambient temperature. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

In addition, another temperature sense diode is placed near the VREG pin. Output from the 5 V regulator is stopped when the temperature of the 5 V regulator exceeds a threshold value due to the over load on the VREG pin (5 V output) or the increased ambient temperature. A temperature sense signal from the 5 V regulator does not directly soft turn off the IGBT or output a fault signal to the primary circuit. However, when the regulator stops and the VREG voltage drops to 4.1 V or less, the under voltage lock out circuit starts operation and soft turns off the IGBT. At this time, the high level is output to the FO pin and the low level is output to the FO_B pin of the primary circuit.

4.7 Fault Signal Output Hold

This feature holds a fault signal output in a certain period of time when any of the following abnormal states is detected on the secondary circuit: under voltage, over current/short circuit, over temperature (IGBT over temperature, IC internal over temperature), TEMP1 and TEMP2 pin open, or timeout. Figure 9 is a fault signal output circuit. Figure 10 is a fault signal output hold time setting circuit.

While a fault signal output is held, the high level and the low level are output from the non-inverted fault output pin (FO) and the inverted fault output pin (FO_B) on the primary circuit, respectively, and the IGBT is forcibly turned off. The IGBT cannot be turned on again until the end of the fault signal output hold time.

The time for which a fault signal output is held can be set by the capacitor C_{FHT1} connected to the FHT1

pin. Table 3 shows the relationship between the hold time of a fault signal output on the primary circuit (MCU side) and the hold time of a soft turn-off output on the secondary circuit (IGBT side).

Table 11 shows the relationship between the capacitance of C_{FHT1} and the fault signal hold time t_{FHT}.

In addition, since the secondary circuit includes a 100 us timer, the fault signal output hold time t_{FHT} is 100 us when the value of C_{FHT1} is smaller than 100 us. Refer to table 4 for the conditions needed to reset a fault signal output after the detection of an abnormal state.

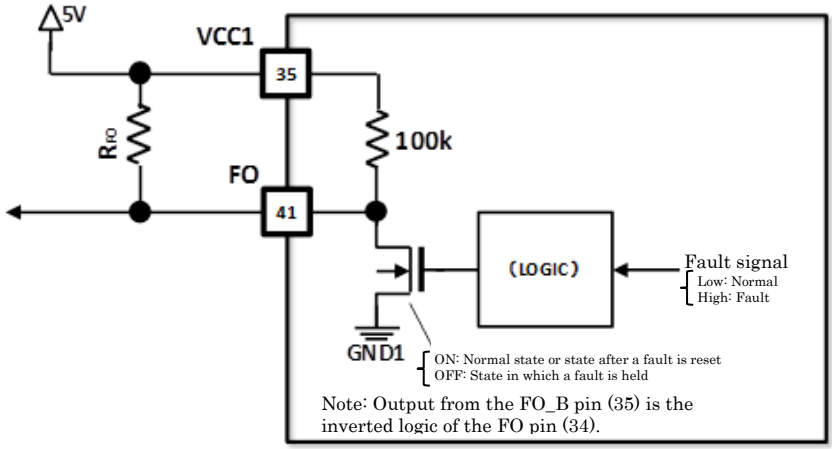


Figure 9: Fault Signal Output Circuit

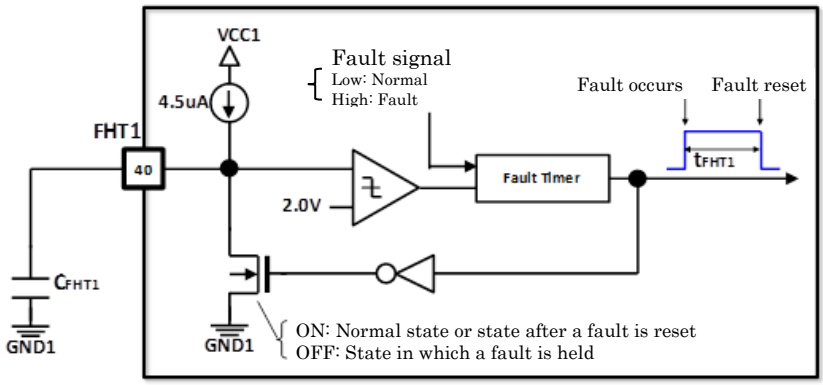


Figure 10: Fault Signal Output Hold Time Setting Circuit

Table 3: Fault Signal Output Hold Time (t_{FHT})

	Hold time for fault signal output and IGBT soft turn-off	
	Without CFHT1	With CFHT1
MCU-side fault signal output hold time (FO & FO_B)	100us	Greater value of tFHT1 or 100 us
IGBT-side soft turn-off hold time	100us	100us

Values are typical

Note: t_{FHT1} is fixed to 100 us when $t_{FHT1} \leqq 100$us.

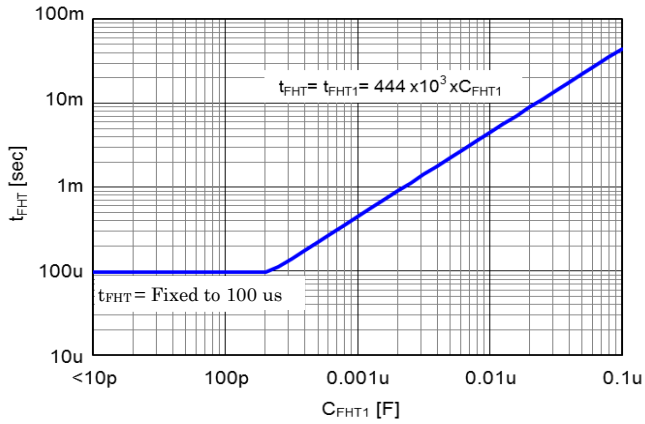


Figure 11: Relationship between Capacitor Value Connected to FHT1 Pin and Fault Signal Output Hold Time

Table 4: Abnormal State Detecting Conditions and Fault Signal Output Hold Resetting Conditions

Out Pins	Fault “SET” conditions	Fault “RESET” conditions
FO FO_B	At least one of the following conditions occurs • Over Current: CS1/2 > 0.25V (When IGBT=ON) • Short Circuit: CS1/2 > 0.5V (When IGBT=ON) • TEMP1/2 < V_{TEMPVL}-0.1V • TEMP1/2 > 4.25V • VCC2 < 10V • VREG < 4.1V • Driver temperature > 200°C • No signal from MCU-side to IGBT-side • No signal from IGBT-side to MCU-side • VCC1 < 4.1V	All the following conditions are satisfied • All the fault “SET” conditions cleared • 100us (typ.) elapsed since fault occurred • t_{FHT1} elapsed since fault occurred • INA=L or INB=H • Signal from IGBT-side detected

Note: All of the values in the table are typical.

Table 5 shows a list of abnormal states and the operations when those abnormal states are detected. If an abnormal state detection signal is instantaneously kept shorter than the filtering time, it is ignored as a noise.

Table 5: List of Abnormal States (When SEL Pin Input Level is Low (= GND2))

		Normal Condition	IGBT-Side Fault								MCU-Side Fault	
			Short Circuit	Over Current Note)	IGBT Over Temp.	TEMP1/2 Open	VCC2 UVLO	VREG UVLO	Timeout	TSD	VCC1 UVLO	Timeout
Input conditions	Monitor Pin	-	CS1/2		TEMP1/2		VCC2	VREG	Internal	Internal	VCC1	Internal
	Fault Criteria	-	> 0.5V	> 0.25V	< V_{TEMPVL}-0.1	> 4.25	< 10V	< 4.1V	No Signal	>200°C	< 4.1V	No Signal
	Filter Time	-	None	1us	10us	10us	25us	2us	20us	2us	2us	20us
Outputs	FO MCU-Side Output	**L**	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**H**	**H**
	FO_B MCU-Side Output	**H**	**L**	**L**	**L**	**L**	**L**	**L**	**L**	**L**	**L**	**L**
	IGBT-Side Operation	IGBT On / Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Soft Turn Off	IGBT Turn Off	-

-: Not related Values are typical

Note: When the SEL pin input level is high (= VREG), the IGBT over current detection function is disabled (4.6.1).

Table 6: I/O Truth Table

MCU-side inputs			IGBT-side inputs					IGBT-side outputs			MCU-side outputs				Note
VCC1	INA	INB	VREG	VCC2	CS1/2	SEL	TEMP1/2	CLAMP	OUTL	OUTH	SOFT	TEMPOUT	FO	FO_B	FHT1	
<4.1V <20us	X	X	>4.2V	>11V	X	X	>VTEMPVL -0.1V and <4.25V	<3.0V	L	High-Z	High-Z	L	H	L	Charge	VCC1 under voltage MCU-side fault output IGBT turn-off
								>3.0V	High-Z							
>4.2V	L	X						<3.0V	L					H	L	IGBT Normal turn-off
								>3.0V	High-Z							
	X	H						<3.0V	L				L			
								>3.0V	High-Z							
	H	L			<0.25V			X	High-Z	H		PWM Output				IGBT Normal turn-on
					>0.25V and <0.5V >1.0us	H		<3.0V	L	High-Z	L	L	H	L	Charge	Over current MCU-side fault output IGBT soft turn-off
						L	X	>3.0V	High-Z							
					>0.5V	X		<3.0V	L							Short circuit MCU-side fault output IGBT soft turn-off
								>3.0V	High-Z							
<4.1V >20us	X	X	X	X	X			<3.0V	L							VCC1 under voltage MCU-side fault output Communication timeout IGBT soft turn-off
								>3.0V	High-Z							
>4.2V	X	X	<4.1V					<3.0V	L							VREG under voltage MCU-side fault output IGBT soft turn-off
								>3.0V	High-Z							
			>4.2V	<10V >25us				<3.0V	L							VCC2 under voltage MCU-side fault output IGBT soft turn-off
								>3.0V	High-Z							
				>11V			<VTEMPVL -0.1V >10us	<3.0V	L			PWM Output				IGBT over-temp MCU-side fault output IGBT soft turn-off
								>3.0V	High-Z							
							>4.25V >10us	<3.0V	L							Open IGBT temp diode MCU-side fault output IGBT soft turn-off
								>3.0V	High-Z							

X: Don't care

Values are typical

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Ta = -40 to 125 degC, PGND2 = GND2=0V, PVCC2 = VCC2, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units
				Min.	Typ.	Max.	
A1	V_{ISO1}	Maximum Isolation (t=60sec)		2500	-	-	V_{RMS}
A2	V_{ISO2}	Maximum Isolation (t=1sec)		3000	-	-	V_{RMS}
A3	V_{ISO3}	Maximum Isolation DC		650			V
A4	V_{CMR}	Common Mode Rejection		35	-	-	KV/us
A5	V_{CC1}	Positive Power Supply MCU-side	VCC1	-0.3	-	6.5	V
A6	V_{CC2}	Positive Power Supply IGBT-side	VCC2, PVCC2	-0.3	-	40	V
A7	V_{OUT2}	Gate Driver Output Voltage	OUTH, OUTL, CLAMP, SOFT	-0.3	-	V_{CC2}+0.3	V
A8	I_{OUTH}	Gate Driver High-Side Peak Current	OUTH f_{ISO}=10kHz, t=1us	-10	-	0	A
A9	I_{OUTL}	Gate Driver Low-Side Peak Current	OUTL, CLAMP f_{ISO}=10kHz, t=1us	0	-	10	A
A10	I_{SOFT}	Soft Turn Off Peak Current	SOFT	0	-	1.0	A
A11	V_{REG}	Regulator Output Voltage	VREG	-0.3	-	6.5	V
A12	I_{REG}	Regulator Output Current	VREG	-10	-	0	mA
A13	V_{OCD}	Overcurrent Sense Input Voltage	CS1, CS2	-0.3	-	V_{CC2}+0.3	V
A14	V_{IN2}	IGBT-Side Input Voltage	TEMP1, TEMP2, SEL, TEMPVL, TREF, CTEMP	-0.3	-	V_{REG}+0.3	V
A15	V_{IN1}	MCU-Side Input Pin Voltage	INA, INB	-0.3	-	V_{CC1}+0.3	V
A16	V_{OUT1}	Fault Output Voltage	FO, FO_B	-0.3	-	V_{CC1}+0.3	V
A17	V_{TOUT}	Temp Monitor Output Voltage	TEMPOUT	-0.3	-	V_{CC1}+0.3	V
A18	V_{FHT1}	MCU-Side Fault Hold Timer Input Voltage	FHT1	-0.3	-	V_{CC1}+0.3	V
A19	V_{ESD1}	ESD Capability (HBM)	FO, FO_B	-1	-	1	kV
			Other Pins	-2	-	2	kV
A20	V_{ESD2}	ESD Capability (MM)	All Pins	-200	-	200	V
A21	V_{ESD3}	ESD Capability (CDM)	All Pins	-500	-	500	V
			Corner Pins	-750	-	750	
A22	P_d	Power Dissipation	Rj-a=83.3℃/W Note1	-	-	0.30	W
A23	T_A	Ambient Temperature	-	-40	-	125	°C
A24	T_J	Junction Temperature	-	-40	-	150	°C
A25	T_{STG}	Storage Temperature	-	-55	-	150	°C

Current flowing directions are:

Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Note1 : Mounted on FR4 board. IC stand alone. JEDEC compliant

5.2 Recommended Operating Conditions

PGND2 = GND2 = 0 V, PVCC2 = VCC2, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units
				Min.	Typ.	Max.	
B1	V_{CC1}	Positive Power Supply MCU-side	Pin: VCC1	4.5	5.0	5.5	V
B2	V_{CC2}	Positive Power Supply IGBT-side	Pin: VCC2, PVCC2	12.5	15	21.5	V
B3	V_{TEMPVL_R}	TEMPVL Input Voltage Range	Pin: TEMPVL	0.5	-	2.4	V
B4	f_{ISO}	Signal Frequency	Pin: INA, INB	-	15	100	kHz
B5	t_{IN}	Minimum Input Pulse Width	Pin: INA, INB	-	20	-	ns
B6	$f_{TEMPOUT}$	TEMPOUT Output Frequency	Pin: TEMPOUT	1	-	10	kHz
B7	T_A	Ambient Temperature	-	-40	-	125	°C

5.3. Power Supply

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions		Values			Units	Note
					Min.	Typ.	Max.		
V1	I_{CC1Q}	VCC1 Quiescent Supply Current	Pin: VCC1 INA, INB=GND1 or VCC1		-	3.1	5.5	mA	
V2	I_{CC1_15k}	VCC1 Operation Supply Current	Pin: VCC1 INA=15kHz, INB=GND1		-	3.5	6.0	mA	
V3	I_{CC2Q}	VCC2 Quiescent Supply Current	Pin: VCC2 INA, INB=GND1 or VCC1		-	6.3	9.0	mA	
V4	I_{CC2_15k}	VCC2 Operation Supply Current	Pin: VCC2, INA=15kHz, INB=GND1, No Load		-	6.8	12.0	mA	
V5	V_{REG1}	VREG Output Voltage	Pin: VREG, I_{REG}=0mA	-40℃～125℃	4.7	5.0	5.3	V	
				25℃	4.8	5.0	5.2		
V6	V_{REG2}	VREG Output Voltage	Pin: VREG, I_{REG}=-5mA		4.7	5.0	5.3	V	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

5.4. Logic Input/Output

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
L1	V_{INL}	Low Level Input Voltage	Pin: INA, INB	-		0.3 x V_{CC1}	V	
L2	V_{INH}	High Level Input Voltage	Pin: INA, INB	0.7 x V_{CC1}	-	-	V	
L3	V_{INHYS}	Input Hysteresis	Pin: INA, INB	-	0.12 x V_{CC1}	-	V	
L4	R_{INA}	INA Pull-down Resistance	Pin: INA,	50	100	200	kΩ	
L5	R_{INB}	INB Pull-up Resistance	Pin: INB,	50	100	200	kΩ	
L6	R_{OL_FO}	FO/FOB Low Level Output Resistance	Pin: FO, FO_B, I_O=2mA	-	20	100	Ω	
L7	R_{OH_FO}	FO/FOB High Level Output Resistance	Pin:FO,FO_B, I_O= -10uA	50	100	250	kΩ	
L8	I_{OFF_FO}	Off Leak Current	Pin: FO, FO_B FO=FO_B=VCC1	-1	-	1	uA	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

5.5. Gate Driver

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
D1	R_{O_OUTH}	OUTH High Level Output Resistance	Pin: OUTH, I_O=-100mA	-	0.5	1.0	Ω	
D2	I_{OL_OUTH}	OUTH Low Level Leak Current	Pin: OUTH, OUTH=PGND2	-10	-	-	uA	
D3	R_{O_OUTL}	OUTL Low Level Output Resistance	Pin: OUTL, I_O=100mA	-	0.5	1.0	Ω	
D4	I_{OH_OUTL}	OUTL High Level Leak Current	Pin: OUTL, OUTL=PVCC2	-	-	10	uA	
D5	t_{PLH}	INA High to OUTH 10% Propagation Delay	Pin: INA, OUTH, R_{GH}=5.1Ω, R_{GL}=5.1Ω	30	70	140	ns	
D6	t_{PHL}	INA Low to OUTL 90% Propagation Delay	Pin: INA, OUTL, R_{GH}=5.1Ω, R_{GL}=5.1Ω	30	70	140	ns	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

5.6. Active Miller Clamp

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
M1	R_{O_CLAMP}	CLAMP Low Level Output Resistance	Pin: CLAMP, I_O=100mA	-	0.5	1.0	Ω	
M2	I_{OH_CLAMP}	CLAMP High Level Leak Current	Pin: CLAMP, CLAMP=PVCC2	-	-	10	uA	
M3	V_{CLAMP}	CLAMP Trip Voltage	Pin: CLAMP	2.7	3.0	3.3	V	
M4	t_{CLAMP}	Active Mirror Clamp Delay Time	Pin: CLAMP	20	70	140	ns	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

5.7. Soft Turn-off

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
S1	R_{o_SOFT}	SOFT Low Level Output Resistance	Pin: SOFT, Io=0.1A	-	3.5	8.5	Ω	
S2	I_{OH_SOFT}	SOFT High Level Leak Current	Pin: SOFT, SOFT=PVCC2	-	-	3	uA	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

5.8. UVLO

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
U1	V_{UVLO_VCC1T}	VCC1 UVLO Trip Voltage	Pin: VCC1	3.8	4.1	4.4	V	
U2	V_{UVLO_VCC1R}	VCC1 UVLO Recovery Voltage	Pin: VCC1	3.9	4.2	4.5	V	
U3	V_{UVLO_VCC1H}	VCC1 UVLO Hysteresis	Pin: VCC1	-	0.1	-	V	
U7	V_{UVLO_VCC2T}	VCC2 UVLO Trip Voltage	Pin: VCC2	9	10	11	V	
U8	V_{UVLO_VCC2R}	VCC2 UVLO Recovery Voltage	Pin: VCC2	10	11	12	V	
U9	V_{UVLO_VCC2H}	VCC2 UVLO Hysteresis	Pin: VCC2	-	1.0	-	V	
U13	V_{UVLO_VREGT}	VREG UVLO Trip Voltage	Pin: VREG	3.8	4.1	4.4	V	
U14	V_{UVLO_VREGR}	VREG UVLO Recovery Voltage	Pin: VREG	3.9	4.2	4.5	V	
U15	V_{UVLO_VREGH}	VREG UVLO Hysteresis	Pin: VREG	-	0.1	-	V	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Note
1. Guaranteed by design and not subject to production testing.

5.9. Over Current (OC) Detection/Short Circuit (SC) Detection

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
C1	I_{CSL}	CS Low Level Input Current	Pin: CS1, CS2 CS1, CS2=GND2	-1	-	-	uA	
C2	I_{CSH}	CS High Level Input Current	Pin: CS1, CS2 CS1, CS2=VREG	-	-	1	uA	
C3	V_{OC}	OC Threshold Voltage	Pin: CS1, CS2 SEL=GND2	0.22	0.25	0.28	V	
C4	$t_{OC-OUTH}$	OC Sense to 90% OUTH Delay	Pin: CS1, CS2, OUTH, SEL=GND2, R_L=1kΩ	-	1.2	2.4	us	
C5	$t_{OC-SOFT}$	OC Sense to 90% SOFT Delay	Pin: CS1, CS2, SOFT, SEL=GND2, R_{SOFT}=1kΩ	-	1.2	2.4	us	
C6	t_{OC-FO_B}	OC Sense to 10% FO_B Delay	Pin: CS1, CS2, FO_B, SEL=GND2, R_{FO}=3kΩ	-	1.2	2.4	us	
C7	V_{SC}	SC Threshold Voltage	Pin: CS1, CS2 SEL=VREG	0.44	0.5	0.56	V	
C8	$t_{SC-OUTH}$	SC Sense to 90% OUTH Delay	Pin: CS1, CS2, OUTH, SEL=VREG, R_L=1kΩ	-	100	400	ns	1
C9	$t_{SC-SOFT}$	SC Sense to 90% SOFT Delay	Pin: CS1, CS2, SOFT, SEL=VREG, R_{SOFT}=1kΩ	-	100	400	ns	1
C10	t_{SC-FO_B}	SC Sense to 10% FO_B Delay	Pin: CS1, CS2, FO_B, SEL=VREG, R_{FO}=3kΩ	-	100	400	ns	1
C11	R_{SEL}	SEL Pull-down Resistance	Pin: SEL	50	100	200	kΩ	
C12	V_{INL_SEL}	Low Level Input Voltage at SEL	Pin: SEL	-		0.3 x V_{REG}	V	
C13	V_{INH_SEL}	High Level Input Voltage at SEL	Pin: SEL	0.7 x V_{REG}		-	V	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Note
1. Guaranteed by design and not subject to production testing.

5.10. Temperature Monitor

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions			Values			Units	Note
						Min.	Typ.	Max.		
T1	V_{TREF}	TREF Output Voltage	Pin: TREF I_{TREF}= -100uA			0.36	0.40	0.44	V	
T2	V_{TEMPVH}	IGBT Temperature Monitor High Limit Input Voltage	(IC internal)			3.50	3.80	4.10	V	1
T3	I_{TEMP}	TEMP Bias Current	Pin: TEMP1, TEMP2 V_{TEMP1}=3.0V V_{TEMP2}=3.0V	I_{TREF}= -10uA		-107	-100	-93	uA	
				I_{TREF}= -100uA		-1070	-1000	-930	uA	
T4	D_{OUT}	PWM On Duty	Pin: TEMPOUT TEMPVL =0.5V	TEMP=1.16V		13	20	27	%	
				TEMP=2.15V	-40℃~125℃	43	50	57	%	
					25℃	45	50	55	%	
				TEMP=3.14V		73	80	87	%	
T5	D_{OUT_UL}	PWM On Duty Upper Limit		TEMP>3.6V		83	90	97	%	
T6	D_{OUT_LL}	PWM On Duty Lower Limit		TEMP<0.7V		3	10	17	%	
T7	I_{TEMPVL}	TEMPVL Input Current	Pin: TEMPVL			-1.0	-	1.0	uA	
T8	$F_{TEMPOUT}$	TEMPOUT Output Frequency	Pin: TEMPOUT TEMPVL=0.5V CTEMP=4.7nF			1	2	4	kHz	
T9	V_{OL_TO}	Low Level Output Voltage	Pin: TEMPOUT, I_O=1mA			-	-	0.20 x V_{CC1}	V	
T10	V_{OH_TO}	High Level Output Voltage	Pin: TEMPOUT, I_O=-1mA			0.80 x V_{CC1}	-	-	V	
T11	V_{OT}	OT Detect Threshold Voltage	Pin: TEMP1, TEMP2, TEMPVL=0.5V			0.36	0.4	0.44	V	
T12	V_{OP}	OPEN Detect Threshold Voltage	Pin: TEMP1, TEMP2			3.85	4.25	4.65	V	
T13	$t_{OT-OUTH}$	OT Sense to 90% OUTH Delay	Pin: TEMP1, TEMP2, OUTH, R_L=1kΩ			5	10	20	us	
T14	$t_{OT-SOFT}$	OT Sense to 90% SOFT Delay	Pin: TEMP1, TEMP2, SOFT, R_{SOFT}=1kΩ			5	10	20	us	
T15	t_{OT-FO}	OT Sense to 10% FO Delay	Pin: TEMP1, TEMP2, FO, R_{FO}=3kΩ			5	10	20	us	
T16	$t_{OP-OUTH}$	OPEN Sense to 90% OUTH Delay	Pin: TEMP1, TEMP2, OUTH, R_L=1kΩ			5	10	20	us	
T17	$t_{OP-SOFT}$	OPEN Sense to 90% SOFT Delay	Pin: TEMP1, TEMP2, SOFT, R_{SOFT}=1kΩ			5	10	20	us	
T18	t_{OP-FO}	OPEN Sense to 10% FO Delay	Pin: TEMP1, TEMP2, FO, R_{FO}=3kΩ			5	10	20	us	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

Note
1. Guaranteed by design and not subject to production testing.

5.11. Fault Signal Output Hold Timer

Ta = -40 to 125 degC, GND1 = GND2 = PGND2 = 0 V, VCC1 = 4.5 to 5.5 V, VCC2 = PVCC2 = 12.5 to 21.5 V, unless otherwise specified.

No.	Symbol	Parameter	Pin, Conditions	Values			Units	Note
				Min.	Typ.	Max.		
F1	V_{FHT1}	Fault Hold Timer Threshold Voltage	Pin: FHT1	1.75	2	2.35	V	
F2	I_{CHG_FHT1}	Fault Hold Timer Charge Current	Pin: FHT1, FHT1=1V	-6	-4.5	-2.5	uA	
F3	I_{DSCHG_FHT1}	Fault Hold Timer Discharge Current	Pin: FHT1, FHT1=1V	1.0	3.6	-	mA	
F4	t_{FHT0}	Fault Hold Time 0	Pin: FO, FO_B,SOFT R_{FO}=3kΩ, C_{FHT1}=0	50	100	200	us	
F5	t_{FHT1}	Fault Hold Time 1	Pin: FO, FO_B R_{FO}=3kΩ, C_{FHT1}=0.047uF	15	21	45	ms	

Current flowing directions are:
Plus (+) or none: from outside to IC, Minus (–): from IC to outside

6. Timing Chart

6.1 Normal Gate Drive Output

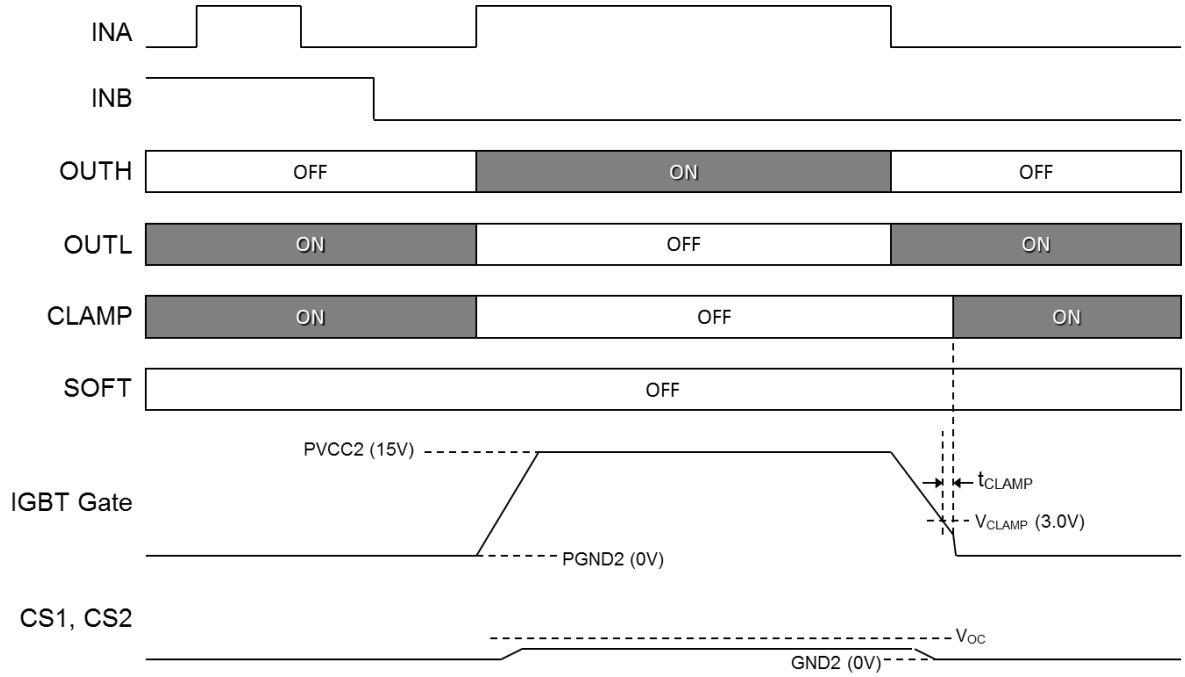


Figure 12: Normal IGBT ON and OFF Operation

6.2 Gate Drive Output at Detection of Abnormal State

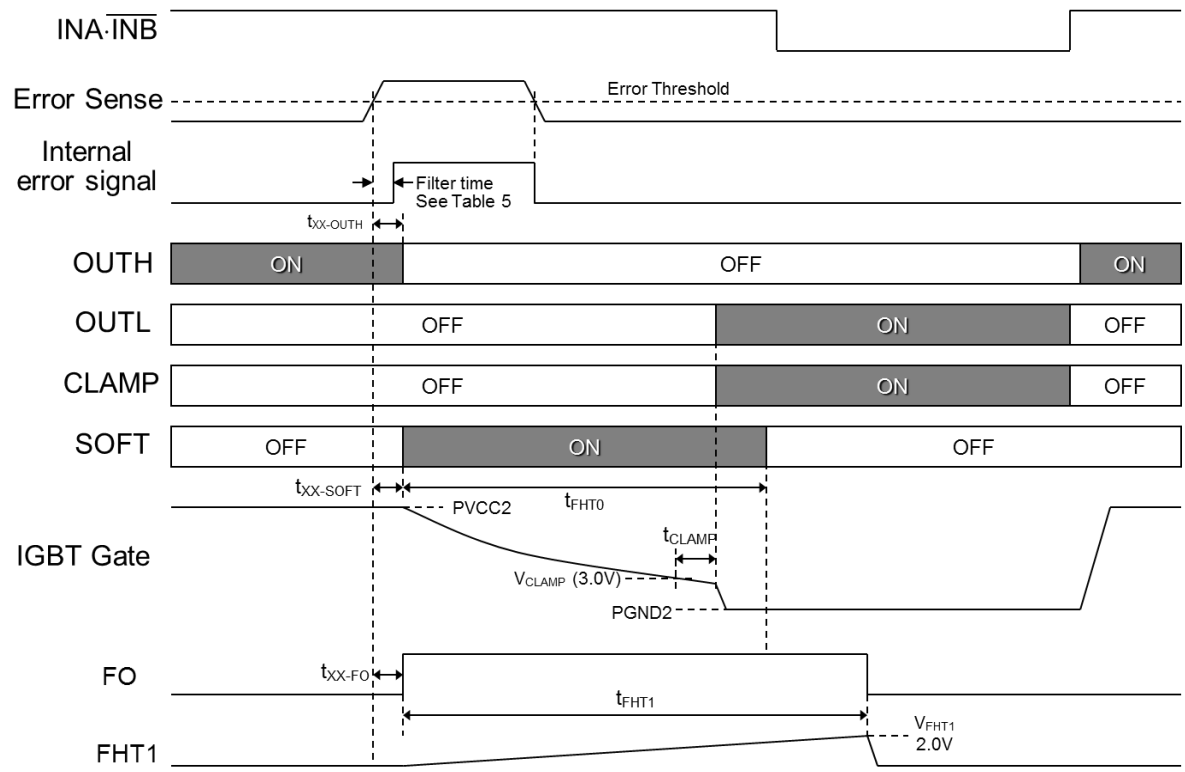


Figure 13: Operation When an Abnormal State is detected with IGBT being ON (Fault Signal Output Cleared by FHT1 Hold Time)

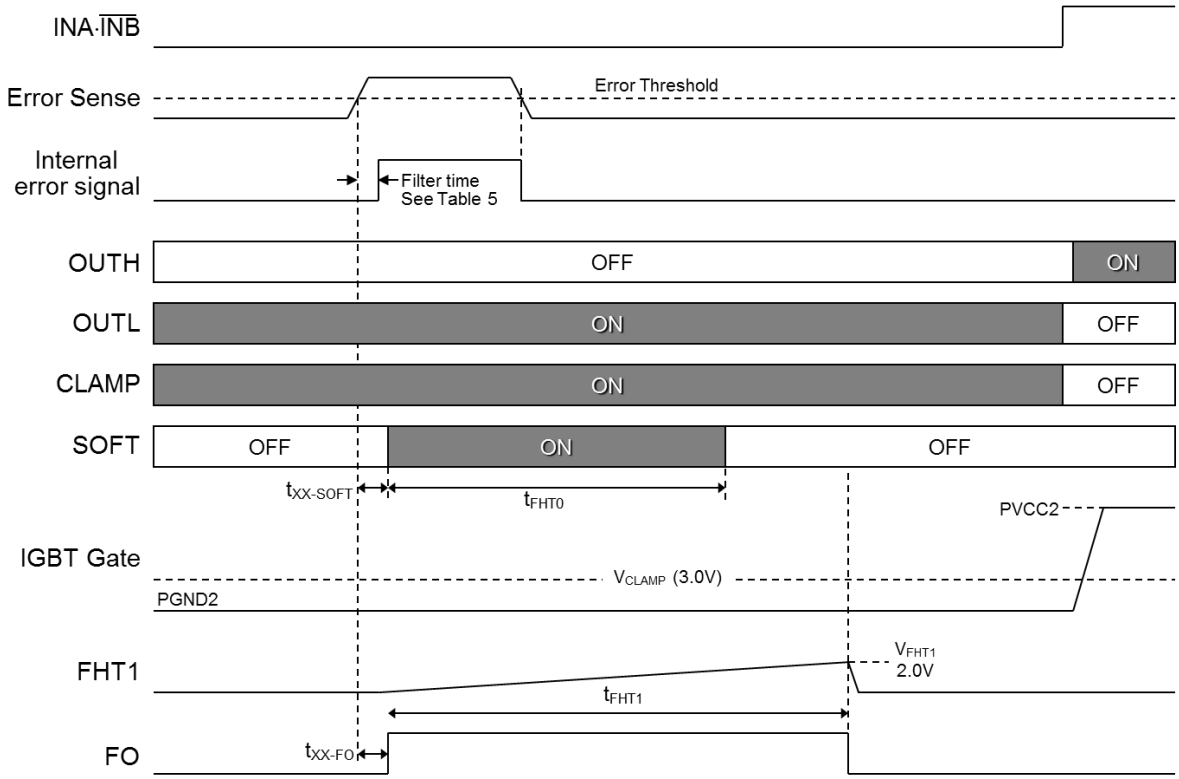


Figure 14: Operation When an Abnormal State is detected with IGBT being OFF (Fault Signal Output Cleared by FHT1 Hold Time)

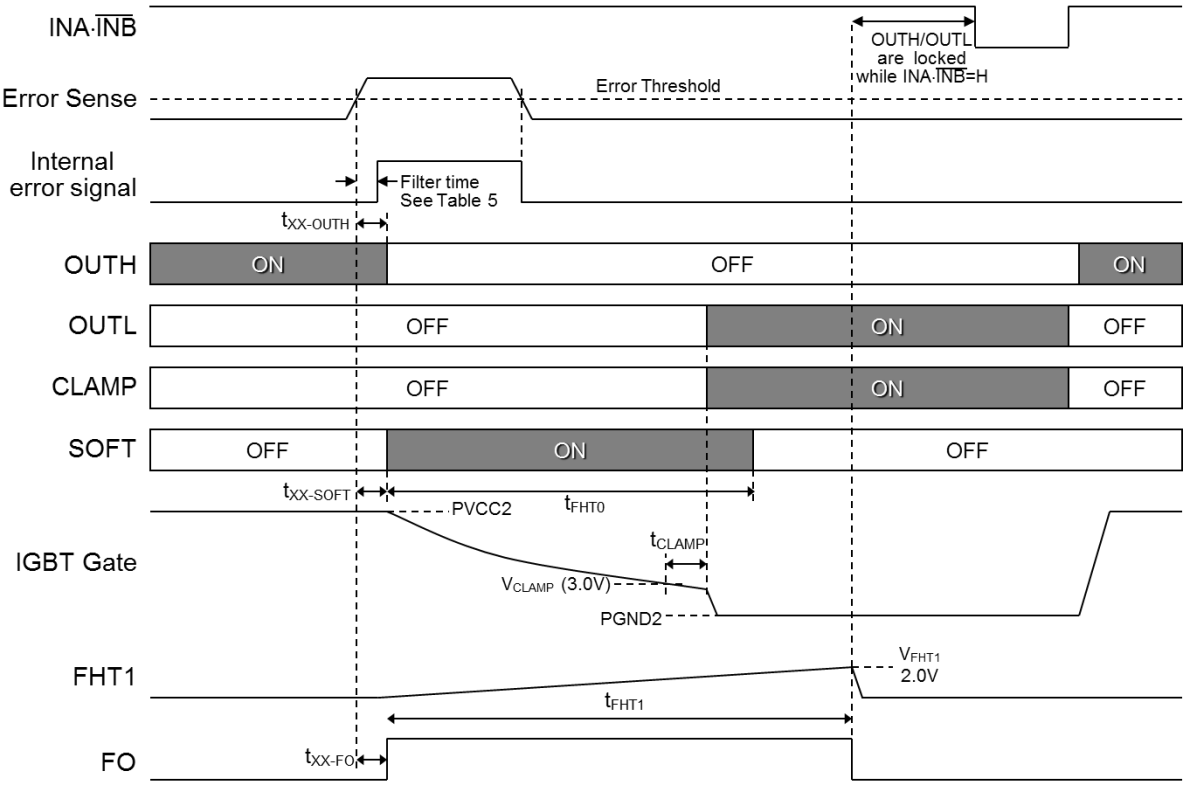


Figure 15: Fault Signal Output Cleared by Edge of INA $\overline{INB}$

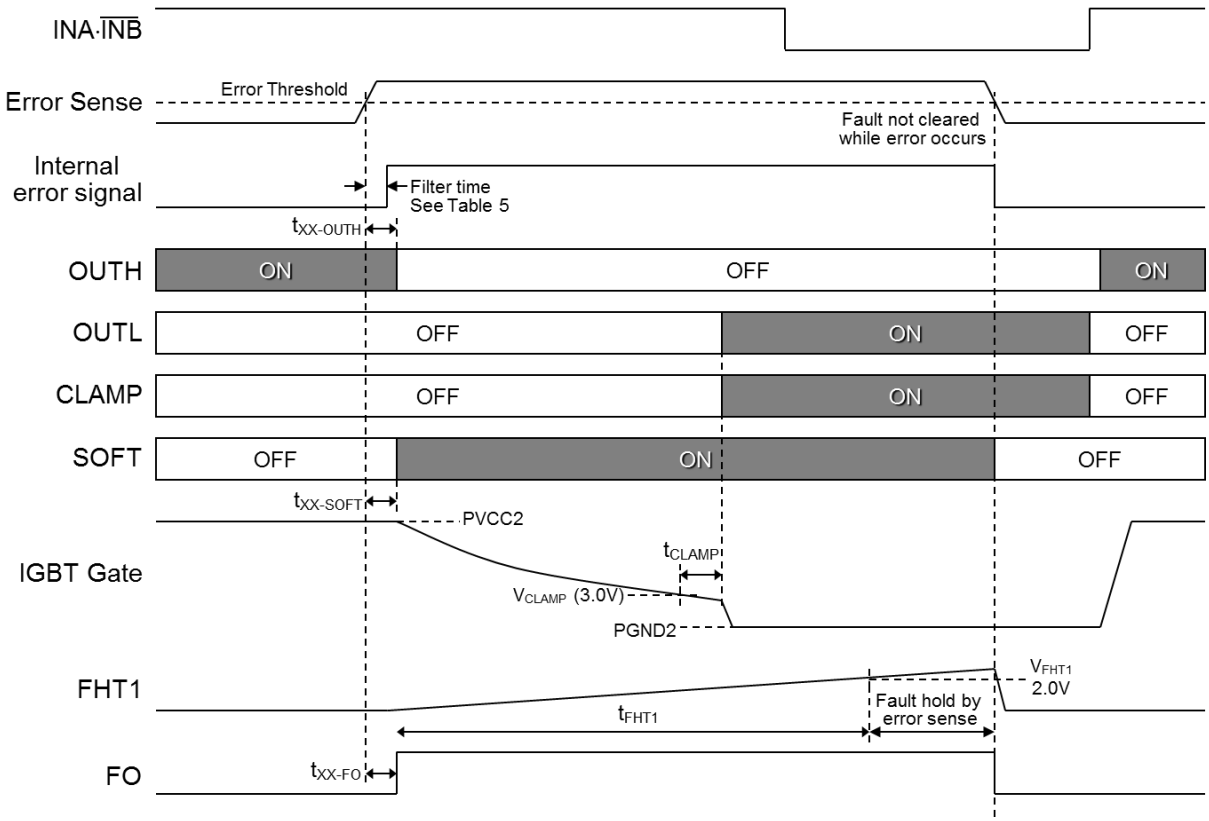


Figure 16: Fault Signal Output Cleared by Falling of Error Input Signal

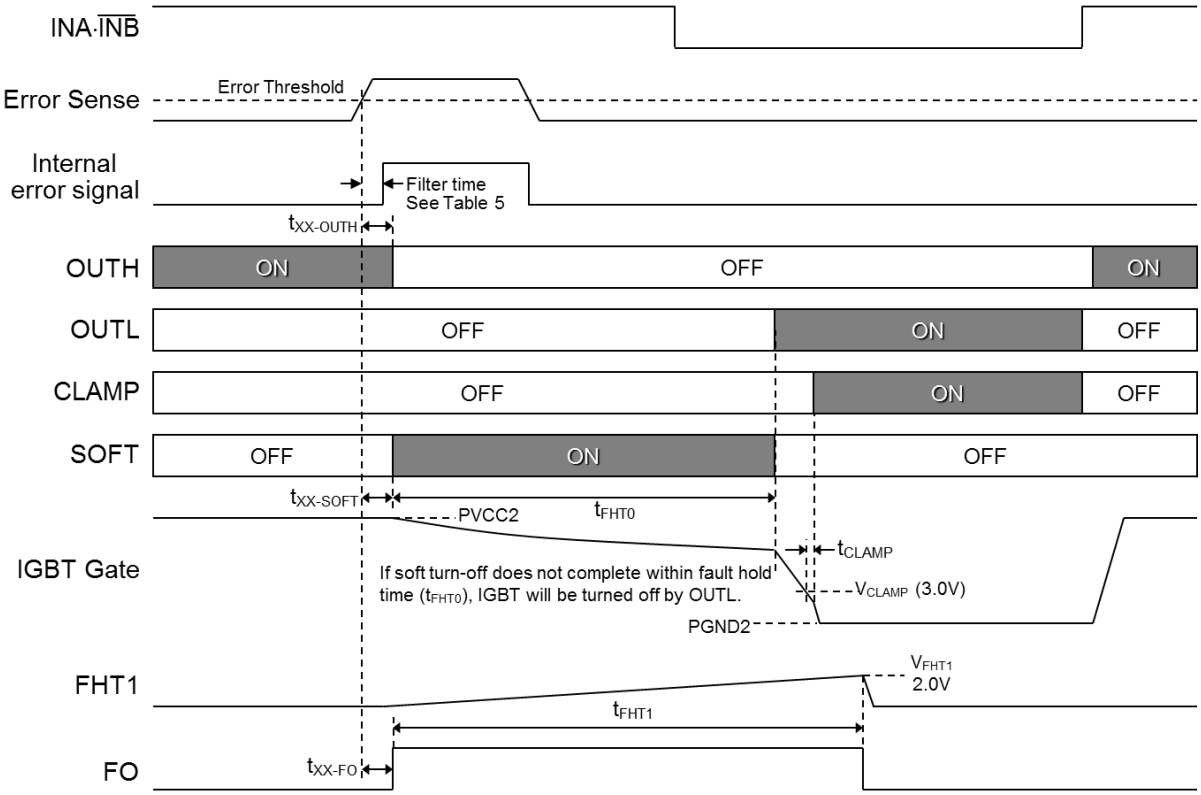


Figure 17: In Case of Uncompleted Soft Turn-off

6.3 Timing Charts for Detections of Various Abnormal States

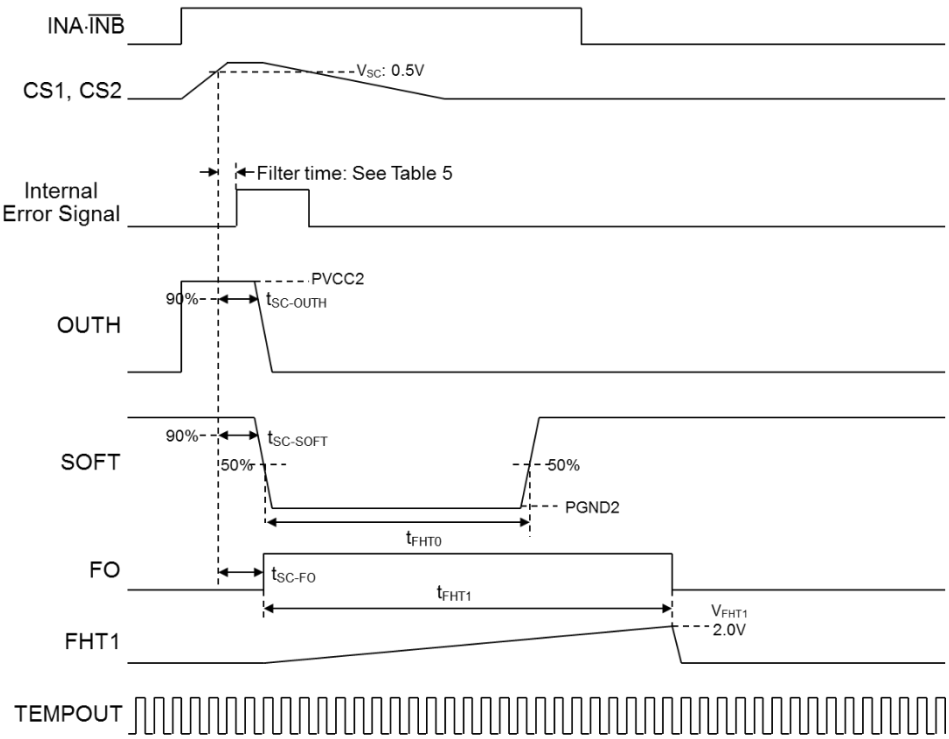


Figure 18: Short Circuit (SC) Detection

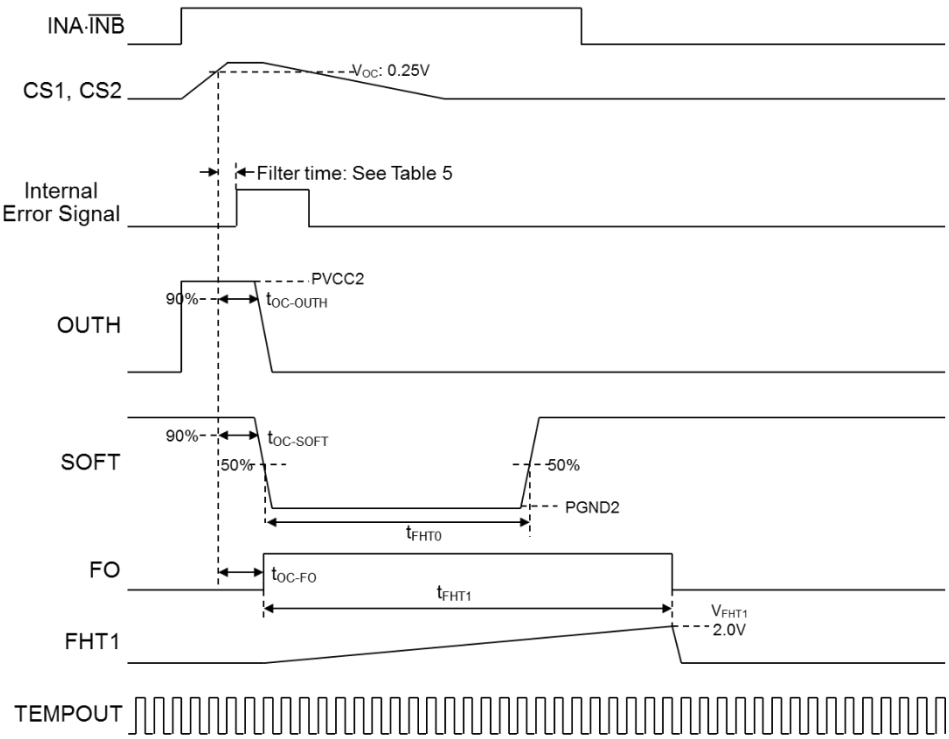


Figure 19: Over Current (OC) Detection

( ) indicates an IC internal voltage.

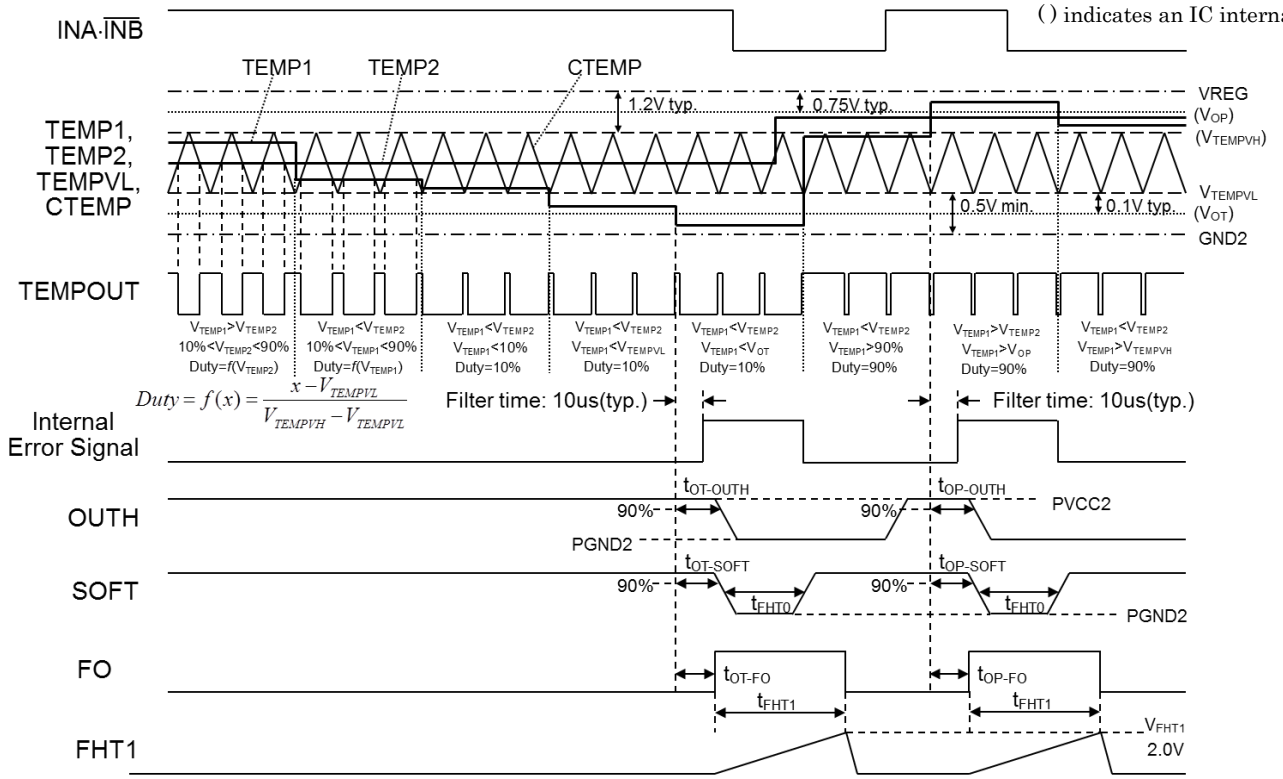


Figure 20: IGBT Temperature Monitor

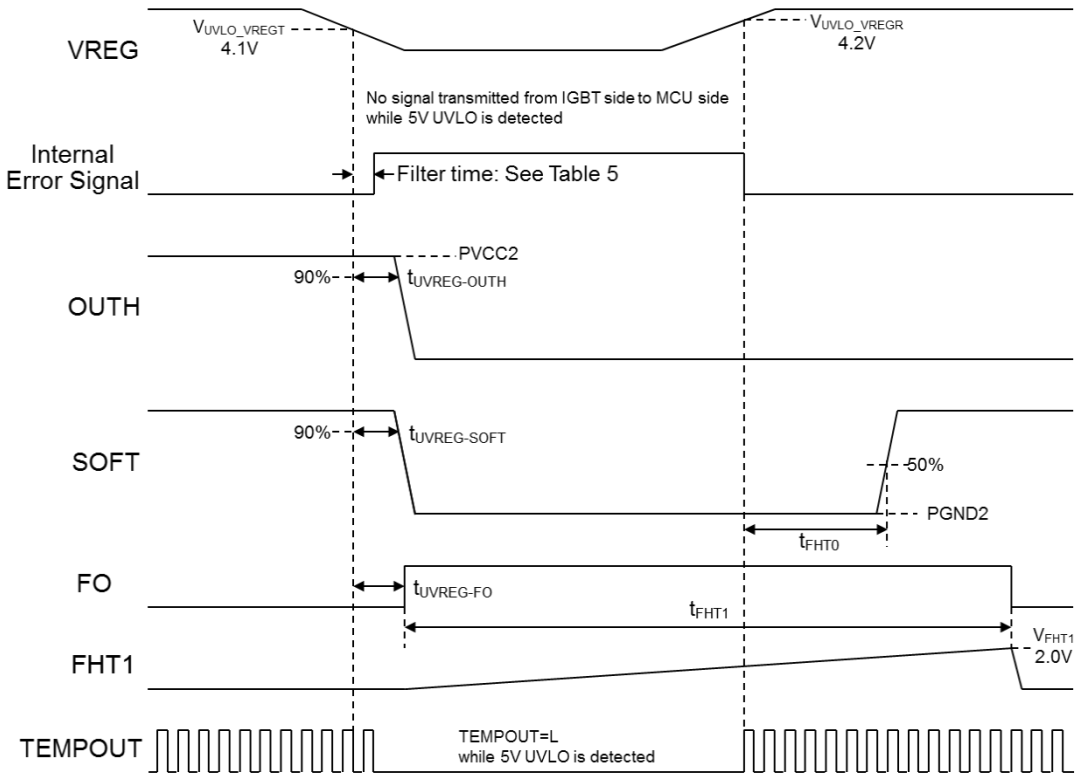


Figure 21: Secondary 5 V UVLO

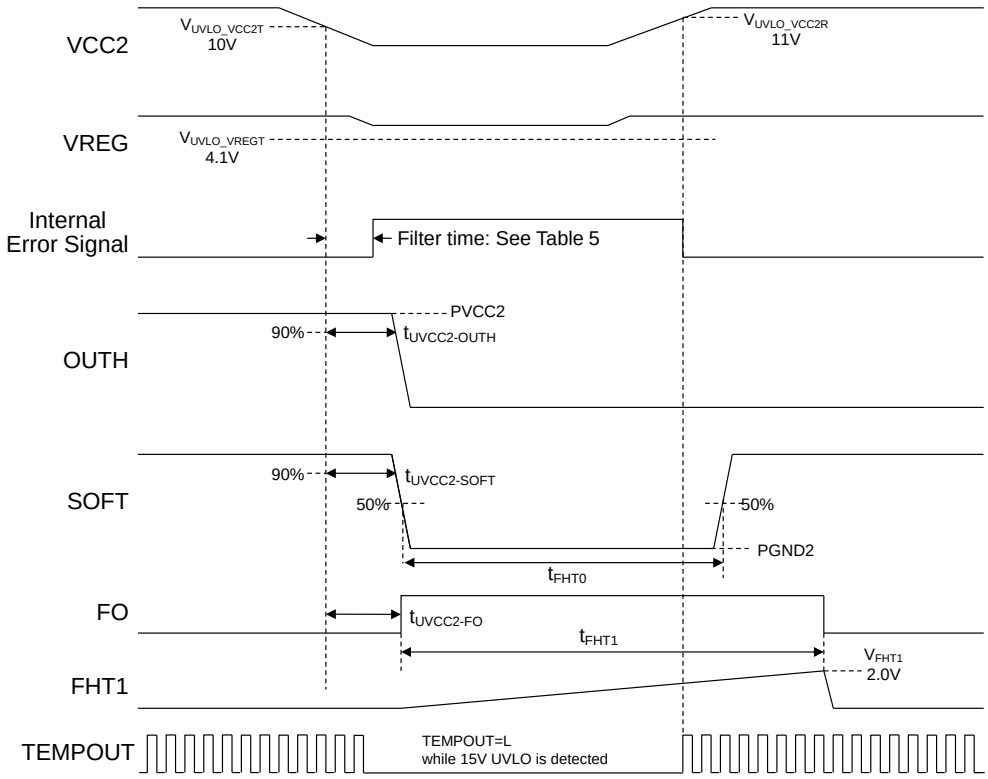


Figure 22: Secondary 15 V UVLO

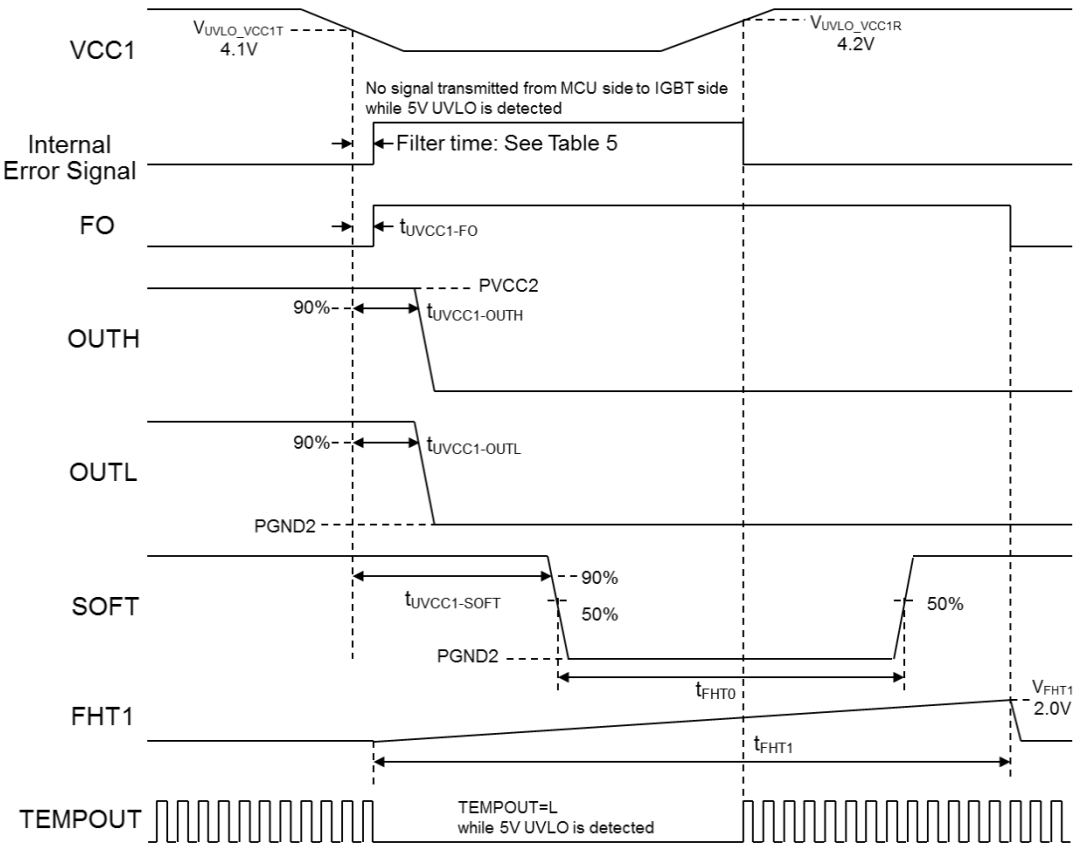


Figure 23: Primary UVLO

7. Package

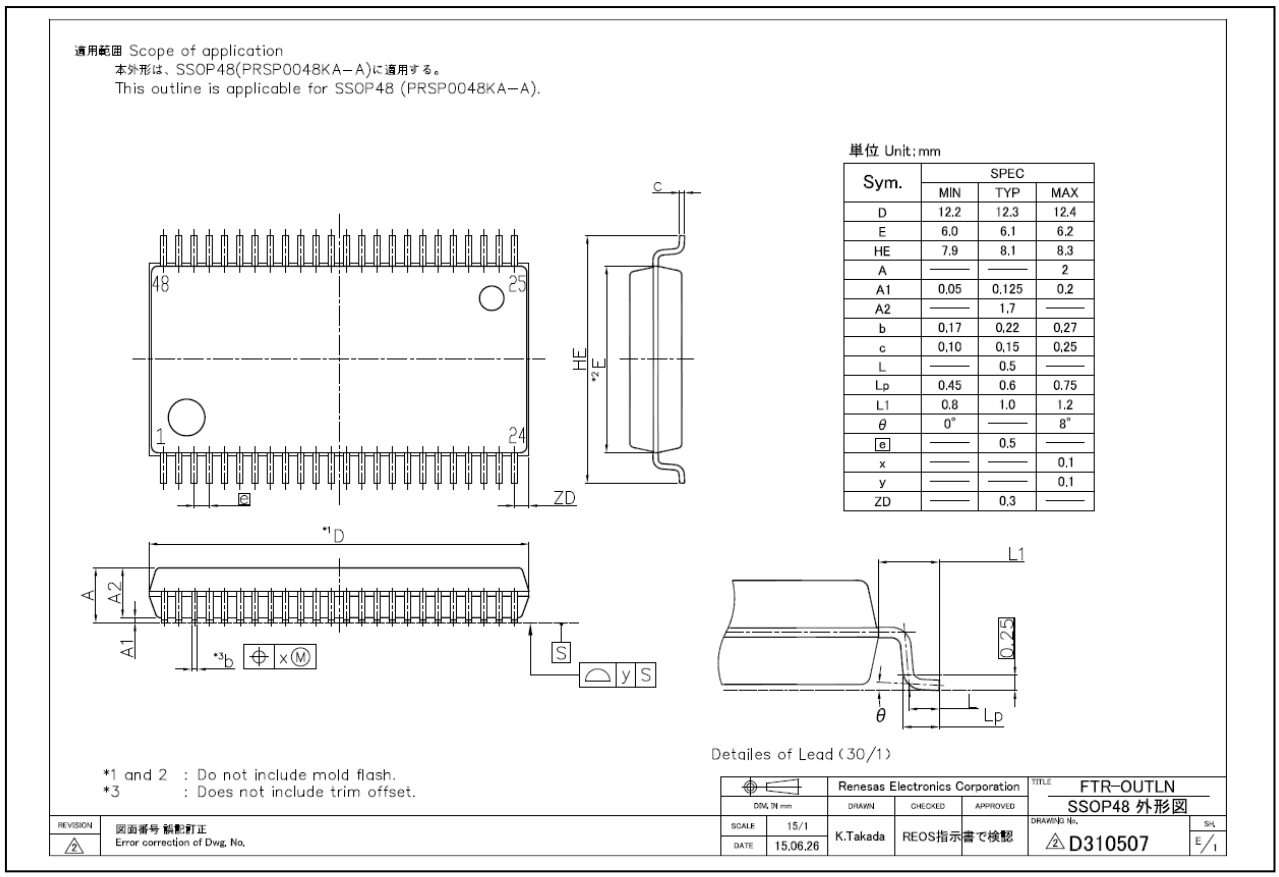


Figure 24: SSOP48 Package

8. Application Examples

Figure 25 shows a circuit example including two IGBTs connected in parallel. In this example, the secondary power supply (VCC2) is 15 V. The primary power supply (VCC1) voltage is the same as the power supply voltage of the MCU (VDD).

For the gate pins of the IGBT, 5.1 ohms are inserted between that and OUTH of the IC (R_{GH}) and between that and OUTL (R_{GL}), respectively. To the gate pins of the IGBT, the SOFT and CLAMP pins of the IC are directly connected via 47 ohms (R_{SOFT}), respectively.

For over current and load short-circuit current detection, the emitter current is detected by a combination of the multi-emitter output IGBT and shunt resistors. In this example, the shunt resistors (R_{CS}) to be connected to the CS1 and CS2 pins are 15 ohms. By this setting, when current flowing into the shunt resistor exceeds 16.7 mA for 1 us or more, it is detected as the over current state; when exceeding 33.3 mA, it is detected as the load short-circuit state immediately (detected as an abnormal state).

For IGBT temperature detection, the TEMP1 and TEMP2 pins are connected to the temperature sense diodes implemented in the IGBTs. Normally, a PWM signal with the on-duty ratio corresponding to a lower voltage of either the TEMP1 or TEMP2 pin is sent out from the TEMPOUT pin to the MCU. Since 4.7 nF is connected with the CTEMP pin, a frequency of the PWM signal to be sent out becomes 2.1 kHz. Since 0.5 V obtained by dividing the VREG pin output is applied to the TEMPVL pin, when either the TEMP1 or TEMP2 pin falls short of 0.4 V (V_{OT} = V_{TEMPVL} - 0.1) or exceeds 4.25 V (V_{OP}), it is detected as an abnormal state.

If an abnormal state is detected, the gate of the IGBT is soft turned off, and a fault signal is sent out from the FO pin to the MCU at the same time. Since 0.047 uF is connected with the FHT1 pin, the fault signal is held for about 21 ms.

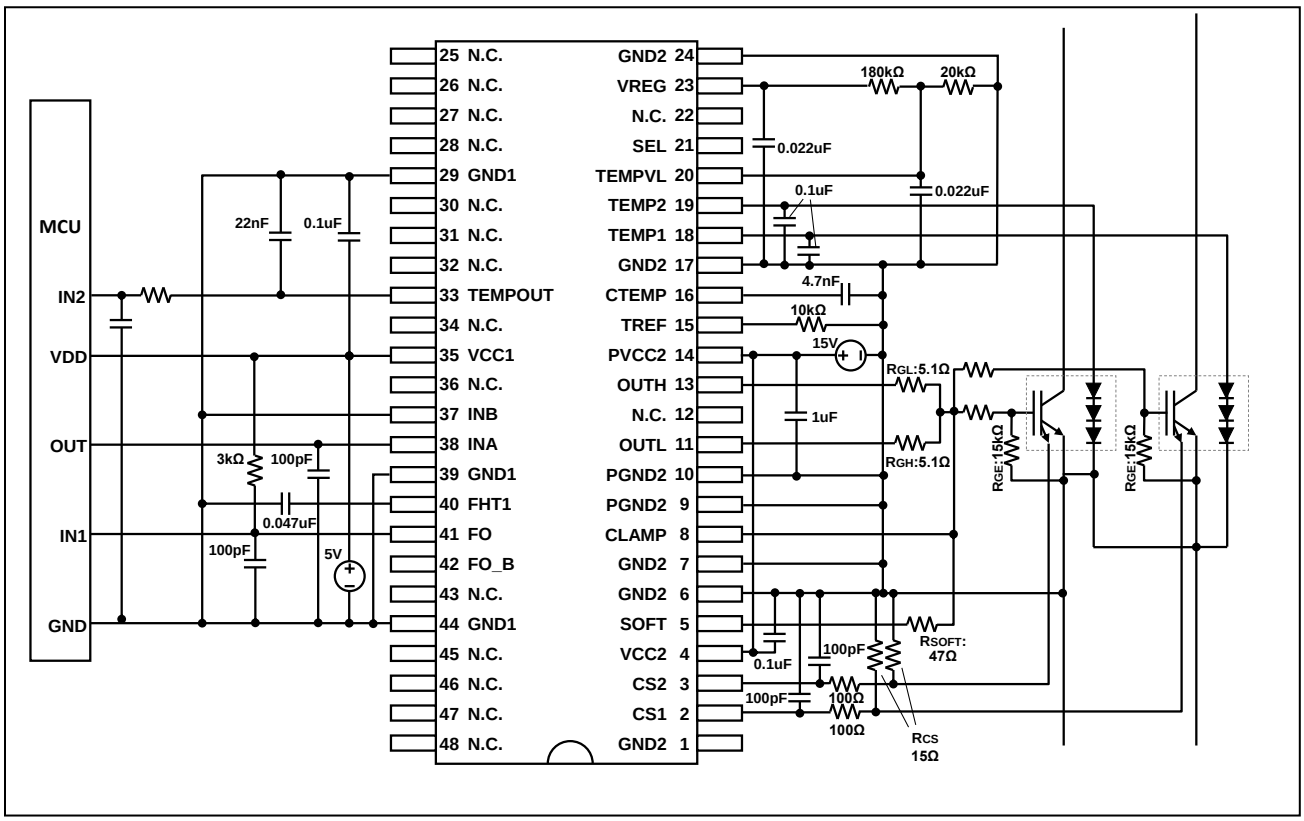


Figure 25: Circuit Example around the IC

8.1 Circuit Example of Power Supply and GND Pins

Figure 26 shows the circuit example of the power supply and GND pins. Two GND1 pins (pin 25 and pin 37) must be short-circuited outside the IC. The GND2 pins (pin 5 and pin 14) and PGND2 pins (pin 8 and pin 7) must be short-circuited outside the IC. The bypass capacitor should be placed near each power supply pin as close as possible.

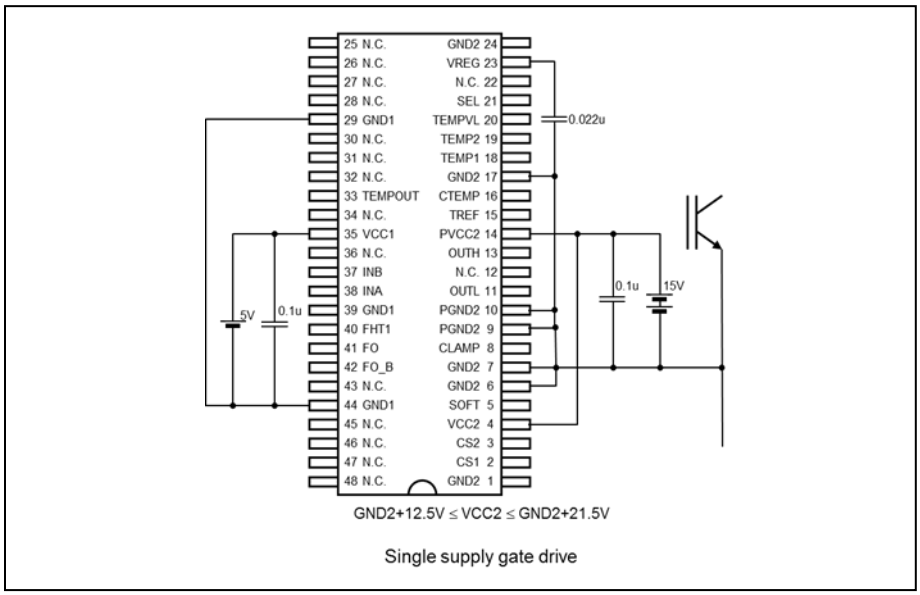


Figure 26: Circuit Example of Power Supply Pins

8.2 Circuit Examples of Inverted/Non-inverted Input Pins

Figure 27 shows the examples in which the inverted input pin and the non-inverted input pin are used. Figure 27 (a) is an example in which the non-inverted input (INA) is used as a gate control signal of the IGBT. The IGBT is tuned on when INA is high. The unused INB pin must be connected to GND1.

Figure 27 (b) is an example in which the inverted input (INB) is used as a gate control signal of the IGBT. IGBT is turned on when INB is low. The unused INA pin must be connected to VCC1.

Figure 27 (c) is an example in which both the non-inverted input (INA) and the inverted input (INB) are used. The IGBT is turned on only when INA = high and INB = low.

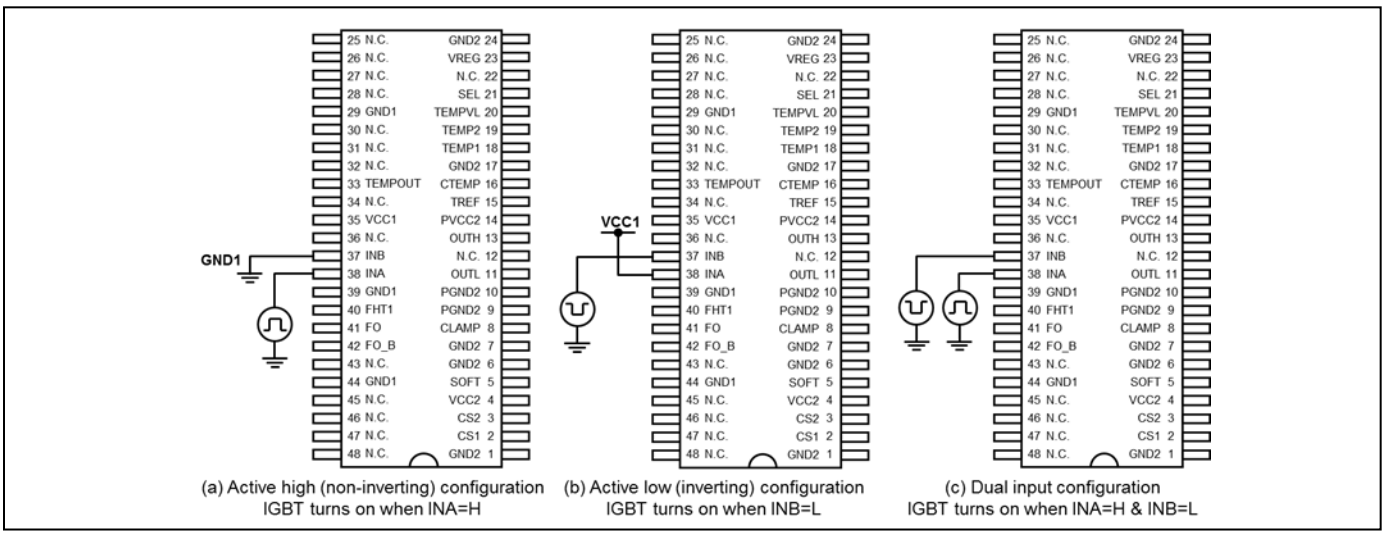


Figure 27: Circuit Examples of Inverted/Non-inverted Input Pins

8.3 Circuit Examples of Gate Driver Output Pins

Figure 28 shows circuit examples of the gate driver output pins. As shown in figure 28 (a), each of the OUTH pin and the OUTL pin must be connected to the gate resistor. Do not short-circuit between the OUTH and OUTL pins as in figure 28 (b).

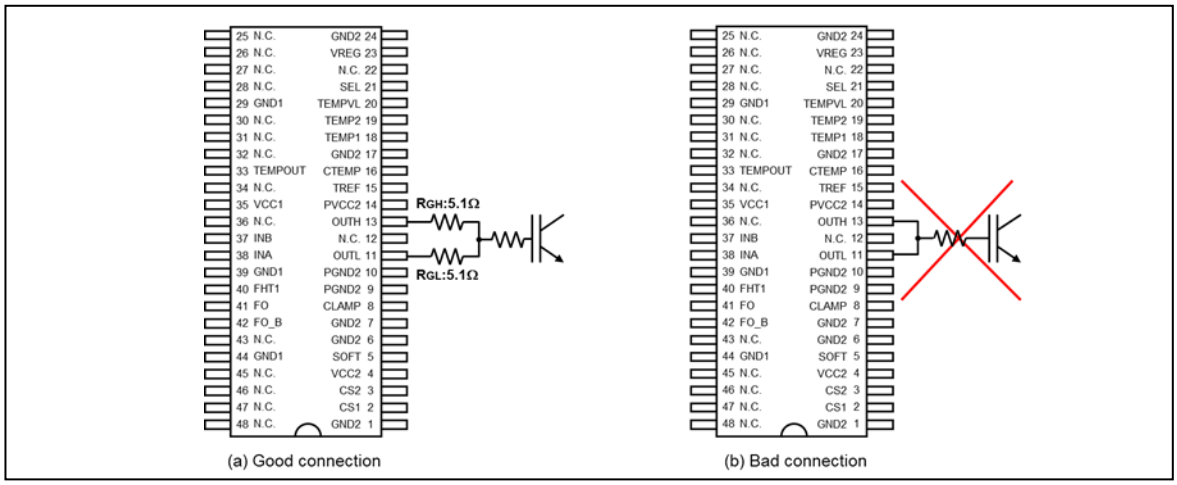


Figure 28: Circuit Examples of Gate Driver Output Pins

8.4 Circuit Examples of Soft Turn-off Output Pin

Figure 29 shows circuit examples of the soft turn-off pin.

As in figure 29 (a), the SOFT pin is connected to the gate pin of the IGBT via the resistor (R_{SOFT}). The soft turn-off time of the IGBT is adjusted by the value of this resistor (R_{SOFT}).

Figure 29 (b) is a circuit example that uses a circuit outside the IC to realize the soft turn-off function. For example, a fault signal (inverted logic: L at fault) can be output at the detection of an abnormal condition by connecting the SOFT pin to the pull-up resistor.

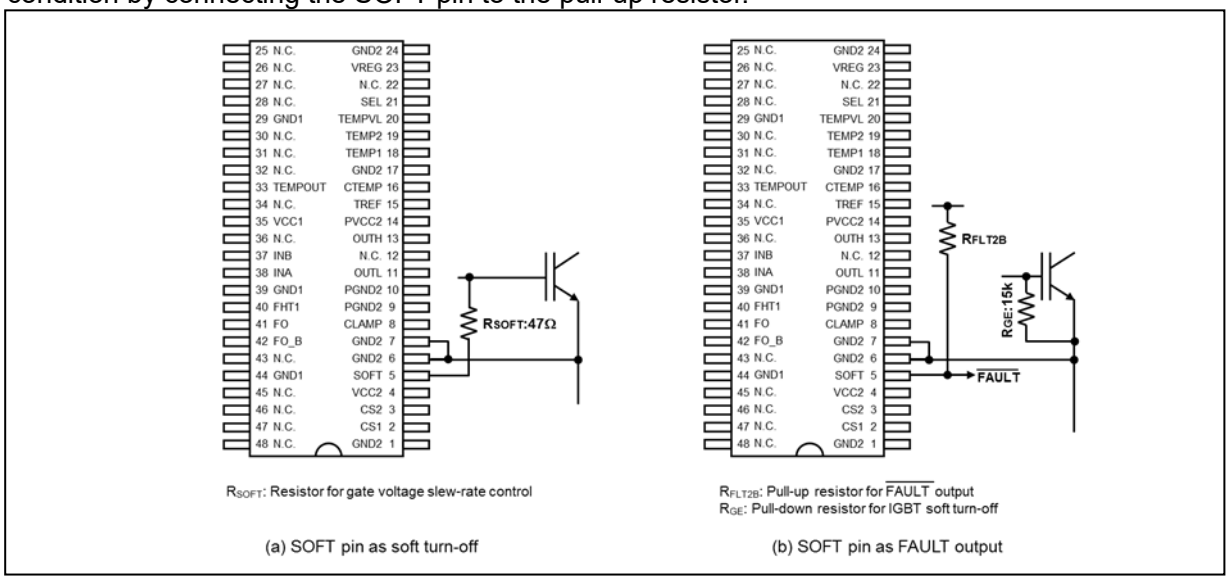


Figure 29: Circuit Examples of Soft Turn-off Output Pin

8.5 Circuit Examples of Over Current/Load Short Circuit Detection Pins

Figure 30 (a) is a circuit example of the over current detection pins when driving the IGBTs in parallel connection. Each of the CS1 pin and the CS2 pin is connected to the shunt resistor for each emitter. In this example, the SEL pin is left open and the over current detection function is enabled.

Figure 30 (b) is a circuit example of the CS1 and CS2 pins when driving a single IGBT. An unused CS pin must be connected to GND2.

Figure 30 (c) is a circuit example when both over current and load short circuit are not detected. Both the CS1 and CS2 pins must be grounded to GND2.

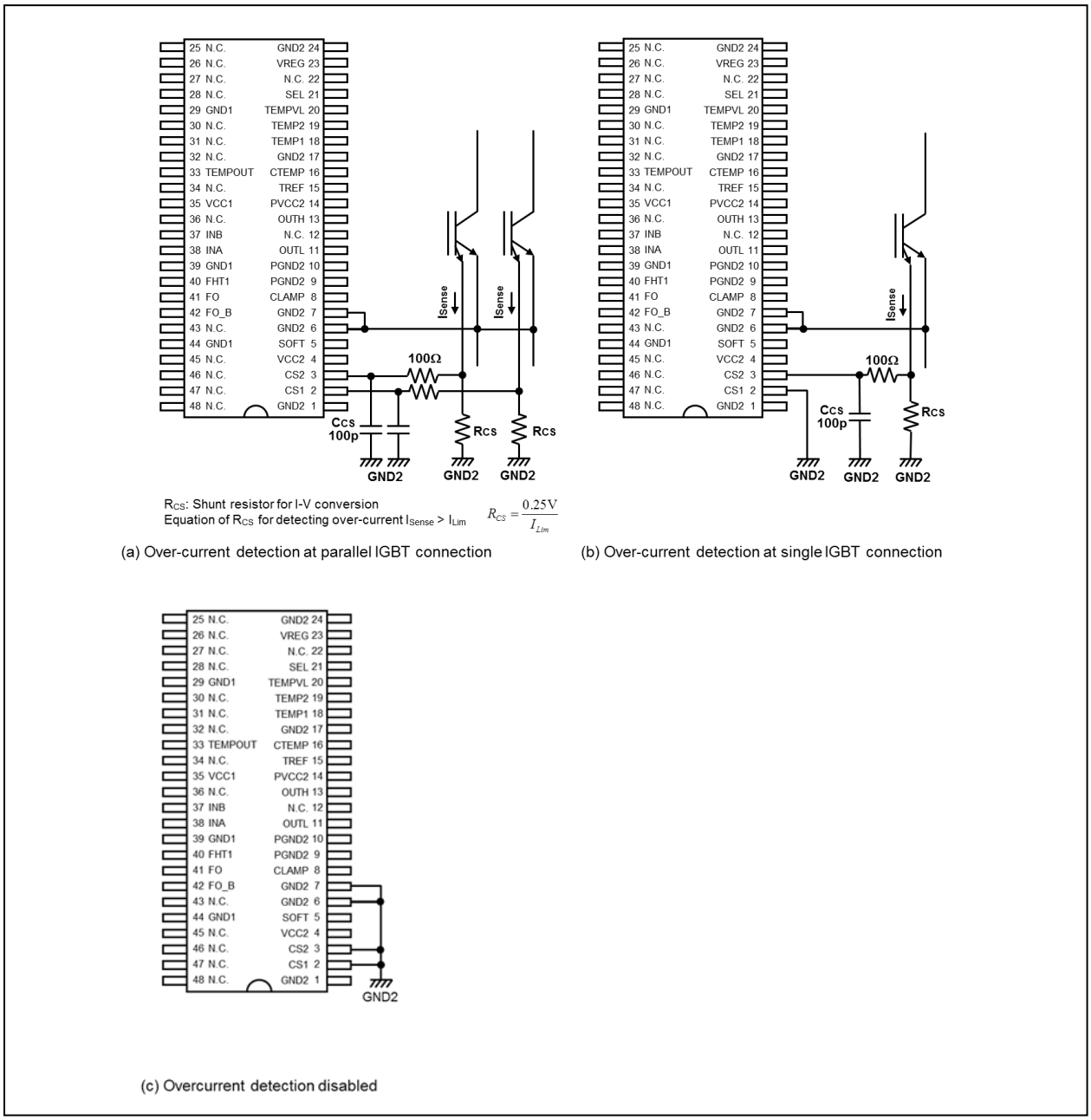


Figure 30: Circuit Examples of Over Current Detection Pins

8.6 Circuit Examples of IGBT Temperature Sense Input

Figure 31 (a) shows the circuit example of detecting the IGBT chip temperature by each of the temperature sense diodes implemented in the IGBTs connected in parallel. The TEMP1 and TEMP2 pins are connected to the anodes of the temperature sense diodes, and the cathodes of the diodes are clamped to GND2. To the TEMPVL pin, the voltage obtained by dividing 5 V output from the VREG pin by the resistors (RTMP1, RTMP2, RTMP3) is applied. When the constant current set by the external resistor of the TREF pin flows from the TEMP1 and TEMP2 pins into the temperature sense diodes in the IGBTs, voltages of the TEMP1 and TEMP2 pins will become forward voltages VF of the diodes. Since VF falls as the temperature rises, voltages of the TEMP1 and TEMP2 pins fall. When the voltage of the TEMP1 or TEMP2 pin becomes further 0.1 V lower than the voltage of the TEMPVL pin, the fault signal is generated.

Figure 31 (b) shows the circuit example of using the NTC thermistor for temperature detection. By outputting the constant current to the NTC thermistor, voltages of the TEMP1 and TEMP2 pins fall as the temperature rises.

Figure 31 (c) shows the circuit example of detecting the chip temperature of a single IGBT by the diode implemented in there. Both the TEMP pins should be short-circuited before use.

Figure 31 (d) shows the circuit example of disabling the IGBT temperature detection function. The TREF pin is connected to the VREG pin, and the voltage obtained by dividing the VREG output by the resistor is applied to the TEMPVL pin. For the TEMP1 and TEMP2 pins, the voltage obtained by dividing the VREG output by the resistor is applied so that the applied voltage may range between the TEMPVL pin voltage and VTEMPVH (3.8 V). The CTEMP pin is pulled down with about 100 ohms. In this case, the TEMPOUT pin output is fixed at the high level (VCC1).

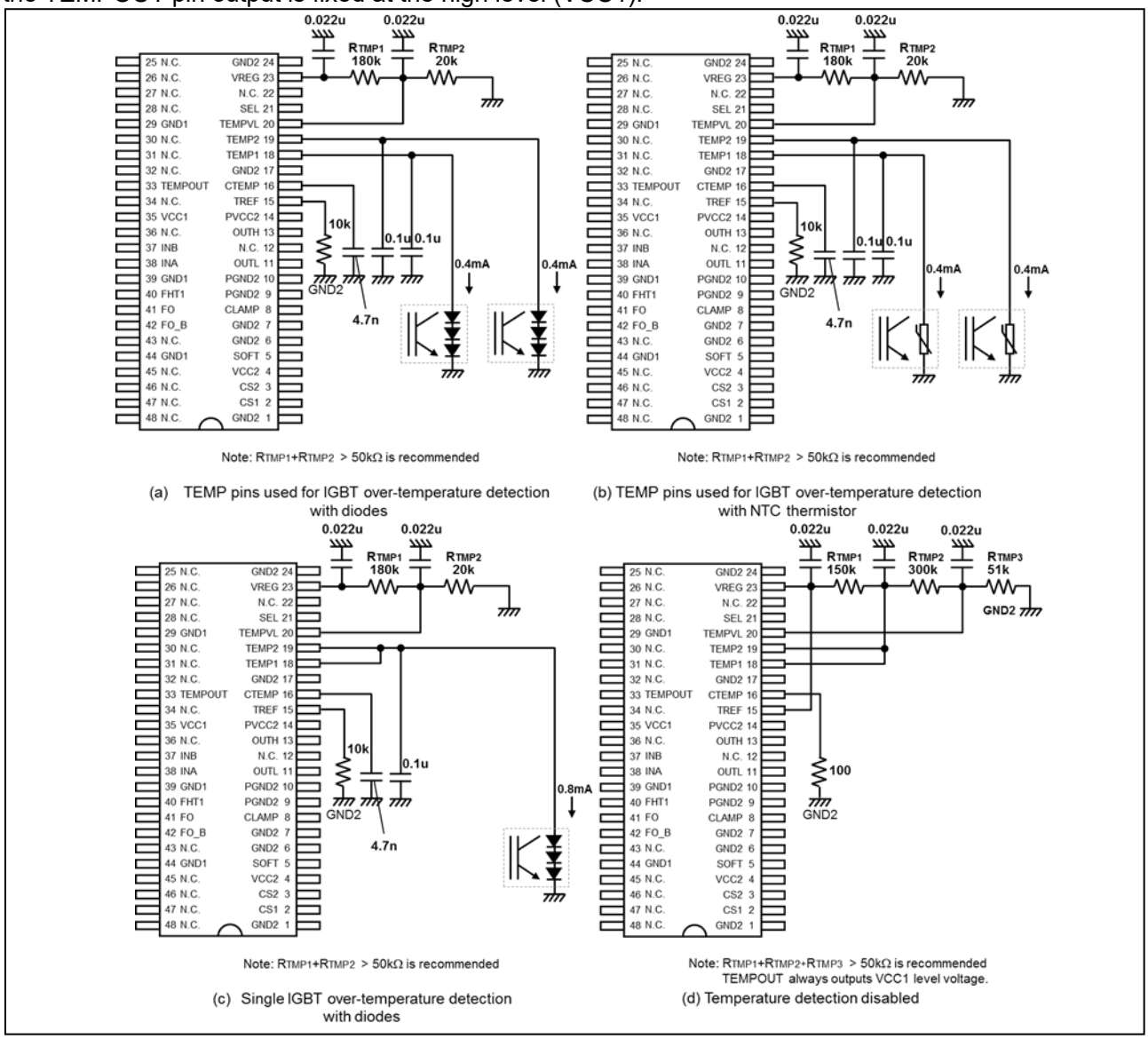


Figure 31: Circuit Examples of IGBT Temperature Sense Input

8.7 Circuit Examples of Fault Signal Output Hold Time Setting Pin

Figure 32 shows the circuit example of the control pin (FHT1) for fault hold time.

Figure 32 (a) shows the circuit example of setting the fault hold time. The fault hold time t_{FHT} is the time t_{FHT1} that is computed from 444 x 10^3 x C_{FHT1} [F] by the capacitor C_{FHT1} connected with the FHT1 pin. If C_{FHT1} is set to make t_{FHT1} less than 100 us, t_{FHT} is fixed at 100 us.

Figure 32 (b) shows that nothing is connected with the FHT1 pin. When the FHT1 pin is not used, it should be open or pulled up to the 5 V power supply via the resistor. The fault hold time is set to 100 us by the timer inside the IC.

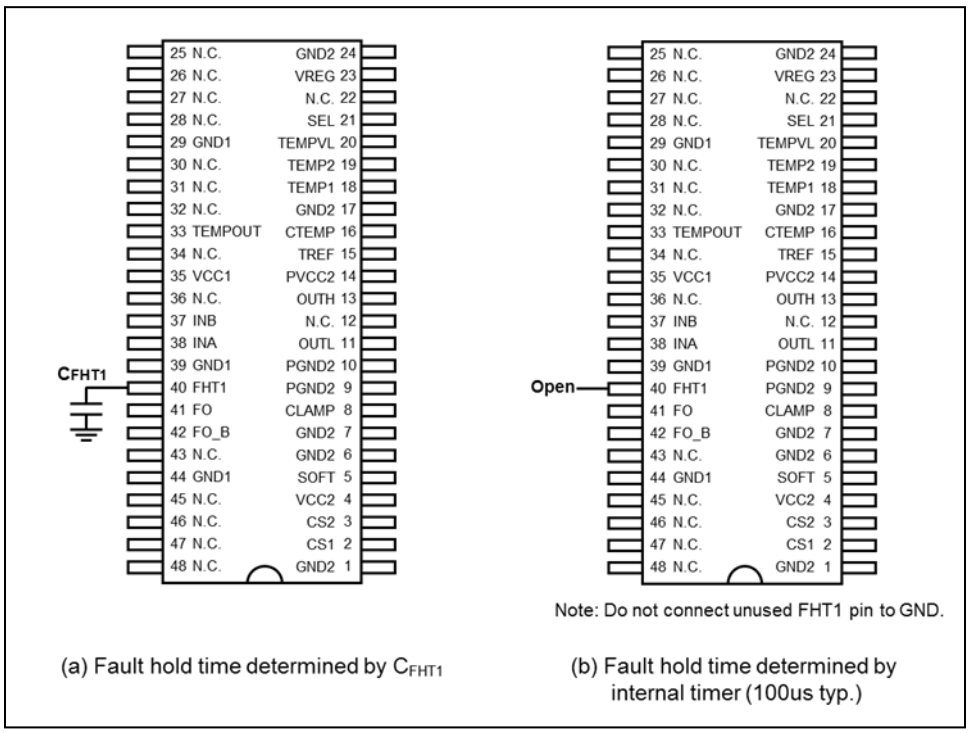


Figure 32: Circuit Examples of Fault Signal Output Hold Time Setting Pin

8.8 Circuit Examples of Fault Signal Output Pins

Figure 33 shows circuit examples of fault output pins. Each fault output pin of FO and FO_B has an internal 100-kohm pulled-up resistor inside the IC, which enables a fault signal to be output without an external resistor as in figure 33 (a). However, it is recommended to externally connect a pull-up resistor with less than 100 k ohms as in figure 33 (b). Since the addition of a pull-up resister lowers the output impedance, the high level output voltage is more stable and the rise time of a fault signal is reduced. Because the FO_B pin outputs the low level at the occurrence of a fault, FO_B is useful for connecting fault output pins of multiple ICs in parallel as in figure 33 (c). In this case, the fault bus is in the high level when all the ICs are operating normally and in the low level when a fault signal is output from one or more IC(s).

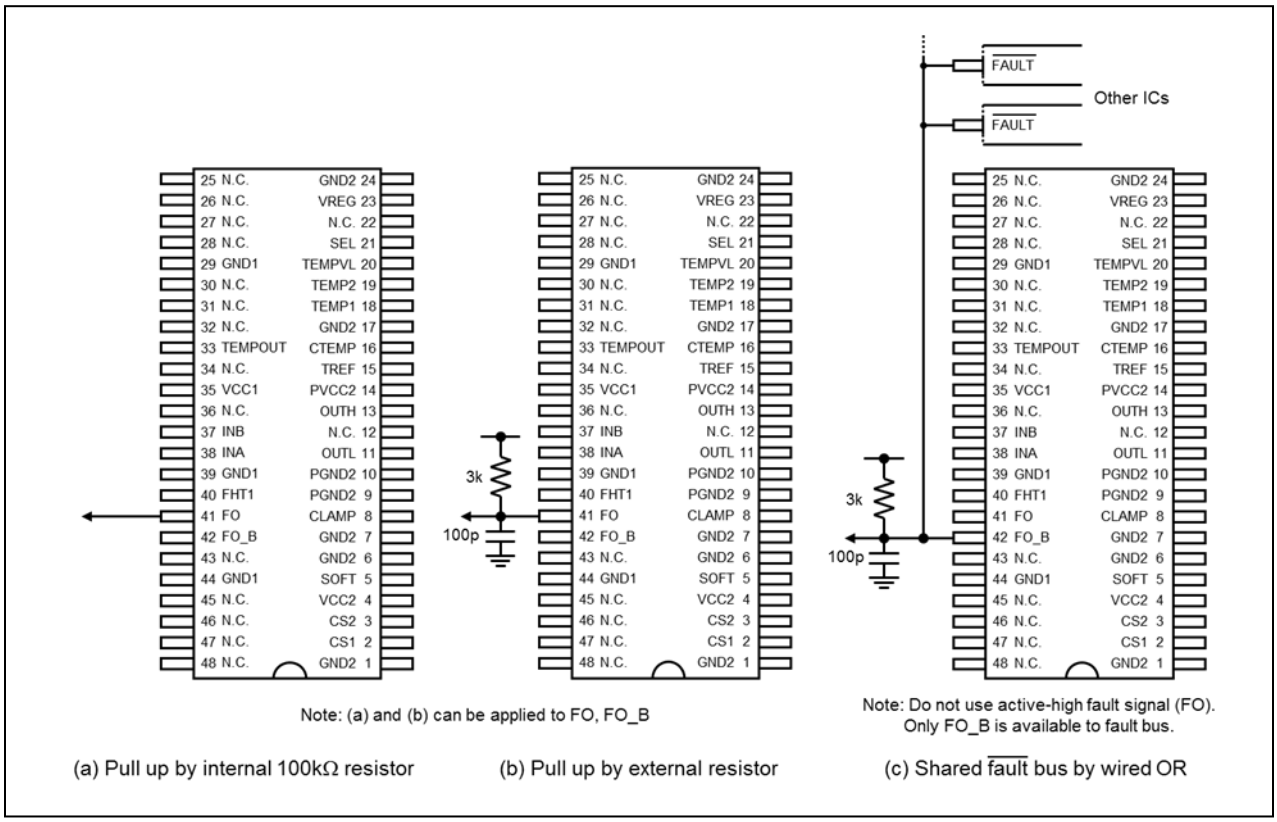
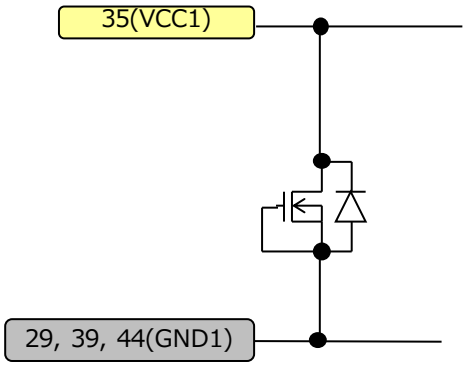


Figure 33: Circuit Examples of Fault Signal Output Pins

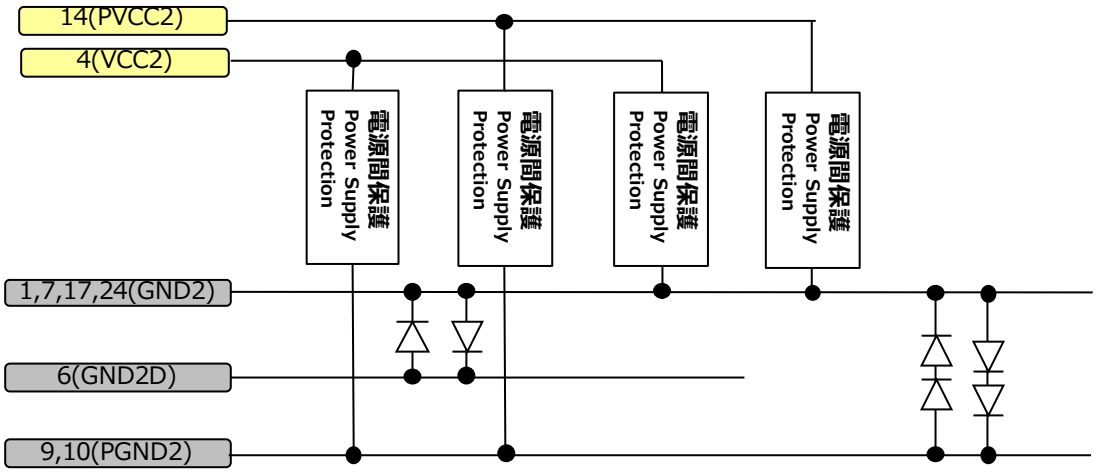
9. 端子等価回路図 (Equivalent Circuit of terminals)

9.1 電源系(Power Supply)

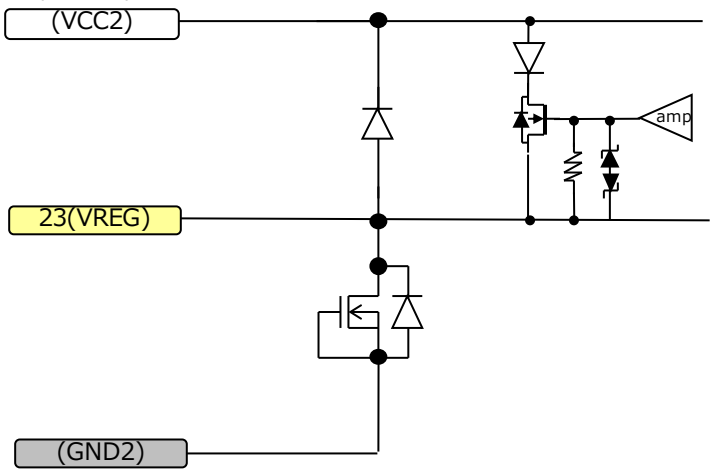
35(VCC1)



4(VCC2),14(PVCC2)

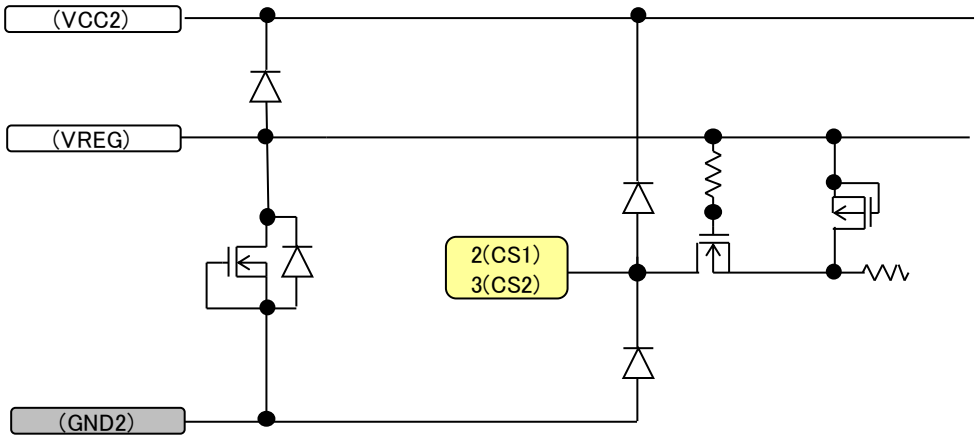


23(VREG)

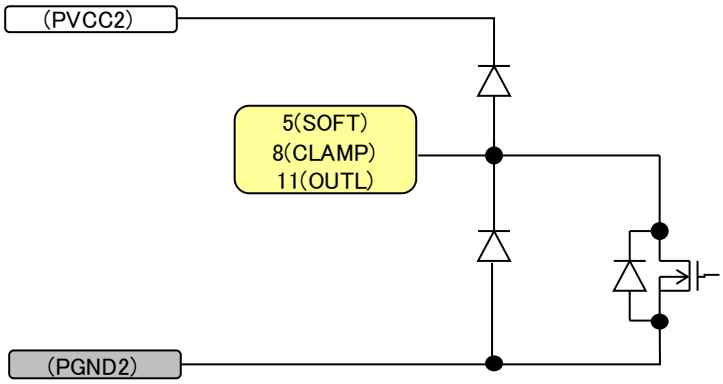


9.2 I/O 系(Input/Output)

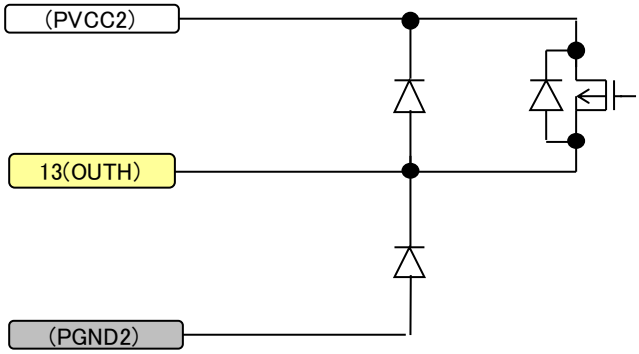
2(CS1), 3(CS2)



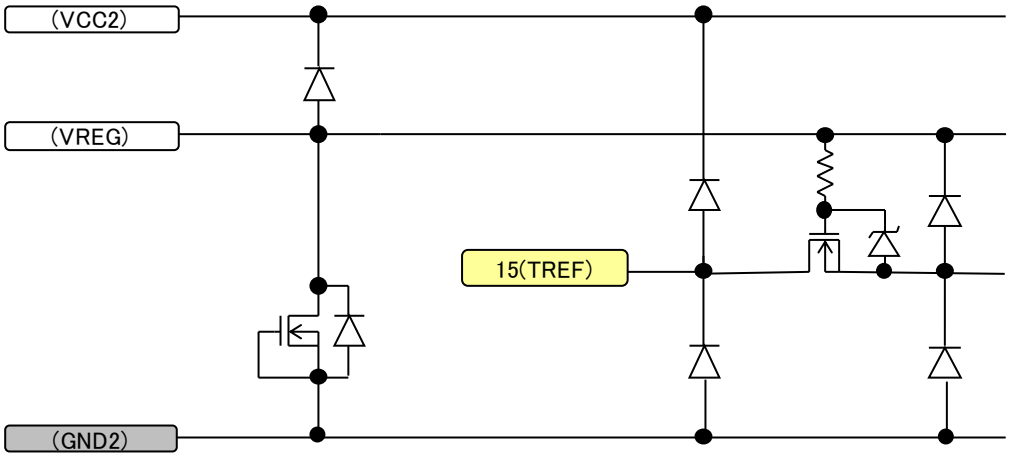
5(SOFT)、8(CLAMP)、11(OUTL)



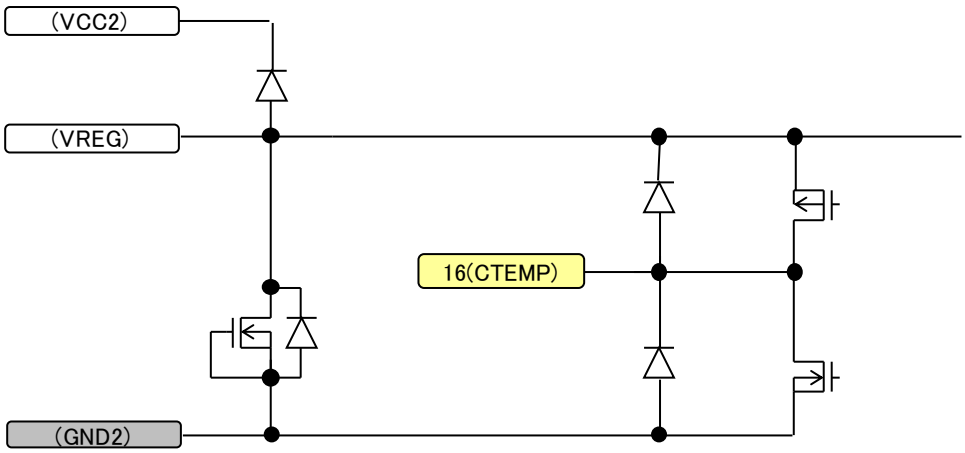
13 (OUTH)



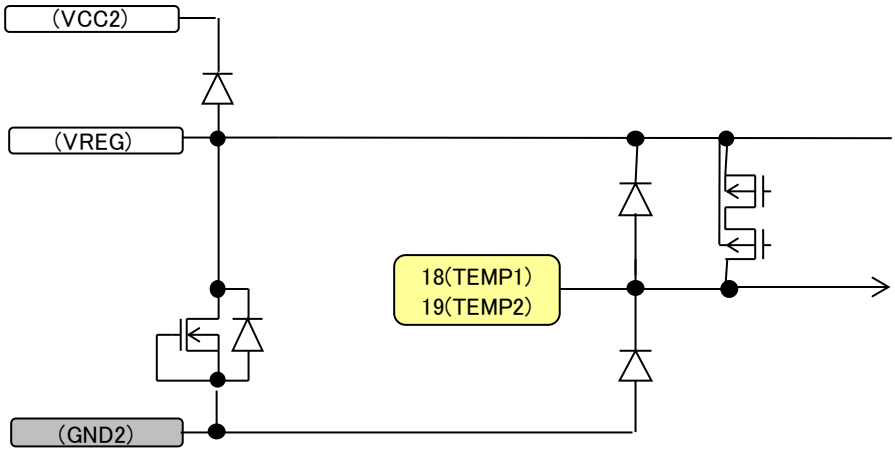
15(TREF)



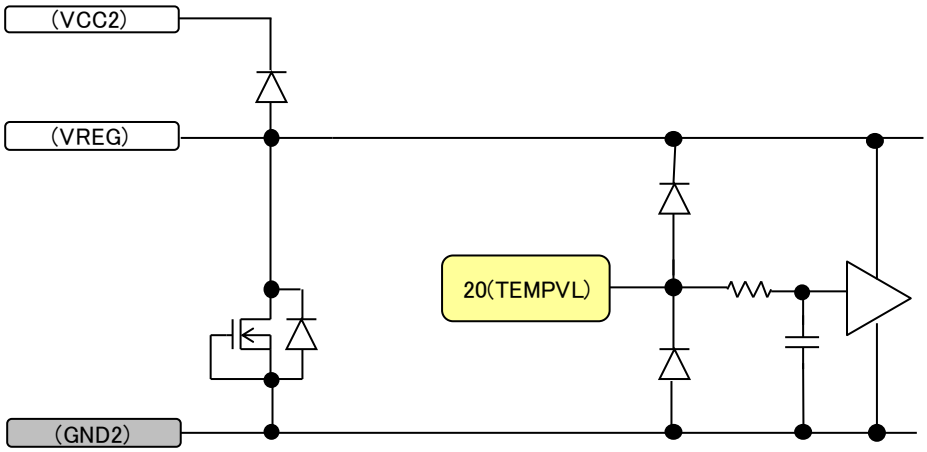
16 (CTEMP)



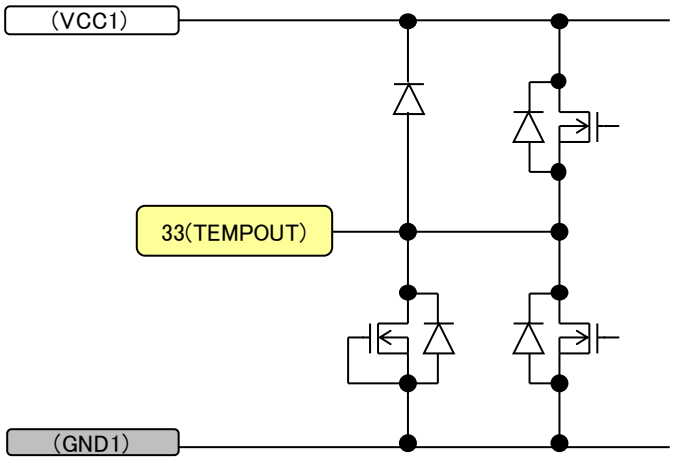
18(TEMP1)、19 (TEMP2)



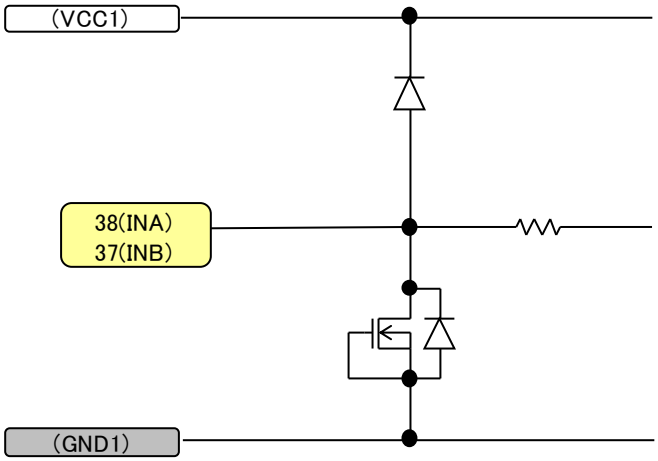
20 (TEMPVL)



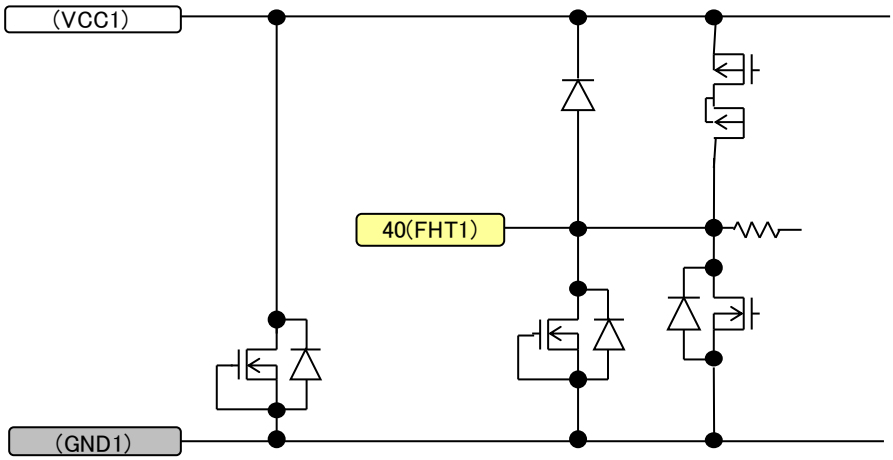
33 (TEMPOUT)



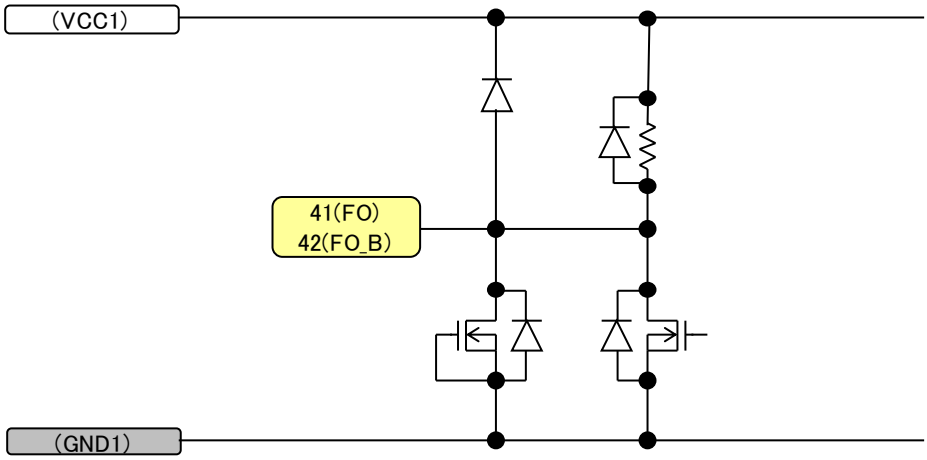
37 (INB)、38 (INA)



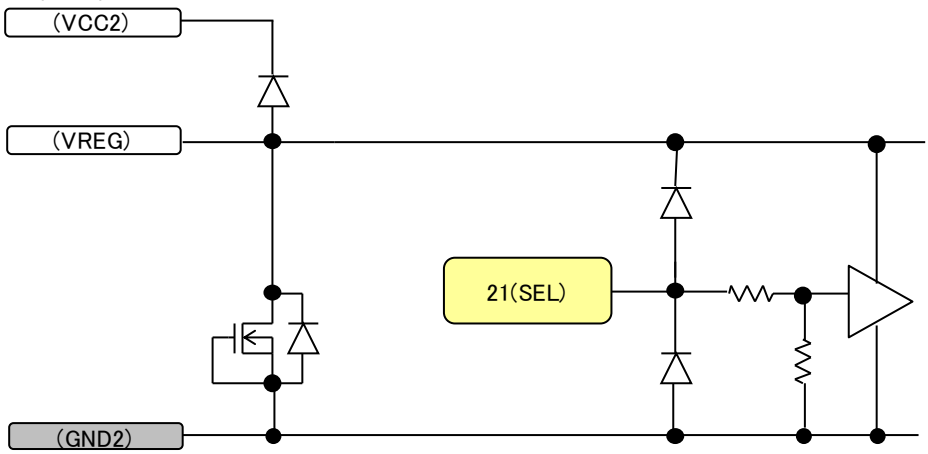
40 (FHT1)



41 (FO) ,42(FO_B)



21(SEL)



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   高质量等级： 运输设备（汽车、火车、轮船等）、交通控制系统、防灾系统、预防犯罪系统以及安全设备等。
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6. 使用本文档中记载的瑞萨电子产品时，应在瑞萨电子指定的范围内，特别是在最大额定值、电源工作电压范围、移动电源电压范围、热辐射特性、安装条件以及其他产品特性的范围内使用。对于在上述指定范围之外使用瑞萨电子产品而产生的故障或损失，瑞萨电子不承担任何责任。
7. 虽然瑞萨电子一直致力于提高瑞萨电子产品的质量和可靠性，但是，半导体产品有其自身的具体特性，如一定的故障发生率以及在某些使用条件下会发生故障等。此外，瑞萨电子产品均未进行防辐射设计。所以请采取安全保护措施，以避免当瑞萨电子产品在发生故障而造成火灾时导致人身事故、伤害或损害的事故。例如进行软硬件安全设计（包括但不限于冗余设计、防火控制以及故障预防等）、适当的老化处理或其他适当的措施等。由于难于对微机软件单独进行评估，所以请用户自行对最终产品或系统进行安全评估。
8. 关于环境保护方面的详细内容，例如每种瑞萨电子产品的环境兼容性等，请与瑞萨电子的营业部门联系。使用瑞萨电子产品时，请遵守对管制物质的使用或含量进行管理的所有相应法律法规（包括但不限于《欧盟RoHS指令》）。对于因用户未遵守相应法律法规而导致的损害或损失，瑞萨电子不承担任何责任。
9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将本文档中记载的瑞萨电子产品或技术用于与军事应用或者军事用途有关的任何目的（如大规模杀伤性武器的开发等）。在将本文档中记载的瑞萨电子产品或技术进行出口时，应当遵守相应的出口管制法律法规，并按照上述法律法规所规定的程序进行。
10. 向第三方分销或处分产品或者以其他方式将产品置于第三方控制之下的瑞萨电子产品买方或分销商，有责任事先向上述第三方通知本文档规定的内容和条件；对于用户或第三方因非法使用瑞萨电子产品而遭受的任何损失，瑞萨电子不承担任何责任。
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