R2J20652ANP

Integrated Driver – MOS FET (DrMOS)

REJ03G1867-0300
Rev.3.00
Feb 26, 2010

Description

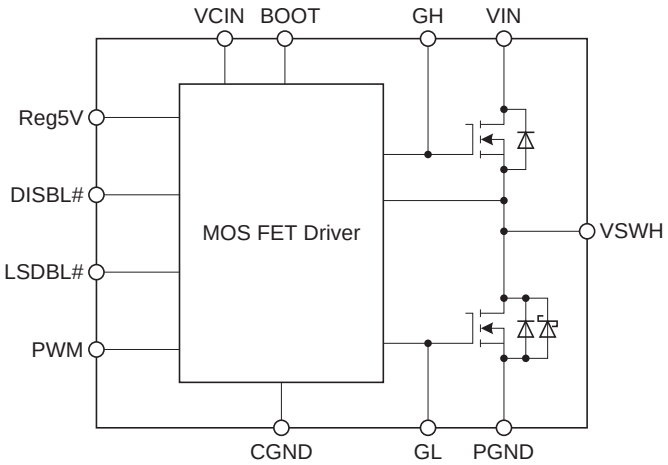
The R2J20652ANP multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. The on and off timing of the power MOS FET is optimized by the built-in driver, making this device suitable for large-current buck converters. The chip also incorporates a high-side bootstrap switch, eliminating the need for an external SBD for this purpose.

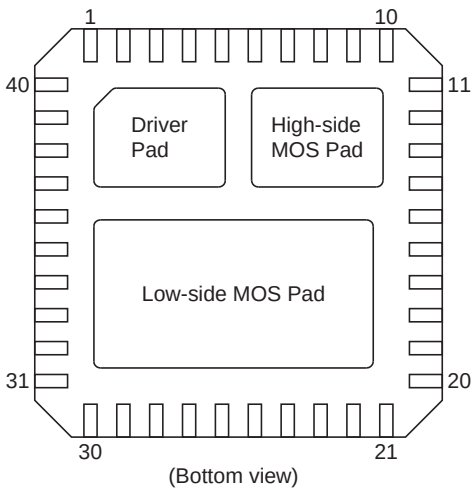
Features

- Based on Intel 6 × 6 DrMOS specification pin out
- Built-in power MOS FET suitable for Notebook, Desktop, Server application
- Low-side MOS FET with built-in SBD for lower loss and reduced ringing
- Built-in driver circuit which matches the power MOS FET
- Built-in tri-state input function which can support a number of PWM controllers
- VIN operating-voltage range: 27 V max
- High-frequency operation (above 1 MHz) possible
- Large average output current (Max. 35 A)
- Achieve low power dissipation
- Controllable driver: Remote on/off
- Low-side MOS FET disabled function for DCM operation
- Built-in bootstrapping switch
- Small package: QFN40 (6 mm × 6 mm × 0.95 mm)
- Terminal Pb-free/Halogen-free

Outline

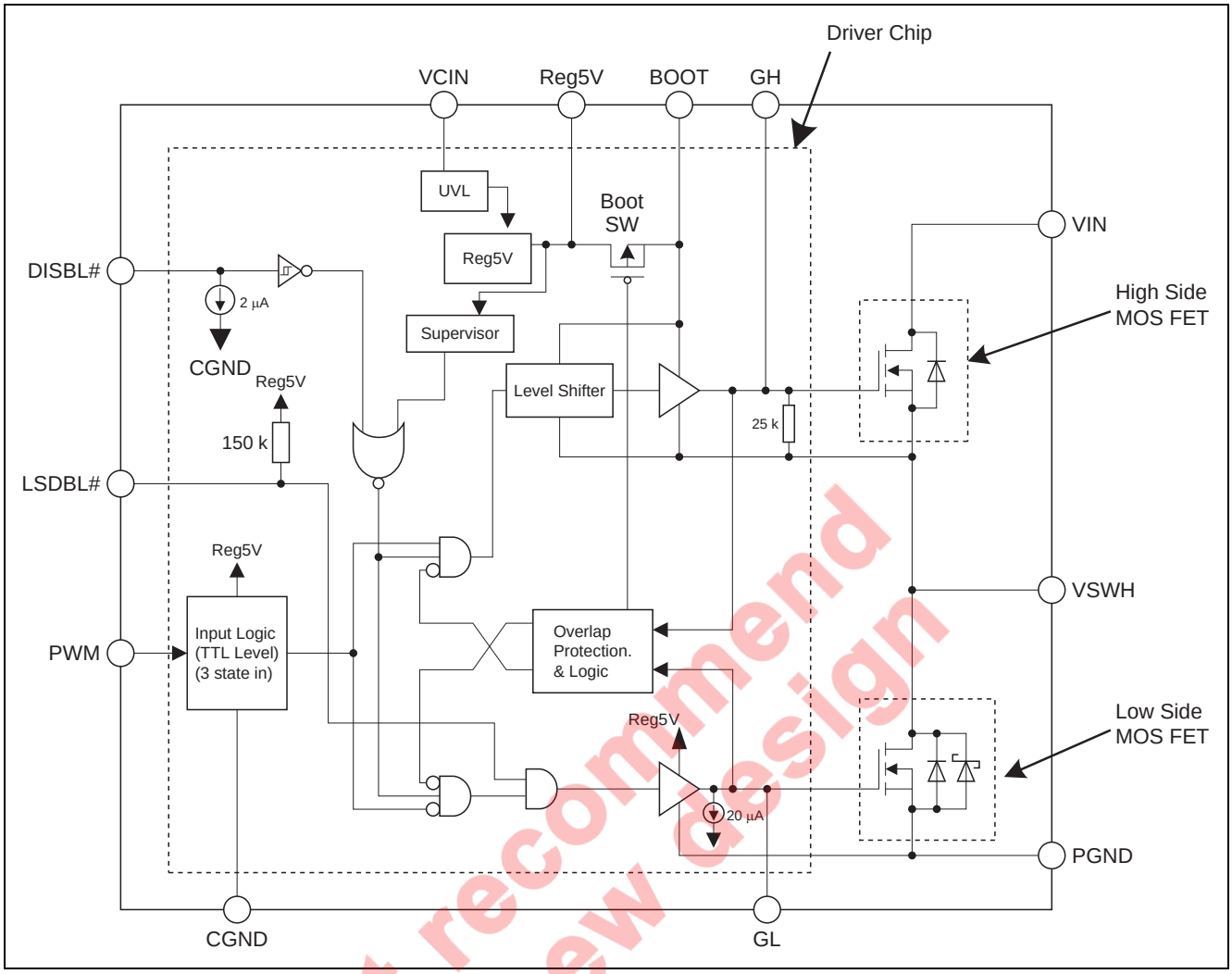
Integrated Driver-MOS FET (DrMOS)
QFN40 package 6 mm × 6 mm





(Bottom view)

Block Diagram



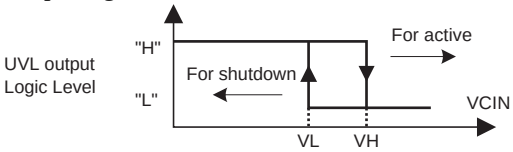
Notes: 1. Truth table for the DISBL# pin.

DISBL# Input	Driver Chip Status
"L"	Shutdown (GL, GH = "L")
"Open"	Shutdown (GL, GH = "L")
"H"	Enable (GL, GH = "Active")

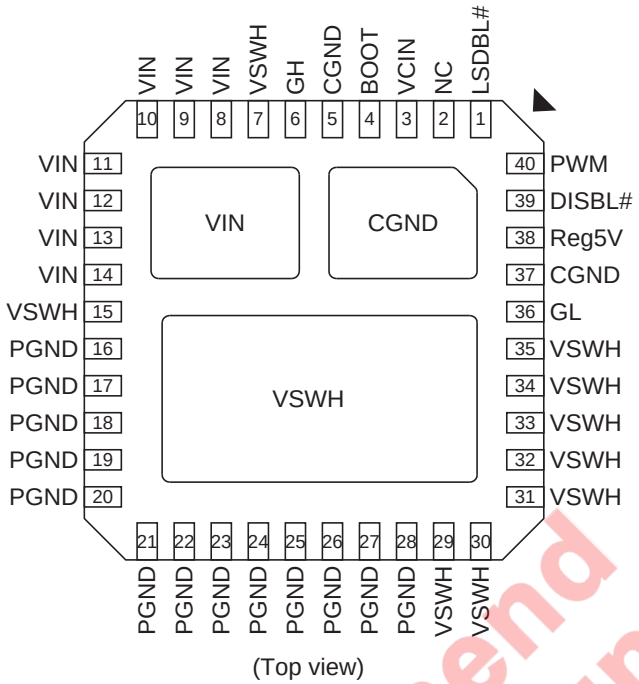
2. Truth table for the LSDBL# pin.

LSDBL# Input	GL Status
"L"	"L"
"Open"	"Active"
"H"	"Active"

3. Output signal from the UVL block



Pin Arrangement



(Top view)

Note: All die-pads (three pads in total) should be soldered to PCB.

Pin Description

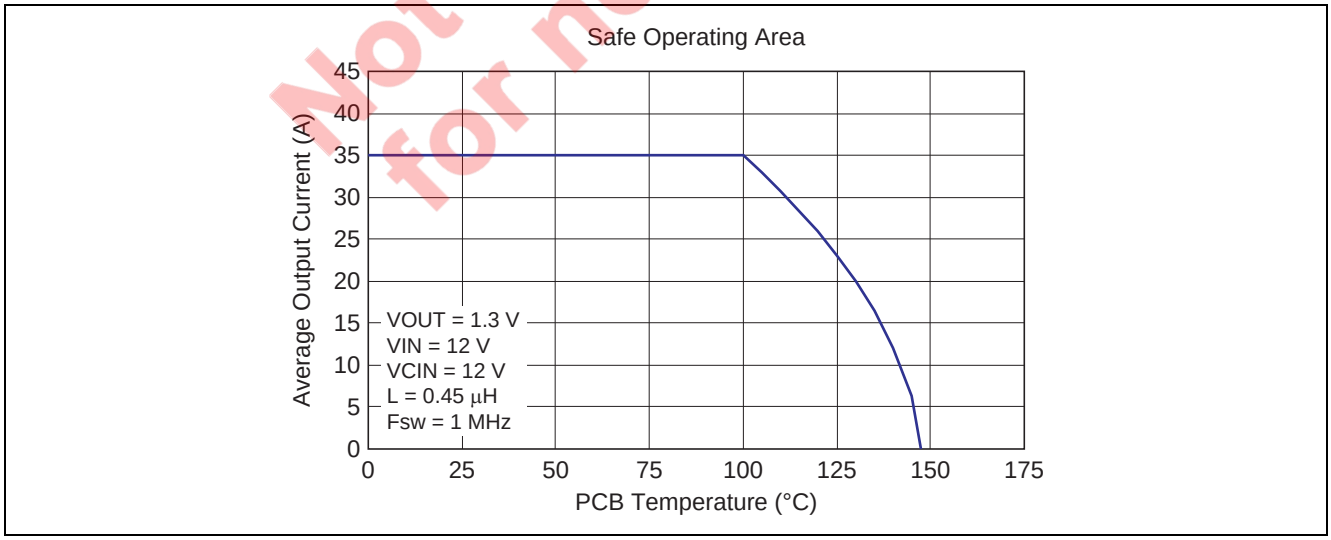
Pin Name	Pin No.	Description	Remarks
LSDBL#	1	Low-side gate disable	When asserted "L" signal, Low-side gate disable
NC	2	No connect	
VCIN	3	Control input voltage	Driver Vcc input
BOOT	4	Bootstrap voltage pin	To be supplied +5 V through internal switch
CGND	5, 37, Pad	Control signal ground	Should be connected to PGND externally
GH	6	High-side gate signal	Pin for Monitor
VIN	8 to 14, Pad	Input voltage	
VSWH	7, 15, 29 to 35, Pad	Phase output/Switch output	
PGND	16 to 28	Power ground	
GL	36	Low-side gate signal	Pin for Monitor
Reg5V	38	+5 V logic power supply output	
DISBL#	39	Signal disable	Disabled when DISBL# is "L"
PWM	40	PWM drive logic input	5 V logic input

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Units	Note
Power dissipation	Pt(25)	25	W	1
	Pt(110)	8		
Average output current	Iout	35	A	
Input voltage	VIN(DC)	–0.3 to +27	V	2
	VIN(AC)	30		2, 4, 6
Switch node voltage	VSWH(DC)	27	V	2
	VSWH(AC)	30		2, 4, 6
BOOT voltage	VBOOT(DC)	32	V	2
	VBOOT(AC)	36		2, 4, 6
Supply voltage	VCIN	–0.3 to +27	V	2
PWM voltage	Vpwm	–0.3 to +5.5 @UVL OFF –0.3 to +0.3 @UVL ON –0.3 to Reg5V + 0.3	V	2, 4 2, 5 2, 7, 8
Other I/O voltage	Vdisbl, Vlsdbl	–0.3 to VCIN + 0.3	V	2
Reg5V voltage	Vreg5V	–0.3 to +6	V	7
Reg5V current	Ireg5V	–20 to +0.1	mA	3
DISBL# current	Idisbl	0 to 1.0	mA	3
Operating junction temperature	Tj-opr	–40 to +150	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Pt(25) represents a PCB temperature of 25°C, and Pt(110) represents 110°C.
2. Rated voltages are relative to voltages on the CGND and PGND pins.
3. For rated current, (+) indicates inflow to the chip and (–) indicates outflow.
4. This rating is when UVL (Under Voltage Lock out) is ineffective (normal operation mode).
5. This rating is when UVL (Under Voltage Lock out) is effective (lock out mode).
6. The specification values indicated "AC" are limited within 100 ns.
7. This rating is when the external power-source is applied to Reg5V pin.
8. Reg5V + 0.3 V < 6 V



Recommended Operating Condition

Item	Symbol	Rating	Units	Note
Input voltage	VIN	4.5 to 22	V	When the usage of VCIN = 4.5 V to 5.5 V, VCIN should be connected to Reg5V (Refer to "Pin Connection")
Supply voltage	VCIN	4.5 to 5.5 or 8 to 22	V	

Electrical Characteristics

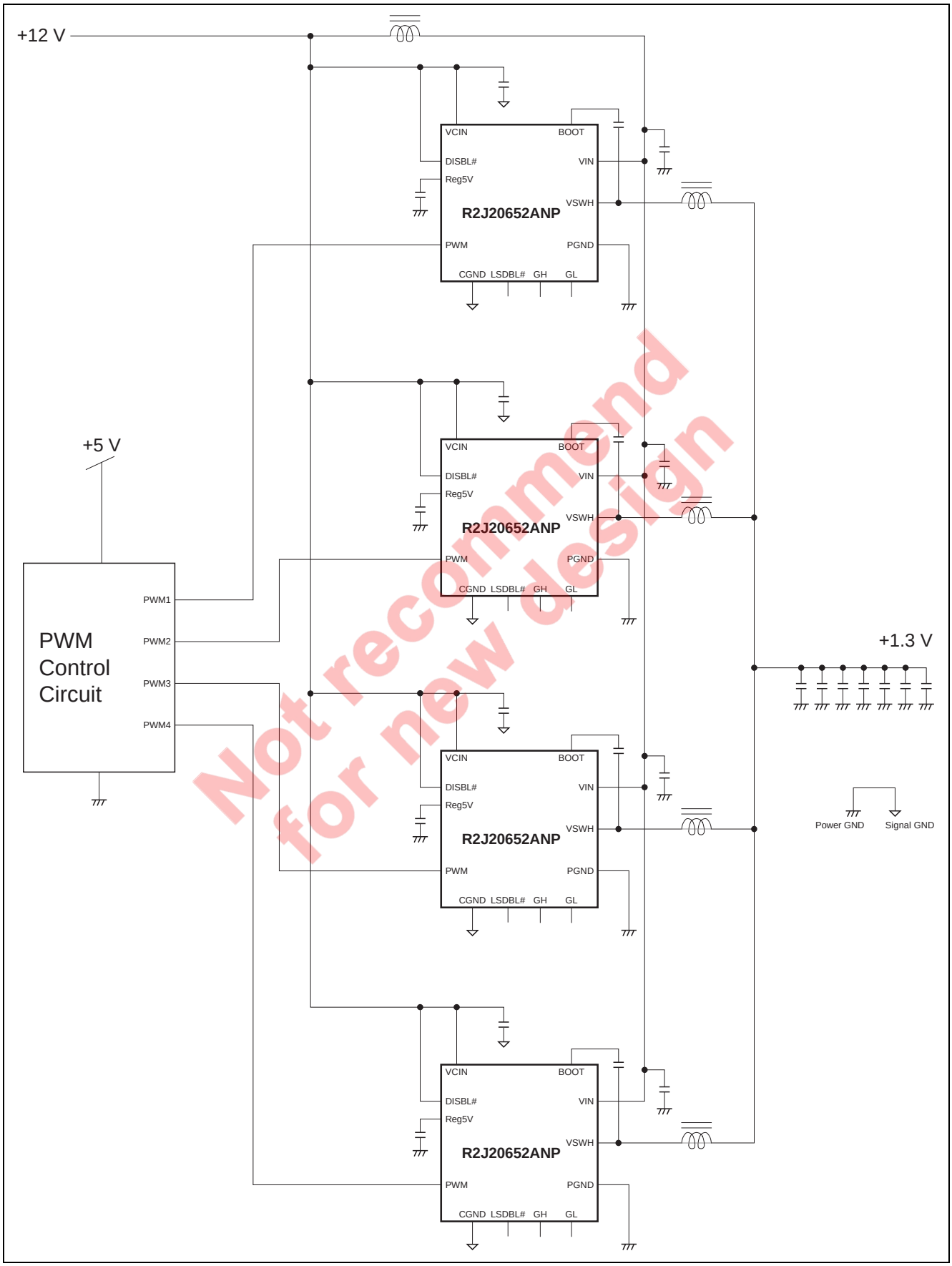
(Ta = 25°C, VCIN = 12 V, VSWH = 0 V, unless otherwise specified)

Item		Symbol	Min	Typ	Max	Units	Test Conditions
Supply	VCIN start threshold	V_H	7.0	7.4	7.8	V	
	VCIN shutdown threshold	V_L	6.6	7.0	7.4	V	
	UVLO hysteresis	dUVL	—	0.4	—	V	$V_H - V_L$
	VCIN operating current	I_{CIN}	—	34	—	mA	f_{PWM} = 1 MHz, Ton_pwm = 120 ns
	VCIN disable current	$I_{CIN-DISBL}$	—	—	2.5	mA	DISBL# = 0 V, PWM = 0 V, LSDBL# = Open
PWM input	PWM rising threshold	V_{H-PWM}	3.0	3.4	3.8	V	
	PWM falling threshold	V_{L-PWM}	0.9	1.2	1.5	V	
	PWM input resistance	R_{IN-PWM}	10	20	40	kΩ	PWM = 1 V
	Tri-state shutdown window	V_{IN-SD}	V_{L-PWM}	—	V_{H-PWM}	V	
	Shutdown hold-off time	$t_{HOLD-OFF}$ *1	—	100	—	ns	
5 V regulator	Output voltage	Vreg	4.95	5.2	5.45	V	
	Line regulation	Vreg-line	–10	0	10	mV	VCIN = 12 V to 16 V
	Load regulation	Vreg-load	–10	0	10	mV	Ireg = 0 to 10 mA
DISBL# input	Disable threshold	V_{DISBL}	0.9	1.2	1.5	V	
	Enable threshold	V_{ENBL}	1.9	2.4	2.9	V	
	Input current	I_{DISBL}	10	20	40	µA	DISBL# = 1 V
LSDBL# input	Low-side activation threshold	V_{LSDBLH}	1.9	2.4	2.9	V	
	Low-side disable threshold	V_{LSDBLL}	0.9	1.2	1.5	V	
	Input current	I_{LSDBL}	–56	–28	–14	µA	LSDBL# = 1 V

Note: 1. Reference values for design. Not 100% tested in production.

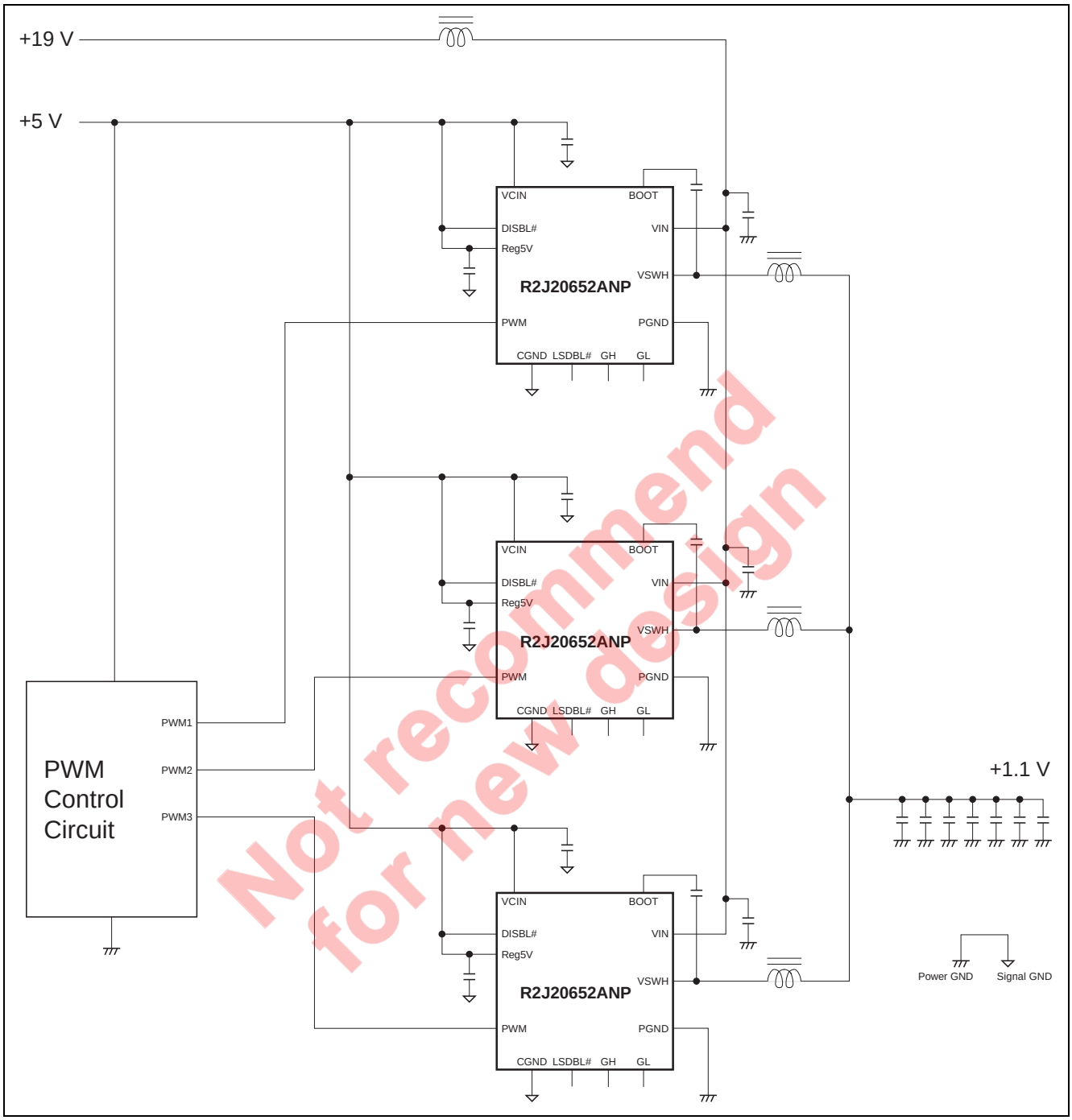
Typical Application

(1) Desktop/Server Application



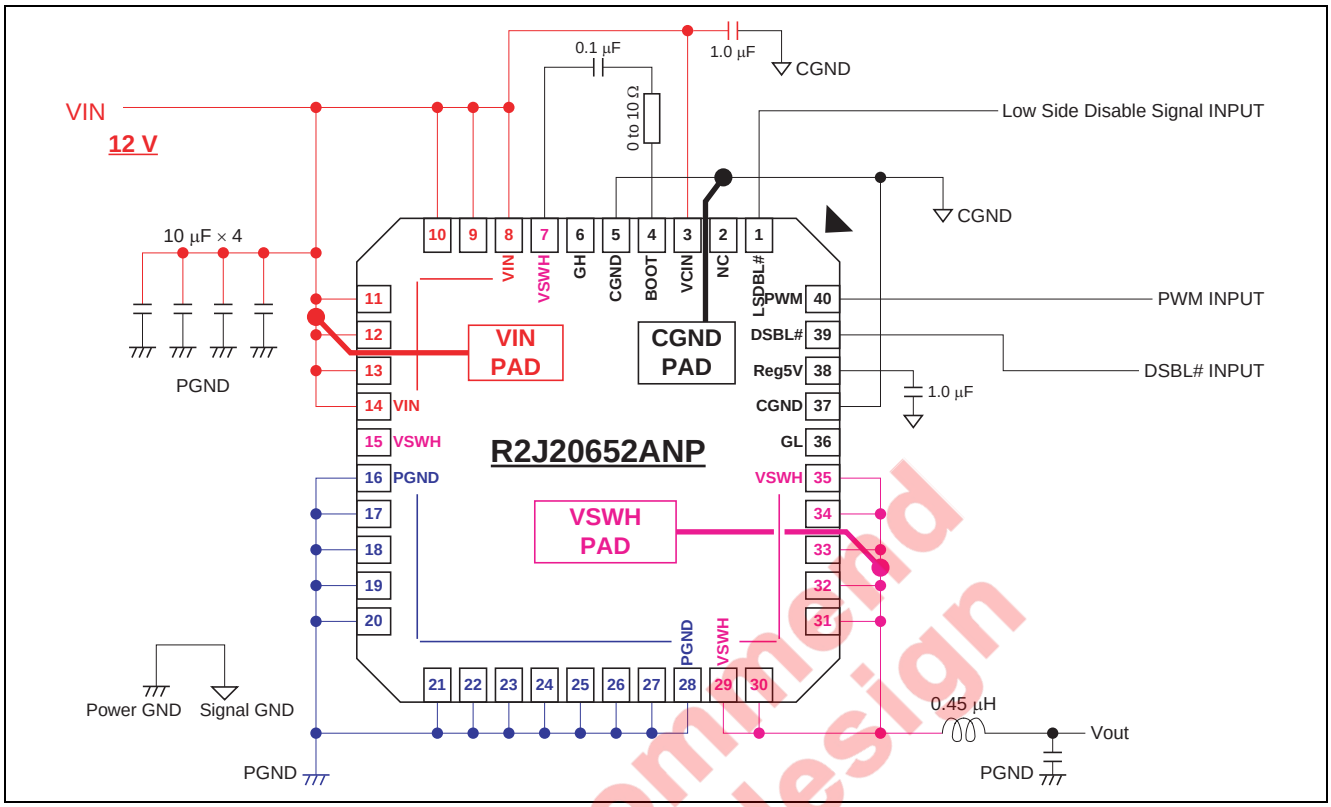
Typical Application (cont.)

(2) Notebook Application

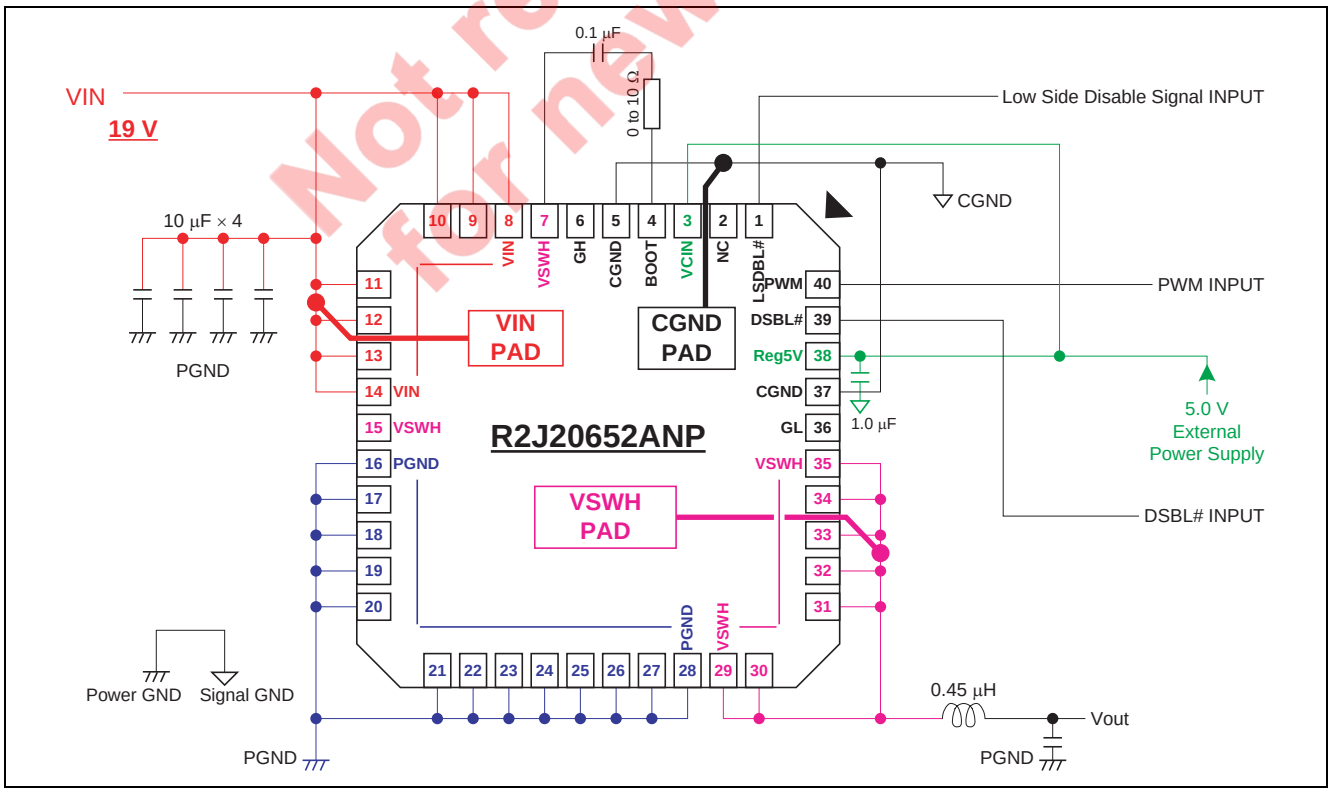


Pin Connection

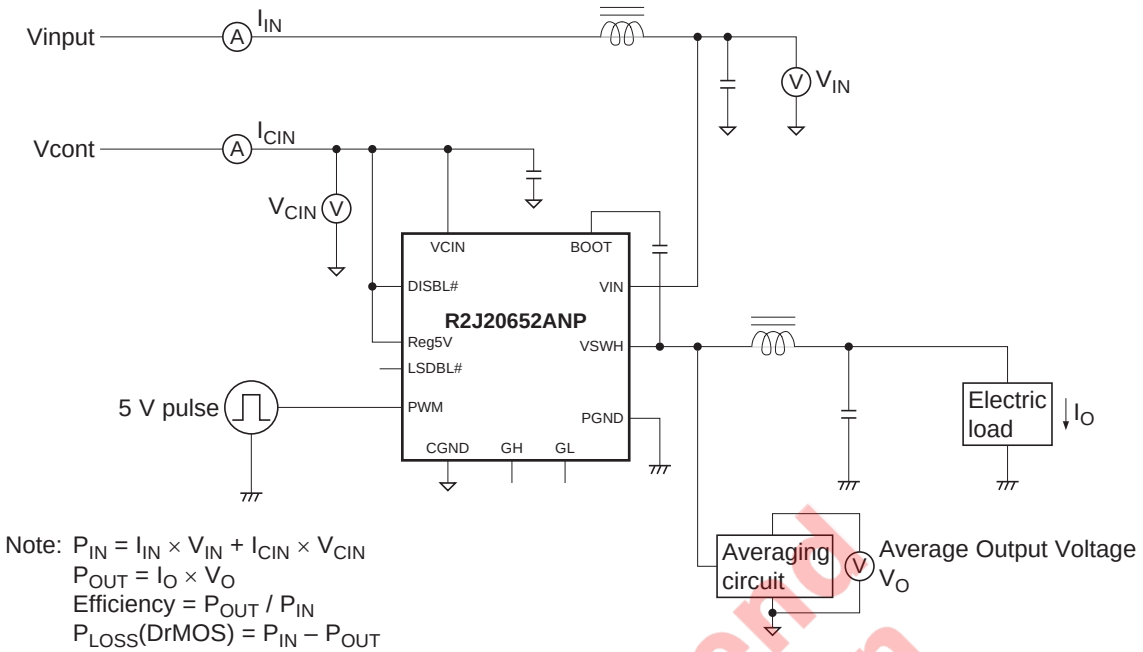
(1) Typical Desktop/Server Application



(2) Typical Notebook Application

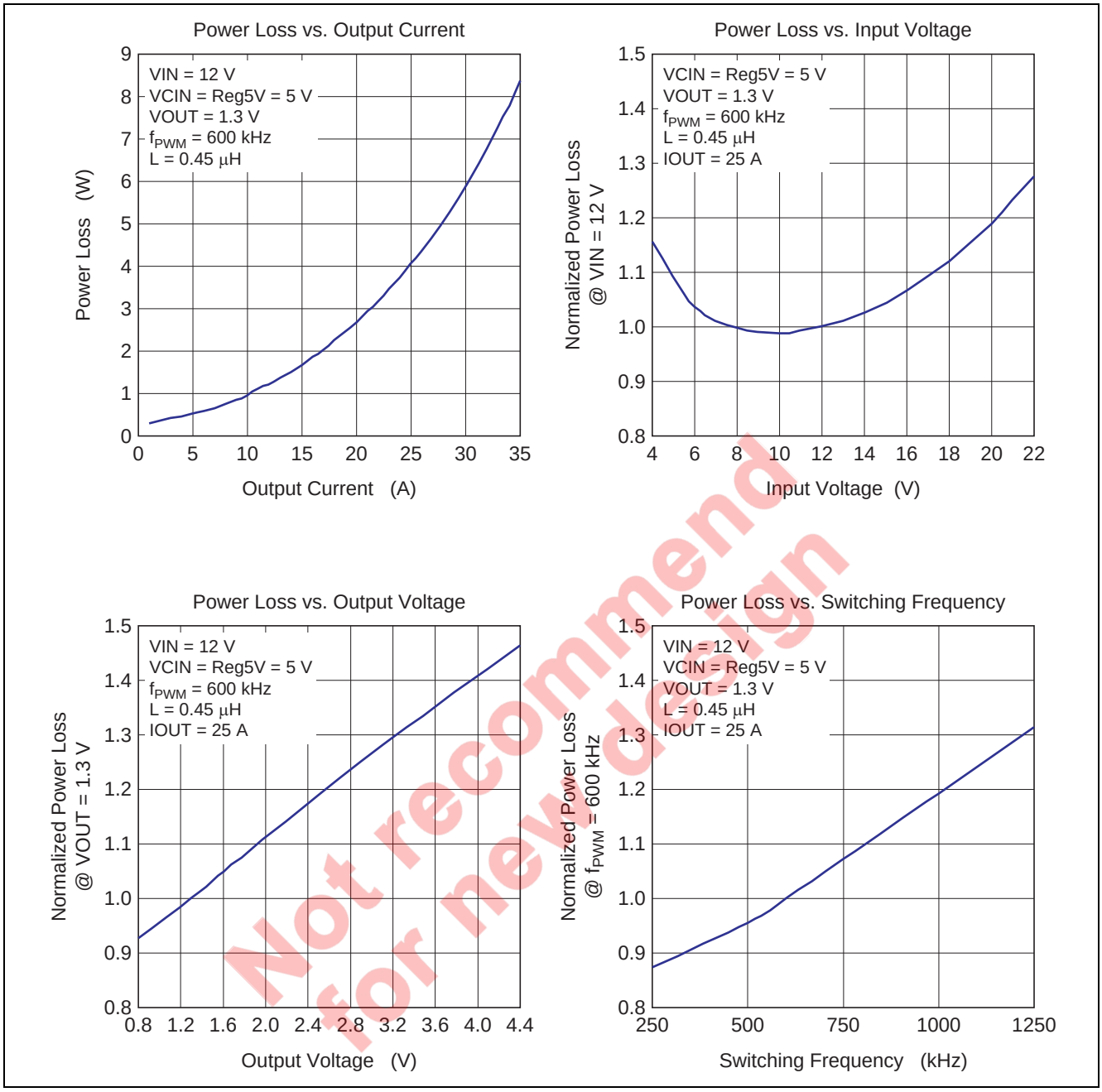


Test Circuit

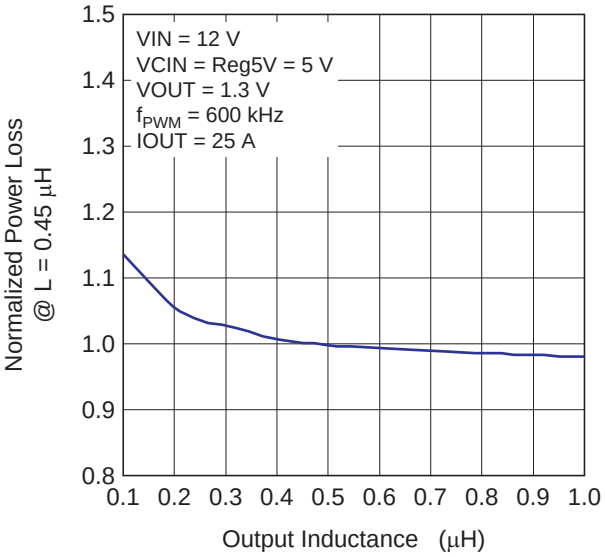


Note: $P_{IN} = I_{IN} \times V_{IN} + I_{CIN} \times V_{CIN}$
$P_{OUT} = I_O \times V_O$
Efficiency = P_{OUT} / P_{IN}
P_{LOSS}(DrMOS) = $P_{IN} - P_{OUT}$
Ta = 27°C

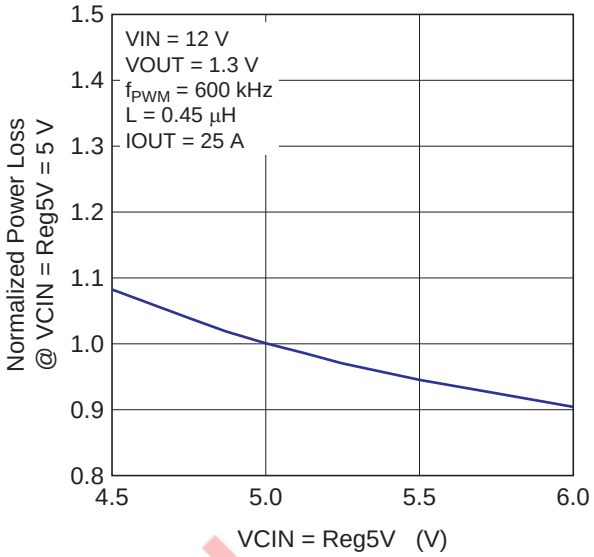
Typical Data



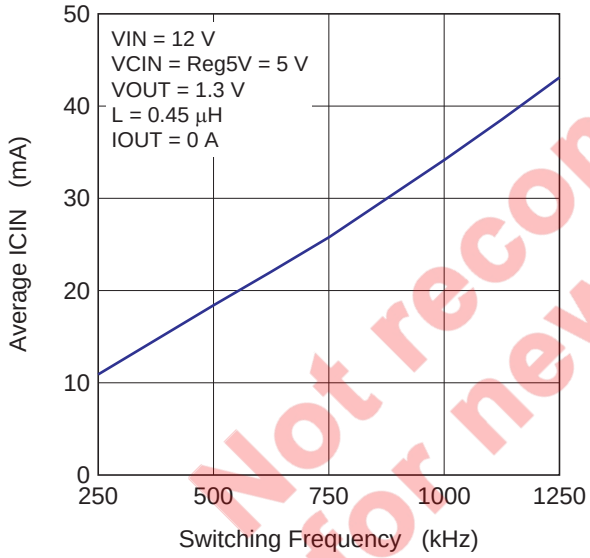
Power Loss vs. Output Inductance



Power Loss vs. VCIN



Average ICIN vs. Switching Frequency



Description of Operation

The DrMOS multi-chip module incorporates a high-side MOS FET, low-side MOS FET, and MOS-FET driver in a single QFN package. Since the parasitic inductance between each chip is extremely small, the module is highly suitable for use in buck converters to be operated at high frequencies. The control timing between the high-side MOS FET, low-side MOS FET, and driver is optimized so that high efficiency can be obtained at low output-voltage.

VCIN & DISBL#

The VCIN pin is connected to the UVL (under-voltage lockout) module, so that the built-in 5 V regulator is disabled as long as VCIN is 7.4 V or less. On cancellation of UVL, the built-in 5 V regulator remains enabled until the UVL input is driven to 7.0 V or less.

The built-in 5 V regulator is a series regulator with temperature compensation. A ceramic capacitor with a value of 0.1 µF or more must be connected between the CGND plane and the Reg5V Pin.

The output of 5 V regulator is monitored by the internal Supervisor circuits. When the Supervisor detects this output is more than 4.2 V (typ.), the driver state becomes active (figure1.1).

Figure 1.2 shows the application when the external 5 V regulator is used. When the Reg5V pin is applied into external 5 V, the Supervisor can activate the driver. In this application usage, VCIN should be connected to Reg5V.

The signal on pin DISBL# also enables or disables the circuit. When UVL disables the circuit, the built-in 5 V regulator does not operate, but when the signal on DISBL# disables the circuit, only output-pulse generation is terminated, and the 5 V regulator is not disabled.

Voltages from –0.3 V to VCIN + 0.3 V can be applied to the DISBL# pin, so on/off control by a logic IC or the use of a resistor, etc., to pull the DISBL# line up to VCIN are both possible.

VCIN	DISBL#	REG5V	Driver State
L	*	0	Disable (GL, GH = L)
H	L	Active	Disable (GL, GH = L)
H	H	Active	Active
H	Open	Active	Disable (GL, GH = L)

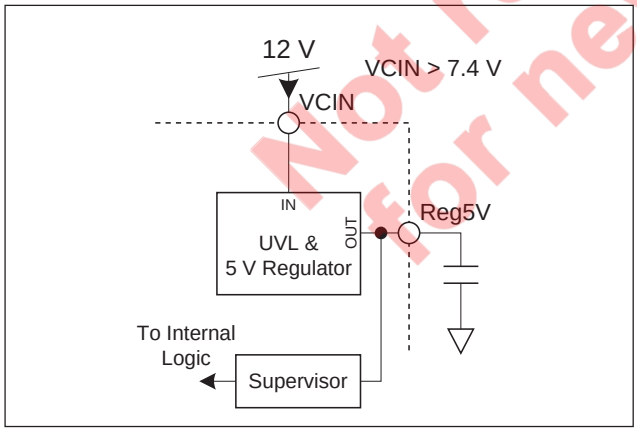


Figure 1.1 Typical 12 V Input Application (Activate Built-in 5 V Regulator)

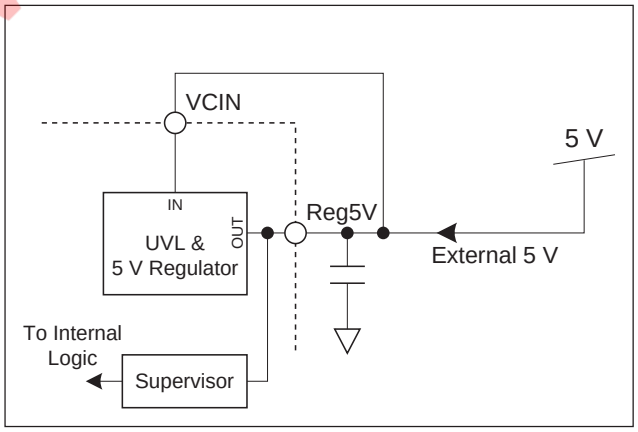


Figure 1.2 External 5 V Application

PWM & LSDBL#

The PWM pin is the signal input pin for the driver chip. When the PWM input is high, the gate of the high-side MOS FET (GH) is high and the gate of the low-side MOS FET (GL) is low.

PWM	GH	GL
L	L	H
H	H	L

The LSDBL# pin is the Low Side Gate Disable pin for "Discontinuous Conduction Mode (DCM)" when LSDBL# is low.

Figure 2 shows the Typical high-side and low-side gate switching and Inductor current (IL) during "Continuous Conduction Mode (CCM)" and low-side gate disabled when asserting LSDBL# signal.
This pin is internally pulled up to Reg5V with 150 kΩ resistor.

When low-side disable function is not used, keep this pin open or pulled up to VCIN.

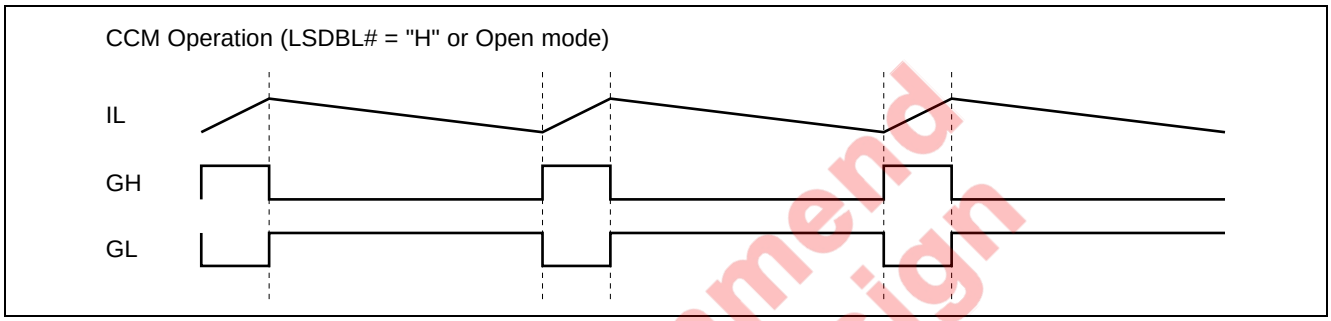


Figure 2.1 Typical Signals during CCM

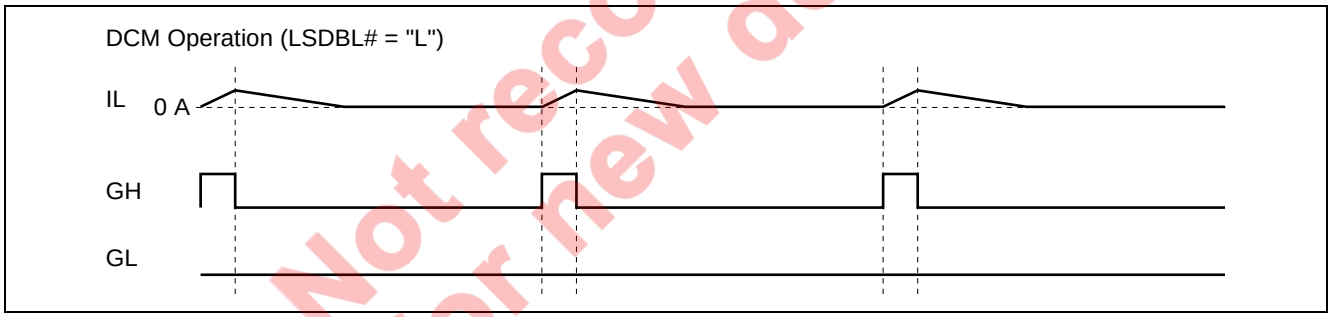


Figure 2.2 Typical Signals during DCM

The PWM input is TTL level and has hysteresis. When the signal route from the control IC is high impedance, the tri-state function turns off the high- and low-side MOS FETs. This function operates when the PWM input signal stays in the input hysteresis window for 100 ns (typ.). After the tri-state mode has been entered and GH and GL have become low, a PWM input voltage of 3.4 V or more is required to make the circuit return to normal operation.

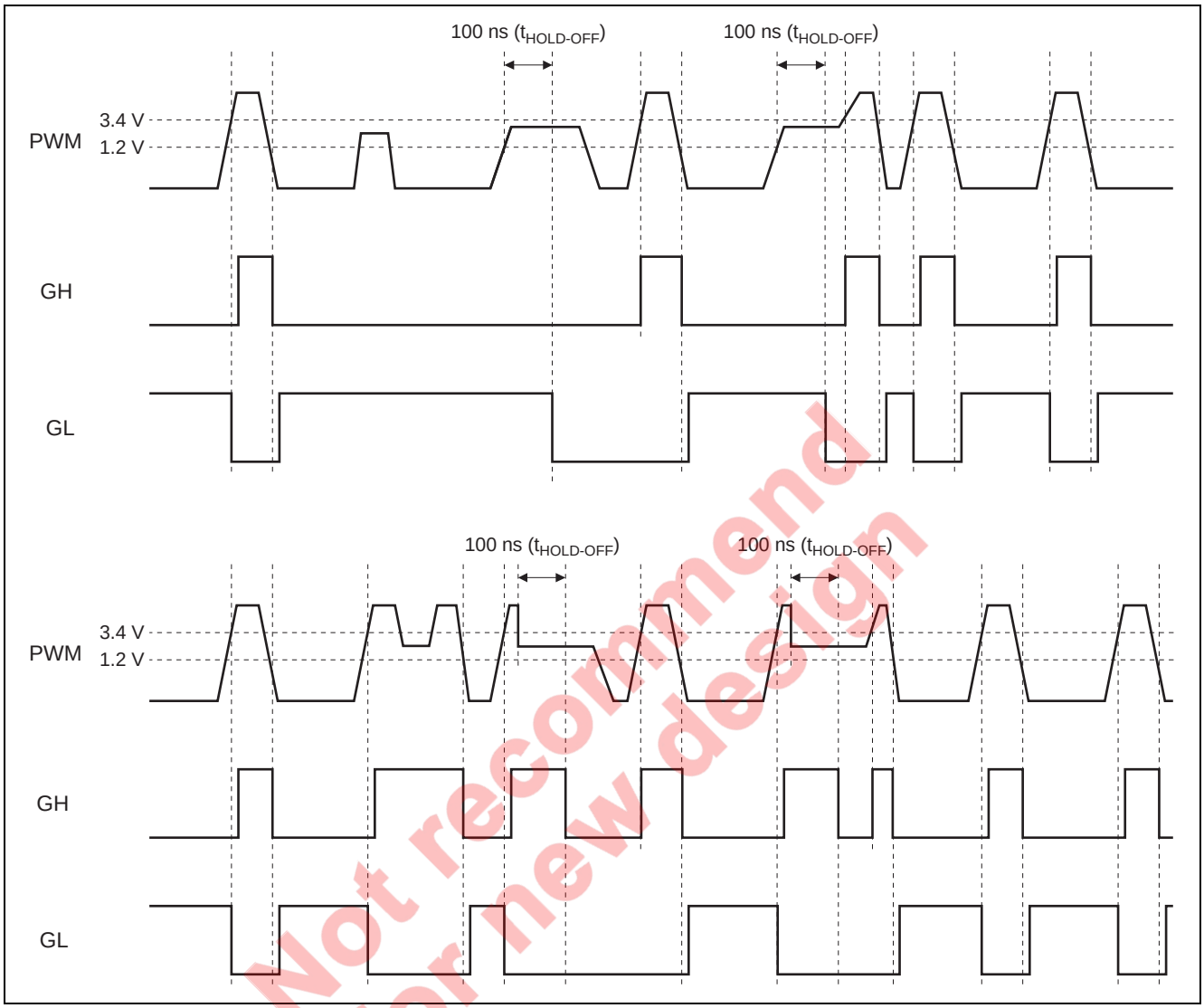


Figure 3 PWM Shutdown-Hold Time Signal

The equivalent circuit for the PWM-pin input is shown in the next figure. M1 is in the ON state during normal operation; after the PWM input signal has stayed in the hysteresis window for 100 ns (typ.) and the tri-state detection signal has been driven high, the transistor M1 is turned off.

When VCIN is powered up, M1 is started in the OFF state regardless of PWM Low or Open state. After PWM is asserted high signal, M1 becomes ON and shifts to normal operation.

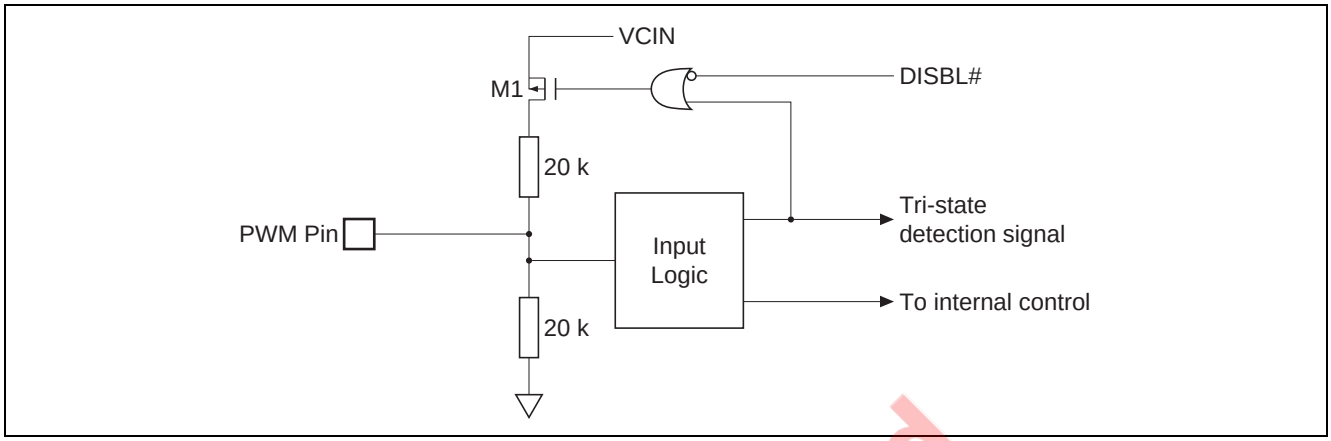


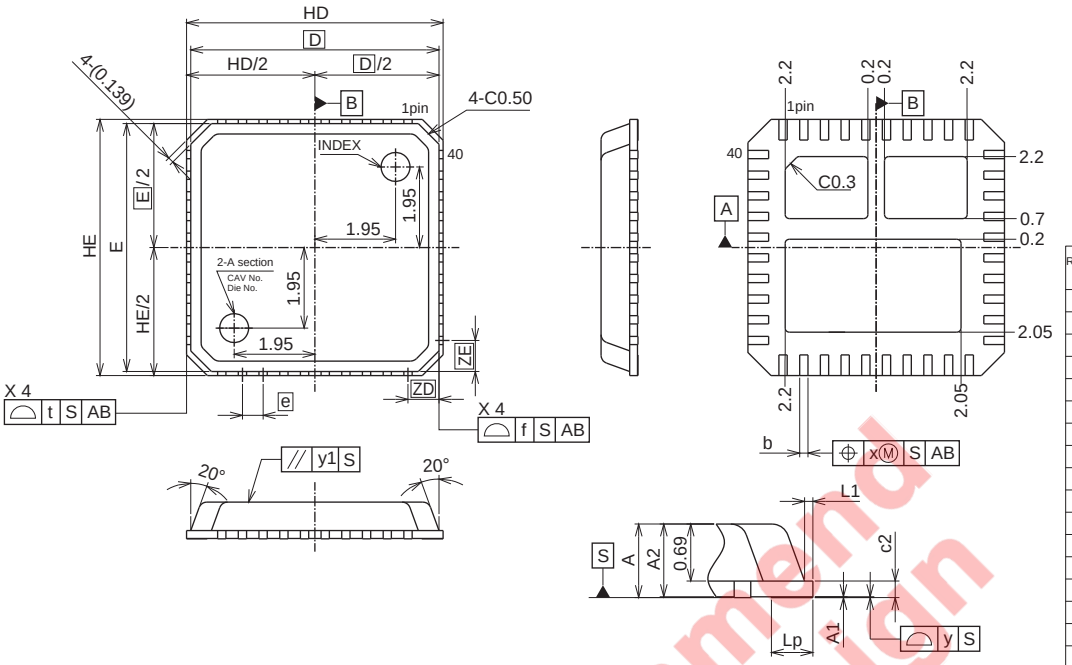
Figure 4 Equivalent Circuit for the PWM-pin Input

MOS FETs

The MOS FETs incorporated in R2J20652ANP are highly suitable for synchronous-rectification buck conversion. For the high-side MOS FET, the drain is connected to the VIN pin and the source is connected to the VSWH pin. For the low-side MOS FET, the drain is connected to the VSWH pin and the source is connected to the PGND pin.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HVQFN40-p-0606-0.50	PVQN0040KC-A	—	—



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A2	0.87	0.89	0.91
f	—	—	0.20
A	0.865	0.91	0.95
A1	0.005	0.02	0.04
b	0.17	0.22	0.27
b1	0.16	0.20	0.24
e	—	0.50	—
Lp	0.40	0.50	0.60
x	—	—	0.05
y	—	—	0.05
y1	—	—	0.20
t	—	—	0.20
HD	6.15	6.20	6.25
HE	6.15	6.20	6.25
ZD	—	0.75	—
ZE	—	0.75	—
L1	0.06	0.10	0.14
c1	0.17	0.20	0.23
c2	0.17	0.22	0.27

Ordering Information

Part Name	Quantity	Shipping Container
R2J20652ANP#G3	2500 pcs	Taping Reel

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