RAA211233

24V, 3A 1.4MHz Integrated Switching Regulator

The RAA211233 is an integrated 24V, 3A, 1.4MHz synchronous buck regulator with current mode constant on-time (COT) control. The RAA211233 features comprehensive protection including input undervoltage lockout (UVLO), overcurrent protection (OCP), output undervoltage protection (OUVP), and over-temperature protection (OTP).

The device is available in a 6 Ld TSOT23 package.

Applications

- General purpose
- Industrial power supplies
- Embedded systems and I/O supplies

Features

- 4.5V to 24V input supply range
- Up to 3A output current
- Integrated high-side (85mΩ) and low-side (45mΩ) MOSFETs
- 1.4MHz switching frequency
- 400µA quiescent current
- Minimum on-time of 66ns
- Minimum off-time of 250ns
- 0.6V reference voltage with 2% accuracy
- PFM mode under light-load condition
- Current mode Constant On-Time (COT) control with internal compensation
- Internal 1.2ms soft-start time
- Protection: Low-Side Overcurrent (LSOC) limit, input Undervoltage Lockout (UVLO), Over-Temperature Protection (OTP), Output Undervoltage Protection (OUVP) with Hiccup Mode
- Accurate EN threshold
- 6 LD TSOT23 package

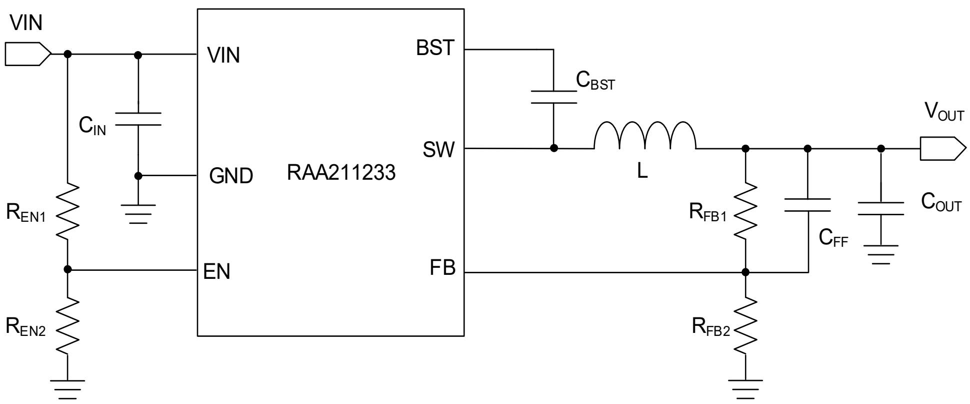


Figure 1. Typical Application Circuit Diagram

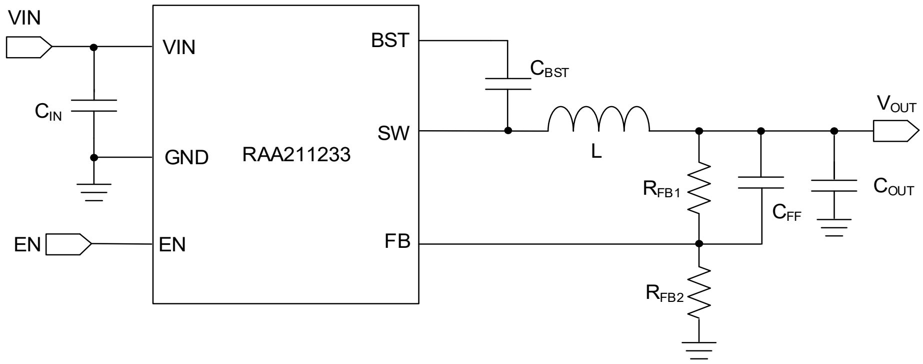


Figure 2. Typical Application Circuit Diagram with V_{IN} UVLO Programming by ENABLE

Table 1. Bill of Materials for Typical Application Circuit (3.3V V_{OUT})

Item	Qty	Reference	Value	Description	Part number
1	1	C_{IN}	10µF	CAP CER 10µF 35V X7R 1206	GMK316AB7106KL-TR
2	1	C_{OUT}	22µF	CAP CER 22µF 6.3V X7R 0805	GRM21BZ70J226ME44L
3	1	C_{BST}	0.1µF	CAP CER 0.1µF 10V X7R 0603	C0603C104K9RACTU
4	1	L_1	1.5µH	WE-MAPI SMD High Current Inductor, 1.5µH, 20%	74438356015
5	1	R_{FB1}	45.3K	1% resistor 0603	Generic
6	1	R_{FB2}	10K	1% resistor 0603	Generic
7		C_{FF}		DNP	

Contents

1. Overview

1.1 Block Diagram

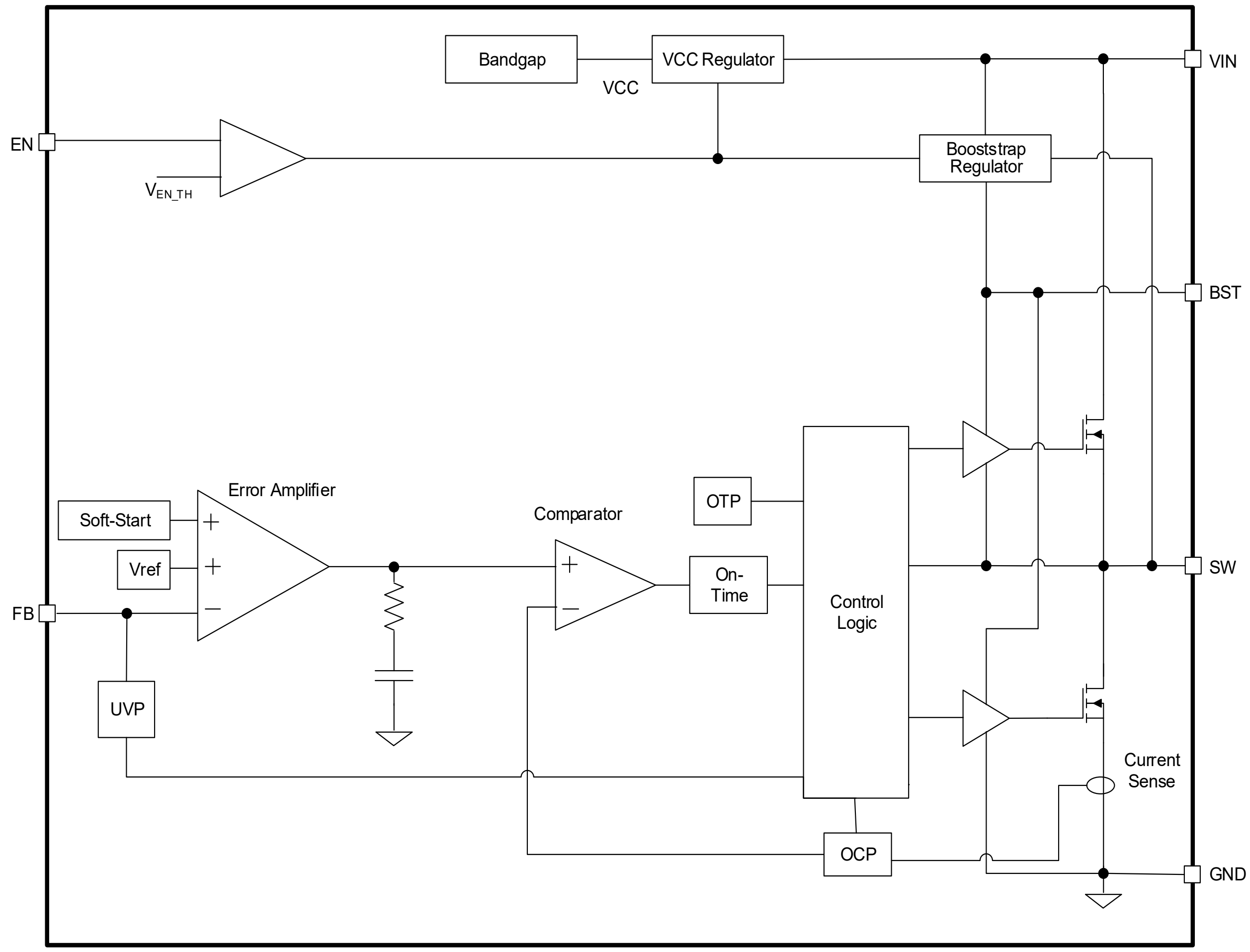


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

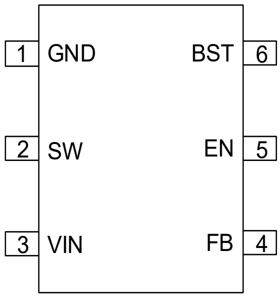


Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	GND	Ground
2	SW	Switch node pin. Connect this pin to the output inductor and bootstrap capacitor.
3	VIN	Voltage input for the IC. Connect to a suitable voltage source within the IC operating range to this pin. Place a ceramic capacitor from VIN to GND close to the IC for decoupling.
4	FB	Feedback input pin for the regulator. The output voltage is set by an external resistor divider connected to FB. FB voltage is 0.6V during normal operation.
5	EN	Accurate enable signal.
6	BST	Bootstrap supply pin. Connect a 0.1µF capacitor from BST to SW.

3. Specifications

3.1 Absolute Maximum Ratings

***Caution**:* Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN	-0.3	26	V
EN	-0.3	VIN + 0.3	V
SW	-0.7	VIN + 0.3	V
SW (20ns transient)	-3	VIN + 2	V
BST	-	SW + 5.5	V
All other pins	-0.3	5	V
Maximum Junction Temperature	-40	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human body model (HBM) (Tested per JS-001-2023)	-	2.5	kV
Charged Device Model (CDM) (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	6 Ld TSOT23	θ_{JA}[1]	Junction to ambient	105	°C/W
		θ_{JA_EVB}[2]	Junction to ambient on board.	51	
		θ_{JC}[3]	Junction to case	45	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. θ_{JA_EVB} is measured in free air with the component mounted on the RTKA211233DE0000BU evaluation board.
3. For θ_{JC}, the case temperature measurement location is the center of top of package.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage, V_{IN}	4.5	24	V
Output Voltage, V_{OUT}	0.6	11	V
Output Current, I_{OUT}	0	3	A
Junction Temperature, T_J	-40	+125	°C

3.4 Electrical Specifications

$T_A = T_J$ = -40°C to +125°C, V_{IN} = 12V, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Symbol	Test Conditions	Minimum[1]	Typical	Maximum[1]	Unit
Supply Voltage						
V_{IN} Voltage Range	V_{IN}	-	4.5	-	24	V
Quiescent Current	I_Q	EN = 2V, V_{FB} = 0.65V, no switching	-	400	-	µA
Shutdown Current	I_{SH}	EN = 0V, V_{IN} = 12, no switching	-	2	5	µA
V_{IN} Undervoltage Lockout	-	V_{IN} Rising	-	4.3	4.55	V
V_{IN} Undervoltage Hysteresis	-	V_{IN} Falling	-	400	-	mV
Output Voltage						
V_{OUT} Voltage Range	V_{OUT}	Subject to t_{OFF_MIN},t_{ON_MIN}	V_{FB}	-	11	V
Enable Voltage						
EN Threshold Voltage	VEN	EN rising	1.2	1.31	1.45	V
Enable Voltage Hysteresis	-	-	-	0.11	-	V
Enable Shutdown Threshold	VENL	-	-	0.69	-	V
EN Pin Resistance to GND	REN	VEN = 3V	-	1900	-	kΩ
Switching Frequency and Timer Control						
Switching Frequency Range	f_{SW}	V_{FB} = 0.6V, V_{OUT} = 1.05V, I_{OUT} = 1A, V_{IN} = 12V	-	1380	-	kHz
Minimum Off-Time	t_{OFF_MIN}	-	-	250	380	ns
Minimum On-Time	t_{ON_MIN}	-	-	66	-	ns
Internal Soft-Start Time	-	Measured at internal ref = V_{SS_done}	-	1.2	-	ms
Feedback Voltage						
Feedback Voltage Reference	V_{FB}	V_{IN} = 12V, EN = 2V	0.588	0.6	0.612	V
Feedback Voltage Line Regulation	-	-	-	±0.01	-	%/V
Internal Integrated MOSFETs						
High-Side On-Resistance	$r_{DS(ON)\_H}$	VBST - VSW = 5.1V	-	85	-	mΩ
Low-Side On-Resistance	$r_{DS(ON)\_L}$	-	-	45	-	mΩ
Current Limit and Protection						
Current Limit	I_{LIM_L}	Valley current, low-side FET, valid when t_{OFF} > 100ns	2.7	3.25	3.5	A
UVP	FB_UV	Fault threshold, V_{FB} falling, soft-start completed	-	400	-	mV
Hiccup Soft-Start Done Time	t_{HICCUP_ON}	-	-	1.5	-	ms
Hiccup Power Off-Time	t_{HICCUP_OFF}	-	-	13.5	-	ms
Thermal Shutdown	TSD	-	-	170	-	°C
Thermal hysteresis	ΔTSD	-	-	40	-	°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Curves

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3µH, unless otherwise noted.

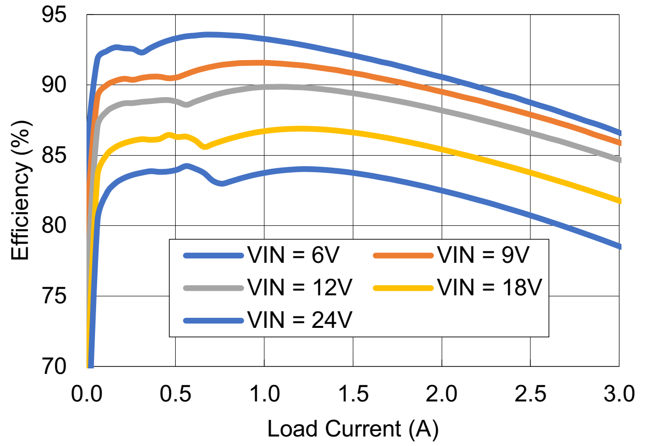


Figure 5. Efficiency vs Load Current (V_{OUT} = 3.3V)

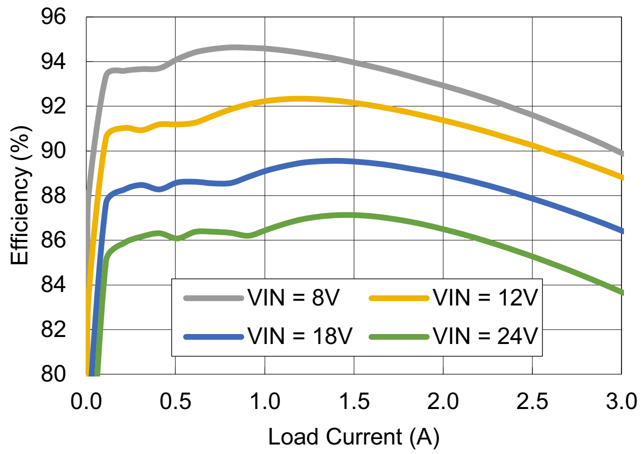


Figure 6. Efficiency vs Load Current (V_{OUT} = 5V)

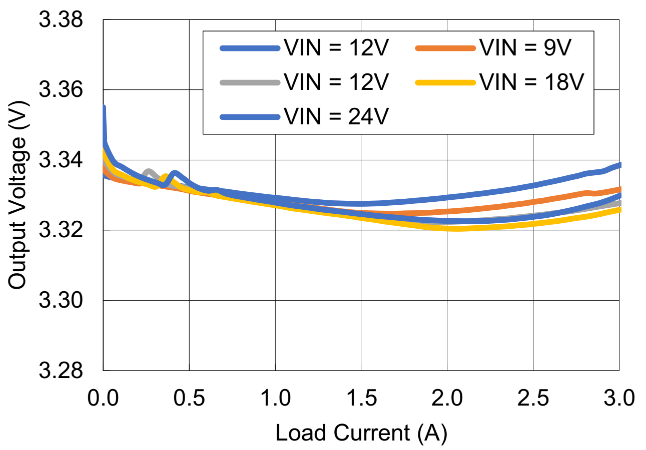


Figure 7. Load Regulation (V_{OUT} = 3.3V)

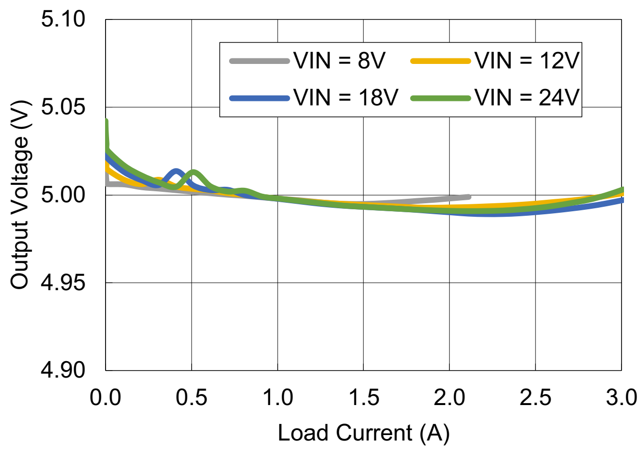


Figure 8. Load Regulation (V_{OUT} = 5V)

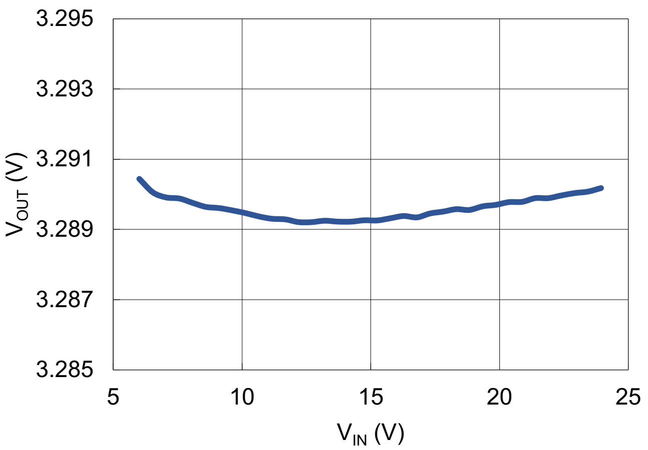


Figure 9. Line Regulation (V_{OUT} = 3.3V, I_{OUT} = 1A)

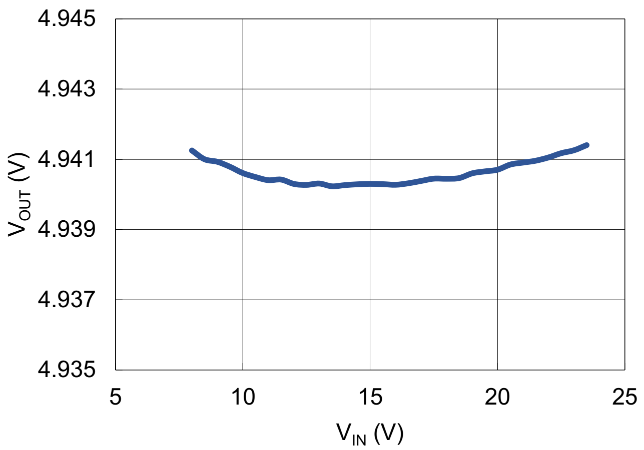


Figure 10. Line Regulation (V_{OUT} = 5V, I_{OUT} = 1A)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3µH, unless otherwise noted. (Cont.)

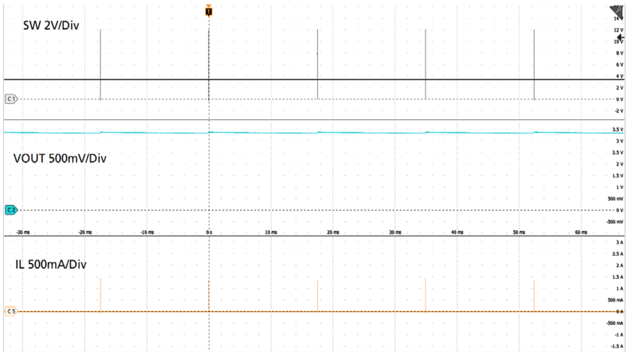


Figure 11. Steady-State Operation, I_{OUT} = 0A (V_{OUT} = 3.3V)

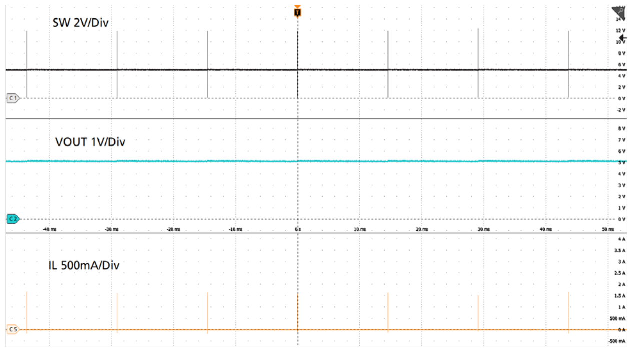


Figure 12. Steady-State Operation, I_{OUT} = 0A (V_{OUT} = 5V)

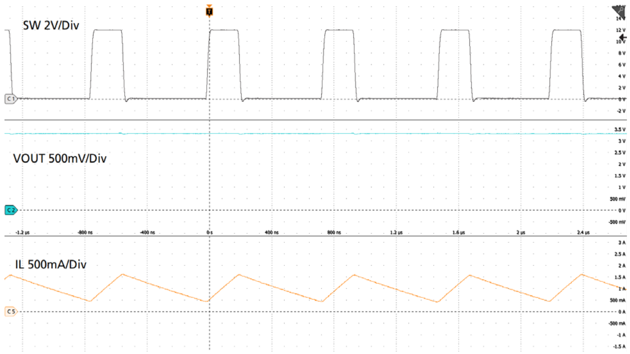


Figure 13. Steady-State Operation, I_{OUT} = 1A (V_{OUT} = 3.3V)

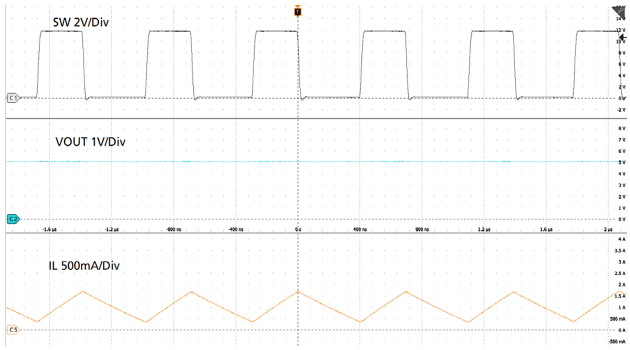


Figure 14. Steady-State Operation, I_{OUT} = 1A (V_{OUT} = 5V)

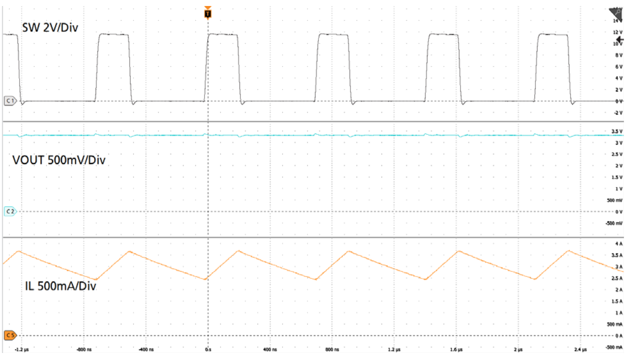


Figure 15. Steady-State Operation, I_{OUT} = 3A (V_{OUT} = 3.3V)

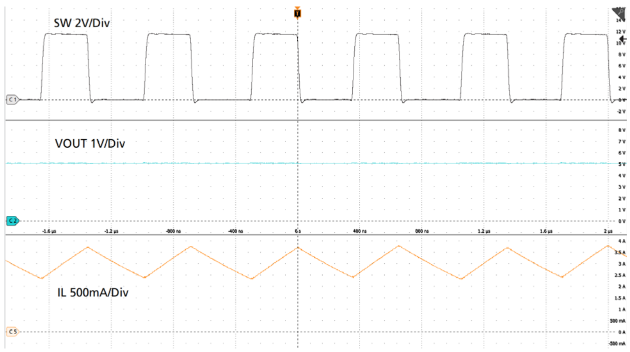


Figure 16. Steady-State Operation, I_{OUT} = 3A (V_{OUT} = 5V)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3µH, unless otherwise noted. (Cont.)

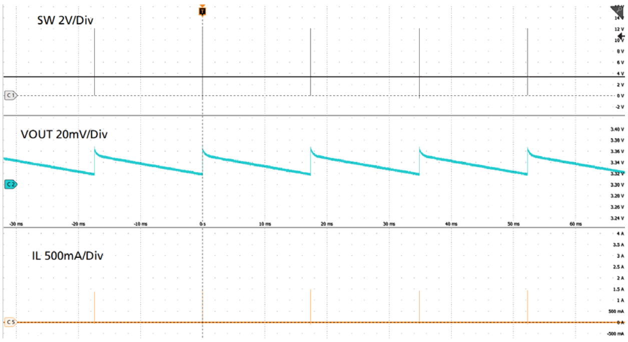


Figure 17. V_{OUT} Ripple at I_{OUT} = 0A (V_{OUT} = 3.3V)

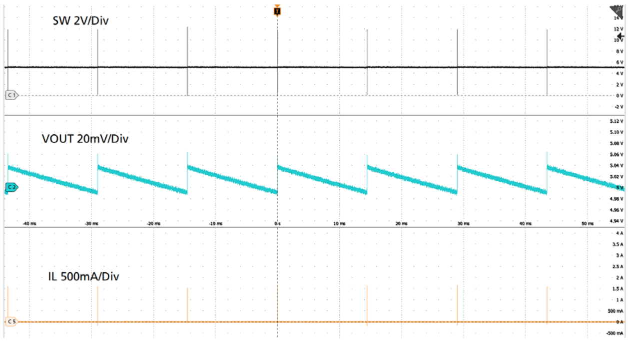


Figure 18. V_{OUT} Ripple at I_{OUT} = 0A (V_{OUT} = 5V)

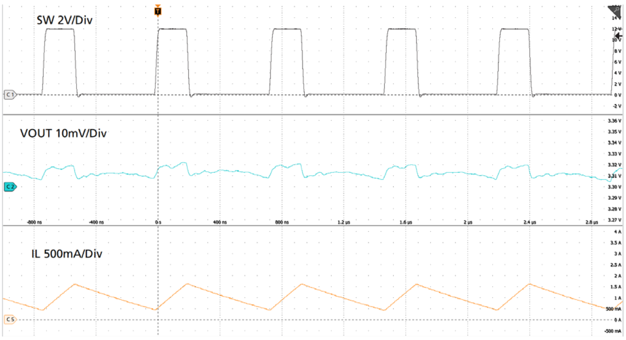


Figure 19. V_{OUT} Ripple at I_{OUT} = 1A (V_{OUT} = 3.3V)

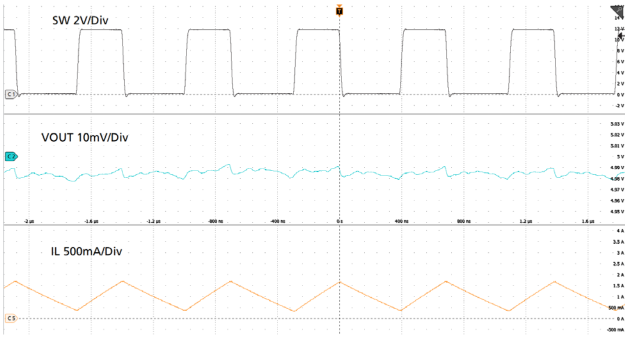


Figure 20. V_{OUT} Ripple at I_{OUT} = 1A (V_{OUT} = 5V)

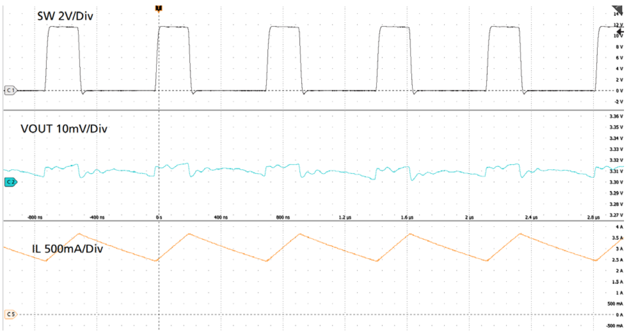


Figure 21. V_{OUT} Ripple at I_{OUT} = 3A (V_{OUT} = 3.3V)

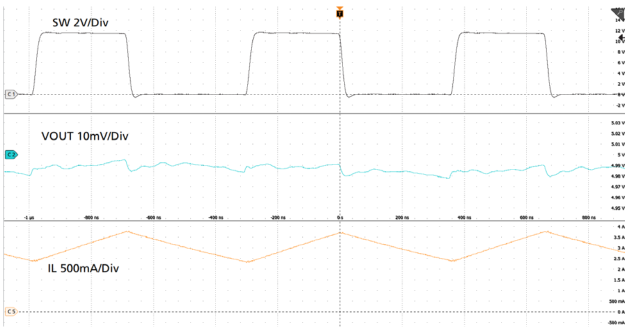


Figure 22. V_{OUT} Ripple at I_{OUT} = 3A (V_{OUT} = 5V)

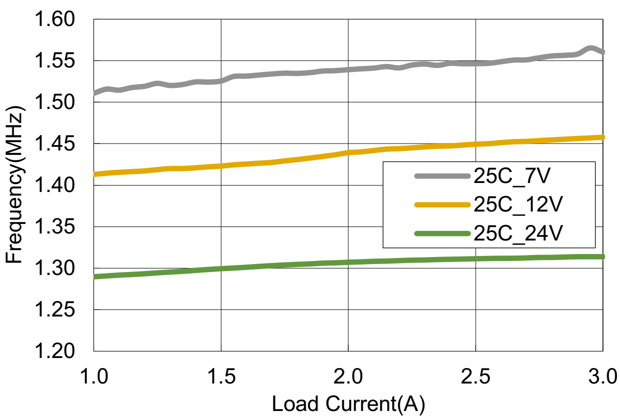


Figure 23. Switching Frequency vs Load Current

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3µH, unless otherwise noted. (Cont.)

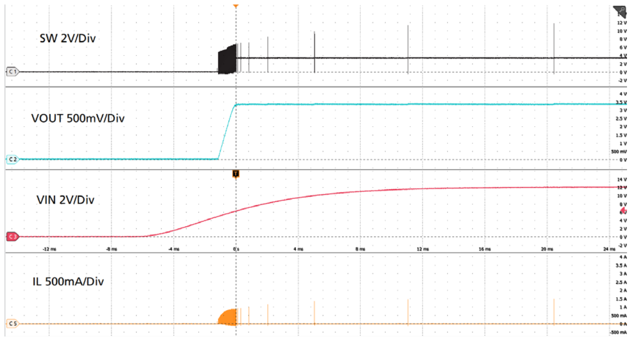


Figure 24. Startup through V_{IN} (I_{OUT} = 0A)

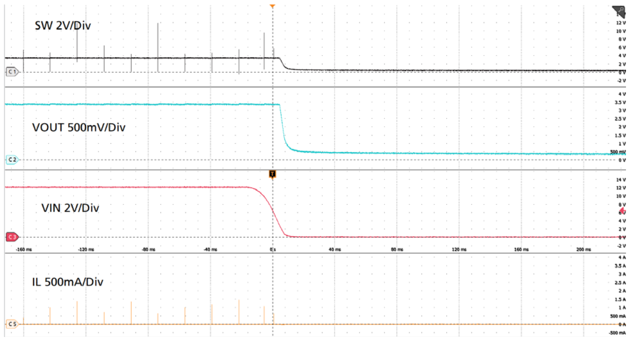


Figure 25. Shutdown through V_{IN} (I_{OUT} = 0A)

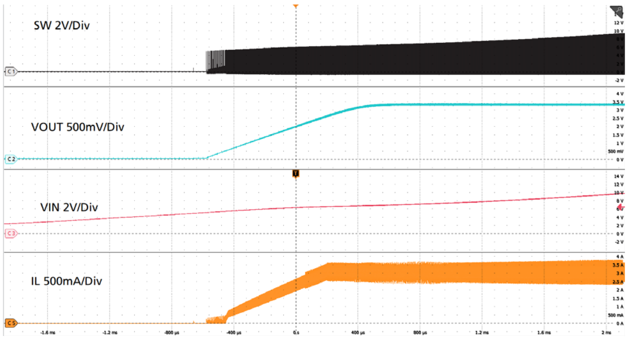


Figure 26. Startup through V_{IN} (I_{OUT} = 3A)

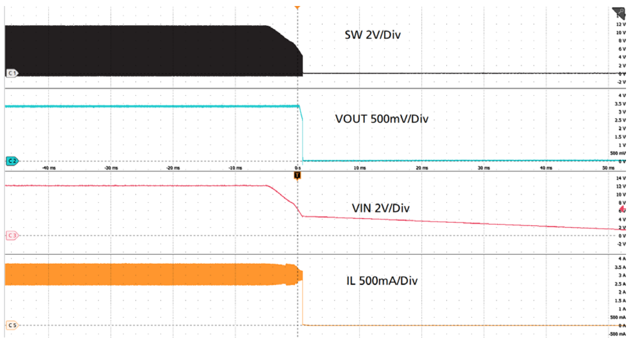


Figure 27. Shutdown through V_{IN} (I_{OUT} = 3A)

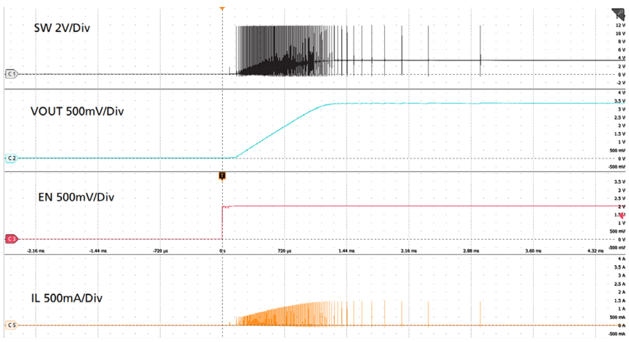


Figure 28. Startup through EN (I_{OUT} = 0A)

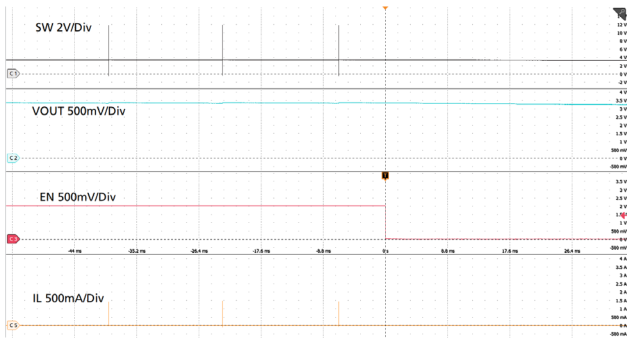


Figure 29. Shutdown through EN (I_{OUT} = 0A)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3µH, unless otherwise noted. (Cont.)

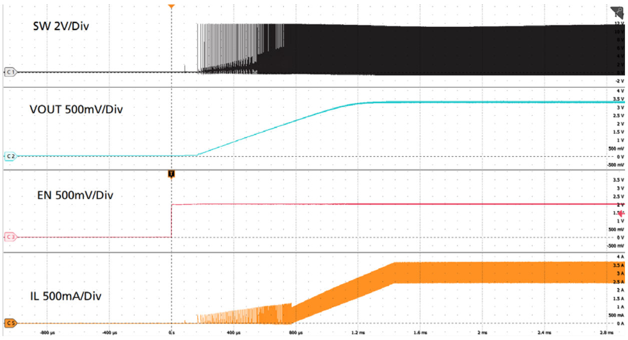


Figure 30. Startup through EN (I_{OUT} = 3A)

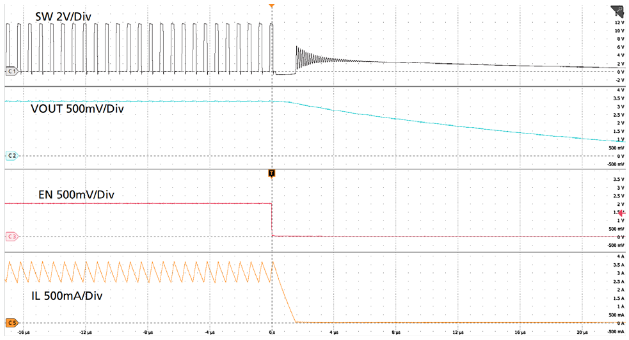


Figure 31. Shutdown through EN (I_{OUT} = 3A)

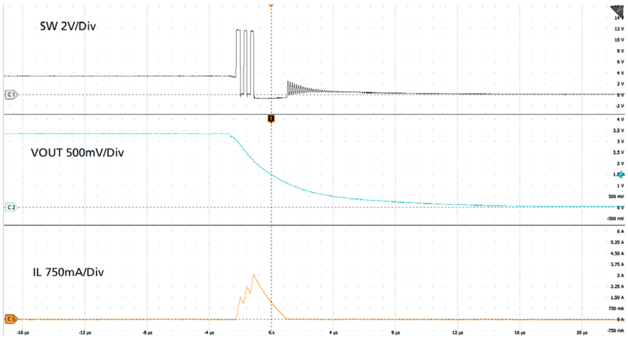


Figure 32. I_{OUT} = 0A to Short-Circuit

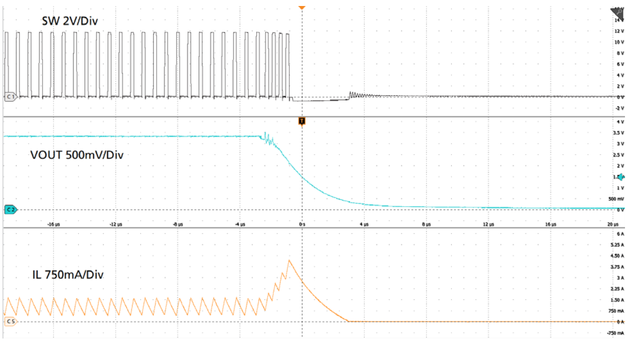


Figure 33. I_{OUT} = 1A to Short-Circuit

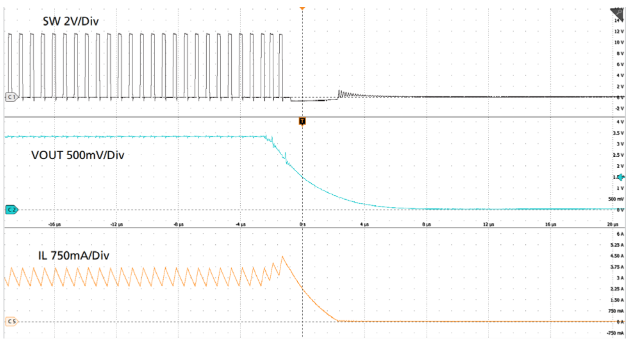


Figure 34. I_{OUT} = 3A to Short-Circuit

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 3.3µH, unless otherwise noted. (Cont.)

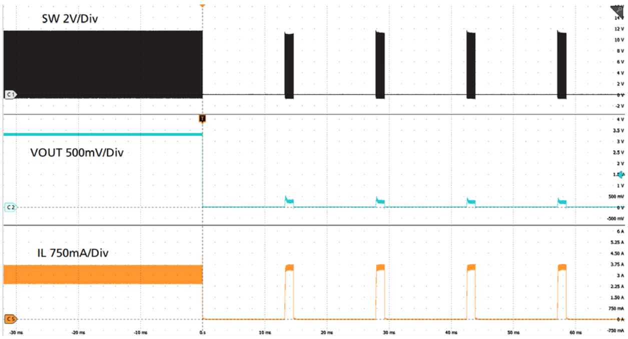


Figure 35. Hiccup after Output Short-Circuit

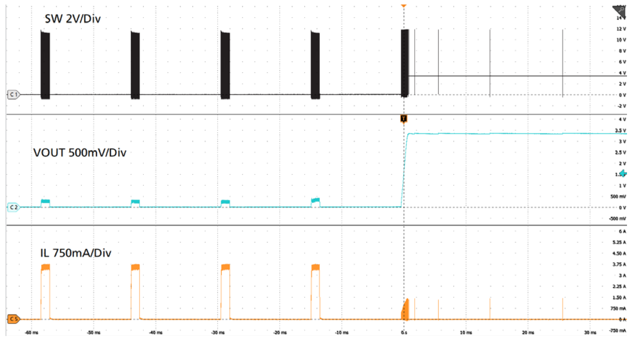


Figure 36. Short-Circuit to 0A Recovery

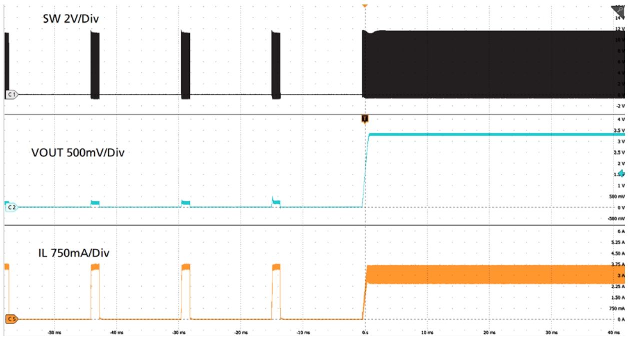


Figure 37. Short-Circuit to 3A Recovery

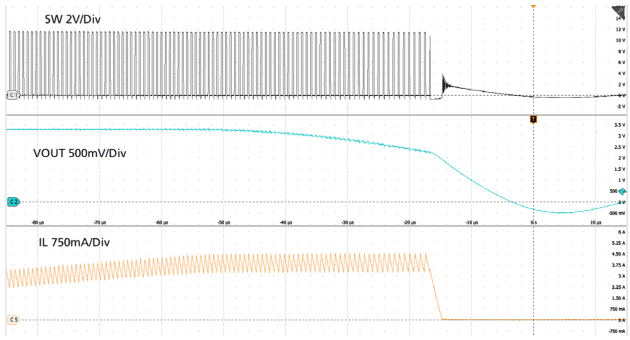


Figure 38. Low-Side Overcurrent (LSOC) Protection

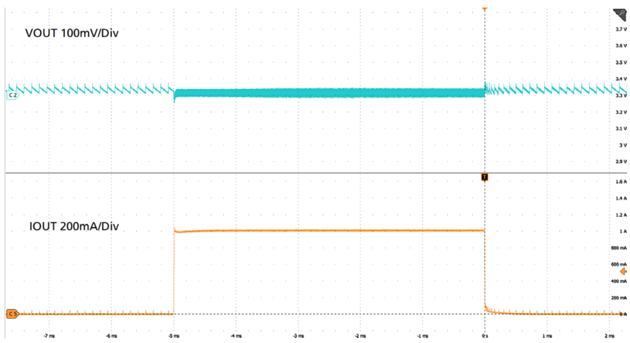


Figure 39. Load Transient, 0A to 1A (0.1A/µs)

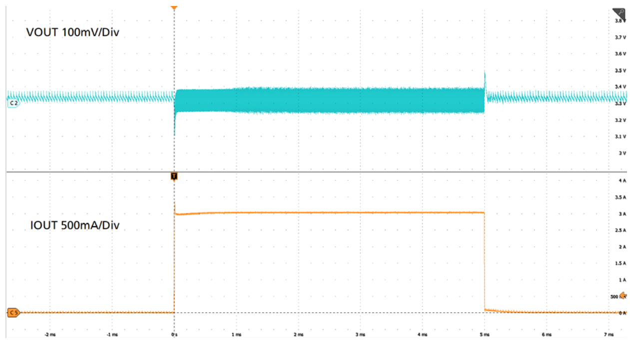


Figure 40. Load Transient, 0A to 3A (0.45A/µs)

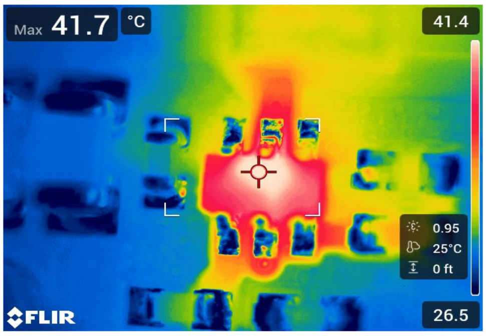


Figure 41. $12V_{IN}$, $3.3V_{OUT}$, 1A load,
IC Temperature = 41.7°C,
Max Ambient Temperature = 106.3°C

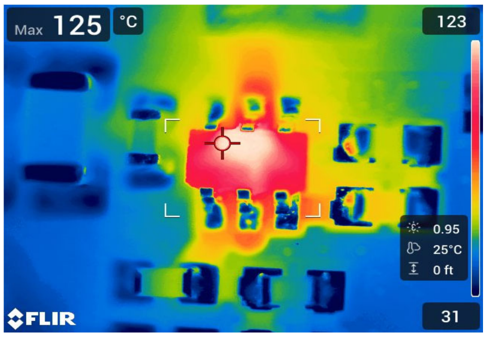


Figure 42. $12V_{IN}$, $3.3V_{OUT}$, 3A load,
IC Temperature = 125°C,
Max Ambient Temperature = 25°C

5. Faults and Fault Handling Description

5.1 System Level Fault Summary

Top level faults (V_{IN} UVLO, OTP) disable V_{OUT} and the IC enters the POR state until the fault is cleared. The device then resumes normal operation according to the state of the EN pin.

Fault Type	Detection Activated When	Detection Delay	Circuit behavior
V_{IN} UVLO falling	EN is higher than threshold.	2µs	POR (Power on Reset), chip restarts from initial reset state when UVLO is satisfied.
Over-temperature (OT) shutdown	After EN pin goes high and IC is in active state.	Immediate	POR using internal regulator, hiccup timer is engaged.
V_{OUT} Undervoltage (UV)	After soft-start done, after Hiccup on-time.	Immediate	After Soft-start is done (1ms), if V_{OUT} falls to 65% of set value and LSOC limit is reached, hiccup timer is engaged.
Low-Side Overcurrent (LSOC) Limit	Start of buck regulator switching.	Immediate	If LSOC is detected, the device keeps LS FET on until current falls below LSOC limit.

6. Functional Description

The RAA211233 is an integrated synchronous buck regulator with current mode constant on-time (COT) control. It can operate across a wide input voltage range from 4.5V to 24V, delivering load current up to 3A across the -40°C to 125°C temperature range. The output voltage is sensed on the FB pin through external feedback resistors when compared with the internal reference of 0.6V to produce the control signal, which decides when to turn on the high-side FET. The internal COT circuit determines the on-time of the high-side FET based on the sensed value of V_{IN} and V_{OUT}.

At light-load conditions, the regulator operates in DCM mode with a switching frequency determined by the output load (pulse-frequency modulation). The part transitions to CCM mode at higher loads with a constant frequency of 1.4MHz (see Figure 23).

6.1 Soft-Start

Soft-start forces the regulator to ramp up in a controlled fashion, which prevents high inrush current or output voltage overshoot at startup (see Figure 30). During soft-start, the reference voltage input of the error amplifier ramps up from 0V to its nominal value in 1.2ms.

6.2 Undervoltage Lockout

The regulator has an undervoltage lockout (UVLO) on the VIN pin that prevents the regulator from starting up until the input voltage exceeds 4.3V (typical). The UVLO threshold has approximately 400mV of hysteresis; therefore, the device continues to operate when V_{IN} decreases until it drops below 3.9V (typical). Hysteresis prevents the part from turning off during power-up if the V_{IN} is non-monotonic. Renesas recommends ensuring that the current path length from the V_{IN} power supply or upstream regulator to the IC is as small as possible to prevent jittering during V_{IN} turn-off and turn-on.

6.3 Enable Control

RAA211233 has an enable pin that turns the device on when pulled high. When EN is low, the IC goes into shutdown mode (see Figure 28 to Figure 31). RAA211233 has an EN rising threshold voltage of 1.31V (typical). EN threshold hysteresis is 110mV (typical). RAA211233 also has an Enable shutdown threshold of 0.69V; below the threshold, all the internal circuitry of the IC shuts down.

The EN pin can be tied directly to VIN for always-on operation. The device has an accurate Enable threshold that allows programming the V_{IN} UVLO threshold by connecting VIN to EN using a resistor divider. The UVLO can be set with the resistor divider based on Equation 1, where V_{INR} is the rising threshold of V_{IN} UVLO (see Figure 2).

(EQ. 1) $$\frac{R_{EN1}}{R_{EN2}} = \left(\frac{V_{INR} - 1.31}{1.31}\right)$$

Use Equation 2 to calculate the resulting input voltage for turning the part off.

(EQ. 2) $$VINF = 1.2 \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}}$$

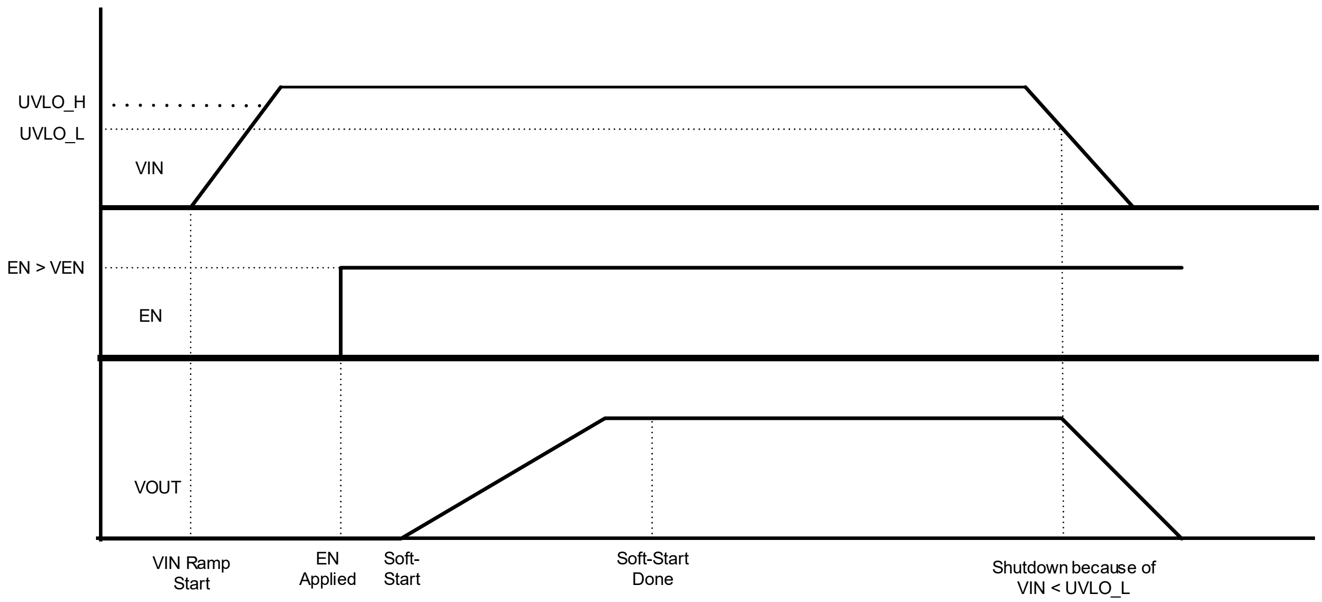


Figure 43. Timing Diagram with EN Turn-On and VIN UVLO Turn-Off

6.4 Overcurrent Protection (OCP) and V_{OUT} Undervoltage Protection

RAA211233 has a low-side overcurrent (LSOC) protection feature. After the regulator starts up, if the current through the internal low-side MOSFET exceeds the current limit, the device skips the high-side cycles until the LSOC condition clears.

RAA211233 also has a V_{OUT} undervoltage (UV) protection. The internal undervoltage comparator compares the FB pin voltage to 65% of the reference voltage. When LSOC is detected, and this voltage drops below 65% of nominal (because of a drop in V_{OUT} to below 65% of its set point), the regulator stops switching and engages Hiccup mode operation at an interval of 13.5ms (see Figure 35).

6.5 Over-Temperature Protection

Over-temperature protection (OTP) limits the maximum junction temperature in the RAA211233, which limits total power dissipation by shutting off the regulator when the IC junction temperature exceeds 170°C (typical). There is a 40°C hysteresis for OTP. After the junction temperature drops below 130°C, the RAA211233 resumes operation by stepping through soft-start.

7. Applications Information

Table 2 lists the recommended component selections for typical applications.

Table 2. Recommended Components Selection for Typical Application

V_{IN} (V)	V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{OUT} (µF)
12	1.8	20	10	1	33
12	3.3	45.3	10	1.5	20.4
12	5	73.2	10	1.5	15
12	8	121	10	1.5	8
5	1.05	7.5	10	0.68	55
5	1.8	20	10	0.68	33
5	3.3	45.3	10	0.68	20.4
24	1.8	20	10	1	33
24	3.3	45.3	10	1.5	20.4
24	5	73.2	10	2.2	15
24	12	191	10	3.3	6.8

7.1 Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.6V with a resistor divider from VOUT to the FB pin to GND based on Equation 3. The recommended R_{FB2} (see Figure 1) resistance is 10kΩ. See Table 2 for R_{FB1} and R_{FB2} values for typical V_{OUT} applications.

(EQ. 3) $$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 0.6}{0.6}$$

High-impedance nodes are more prone to pickup noise. The recommended range of feedback resistors (R_{FB1} + R_{FB2}) is 5kΩ to 150kΩ.

Analog circuitry in the Boot regulator outputs 40µA at the SW node. For applications using zero-load condition, this 40µA must be consumed by the feedback resistors to prevent positive drift of V_{OUT}. Renesas recommends the following maximum impedance $(R_{FB1} + R_{FB2})_{max}$ for applications using zero-load condition, where R_{FB1} and R_{FB2} are in kΩ:

(EQ. 4) $$(R_{FB1} + R_{FB2})_{max} = 0.8 \times \frac{V_{OUT}}{40} \times 10^3$$

For Applications using V_{IN} less than 10V, Renesas recommends limiting $(R_{FB1} + R_{FB2})$ to under 3kΩ.

The absolute maximum output voltage for RAA211233 is 11V. Equation 5 calculates the maximum operating output voltage for a given input voltage when the max V_{OUT} is less than 11V. Renesas recommends leaving some margin for max V_{OUT} calculated in Equation 5 to account for losses in the circuit. Figure 44 shows the operating V_{OUT} range across V_{IN}.

(EQ. 5) $$V_{OUTmax} = V_{IN} \times f_{SW} \times \left(\frac{1}{f_{SW}} - t_{OFFmin}\right)$$

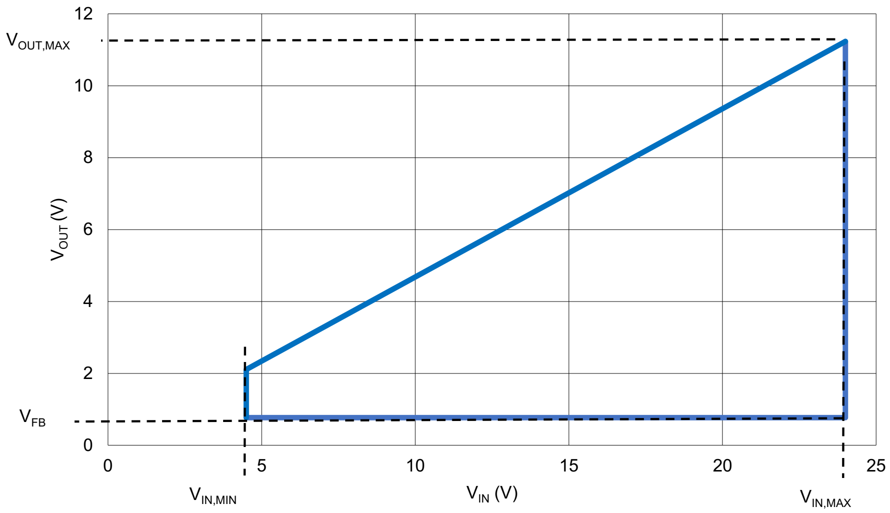


Figure 44. Operating Range for V_{IN} and V_{OUT}

7.2 Inductor Selection

Select an inductor with the lowest possible DC resistance (DCR) to minimize power losses. The saturation current rating of the inductor should be high enough to accommodate the DC load current and AC ripple current with an additional margin for overload conditions. The inductor of the buck converter determines its ripple current so that it also determines its output ripple voltage. Selecting a higher inductance value results in lower output ripple voltage, but it may increase the response time and output voltage drop during a load transient. The ripple voltage and current are approximated by Equation 6 and Equation 7.

(EQ. 6) $$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{sw} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

(EQ. 7) $$\Delta V_{OUT} = \Delta I \times ESR$$

A reasonable starting point for the inductor ripple current is 20% to 50% of the maximum output current. Reference Table 2 for selecting the inductor value for typical V_{OUT} applications.

During overcurrent and short circuit conditions, the peak inductor current becomes higher than the current during normal operation. Renesas recommends using inductors with soft saturation characteristics.

7.3 Input Capacitor Selection

The input capacitor in a buck converter maintains the input voltage by suppressing the voltage ripple induced by discontinuous switching current. Use Equation 8 to approximate the required RMS current rating $I_{IN(RMS)}$ of the input capacitor, where $I_{OUT(MAX)}$ is the maximum average load current and D is the duty ratio.

(EQ. 8) $$I_{IN(RMS)} = I_{OUT(MAX)} \times \sqrt{D \times (1-D)}$$

When D equals 0.5, $I_{IN(RMS)}$ has the highest value, $I_{OUT(MAX)}/2$.

The voltage rating of the input capacitor should be higher than the maximum input voltage. Use Equation 9 to calculate the required capacitance C_{IN} of the input capacitor to ensure the expected peak-to-peak input voltage ripple ΔV_{IN}, where f_{SW} is the switching frequency.

(EQ. 9) $$C_{IN} = I_{OUT(MAX)} \times \frac{D \times (1-D)}{f_{SW} \times \Delta V_{IN}}$$

The required capacitance also has the maximum value when D equals 0.5.

Renesas recommends using low ESR/low ESL ceramic capacitors across the input of the regulator. When selecting ceramic capacitors for power supply applications, consider that the effective capacitance reduces with DC bias voltage across it, so consult the capacitor datasheet to understand the impact of this effect. Renesas also recommends using X5R/X7R dielectric ceramic capacitors because of their small temperature coefficient.

If the input to the regulator is fed through a high-impedance path, Renesas recommends adding an electrolytic capacitor in addition to the ceramic capacitor to dampen the input voltage oscillation effects.

7.4 Output Capacitor Selection

Output capacitor selection impacts both the steady state and transient performance of the buck converter. Factors such as output ripple voltage, output voltage excursion during transients, and control loop stability should be considered when selecting the output capacitor. Renesas recommends using X5R/X7R dielectric ceramic for the output capacitor. When selecting the ceramic capacitor, consider that the effective capacitance reduces with a DC bias voltage across it.

Use the effective capacitance of the ceramic capacitor when determining the output voltage ripple. Use Equation 10 to calculate the required capacitance $C_{OUT(RIPPLE)}$, where ΔI_L is the inductor peak-to-peak current ripple and f_{SW} is the switching frequency.

(EQ. 10) $$C_{(OUTRIPPLE)} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT(RIPPLE)}}$$

To meet the output voltage variation requirements during load step-up and load step-down transients, use Equation 11 to calculate the required capacitance $C_{OUT(STEPUP)}$ and Equation 12 to calculate the $C_{OUT(STEPDOWN)}$, where I_{STEP} is the transient load step, and ΔV_{OUT} is the expected voltage variation during the transient.

(EQ. 11) $$C_{OUT(STEPUP)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT}}$$

(EQ. 12) $$C_{OUT(STEPDOWN)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times V_{OUT} \times \Delta V_{OUT}}$$

To have a stable control loop with adequate gain margin, phase margin, and bandwidth, use Equation 13 to derive the required capacitance $C_{OUT(LOOP)}$, where $C_{OUT(LOOP)}$ is in μF and V_{OUT} is in V:

(EQ. 13) $$C_{OUT(LOOP)}(\mu F) = \frac{58.1}{V_{OUT}}$$

The output capacitors should be selected so that previous requirements are met: this means that the total capacitance should be greater than the highest value calculated in Equation 10, Equation 11, Equation 12, or Equation 13.

See Table 2 for recommended values of output capacitor for typical V_{OUT} applications.

7.5 BOOT Refresh and Capacitor Selection

Approximately 85μs after EN is driven high and before the start-up process begins, the RAA211233 turns on the internal BOOT voltage regulator. This action charges the boot capacitor before the start-up process begins. To prevent turn-on of HS FET at low BOOT Voltages, the BOOT UVLO function is provided. When the BOOT voltage is below 2.5V, the regulator skips the HS pulse and provides LS pulse until the BOOT voltage rises above 2.5V.

A capacitor is needed between the BST pin and the SW pin to provide gate voltage for the high-side internal MOSFET. Renesas recommends using a greater than 10V X5R/X7R 0.1μF ceramic capacitor as the bootstrap capacitor for most applications.

8. Component Placement and Layout Suggestions

The printed circuit board (PCB) layout is critical for proper operation of the RAA211233. The following guidelines are recommended to achieve good performance.

- Use a combination of a bulk capacitor and smaller ceramic capacitors with low ESL for input capacitors and place them as close as possible to the IC. Place the input ceramic capacitor(s) as close as possible to the IC.
- Keep the power loop (input ceramic capacitor, IC VIN and PGND pins) as small as possible to minimize switch node voltage ringing caused by parasitic inductance in the PCB traces. Minimizing loop size also results in better EMI performance.
- Place bootstrap capacitors close to the IC between BST and SW pins on the same side of the PCB as the IC. Renesas recommends using a 0.1μF ceramic capacitor.
- Keep the phase node copper area small to reduce the parasitic capacitance, but large enough to handle the load current. Place the inductor close to the regulator.
- Route the output voltage feedback signal away from SW and BST. Place feedback resistors close to the FB pin of the regulator.
- Place an output capacitor close to the inductor.

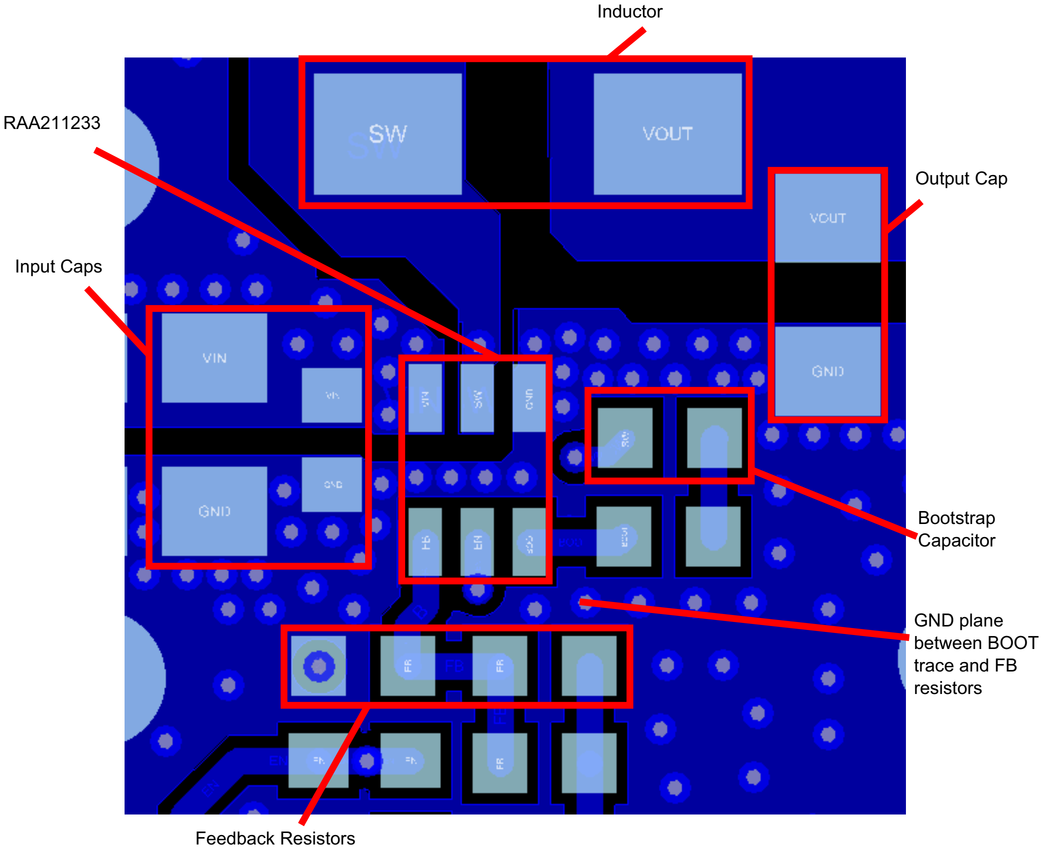
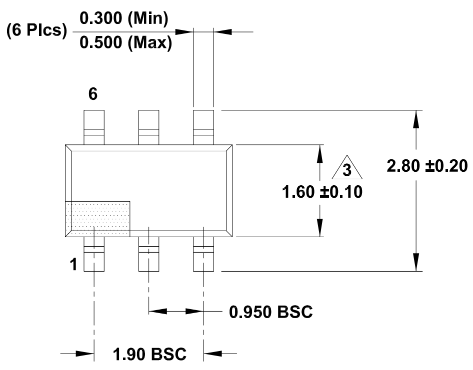


Figure 45. Example Layout

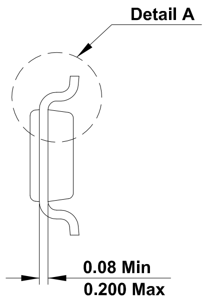
9. Package Outline Drawing

For the most recent package outline drawing, see P6.064C.

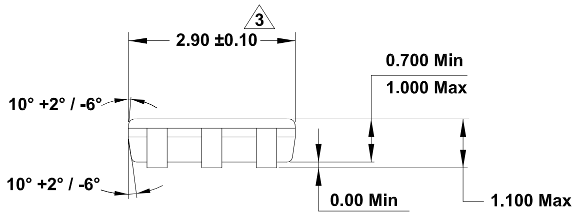
P6.064C
6 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 2, 12/20



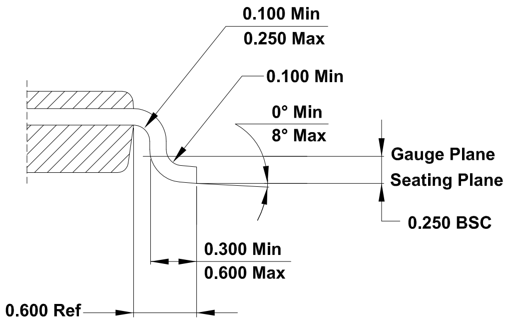
Top View



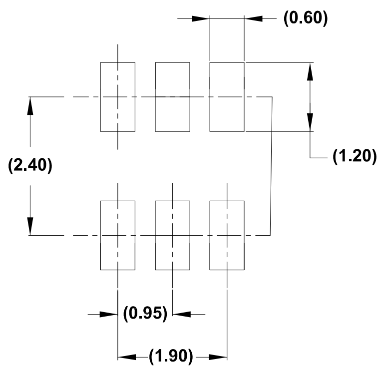
End View



Side View



Detail A



Typical Recommended Land Pattern

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

10. Ordering Information

Part Number[1][2]	Part Marking[3]	Package Description[4] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[5]	Temp Range
RAA2112334GP3#JA0	233	6Ld TSOT-23	P6.064C	Reel, 3k	-40 to +125°C
RTKA211233DE0000BU	RAA211233 Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA211233 device page. For more information about MSL, see TB363.
3. The part marking is located on the bottom of the part.
4. For the Pb-Free Reflow Profile, see TB493.
5. See TB347 for details about reel specifications.

11. Revision History

Rev.	Date	Description
1.00	Nov 14, 2023	Initial release

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/