Datasheet

RAA211320

30V 2A Integrated Switching Regulator

The RAA211320 is an integrated 30V, 2A synchronous buck regulator with current mode constant on-time (COT) control. The RAA211320 features comprehensive protection including input undervoltage lockout (UVLO), overcurrent protection (OCP), output undervoltage protection (OUVP), and over-temperature protection (OTP).

The device is available in a 6 Ld TSOT23 package.

Applications

- General purpose
- Industrial power supplies
- Embedded systems and I/O supplies

Features

- 4.5V to 30V input supply range
- Up to 2A output current
- Integrated high-side (125mΩ) and low-side (75mΩ) MOSFETs
- 400µA quiescent current
- Minimum on-time of 70ns
- Minimum off-time of 225ns
- 0.765V reference voltage with 2% accuracy
- PFM mode under light load condition
- Current mode Constant On-Time (COT) control with internal compensation
- Internal 0.8ms soft start time
- Protection: Low-Side Overcurrent (LSOC) limit, input Undervoltage Lockout (UVLO), Over-Temperature Protection (OTP), Output Undervoltage Protection (OUVP) with Hiccup Mode
- Accurate EN threshold
- 6 LD TSOT23 package

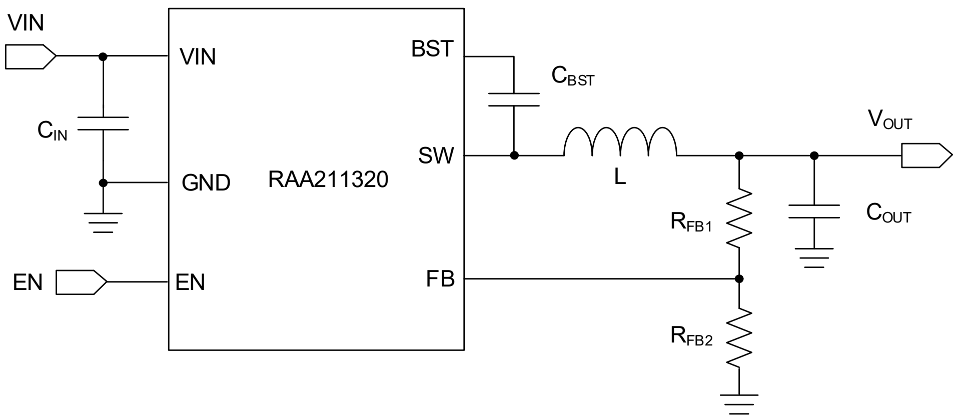

Figure 1. Typical Application Circuit Diagram

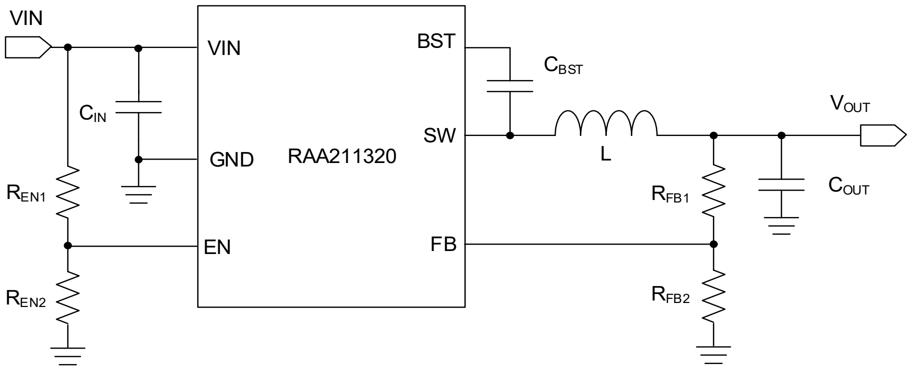

Figure 2. Typical Application Circuit Diagram with V_{IN} UVLO Programming by ENABLE

Table 1. Bill of Materials for Typical Application Circuit (3.3V V_{OUT})

Item	Qty	Reference	Value	Description	Part number
1	1	C_{IN}	10µF	CAP CER 10µF 35V X7R 1206	GMK316AB7106KL-TR
2	1	C_{OUT}	22µF	CAP CER 22µF 6.3V X7R 0805	GRM21BZ70J226ME44L
3	1	C_{BST}	0.1µF	CAP CER 0.1µF 10V X7R 0603	C0603C104K9RACTU
4	1	L_1	6.5µH	WE-HCI SMD High Current Inductor, 6.5µH, 20%	744314650
5	1	R_{FB1}	33.2k	1% resistor 0603	Generic
6	1	R_{FB2}	10k	1% resistor 0603	Generic

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1. Overview

1.1 Block Diagram

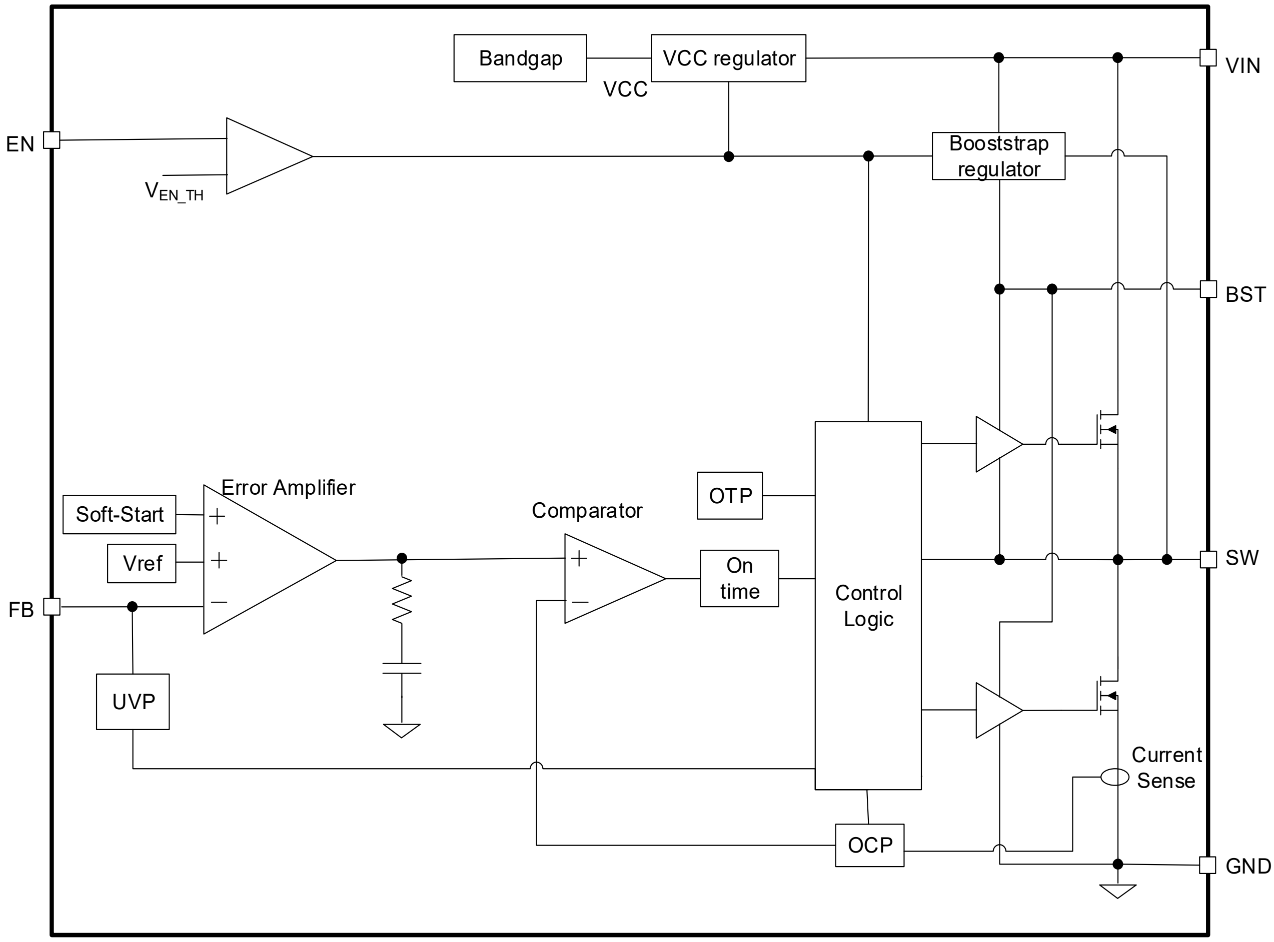
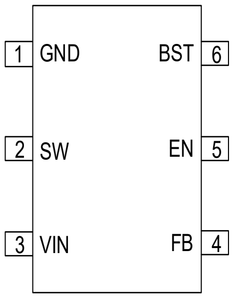


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	GND	Ground
2	SW	Switch node pin. Connect this pin to the inductor.
3	VIN	Voltage input for the IC. Connect to a suitable voltage source within the IC operating range to this pin. Place a ceramic capacitor from VIN to GND close to the IC for decoupling.
4	FB	Feedback input pin for the regulator. The output voltage is set by an external resistor divider connected to FB. FB voltage is 0.765V during normal operation.
5	EN	This pin Enable and Disable the IC. A resistor divider from VIN can be connected to EN to program VIN UVLO. Drive EN with impedance less than 10kΩ.
6	BST	Bootstrap supply pin. Connect a 0.1µF capacitor from BST to SW.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN	-0.3	32	V
EN	-0.3	VIN + 0.3	V
SW	-0.7	VIN + 0.3	V
SW (20ns transient)	-3	VIN + 2	V
BST	-	SW + 5.5	V
All other pins	-0.3	5	V
Human Body Model (HBM) (Tested per JS-001-2017)	-	2	kV
Charged Device Model (CDM) (Tested per JS-002-2018)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	6 Ld TSOT23	θ_{JA}[1]	Junction to air	105	°C/W
		θ_{JA_EVB}[2]	Junction to air, evaluation board	50	°C/W
		θ_{JC}[3]	Junction to case	45	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
2. θ_{JA_EVB} is measured in free air with the component mounted on the RTKA211320DE0020BU evaluation board.
3. For θ_{JC}, the case temperature measurement location is the center of top of package.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-40	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage, V_{IN}	4.5	30	V
Output Voltage, V_{OUT}	0.765	16	V
Output Current, I_{OUT}	0	2	A
Junction Temperature, T_J	-40	+125	°C

3.4 Electrical Specifications

$T_A = T_J$ = -40°C to +125°C, V_{IN} = 12V, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Symbol	Test Conditions	Min[1]	Typical	Max[1]	Unit
Supply Voltage						
V_{IN} Voltage Range	V_{IN}	-	4.5	-	30	V
Quiescent Current	I_Q	EN = 2V, VFB = 0.8V, no switching	-	400	-	µA
Shutdown Current	I_{SH}	EN = 0V, V_{IN} = 12, no switching	-	1.5	10	µA
V_{IN} Undervoltage Lockout	-	VIN Rising	-	4.3	4.55	V
V_{IN} Undervoltage Hysteresis	-	VIN Falling	-	425	-	mV
Enable Voltage						
EN Threshold Voltage	VEN	EN rising	1.2	1.3	1.45	V
Enable Voltage Hysteresis	-	-	-	100	-	mV
Enable Shutdown Threshold	VENL	-	-	0.7	-	V
EN Pin Resistance to GND	REN	VEN = 2V	-	2000	-	kΩ
Switching Frequency and Timer Control						
Switching Frequency Range	f_{SW}	VFB = 0.765V, V_{OUT} = 1.05V, I_{OUT} = 1A, V_{IN} = 12V	-	475	-	kHz
Minimum Off-Time	t_{OFF_MIN}	VFB = 0.75V	-	225	330	ns
Minimum On-Time	t_{ON_MIN}	-	-	70	-	ns
Internal Soft-Start Time	-	-	-	0.8	-	ms
Feedback Voltage						
Feedback Voltage Reference	V_{FB}	V_{IN} = 12V, EN = 2V, 25°C	0.75	0.765	0.78	V
Feedback Voltage Line Regulation	-	-	-	0.005	-	%/V
Internal Integrated MOSFETs						
High-Side On-Resistance	$r_{DS(ON)\_H}$	VBST-VSW = 5.1V	-	125	-	mΩ
Low-Side On-Resistance	$r_{DS(ON)\_L}$	-	-	75	-	mΩ

T_A = T_J = -40°C to +125°C, V_{IN} = 12V, unless otherwise noted. Typical values are at T_A = +25°C. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typical	Max[1]	Unit
Current Limit and Protection						
Current Limit	I_{LIM_L}	Valley current, low-side FET, valid when t_{OFF} > 100ns	1.75	2.3	3	A
UVP	FB_UV	Fault threshold, V_{FB} falling, soft-start completed	-	500	-	mV
Hiccup Soft-Start Done Time	t_{HICCUP_ON}	-	-	1	-	ms
Hiccup Power Off-Time	t_{HICCUP_OFF}	-	-	13	-	ms
Thermal Shutdown	TSD	-	-	170	-	°C
Thermal hysteresis	ΔTSD	-	-	40	-	°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Curves

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted.

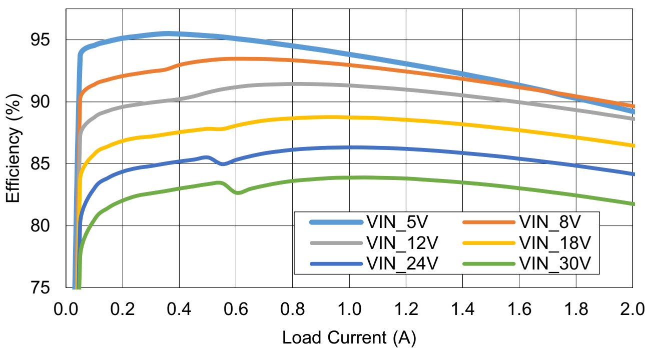


Figure 4. Efficiency vs Load Current (V_{OUT} = 3.3V)

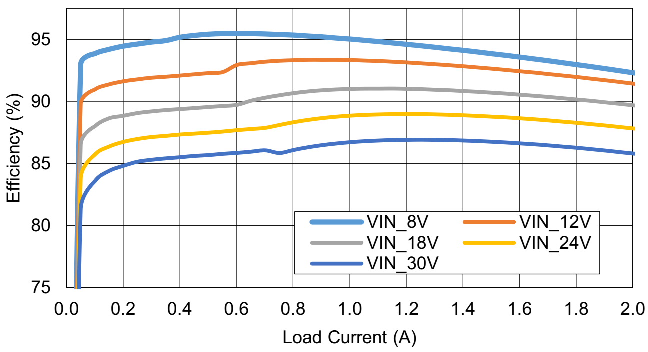


Figure 5. Efficiency vs Load Current (V_{OUT} = 5V)

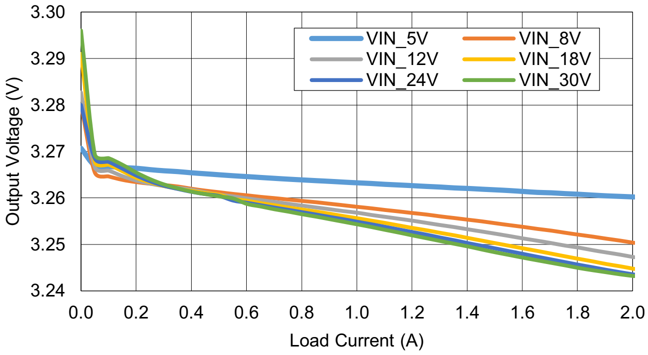


Figure 6. Load Regulation (V_{OUT} = 3.3V)

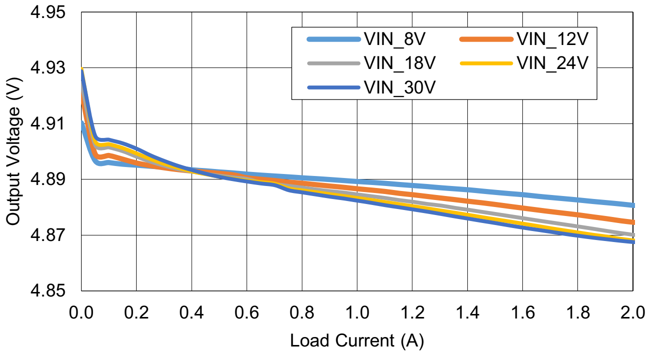


Figure 7. Load Regulation (V_{OUT} = 5V)

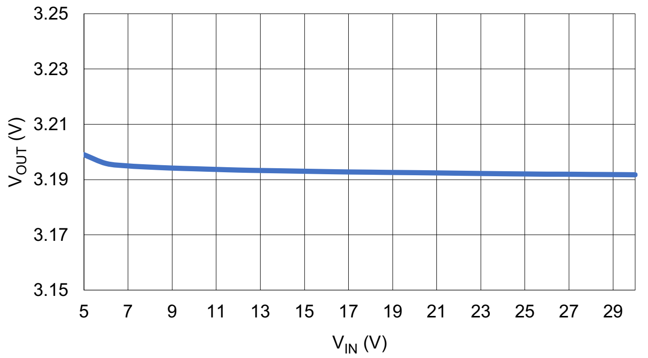


Figure 8. Line Regulation (V_{OUT} = 3.3V, I_{OUT} = 1A)

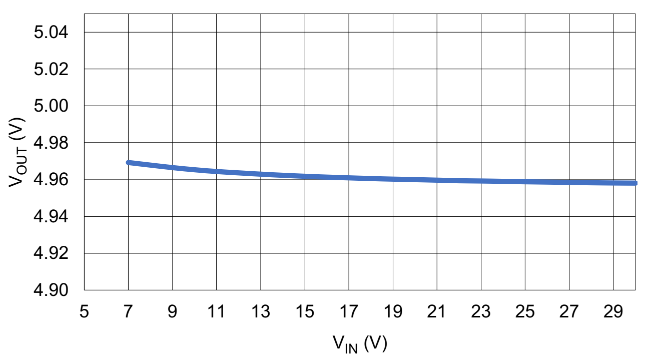


Figure 9. Line Regulation (V_{OUT} = 5V, I_{OUT} = 1A)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted. (Cont.)

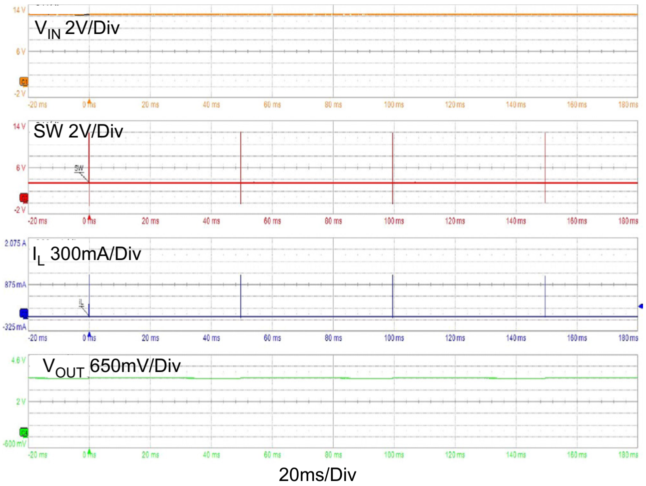


Figure 10. Steady-State Operation I_{OUT} = 0A (V_{OUT} = 3.3V)

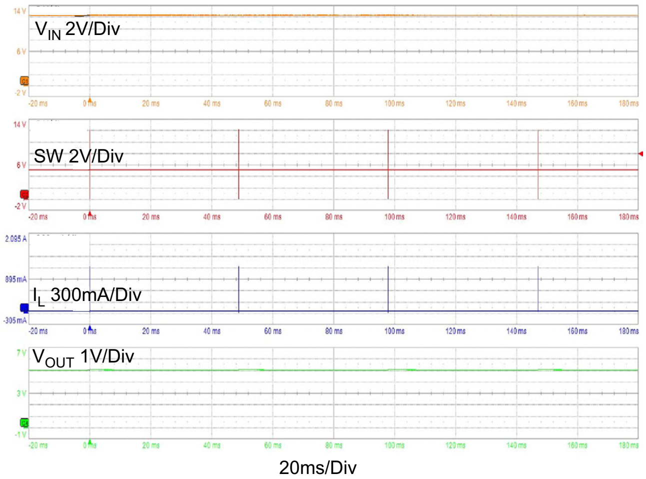


Figure 11. Steady-State Operation I_{OUT} = 0A (V_{OUT} = 5V)

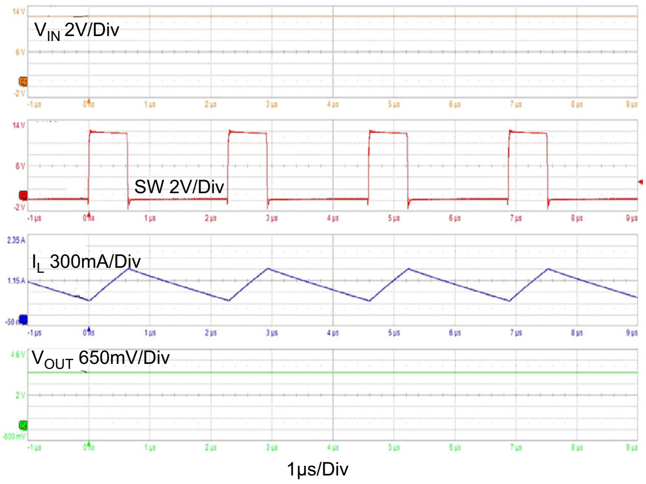


Figure 12. Steady-State Operation I_{OUT} = 1A (V_{OUT} = 3.3V)

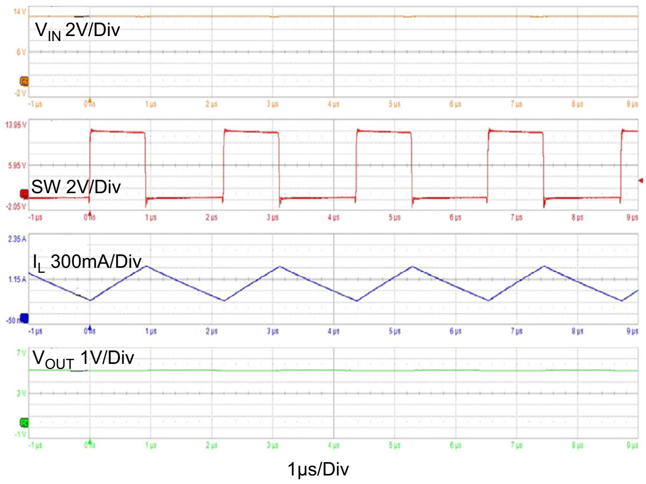


Figure 13. Steady-State Operation I_{OUT} = 1A (V_{OUT} = 5V)

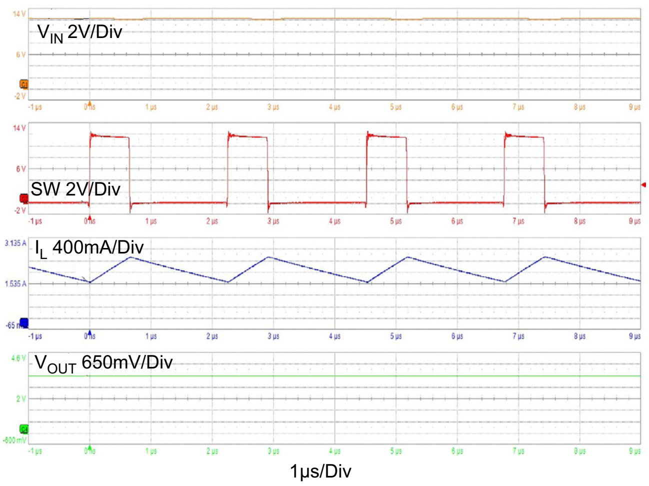


Figure 14. Steady-State Operation I_{OUT} = 2A (V_{OUT} = 3.3V)

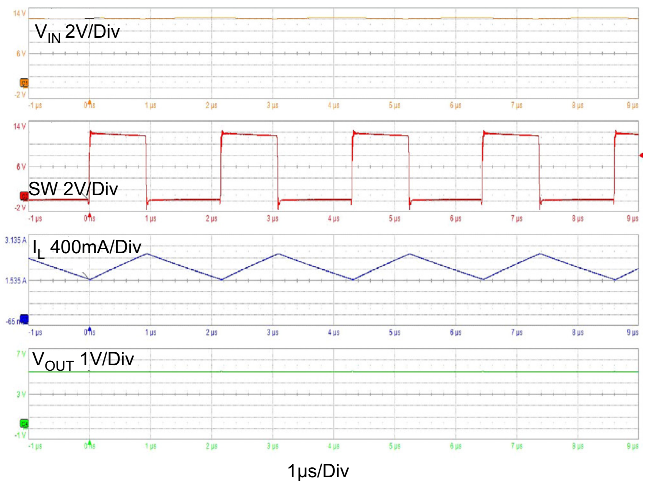


Figure 15. Steady-State Operation I_{OUT} = 2A (V_{OUT} = 5V)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted. (Cont.)

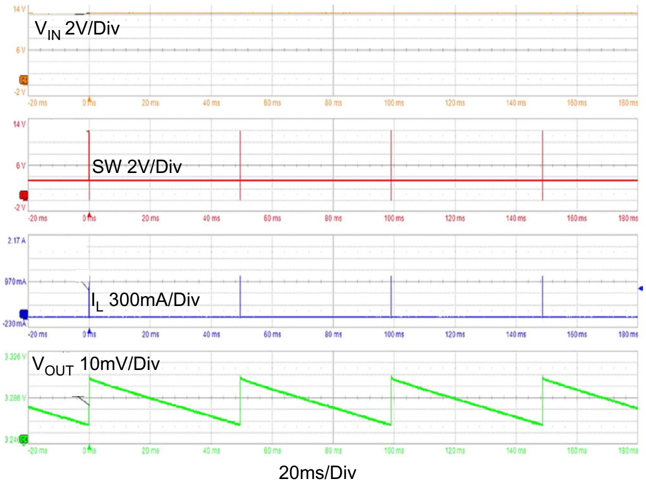


Figure 16. V_{OUT} Ripple at I_{OUT} = 0A (V_{OUT} = 3.3V)

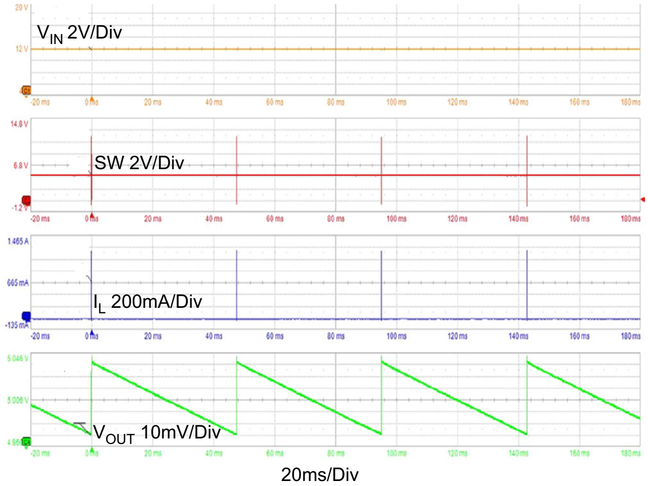


Figure 17. V_{OUT} Ripple at I_{OUT} = 0A (V_{OUT} = 5V)

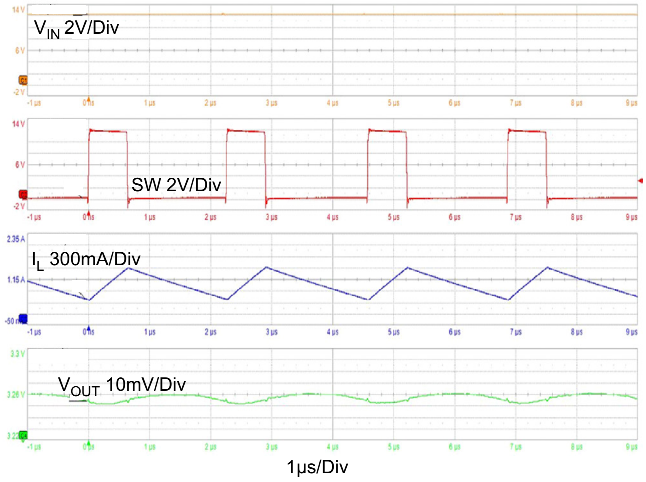


Figure 18. V_{OUT} Ripple at I_{OUT} = 1A (V_{OUT} = 3.3V)

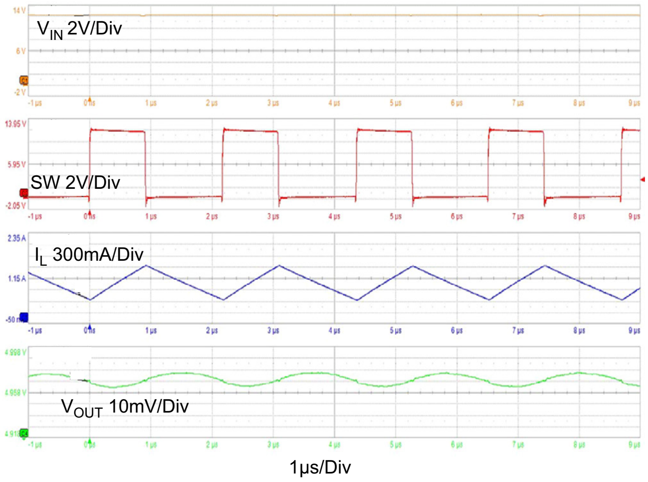


Figure 19. V_{OUT} Ripple at I_{OUT} = 1A (V_{OUT} = 5V)

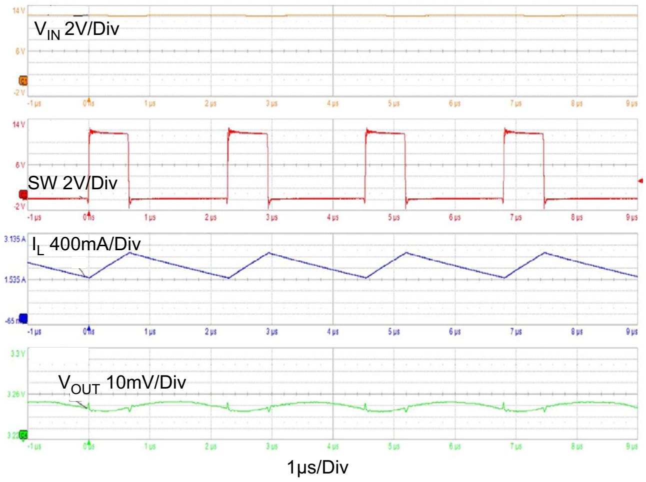


Figure 20. V_{OUT} Ripple at I_{OUT} = 2A (V_{OUT} = 3.3V)

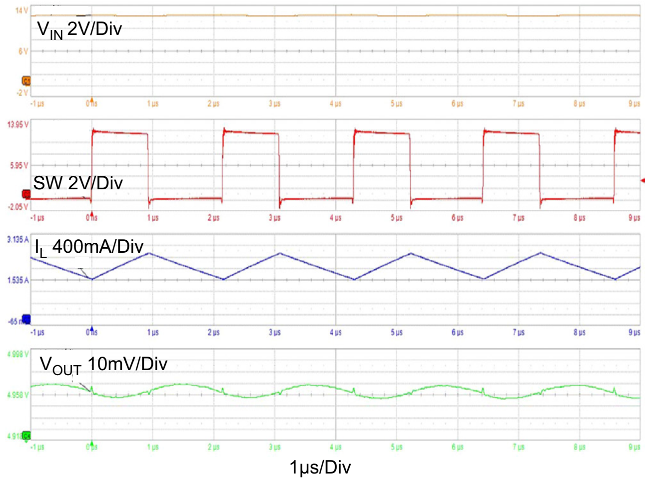


Figure 21. V_{OUT} Ripple at I_{OUT} = 2A (V_{OUT} = 5V)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted. (Cont.)

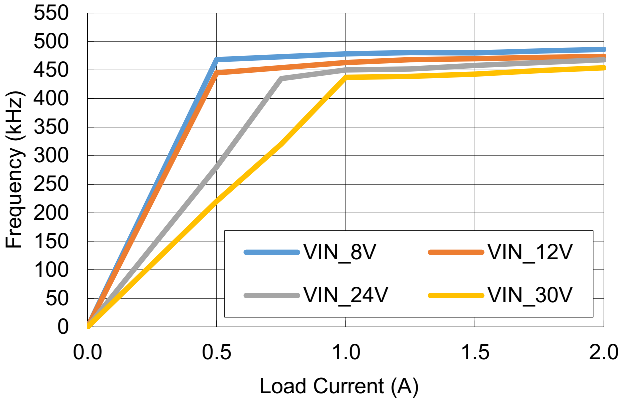


Figure 22. Switching Frequency vs Load Current

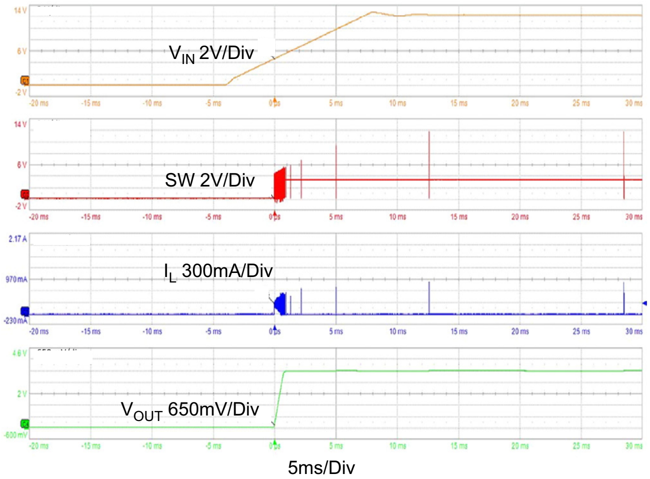


Figure 23. Startup through V_{IN} (I_{OUT} = 0A)

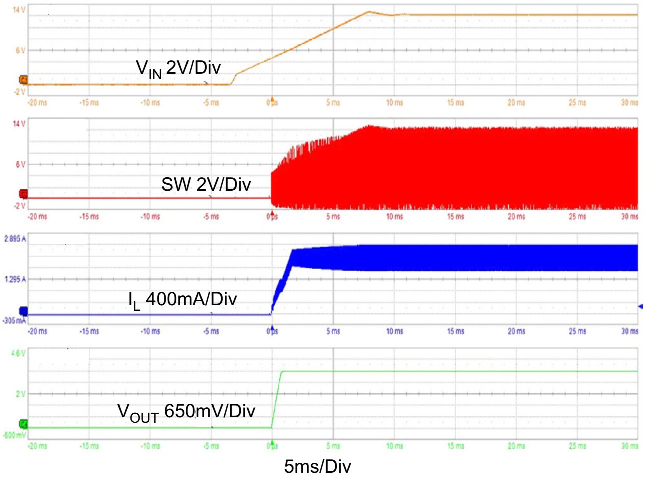


Figure 24. Startup through V_{IN} (I_{OUT} = 2A)

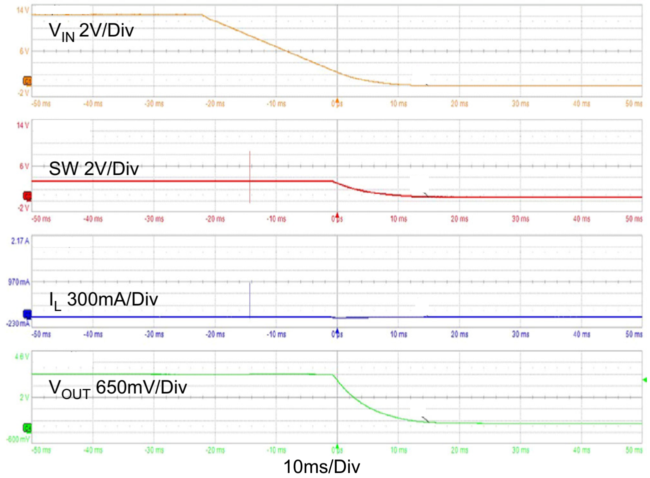


Figure 25. Shutdown through V_{IN} (I_{OUT} = 0A)

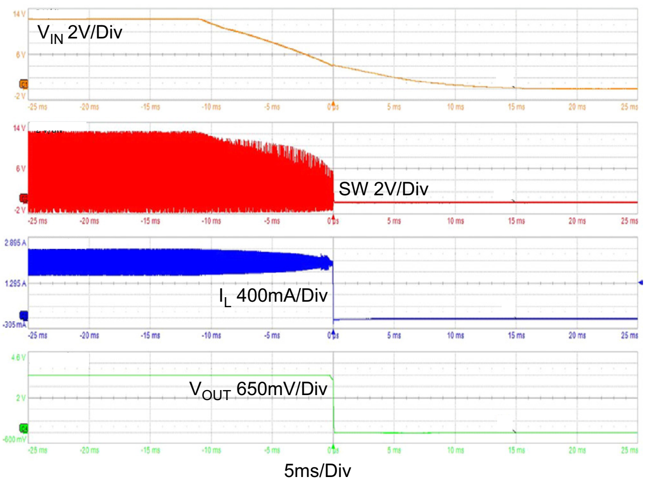


Figure 26. Shutdown through V_{IN} (I_{OUT} = 2A)

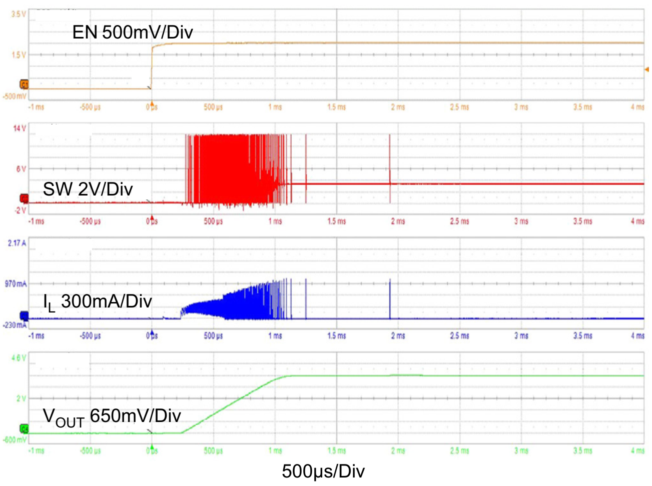


Figure 27. Startup through EN (I_{OUT} = 0A)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted. (Cont.)

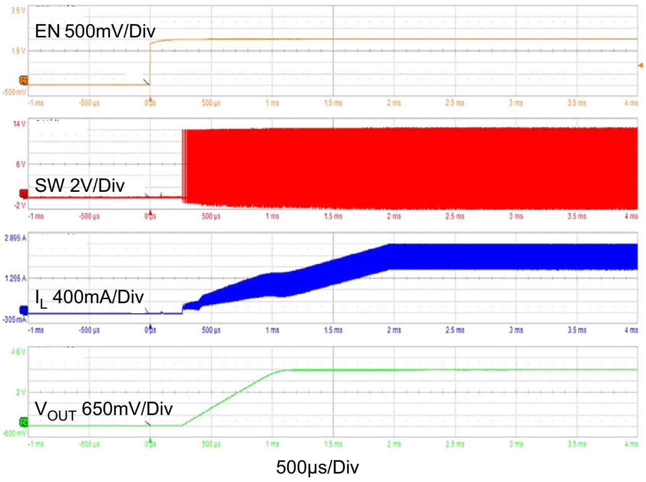


Figure 28. Startup through EN (I_{OUT} = 2A)

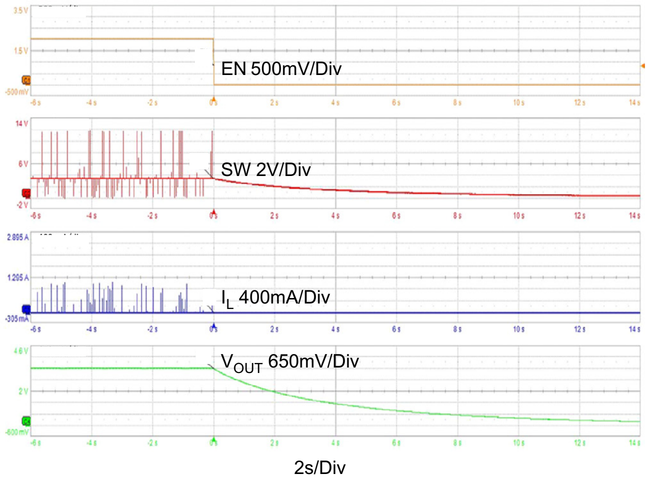


Figure 29. Shutdown through EN (I_{OUT} = 0A)

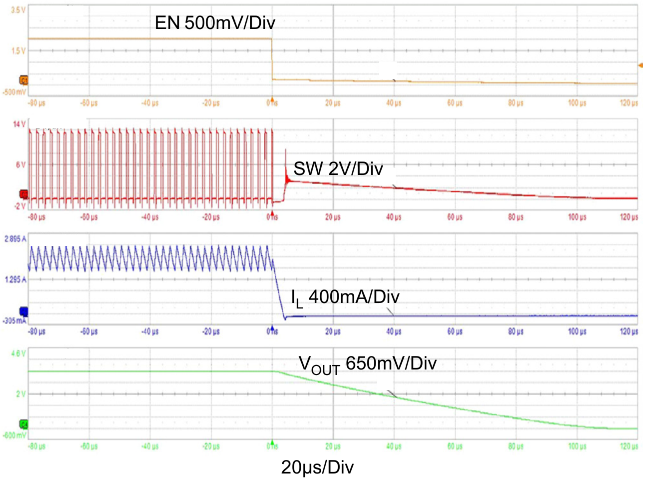


Figure 30. Shutdown through EN (I_{OUT} = 2A)

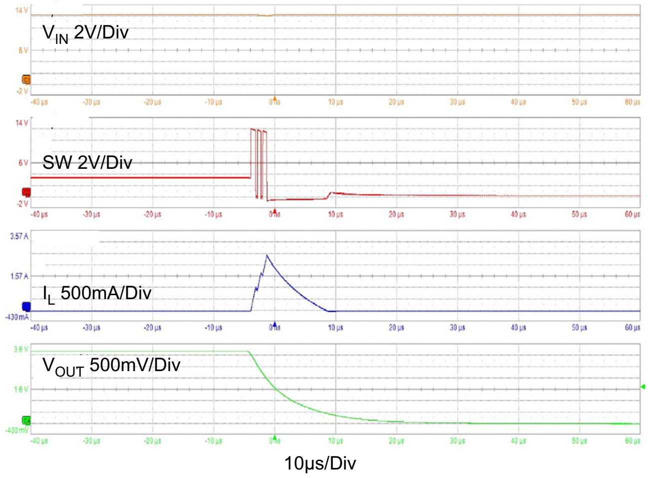


Figure 31. I_{OUT} = 0A to Short-Circuit

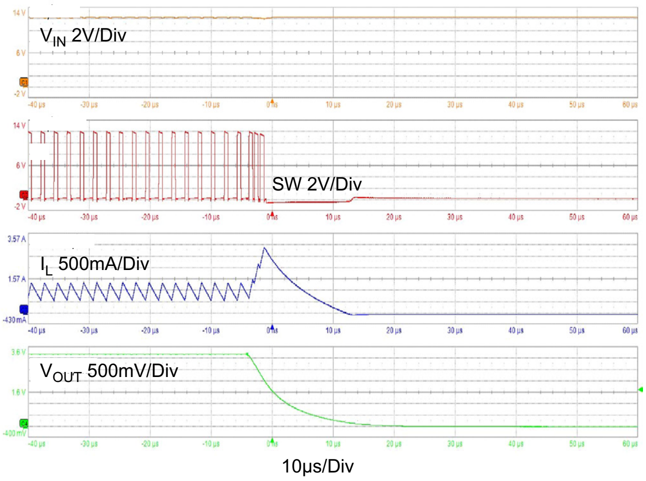


Figure 32. I_{OUT} = 1A to Short-Circuit

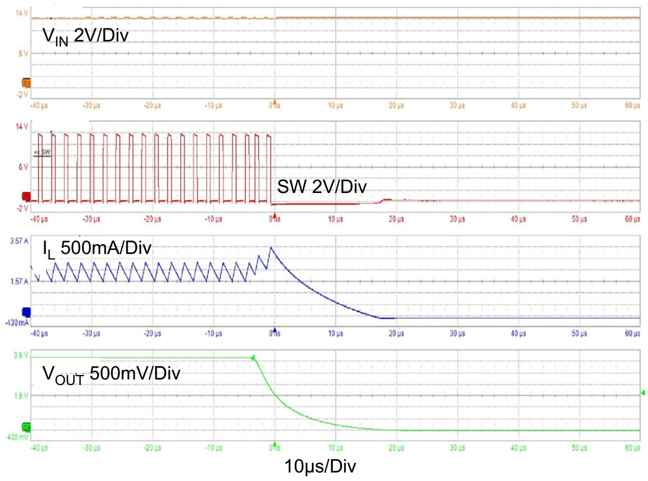


Figure 33. I_{OUT} = 2A to Short-Circuit

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted. (Cont.)

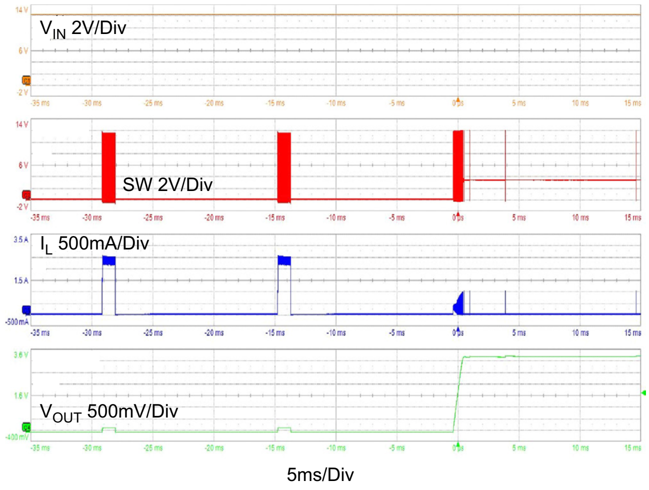


Figure 34. Short-Circuit to 0A Recovery

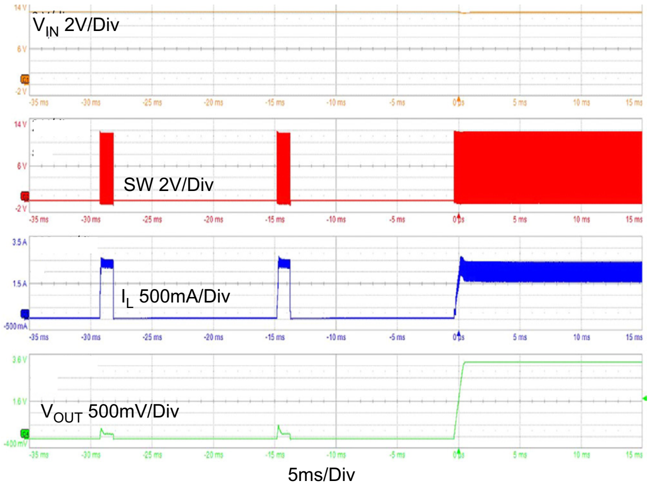


Figure 35. Short-Circuit to 2A Recovery

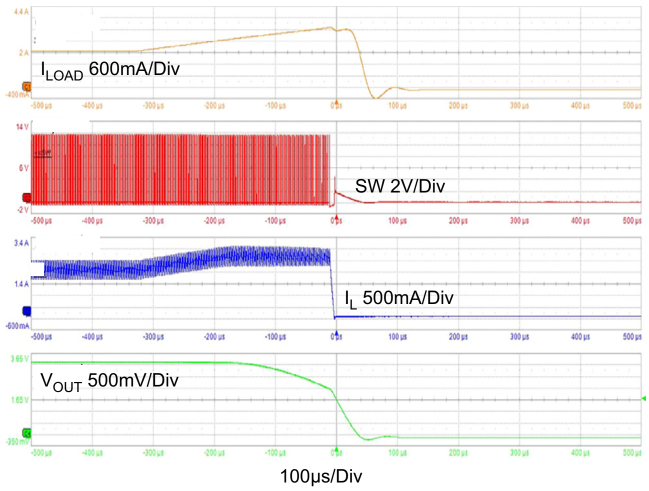


Figure 36. Low-Side Overcurrent (LSOC) Protection

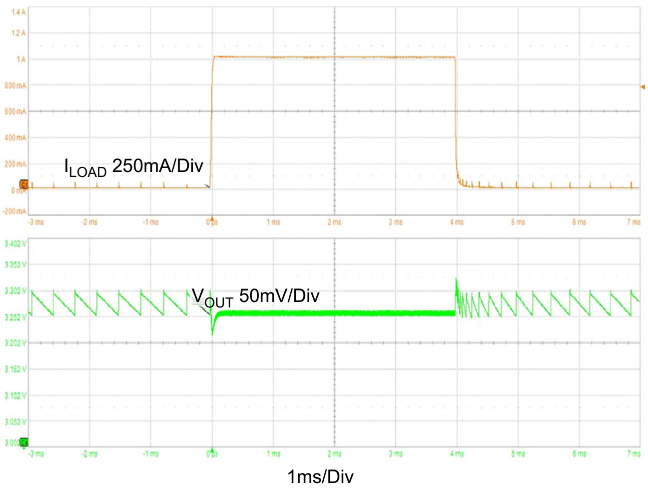


Figure 37. Load Transient I_{OUT} = 0A -> 1A -> 0 (0.5A/µs)

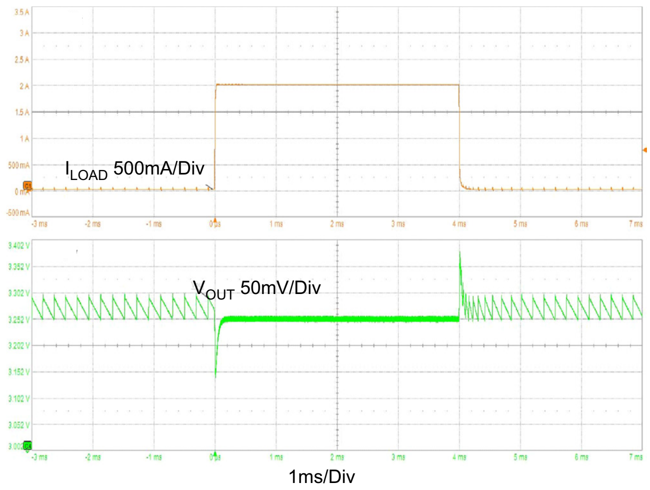


Figure 38. Load Transient I_{OUT} = 0A -> 2A -> 0 (0.5A/µs)

Typical Values are at T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L = 6.5µH, unless otherwise noted. (Cont.)

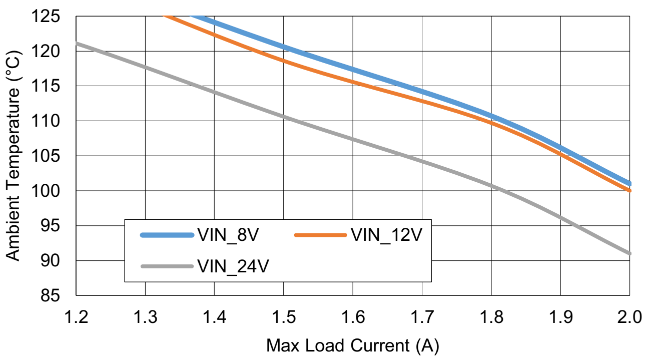


Figure 39. Max I_{OUT} vs Ambient Temp (V_{OUT} = 3.3V)

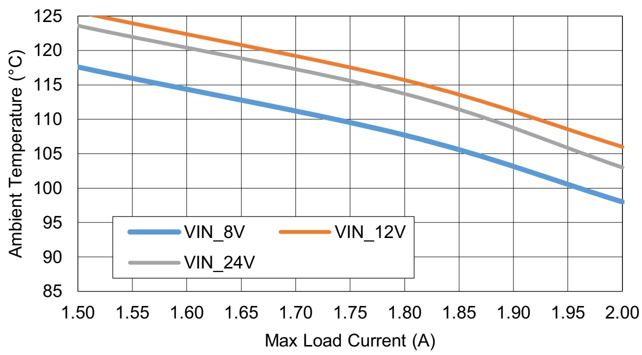


Figure 40. Max I_{OUT} vs Ambient Temp (V_{OUT} = 5V)

5. Functional Description

The RAA211320 is an integrated synchronous buck regulator with current mode constant on-time (COT) control. It can operate across a wide input voltage range from 4.5V to 30V with 2A capability. The output voltage is sensed on the FB pin through external feedback resistors, and it is compared with the internal reference of 0.765V to produce the control signal, which decides when to turn on the high-side FET. The internal COT circuit determines the on-time of the high-side FET based on the sensed value of V_{IN} and V_{OUT}.

At light load conditions, the regulator operates in DCM mode with a switching frequency determined by the output load (pulse-frequency modulation). The part transitions to CCM mode at higher loads with a constant frequency of 475kHz (see Figure 22).

5.1 Soft-Start

Soft-start forces the regulator to ramp up in a controlled process, which prevents high inrush current or output voltage overshoot at startup (see Figure 28). During soft-start, the reference voltage input of the error amplifier ramps up from 0V to its nominal value of 0.765V in 0.8ms.

If an overcurrent condition is initiated during startup, it occurs after the soft-start is done. V_{OUT} undervoltage protection only occurs after soft-start is completed.

5.2 Undervoltage Lockout

The regulator has undervoltage lockout (UVLO) on the VIN pin. It prevents the regulator from starting up until the input voltage exceeds 4.3V (typical). The UVLO threshold has approximately 360mV of hysteresis; therefore, the device continues to operate when V_{IN} decreases until it drops below 3.95V (typical). Hysteresis prevents the part from turning off during power-up if the V_{IN} is non-monotonic. Renesas recommends keeping the current path length from V_{IN} power supply or upstream regulator to the IC to be as small as possible to prevent jittering during V_{IN} turn-off and turn-on.

5.3 Enable Control

RAA211320 has an enable pin that turns the device on when pulled high. When EN is low, the IC goes into shutdown mode (see Figure 27 through Figure 30). RAA211320 has an EN rising threshold voltage of 1.3V (typical). EN threshold hysteresis is 100mV (typical). Also, RAA211320 has an enable shutdown threshold of 0.7V that allows the internal circuitry of the IC to shut down. Drive EN with impedance less than 10kΩ.

The EN pin can be tied directly to V_{IN} for an always-on operation. The device has an accurate enable threshold that allows you to program the V_{IN} UVLO threshold by connecting VIN to EN using a resistor divider. The UVLO is set with the resistor divider based on Equation 1, where V_{INR} is the rising threshold of V_{IN} UVLO, see Figure 41. Choose R_{EN1} and R_{EN2} so that $R_{EN1} \parallel R_{EN2}$ is less than 10kΩ.

(EQ. 1)
$$\frac{R_{EN1}}{R_{EN2}} = \left(\frac{V_{INR} - 1.3}{1.3}\right)$$

You can use Equation 2 to calculate the resulting input voltage for the part to be turned off:

(EQ. 2)
$$VINF = 1.2X\frac{R_{EN1} + R_{EN2}}{R_{EN2}}$$

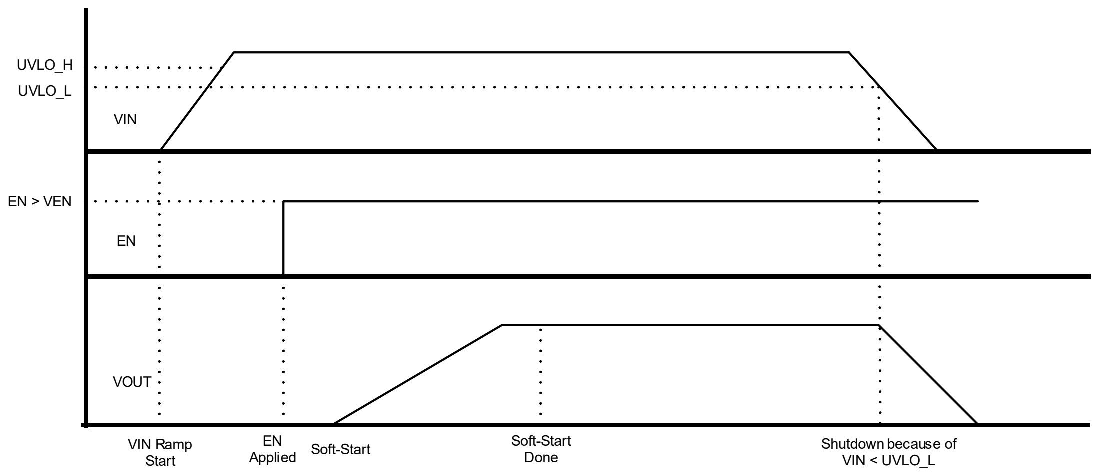


Figure 41. Timing Diagram with EN Turn On and V_{IN} UVLO Turn Off

5.4 Overcurrent Protection (OCP)

RAA211320 has a low-side overcurrent (LSOC) protection feature. After the regulator starts up, if the current through the internal low-side MOSFET exceeds the current limit, the device does not turn on the high-side FET until the LSOC condition clears.

5.5 V_{OUT} Undervoltage Protection (UVP)

RAA211320 has a V_{OUT} undervoltage (UV) protection feature. The internal undervoltage comparator compares the FB pin voltage to 65% of the reference voltage. When both LSOC is detected and this voltage drops below 65% of nominal (because of a drop in V_{OUT} to below 65% of its set point), the regulator stops switching and engages Hiccup mode operation at an interval of 13ms (see Figure 36).

5.6 Over-Temperature Protection (OTP)

Over-temperature protection (OTP) limits the maximum junction temperature in the RAA211320, and it limits the total power dissipation by turning off the regulator when the IC junction temperature exceeds 170°C (typical). There is a 40°C hysteresis for OTP. After the junction temperature drops below 130°C, the RAA211320 resumes operation.

5.7 System Level Fault Summary

The top-level faults (V_{IN} UVLO, OTP) disable VOUT, and the IC enters the POR state until the fault clears. The device then resumes normal operation according to the state of the EN pin.

Fault Type	Detection Activated When	Detection Delay	Circuit Behavior
V_{IN} UVLO Falling	EN is higher than threshold.	2µs	POR (Power on Reset), chip restarts from initial reset state when UVLO is satisfied.
Over-Temperature (OT) Shutdown	After EN pin goes high and IC is in active state.	Immediate	POR using internal regulator, hiccup timer is engaged.
V_{OUT} Undervoltage (UV)	After soft-start done, after Hiccup on-time.	Immediate	After soft-start is done (0.8ms), if V_{OUT} falls to 65% of set value and LSOC limit is reached, hiccup timer is engaged.
Low-Side Overcurrent (LSOC) Limit	Start of buck regulator switching.	Immediate	If LSOC is detected, the device keeps LS FET on until the current falls below LSOC limit.

6. Applications Information

Table 2 lists the recommended component selections for typical applications.

Table 2. Recommended Components Selection for Typical Application

V_{IN}(V)	V_{OUT}(V)	R_{FB1}(kΩ)	R_{FB2}(kΩ)	L(µH)	C_{OUT}(µF)
5	1.05	3.74	10	2.2	120
5	1.8	13.7	10	3.3	68
5	3.3	33.2	10	3.3	47
12	1.8	13.7	10	4.7	68
12	3.3	33.2	10	6.5	47
12	5	54.9	10	7.6	22
12	8	95.3	10	7.6	22
24	1.8	13.7	10	4.7	68
24	3.3	33.2	10	7.6	47
24	5	54.9	10	10	22
24	12	147	10	15	10

6.1 Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.765V with a resistor divider from V_{OUT} to the FB pin to GND based on Equation 3. The recommended R_{FB2} (see Figure 1) resistance is 10kΩ. See Table 2 for R_{FB1} and R_{FB2} values for typical V_{OUT} applications.

(EQ. 3) $$R_{FB1} = R_{FB2} X \frac{V_{OUT} - 0.765}{0.765}$$

High-impedance nodes are more prone to pick up noise. The recommended range of feedback resistors (R_{FB1} + R_{FB2}) is 5kΩ to 150kΩ.

Analog circuitry in the FET driver consumes 40µA of current and uses the SW pin as the current return path. For applications using zero-load conditions, this 40µA must be consumed by the feedback resistors to prevent positive drift of V_{OUT}. The factory recommends the following maximum impedance $(R_{FB1} + R_{FB2})_{max}$ for applications using zero-load condition, Equation 4, where R_{FB1} and R_{FB2} are in kΩ.

(EQ. 4) $$(R_{FB1} + R_{FB2})_{max} = 0.8X\frac{V_{OUT}}{40} \times 10^3$$

The absolute maximum output voltage for RAA211320 is 16V. The maximum operating output voltage for a given input voltage is determined by DMAX, which is a function of minimum-off time and switching frequency.

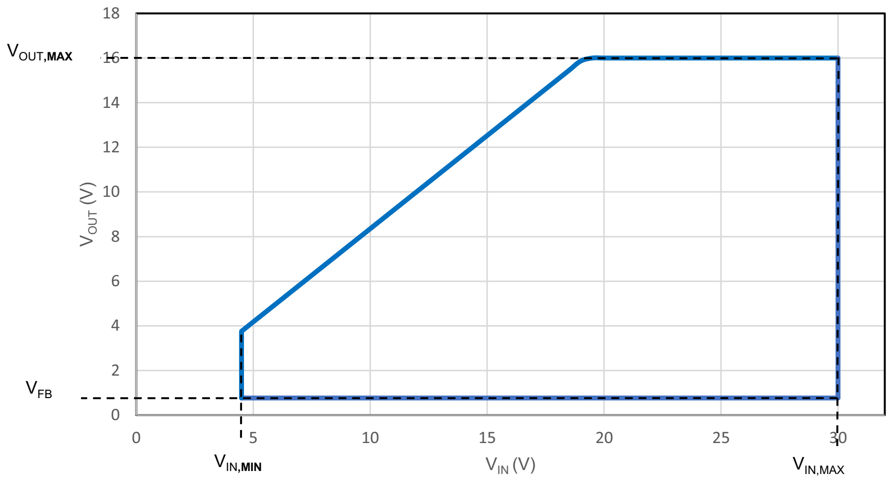


Figure 42. Operating Range for V_{IN} and V_{OUT}

6.2 Inductor Selection

Select an inductor with the lowest possible DC resistance (DCR) to minimize power losses. The saturation current rating of the inductor must be high enough to accommodate the DC load current and AC ripple current with an additional margin for overload conditions. The inductor of the buck converter determines its ripple current; therefore, it also determines its output ripple voltage. Selecting a higher inductance value results in lower output ripple voltage, but it may increase the response time and output voltage drop during a load transient. The ripple voltage and current are approximated by Equation 5 and Equation 6.

(EQ. 5) $$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{sw} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

(EQ. 6) $$\Delta V_{OUT} = \Delta I \times ESR$$

A reasonable starting point for the inductor ripple current is 20% to 50% of the maximum output current. You can reference Table 2 for selecting the inductor value for typical V_{OUT} applications.

During overcurrent and short-circuit conditions, the peak inductor current becomes higher than the current during normal operation. Renesas recommends using inductors with soft saturation characteristics.

6.3 Input Capacitor Selection

The input capacitor in a buck converter maintains the input voltage by suppressing the voltage ripple induced by discontinuous switching current. Approximate the required RMS current rating $I_{IN(RMS)}$ of the input capacitor with Equation 7, where $I_{OUT(MAX)}$ is the maximum average load current and D is the duty ratio.

(EQ. 7)

$$I_{IN(RMS)} = I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

When D equals 0.5, $I_{IN(RMS)}$ has the highest value which is $I_{OUT(MAX)}/2$.

The voltage rating of the input capacitor must be higher than the maximum input voltage. Calculate the required capacitance CIN of the input capacitor, to ensure the expected peak-to-peak input voltage ripple $\Delta V_{IN,}$ by using Equation 8 where f_{SW} is the switching frequency.

(EQ. 8)

$$CIN = I_{OUT(MAX)} \times \frac{D \times (1 - D)}{f_{SW} \times \Delta V_{IN}}$$

The required capacitance also has the maximum value when D equals 0.5.

Renesas recommends using low ESR/low ESL ceramic capacitors across the input of the regulator. When selecting the ceramic capacitors for power supply applications, consider that the effective capacitance reduces with DC bias voltage across it; therefore, you need to consult the capacitor datasheet to understand the impact of this effect. Renesas recommends using X5R/X7R dielectric ceramic capacitors because of their small temperature coefficient.

If the input to the regulator is directed through a high-impedance path, Renesas recommends adding an electrolytic capacitor (in addition to the ceramic capacitor) to dampen the input voltage oscillation effects.

6.4 Output Capacitor Selection

Output capacitor selection impacts the steady state and transient performance of the buck converter. Factors such as output ripple voltage, output voltage excursion during transients, and control loop stability should be considered when selecting the output capacitor. Renesas recommends using the X5R/X7R dielectric ceramic for the output capacitor. When selecting the ceramic capacitor, consider that the effective capacitance reduces with DC bias voltage across it.

The effective capacitance of the ceramic capacitor is used when determining the output voltage ripple. The required capacitance $C_{OUT(RIPPLE)}$ is calculated using Equation 9, where ΔI_L is the inductor peak-to-peak current ripple and f_{SW} is the switching frequency:

(EQ. 9)

$$C_{OUT(RIPPLE))} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT(RIPPLE)}}$$

To meet the output voltage variation requirements during load step up and load step down transients, the required capacitance $C_{OUT(STEPUP)}$ is calculated using Equation 10, and $C_{OUT(STEPDOWN)}$ is calculated using Equation 11, where I_{STEP} is the transient load step and ΔV_{OUT} is the expected voltage variation during the transient.

(EQ. 10)

$$C_{OUT(STEPUP)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT}}$$

(EQ. 11)

$$C_{OUT(STEPDOWN)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times V_{OUT} \times \Delta V_{OUT}}$$

To have a stable control loop with adequate gain margin, phase margin, and bandwidth, calculate the required capacitance $C_{OUT(LOOP)}$ using Equation 12, where $C_{OUT(LOOP)}$ is in µF and V_{OUT} is in V.

(EQ. 12) $$C_{OUT(LOOP)}(\mu F) = \frac{162.7}{V_{OUT}}$$

Select the output capacitors so that prior stated requirements are met: the total capacitance should be greater than the highest value calculated in Equation 9, Equation 10, Equation 11, or Equation 12.

See Table 2 for recommended values of output capacitor for typical V_{OUT} applications.

6.5 BOOT Refresh and Capacitor Selection

After EN and before the start-up process, approximately 85µs is driven high, and the RAA211320 turns on the internal BOOT voltage regulator. This action charges the boot capacitor before the start-up process begins. BOOT UVLO function is provided to prevent the turn on of HS FET at low BOOT Voltages. When the BOOT voltage is below 2.5V, the regulator skips the HS pulse and provides the LS pulse until BOOT voltage rises above 2.5V.

A capacitor is needed between the BST pin and the SW pin to provide gate voltage for the high-side internal MOSFET. For most applications, Renesas recommends using a ceramic capacitor greater than 10V X5R/X7R 0.1µF as the bootstrap capacitor.

7. Component Placement and Layout Suggestions

The printed circuit board (PCB) layout is critical for properly operating the RAA211320. Renesas recommends the following guidelines to achieve good performance.

- Use a combination of a bulk capacitor and smaller ceramic capacitors with low ESL for input capacitors, and place them as close as possible to the IC. Place the input ceramic capacitor(s) as close as possible to the IC.
- Keep the power loop (input ceramic capacitor, IC VIN, and PGND pins) as small as possible to minimize switch node voltage ringing caused by parasitic inductance in the PCB traces. Minimizing loop size also results in better EMI performance.
- Place bootstrap capacitors close to the IC between BST and SW pins on the same side of the PCB as the IC. Renesas recommends using a 0.1µF ceramic capacitor.
- Keep the phase node copper area small to reduce the parasitic capacitance but large enough to handle the load current. Place the inductor close to the regulator.
- Route the output voltage feedback signal away from SW and BST. Place feedback resistors close to the FB pin of the regulator.
- Place an output capacitor close to the inductor.

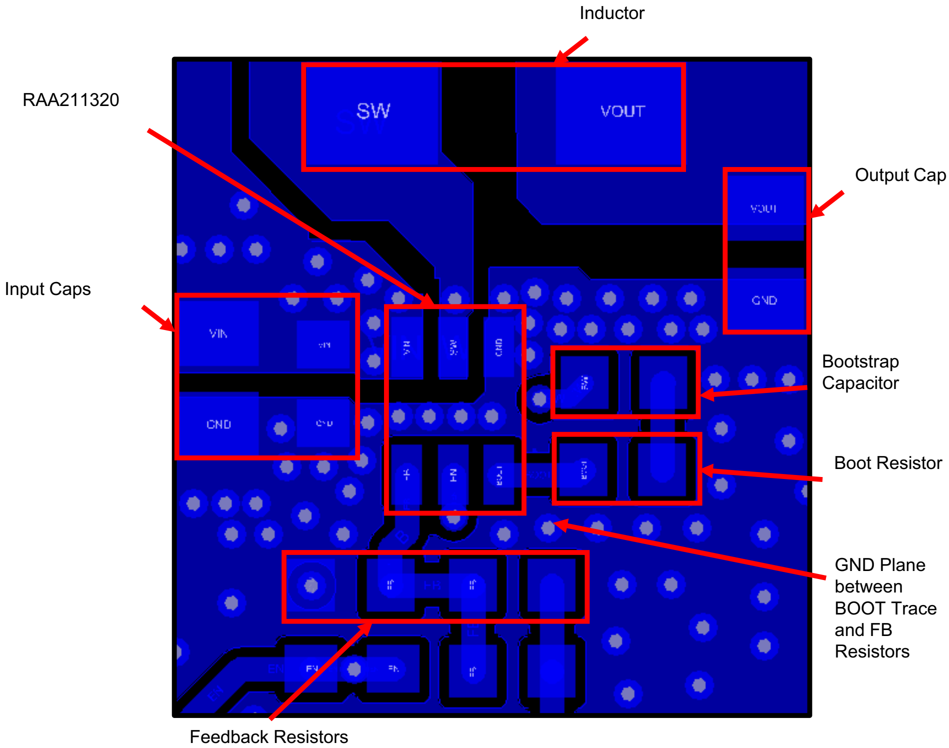
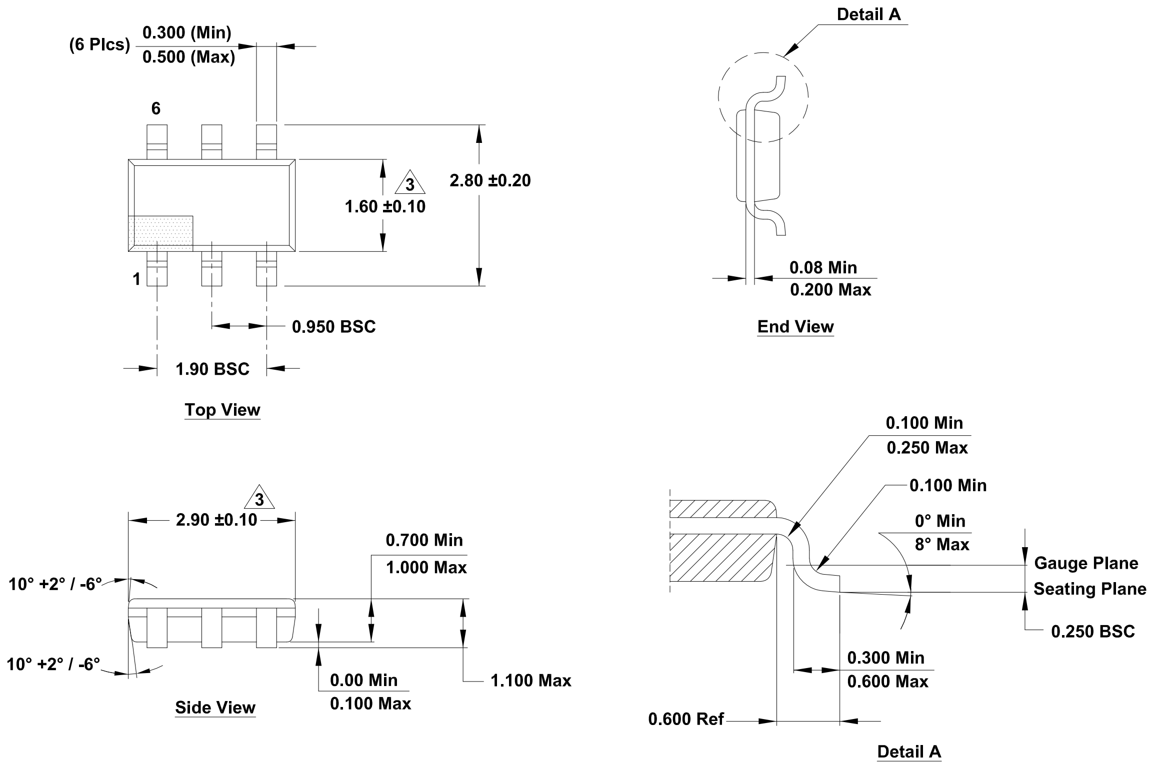


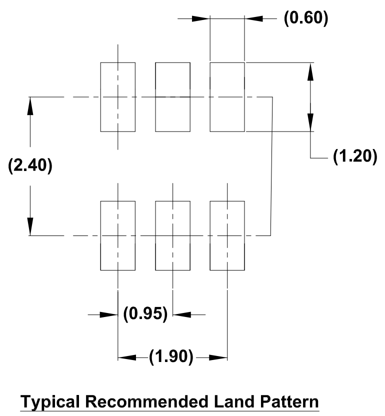
Figure 43. Example Layout for RAA211320

8. Package Outline Drawing

For the most recent package outline drawing, see P6.064C.

P6.064C
6 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 2, 12/20





Note:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. (Δ) Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

9. Ordering Information

Part Number[1][2]	Part Marking[3]	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp Range
RAA2113204GP3#JA0	320	6Ld TSOT-23	P6.064C	Reel, 3k	-40 to +125°C
RTKA211320DE0030BU	RAA211320 Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA211320 device page. For more information about MSL, see TB363.
3. The part marking is located on the bottom of the part.
4. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.01	May 18, 2023	Corrected Note in the Thermal Information section. Updated the output voltage minimum from 0.786V to 0.765V in the Recommended Operating Conditions section. Removed VOUT Voltage Range from the EC table. Updated Figure 40.
1.00	Apr 12, 2023	Initial release.

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