RAA211605

60V 0.5A DC/DC Step-Down Regulator with 450kHz Switching Frequency

The RAA211605 is a DC/DC step-down buck regulator that supports a wide operating input voltage range (from 4.5V to 60V) and adjustable output voltage. It can deliver up to continuous 0.5A output current with excellent load regulation and line regulation performance.

The RAA211605 employs peak-current mode control with a 450kHz nominal switching frequency and pulse skipping mode under light load. It provides fast and robust transient response performance. Internally implemented soft-start and loop compensation circuitry also help to simplify design and minimize BOM cost.

The RAA211605 also offers protection features such as cycle-by-cycle current limit, input voltage UVLO, output voltage undervoltage protection, and thermal shutdown.

The RAA212605 is available in the TSOT23-6 package.

Features

- Wide input voltage range: 4.5V to 60V
- Adjustable output voltage
- Up to 0.5A output current
- Internal compensation
- Internal soft start
- 600mΩ internal MOSFET
- 450kHz nominal switching frequency
- Pulse skipping mode under light load condition
- Cycle-by-cycle current limit
- Input voltage UVLO and output voltage undervoltage protection
- Thermal shutdown
- Available in the TSOT23-6 package

Applications

- Power meters
- Battery powered devices
- Distributed power systems
- Handheld power tools

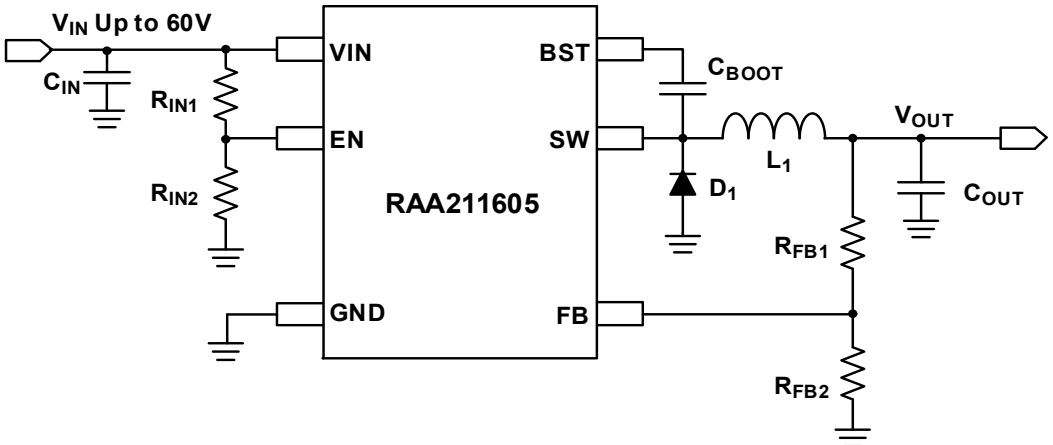

Figure 1. Typical Application Schematic

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1. Overview

1.1 Block Diagram

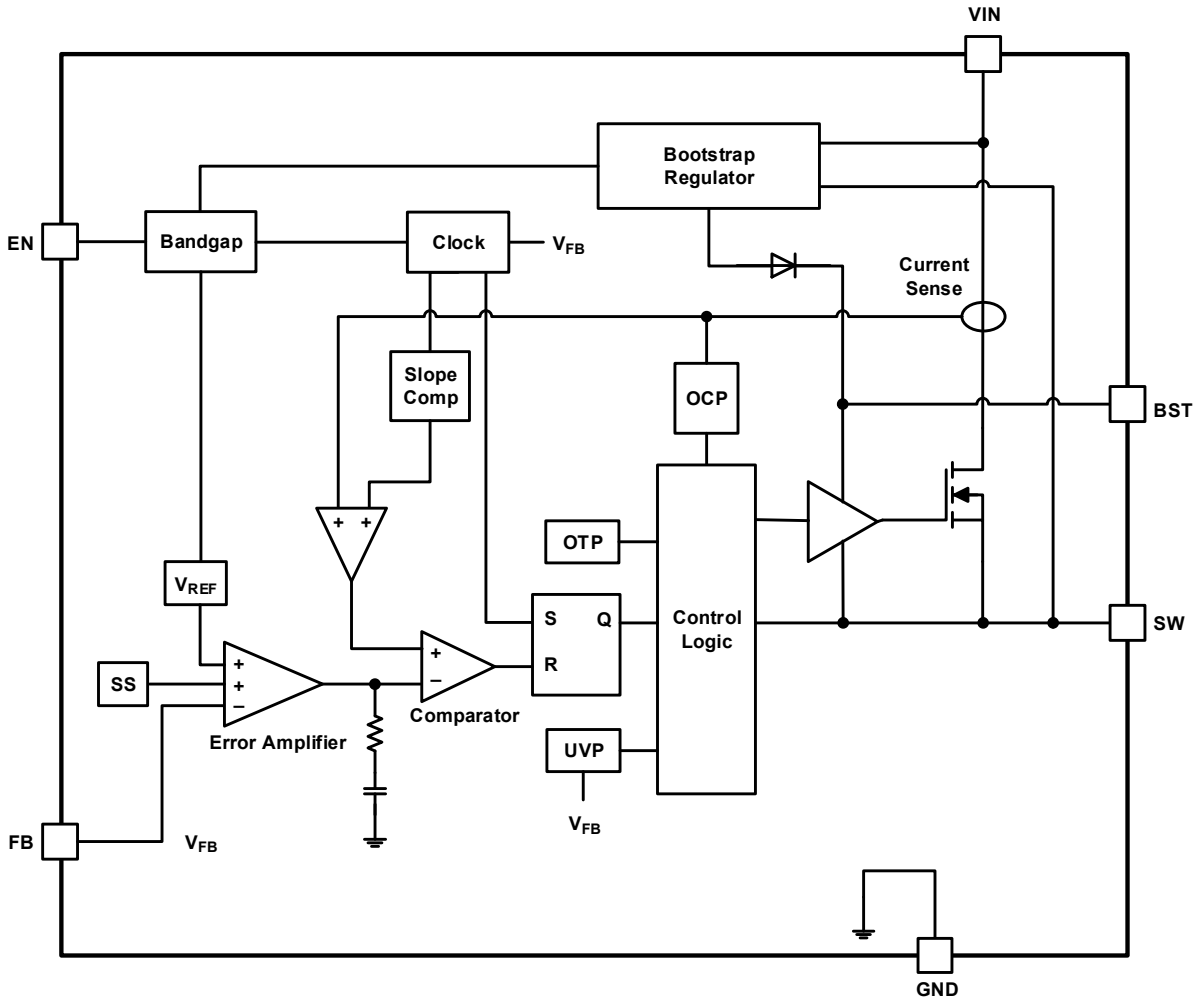
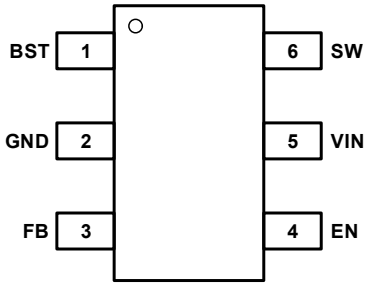


Figure 2. RAA211605 Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	BST	The bootstrap circuit supply pin. Connect this pin to SW with a capacitor to provide bias voltage for the integrated MOSFET gate driver.
2	GND	Ground connection pin
3	FB	The FB pin connects to the inverting input of the feedback error amplifier and should be connected to a properly selected resistor divider from VOUT to ground to set the output voltage.
4	EN	The enable pin. It is high voltage tolerant and therefore, can be directly connected to VIN.
5	VIN	Te VIN pin is connected to the drain of the integrated MOSFET. This pin is also connected to the input of internal linear regulator that provide bias for the IC. Connect this pin to the input rail.
6	SW	This pin is the phase node of the regulator and is connected to the source of the integrated MOSFET. Connect this pin to the inductor, diode, and boot capacitor.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Min	Max	Unit
VIN	-0.3	65	V
EN	-0.3	65	V
SW	-0.7	V_{IN} + 0.3	V
BST		SW + 4	V
BST to SW	-0.3	4	V
All other pins	-0.3	4	V
Operating junction temperature	–40	150	°C
Storage temperature range	–65	150	°C
ESD Ratings	**Value**		**Unit**
Human Body Model (tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2018)	750		V
Latch-Up (tested per JESD78E; Class 2, Level A)	100		mA

1. All voltages referenced to VSS unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter	Min	Max	Unit
Input Voltage, V_{IN}	4.5	60	V
Output Voltage, V_{OUT}	0.8	$V_{IN} \times D_{MAX}$[1]	V
Output Current, I_{OUT}	0	0.5	A
Junction Temperature, T_J	-40	125	°C

1. D_{MAX} is 89% to 91%. Also, see the BST Refresh section for refresh considerations.

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
6 Ld TSOT23	114	42

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is on the top side of the package.

3.4 Electrical Specifications

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted. Min and Max values apply across the junction temperature range, -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		4.5		60	V
Shutdown Current	I_{SHDN}			2.75		µA
Quiescent Current	I_Q	EN = 2V, V_{FB} = 0.825V, No Switching		300	425	µA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 5V to 60V		0.25		µV/V
V_{IN} UVLO/EN						
V_{IN} UVLO Rising Threshold			4.05	4.25	4.45	V
V_{IN} UVLO Falling Hysteresis				250		mV
EN Rising Threshold			1.15	1.275	1.45	V
EN Falling Hysteresis				125		mV
Feedback Voltage Reference						
Feedback Voltage Reference	V_{FB}	25 °C	0.788	0.8	0.812	V
		-40 °C to 125 °C	0.776	0.8	0.824	V
Integrated MOSFET						
High-side FET On-Resistance	RDS_onh			600		mΩ
Soft-Start						
Internal Soft-Start Time	t_{SS}			1		ms
Oscillator/PWM Comparator						
Switching Frequency	f_{SW}	V_{FB} = 0.8 V	409.5	450	500.5	kHz
Minimum On-Time	t_{ON_MIN}			96		ns
Minimum Off-Time	t_{OFF_MIN}			212		ns
Overcurrent Protection (OCP)/VOUT Undervoltage Protection (UVP)						
Peak Current Limit Threshold	I_{HSOC}	Duty ratio = 0.9, 25 °C	0.7	0.9		A
VFB Undervoltage Threshold				0.24		V
Foldback Frequency		V_{FB} = 0V		100		kHz
Hiccup Time	t_{HICCUP}			23		ms
Thermal Shutdown (OTP)						
Thermal Shutdown Threshold				155		°C
Thermal Shutdown Recovery Hysteresis				20		°C

1. Compliance to datasheet limits is established by one or more methods: production test, characterization, and/or design.

4. Typical Performance Curves

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted.

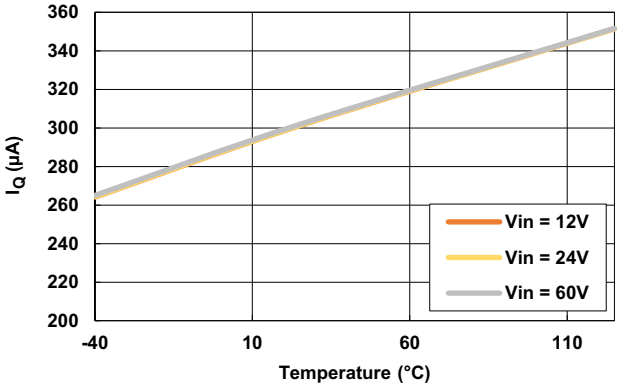


Figure 3. Quiescent Current vs Temperature

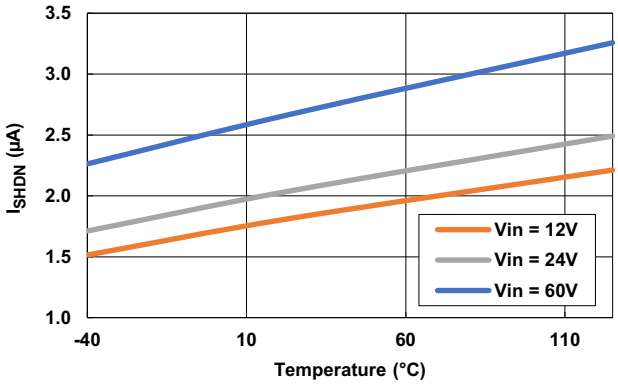


Figure 4. Shutdown Current vs Temperature

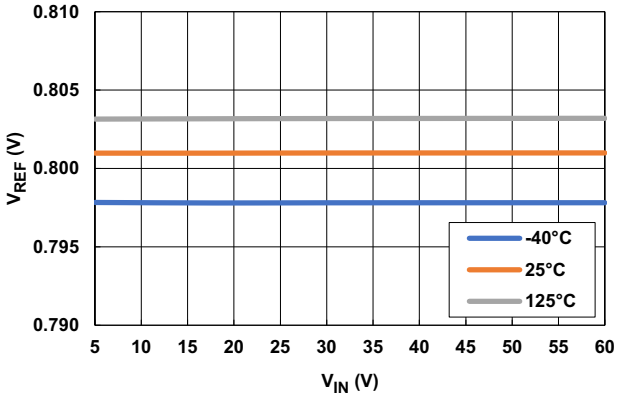


Figure 5. V_{REF} vs Temperature

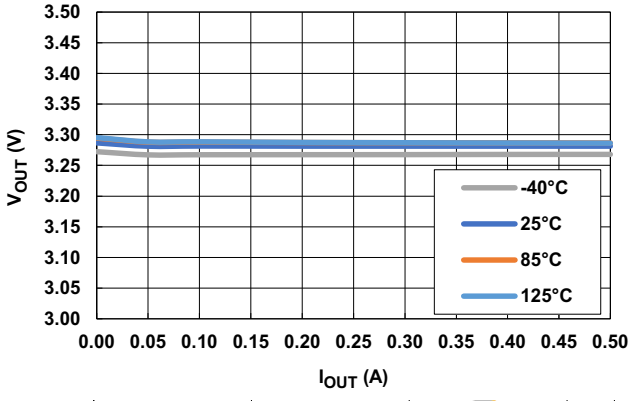


Figure 6. V_{OUT} vs Load

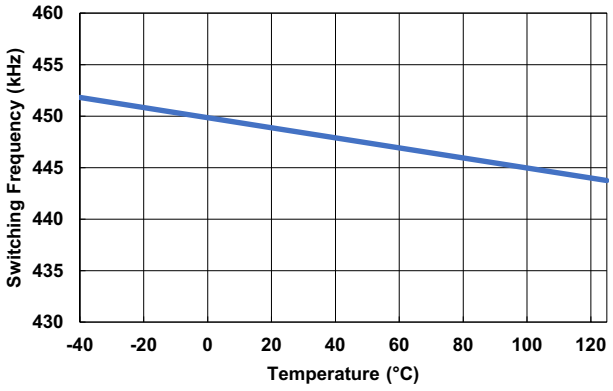


Figure 7. Switching Frequency vs Temperature

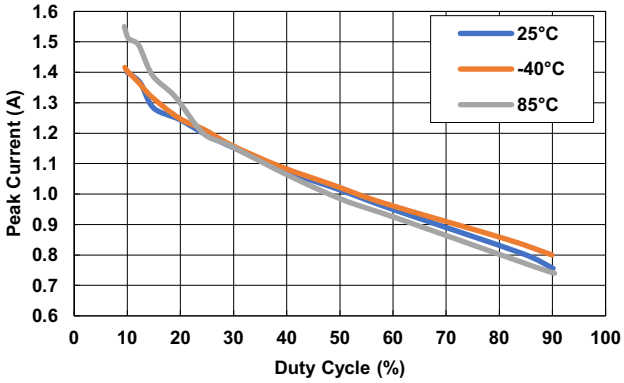


Figure 8. Peak Current vs Duty Cycle (V_{OUT} = 5V)

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted.

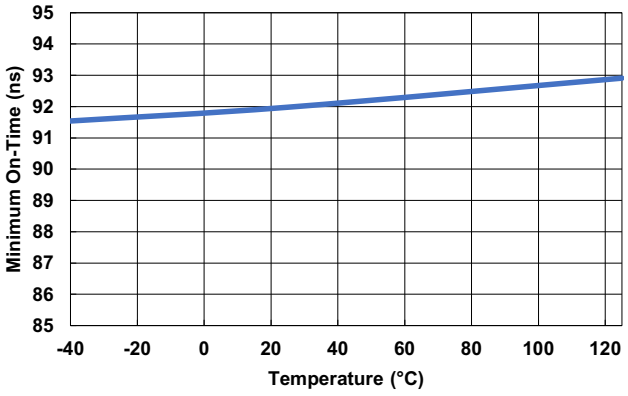


Figure 9. Minimum On-Time vs Temperature

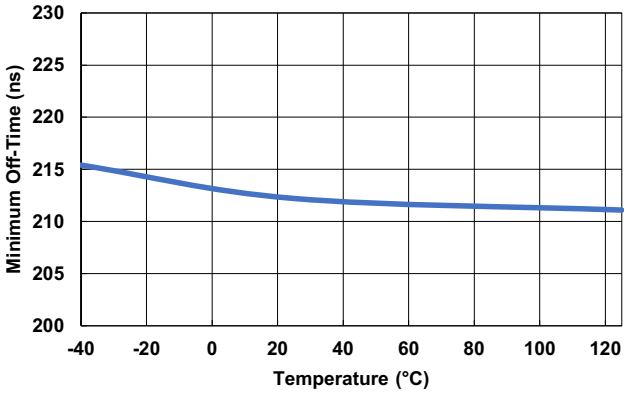


Figure 10. Minimum Off-Time vs Temperature

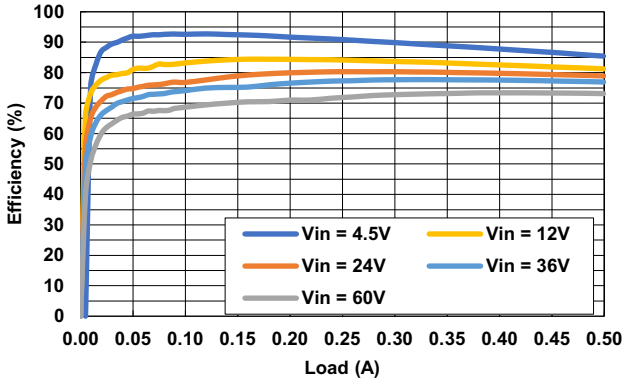


Figure 11. Efficiency (V_{OUT} = 3.3V)

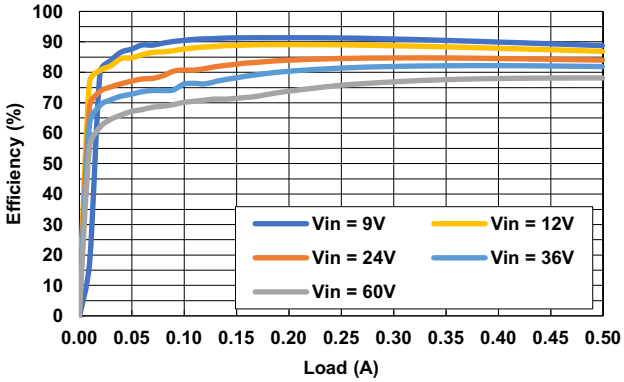


Figure 12. Efficiency (V_{OUT} = 5V)

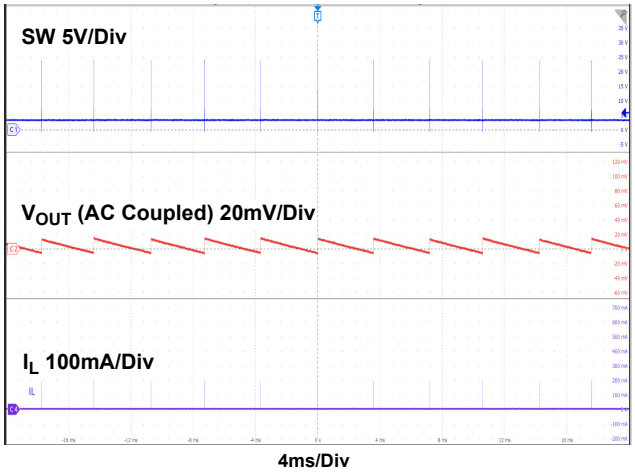


Figure 13. Typical Operation (No Load)

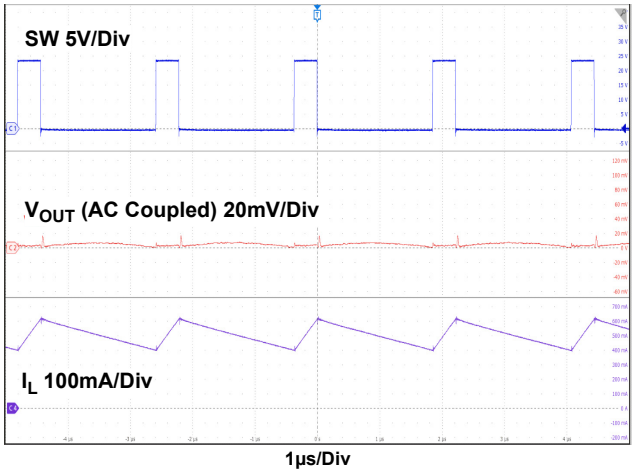


Figure 14. Typical Operation (Full Load)

Typical Values are at T_A = +25°C, V_{IN} = 24V, V_{OUT} = 3.3V, C_{OUT} = 10µF, unless otherwise noted.

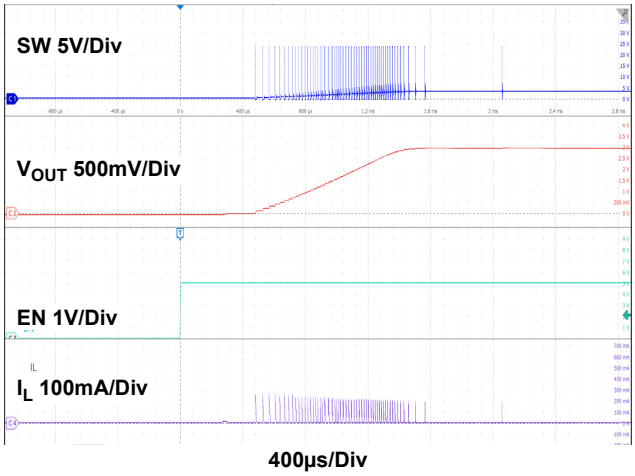


Figure 15. Startup by EN (No Load)

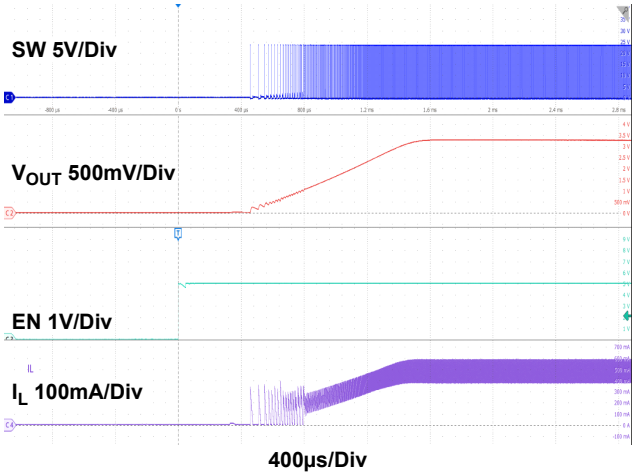


Figure 16. Startup by EN (Full Load)

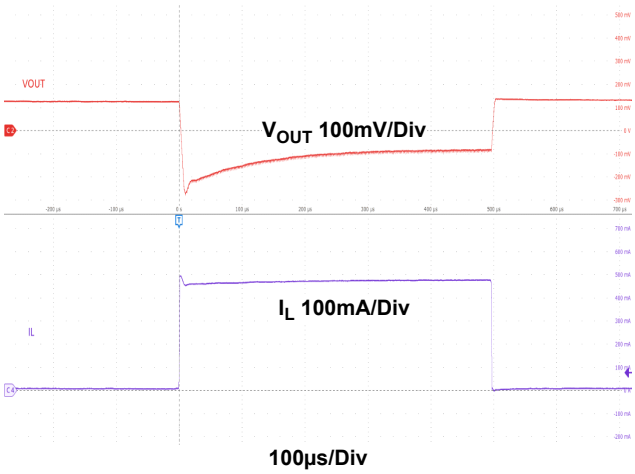


Figure 17. Load Transient Response (0 to 500mA)

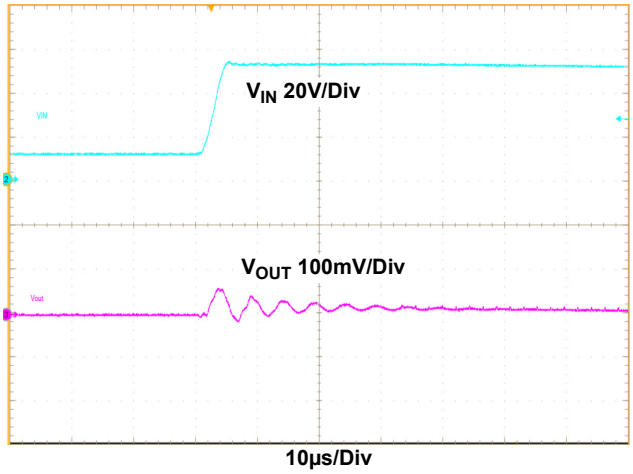


Figure 18. Line Transient Response at Full Load (12V to 48V)

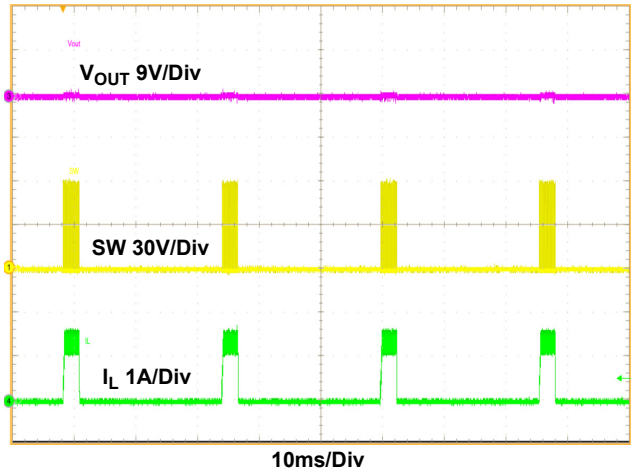


Figure 19. Overcurrent Protection (V_{IN} = 60V, V_{OUT} = 0)

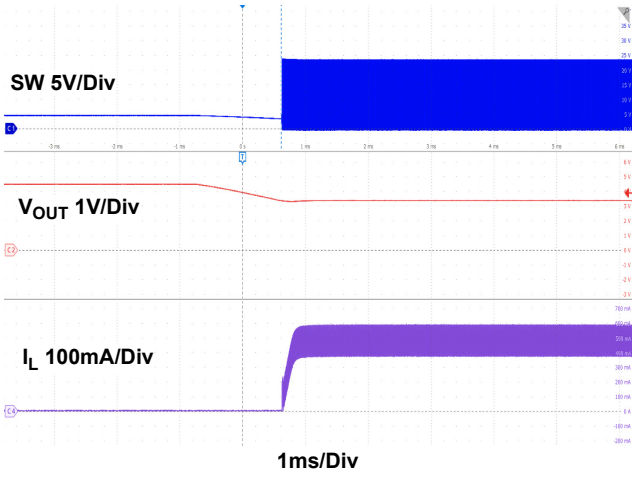


Figure 20. Overvoltage Protection (I_{OUT} = 500mA)

5. Functional Description

The RAA211605 is a peak current mode DC/DC step-down regulator with internal loop compensation. At light load or no load, it operates in pulse skipping mode. As the load increases and the regulator transitions from DCM to CCM, it operates at a fixed switching frequency of 450kHz.

5.1 Soft-Start

Soft-start forces the regulator output to ramp up in a controlled fashion, which helps reduce input inrush current into the buck output capacitors. During the soft-start period for the buck converter, the reference voltage of the error amplifier ramps from 0V to its nominal value of 0.8V in approximately 1ms.

5.2 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the RAA211605 from operating until the input voltage exceeds 4.25V (typical). The UVLO threshold has approximately 250mV of hysteresis, therefore the device continues to operate when V_{IN} decreases until it drops below 4V (typical). Hysteresis prevents the part from turning off during power-up if V_{IN} is non-monotonic.

5.3 Current Limit

The RAA211605 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 0.9A (typical) and turns off the switch until the next switching cycle begins. As the output voltage and the voltage on the FB pin decreases, the frequency foldback function kicks in. When VFB is 0, the foldback frequency is around 100kHz.

5.4 Output Undervoltage Protection

The internal undervoltage comparator compares the FB pin voltage to 30% of the reference voltage. When this voltage drops below 30% of nominal (because of a drop of V_{OUT} to below 30% of its setpoint), the controller turns off the internal high-side FET and engages Hiccup mode operation at an interval of 23ms. If there is a short on the output, switching frequency folds back to 100kHz as short-circuit protection. When this fault is removed and V_{OUT} is above 30% of the nominal setpoint, the controller returns to normal voltage regulation.

5.5 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 155°C (typical). After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 135°C (typical).

6. Applications Information

The recommended component selections for typical applications are listed in Table 1.

Table 1. Recommended Components Selection for Typical Applications

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{OUT}
0.8	0	20	8.2	22uF/10V/X7R
1.8	24.9	20	18	22uF/10V/X7R
3.3	61.9	20	33	10uF/10V/X7R
5	105	20	47	10uF/10V/X7R
12	280	20	120	4.7uF/50V/X7R
24	576	20	220	4.7uF/50V/X7R

6.1 Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V with a resistor divider from VOUT to FB pin to GND based on Equation 1. The recommended R_{FB2} (see Figure 1) resistance is 20kΩ. Table 1 can be referenced for R_{FB1} and R_{FB2} for typical V_{OUT} applications.

(EQ. 1) $$R_{FB1} = R_{FB2} \bullet \frac{V_{OUT} - 0.8}{0.8}$$

6.2 Input Undervoltage Lockout

The input undervoltage lockout level can be set with a resistor divider from VIN to EN pin to GND based on Equation 2 (see Figure 1).

(EQ. 2) $$R_{IN1} = R_{IN2} \bullet \frac{V_{INR} - 1.275}{1.275}$$

where V_{INR} is the minimum input voltage for the part to turn on. The resulting input voltage V_{INF} for the part to be turned off is calculated based on Equation 3 (see Figure 1).

(EQ. 3) $$V_{INF} = 1.15 \bullet \frac{R_{IN1} + R_{IN2}}{R_{IN2}}$$

6.3 Inductor Selection

The inductor of the buck converter determines its current ripple and factors such as inductance, saturation current, DC resistance should be considered when selecting it. Choosing the inductance requires the choice of inductor current ripple. Larger inductance results in less inductor current ripple and therefore less output voltage ripple. However, it may increase the response time and output voltage variance during a load transient. A reasonable starting point for inductor current ripple is 30% to 60% of the maximum output current. Considering the wide operating input voltage range of the part, Renesas recommends calculating required inductance L based on Equation 4. Table 1 can be referenced for selecting the inductance for typical V_{OUT} applications.

(EQ. 4) $$L = 10 \bullet V_{OUT}$$

where V_{OUT} is the output voltage in V and the inductance L is in µH. In addition, the saturation current rating of the inductor should be higher than the peak current under overload conditions. For lower loss and smaller output voltage ripple, the inductor with smallest possible DC resistance should be selected provided its mechanical dimensions meet application requirements.

The RMS current rating of the inductor needs to meet the maximum load and the recommended rating of the saturation current is 1A or higher.

6.4 Input Capacitor Selection

The input capacitor is used in the Buck converter to maintain the input voltage by suppressing the voltage ripple induced by discontinuous switching current. The required RMS current rating $I_{IN(RMS)}$ of the input capacitor is calculated using Equation 5.

(EQ. 5) $$I_{IN(RMS)} = I_{OUT(MAX)} \bullet \sqrt{D \bullet (1 - D)}$$

where $I_{OUT(MAX)}$ is the maximum average load current and D is the duty ratio. When D equals 0.5, $I_{IN(RMS)}$ has the maximum value which is $I_{OUT(MAX)}/2$.

The voltage rating of the input capacitor should be higher than the maximum input voltage. The required capacitance C_{IN} of the input capacitor to ensure the expected peak-to-peak input voltage ripple ΔV_{IN} is calculated using Equation 6:

(EQ. 6) $$C_{IN} = I_{OUT(MAX)} \bullet \frac{D \bullet (1 - D)}{f_{SW} \bullet \Delta V_{IN}}$$

where f_{SW} is the switching frequency. The required capacitance also has the maximum value when D equals 0.5. Renesas recommends using ceramic capacitors as an input capacitor, which has low ESR and low ESL. When selecting the ceramic capacitor, consider that the effective capacitance reduces with DC bias voltage across it. Also, Renesas recommends using X7R ceramic capacitors because of their small temperature coefficient.

If the part is connected to the power source through a high impedance path, Renesas recommends adding an electrolytic capacitor in addition to the ceramic capacitor to damp the input voltage oscillation.

6.5 Output Capacitor Selection

The output capacitor determines both steady-state performance and transient performance of the Buck converter. Factors such as output voltage ripple, output voltage variation during transients, and control loop stability should be considered when selecting the output capacitor. For this part, Renesas recommends using X7R ceramic capacitors as the output capacitor. When selecting the ceramic capacitor, consider that the effective capacitance reduces with DC bias voltage across it.

For the ceramic capacitor, its capacitance is dominating the voltage ripple. Therefore, the required capacitance $C_{OUT(RIPPLE)}$ for the expected peak-to-peak output voltage ripple $\Delta V_{OUT(RIPPLE)}$ is calculated using Equation 7.

(EQ. 7) $$C_{OUT(RIPPLE)} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet \Delta V_{OUT(RIPPLE)}}$$

where ΔI_L is the inductor the inductor peak-to-peak current ripple and f_{SW} is the switching frequency.

To meet the output voltage variation requirements during load step-up and load step-down transients, the required capacitance $C_{OUT(STEPUP)}$ is calculated using Equation 8 and $C_{OUT(STEPDOWN)}$ is calculated using Equation 9.

(EQ. 8) $$C_{OUT(STEPUP)} = \frac{L \bullet \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \bullet (V_{IN} - V_{OUT}) \bullet \Delta V_{OUT}}$$

(EQ. 9) $$C_{OUT(STEPDOWN)} = \frac{L \bullet \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \bullet V_{OUT} \bullet \Delta V_{OUT}}$$

where I_{STEP} is the transient load step and ΔV_{OUT} is the expected voltage variation during the transient.

For the control loop to be stable with gain and phase margin in addition to sufficient bandwidth, the required capacitance $C_{OUT(LOOP)}$ is derived using Equation 10.

(EQ. 10) $$C_{OUT(LOOP)} = \frac{32}{V_{OUT}}$$

where $C_{OUT(LOOP)}$ is in µF and V_{OUT} is in V. Select the output capacitors such that aforementioned requirements are met, which means the total output capacitance should be higher than the maximum value of the above calculated capacitance.

For convenience, Table 1 can be referenced when selecting output capacitors for typical V_{OUT} applications.

6.6 Diode Selection

The RAA211605 requires a freewheeling diode for the inductor current to flow when the internal high-side MOSFET is turned off. Select a diode with a reverse voltage rating at least 20% higher than the maximum input voltage. The continuous current rating of the diode should be greater than the highest output current. For better efficiency, select a diode with low forward voltage drop and fast reverse recovery time. Schottky diodes are recommended for this application.

6.7 BST Refresh

BST voltage is generated by an internal 3V regulator and acts as the power supply for gate driver of the high-side MOSFET. The internal regulator charges the boot capacitor when the SW node is pulled low during the switching cycle, in addition to any time VIN - SW is greater than 3V. For the typical case of high VIN voltage and low VOUT voltage (VIN – VOUT > 3V), no switching is needed to keep BST refreshed and the device can skip cycles for an unlimited duration in light load for improved efficiency. If an application runs in the dropout mode of the BST regulator (VIN-VOUT < 3V), Renesas recommends using a minimum load of 5-10mA to ensure some occasional switching, which keeps BST refreshed.

6.8 Boot Capacitor Selection

A capacitor is needed between the BST pin and the SW pin to provide gate voltage for the high-side internal MOSFET. Renesas recommends using a 16V X7R 0.1µF ceramic capacitor as the bootstrap capacitor for most applications.

6.9 Thermal Considerations

The RAA211605 is packaged in the compact TSOT-23 package, which is capable of supporting high loads on a PCB designed with good heat sinking. To lower the thermal resistance of the package, apply large trace metal area and ground plane on the PCB. Ground vias underneath the IC and around the ground node of the input and output capacitors in addition to the output diode also help to dissipate heat. For example, the θ_{JA} of this device measured on a PCB with 1 inch^2 ground trace area using 2oz copper is around 65°C/W. To stay under the recommended maximum junction temperature of 125°C, Figure 21 shows the approximate maximum ambient temperature at different loads (V_{OUT} = 3.3V) allowed for the IC mounted on the aforementioned PCB.

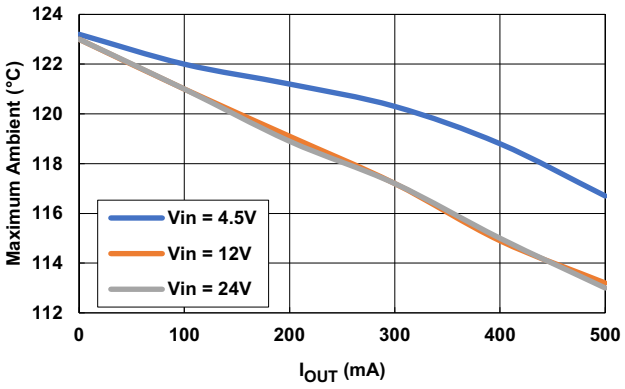


Figure 21. Maximum Ambient Temperature vs Output Current

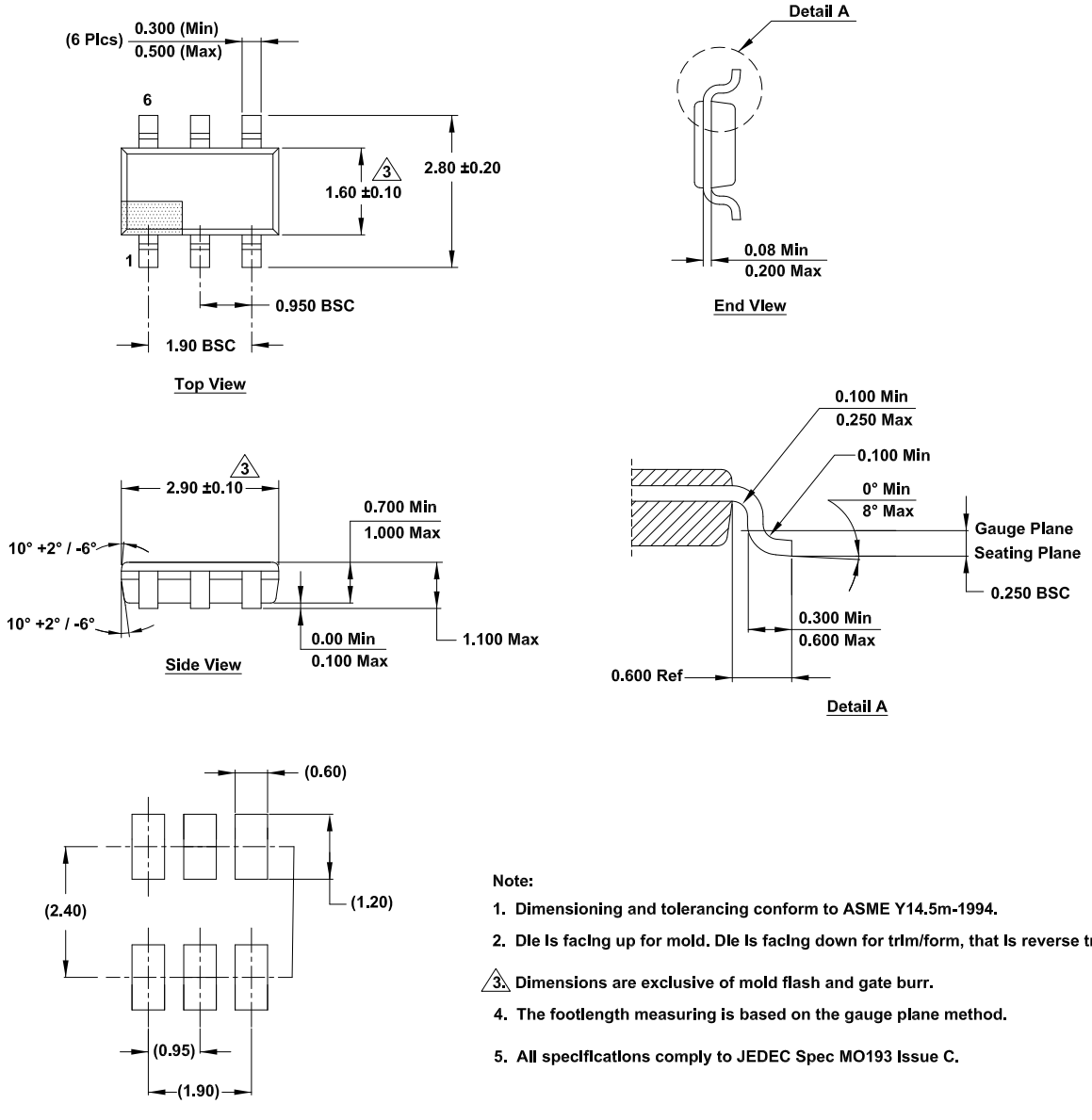
7. Layout Suggestions

- Place the input ceramic capacitor(s) as close as possible to the IC VIN pin and the diode. Keep the power loop (input ceramic capacitor, IC VIN pin, and diode) as small as possible to minimize phase node voltage ringing induced by trace parasitic inductance. This also results in better EMI performance.
- If an aluminum electrolytic capacitor is used, place it as close as possible to the IC VIN pin.
- Keep the phase node copper area small for less parasitic capacitance but large enough to handle the load current.
- Place the output capacitor(s) close to the inductor and freewheel diode.
- Connect the power ground (CIN, diode, and COUT ground) to the analog ground plane, which connects to the GND pin. Use a single point connection.
- Place feedback resistors close to the FB and GND pins, and away from phase node.
- Use a large etch metal area and ground plane on the PCB. Place ground vias underneath the IC and around the ground node of the input and output capacitors in addition to the output diode, facilitating better heat dissipation.

8. Package Outline Drawing

For the most recent package outline drawing, see P6.064C.

P6.064C
6 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 2, 12/20



Typical Recommended Land Pattern

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

9. Ordering Information

Part Number[1][2]	Part Marking[3]	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Junction Temp Range
RAA2116054GP3#JA0	605	TSOT23-6	P6.064C	Reel, 3k	-40 to 125°C
RTKA211605DR0000BU	RAA211605 Demonstration Board				
RTKA211605DR0010BU	RAA211605 DC/DC step-down regulator small form factor demonstration board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA211605 device page. For more information about MSL, see TB363.
3. Part marking is located on the bottom of the part.
4. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.06	Mar 24, 2023	Updated Max for Output Voltage, VOUT in Recommended Operating Conditions.
1.05	Oct 13, 2021	Corrected Typo in EC table changed unit for Line Regulation from mV/V to µV/V.
1.04	Oct 4, 2021	Updated Features bullet
1.03	Sep 21, 2021	Updated Ordering Information table.
1.02	Sep 10, 2021	Corrected typo in the paragraph under Equation 10 on page 12.
1.01	Jul 29, 2021	Updated Functional Description section. Added BST Refresh section.
1.00	Jul 14, 2021	Initial release.

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