RAA211651

60V 5A Low Quiescent Current Integrated Switching Regulator

The RAA211651 is an integrated 60V, 5A synchronous buck regulator with the Constant On-Time (COT) control scheme. It supports a wide range of input voltage from 4.5V to 60V and adjustable output voltage (0.8V to maximum duty cycle * V_{IN}). It also features a very low quiescent current, typically 19µA at 24V input. The modulation scheme used allows for high efficiency at all output load levels, especially at light-load conditions.

The RAA211651 is based on the COT modulator, where the on-time is determined by the input voltage level and the resistor connected to the SET pin. The switching frequency varies with the load. At light load, switching frequency drops reducing the switching losses. Also, with internal compensation, the regulator works in Diode Emulation mode reducing the losses at light-load conditions.

To limit inrush current during startup the RAA211651 has 2ms fixed internal soft-start time. It can also be programed by an external capacitor. The RAA211651 also provides programmable startup delay time for sequencing purposes.

The RAA211651 provides comprehensive protections including undervoltage lockout, overcurrent (positive and negative), overvoltage, and over-temperature protections.

The device is available in 28 Ld 4mmx5mm QFN package.

Features

- 4.5V to 60V input supply range
- 0.8V reference voltage with 1% accuracy
- Adjustable output voltage (0.8V to Dmax*V_{IN})
- Modulator: Constant On-Time (COT)
- Low quiescent current
- Excellent line and load regulation
- Selectable internal or external control loop compensation
- Variable load dependent switching frequency
- Output Power-Good (PG) indicator
- Programmable and optional fixed 2ms soft-start feature
- Programmable startup and shutdown delay
- Integrated LDO with bypass capability allowing for high-efficiency operation
- Full protection: High-Side Overcurrent (HSOC) and low-side current protections in both directions, output Overvoltage Protection (OVP) and Output Undervoltage Protection (OUVP), input Undervoltage Lockout (UVLO), and Over-Temperature Protection (OTP)
- Optional 3.3V default V_{OUT} using internal feedback
- 28 Ld 4mmx5mm QFN package

Applications

- Industrial power supplies
- 48V industrial and computing PoL
- Battery powered applications
- ATM, vending, and gaming machines
- Robotics
- Programmable logic controllers
- After-market automotive

Contents

1. Overview

1.1 Typical Applications

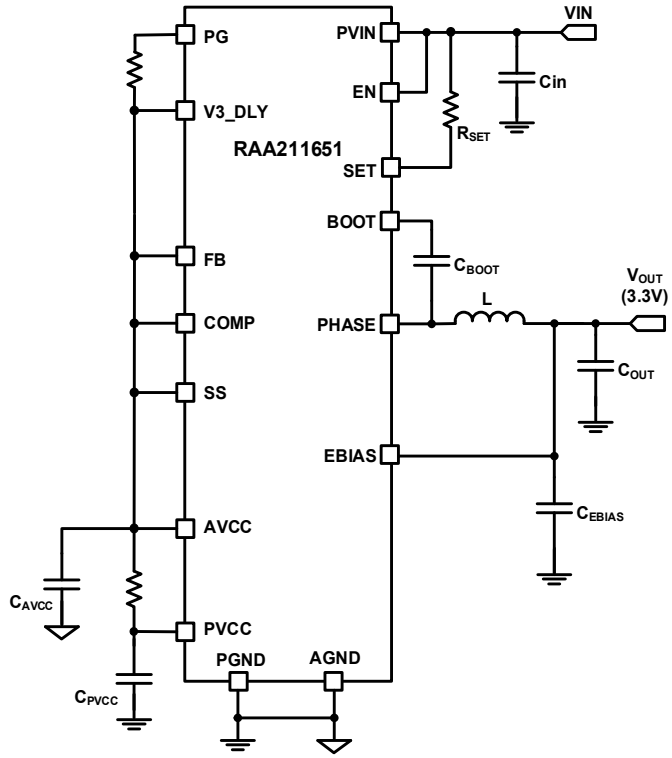


Figure 1. Typical Application Circuit Diagram for 3.3V V_{OUT} Using Internal Features

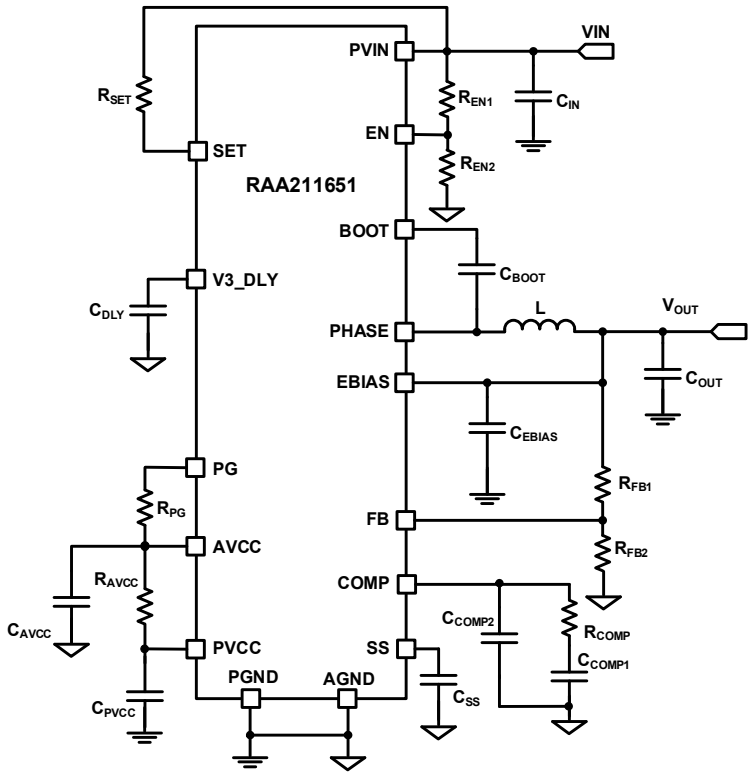


Figure 2. Typical Application Circuit Diagram with External Features, V_{OUT} <12V

1.2 Block Diagram

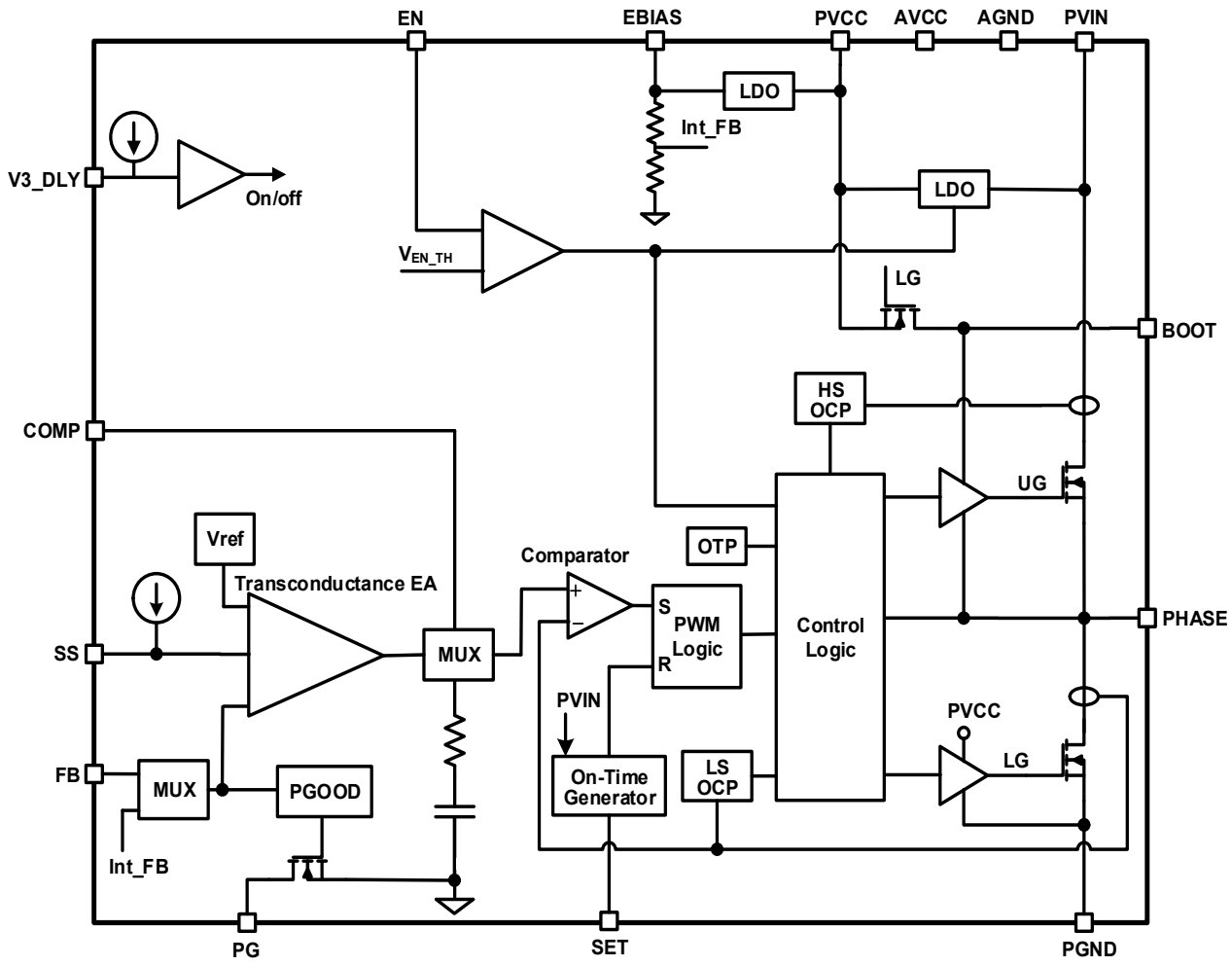
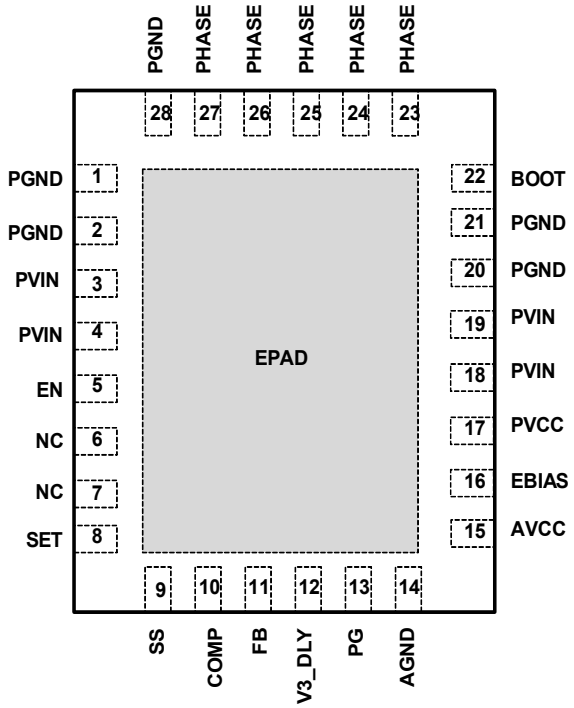


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

28 Ld QFN
Top View



2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 20, 21, 28	PGND	Power ground terminal
3, 4, 18, 19	PVIN	Voltage supply input. The main power input for the IC. Connect to a suitable voltage source within the IC operating range. Place a ceramic capacitor from PVIN to PGND close to the IC for decoupling.
5	EN	Accurate enable signal, accurate to ±5%
6, 7	NC	No connection pin. Renesas recommends connecting these pins to AGND.
8	SET	The resistor connected from SET to PVIN programs the on-time. Use the design spreadsheet to calculate the resistor value.
9	SS	Soft-start input. SS controls the soft-start. SS is tied to AVCC for the internal soft-start of 2ms. A capacitor connected from SS to ground sets the programmable soft-start time. The SS pin sources 5µA in soft-start. When the SS pin voltage reaches 0.8V, the soft-start ramp finishes and regulation starts based on the internal set reference of 0.8V.
10	COMP	Compensation node. COMP is the output of the transconductance error amplifier. Connect COMP to AVCC to select internal compensation. This also activates diode emulation. Connect an RC network from COMP to GND when using external compensation. This also forces continuous conduction mode.
11	FB	Feedback input pin for the regulator. The output voltage is set by an external resistor divider connected to FB. To use an internal feedback that regulates output voltage at 3.3V, tie the FB pin to AVCC and tie EBIAS pin to V_{OUT}.

Pin Number	Pin Name	Description
12	V3_DLY	Delay input pin. Connect a capacitor from V3_DLY to AGND to set a delay time that can be used for sequencing. The delay timer starts when EN is driven to logic high and ends with the beginning of soft-start. When EN is driven to logic low, the capacitor on V3_DLY adds delay time to the regulator shutdown. A 5µA current is sourced out of the V3_DLY pin, and when the pin voltage crosses 1.2V, the delay period is ended. Tie V3_DLY to AVCC if no delay is required.
13	PG	Power-good indicator pin. PG asserts high when soft start completes and the FB voltage exceeds 91% of VREF. When the buck regulator is in normal operation, PG is remains high. PG goes low if EN is driven low or the FB voltage exceeds the ±12% PG tolerance or any fault conditions exists. This is an open drain pin.
14	AGND	Analog/signal ground
15	AVCC	Analog bias supply. Internal LDOs generate the PVCC. Connect an RC filter from PVCC to AVCC. See Figure 67 for connection example. Renesas recommends using a resistor of 1Ω and capacitor of 1µF for the AVCC filter.
16	EBIAS	External bias pin. This pin can be connected to an external voltage source ranging from 3.15V to 12V. EBIAS is connected to the internal LDO that generates PVCC. If EBIAS is connected to a voltage source, the IC starts up with the PVCC LDO powered from PVIN and switches over to the EBIAS LDO. The EBIAS voltage source can be derived from the output voltage of the switching regulator if it is <12V. Using the EBIAS pin reduces power dissipation in the controller, particularly in applications with high PVIN voltage. **Note:** If EBIAS is not used, connect the EBIAS pin to the ground.
17	PVCC	PVCC is the output of the internal 3.3V LDO regulators. When the IC initially starts up, PVCC is supplied by the LDO tied to PVIN. If there is voltage available on EBIAS, it switches over to the EBIAS LDO to supply PVCC. PVCC is used as the gate drive supply voltage for the internal MOSFETs.
22	BOOT	Bootstrap supply pin. Connect a 0.1µF capacitor from BOOT to PHASE.
23, 24, 25, 26, 27	PHASE	Switch node pins. Connect these pins to the output inductor and the bootstrap capacitor.
-	EPAD	The EPAD is connected to PGND. It provides thermal relief for the package. Connect the EPAD to the board ground plane using as many vias as possible.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVIN, EN	-0.3	65	V
EN		PVIN + 6	V
EBIAS	-0.3	15	V
PHASE, SET	-0.3	PVIN + 0.3	V
PHASE, 20ns transient	-2	PVIN + 0.3	V
BOOT		Phase + 4	V
BOOT to PHASE and PVCC/AVCC to AGND	-0.3	4	V
All other pins	-0.3	AVCC + 0.3	V
Human Body Model (Tested per JS-001-2017)	-	2.5	kV
Charged Device Model (Tested per JS-002-2014)	-	2	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
28 Ld 4x5 QFN Package	35	1.2

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage, PVIN	4.5	60	V
External Bias Voltage	3.15	12	V
Output Voltage, V_{OUT}	0.8	Dmax*PVIN[1]	V
Output Current, I_{OUT}	0	5	A
Junction Temperature, T_J	-40	+125	°C

1. Limited by minimum off-time.

3.4 Electrical Specifications

T_J = -40°C to +125°C, PVIN = 4.5V to 60V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Supply voltage						
PVIN Voltage Range	PVIN		**4.5**		**60**	V
PVIN Typical Shutdown Current	ISDN	PVIN = 24V, EN = 0V		1	4	µA
PVIN Quiescent Current	Iq	PVIN = 24, VFB = 0.825V, EBIAS = 3.4V, not switching, (measured as I(PVIN) + I(EBIAS) scaled by 3.3/24)		16		µA
		PVIN = 24, EBIAS = V_{OUT}, FB = AVCC, switching		19		µA
PVCC+AVCC Supply Current		EN = 2V, FB = 0.9V, no load		100		µA
		EN = 2V, FB = 0.7V		6.5		mA
PVIN Undervoltage Lockout		PVIN rising	**3.95**	4.15	**4.45**	V
PVIN UVLO Hysteresis		PVIN falling		300		mV
AVCC Output Voltage using PVIN Linear Regulator		EBIAS = 0V	**3.1**	3.3	**3.5**	V
AVCC Output Voltage from EBIAS Linear Regulator		EBIAS = 5V	**3.1**	3.3	**3.5**	V
AVCC Undervoltage Lockout	VCCUV	VCC Rising	**2.75**	2.9	**3.05**	V
AVCC UVLO Hysteresis			**125**	200	**300**	mV
AVCC Current Limit from PVIN		PVIN = 6V	**80**	115	**150**	mA
AVCC Current Limit from EBIAS		EBIAS = 6V	**80**	115	**150**	mA
EBIAS			**3.15**	-	**12**	V
EBIAS Rising Threshold				3	**3.15**	V
EBIAS Hysteresis				170		mV
On-Time Generator						
On-Time		RSET = 82.5kΩ, PVIN = 24V, V_{OUT} = 3.3V, DCM mode		350		ns
		RSET = 82.5kΩ, PVIN = 24V, V_{OUT} = 3.3V, CCM mode		270		ns

T_J = -40°C to +125°C, PVIN = 4.5V to 60V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Frequency	f_{SW}	RSET = 82.5kΩ, PVIN = 24V, V_{OUT} = 3.3V, 5A load, CCM mode, L = 3.3µH, C_{OUT} = 80µF		565		kHz
Buck Converter						
V_{OUT} Voltage Range	V_{OUT}		**0.8**		**Dmax*PVIN**	V
Feedback Voltage Reference	V_{REF}			0.800		V
Feedback Voltage Reference Accuracy		PVIN = 24V, I_{OUT} = 2A, room temperature	-0.6		+0.6	%
		Over-temperature -40 to 125°	**-1**		**1**	%
Feedback Voltage Line Regulation		PVIN = 5V to 60V[2]		0.1		%/V
Typical Error Amplifier Transconductance		External compensation mode		2		mS
Typical Current Sense Gain				0.06		V/A
Output Current			**5**			A
Minimum On-Time				45		ns
Minimum Off-Time			**235**	265	**295**	ns
Peak Efficiency		(PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, EBIAS = V_{OUT}		89.5		%
Efficiency (5A)				87		%
Efficiency (100mA)				85.7		%
Power MOSFETs						
Upper FET $r_{DS(ON)}$				90		mΩ
Lower FET $r_{DS(ON)}$				37		mΩ
Enable Input						
Accurate EN/UVLO Threshold		EN/UV rising	**1.425**	1.5	**1.575**	V
EN Hysteresis				140		mV
Coarse EN/UVLO Rising Threshold			**0.85**	1	**1.2**	V
Coarse EN/UVLO Hysteresis			**40**	110	**250**	mV
Power-Good Open-Drain Output						
PGOOD Logic Low		Sink 2mA			**0.3**	V
PGOOD Deglitch Filter[2]				5		µs
PG		Lower PG threshold, VFB falling	**85**	88	**91**	%
		Lower PG threshold hysteresis		3		%
		Upper PG threshold, VFB rising	**109**	112	**115**	%
		Upper PG hysteresis		3		%
Internal Soft-Start Function						
Soft-Start Time	t_{SS}	SS = AVCC (internal SS mode)	**1.73**	2	**2.33**	ms
Internal SS Completion Time		Internal SS mode (SS begin to PG assert)	**2.6**	3	**3.5**	ms

T_J = -40°C to +125°C, PVIN = 4.5V to 60V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
External Soft-Start Function						
SS Charge Current		External SS mode	**4**	5	**6**	µA
SS Pull-Down Resistance		External SS mode		560		Ω
External SS Completion Threshold[3]		External SS mode		1.2		V
DELAY Function						
DELAY Charging Current		V3_DLY = 0V	**4**	5	**6**	µA
DELAY Threshold				1.2		V
DELAY Pull-Down Resistance				700		Ω
Fault Protection						
Valley Current Limit			**6**	7.2	**9**	A
High-Side MOSFET OCP[2]			**10**	12		A
Negative Current Limit			**-4.3**	-3.5	**-2.9**	A
OVP[2]		VFB rising	**116**	120	**128**	%
OVP Deglitch[2]				2		µs
UVP (Undervoltage Protection, Short-Circuit Protection)	FBUVP	VFB falling after soft-start completed	**65**	70	**74**	%
Hiccup Timer	T_hiccup			200		ms
Thermal Shutdown[2]	T_{SD}			153		°C
Thermal Hysteresis[2]	T_{HYS}			30		°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
3. V_{OUT} is settled when the SS pin crosses 0.8V. PG asserts when SS crosses 1.2V.

4. Typical Performance Graphs

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated.

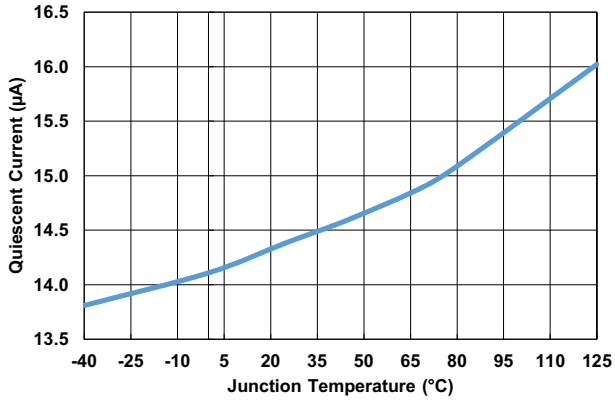


Figure 4. PVIN Quiescent Current vs Junction Temperature

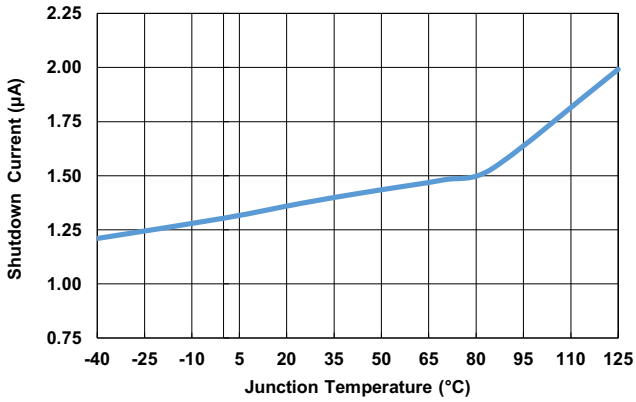


Figure 5. PVIN Shutdown Current vs Junction Temperature

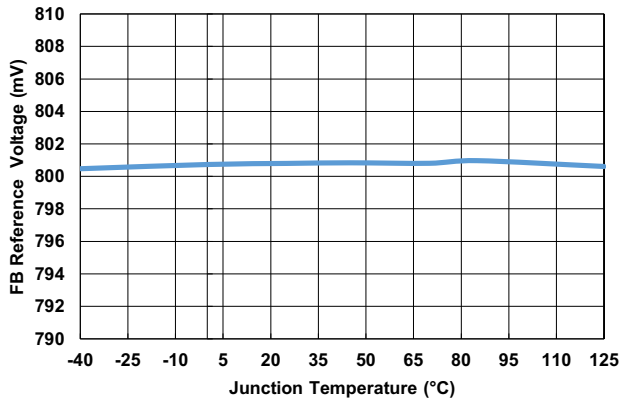


Figure 6. Feedback Voltage vs Junction Temperature

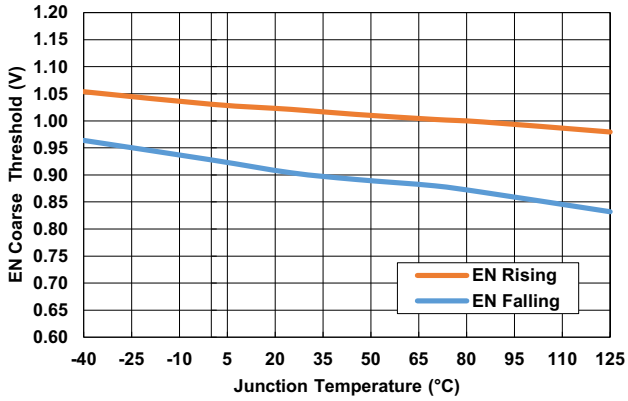


Figure 7. Enable Coarse Threshold vs Junction Temperature

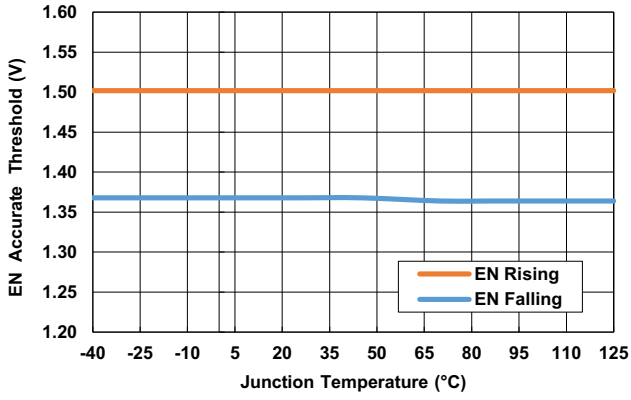


Figure 8. Enable Accurate Threshold vs Junction Temperature

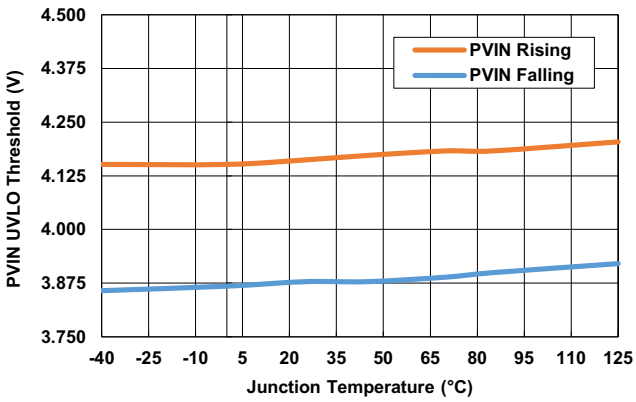


Figure 9. PVIN UVLO Threshold vs Junction Temperature

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

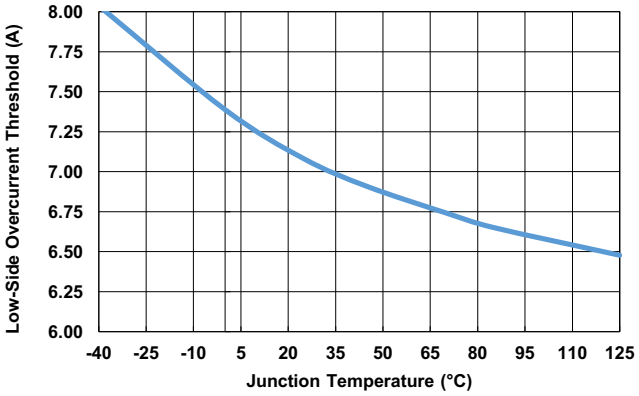


Figure 10. Low-Side Overcurrent (LSOC) Threshold vs Junction Temperature

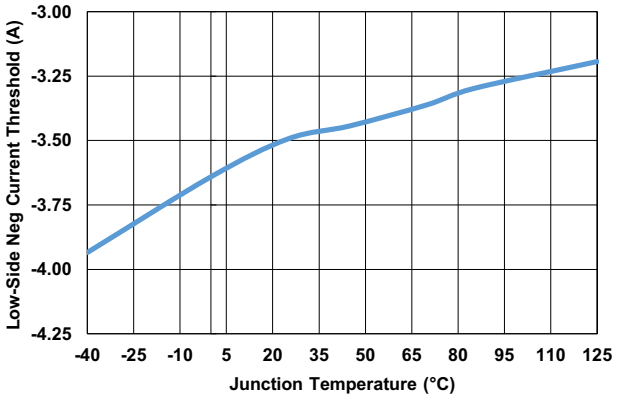


Figure 11. Low-Side Negative Current (NOC) Threshold vs Junction Temperature

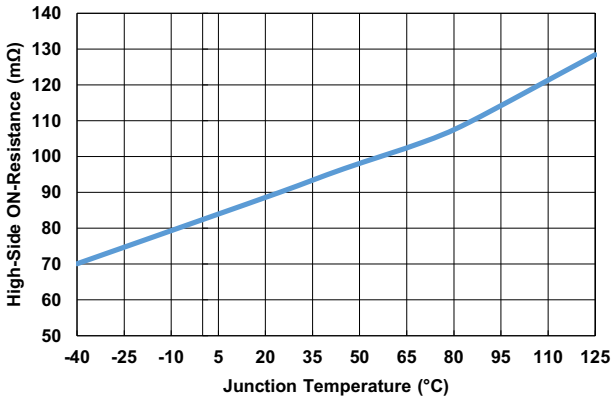


Figure 12. High-Side $r_{DS(ON)}$ vs Junction Temperature

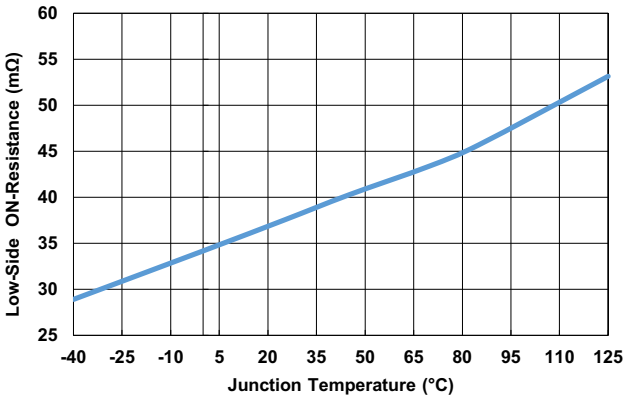


Figure 13. Low-Side $r_{DS(ON)}$ vs Junction Temperature

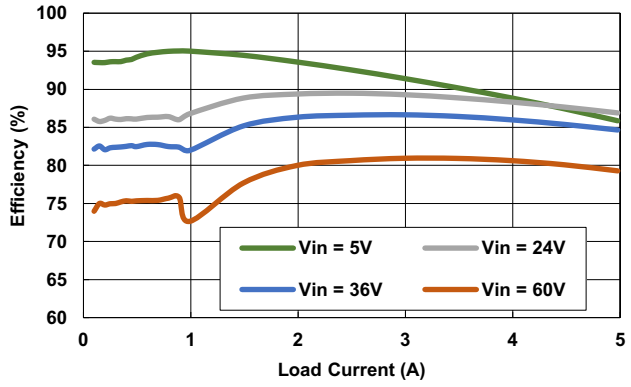


Figure 14. Efficiency vs Load Current (V_{OUT} = 3.3V)

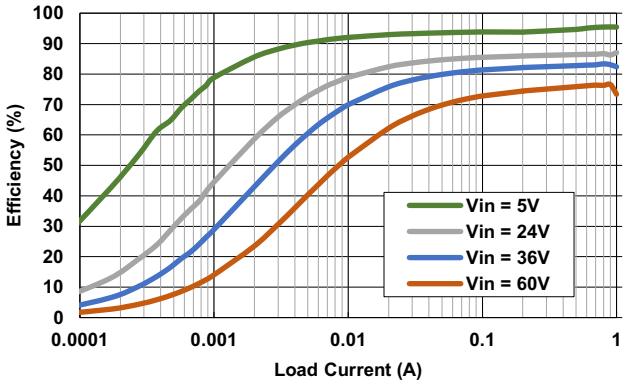


Figure 15. Efficiency vs Load Current (V_{OUT} = 3.3V)

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

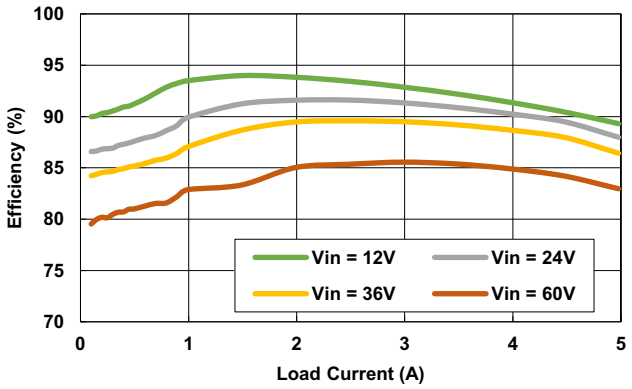


Figure 16. Efficiency vs Load Current (V_{OUT} = 5V), L = 4.7µH, COUT = 70µF, RSET = 125kΩ

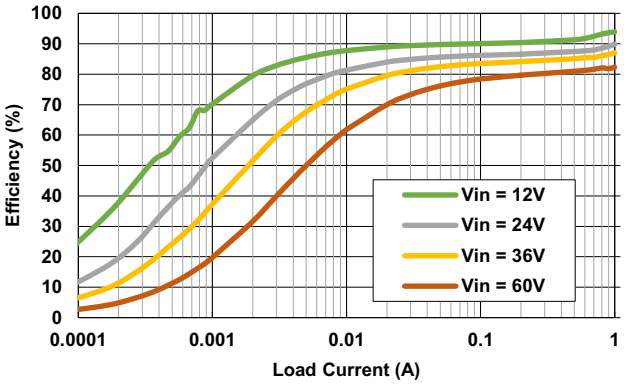


Figure 17. Efficiency vs Load Current (V_{OUT} = 5V), L = 4.7µH, COUT = 70µF, RSET = 125kΩ

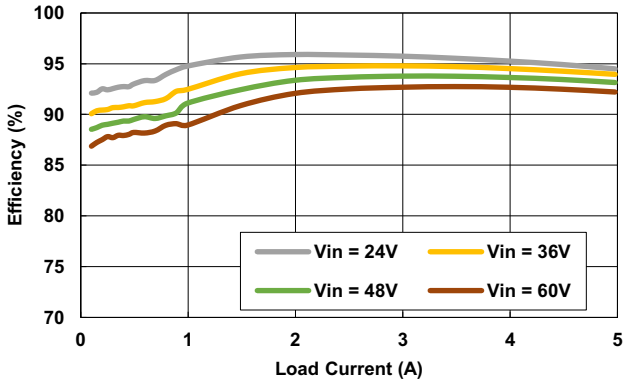


Figure 18. Efficiency vs Load Current (V_{OUT} = 12V), L = 10µH, COUT = 50µF, RSET = 300kΩ

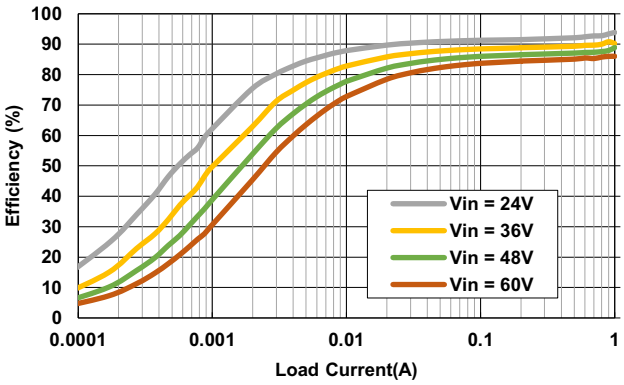


Figure 19. Efficiency vs Load Current (V_{OUT} = 12V), L = 10µH, COUT = 50µF, RSET = 300kΩ

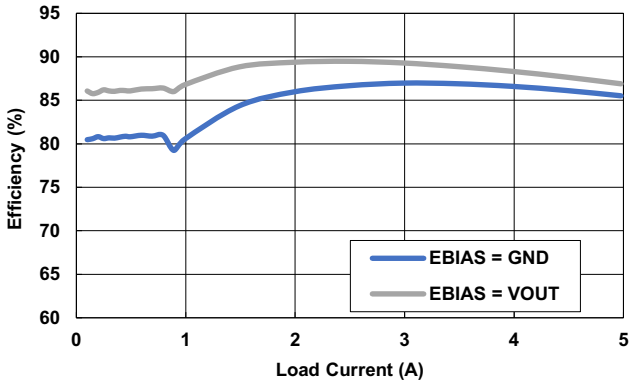


Figure 20. Efficiency (V_{OUT} = 3.3V) with EBIAS = V_{OUT} and EBIAS = GND

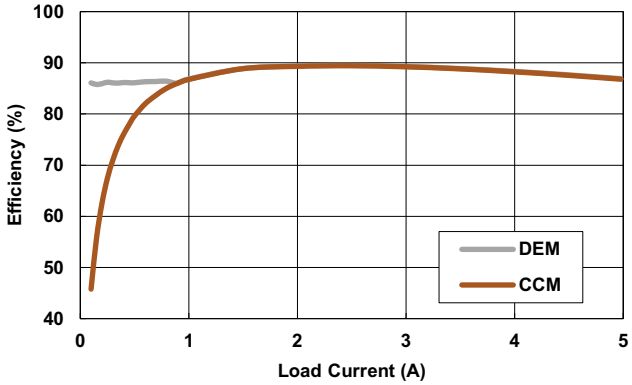


Figure 21. Efficiency (V_{OUT} = 3.3V) with DEM and CCM, PVIN = 24V

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

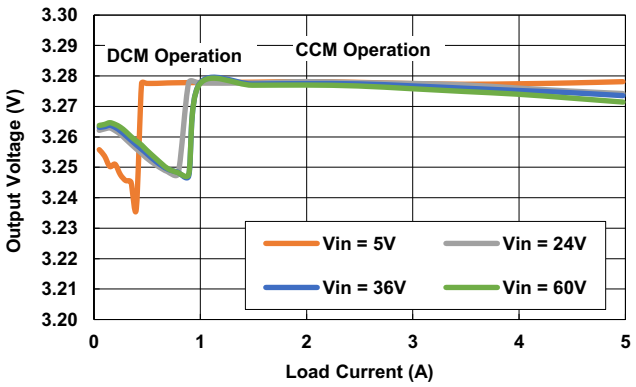


Figure 22. Load Regulation

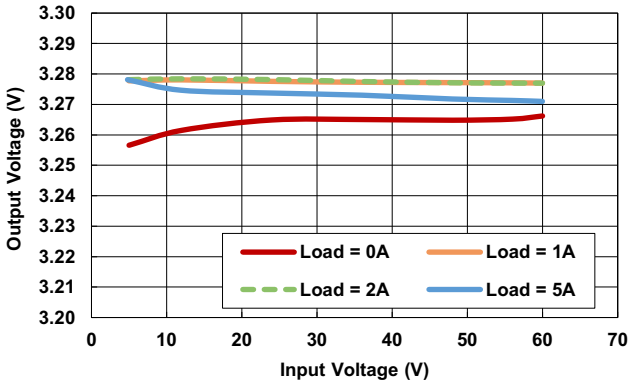


Figure 23. Line Regulation

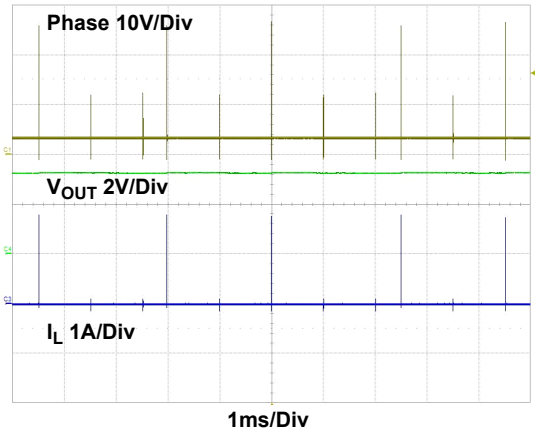


Figure 24. Steady-State Operation at I_{OUT} = 0A, 1ms/Div

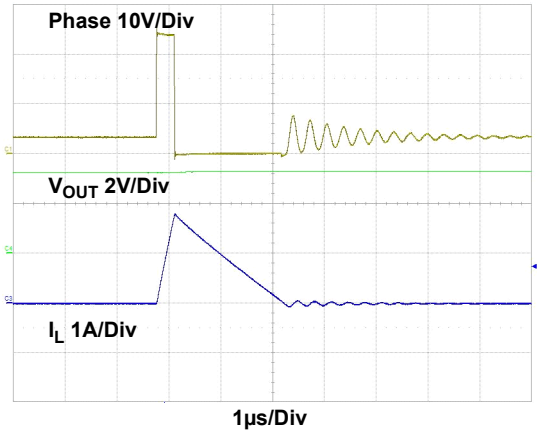


Figure 25. Steady-State Operation at I_{OUT} = 0A, 1µs/Div

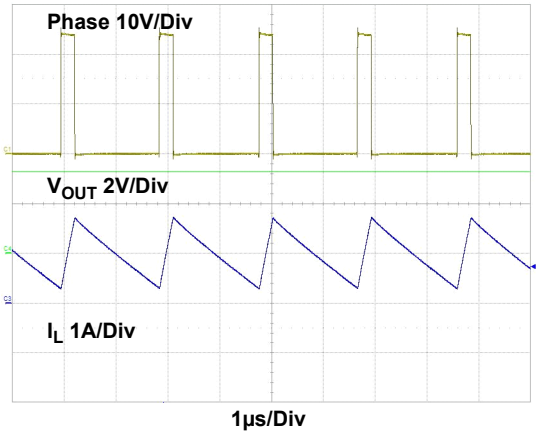


Figure 26. Steady-State Operation at I_{OUT} = 1A

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

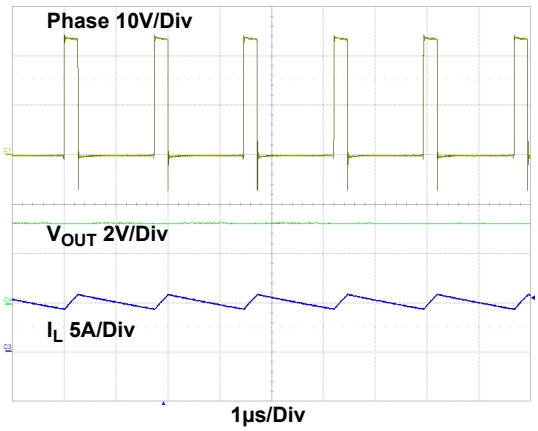


Figure 27. Steady-State Operation at I_{OUT} = 5A

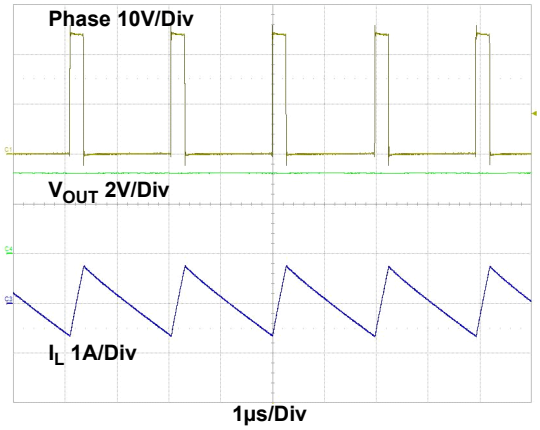


Figure 28. Steady-State Operation at I_{OUT} = 0A, CCM Operation

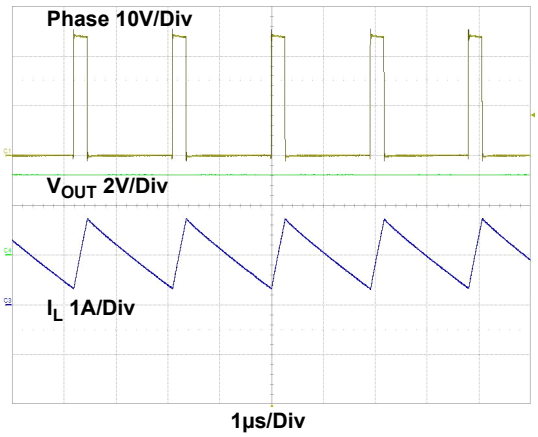


Figure 29. Steady-State Operation at I_{OUT} = 1A, CCM Operation

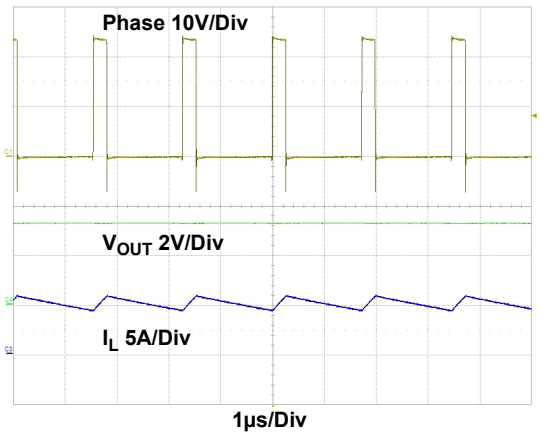


Figure 30. Steady-State Operation at I_{OUT} = 5A, CCM Operation

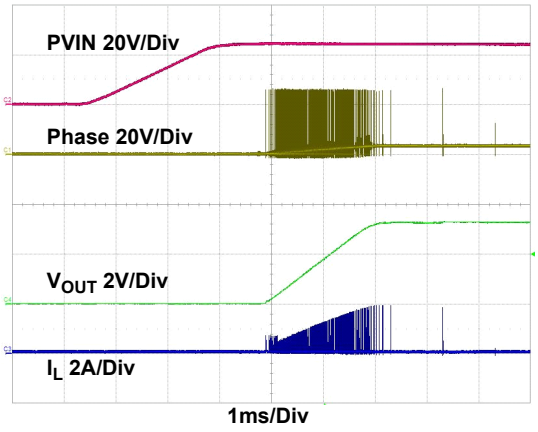


Figure 31. Start-Up through PVIN, I_{OUT} = 0A

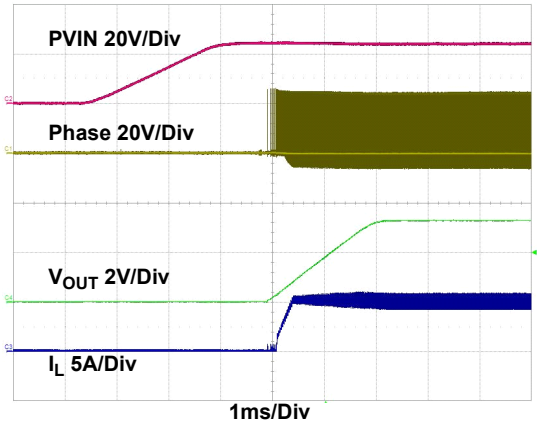


Figure 32. Start-Up through PVIN, I_{OUT} = 5A

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

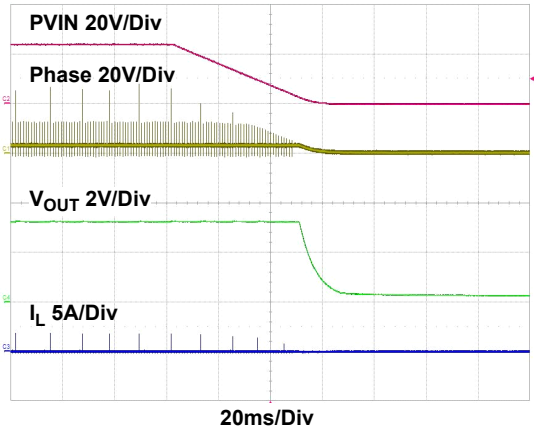


Figure 33. Shutdown through PVIN, I_{OUT} = 0A

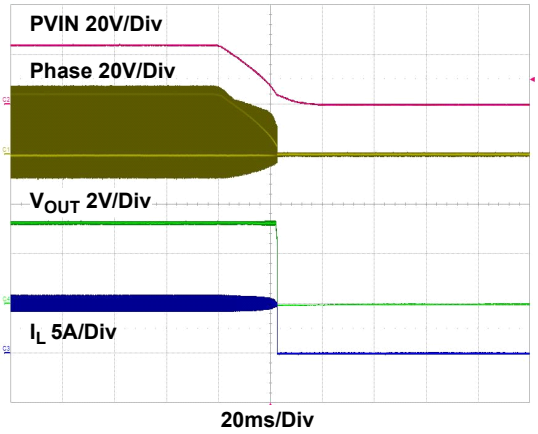


Figure 34. Shutdown through PVIN, I_{OUT} = 5A

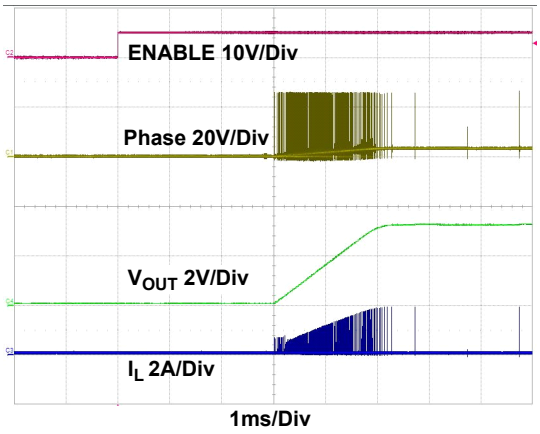


Figure 35. Start-Up through EN, I_{OUT} = 0A

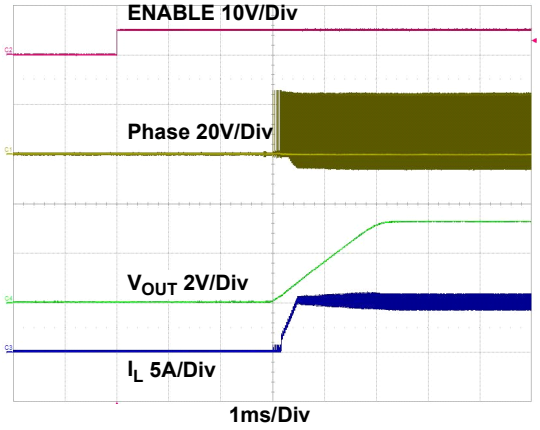


Figure 36. Start-Up through EN, I_{OUT} = 5A

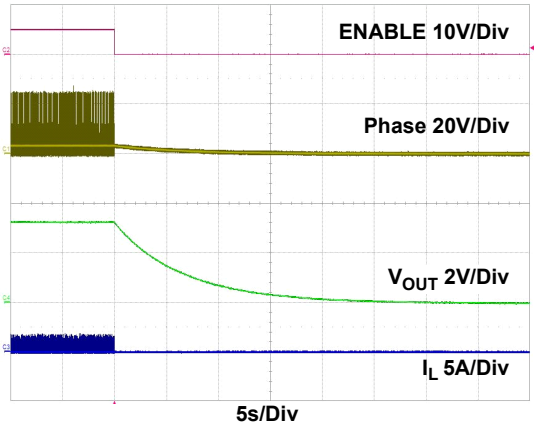


Figure 37. Shutdown through EN, I_{OUT} = 0A

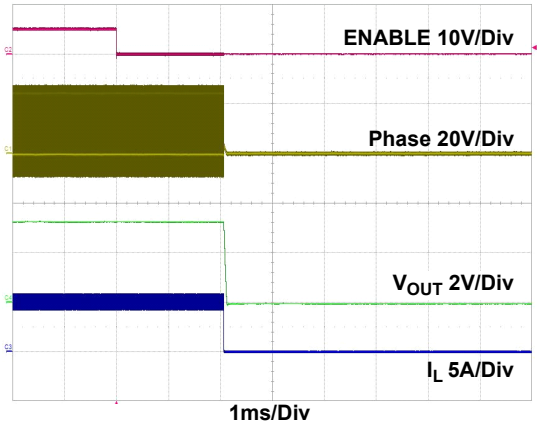


Figure 38. Shutdown through EN, I_{OUT} = 5A

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

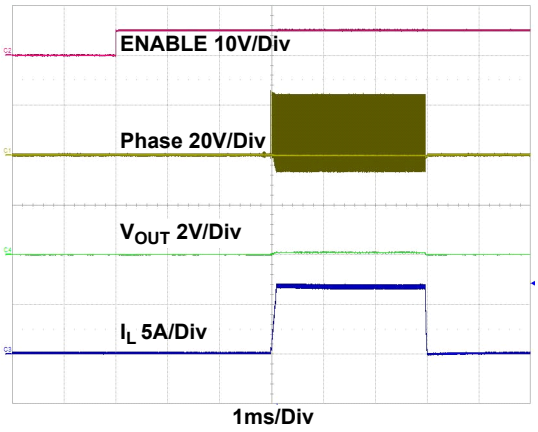


Figure 39. Start-Up with V_{OUT} Short-Circuit

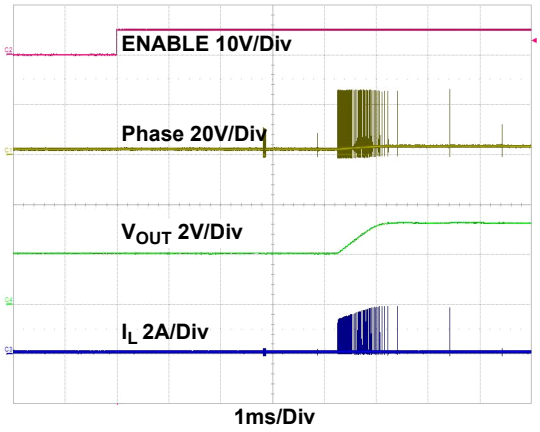


Figure 40. Start-Up with V_{OUT} Pre-Biased to 2V

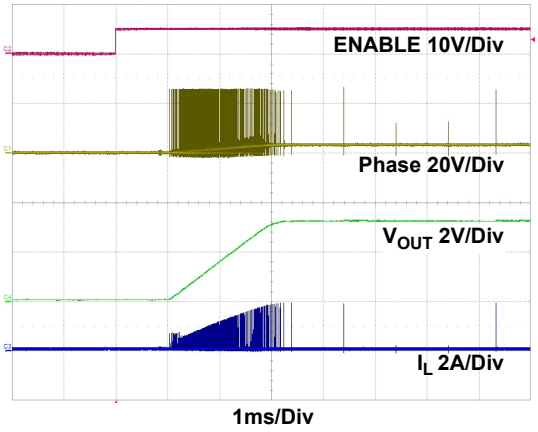


Figure 41. Start-Up without Delay (V3DLY = AVCC)

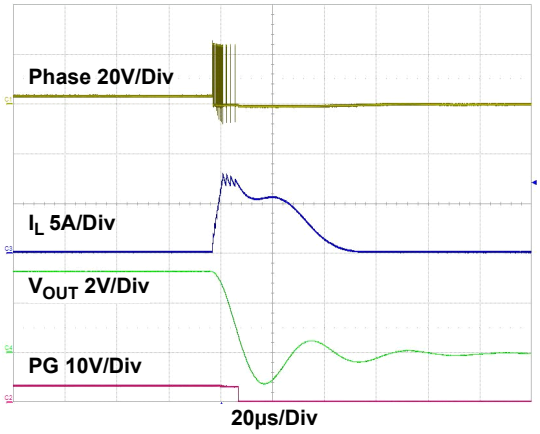


Figure 42. I_{OUT} 0A to Short-Circuit

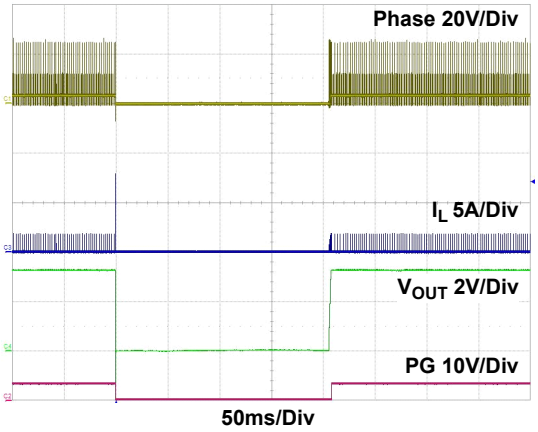


Figure 43. I_{OUT} 0A to Short-Circuit to 0A Recovery

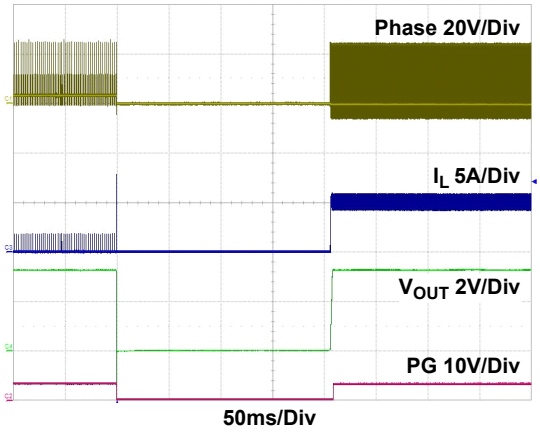


Figure 44. I_{OUT} 0A to Short-Circuit to 5A Recovery

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

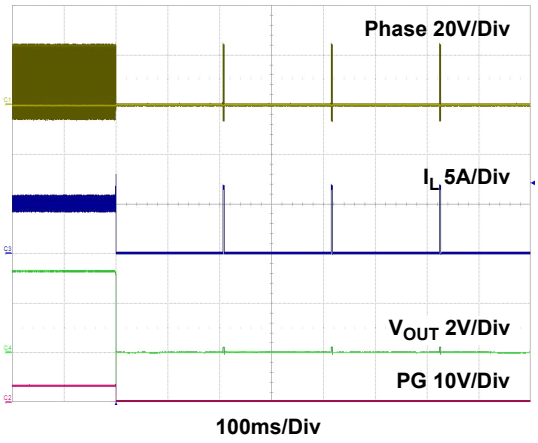


Figure 45. Hiccup after Output Short-Circuit

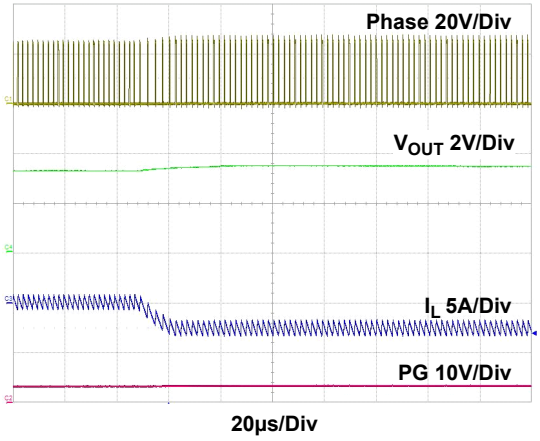


Figure 46. Negative Overcurrent (NOC) Protection, CCM Operation

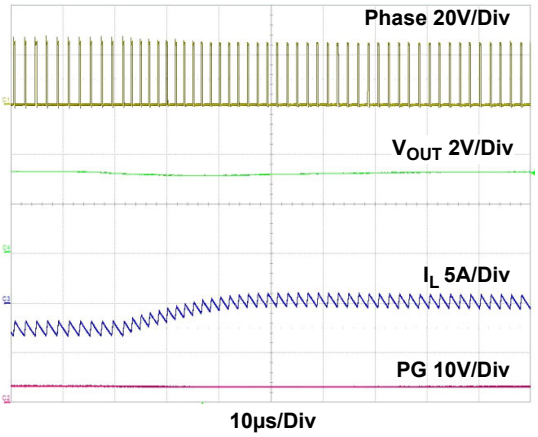


Figure 47. Recovery from Negative Overcurrent (NOC) Protection, CCM operation

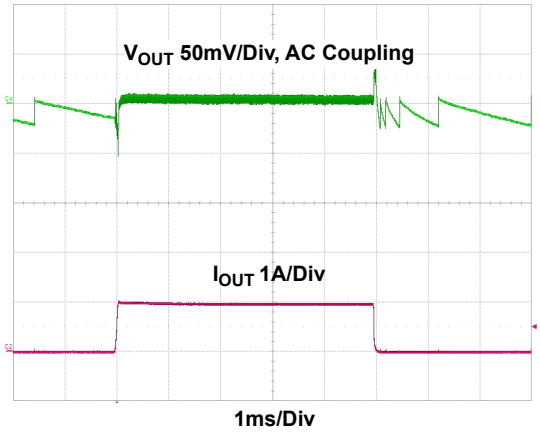


Figure 48. Load Transient I_{OUT} = 0A to->1A->0, Slew Rate 0.5A/µs

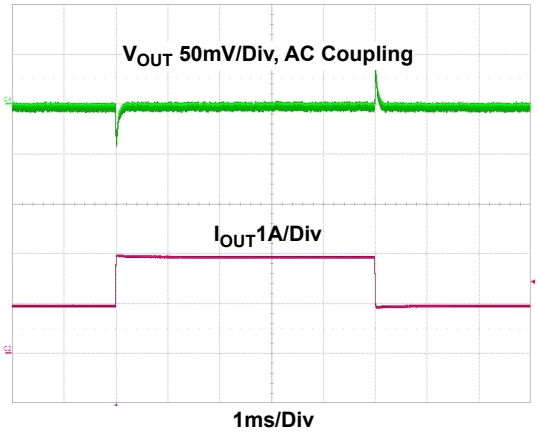


Figure 49. Load Transient I_{OUT} = 1A -> 2A-> 1A, Slew Rate 0.5A/µs

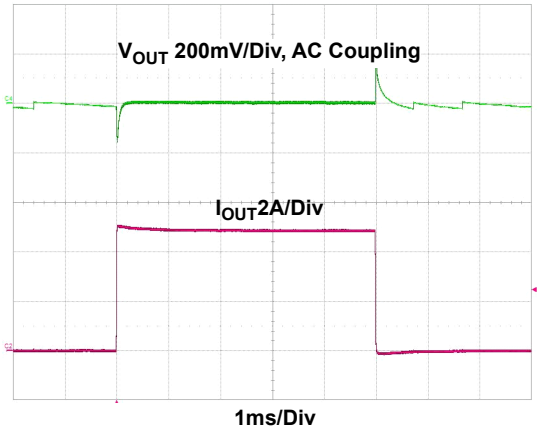


Figure 50. Load Transient I_{OUT} = 0A -> 5A-> 0A, Slew Rate 0.5A/µs

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

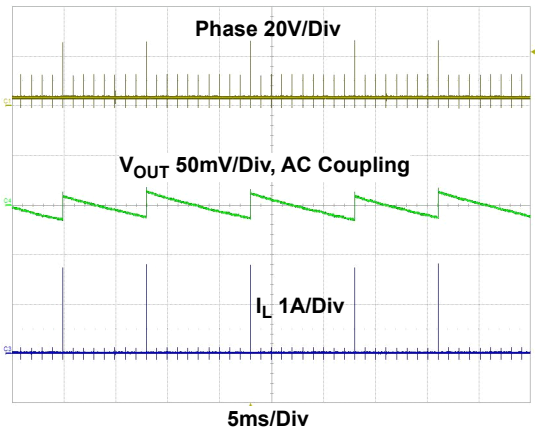


Figure 51. Output Voltage Ripple at I_{OUT} = 0A

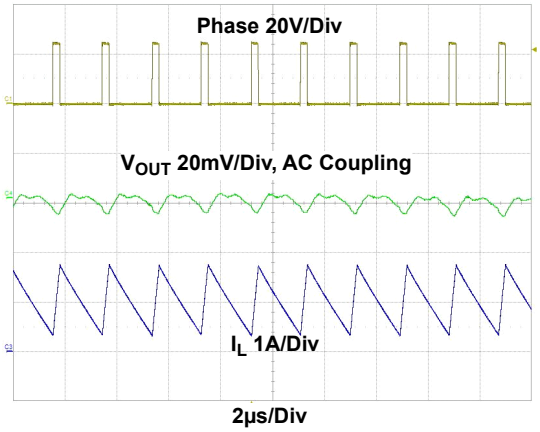


Figure 52. Output Voltage Ripple at I_{OUT} = 1A

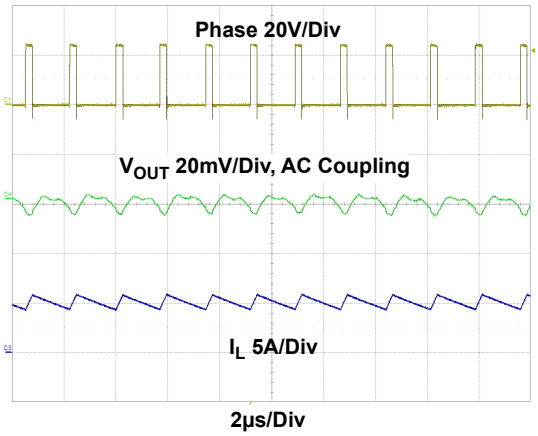


Figure 53. Output Voltage Ripple at I_{OUT} = 5A

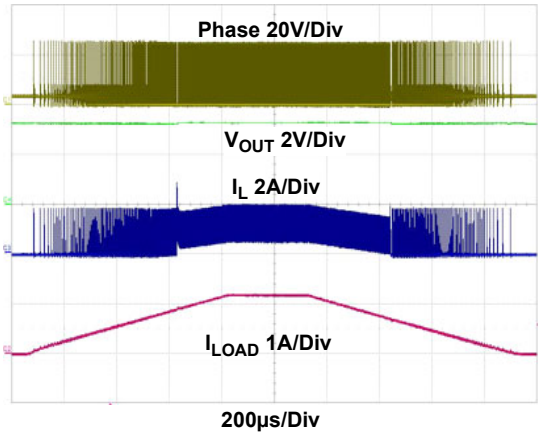


Figure 54. DCM-CCM-DCM Mode Transitions

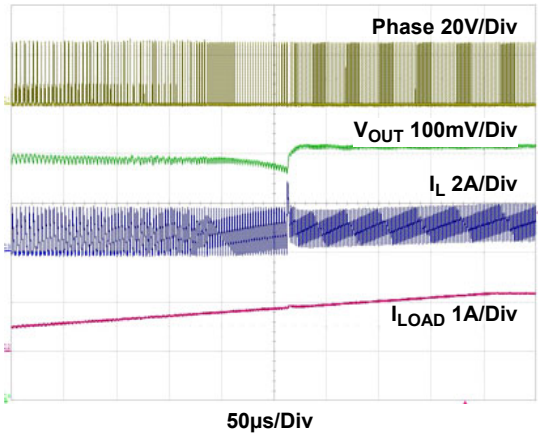


Figure 55. DCM-CCM Mode Transition

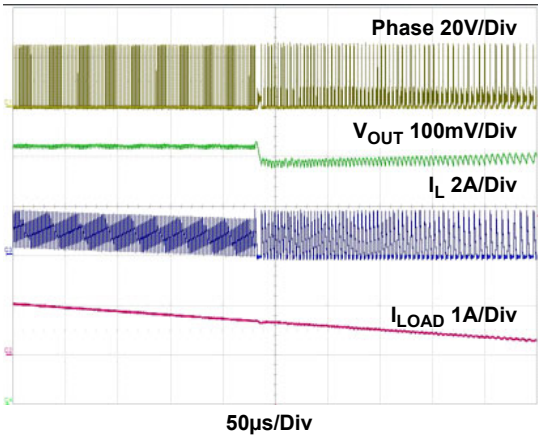


Figure 56. CCM-DCM Mode Transition

PVIN = 24V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} = 80µF, R_{SET} = 82.5kΩ, T_A = +25°C, internal compensation, internal soft-start unless otherwise stated. (Cont.)

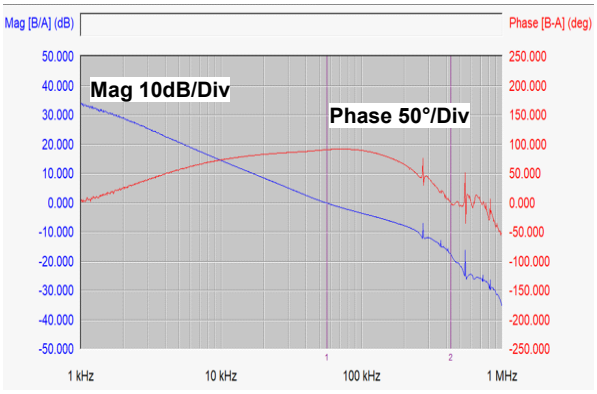


Figure 57. Loop Gain at I_{OUT} = 3A

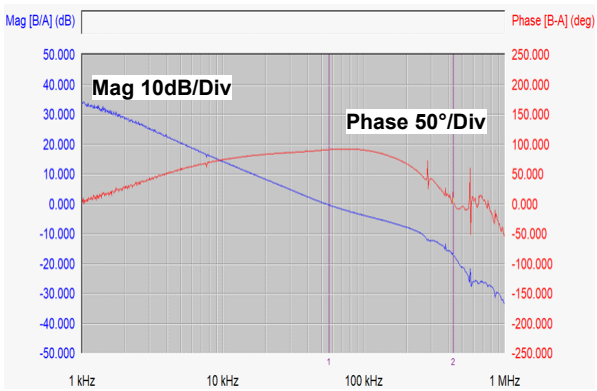


Figure 58. Loop Gain at I_{OUT} = 5A

5. Functional Description

The RAA211651 is a high-efficiency integrated synchronous buck regulator. It can operate across a wide input voltage range from 4.5V to 60V delivering load current up to 5A across the -40°C to 125°C temperature range. It has a built-in internal feedback option preset for 3.3V output. The regulator works with constant on-time, load-dependent switching frequency.

Figure 59 shows the functional block diagram for RAA211651. The resistor connected between the PVIN and SET pins determines the on-time. When the PHASE pin makes the transition to high, the PVIN to SET resistor begins to charge an internal 100pF capacitor (110pF in Discontinuous Conduction Mode (DCM)). When the SET pin voltage crosses 0.8V, the on-time expires and the PHASE pin transitions to low. When the PHASE pin is low, the SET pin is pulled low internally with an open-drain MOSFET discharging the internal capacitor.

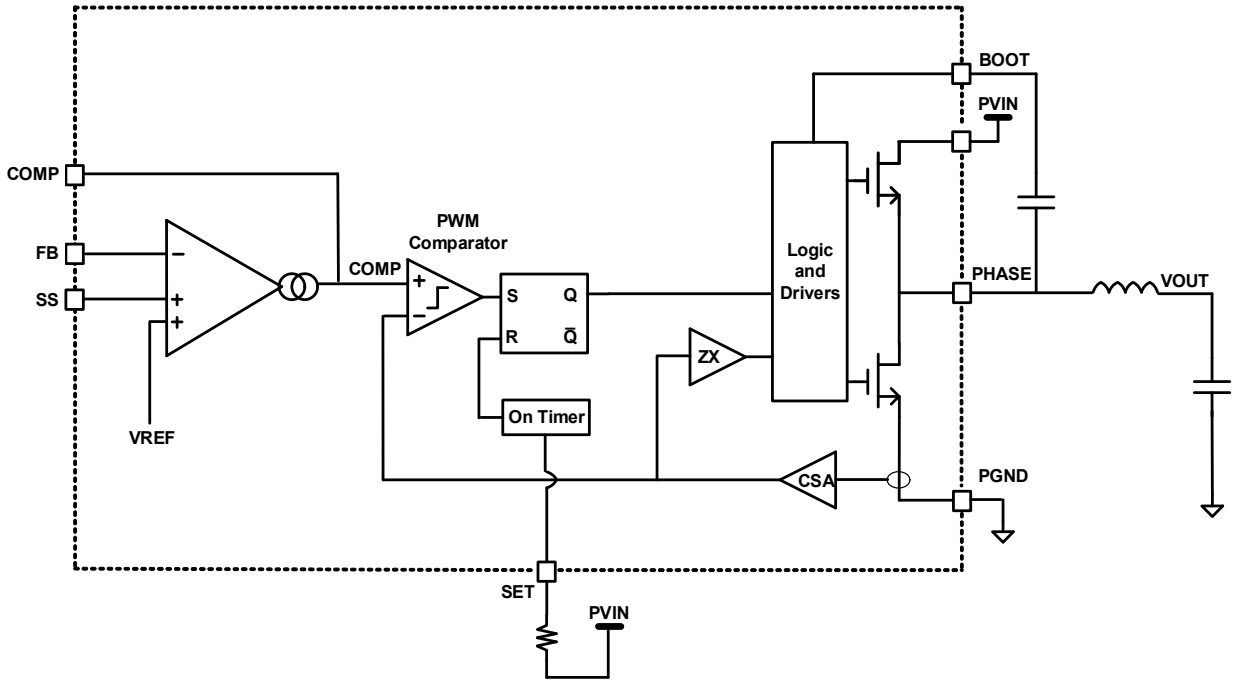


Figure 59. COT Functional Block Diagram

In Diode Emulation Mode (DEM), only internal compensation can be used. If an external RC network is placed on the COMP pin, the regulator does not enable DCM and it can only operate in the CCM mode with a constant on-time.

The output voltage is sensed by a resistor divider from V_{OUT} to the FB pin. An internal transconductance Error Amplifier (EA) compares FB voltage with the internal 0.8V reference voltage and produces an amplified compensated signal COMP to minimize the error in V_{OUT}. The EA has internal compensation, which provides stable operation across the device operating range. EA uses internal compensation when COMP is connected to AVCC. An external RC network can be connected between COMP and AGND to use external compensation. The COMP signal is compared with the sensed low-side current. When the low-side current signal hits the COMP level, the high-side MOSFET is turned on for the time determined by the constant on-time generator. The high-side MOSFET is turned off when the on-time expires. When the high-side MOSFET is turned off, the inductor current starts to ramp down initially freewheeling through the low-side MOSFET body diode. After a small dead time, the low-side MOSFET is turned on and the inductor current shifts from the body diode to its channel. During each switching cycle when the high-side MOSFET is turned on, the inductor stores the energy and it is delivered to the load when it is turned off.

With the internal compensation, a Zero Cross Detector (ZCD) is used to put the regulator in DEM, where a DCM operation is enabled when the inductor current hits zero. This operation keeps both the top and bottom MOSFETs off until the on-time generator resets the flip-flop to start the next switching cycle. As a result, the regulator operates in the DEM mode at light-load conditions to achieve better efficiency.

Figure 60 shows the flow chart for two possible modes based on how the COMP pin is configured either for internal or external compensation.

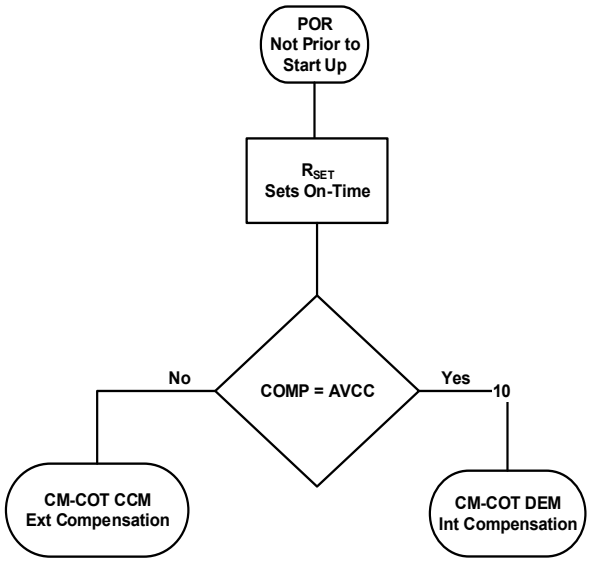


Figure 60. Different Modes of Operation

5.1 Supported Output Voltage Range

RAA211651 is capable of a low minimum off time, typical 265ns. This allows for high duty cycle operation to regulate high V_{OUT}. Considering the variation on the minimum off time, Figure 61, shows the maximum possible V_{OUT} for three different switching frequencies. At 2.5MHz, with PVIN of 60V, it is possible to get V_{OUT} up to 15.75V while with lower switching frequency higher VOUT is possible. Equation 1 can be used to find the possible maximum V_{OUT} for a selected PVIN and switching frequency.

(EQ. 1) $$V_{OUT\_max} = (1 - t_{min\_off\_time} \times f_{SW}) \times PVIN$$

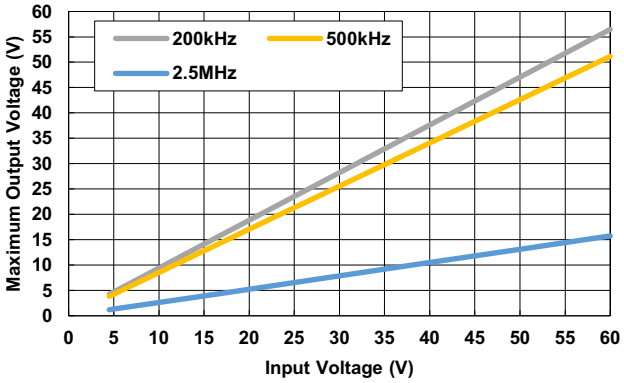


Figure 61. Maximum Output Voltage Supported vs Input Voltage for Various f_{SW} Values

RAA211651 has a small minimum on time, typical 45ns. Also, the output voltage cannot be smaller than the feedback reference voltage of 0.8V. Therefore, for a switching frequency and input voltage, the minimum possible output voltage is calculated using Equation 2.

(EQ. 2) $$V_{OUT\_min} = \max(0.8, t_{min\_on\_time} \times f_{SW} \times PVIN)$$

Figure 62 shows possible minimum output voltage plots for three switching frequencies for the PVIN range.

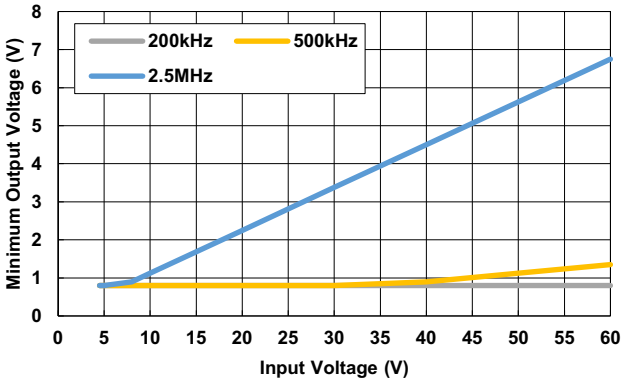


Figure 62. Minimum Output Voltage Supported vs Input Voltage for Various f_{SW} Values

To regulate the selected V_{OUT} and proper operation of the regulator, the output inductor, capacitor, and SET resistor must be appropriately selected. Renesas recommends using the design spreadsheet to calculate the component values.

5.2 Soft-Start

The RAA211651 has a Soft-Start (SS) function that provides a ramp reference to the input of the error amplifier. Soft-start prevents high inrush current or output voltage overshoot at startup.

The soft-start ramp can be generated either internally or by an external capacitor on the SS pin. When this pin is tied to AVCC, the SS time is internally set to 2ms. Programmable soft-start timing is implemented by connecting a capacitor from the SS pin to AGND. SS sources 5µA during soft-start. The SS capacitor is calculated using Equation 3:

(EQ. 3) $$C_{SS}[nF] = 6.25T_{SS}[ms]$$

where T_{ss} is the soft-start time in milliseconds.

When the SS ramp is lower than the 0.8V internal bandgap-referenced voltage, the error amplifier uses the SS voltage as the reference. When it reaches 0.8V, the bandgap-referenced voltage takes over. PGOOD is asserted when SS reaches 1.2V.

5.3 Delay

The delay function adds a delay time before the onset of soft-start and shutdown so the output rail does not ramp up or down before the delay time expires. The time can be set by a capacitor connected between the V3_DLY pin and ground. The capacitor is charged by a 5µA current source at the V3_DLY pin and the delay time is set using Equation 4:

(EQ. 4) $C_{DELAY}[nF] = 4.17T_{DELAY}[ms]$

The delay time starts when the EN logic goes high or low. It is complete when the voltage on the capacitor reaches 1.2V, at which time ramping of soft-start or shutdown happens. The timing diagram in Figure 63 illustrates the sequence of signals in an EN triggered power-up or power-down event.

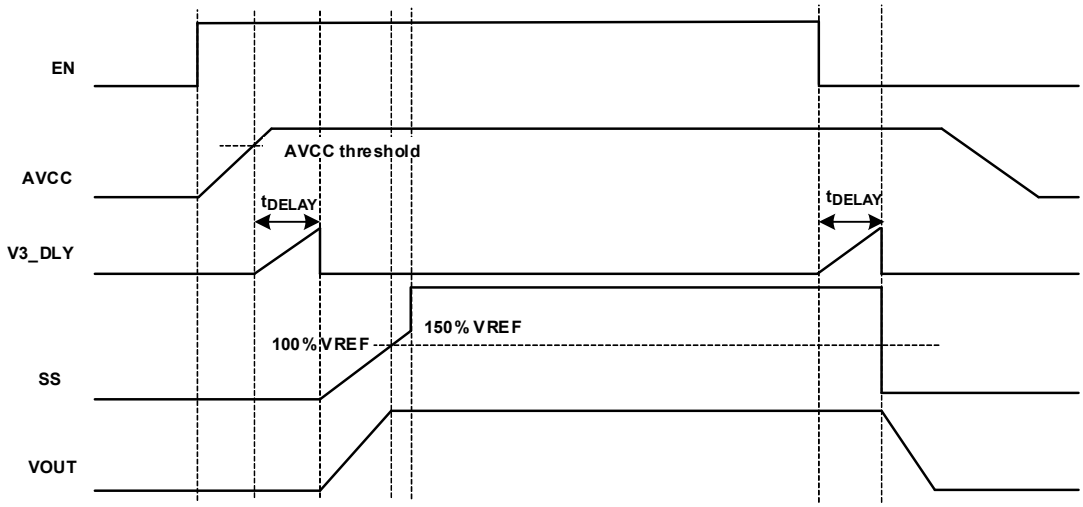


Figure 63. Delay Function

The delay function ensures proper power sequencing of two or more supplies. For example, if V_{OUT1} needs to come up before V_{OUT2} and come down after V_{OUT2}, and the PG signal of the first buck regulator is used as the EN signal for the second one, the delay time set in the first regulator produces the correct power-up/down sequence of the two outputs as shown in Figure 64 (ignoring delay for the second regulator).

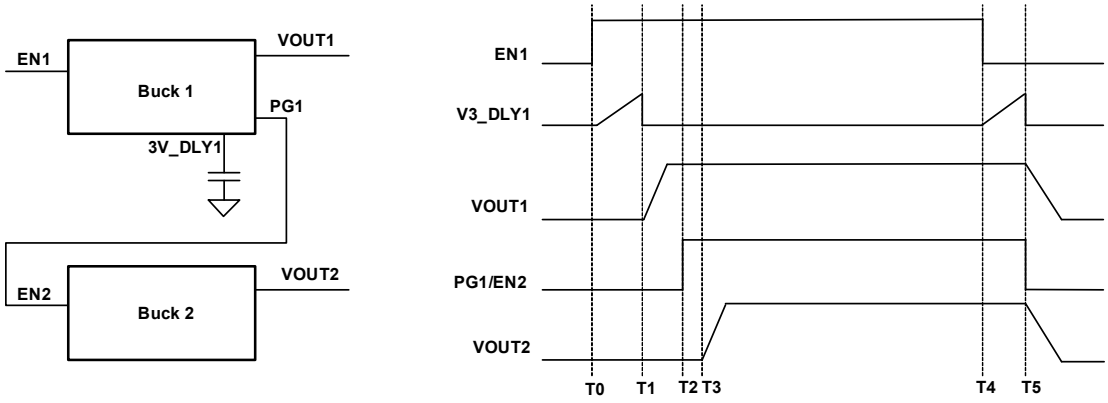


Figure 64. Sequencing Power Supplies with Delay Function

5.4 Power-Good

The RAA211651 provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. The PG pin is the open drain of a MOSFET. For logic level output voltages, connect it to a voltage source through a pull-up resistor. At power-on, the PG signal is held low before SS is ready, and it is asserted when the SS voltage reaches 1.2V and the FB voltage is within the regulation window. When the FB voltage goes 12% below or 12% above the nominal value, PG is pulled low, as shown in Figure 65. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start.

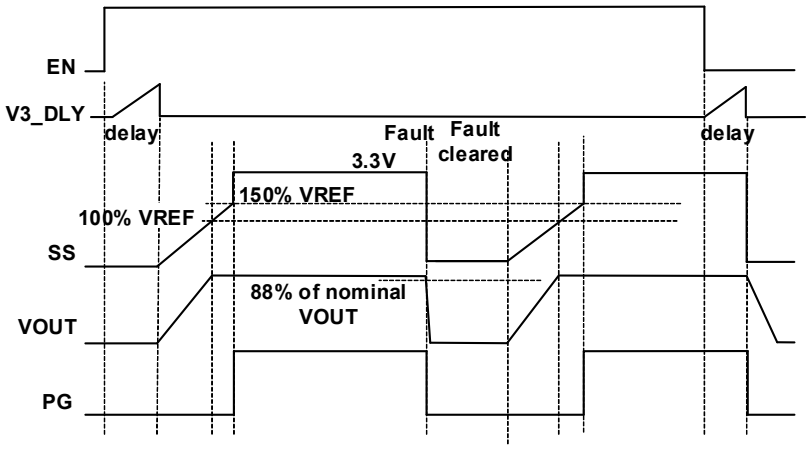


Figure 65. Power-Good Signal

5.5 Bias Supply PVCC, AVCC

The regulator has two internal LDOs to generate the 3.3V analog bias power supply. One LDO is connected to PVIN and the other LDO is connected to EBIAS. The regulator starts up with the LDO on PVIN and switches to the EBIAS LDO if EBIAS voltage is in the 3V to 12V range. The output of the internal LDOs are connected to the PVCC pin. A 2.2µF ceramic capacitor is recommended for decoupling PVCC. AVCC can be generated from PVCC. An RC filter is recommended to keep AVCC clean. If V_{OUT} is set to 3.3V, connecting EBIAS to V_{OUT} and using the EBIAS LDO results in better overall efficiency.

5.6 Pre-biased Output

The regulator supports pre-biased start up. When the device starts up into a pre-biased condition, both high-side and low-side MOSFETs are turned off to prevent sinking or sourcing the current into the load. The switching starts only when the output voltage rises to a pre-biased level or when soft-start is over.

5.7 High-Side Overcurrent (HSOC) Protection

After the regulator starts up, if the current through the internal high-side MOSFET is over 200% of the maximum output current, both the high-side and low-side MOSFETs are turned off. The regulator enters Hiccup mode with a 200ms period. When the high-side MOSFET current is less than 200% of the maximum output current and there are no other faults, the regulator resumes normal operation.

5.8 Low-Side Overcurrent (LSOC) Protection

After the regulator starts, if the current in low-side MOSFET is over the current limit, the device skips the high-side on-time and keeps the LS MOSFET on until the current falls below LSOC. The high-side MOSFET gets the COT pulse when the current falls below LSOC limit.

5.9 Low-Side Negative Overcurrent Protection

After the regulator starts, if the negative current in low-side MOSFET is detected to be more than the negative current limit, the low-side negative overcurrent protection is latched, the regulator turns off the low-side MOSFET, and turns on the high-side MOSFET for the on-time set by the SET resistor and PVIN.

5.10 Output Overvoltage Protection

After soft-start completes and the FB voltage is in the regulation range, the PG signal goes high. If the voltage detected on the FB pin is over 120% of the reference voltage, overvoltage protection is activated after a 1µs to 2µs delay time and the regulator enters Hiccup mode with a 200ms period. When the FB voltage is lower than 120% of the reference voltage, the regulator resumes normal operation.

5.11 Output Undervoltage Protection

If the voltage detected on the FB pin is below 70% of the reference voltage, and LSOC is also detected, undervoltage protection is activated and the regulator enters hiccup mode with a 200ms period. When the FB voltage is higher than 70% of the reference voltage and the LSOC condition has cleared, the regulator resumes normal operation. **Note:** Both low FB voltage and an LSOC conditions are required to trigger the output undervoltage protection fault. Simply having FB lower than 70% of the reference voltage does not trigger a fault.

5.12 PVIN UVLO and Enable

The regulator has UVLO on PVIN. The PVIN rising threshold is 4.15V, while the falling threshold is 3.85V. The regulator switches on when the input voltage rises above 4.15V and switches off when it falls below 3.85V. The UVLO set point can be programmed through a resistor divider between PVIN and EN, as shown in Figure 66. The resistor values are calculated using Equation 5

(EQ. 5) $$R_{EN1} = R_{EN2}\left(\frac{PVIN_{UVLO}}{V_{ENTH}} - 1\right)$$

where $PVIN_{UVLO}$ is the desired PVIN UVLO level and V_{ENTH} is the EN threshold, which is 1.5V for rising and 1.375V for falling.

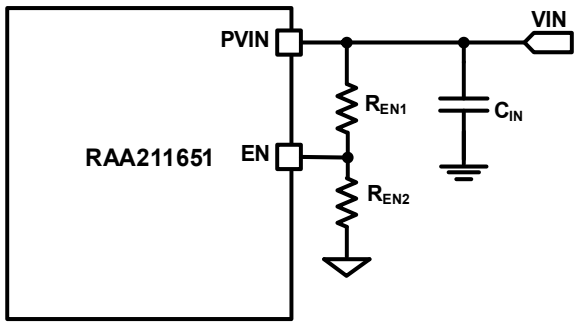


Figure 66. PVIN UVLO Using EN

5.13 Over-Temperature Protection

Over-Temperature Protection (OTP) limits the maximum junction temperature in the RAA211651. After PG is asserted, if the junction temperature reaches 153°C (typical), the regulator is shut down and PG is held low during this time. There is a 30°C hysteresis for OTP. After the junction temperature drops below 123°C, the RAA211651 resumes operation by stepping through soft-start.

5.14 AVCC Undervoltage Protection

RAA211651 has undervoltage lockout protection on AVCC to prevent the regulator from operation with insufficient bias voltage. The AVCC UVLO comparator monitors the AVCC voltage and if it goes below 2.7V, the regulator switches off. It starts up with the normal startup sequence when the AVCC voltage is over 2.9V.

6. Application Information

6.1 Design Examples

The regulator is designed using the specifications shown in Table 1.

Table 1. Regulator Design Specifications

Parameter	Symbol	Values
Input Voltage Range	PVIN	24V
Output Voltage	V_{OUT}	3.3V
Switching Frequency	f_{SW}	500kHz
Maximum Inductor Current Ripple	$I_{ripplemax}$	50%
Maximum Output Capacitor Voltage Ripple	$V_{ripplemax}$	5%
Maximum Output Current	I_{OUTmax}	5A

6.1.1 Design Example 1

The first design example uses the internal compensation, internal soft-start, and internal feedback. The application circuit is shown in Figure 67.

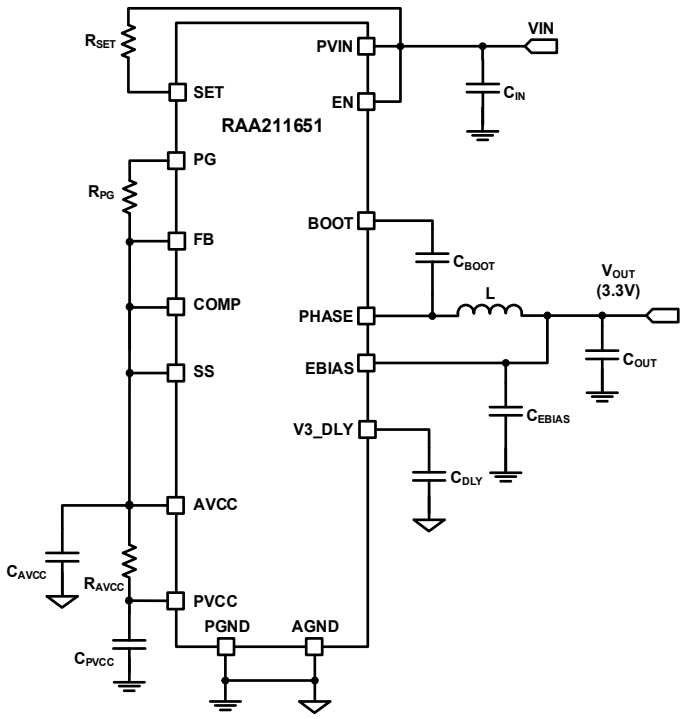


Figure 67. Application Circuit for Design Example 1

From the design specification given in Table 1, the maximum inductor current ripple and output voltage ripple are shown in Equation 6 and Equation 7.

(EQ. 6) $$\Delta I_{max} = I_{ripplemax} \times I_{OUTmax} = 0.5 \times 5 = 2.5A$$

(EQ. 7) $$\Delta V_{OUTmax} = V_{ripplemax} \times V_{OUT} = 0.05 \times 3.3 = 0.165V$$

The design of the inductor depends on the operating frequency, load current, ripple current, output voltage and input voltage. To keep the design simple for buck converters with a wide input voltage range operating in the Continuous Conduction Mode (CCM), the minimum value of the inductor required can be determined using Equation 8.

(EQ. 8) $$L_{min} \approx \frac{V_{OUT}}{\Delta I_{max} f_{sw}} = \frac{3.3}{2.5 \times 500 \times 10^3} = 2.64\mu H$$

Select an inductor with a value greater than L_{min}. The nearest standard value of 3.3µH is used. The maximum ripple expected with this inductor is shown in Equation 9.

(EQ. 9) $$I_{ripplemaxact} = \frac{V_{OUT}(1-D)}{L \times f_{SW}} = \frac{3.3\left(1-\frac{3.3}{24}\right)}{3.3 \times 10^{-6} \times 500 \times 10^3} = 1.725A$$

The peak inductor current is $I_{Lpeak} = I_{OUTmax} + I_{ripplemaxact} = 5 + 0.863 = 5.863A$.

Note: To prevent magnetic core saturation, the L selected must have a peak current rating greater than 5.863A. Also, the inductor must have an RMS current rating greater than I_{OUTmax}. Selecting an inductor with a conservative current rating results in a bulky inductor.

The output capacitor filters the inductor current ripple and delivers a smooth DC voltage to load. It must ensure the converter operates stably in all operating conditions with acceptable voltage ripple during load transients. Therefore, the selection of C_{OUT} considers the closed loop unity gain crossover frequency, voltage overshoot, and voltage undershoot requirements during load transient. The C_{OUT} selected should be the largest of all three so that all criteria are met.

(EQ. 10) $$C_{OUT} = \max(C_{Linear}, C_{OUT\_MIN\_STEP\_DOWN}, C_{OUT\_MIN\_STEP\_UP})$$

Let F_T be the unity gain crossover frequency and F_{ratio} is F_T/f_{SW}. Assuming $F_{ratio} = 0.1$, the output capacitor required is:

(EQ. 11) $$C_{Linear} = \frac{V_{REF} G_{mEA} R_{COMP}}{2\pi F_T V_{OUT} R_{CSA}} = \frac{V_{REF} G_{mEA} R_{COMP}}{2\pi F_{ratio} f_{SW} V_{OUT} R_{CSA}} = \frac{0.8 \times 14 \times 10^{-6} \times 0.5 \times 10^6}{2\pi \times 0.1 \times 500 \times 10^3 \times 3.3 \times 60 \times 10^{-3}} = 90.02\mu F$$

With a load step I_{step} = 1A, output capacitance required to keep the overshoot within limits during load step down is:

(EQ. 12) $$C_{OUT\_MIN\_STEP\_DOWN} = \frac{L\left(I_{step} + \frac{I_{ripplemaxact}}{2}\right)^2}{2V_{OUT}\Delta V_{OUT\_max}} = \frac{3.3 \times 10^{-6} \times (1+0.863)^2}{2 \times 3.3 \times 0.165} = 10.5\mu F$$

With the load step up, the output capacitance required to keep the understood within specification is:

(EQ. 13) $$C_{OUT\_MIN\_STEP\_UP} = \frac{L\left(I_{step} + \frac{I_{I_{ripplemaxact}}}{2}\right)^2}{2(V_{IN} - V_{OUT})\Delta V_{OUT\_max}} = \frac{3.3\times10^{-6}\times(1+0.863)^2}{2\times(24-3.3)\times0.165} = 1.68\mu F$$

Therefore, the C_{OUT} of 100µF is selected.

The R_{SET} determines the on-time. Its value is calculated using Equation 14.

(EQ. 14) $$R_{SET} \approx \frac{V_{OUT}}{V_{REF}\times f_{SW}\times C_T} = \frac{3.3}{0.8\times500\times10^3\times100\times10^{-12}} = 82.5k\Omega$$

For this example we designed for a delay of 1ms from the time ENABLE goes high to the time the regulator starts switching, the delay capacitor is calculated using Equation 15.

(EQ. 15) $$C_{DLY}(nF) = 4.17T_{DELAY}(ms) = 4.17\times2 = 8.34nF$$

C_{BOOT} provides the gate drive voltage for the high-side MOSFET. For this design example we designed for 0.1V drop on boot voltage each time C_{BOOT} supplies charge to the high-side MOSFET, the required C_{BOOT} is shown in Equation 16.

(EQ. 16) $$C_{BOOT} \approx \frac{Q_{gHS}}{\Delta V_{BOOT}} = \frac{10\times10^{-9}}{0.1} = 100nF$$

where Q_{gHS} is typical gate charge value for high-side MOSFET.

The input capacitor C_{IN} provides a low impedance voltage source for the regulator. It minimizes input voltage ripple and supplies the pulsating current drawn by the regulator. The minimum input capacitance required to achieve ΔV_{INMAX} is shown in Equation 17.

(EQ. 17) $$C_{INMIN} = \frac{1.5\times I_{out\_max}\times0.25}{\Delta V_{INMAX} f_{SW}} = \frac{1.5\times5\times0.25}{0.05\times500\times10^3} = 75\mu F$$

where 1.5 is the factor used for safety margin. The RMS current of the input capacitor is calculated using Equation 18

(EQ. 18) $$I_{CIN\_rms\_maz} = \frac{1.5\times I_{out\_max}}{2} = \frac{1.5\times5}{2} = 3.75A$$

Use an electrolytic capacitor of 68µF rated for input voltage. Place four 10µF ceramic capacitors in parallel and close to the IC input pins.

Renesas recommends using a 1Ω filter resistor for R_{AVCC} between PVCC and AVCC. Capacitances C_{PVCC} = 2.2µF and C_{AVCC} = 1µF are also recommended. If the PG pin monitors the PGOOD signal, Renesas recommends pulling this pin to AVCC using a 100kΩ resistor.

6.1.2 Design Example 2

The second design example implements using external compensation, external soft-start, and external feedback. The application circuit is shown in Figure 68.

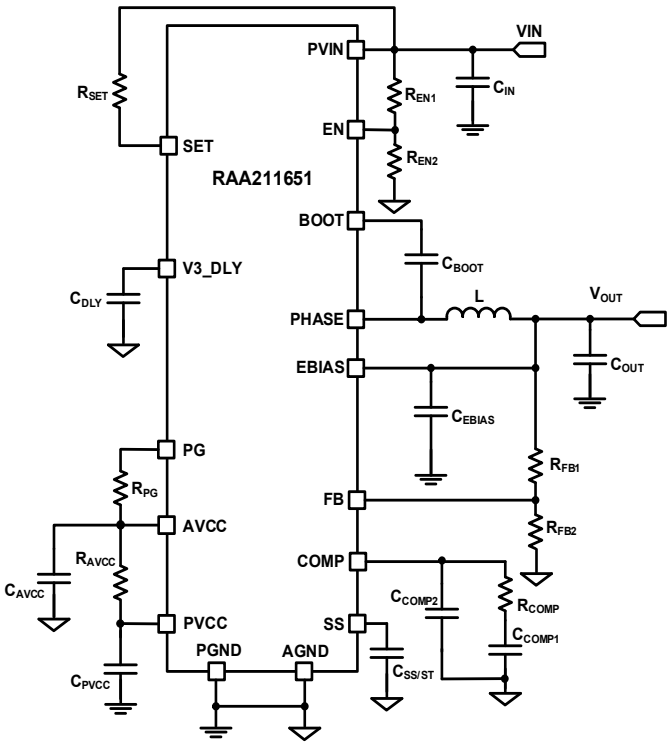


Figure 68. Application Circuit for Design Example 2

The calculation of L, $C_{OUT\_MIN\_STEP\_DOWN}$, $C_{OUT\_MIN\_STEP\_UP}$, R_{SET}, C_{DLY}, C_{BOOT}, C_{IN} are the same as in Example 1 and are not repeated here.

The ripple on V_{OUT} is 5%, considering the tolerances the compensation has to be designed targeting a much smaller ripple. Let us assume 1% ripple for a change of 1A load current. The R_{COMP} is shown in Equation 19.

(EQ. 19)
$$R_{COMP} = \frac{V_{OUT}R_{CSA}}{V_{REF}G_{m_{EA}}\frac{\Delta V_{OUT}}{\Delta I_{OUT}}} = \frac{3.3 \times 60 \times 10^{-3}}{0.8 \times 2 \times 10^{-3} \times \frac{0.033}{1}} = 3.75k\Omega$$

Assuming F_{ratio} = 0.1 and F_z is 1/10 of F_T, the compensation capacitor is shown in Equation 20.

(EQ. 20)
$$C_{COMP1} = \frac{1}{2\pi F_z R_{COMP}} = \frac{1}{2\pi \times 5 \times 10^3 \times 3.4 \times 10^3} = 8.5nF$$

The error amplifier gain for external compensation is 2mS. The output capacitor required is shown in Equation 21.

(EQ. 21)
$$C_{Linear} = \frac{V_{REF}G_{m_{EA}}R_{COMP}}{2\pi F_T V_{OUT}R_{CSA}} = \frac{V_{REF}G_{m_{EA}}R_{COMP}}{2\pi F_{ratio}f_{SW}V_{VOUT}R_{CSA}} = \frac{0.8 \times 2 \times 10^{-3} \times 3.75 \times 10^3}{2\pi \times 0.1 \times 500 \times 10^3 \times 3.3 \times 60 \times 10^{-3}} = 96.5\mu F$$

Considering the previous C_{Linear} and $C_{OUT\_MIN\_STEP\_DOWN}$ and $C_{OUT\_MIN\_STEP\_UP}$ from the first design, C_{OUT} of 100µF is selected.

To have a good feedback signal, feedback resistors in the range of a few tens of kΩ are recommended. With R_{FB2} = 20kΩ in the feedback divider, the R_{FB1} is calculated using Equation 22.

(EQ. 22) $$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) = 20 \times \left(\frac{3.3}{0.8} - 1 \right) = 62.5k\Omega$$

The soft-start time is controlled by C_{SS} capacitor. For 1ms soft-start, its value is shown in Equation 23:

(EQ. 23) $$C_{SS}(nF) = 6.25T_{SS}(ms) = 6.25 \times 1 = 6.25nF$$

R_{EN1} and R_{EN2} can be designed to change the PVIN UVLO level to a value higher than 4.25V. With R_{E2} = 10kΩ and the part enabled when PVIN reaches 6V, the required R_{E1} is shown in Equation 24.

(EQ. 24) $$R_{EN1} = R_{EN2} \times \left(\frac{V_{IN_{UVLO}}}{V_{EN_{UVLO}}} - 1 \right) = 10 \times \left(\frac{6}{1.5} - 1 \right) = 30k\Omega$$

Renesas recommends using the design spreadsheet of the regulator to plot and verify the compensation values and check the gain and phase margins.

6.2 PCB Layout Guidelines

A good layout of the Printed Circuit Board (PCB) is essential for proper functioning of the regulator.
Important: Keep all traces carrying high di/dt currents short and wide. Also, the loops formed by these pulsed currents must be as small as possible. Place the noise sensitive analog circuit components away from noise sources. To achieve proper functioning of the regulator, Renesas recommends following the layout guidelines.

- Place the ceramic input capacitor on the same PCB surface layer as the regulator and as close as possible to the pins. A small 0603 package ceramic bypass capacitor, close to the PVIN pin, is recommended.
- Place the ceramic AVCC capacitor on the same PCB surface layer as the regulator and as close as possible to the AVCC and AGND pins.
- Place the ceramic PVCC capacitor on the same PCB surface layer as the regulator and as close as possible to the PVCC and PGND pins.
- Add plenty of thermal vias under the exposed pad of the regulator for better heat dissipation.
- The copper area of the switching node should not be more than needed. Place the inductor close to regulator.
- Place the output capacitor close to the inductor.
- Route the output voltage feedback signal away from BOOST and PHASE.
- Keep the R_{SET} close to the SET pin. Avoid running other analog signal close to SET/R_{SET}.
- Keep feedback resistors close to FB pin.

The recommended PCB board layout example is shown in Figure 69 through Figure 72.

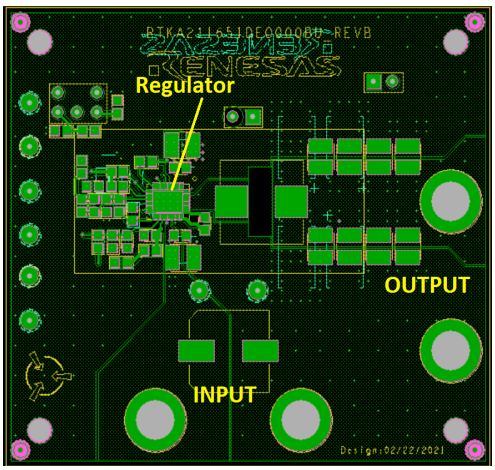


Figure 69. Top Layer

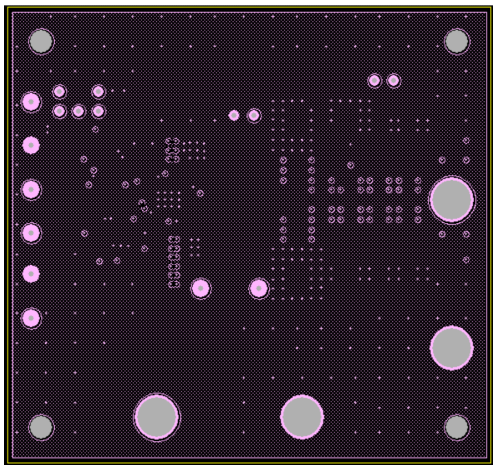


Figure 70. Second Layer

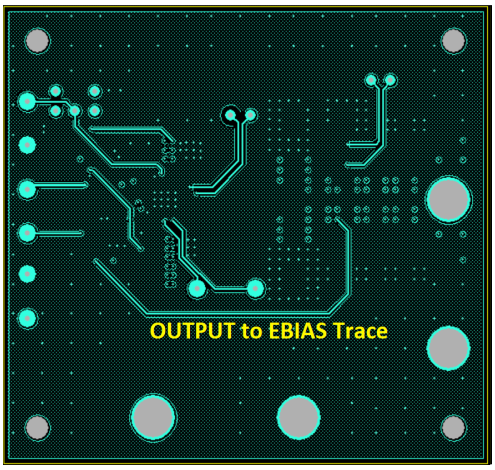


Figure 71. Third Layer

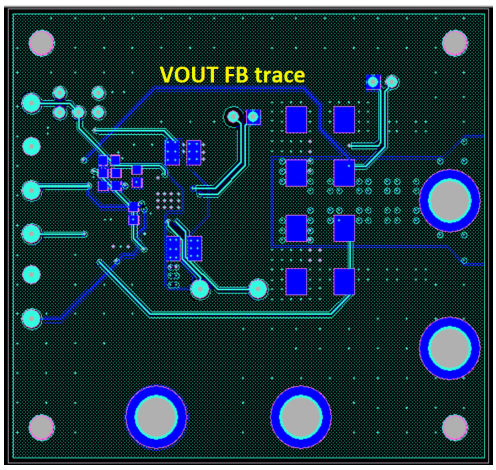


Figure 72. Bottom Layer

7. Faults Sensing and Handling

Top level faults (PVIN UVLO, VCC UVLO, OTP) stop V_{OUT} and enter the POR state until the fault is relieved. The chip then starts normally according to EN state.

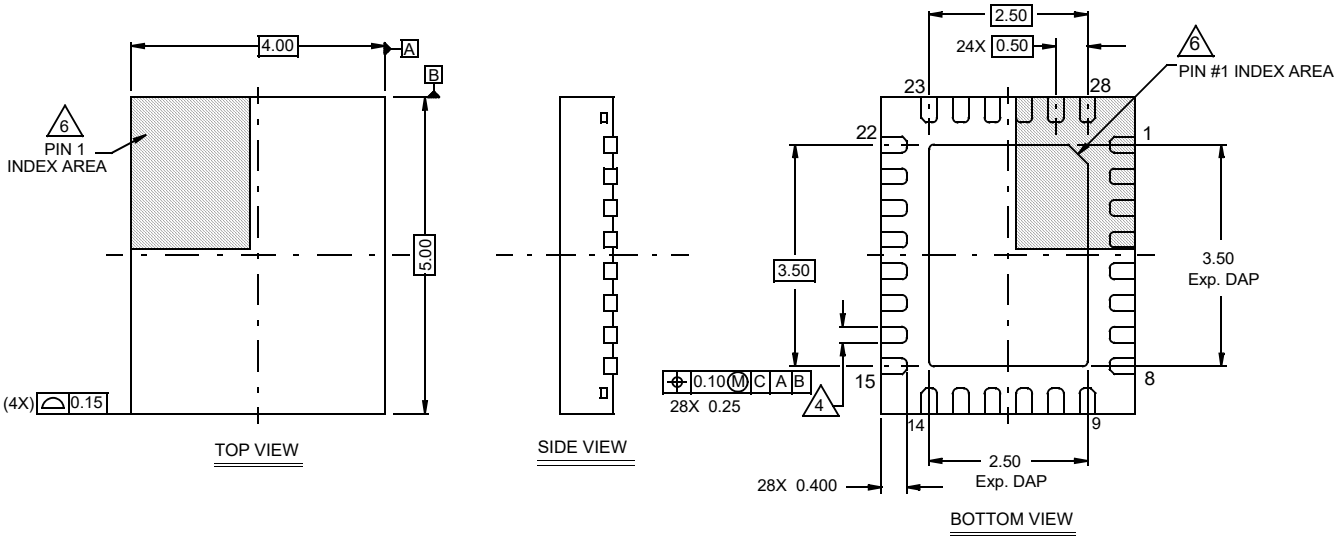
Table 2. System Level Fault Requirements

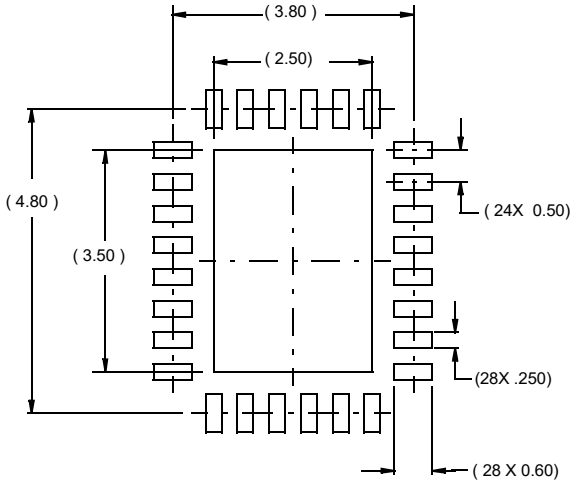
Fault Type	Detection Activated When	Detection Delay	Design Implementation
PVIN UVLO	EN is higher than threshold	1µs to 2µs	POR, chip restarts from Initial reset state when UVLO is satisfied.
Over-Temperature (OT) Shutdown	After soft-start done	N/A	When the over-temperature is detected, it stops the switching for all channels until the temperature falls its hysteresis level.
AVCC UVLO	EN is higher than threshold	1µs to 2µs detection	POR, chip restarts from initial reset state when AVCC UVLO is satisfied.
V_{OUT} Overvoltage (OV)	After POR	1µs to 2µs	If OV is detected after soft-start is done, it stops switching and enters hiccup every 200ms.
V_{OUT} Undervoltage (UV)	After soft-start done	N/A	If UV fault (VFB -<70%VREF) and low-side overcurrent fault occur simultaneously, the regulator stops switching and enters hiccup every 200ms. No fault response for UV or current limit alone. UV is blocked during soft-start
Low-Side Overcurrent (LSOC) Limit	After POR	N/A	If LSOC is detected, the device keeps LS FET on until current falls below LSOC limit.
High-Side Overcurrent (HSOC)	After POR	N/A	When the high-side current is detected to be roughly about 200% of maximum IOUT, it terminates the switching and enters hiccup every 200ms.
Low-Side Negative Overcurrent (LSNOC)	After POR	N/A	When the low-side negative overcurrent is detected, low-side MOSFET is turned off and high-side MOSFET is turned on for a time set by RSET and PVIN.

8. Package Outline Drawing

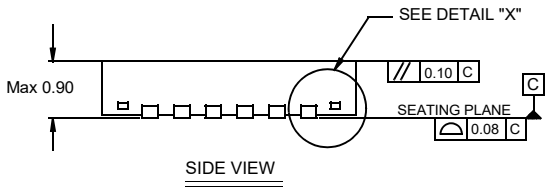
For the most recent package outline drawing, see L28.4x5A.

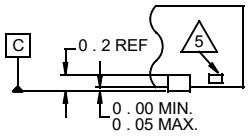
L28.4x5A
28 Lead Quad Flat No-Lead Plastic Package
Rev 2, 06/08





TYPICAL RECOMMENDED LAND PATTERN





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Junction Temp Range
RAA2116514GNP#HA0	RA211651	28 Ld QFN	L28.4x5A	Reel, 6k	-40 to +125°C
RAA2116514GNP#MA0				Reel, 250	
RTKA211651DE0000BU	Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA211651 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 3. Key Comparison between Family of Parts

Part Number	Int/Ext Comp	DEM	Int/Ext Soft-Start	Int/Ext Feedback	Programmable Delay	Modulation	Switching Frequency	Ext Freq Sync	Quiescent Current (Switching)
RAA211650	Yes	No	Yes	Yes	Yes	Valley current sampled fixed frequency PWM	fixed, resistor programmable	Yes	16.5mA
RAA211651	Yes	Yes	Yes	Yes	Yes	Constant on-time	Load dependent, resistor programmable	No	19µA

10. Revision History

Rev.	Date	Description
2.00	Dec 1, 2023	Corrected typo for the max junction and max storage temp specs by changing them to 150°C.
1.1	May 6, 2021	Updated Minimum Off-Time minimum spec from 245 to 235. Added a note reference to OVP line in the spec table. Added Figures 15, 17, and 19.
1.0	May 3, 2021	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

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