RAA458100GNP

Wireless Charging System Transmitter IC for Low Power Applications

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1. Product Outline

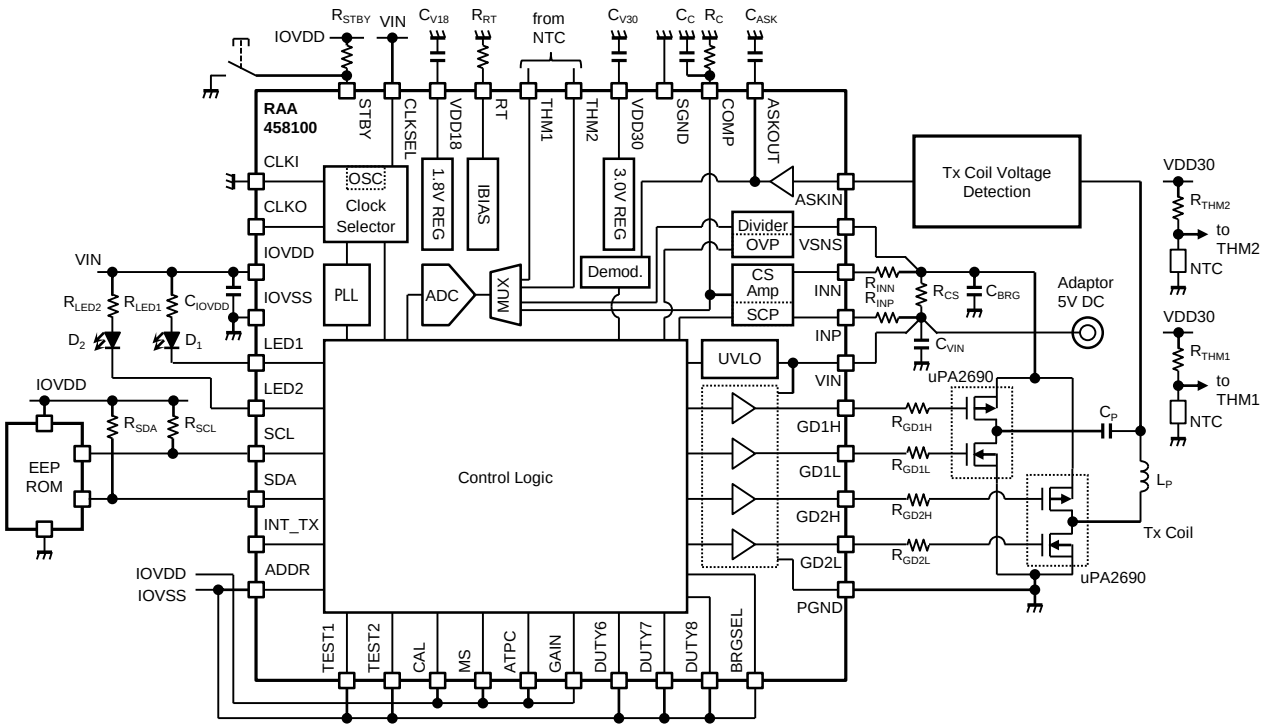
Description

RAA458100 is wireless charging system transmitter IC for low power applications. When RAA457100 is used in a receiver, a wireless charging system with bi-directional communication can be constructed.

Features

- Three operation modes which are available for various applications
  ATPC(AuTomatic Power Control）Mode , MCU Control Mode , Stand Alone Mode
- Gate drive output for MOSFET bridge circuit : half bridge or full bridge is selectable
- Over current protection for bridge circuit (OCP), Over temperature protection (THM), and various protection functions
- Monitoring input voltage or current of bridge circuit and thermistor voltage (Temperature) by 12bit A/D convertor
- Modulation/Demodulation function for bi-directional communication between transmitter and receiver
- RAA457100 registers can be set by bi-directional communication from RAA458100 (ATPC Mode)

2. Block Diagram (Example for Application Circuit : ATPC Mode)

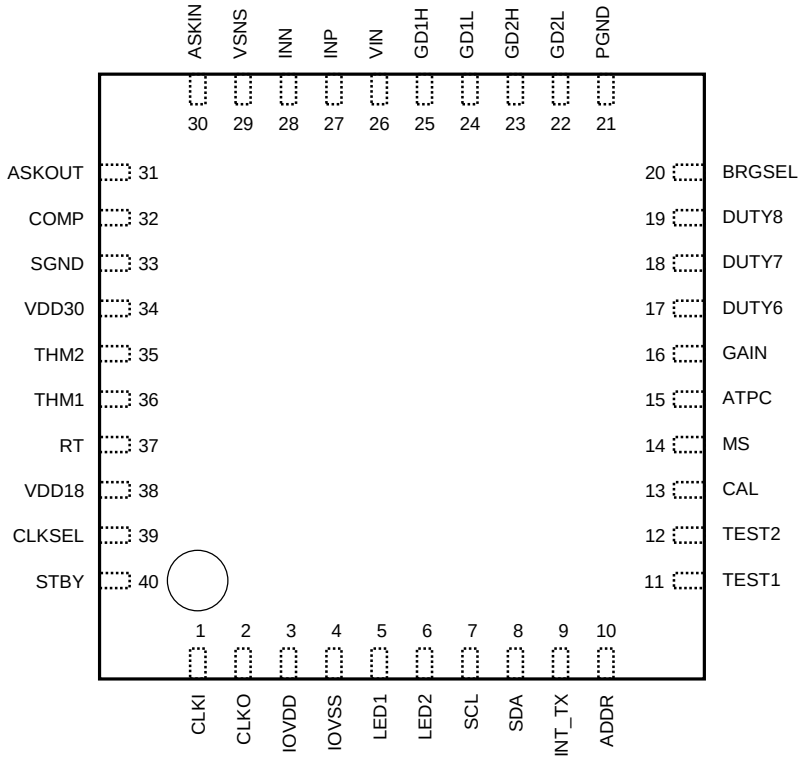


3. Pin Functions

Pin No.	Pin Name	A/D *1	I/O *2	Function	Remark
1	CLKI	D	I	Reference clock input / Connection pin to ceramic resonator	Connect to IOVSS when on-chip clock is used.
2	CLKO	D	O	Connection pin to ceramic resonator	This pin should be open, when ceramic resonator is not used.
3	IOVDD	A	I	Power supply voltage input for digital I/O	Connect C_{IOVDD} to IOVSS.
4	IOVSS	-	-	GND for digital I/O	-
5	LED1	D	O	LED driver output 1	Open drain.
6	LED2	D	O	LED driver output 2	Open drain.
7	SCL	D	I/O	Clock input or output for 2-wire serial interface	Connect R_{SCL} to IOVDD.
8	SDA	D	I/O	Data input or output for 2-wire serial interface	Connect R_{SDA} to IOVDD.
9	INT_TX	D	O	Notification output at WPT communication packet reception or abnormal condition detection	-
10	ADDR	D	I	Slave address setting pin for 2-wire serial interface	Connect to IOVDD or IOVSS.
11	TEST1	-	I	Test pin 1	Connect to IOVSS.
12	TEST2	-	I	Test pin 2	Connect to IOVSS.
13	CAL	D	I	Enable pin for CS amplifier offset calibration function	Connect to IOVDD or IOVSS.
14	MS	D	I	Master or slave device setting pin for 2-wire serial interface	Connect to IOVDD or IOVSS.
15	ATPC	D	I	Enable pin for automatic transmission power control function	Connect to IOVDD or IOVSS.
16	GAIN	D	I	Gain setting pin for automatic transmission power control	Connect to IOVDD or IOVSS.
17	DUTY6	D	I	Bridge driver output pulse duty setting pin 6	Connect to IOVDD or IOVSS.
18	DUTY7	D	I	Bridge driver output pulse duty setting pin 7	Connect to IOVDD or IOVSS.
19	DUTY8	D	I	Bridge driver output pulse duty setting pin 8	Connect to IOVDD or IOVSS.
20	BRGSEL	D	I	Selection pin for Half or Full bridge circuit	Connect to IOVDD or IOVSS.
21	PGND	-	-	GND for bridge driver	-
22	GD2L	D	O	Bridge driver output 2 (Low Side)	Driving low Side Nch MOSFET.
23	GD2H	D	O	Bridge driver output 2 (High Side)	Driving high Side Pch MOSFET.
24	GD1L	D	O	Bridge driver output 1 (Low Side)	Driving low Side Nch MOSFET.
25	GD1H	D	O	Bridge driver output 1 (High Side)	Driving high Side Pch MOSFET.
26	VIN	A	I	Power supply voltage input	Input DC5V, connect C_{VIN} to SGND.
27	INP	A	I	CS amplifier positive input	Connect R_{INP}(1kΩ) to R_{CS}.
28	INN	A	I	CS amplifier negative input	Connect R_{INN}(1kΩ) to R_{CS}.
29	VSNS	A	I	Voltage sense pin for bridge circuit input voltage	-
30	ASKIN	A	I	Amplitude modulation signal input	-
31	ASKOUT	A	O	Amplitude modulation signal output	Connect C_{ASK} to SGND.
32	COMP	A	O	CS amplifier output	Connect R_C(10kΩ) and C_C to SGND.
33	SGND	-	-	GND for internal circuits	-
34	VDD30	A	O	3.0V regulator output	Connect C_{V30} to SGND. Bias voltage for thermistor.
35	THM2	A	I	Connection pin to thermistor 2	Input divided VDD30 voltage by R_{THM2} and thermistor.
36	THM1	A	I	Connection pin to thermistor 1	Input divided VDD30 voltage by R_{THM1} and thermistor.
37	RT	A	O	Internal circuits bias current setting pin	Connect R_{RT}(100kΩ) to SGND.
38	VDD18	A	O	1.8V regulator output	Connect C_{V18} to SGND.
39	CLKSEL	D	I	Clock selection pin (on-chip clock or external clock input)	Connect to VIN or SGND.
40	STBY	D	I	Standby control	Applied to IOVDD or IOVSS voltage level. IC is activated when STBY is applied to IOVDD. IC is initialized(reset) when STBY is applied to IOVSS.

*1 A means analog signal (Including power supply voltage) and D means Digital signal.
*2 I : Input pin, O : Output pin, I/O : Input and Output pin.

4. Pin Configuration (Top View)



5. Absolute Maximum Ratings (Tj=25[degC] unless otherwise noted)

Item	Symbol	Value	Unit	Remark
Pin Voltage	VIN, IOVDD	-0.3 to 5.5	V	
	VSNS, INP, INN, CLKSEL ASKIN, LED1, LED2	-0.3 to VIN+0.3	V	Max. 5.5V
	SDA, SCL, INT_TX, MS, ATPC, GAIN, ADDR, CLKI, BRGSEL, STBY, DUTY6, DUTY7, DUTY8, TEST1, TEST2, CAL	-0.3 to IOVDD+0.3	V	Max. 5.5V
	THM1, THM2, COMP, ASKOUT	VDD30	V	
Pin Current	SDA, SCL, INT_TX	±1	mA	
	RT	-300	uA	
	COMP	-1	mA	
	LED1, LED2	10	mA	
	VDD18, VDD30	-100	uA	
Operating temperature	Ta	-20 to 60	degC	
Junction temperature	Tj	-20 to 80	degC	
Storage temperature	Tstg	-40 to 125	degC	
Thermal resistance	θj-a	35.0	degC/W	JEDEC 4L board (76.2mm x 114.3mm)

6. Recommended Operating Conditions

Item	Symbol	Value	Unit	Remark
VIN pin voltage	V_{VIN}	4.4 to 5.25	V	
IOVDD pin voltage	V_{IOVDD}	3 to 5.25	V	
Input clock frequency	f_{CLKIN}	8	MHz	

7. Electrical Characteristics

Tj=25[degC] unless otherwise noted.

Items	Symbol	Condition	min	typ	max	Unit
Power Supply Pin : VIN						
Operating voltage range	V_{OP_VIN}		4.4	5.0	5.25	V
UVLO detection voltage	$V_{UVLO\_DET\_VIN}$		3.8	3.9	4.0	V
UVLO Hysteresis voltage	$V_{UVLO\_HYS\_VIN}$		0.1	0.2	0.3	V
Operating current	I_{OP_VIN}	F_{DRV}=125kHz, C_L=510pF *1, BRGSEL=L	-	5	-	mA
Standby current	I_{STBY_VIN}	STBY=L	-	-	20	uA
PLL						
PLL output frequency	F_{PLL}		-	128	-	MHz
Bridge Driver Pin : GD1H, GD1L, GD2H, GD2L						
Switching frequency	F_{DRV}	Register f_drive[10:0]=1024	-	125	-	kHz
High level output voltage	V_{OH_GD}	Source current=-5mA	VIN-0.2	VIN-0.1	-	V
Low level output voltage	V_{OL_GD}	Sink current=5mA	-	0.1	0.2	V
3.0V Regulator Pin : VDD30						
VDD30 output voltage	V_{VDD30}		-	3.0	-	V
1.8V Regulator Pin : VDD18						
VDD18 output voltage	V_{VDD18}		-	1.8	-	V
Temperature Detection Pin : THM1, THM2						
Input voltage range	V_{I_THM}		0.0	-	V_{VDD30}	V
Bridge Circuit Current Pin : INP, INN						
Short circuit protection detection voltage	V_{SCP_DET}	R_{CS} voltage drop	-	2.2	-	V
LED Pin : LED1, LED2						
Low level output voltage	V_{OL_LED}	Sink current=1mA	-	-	0.1	V
Leak current	I_{L_LED}	LED1=5V, LED2=5V	-	-	1	uA
Standby Pin : STBY						
High level input voltage	V_{IH_STBY}	IOVDD=5V	3.5	-	-	V
Low level input voltage	V_{IL_STBY}	IOVDD=5V	-	-	1.5	V
Input current	I_{L_STBY}	STBY=5V	-	15	-	uA
ASK Input Pin : ASKIN						
ASKIN Input voltage range	V_{I_ASK}		0.0	-	V_{VDD30}	V
ASKIN Input current	I_{L_ASK}		-	1	-	uA
Digital Input Pin : ADDR, MS, ATPC, GAIN, DUTY6, DUTY7, DUTY8, BRGSEL, CLKSEL *2						
High level input voltage	V_{IH}	IOVDD=5V, VIN=5V	3.5	-	-	V
Low level input voltage	V_{IL}	IOVDD=5V, VIN=5V	-	-	1.5	V
Digital Output Pin : INT_TX						
High level output voltage	V_{OH_INT}	IOVDD=5V, Source current=-1mA	3.6	-	-	V
Low level output voltage	V_{OL_INT}	IOVDD=5V, Sink current=1mA	-	-	1.4	V
Digital Input/Output Pin : SDA, SCL						
High level input voltage	V_{IH_I2C}	IOVDD=5V	3.5	-	-	V
Low level input voltage	V_{IL_I2C}	IOVDD=5V	-	-	1.5	V
Low level output voltage	V_{OL_I2C}	IOVDD=5V, Sink current=1mA	-	-	0.2	V

*1 C_L shows the load capacitance to the bridge drivers (GD1H, GD1L, GD2H, GD2L).

*2 High level reference voltage of CLKSEL is VIN. High level reference voltage of other digital input pins is IOVDD.

8. Functions Description (The values described in this chapter are reference values, not guaranteed values.)

8.1 Operation Mode and Start Up Flow

This IC has two operation modes of Initial Mode and Drive Mode. Initial Mode is an operation mode to perform initial setting such as this IC's register setting before changing to Drive Mode. Drive Mode is an operation mode to drive a bridge circuit and transmit power to receiver. Drive Mode includes the three operation modes of ATPC Mode, MCU Control Mode and Stand Alone Mode which can be selected by some pins setting(MS, ATPC, DUTY6, DUTY7, DUTY8). Table 8.1.1 shows operation mode overview. Figure 8.1.1 shows start up flow from Initial Mode(power on reset is released) to Drive Mode(power transmitting is started).

Table 8.1.1 Operation mode overview

Operation mode	Pin setting					Description
	MS	ATPC	DUTY6	DUTY7	DUTY8	
Initial Mode	X	X	X	X	X	Initial setting such as register setting is performed based on pins setting.
Drive Mode						
Stand Alone Mode (w/o ROM , MCU)	L	L	Set one or more pins to high level			This IC operates independently. Power is transmitted on a fixed bridge frequency and duty.
ATPC Mode (w/ ROM)	H	H	L	L	L	Transmission power is controlled on receiver power information which is included in WPT communication packet. Register of this IC can be set from external EEPROM or external controller(MCU) by 2-wire serial communication. MS pin should be high level when external EEPROM is used.
ATPC Mode (w/ MCU)	L	H	L	L	L	
MCU Control Mode (w/ MCU)	L	L	L	L	L	This IC is controlled by external controller. Register setting and start / stop control of power transmitting can be performed by 2-wire serial communication.

Start up flow	Description
Initial Mode: Power On Reset	The regulators output voltages(VDD30 and VDD18 pin voltage) rise and power on reset is released when power is supplied to this IC or STBY pin is set to high level.
100ms Wait	Wait time(100ms) is set for stabilizing internal circuits after power on reset is released.
Load DUTY* Setting	DUTY6, DUTY7, DUTY8 pin settings(H/L voltage level) are loaded to the bridge driver output pulse duty setting register. DUTY6, DUTY7, DUTY8 pin settings correspond to register 0x06 D[6], 0x06 D[7], 0x07 D[0], respectively. After this timing, duty setting register can be changed from external EEPROM or external controller.
MS=H ? Yes / No; Load ROM Data	Register values of this IC are loaded from external EEPROM when MS pin is high level. If register values of this IC are written to EEPROM previously, register values can be set (such as selection of functions to use, threshold values of protection functions and so on). When MS pin is high level and DUTY6, DUTY7, DUTY8 pin all are low level, register 0x00 D[1] should be set to 1 for mode transition to Drive Mode at this timing.
CS Amp Calibration, 400ms Wait	Wait time(400ms) is set for stabilizing internal circuits. When CAL pin is high level, input offset voltage of bridge circuit current sense amplifier(CS Amp) is calibrated. It recommends high level as CAL pin voltage.
DUTY*=H ? No / Yes; 0x00 D[1]=1 ? No / Yes	When one or more pins within DUTY6, DUTY7, DUTY8 are high level, operation mode changes from Initial Mode to Drive Mode. When DUTY6, DUTY7, DUTY8 pin all are low level, operation mode does not change to Drive Mode until register 0x00 D[1] is set to 1. When this IC is controlled by external controller, register of this IC should be set at this timing. After setting desired register values, register 0x00 D[1] should be finally set to 1.
Drive Mode: ATPC=H ? Yes / No; Error Detection; ATPC Mode	**ATPC Mode** When ATPC pin is high level, ATPC Mode is selected. Power transmitting is started based on register and pins setting. When any error is detected (protection detection or WPT communication error), bridge driver output pulse duty is returned to initial value set at initial mode, and power transmitting is restarted (Restart processing). **Stand Alone Mode** When ATPC pin is low level and one or more pins within DUTY6, DUTY7, DUTY8 are high level, Stand Alone Mode is selected. Power transmitting is started on bridge driver output pulse duty set by DUTY6, DUTY7, DUTY8 pin. **MCU Control Mode** When ATPC pin is low level and DUTY6, DUTY7, DUTY8 pin all are low level, MCU Control Mode is selected. Power transmitting can be started or stopped by register 0x00 D[0]. Other register values can be also set.
DUTY*=H ? Yes / No; MCU Control Mode; Stand Alone Mode	

Figure 8.1.1 Start up flow from Initial Mode(power on reset is released) to Drive Mode(power transmitting is started)

8.2 Reference Clock

The reference clock frequency should be 8[MHz]. The reference clock source can be selected within external clock, ceramic resonator, and on chip oscillator by setting of CLKSEL, CLKI, and CLKO pin. Table 8.2.1 shows the selection of reference clock.

Table 8.2.1 Selection of reference clock

Reference clock 8[MHz]	Pin setting			Remark
	CLKSEL	CLKI	CLKO	
External clock	L	External clock	Open	CLKSEL H / L voltage level H : VIN / L : SGND CLKI, CLKO H / L voltage level H : IOVDD / L : IOVSS
Ceramic resonator	L	Ceramic resonator		
On chip oscillator	H	L	Open	

8.3 Bridge Driver (GD1H, GD1L, GD2H, GD2L pin)

Bridge driver drives full or half bridge circuit composed of external MOSFET (high side switch : Pch MOSFET, low side switch : Nch MOSFET). Figure 8.3.1 shows bridge driver output waveform for driving full bridge circuit. When half bridge circuit is selected, bridge driver outputs driving pulse from GD1H, GD1L and stops to output driving pulse from GD2H, GD2L (GD2H=H, GD2L=L). Table 8.3.1 shows parameters setting for bridge driver. Soft start function as changing duty slowly is implemented for start up and changing bridge driver output pulse duty.

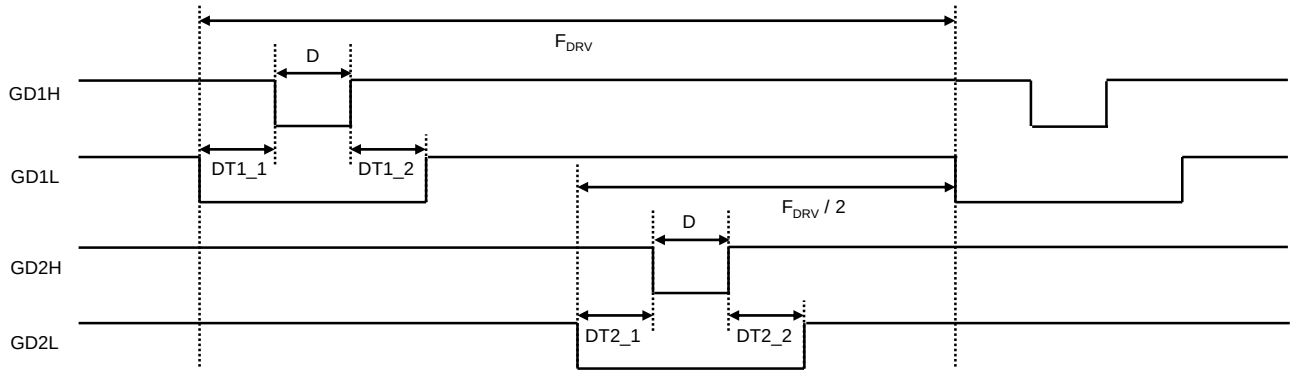


Figure 8.3.1 Bridge driver output waveform for driving MOSFET gate of full bridge circuit

Table 8.3.1 Parameters setting for bridge driver

Item	Symbol	Setting	Calculation formula, Remark
Full or half bridge selection	-	BRGSEL pin	BRGSEL=L : Driver output for full bridge circuit BRGSEL=H : Driver output for half bridge circuit
Output pulse frequency	F_{DRV}	Register f_drive[10:0] (0x05 D[2:0] , 0x04 D[7:0])	F_{DRV} = 1000 x (128 / (f_drive[10:0])) [kHz] The condition $F_{DRV} \leq 125$[kHz] is recommended.
Output pulse duty	D	Register duty[9:0] (0x07 D[1:0] , 0x06 D[7:0])	D = 100 x (duty[9:0] / f_drive[10:0]) [%] The condition D ≤ 50[%] is needed.
Output pulse dead time	DT1_1	Register dt_gd1_1[4:0] (0x09 D[4:0])	DT1_1 = 100 x (dt_gd1_1[4:0] / f_drive[10:0]) [%]
	DT1_2	Register dt_gd1_2[4:0] (0x0A D[4:0])	DT1_2 = 100 x (dt_gd1_2[4:0] / f_drive[10:0]) [%]
	DT2_1	Register dt_gd2_1[4:0] (0x0B D[4:0])	DT2_1 = 100 x (dt_gd2_1[4:0] / f_drive[10:0]) [%]
	DT2_2	Register dt_gd2_2[4:0] (0x0C D[4:0])	DT2_2 = 100 x (dt_gd2_2[4:0] / f_drive[10:0]) [%]
Output pulse duty for modulation	ΔD_{MOD}	Register modulation_duty[6:0] (0x0D D[6:0])	ΔD_{MOD} = 100 x (modulation_duty[6:0] / f_drive[10:0]) [%] (For transmitting of WPT communication packet)
Output pulse maximum duty	D_{MAX}	Register duty_max[9:0] (0x14 D[1:0] , 0x13 D[7:0])	D_{MAX} = 100 x (duty_max[9:0] / f_drive[10:0]) [%] The condition $D_{MAX} \leq 50$[%] is needed.
Output pulse setting constraints			
Only condition (1) should be satisfied for BRGSEL=H. Both of condition (1) and (2) should be satisfied for BRGSEL=L. (1) (0.5 x f_drive[10:0] > duty[9:0] + dt_gd1_1[4:0] + dt_gd1_2[4:0] + modulation_duty[6:0]) And (duty_max[9:0] > duty[9:0] + dt_gd1_1[4:0] + dt_gd1_2[4:0] + modulation_duty[6:0]) (2) (0.5 x f_drive[10:0] > duty[9:0] + dt_gd2_1[4:0] + dt_gd2_2[4:0] + modulation_duty[6:0]) And (duty_max[9:0] > duty[9:0] + dt_gd2_1[4:0] + dt_gd2_2[4:0] + modulation_duty[6:0])			

8.4 A/D Converter

Some pin voltages are converted to digital code by 12bit A/D converter. Table 8.4.1 shows the monitored items by A/D converter. These items are monitored in 4[ms] period. Some protection functions are detected by using A/D converted data. The storage registers of A/D converted data can be read by 2-wire serial communication. The storage registers aren't updated automatically. When register 0x20 D[0] is set to 1, the storage registers are updated.

Table 8.4.1 Monitored items by A/D converter

Item	Monitored pin	Output code *1	Input voltage range *2	Register
Input voltage of bridge circuit	VSNS pin voltage V_{SNS}	(4096 / 3) x V_{SNS} / 2.16	0 to 5.5 V	0x21 D[7:4] 0x22 D[7:0]
Average input current of bridge circuit (I_{BRIDGE})	COMP pin voltage V_{COMP}	(4096 / 3) x V_{COMP} V_{COMP} = CS_AMP_GAIN x V_{RCS} = 10 x V_{RCS} (CS_AMP_GAIN = R_C / R_{INP} =10) I_{BRIDGE} = V_{RCS} / R_{CS}	0 to 3.0 V	0x23 D[7:4] 0x24 D[7:0]
Thermistor temperature (THM1)	THM1 pin voltage V_{THM1}	(4096 / 3) x V_{THM1}	0 to 3.0 V	0x25 D[7:4] 0x26 D[7:0]
Thermistor temperature (THM2)	THM2 pin voltage V_{THM2}	(4096 / 3) x V_{THM2}	0 to 3.0 V	0x27 D[7:4] 0x28 D[7:0]

*1 Output code range is from 0 to 4095.
*2 Pin voltage should be within input voltage range to prevent error conversion.

8.5 LED Flashing Pattern

LED1 and LED2 pin are LED driver for displaying operation state. Flashing patterns on each operation state are implemented. External controller (MCU) can select any flashing pattern in MCU Control Mode. Table 8.5.1 shows operation mode, operation state, setting register, and LED flashing pattern.

Table 8.5.1 Operation mode, Operation state, Setting register, and LED flashing pattern

Mode	Operation state	Setting register 1	Setting register 2	Value	LED1	LED2
Initial	During start up	-	-	-	Off	Off
ATPC	Under WPT communication (Battery charging is available)	0x10 D[3]=0 led_force_mode *3	0x12 D[1:0] led_trans_sel	0	Flashing (0.25sec)	Off
				1	Off	Flashing (0.25sec)
				2	On	Off
				3	Off	On
	Under battery charging		0x12 D[2] led_charge_sel	0	On	Off
				1	Off	On
	Battery charge complete		0x12 D[4] led_end_sel	0	Off	Off
				1	Off	On
	Restart *1		0x12 D[6] led_err_sel	0	Flashing (1sec)	Off
				1	Off	Off
	Transmitting power stopped *2		0x12 D[7] led_errend_sel	0	Flashing (1sec)	Off
				1	Off	Off
Stand Alone	Transmitting power		-	-	On	Off
	Transmitter timer timeout		-	-	Off	Off
	Protection detected		-	-	Flashing (1sec)	Off
MCU Control	Selection by external controller(MCU)	0x10 D[3]=1 led_force_mode *4	0x10 D[1:0] led1_force_sel	0	Off	-
				1	Flashing (1sec)	-
				2	Flashing (0.25sec)	-
				3	On	-
			0x10 D[5:4] led2_force_sel	0	-	Off
				1	-	Flashing (1sec)
				2	-	Flashing (0.25sec)
				3	-	On

*1 Restart is processing when protection is detected or WPT communication error is occurred.
*2 Transmitting power is completely stopped when the count of protection detection or WPT communication error becomes specified number.
*3 Register setting of 0x10 D[3] should be 0 in ATPC Mode and Stand Alone Mode.
*4 Register setting of 0x10 D[3] should be 1 in MCU Control Mode. LED is off regardless of setting in 0x10 D[1:0] and 0x10 D[5:4] when 0x10 D[3] is 0.

8.6 Protection Functions

The protection functions for power supply voltage, bridge circuit and temperature are implemented. Table 8.6.1 shows protection functions. Transmitter timer is also implemented. Transmitter timer starts at the timing of mode transition to Drive Mode, power transmitting is stopped when Drive Mode continues for a fixed period. Table 8.6.2 shows the registers related to transmitter timer. Reset of this IC by power on again or STBY pin is needed to return from stopping power transmitting caused by transmitter timer.

Table 8.6.1 Protection items, threshold, detection delay time, and operation

Item (Detecting target)	Detection timing	Threshold (Release)	Detection delay time	Description
Under voltage lock out (VIN pin voltage)	At any time	3.9V (4.1V)	-	This IC becomes power on reset(POR) condition when under voltage lock out is detected. (This IC becomes POR condition regardless of VIN pin voltage when STBY pin is low.)
Short circuit protection for bridge circuit (R_{CS} voltage drop)	Drive Mode	2.2V	1us	Bridge driver is stopped (latch stop) when short circuit or over current for bridge circuit is detected at Drive Mode. The reset of this IC by power on again or STBY pin is needed to return from this protection.
Over current protection for bridge circuit (COMP pin voltage)	Drive Mode	0x16 D[3:0] 0x15 D[7:0]	16ms x 0x36 D[3:0]	
Over voltage protection for bridge circuit *2 (VSNS pin voltage)	After 16ms passed after releasing POR	5.7V (5.5V)	1ms x 4	Bridge driver is stopped when over voltage for bridge circuit is detected at Drive Mode. Operation mode does not change to Drive Mode when over voltage is detected at Initial Mode. In ATPC Mode, bridge driver output pulse duty is returned to initial value set at Initial Mode, then bridge driver restarts. In Stand Alone Mode and MCU Control Mode, bridge driver restarts when the voltage decreases to release threshold voltage.
Temperature protection 1 (THM1 pin voltage)	Drive Mode	0x18 D[3:0] 0x17 D[7:0] (0x29 D[7:0] *1)	16ms x 0x36 D[7:4]	Over temperature of a target is detected by NTC thermistor *3 . Detection threshold and hysteresis can be adjusted by setting the registers. If register value can not be changed, a threshold can be changed by adjusting a value of pull up resistor connected to the thermistor. Bridge driver is stopped when temperature protection is detected. In ATPC Mode, bridge driver output pulse duty is returned to initial value set at Initial Mode, then bridge driver restarts. In Stand Alone Mode and MCU Control Mode, bridge driver restarts when temperature decreases to release threshold.
Temperature protection 2 (THM2 pin voltage)	Drive Mode	0x1A D[3:0] 0x19 D[7:0] (0x2A D[7:0] *1)		
Maximum output pulse duty of bridge driver	Drive Mode	0x14 D[1:0] 0x13 D[7:0]	1us	Bridge driver is stopped when bridge driver output pulse duty exceeds maximum output pulse duty. In ATPC Mode, bridge driver output pulse duty is returned to initial value set at Initial Mode, then bridge driver restarts. In MCU Control Mode, bridge driver restarts when pulse duty is set under maximum output pulse duty.

*1 Hysteresis setting register.
*2 Detection voltage of over voltage protection is higher than absolute maximum rating.
The system design that this protection doesn't work is needed substantially to avoid device destruction or deterioration.
*3 NCP03WF104F05RL, NCP15WF104F03RC(Murata) or an equivalent device is recommended.

Table 8.6.2 Registers related to transmitter timer

Item	Register	Description
Transmitter timer enable	0x11 D[5]	Enable or disable selection of transmitter timer. 0 : Enable 1 : Disable(Bridge driver pulse output is continued.)
Transmitter timer timeout period setting	0x11 D[7:6]	Timeout period setting 0 : 198[min] 1 : 264[min] 2 : 330[min] 3 : 396[min]
Transmitter timer timeout notification	0x12 D[5]	Timeout notification 0 : Timeout is not detected 1 : Timeout is detected

8.7 Interruption Signal Output Function (INT_TX pin)

Interruption signal (event detection signal) is outputted from INT_TX pin when WPT communication packet is received or protection is operated (refer to Table 8.6.1). Table 8.7.1 shows the events that interruption signal is outputted. Events to output the signal can be selected by setting enable registers. When enable register value is “1”, low level is outputted from INT_TX pin when applicable event is occurred. Reset register should be set to “1” in order to return to high level at INT_TX pin. If an event occurs continuously, low level is outputted again from INT_TX pin even though reset register is set to “1”. When enable register value is “0” (disable), low level is not outputted from INT_TX pin but applicable notification register is set to “1”.

Table 8.7.1 Event to interruption signal output

Event	Notification register	Enable register	Reset register	Condition to notify (Notification register is asserted.)
WPT communication packet is received	0x1B D[1]	0x1B D[7]	0x1B D[0]	Notification register is set to “1” when WPT communication packet is received in MCU Control Mode.
WPT communication write completion	0x1B D[2]	0x1B D[7]	0x1B D[0]	These events occur in ATPC Mode. RAA458100 can write or read register of receiver device (RAA457100) by WPT communication. When register write / read operation is normally performed in receiver device, command completion information is sent from receiver device. When this IC receives the information, notification register of write completion or read completion is set to “1” and interruption signal is outputted. When register write / read operation is not performed in receiver device, this IC recognizes as WPT communication error and then the bridge driver is stopped and restarted(restart operation). Register 0x1B D[4] is set to “1” when restart is performed.
WPT communication read completion	0x1B D[3]			
Restart operation	0x1B D[4]			
Temperature protection 1	0x1D D[0]	0x1F D[0] 0x1C D[1]	0x1C D[0]	Notification register is set to “1” and interruption signal is outputted when protection showed in Table 8.6.1 is detected except for under voltage lock out detection. Enable registers(0x1F D[5:0]) for interruption signal output are assigned for each event. If interruption signal output is not needed, register 0x1C D[1] should be set to “0”. When temperature protection 1, temperature protection 2, over voltage protection for bridge circuit, or maximum output pulse duty of bridge driver is detected in ATPC Mode, the bridge driver is stopped and restarted(restart operation). Register 0x1B D[4] is set to “1” when restart is performed.
Temperature protection 2	0x1D D[1]	0x1F D[1] 0x1C D[1]		
Over voltage protection for bridge circuit	0x1D D[2]	0x1F D[2] 0x1C D[1]		
Short circuit protection for bridge circuit	0x1D D[3]	0x1F D[3] 0x1C D[1]		
Maximum output pulse duty of bridge driver	0x1D D[4]	0x1F D[4] 0x1C D[1]		
Over current protection for bridge circuit	0x1D D[5]	0x1F D[5] 0x1C D[1]		

8.8 2-wire Serial Communication Interface

RAA458100 can communicate to external ROM(EEPROM) or external controller(MCU) by 2-wire serial communication. Master device setting is needed when external ROM is used, slave device setting is needed when external controller is used. Master device or slave device can be selected by MS pin setting. Figure 8.8.1(a), (b) shows SDA data format in slave device. Figure 8.8.2 shows timing specification.

Table 8.8.1 Outline of 2-wire serial communication

MS pin	SCL Frequency	Description
L (IOVSS)	64 [kHz]	RAA458100 is slave device for 2-wire serial communication. External controller can write / read the register of RAA458100. The slave address can be changed by ADDR pin. ADDR pin =L : 0001010, ADDR pin =H : 1101010
H (IOVDD)	64 [kHz]	RAA458100 is master device for 2-wire serial communication. RAA458100 can read register setting values from EEPROM in Initial Mode. The communication between RAA458100 and EEPROM is read operation only. The slave address of EEPROM can be selected by ADDR pin. ADDR pin =L : 1010000, ADDR pin =H : 1010001

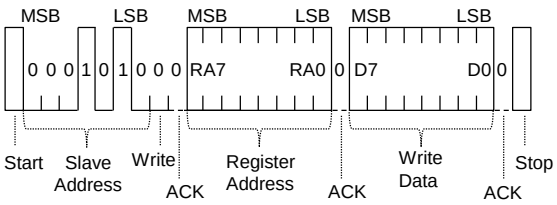


Figure 8.8.1(a) SDA data format (Slave, Write)

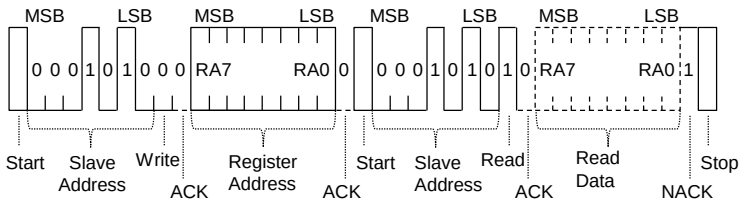
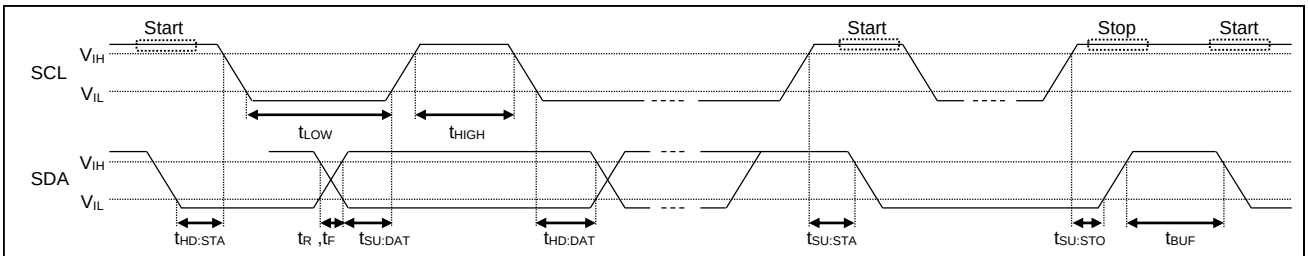


Figure 8.8.1(b) SDA data format (Slave, Read)



Symbol	Item	Min	Max	Unit
fSCL	SCL clock frequency	0	64	kHz
tBUF	Bus free time between Stop condition and Start condition	8.1	-	us
tHD:STA	Hold time of Start condition or repeated Start condition (First clock pulse is generated after this period.)	3.7	-	us
tLOW	Low hold time of the SCL clock	8.1	-	us
tHIGH	High hold time of the SCL clock	3.7	-	us
tSU:STA	Set-up time for a repeated Start condition	3.7	-	us
tHD:DAT	Data hold time (for input data)	3.7	-	us
tSU:DAT	Data set-up time	3.7	-	us
tR	Rise time of both SDA and SCL signals	-	0.3	us
tF	Fall time of both SDA and SCL signals	-	0.3	us
tSU:STO	Set-up time for Stop condition	3.7	-	us

Figure 8.8.2 SCL and SDA timing specification of 2-wire serial communication (for reference)

8.9 WPT Communication

8.9.1 Outline

RAA458100 and RAA457100(Receiver IC) support a bidirectional communication by amplitude modulation on wireless power transmission carrier signal. In receiver to transmitter communication, RAA457100 changes transmitting antenna voltage by load modulation and then RAA458100 detects the voltage variation and demodulates data. In transmitter to receiver communication, RAA458100 changes rectified voltage of RAA457100 by changing transmission power and then RAA457100 detects the voltage variation and demodulates data.

8.9.2 Packet Format in WPT Communication

The packet of WPT communication is consisted of fixed data length packet including Preamble, Header, Message1, Message2, Checksum showed in Figure 8.9.2. The Header, Message1, Message2 have 1 bit of odd parity bit respectively, and the check sum generated by exclusive OR is added to the last of the packet. When ATPC pin level of RAA458100 and RAA457100 is high, automatic transmission power control function is available (ATPC Mode). In ATPC Mode, the packet which includes a special header code (0x00 to 0x0F) is sent from RAA457100 to RAA458100 periodically, and RAA458100 adjusts transmission power based on the data included in packet.

Preamble (11bit)	St	Header (8bit)	Pr	Sp	St	Message1 (8bit)	Pr	Sp	St	Message2 (8bit)	Pr	Sp	St	Checksum (8bit)	Pr	Sp

St : Start bit(1bit), Pr : Parity bit(1bit), Sp : Stop bit(1bit)

Figure 8.9.2 Data packet format

Table 8.9.2 Header code

Header code	Explanation
0x00 to 0x0F	Header code for automatic transmission power control (ATPC Mode)
0x10 to 0xFF	Header code for any user purpose

8.9.3 Data Transfer Function

The transmission power is modulated by changing bridge driver output pulse duty depending on packet data.

8.9.4 Data Receive Function

A data packet described in Figure 8.9.2 sent from receiver is demodulated.
The voltage variation on transmitting antenna is detected and demodulated by a buffer amplifier (input : ASKIN pin, output : ASKOUT pin) and demodulation circuits.

8.9.5 Communication Bit Rate

Table 8.9.5 shows communication bit rate. The transmission data rate is 125[bps], the reception data rate is 250[bps].

Table 8.9.5 Setting for communication rate

Communication direction	Bit rate	Remark
Data transmission (Transmitter to receiver)	125bps	
Data reception (Receiver to transmitter)	250bps	

9. Register Map (The values described in this chapter are reference values, not guaranteed values.)

9.1 Address 0x00 to 0x07 (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x00	D0	drive_on	0	R/W	Bridge driver ON/OFF control in MCU Control Mode. 0 : OFF 1 : ON
	D1	drive_mode_on	0	R/W	The register to change operation mode when DUTY6,7,8 pin all are low level. 0 : Initial Mode 1 : Change to Drive Mode
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6	auto_drive_on	0	R	Bridge driver ON/OFF notification in ATPC Mode and Stand Alone Mode. 0 : OFF 1 : ON
	D7	atpc_eep_end_mode	0	R	Data loading from ROM(EEPROM) completion notification in ATPC Mode. 0 : Not complete 1 : Completed
0x01	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		1	R/W	
	D2		1	R/W	
	D3		1	R/W	
	D4		0	R/W	
	D5		0	R/W	
	D6		0	R/W	
	D7		0	R/W	
0x02	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4		0	R/W	
	D5		0	R/W	
	D6		0	R/W	
	D7		0	R/W	
0x03	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4		0	R/W	
	D5		0	R/W	
	D6		0	R/W	
	D7		0	R/W	
0x04	D0	f_drive [0]	0	R/W	Frequency of bridge driver output pulse. Frequency F_{DRV} = 1000 x (128 / f_drive[10:0]) [kHz]. This register value is applied when register 0x05 D[7] is set to “1”.
	D1	f_drive [1]	0	R/W	
	D2	f_drive [2]	0	R/W	
	D3	f_drive [3]	0	R/W	
	D4	f_drive [4]	0	R/W	
	D5	f_drive [5]	0	R/W	
	D6	f_drive [6]	0	R/W	
	D7	f_drive [7]	0	R/W	
0x05	D0	f_drive [8]	0	R/W	
	D1	f_drive [9]	0	R/W	
	D2	f_drive [10]	1	R/W	
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7	f_drive_reg_update	0	R/W	1 : The value of f_drive[10:0] is applied. (This register automatically returns to 0 after applying.)
0x06	D0	duty [0]	0	R/W	Duty of bridge driver output pulse. Duty = 100 x (duty[9:0] / f_drive[10:0]) [%]. This register value is applied when register 0x07 D[7] is set to “1”.
	D1	duty [1]	0	R/W	
	D2	duty [2]	0	R/W	
	D3	duty [3]	0	R/W	
	D4	duty [4]	0	R/W	
	D5	duty [5]	0	R/W	
	D6	duty [6]	0	R/W	
	D7	duty [7]	0	R/W	
0x07	D0	duty [8]	0	R/W	
	D1	duty [9]	0	R/W	
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7	duty_reg_update	0	R/W	1 : The value of duty[9:0] is applied. (This register automatically returns to 0 after applying.)

9.2 Address 0x08 to 0x0F (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x08	D0	ss_interval [0]	0	R/W	Duty code transition time of bridge driver output pulse [code/F_{DRV}]. 0 : 1 1 : 1/2 2 : 1/3 3 : 1/4 4 : 1/5 5 : 1/6 6 : 1/7 7 : 1/8 Setting example "2": Driver output pulse duty is changed by 1 code at every 3 pulse periods when duty setting is changed.
	D1	ss_interval [1]	0	R/W	
	D2	ss_interval [2]	0	R/W	
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7		0	R/W	*1
0x09	D0	dt_gd1_1 [0]	0	R/W	Dead time of bridge driver output pulse (DT1_1). DT1_1 = 100 x (dt_gd1_1[4:0] / f_drive[10:0]) [%].
	D1	dt_gd1_1 [1]	0	R/W	
	D2	dt_gd1_1 [2]	0	R/W	
	D3	dt_gd1_1 [3]	0	R/W	
	D4	dt_gd1_1 [4]	1	R/W	
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7		0	R/W	*1
0x0A	D0	dt_gd1_2 [0]	0	R/W	Dead time of bridge driver output pulse (DT1_2). DT1_2 = 100 x (dt_gd1_2[4:0] / f_drive[10:0]) [%].
	D1	dt_gd1_2 [1]	0	R/W	
	D2	dt_gd1_2 [2]	0	R/W	
	D3	dt_gd1_2 [3]	0	R/W	
	D4	dt_gd1_2 [4]	1	R/W	
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7		0	R/W	*1
0x0B	D0	dt_gd2_1 [0]	0	R/W	Dead time of bridge driver output pulse (DT2_1). DT2_1 = 100 x (dt_gd2_1[4:0] / f_drive[10:0]) [%].
	D1	dt_gd2_1 [1]	0	R/W	
	D2	dt_gd2_1 [2]	0	R/W	
	D3	dt_gd2_1 [3]	0	R/W	
	D4	dt_gd2_1 [4]	1	R/W	
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7		0	R/W	*1
0x0C	D0	dt_gd2_2 [0]	0	R/W	Dead time of bridge driver output pulse (DT2_2). DT2_2 = 100 x (dt_gd2_2[4:0] / f_drive[10:0]) [%].
	D1	dt_gd2_2 [1]	0	R/W	
	D2	dt_gd2_2 [2]	0	R/W	
	D3	dt_gd2_2 [3]	0	R/W	
	D4	dt_gd2_2 [4]	1	R/W	
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7		0	R/W	*1
0x0D	D0	modulation_duty [0]	1	R/W	Modulation duty of bridge driver output pulse (ΔD_{MOD}). ΔD_{MOD} = 100 x (modulation_duty[6:0] / f_drive[10:0]) [%].
	D1	modulation_duty [1]	0	R/W	
	D2	modulation_duty [2]	0	R/W	
	D3	modulation_duty [3]	1	R/W	
	D4	modulation_duty [4]	0	R/W	
	D5	modulation_duty [5]	1	R/W	
	D6	modulation_duty [6]	0	R/W	
	D7	modulation_code	0	R/W	0 : Add ΔD_{MOD} to current duty 1 : Subtract ΔD_{MOD} from current duty
0x0E	D0		0	R/W	*1
	D1	modulation_frequency [0]	0	R/W	WPT communication data rate setting (Transmitter to Receiver communication). 0 : 125bps 1 : 250bps 2 : 500bps 3 : 1000bps
	D2	modulation_frequency [1]	0	R/W	
	D3		0	R/W	*1
	D4	modulation_start	0	R/W	In MCU Control Mode, WPT communication start. 1 : Start WPT modulation (This register automatically returns to 0 after processing.)
	D5	modulation_start_sync	0	R/W	In ATPC Mode with external controller, WPT communication start. 1 : Start WPT modulation (This register automatically returns to 0 after processing.)
	D6		0	R/W	*1
	D7		0	R/W	*1
0x0F	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4		0	R/W	
	D5		0	R/W	
	D6		0	R/W	
	D7		0	R/W	

9.3 Address 0x10 to 0x17 (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x10	D0	led1_force_sel [0]	0	R/W	LED1 flashing pattern selection. Refer to Table 8.5.1 for setting.
	D1	led1_force_sel [1]	0	R/W	
	D2		0	R/W	*1
	D3	led_force_mode	0	R/W	LED1,2 control setting. Refer to Table 8.5.1 for setting.
	D4	led2_force_sel [0]	0	R/W	LED2 flashing pattern selection. Refer to Table 8.5.1 for setting.
	D5	led2_force_sel [1]	0	R/W	
	D6		0	R/W	*1
	D7		0	R/W	*1
0x11	D0	cntrl_err_th [0]	1	R/W	Threshold to detect control error convergence. Control error convergence is detected if absolute value of control error sent from receiver is smaller than this threshold. Control error convergence is one of conditions for starting WPT communication packet in ATPC Mode.
	D1	cntrl_err_th [1]	1	R/W	
	D2	cntrl_err_th [2]	1	R/W	
	D3	cntrl_err_th [3]	1	R/W	
	D4	cntrl_err_th [4]	0	R/W	
	D5	tim_chg_off	0	R/W	Transmitter timer enable or disable selection. 0 : Enable 1 : Disable
	D6	tim_chg_cccv [0]	1	R/W	Transmitter timer timeout period. 0 : 198[min] 1 : 264[min] 2 : 330[min] 3 : 396[min]
	D7	tim_chg_cccv [1]	1	R/W	
0x12	D0	led_trans_sel [0]	0	R/W	LED flashing pattern setting under WPT communication (battery charging available) in ATPC Mode. Refer to Table 8.5.1 for setting.
	D1	led_trans_sel [1]	0	R/W	
	D2	led_charge_sel	0	R/W	LED flashing pattern setting under battery charging in ATPC Mode. Refer to Table 8.5.1 for setting.
	D3		0	R/W	*1
	D4	led_end_sel	0	R/W	LED flashing pattern setting for battery charge complete in ATPC Mode. Refer to Table 8.5.1 for setting.
	D5	tim_chg_end_flag	0	R	Timeout notification of transmitter timer. 0 : Not detected 1 : Detected
	D6	led_err_sel	0	R/W	LED flashing pattern setting for restart in ATPC Mode. Refer to Table 8.5.1 for setting.
	D7	led_errend_sel	0	R/W	LED flashing pattern setting for transmitting power stopped in ATPC Mode. Refer to Table 8.5.1 for setting.
0x13	D0	duty_max [0]	1	R/W	Maximum duty threshold for bridge driver output pulse (D_{MAX}). D_{MAX} = 100 x (duty_max[9:0] / f_drive[10:0]) [%]. This register value is applied when register 0x14 D[7] is set to “1”.
	D1	duty_max [1]	1	R/W	
	D2	duty_max [2]	0	R/W	
	D3	duty_max [3]	0	R/W	
	D4	duty_max [4]	0	R/W	
	D5	duty_max [5]	0	R/W	
	D6	duty_max [6]	1	R/W	
	D7	duty_max [7]	1	R/W	
0x14	D0	duty_max [8]	1	R/W	
	D1	duty_max [9]	0	R/W	
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7	duty_max_reg_update	0	R/W	1 : The value of duty_max[9:0] is applied. (This register automatically returns to 0 after applying.)
0x15	D0	ibridge_max [0]	0	R/W	Over current protection threshold for bridge circuit. 0.7324[mV/code] (Converted to COMP pin voltage). (0.7324 / CS_AMP_GAIN) / R_{CS} [mA/code] (Converted to the input current of bridge circuit). This register value is applied when register 0x16 D[7] is set to “1”.
	D1	ibridge_max [1]	0	R/W	
	D2	ibridge_max [2]	0	R/W	
	D3	ibridge_max [3]	0	R/W	
	D4	ibridge_max [4]	0	R/W	
	D5	ibridge_max [5]	0	R/W	
	D6	ibridge_max [6]	0	R/W	
	D7	ibridge_max [7]	0	R/W	
0x16	D0	ibridge_max [8]	0	R/W	
	D1	ibridge_max [9]	0	R/W	
	D2	ibridge_max [10]	0	R/W	
	D3	ibridge_max [11]	1	R/W	
	D4	ocp_short_off	0	R/W	Short circuit protection for bridge circuit enable or disable selection. 0 : Enable 1 : Disable
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7	ibridge_max_reg_update	0	R/W	1 : The value of ibridge_max[11:0] is applied. (This register automatically returns to 0 after applying.)
0x17	D0	th1h [0]	0	R/W	Temperature protection 1 threshold. (NTC thermistor must be used.) This threshold is compared with AD converted data of THM1 pin voltage. 0.7324[mV/code] (Converted to THM1 pin voltage). This register value is applied when register 0x18 D[7] is set to “1”. Release threshold of this protection is set to th1h[11:0] + { 0, th1h_hys[7:0], 000 }.
	D1	th1h [1]	1	R/W	
	D2	th1h [2]	0	R/W	
	D3	th1h [3]	1	R/W	
	D4	th1h [4]	0	R/W	
	D5	th1h [5]	1	R/W	
	D6	th1h [6]	0	R/W	
	D7	th1h [7]	1	R/W	

9.4 Address 0x18 to 0x1F (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x18	D0	th1h [8]	0	R/W	Refer to description of th1h [7:0].
	D1	th1h [9]	1	R/W	
	D2	th1h [10]	0	R/W	
	D3	th1h [11]	0	R/W	
	D4	th_recover	0	R/W	Restart condition in temperature protection in ATPC Mode. 1 : Do not restart until releasing temperature protection.
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7	th1h_reg_update	0	R/W	1 : The value of th1h[11:0] is applied. (This register automatically returns to 0 after applying.)
0x19	D0	th2h [0]	0	R/W	Temperature protection 2 threshold. (NTC thermistor must be used.) This threshold is compared with AD converted data of THM2 pin voltage. 0.7324[mV/code] (Converted to THM2 pin voltage). This register value is applied when register 0x1A D[7] is set to “1”. Release threshold of this protection is set to th2h[11:0] + { 0, th2h_hys[7:0], 000 }.
	D1	th2h [1]	1	R/W	
	D2	th2h [2]	0	R/W	
	D3	th2h [3]	1	R/W	
	D4	th2h [4]	0	R/W	
	D5	th2h [5]	1	R/W	
	D6	th2h [6]	0	R/W	
	D7	th2h [7]	1	R/W	
0x1A	D0	th2h [8]	0	R/W	
	D1	th2h [9]	1	R/W	
	D2	th2h [10]	0	R/W	
	D3	th2h [11]	0	R/W	
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7	th2h_reg_update	0	R/W	1 : The value of th2h[11:0] is applied. (This register automatically returns to 0 after applying.)
0x1B	D0	int_rcv_rst	0	R/W	1 : Notification registers 0x1B D[4:1] are cleared, and then this register automatically returns to 0.
	D1	intrcv	0	R	Notification of WPT communication packet reception in MCU Control Mode. 0 : Not received 1 : Received
	D2	int_rcv_write	0	R	Notification of receiver device’s register write completion in ATPC Mode. 1 : Write is completed
	D3	int_rcv_read	0	R	Notification of receiver device’s register read completion in ATPC Mode. 1 : Read is completed
	D4	int_atpcerr	0	R	Notification of restart in ATPC Mode. 1 : Restart is performed
	D5	wpt_rcv	0	R	Notification of under reception condition of WPT communication packet. 1 : Packet is receiving
	D6	wpt_send	0	R	Notification of under transmission condition of WPT communication packet. 1 : Packet is transmitting
	D7	int_rcv_en	1	R/W	INT_TX pin output selection when events notified by 0x1B D[4:1] are occurred. 0 : Not output 1 : Output
0x1C	D0	int_state_rst	0	R/W	1 : Notification registers 0x1D D[5:0] are cleared, and then this register automatically returns to 0.
	D1	int_state_en	1	R/W	INT_TX pin output selection when events notified by 0x1D D[5:0] are occurred. 0 : Not output 1 : Output
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6	int_pin_inv	0	R/W	INT_TX pin output polarity inversion. 0 : Normal(Low level at interruption) 1 : Inversion(High level at interruption)
	D7	int_pin_fix	0	R/W	INT_TX pin output enable. 0 : Enable(output based on event) 1 : Disable(Not output based on event)
0x1D	D0	int_th1	0	R	Notification of temperature protection 1. 0 : Not detected 1 : Detected
	D1	int_th2	0	R	Notification of temperature protection 2. 0 : Not detected 1 : Detected
	D2	int_ovp	0	R	Notification of over voltage protection for bridge circuit. 0 : Not detected 1 : Detected
	D3	int_ocp_short	0	R	Notification of short circuit protection for bridge circuit. 0 : Not detected 1 : Detected
	D4	int_duty_max	0	R	Notification of maximum output pulse duty of bridge driver. 0 : Not detected 1 : Detected
	D5	int_ibridge_max	0	R	notification of over current protection for bridge circuit. 0 : Not detected 1: :Detected
	D6		0	R/W	*1
	D7		0	R/W	*1
0x1E	D0		0	R	Test register. Write access is NOT allowed.
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R/W	
	D7		0	R/W	
0x1F	D0	int_th1_en	1	R/W	INT_TX pin output selection when temperature protection 1 is detected. 0 : Not output 1 : Output
	D1	int_th2_en	1	R/W	INT_TX pin output selection when temperature protection 2 is detected. 0 : Not output 1 : Output
	D2	Int_ovp_en	1	R/W	INT_TX pin output selection when over voltage protection is detected. 0 : Not output 1 : Output
	D3	int_ocp_short_en	1	R/W	INT_TX pin output selection when short circuit protection is detected. 0 : Not output 1 : Output
	D4	int_duty_max_en	1	R/W	INT_TX pin output selection when maximum output pulse duty is detected. 0 : Not output 1 : Output
	D5	int_ibridge_max_en	1	R/W	INT_TX pin output selection when over current protection is detected. 0 : Not output 1 : Output
	D6		0	R/W	*1
	D7		0	R/W	*1

9.5 Address 0x20 to 0x27 (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x20	D0	adc_upload	0	R/W	1 : AD converted data is uploaded to the registers of 0x21 to 0x28.
	D1	atpc_auto_upload_off	1	R/W	Uploaded timing for the storage registers of AD converted data (0x21 to 0x28) in ATPC Mode. 0: When 0x20 D[0]=1 is written, the registers are uploaded after receiving WPT communication packet. 1: When 0x20 D[0]=1 is written, the registers are uploaded immediately.
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4		0	R/W	*1
	D5		0	R/W	*1
	D6		0	R/W	*1
	D7		0	R/W	*1
0x21	D0		0	R/W	*1
	D1		0	R/W	*1
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4	vbridge [0]	0	R	AD converted data of input voltage of bridge circuit. 1.5820[mV/code] (Converted to VSNS pin voltage)
	D5	vbridge [1]	0	R	
	D6	vbridge [2]	0	R	
	D7	vbridge [3]	0	R	
0x22	D0	vbridge [4]	0	R	
	D1	vbridge [5]	0	R	
	D2	vbridge [6]	0	R	
	D3	vbridge [7]	0	R	
	D4	vbridge [8]	0	R	
	D5	vbridge [9]	0	R	
	D6	vbridge [10]	0	R	
	D7	vbridge [11]	0	R	
0x23	D0		0	R/W	*1
	D1		0	R/W	*1
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4	ibridge [0]	0	R	AD converted data of average input current of bridge circuit. 0.7324[mV/code] (Converted to COMP pin voltage) (0.7324 / CS_AMP_GAIN) / R_{CS} [mA/code] (Converted to average input current)
	D5	ibridge [1]	0	R	
	D6	ibridge [2]	0	R	
	D7	ibridge [3]	0	R	
0x24	D0	ibridge [4]	0	R	
	D1	ibridge [5]	0	R	
	D2	ibridge [6]	0	R	
	D3	ibridge [7]	0	R	
	D4	ibridge [8]	0	R	
	D5	ibridge [9]	0	R	
	D6	ibridge [10]	0	R	
	D7	ibridge [11]	0	R	
0x25	D0		0	R/W	*1
	D1		0	R/W	*1
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4	th1 [0]	0	R	AD converted data of thermistor temperature 1. 0.7324[mV/code] (Converted to THM1 pin voltage)
	D5	th1 [1]	0	R	
	D6	th1 [2]	0	R	
	D7	th1 [3]	0	R	
0x26	D0	th1 [4]	0	R	
	D1	th1 [5]	0	R	
	D2	th1 [6]	0	R	
	D3	th1 [7]	0	R	
	D4	th1 [8]	0	R	
	D5	th1 [9]	0	R	
	D6	th1 [10]	0	R	
	D7	th1 [11]	0	R	
0x27	D0		0	R/W	*1
	D1		0	R/W	*1
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4	th2 [0]	0	R	AD converted data of thermistor temperature 2. 0.7324[mV/code] (Converted to THM2 pin voltage)
	D5	th2 [1]	0	R	
	D6	th2 [2]	0	R	
	D7	th2 [3]	0	R	

9.6 Address 0x28 to 0x2F (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x28	D0	th2 [4]	0	R	Refer to description of th2 [3:0].
	D1	th2 [5]	0	R	
	D2	th2 [6]	0	R	
	D3	th2 [7]	0	R	
	D4	th2 [8]	0	R	
	D5	th2 [9]	0	R	
	D6	th2 [10]	0	R	
	D7	th2 [11]	0	R	
0x29	D0	th1h_hys[0]	0	R/W	Hysteresis of temperature protection 1 threshold. After detecting temperature protection, { 0, th1h_hys[7:0], 000 } is added to th1h[11:0]. That means protection release threshold is set to th1h[11:0] + { 0, th1h_hys[7:0], 000 }.
	D1	th1h_hys[1]	1	R/W	
	D2	th1h_hys[2]	0	R/W	
	D3	th1h_hys[3]	1	R/W	
	D4	th1h_hys[4]	0	R/W	
	D5	th1h_hys[5]	0	R/W	
	D6	th1h_hys[6]	0	R/W	
	D7	th1h_hys[7]	0	R/W	
0x2A	D0	th2h_hys[0]	0	R/W	Hysteresis of temperature protection 2 threshold. After detecting temperature protection, { 0, th2h_hys[7:0], 000 } is added to th2h[11:0]. That means protection release threshold is set to th2h[11:0] + { 0, th2h_hys[7:0], 000 }.
	D1	th2h_hys[1]	1	R/W	
	D2	th2h_hys[2]	0	R/W	
	D3	th2h_hys[3]	1	R/W	
	D4	th2h_hys[4]	0	R/W	
	D5	th2h_hys[5]	0	R/W	
	D6	th2h_hys[6]	0	R/W	
	D7	th2h_hys[7]	0	R/W	
0x2B	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x2C	D0		0	R	Test register.
	D1		0	R	
	D2		0	R	
	D3		0	R	
	D4		0	R	
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x2D	D0		0	R/W	*1
	D1		0	R/W	*1
	D2		0	R/W	*1
	D3		0	R/W	*1
	D4	Ibridge_offset [0]	0	R	AD converted result of input offset current of bridge circuit (offset voltage of CS amplifier). 0.7324[mV/code] (Converted to COMP pin voltage) (0.7324 / CS_AMP_GAIN) / R_{CS} [mA/code] (Converted to input current of bridge circuit) When CAL pin is high level, offset current is acquired at Initial Mode. The data subtracted this offset current from original AD converted data is stored to 0x24 D[7:0], 0x23 D[7:4].
	D5	Ibridge_offset [1]	0	R	
	D6	Ibridge_offset [2]	0	R	
	D7	Ibridge_offset [3]	0	R	
0x2E	D0	Ibridge_offset [4]	0	R	
	D1	Ibridge_offset [5]	0	R	
	D2	Ibridge_offset [6]	0	R	
	D3	Ibridge_offset [7]	0	R	
	D4	Ibridge_offset [8]	0	R	
	D5	Ibridge_offset [9]	0	R	
	D6	Ibridge_offset [10]	0	R	
	D7	Ibridge_offset [11]	0	R	
0x2F	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4		0	R/W	
	D5		0	R/W	
	D6		0	R/W	
	D7		0	R/W	

9.7 Address 0x30 to 0x37 (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x30	D0	wpt_r_diff_wait [0]	1	R/W	Timing to acquire ASKOUT pin voltage variation for WPT communication packet demodulation. Recommended value 125bps : - 250bps : 3 500bps : - 1000bps : -
	D1	wpt_r_diff_wait [1]	1	R/W	
	D2	wpt_r_diff_wait [2]	0	R/W	
	D3	wpt_r_diff_wait [3]	0	R/W	
	D4	wpt_r_diff_old [0]	1	R/W	Assigning data point to calculate ASKOUT pin voltage variation for WPT communication packet demodulation. 0 : Previous data 1 : Data 2 times before 2 : Data 3 times before 3 : Data 4 times before
	D5	wpt_r_diff_old [1]	1	R/W	
	D6	ask_filter [0]	0	R/W	ASK IN filter setting. 0 : 10KHz 1 : 5KHz
	D7	ask_filter [1]	0	R/W	ASK IN sink current setting. 0 : 1uA 1 : Hi-z
0x31	D0	wpt_r_diff_th [0]	1	R/W	Threshold to detect ASKOUT pin voltage variation for WPT communication packet demodulation. 1.465[mV/code] (Converted to ASKIN pin voltage, 11bit resolution) { 000, wpt_r_diff_th[7:0], 0 } Compare with 12bit data of ASKOUT pin voltage variation. Recommended value 125bps : - 250bps : 17 500bps : - 1000bps : -
	D1	wpt_r_diff_th [1]	0	R/W	
	D2	wpt_r_diff_th [2]	0	R/W	
	D3	wpt_r_diff_th [3]	0	R/W	
	D4	wpt_r_diff_th [4]	1	R/W	
	D5	wpt_r_diff_th [5]	0	R/W	
	D6	wpt_r_diff_th [6]	0	R/W	
	D7	wpt_r_diff_th [7]	0	R/W	
0x32	D0	wpt_r_cnt_over_err [0]	0	R/W	Bit count threshold to detect abnormal data for WPT communication packet demodulation. 0 : 4[bit] 1 : 1[bit] 2 : 2[bit] 3 : 8[bit] 4 : 16[bit] 5 : 32[bit] 6 : 48[bit] 7 : 63[bit]
	D1	wpt_r_cnt_over_err [1]	0	R/W	
	D2	wpt_r_cnt_over_err [2]	0	R/W	
	D3	i2c_master_err	0	R	Notification of access error to EEPROM
	D4	pwer_err_set [0]	0	R/W	Error count threshold to detect differential power error between transmitting power and receiving power. 0 : OFF 1 to 15 : Register setting count
	D5	pwer_err_set [1]	0	R/W	
	D6	pwer_err_set [2]	0	R/W	
	D7	pwer_err_set [3]	0	R/W	
0x33	D0	wpt_r_cnt_th [0]	1	R/W	Counter timing to detect data 1 / 0 for WPT communication packet demodulation. Recommended value 125bps : - 250bps : 11 500bps : - 1000bps : -
	D1	wpt_r_cnt_th [1]	1	R/W	
	D2	wpt_r_cnt_th [2]	0	R/W	
	D3	wpt_r_cnt_th [3]	1	R/W	
	D4	wpt_r_cnt_th [4]	0	R/W	
	D5	wpt_r_cnt_th [5]	0	R/W	
	D6	wpt_r_cnt_th [6]	0	R/W	
	D7	wpt_r_cnt_th [7]	0	R/W	
0x34	D0	wpt_r_cnt_th_1cyc [0]	0	R/W	Counter timing to detect data1,0 / no data for WPT communication packet demodulation. Recommended value 125bps : - 250bps : 20 500bps : - 1000bps : -
	D1	wpt_r_cnt_th_1cyc [1]	0	R/W	
	D2	wpt_r_cnt_th_1cyc [2]	1	R/W	
	D3	wpt_r_cnt_th_1cyc [3]	0	R/W	
	D4	wpt_r_cnt_th_1cyc [4]	1	R/W	
	D5	wpt_r_cnt_th_1cyc [5]	0	R/W	
	D6	wpt_r_cnt_th_1cyc [6]	0	R/W	
	D7	wpt_r_cnt_th_1cyc [7]	0	R/W	
0x35	D0	sterr_set [0]	1	R/W	In ATPC Mode, restart caused by non-reception of WPT communication packet is performed for the number of times set by this register. 0 : Unlimited 1 to 15 : The number of times of restart
	D1	sterr_set [1]	1	R/W	
	D2	sterr_set [2]	1	R/W	
	D3	sterr_set [3]	1	R/W	
	D4	rxerr_set [0]	0	R/W	In ATPC Mode, restart caused by WPT communication error is performed for the number of times set by this register. 0 : Unlimited 1 to 15 : The number of times of restart
	D5	rxerr_set [1]	0	R/W	
	D6	rxerr_set [2]	1	R/W	
	D7	rxerr_set [3]	0	R/W	
0x36	D0	err_ocp_set [0]	0	R/W	Detection delay time setting of over current protection for bridge circuit. 0 : Disable detection 1 to 15 : 16[ms] x err_ocp_set[3:0]
	D1	err_ocp_set [1]	0	R/W	
	D2	err_ocp_set [2]	1	R/W	
	D3	err_ocp_set [3]	0	R/W	
	D4	err_th_set [0]	0	R/W	Detection delay time setting of temperature protection 1 and temperature protection 2. 0 : Disable detection 1 to 15 : 16[ms] x err_th_set[3:0]
	D5	err_th_set [1]	0	R/W	
	D6	err_th_set [2]	1	R/W	
	D7	err_th_set [3]	0	R/W	
0x37	D0	err_recover_set [0]	0	R/W	In ATPC Mode, restart caused by protection function (over voltage for bridge circuit, maximum output pulse duty, temperature protection 1, temperature protection 2) is performed for the number of times set by this register. 0 : Unlimited 1 to 14 : The number of times of restart 15 : Setting is not allowed
	D1	err_recover_set [1]	0	R/W	
	D2	err_recover_set [2]	1	R/W	
	D3	err_recover_set [3]	0	R/W	
	D4	wpt_err_set [0]	0	R/W	In ATPC Mode, re-access to receiver device's register by WPT communication is performed for the number of times set by this register when access error is detected.
	D5	wpt_err_set [1]	0	R/W	
	D6	wpt_err_set [2]	1	R/W	
	D7		0	R/W	*1

9.8 Address 0x38 to 0x3F (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x38	D0	writ_err_cnt [0]	0	R	Error count value. In ATPC Mode, the value is counted up when receiver device's register access error in WPT communication is detected.
	D1	writ_err_cnt [1]	0	R	
	D2	writ_err_cnt [2]	0	R	
	D3	writ_err_cnt [3]	0	R	
	D4		0	R	Test register.
	D5		0	R	
	D6		0	R	
	D7		0	R	
0x39	D0	stat_err_cnt [0]	0	R	Error count value. In ATPC Mode, the value is counted up when receiver device's charging state error is detected.
	D1	stat_err_cnt [1]	0	R	
	D2	stat_err_cnt [2]	0	R	
	D3	stat_err_cnt [3]	0	R	
	D4	powe_err_cnt [0]	0	R	Error count value. In ATPC Mode, the value is counted up when over power of transmission power is detected.
	D5	powe_err_cnt [1]	0	R	
	D6	powe_err_cnt [2]	0	R	
	D7	powe_err_cnt [3]	0	R	
0x3A	D0	rxcl_err_cnt [0]	0	R	Error count value. In ATPC Mode, the value is counted up when receiver device's register access error in WPT communication is detected.
	D1	rxcl_err_cnt [1]	0	R	
	D2	rxcl_err_cnt [2]	0	R	
	D3	rxcl_err_cnt [3]	0	R	
	D4	reco_err_cnt [0]	0	R	Restart count value. In ATPC Mode, the value is counted up when over voltage for bridge circuit, maximum output pulse duty, temperature protection 1 and temperature protection 2 is detected and then restart is performed.
	D5	reco_err_cnt [1]	0	R	
	D6	reco_err_cnt [2]	0	R	
	D7	reco_err_cnt [3]	0	R	
0x3B	D0	pslope [0]	0	R/W	Setting parameter for detection threshold of over power of transmission power in ATPC Mode.
	D1	pslope [1]	0	R/W	
	D2	pslope [2]	0	R/W	
	D3	pslope [3]	0	R/W	
	D4	pslope [4]	0	R/W	
	D5	pslope [5]	0	R/W	
	D6	pslope [6]	0	R/W	
	D7	pslope [7]	0	R/W	
0x3C	D0	poffset [0]	0	R/W	Setting parameter for detection threshold of over power of transmission power in ATPC Mode.
	D1	poffset [1]	0	R/W	
	D2	poffset [2]	0	R/W	
	D3	poffset [3]	0	R/W	
	D4	poffset [4]	0	R/W	
	D5	poffset [5]	0	R/W	
	D6	poffset [6]	0	R/W	
	D7	poffset [7]	0	R/W	
0x3D	D0		0	R/W	Test register. Write access is NOT allowed.
	D1		0	R/W	
	D2		0	R/W	
	D3		0	R/W	
	D4		0	R/W	
	D5		0	R/W	
	D6		0	R/W	
	D7		0	R/W	
0x3E	D0	slope_fix_duty [0]	0	R/W	Setting parameter for detection threshold of over power of transmission power in ATPC Mode.
	D1	slope_fix_duty [1]	0	R/W	
	D2	slope_fix_duty [2]	0	R/W	
	D3	slope_fix_duty [3]	0	R/W	
	D4	slope_fix_duty [4]	0	R/W	
	D5	slope_fix_duty [5]	0	R/W	
	D6	slope_fix_duty [6]	0	R/W	
	D7	slope_fix_duty [7]	0	R/W	
0x3F	D0	rcs_sel [0]	0	R/W	R_{CS} value setting for input current detection of bridge circuit. 0 : 0.25Ω 1 : 0.5Ω 2 : 1Ω 3 : 2Ω
	D1	rcs_sel [1]	0	R/W	
	D2	power_mask_ctrlerr	0	R/W	1 : Detection of over power of transmission power is not executed in control error non-convergence condition.
	D3	pod_en	0	R/W	Enable detection function of over power of transmission power in ATPC Mode. 0 : Disable 1 : Enable
	D4		0	R/W	*1
	D5	rx_end_power [0]	0	R	Notification of request to stop transmitting power from receiver device(RAA457100). rx_end_power[0]=1 : No convergence in control error rx_end_power[1]=1 : Maximum junction temperature detection (rx_end_power[2]=1 : Not assigned.)
	D6	rx_end_power [1]	0	R	
	D7	rx_end_power [2]	0	R	

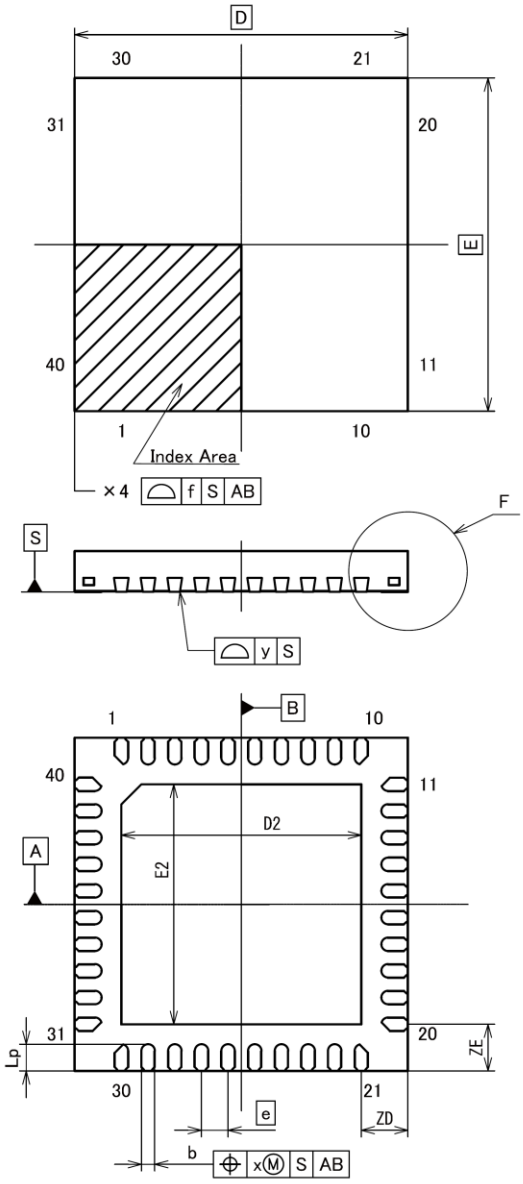
9.9 Address 0x40 to 0x47 (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

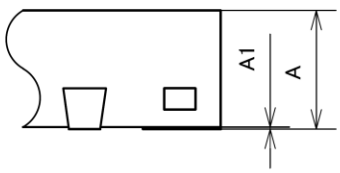
Address	Bit No.	Register Name	Init	R/W	Description
0x40	D0	rx_identif_data [0]	0	R	Message1 of WPT communication reception packet (Header 0x01) in ATPC Mode.
	D1	rx_identif_data [1]	0	R	
	D2	rx_identif_data [2]	0	R	
	D3	rx_identif_data [3]	0	R	
	D4	rx_identif_data [4]	0	R	
	D5	rx_identif_data [5]	0	R	
	D6	rx_identif_data [6]	0	R	
	D7	rx_identif_data [7]	0	R	
0x41	D0	rx_setting_data [0]	0	R	Message2 of WPT communication reception packet (Header 0x01) in ATPC Mode.
	D1	rx_setting_data [1]	0	R	
	D2	rx_setting_data [2]	0	R	
	D3	rx_setting_data [3]	0	R	
	D4	rx_setting_data [4]	0	R	
	D5	rx_setting_data [5]	0	R	
	D6	rx_setting_data [6]	0	R	
	D7	rx_setting_data [7]	0	R	
0x42	D0	rx_status [0]	1	R	Message2 of WPT communication reception packet (Header 0x03) in ATPC Mode.
	D1	rx_status [1]	1	R	
	D2	rx_status [2]	1	R	
	D3	rx_status [3]	1	R	
	D4	rx_status [4]	1	R	
	D5	rx_status [5]	1	R	
	D6	rx_status [6]	1	R	
	D7	rx_status [7]	1	R	
0x43	D0	rx_power [0]	0	R	Message2 of WPT communication reception packet (Header 0x04) in ATPC Mode.
	D1	rx_power [1]	0	R	
	D2	rx_power [2]	0	R	
	D3	rx_power [3]	0	R	
	D4	rx_power [4]	0	R	
	D5	rx_power [5]	0	R	
	D6	rx_power [6]	0	R	
	D7	rx_power [7]	0	R	
0x44	D0	wpt_read_data [0]	0	R	Message2 of WPT communication reception packet (Header 0x02) in ATPC Mode.
	D1	wpt_read_data [1]	0	R	
	D2	wpt_read_data [2]	0	R	
	D3	wpt_read_data [3]	0	R	
	D4	wpt_read_data [4]	0	R	
	D5	wpt_read_data [5]	0	R	
	D6	wpt_read_data [6]	0	R	
	D7	wpt_read_data [7]	0	R	
0x45	D0	receive_header_data [0]	0	R	Header of WPT communication reception packet. This register is overwritten by receiving next packet.
	D1	receive_header_data [1]	0	R	
	D2	receive_header_data [2]	0	R	
	D3	receive_header_data [3]	0	R	
	D4	receive_header_data [4]	0	R	
	D5	receive_header_data [5]	0	R	
	D6	receive_header_data [6]	0	R	
	D7	receive_header_data [7]	0	R	
0x46	D0	receive_message1_data [0]	0	R	Message1 of WPT communication reception packet. This register is overwritten by receiving next packet.
	D1	receive_message1_data [1]	0	R	
	D2	receive_message1_data [2]	0	R	
	D3	receive_message1_data [3]	0	R	
	D4	receive_message1_data [4]	0	R	
	D5	receive_message1_data [5]	0	R	
	D6	receive_message1_data [6]	0	R	
	D7	receive_message1_data [7]	0	R	
0x47	D0	receive_message2_data [0]	0	R	Message2 of WPT communication reception packet. This register is overwritten by receiving next packet.
	D1	receive_message2_data [1]	0	R	
	D2	receive_message2_data [2]	0	R	
	D3	receive_message2_data [3]	0	R	
	D4	receive_message2_data [4]	0	R	
	D5	receive_message2_data [5]	0	R	
	D6	receive_message2_data [6]	0	R	
	D7	receive_message2_data [7]	0	R	

9.10 Address 0x48 to 0x60 (*1 Test Register : The same value as initial value (init) should be written here at write access to this address.)

Address	Bit No.	Register Name	Init	R/W	Description
0x48	D0	send_header_data [0]	0	R/W	Header of WPT communication transmission packet.
	D1	send_header_data [1]	0	R/W	
	D2	send_header_data [2]	0	R/W	
	D3	send_header_data [3]	0	R/W	
	D4	send_header_data [4]	0	R/W	
	D5	send_header_data [5]	0	R/W	
	D6	send_header_data [6]	0	R/W	
	D7	send_header_data [7]	0	R/W	
0x49	D0	send_message1_data [0]	0	R/W	Message1 of WPT communication transmission packet.
	D1	send_message1_data [1]	0	R/W	
	D2	send_message1_data [2]	0	R/W	
	D3	send_message1_data [3]	0	R/W	
	D4	send_message1_data [4]	0	R/W	
	D5	send_message1_data [5]	0	R/W	
	D6	send_message1_data [6]	0	R/W	
	D7	send_message1_data [7]	0	R/W	
0x4A	D0	send_message2_data [0]	0	R/W	Message2 of WPT communication transmission packet.
	D1	send_message2_data [1]	0	R/W	
	D2	send_message2_data [2]	0	R/W	
	D3	send_message2_data [3]	0	R/W	
	D4	send_message2_data [4]	0	R/W	
	D5	send_message2_data [5]	0	R/W	
	D6	send_message2_data [6]	0	R/W	
	D7	send_message2_data [7]	0	R/W	
0x4B	D0	sterr [0]	0	R	Error count value. In ATPC Mode, the value is counted up when WPT communication packet is not received.
	D1	sterr [1]	0	R	
	D2	sterr [2]	0	R	
	D3	sterr [3]	0	R	
	D4	rxerr [0]	0	R	Error count value. In ATPC Mode, the value is counted up when WPT communication error is detected.
	D5	rxerr [1]	0	R	
	D6	rxerr [2]	0	R	
	D7	rxerr [3]	0	R	
0x4C to 0x60	Test register. Write access is NOT allowed.				

10. Package Dimensions





Detail F

Referrence Symbol	Dimension in Milimeters		
	Min	Nom	Max
D	—	5.00	—
E	—	5.00	—
A	—	—	0.65
A1	0.00	—	—
b	0.15	0.20	0.25
e	—	0.40	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.08
f	—	—	0.10
ZD	—	0.70	—
ZE	—	0.70	—
D2	—	3.60	—
E2	—	3.60	—

REVISION HISTORY	RAA458100GNP Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb.28.2017	-	First Edition issued
1.01	Sep.03.2018	7	LED1, LED2 flashing pattern of battery charge complete state in Table 8.5.1

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