RAA489400

USB Type-C® Port Controller

The RAA489400 is a USB Type-C® Port controller that is based on the Universal Serial Bus Type-C Port Controller Interface Specification, USB Type-C Cable and Connector Specification, and USB Power Delivery Specification.

A Single USB Type-C Port Manager combines with multiple RAA489400 devices to implement all USB PD functions (such as power negotiation and Alternate Mode support) for multiple USB Type-C ports.

The RAA489400 supports a 60V Absolute Maximum Rating for both a VBUS voltage monitor (with relevant pin functions) and a CC1/CC2 allowing for a system that can provide an Extended Power Range operation up to 240W/48V.

Features

- USB Type-C Port Controller (TCPC) with integrated TCPC PHY, CC-Logic
  - Supports Type-C Port Controller Interface (TCPCi) Revision 2.0 with Extended Power Range (EPR)
  - Supports USB Power Delivery (USB PD) Revision 3.1 (Certified Silicon TID: 10147)
  - Supports Universal Serial Bus (USB) Type-C Release 2.1
  - CC1/CC2 absolute maximum rating (Abs Max): 60V
  - Dead battery Rd support
  - SMBus/I^2C slave target with ALERT# for USB Type-C Port Manager (TCPM)
- Integrated VCONN MUX
  - RDS(on): 500mΩ for 5V VCONN power
  - VCONN OCP/OVP/UVP/OTP/RVP protection
  - Overcurrent threshold: 600mA (default), 400mA (option) and 800mA (option)
- 48V tolerance for VBUS based on USB PD Revision 3.1 EPR
  - Recommended operating condition: 55V (maximum)
  - Abs Max Rating: 60V
  - VBUS discharge
  - VBUS OCP/OVP/UVP/RVP protection
  - VBUS-CC short-circuit protection
- VBUS source power path gate driver with external NFET
- VBUS sink power path gate driver with external NFET
- OCP# fault signal output
- Sink Fast Role Swap (FRS) support
- 4-ch GPIO (such as VBUS Source gate enable control, VBUS sink gate enable control with VBUS power switch, overcurrent input from external power switch)
- PROCHOT# output to notify VBUS source adapter disconnection and FRS Event
- Internal sink path discharge
- Integrated 3.3V LDO for TCPM power supply in dead battery case
- ADC for VBUS voltage and current measurement
- VSYS33 (main power): Typical 3.3V
- 32pin FCQFN, 3.0×5.0mm

Applications

- General purpose application with high power up to 240W
  - Battery powered mobile devices
  - Electric bikes, robots, and drones
  - Power tools, battery packs
  - Home appliances such as vacuum cleaners
  - Notebooks, tables, power banks, and desktop PCs

Contents

1. Overview

1.1 Block Diagram

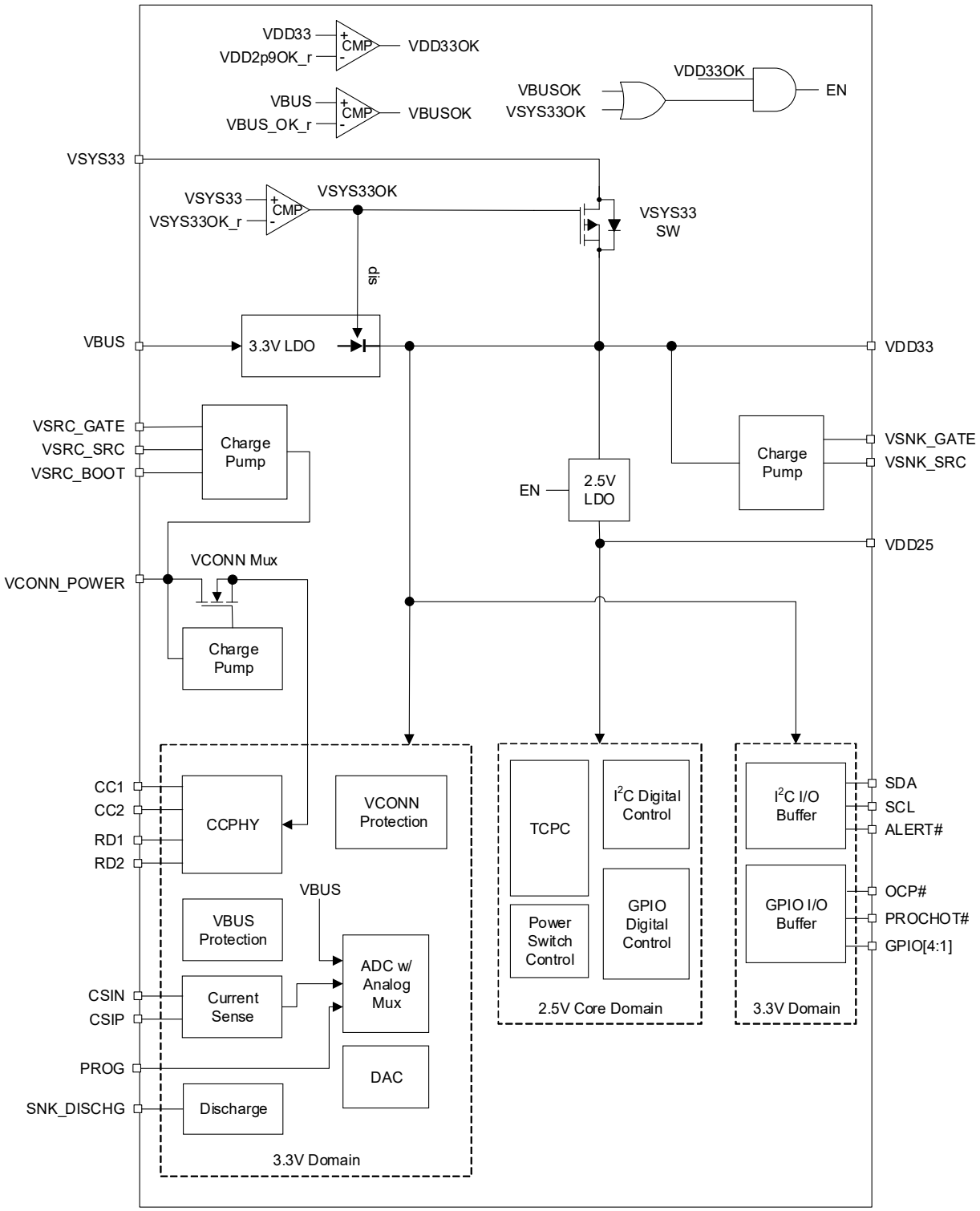


Figure 1. Block Diagram

1.2 Typical Application

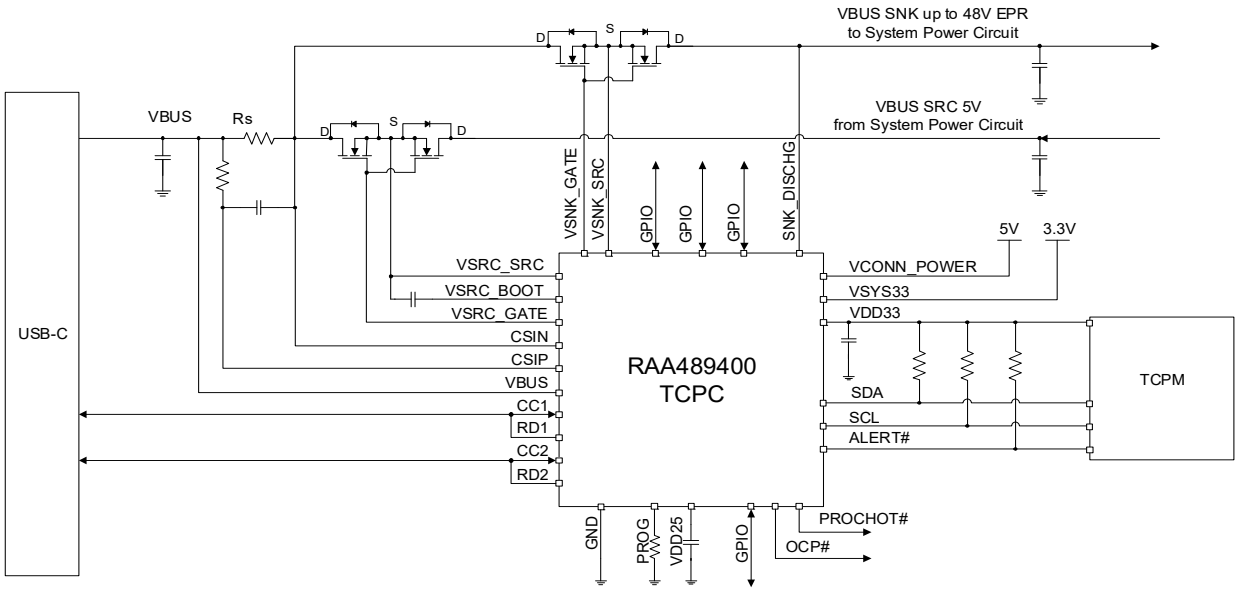


Figure 2. Typical USB-C Application Based on TCPC and TCPM for DRP (Dual Role Power) System, Supports VBUS SNK: Up to 48V and SRC: Up to 5V

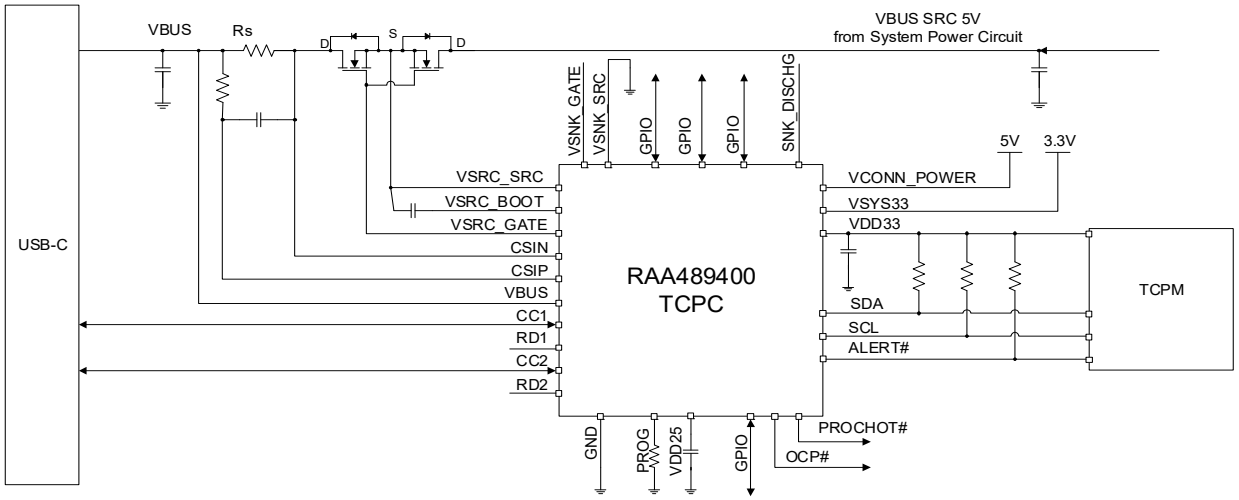


Figure 3. Typical USB-C Application Based on TCPC and TCPM for Source Only System, Supports VBUS SRC: Up to 5V

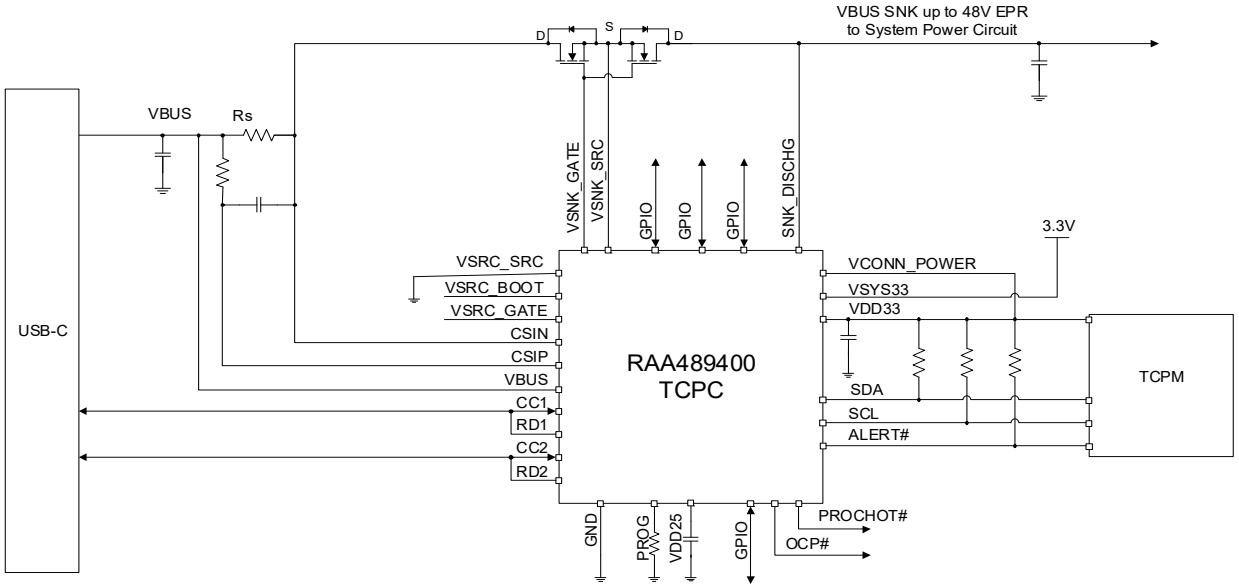


Figure 4. Typical USB-C Application Based on TCPC and TCPM for Sink Only System, Supports VBUS SNK: Up to 48V

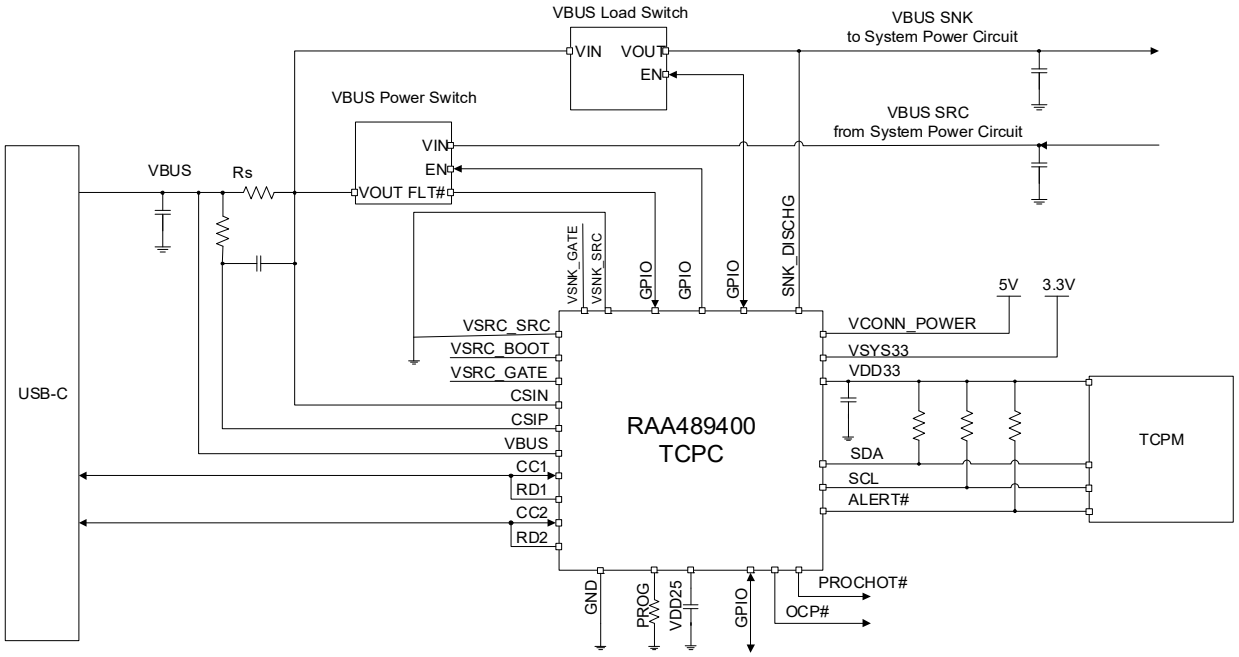


Figure 5. Typical USB-C Application Based on TCPC and TCPM for DRP System with GPIO Control

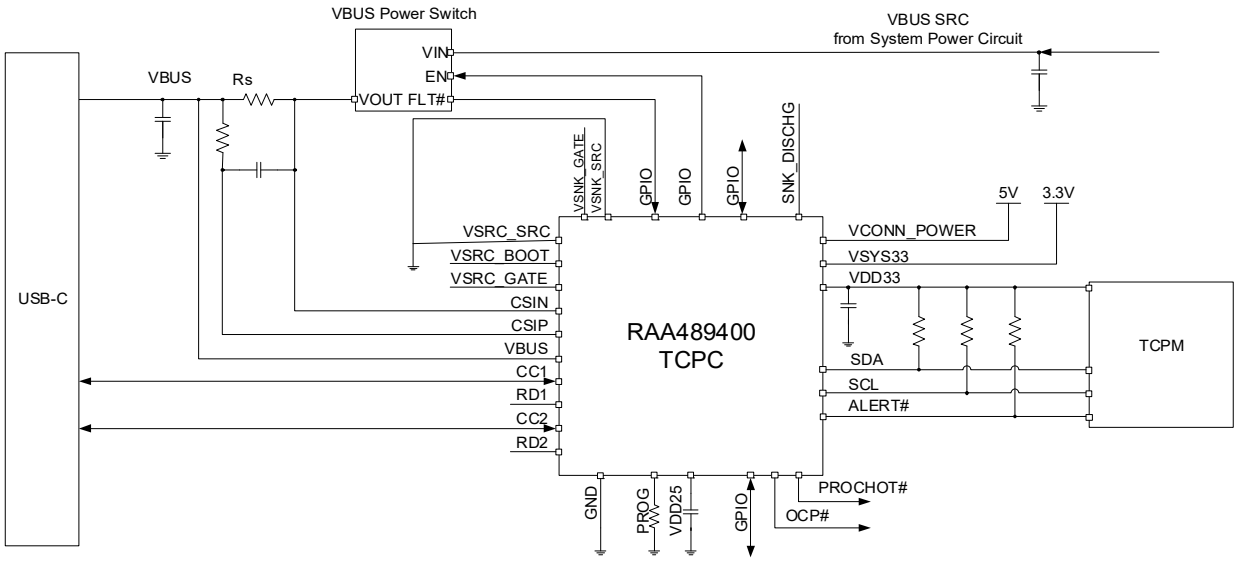


Figure 6. Typical USB-C Application based on TCPC and TCPM for Source Only System with GPIO Control

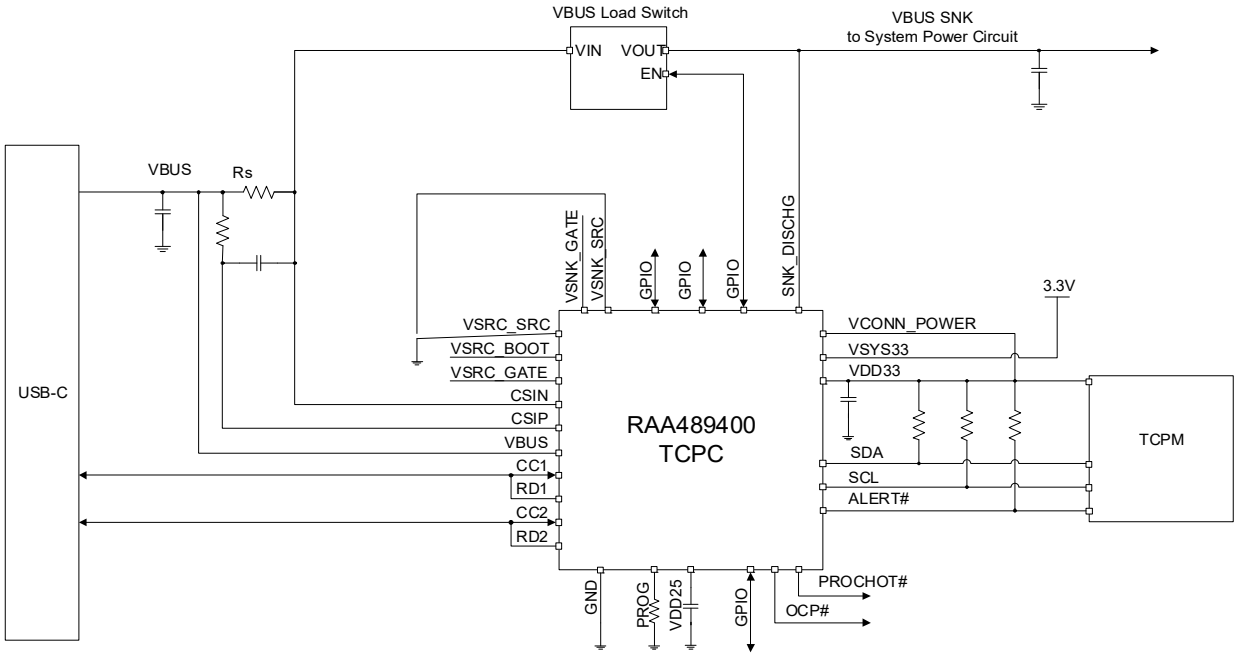


Figure 7. Typical USB-C Application Based on TCPC and TCPM for Sink Only System with GPIO Control

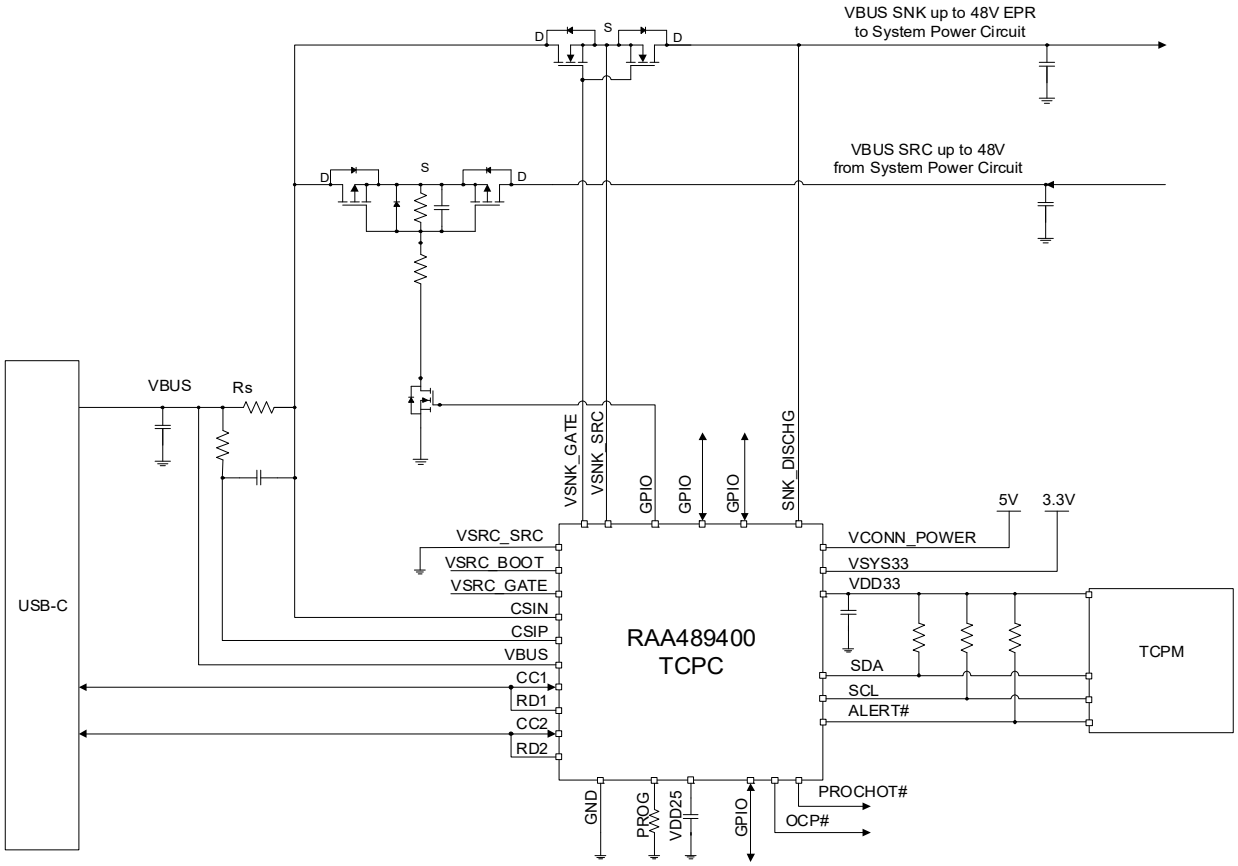


Figure 8. Example of USB-C Application Based on TCPC and TCPM for DRP (Dual Role Power) System with VSNK_GATE and GPIO Control, Supports VBUS SNK: Up to 48V and SRC: Up to 48V

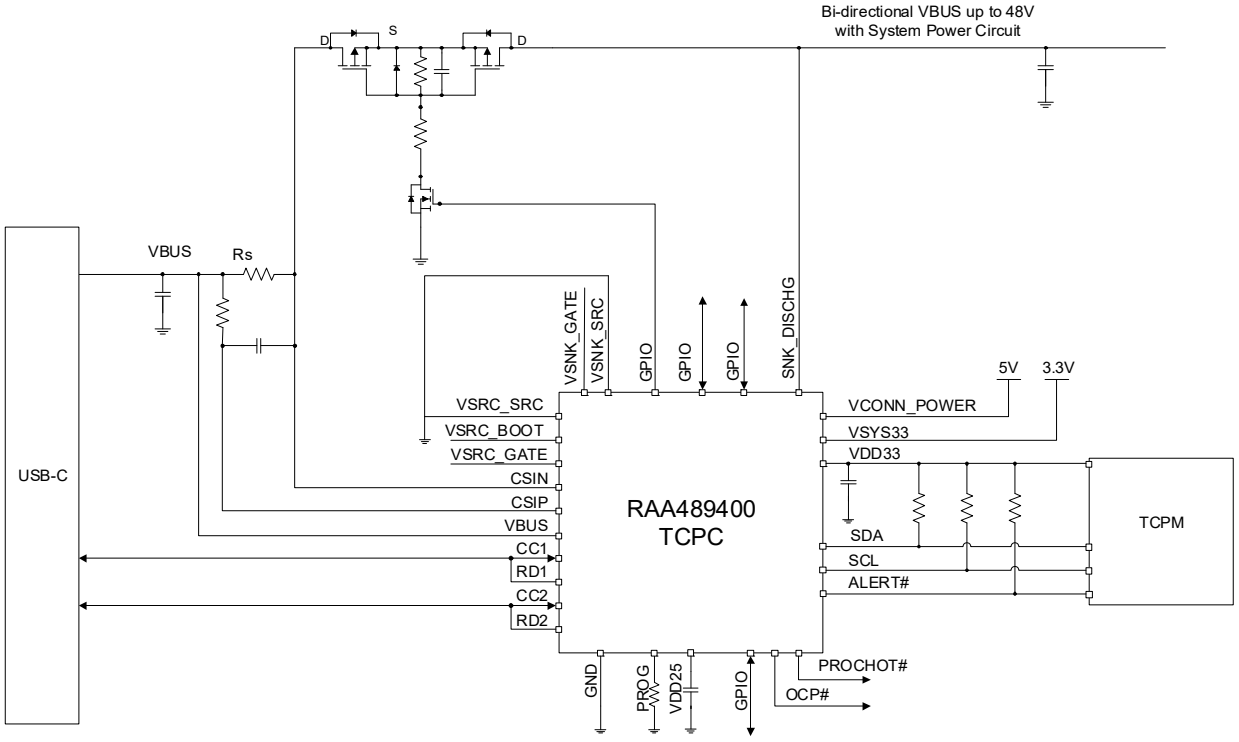


Figure 9. Example of USB-C Application Based on TCPC and TCPM for Bi-directional DRP (Dual Role Power) System with GPIO Control, Supports VBUS SNK: Up to 48V and SRC: Up to 48V

2. Pin Information

2.1 Pin Assignments

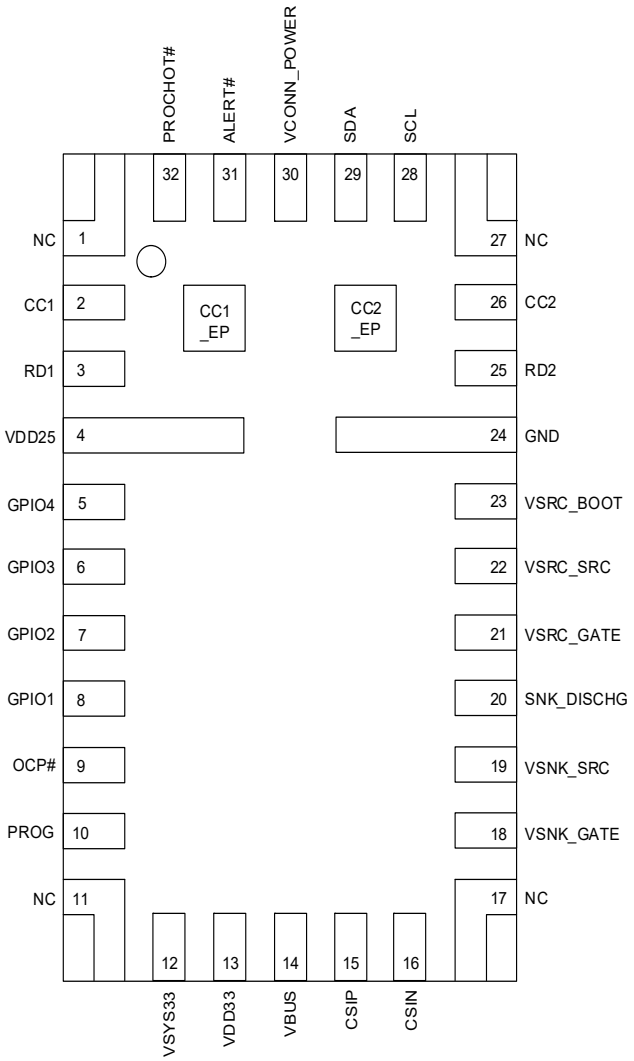


Figure 10. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	NC	No connection
2	CC1	Configuration Channel 1, Analog pin from CC-PHY.
3	RD1	Dead battery Rd, Analog pin from CC-PHY. Tie to CC1 when dead battery Rd is supported.
4	VDD25	2.5V LDO output provides the bias power for internal digital logic and the TCPC transmitter. Connect a ceramic capacitor to GND. The effective capacitance of VDD25 capacitor should be at least 1µF at 2.5V. This pin cannot source current to external circuits.

5	GPIO4	General purpose input and output with a 3.3V push-pull output, 1.8V or 3.3V open-drain output, 1.8V or 3.3V input, or disable. It can be used as a VBUS source or a sink switch control and overcurrent input. ▪ VBUS source power switch enable ▪ VBUS sink power switch enable ▪ Overcurrent Input (from external VBUS source power switch) ▪ General Purpose Input ▪ General Purpose Output (push-pull) ▪ General Purpose Output (open-drain) GPIO1_CTRL Register, GPIO2_CTRL Register, GPIO3_CTRL Register, GPIO4_CTRL Register, VBUS_PATH_CTRL Register, VBUS_GPIO_CTRL Register, and GPIO_OC_EN Register control those configurations.
6	GPIO3	
7	GPIO2	
8	GPIO1	
9	OCP#	Open-drain output with 1.8V or 3.3V pull-up. Active low when a fault condition configured in OCP_OUTPUT_CTRL Register (A8h) is detected. When all fault conditions are removed, OCP# pin is deasserted to high.
10	PROG	A resistor from the PROG pin to GND to set the SMBus/I^2C slave target address.
11	NC	No connection
12	VSYS33	Main power input (minimum 3.0V, typical 3.3V). Connect a ceramic capacitor to GND. Recommended capacitance: 4.7µF.
13	VDD33	3.3V LDO output provides the bias power for the internal analog and digital circuit. It also supplies power for the external TCPM. Connect a ceramic capacitor to GND. The effective capacitance of VDD33 capacitor should be at least 1µF at 3.3V. Do not apply additional load on the VDD33 pin other than TCPM and a pull-up resistor for SDA/SCL/ALERT# between RAA489400 and TCPM. *Note:* If two or more RAA489400 VDD33 supplies 3.3V to TCPM, a diode is required for each VDD33 pin.
14	VBUS	VBUS voltage sense and discharge input. Input for internal LDO power on dead battery mode (VSYS33 = 0V).
15	CSIP	Connect to the VBUS source current-sense resistor positive input through a resistor. Place a ceramic capacitor between CSIP and CSIN to provide differential-mode filtering. The current sense resistor value must be 10mΩ.
16	CSIN	Input for sensing VBUS voltage. Connect to the VBUS source current-sense resistor negative input. Use a Kelvin line between the voltage sense point and CSIN.
17	NC	No connection
18	VSNK_GATE	Gate drive output of N-channel MOSFET USB-C/PD VBUS sink path FET.
19	VSNK_SRC	N-channel MOSFET source input reference for USB-C/PD VBUS sink path FET(s).
20	SNK_DISCHG	Internal system sink path discharge between the VBUS sink path gate and system load (such as battery charger adapter side).
21	VSRC_GATE	Gate drive output of N-channel MOSFET USB-C/PD Source FET, pumped 5V above VSRC_SRC.
22	VSRC_SRC	N-channel MOSFET source input reference for USB-C/PD VBUS Source path FET(s).
23	VSRC_BOOT	Connect external capacitor for charge pump of VSRC_GATE. Recommended capacitance: 0.047µF.
24	GND	Ground
25	RD2	Dead battery Rd, Analog pin from CC-PHY. Tie to CC2 when dead battery Rd is supported.
26	CC2	Configuration Channel 2, Analog pin from CC-PHY.

27	N.C.	No connection
28	SCL	SMBus/I^{2}C clock I/O. Connect to the clock line from TCPM for TCPC control.
29	SDA	SMBus/I^{2}C data I/O. Connect to the data line from TCPM for TCPC control.
30	VCONN_POWER	5V Input to the VCONN MUX providing power to the CC1/CC2 and the VSRC_GATE driver. Connect a ceramic capacitor to GND. The VCONN_POWER capacitor should be at least 4.7µF.
31	ALERT#	Interrupt line for SDA and SCL.
32	PROCHOT#	Open-drain output with 1.8V or 3.3V pull-up. Active low when either VBUS source device disconnection or Sink Fast Role Swap is detected. The assertion condition configured in PROCHOT_EN Register (AAh) is detected. When the condition is removed, the PROCHOT# pin is deasseted to high.
CC1-EP	CC1	Exposed pad for CC1.
CC2-EP	CC2	Exposed pad for CC2.

2.3 Unused Pin Termination

Pin Number	Pin Name	Connection Method
1, 11, 17, 27	NC	Open
3	RD1	Open
5	GPIO4	Open
6	GPIO3	
7	GPIO2	
8	GPIO1	
9	OCP#	Open
12	VSYS33	Connect to GND if VSYS33 is not used for start-up.
18	VSNK_GATE	Open
19	VSNK_SRC	Connect to GND through a 0Ω resistor.
21	VSRC_GATE	Open
22	VSRC_SRC	Connect to GND through a 0Ω resistor.
23	VSRC_BOOT	Open
25	RD2	Open
30	VCONN_POWER	Connect to VDD33 if VCONN function is not used.
32	PROCHOT#	Open

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
CC1, CC2, RD1, RD2, CSIN, CSIP, VBUS, SNK_DISCHG	-0.3	+60	V
CSIP-CSIN	-0.5	+0.5	V
VSNK_SRC	-0.3	+60	V
VSNK_GATE	-0.3	+66.5	V
	VSNK_SRC - 0.3	VSNK_SRC + 6.5	V
VSRC_SRC	-0.3	+6.5	V
VSRC_BOOT	-0.3	+13	V
	VSRC_SRC - 0.3	VSRC_SRC + 6.5	V
VSRC_GATE	-0.3	+13.3	V
	VSRC_SRC - 0.3	VSRC_BOOT + 0.3	V
GPIO1, GPIO2, GPIO3, GPIO4	-0.3	+6.5	V
OCP#, PROCHOT#, ALERT#	-0.3	+6.5	V
PROG	-0.3	+6.5	V
VSYS33, VDD33	-0.3	+6.5	V
VDD25	-0.3	+3	V
VCONN_POWER	-0.3	+6.5	V
SDA, SCL	-0.3	+6.5	V
GPIO1, GPIO2, GPIO3, GPIO4, SDA, SCL, OCP#, PROCHOT#, ALERT#	-	4	mA
Maximum Junction Temperature	-40	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-1.5	1.5	kV
Charged Device Model (Tested per JS-002-2022)	-0.75	0.75	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VSYS33, VDD33	-0.3	+3.6	V
VCONN_POWER	-0.3	+5.5	V
CSIN, CSIP, VBUS, SNK_DISCHG	-0.3	+55	V
VSNK_SRC	-0.3	+55	V
VSNK_GATE	-0.3	+60.5	V
	VSNK_SRC - 0.3	VSNK_SRC + 5.5	V
VSRC_SRC	-0.3	+5.5	V
VSRC_BOOT	-0.3	+11	V
	VSRC_SRC - 0.3	VSRC_SRC + 5.5	V
VSRC_GATE	-0.3	+11.3	V
	VSRC_SRC - 0.3	VSRC_BOOT + 0.3	V
CC1, CC2, RD1, RD2	-0.3	+5.5	V
SDA, SCL, ALERT#, OCP#, PROCHOT#	-0.3	+5.5	V
GPIO1, GPIO2, GPIO3, GPIO4	-0.3	+3.6	V
Ambient Temperature			
Part number: RAA489400ARGNP#HA0 RAA489400ARGNP#MA0	-10	+100	°C
Part number: RAA489400A3GNP#HA0 RAA489400A3GNP#MA0	-40	+105	°C
Junction Temperature	-10	+125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	32 Ld FCQFN Package	θ_{JA}[1]	Junction to ambient	40	°C/W
		θ_{JC}[2]	Junction to case	6	°C/W

1. θ_{JA} is measured on JEDEC std. PCB with Direct Attach features including two 100µm dia. vias under pin #4, and two 100µm dia. vias under pin #24. See TB379.
2. For θ_{JC}, the case temperature is measured on the package bottom surface at pins #4 and #24.

3.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. VSYS33 = 3.3V, VCONN_POWER = 5.0V, and T_A = -40°C to +105°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UVLO/ACOK						
VBUS OK Rising	VBUS_OK_r	-	3.6	3.81	3.95	V

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VBUS OK Hysteresis	VBUS_OK_h	-	-	300	-	mV
VSYS33 OK Rising	VSYS33OK_r	-	2.8	2.9	3	V
VSYS33 OK Falling	VSYS33OK_f	-	2.6	2.68	2.8	V
VDD25 2P4 POR Rising	VDD2p5_2P4_r	SMBus	-	2.3	-	V
VDD25 2P4 POR Hysteresis	VDD2p5_2P4_h	-	-	125	-	mV
VDD33 OK Rising	VDD2p9OK_r	-	2.65	2.857	3.06	V
VDD33 OK Hysteresis	VDD2p9OK_h	-	-	100	-	mV
Linear Regulator						
VDD25 Output Voltage	VDD2P5	3.0V < VDD33 < 3.6V, no load	2.45	2.55	2.7	V
VDD25 Dropout Voltage	VDD2P5_dp	10mA, VDD33 = 2.5V	44	66	88	mV
VDD25 Overvoltage Rising	VDD2P5_OV_r	-	-	3.3	-	V
VDD25 Overvoltage Hysteresis		-	-	200	-	mV
VDD33 Output Voltage	VDD3P3	3.8V < VBUS < 51V, no load	3.1	3.3	3.5	V
VDD33 Dropout Voltage	VDD3P3_dp	30mA, VBUS > 3.8V	-	25	-	mV
VDD33 Overcurrent Threshold	VDD3P3_OC	-	25	40	55	mA
Input Current Sense Amplifier, Rs = 10mΩ						
CSIP/CSIN Input Voltage Range	VCSIP/N	-	4	-	55	V
Fast Role Swap						
VBUS Top Window Comparator Falling Threshold	vFrsVbus	Setting 1 (5.2V)	4.9	5.1	5.3	V
		Setting 2 (5.5V)	5.25	5.4	5.55	V
		Setting 3 (5.8V)	5.5	5.7	5.9	V
VBUS Top Window Comparator Hysteresis	-	-	-	0.36	-	V
Protection						
Over-Temperature Threshold	tVconn_ot	-	-	155	-	°C
VBUS Overvoltage Rising Threshold (SPR)	vSprMax	-	23	23.41	24	V
VBUS Overvoltage Hysteresis (SPR)	vVbusOvHysSpr	-	-	260	-	mV
VBUS Overvoltage Rising Threshold (EPR)	vEprMax	-	52.6	54.0	56.2	V
VBUS Overvoltage Hysteresis (EPR)	vVbusOvHysEpr	-	-	550	-	mV
SRC VBUS Undervoltage Falling Threshold	vVbusUv	-	3.45	3.76	4.25	V
SRC VBUS Undervoltage Hysteresis	-	-	-	360	-	mV
SRC 5V VBUS Overvoltage Rising Threshold	vVbusOv	-	5.8	6.3	6.6	mV
SRC 5V VBUS Overvoltage Hysteresis	-	-	-	600	-	mV
SRC VBUS Reverse Voltage Rising Threshold	vVbusRv	$V_{VBUS} - V_{CSIN}$	20	-	100	mV
SRC VBUS Reverse Voltage Hysteresis	-	-	-	2	-	mV

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VBUS Overcurrent Rising Threshold	iVbusOc	Setting 1 (1.5A)	1.65	-	1.88	A
		Setting 2 (3A)	3.3	-	3.6	A
		Setting 3 (4A)	4.4	-	4.8	A
		Setting 4 (5A)	5.5	-	6.0	A
VBUS Overcurrent Hysteresis	iVbusOcHys	-	-	400	-	mA
VCONN Overvoltage Rising Threshold	vVconnOv	-	5.8	6.26	6.6	V
VCONN Overvoltage Hysteresis	vVconnOvHys	-	-	500	-	mV
VCONN Undervoltage Falling Threshold	vVconnUv	-	3.45	3.79	4.25	V
VCONN Undervoltage Hysteresis	vVconnUvHys	-	170	210	320	mV
VCONN Reverse Voltage Rising Threshold	vVconnRv	$V_{CC1/CC2}$ – VCONN	250	325	500	mV
VCONN Reverse Voltage Hysteresis	vVconnRvHys	-	-	100	-	mV
VCONN Overcurrent Rising Threshold	iVconnOc	Setting 1 (400mA)	400	-	600	mA
		Setting 2 (600mA)	600	-	800	mA
		Setting 3 (800mA)	800	-	1050	mA
VCONN OC Blanking Time[2]	tVconnOcBlnk	-	-	5	-	ms
Oscillator						
24MHz Oscillator Frequency, Digital Core Only	-	-	-	24	-	MHz
3MHz Oscillator Frequency	-	-	-	3	-	MHz
Digital Debounce Time Accuracy[2]	-	-	-15	-	15	%
30kHz Oscillator Frequency	-	-	-	30	-	kHz
Charge Pump Gate Drivers						
VBUS Source Gate Vgs	-	VSRC_GATE - VSRC_SRC	4.2	4.4	4.6	V
VBUS Sink Gate Vgs	-	VSNK_GATE - VSNK_SRC	4.5	5.1	5.5	V
Charge Pump Startup Time	tCpStart[2]	-	-	-	50	ms
VBUS						
VBUS ADC Accuracy	VBUS > 2.8V	VBUS Voltage	-2	-	+2	%
	2.0V ≤ VBUS ≤ 2.8V	VBUS Voltage	-50	-	+50	mV
	VBUS < 2.0V	VBUS Voltage	-75	-	+75	mV
	VBUS > 600mA	VBUS Current	-5	-	+5	%
	VBUS = 500mA	VBUS Current	-	498	-	mA
	VBUS = 200mA	VBUS Current	-	197	-	mA
	VBUS = 100mA	VBUS Current	-	104	-	mA
SNK VBUS Disconnect Detect DAC Accuracy	-	11-bit DAC, LSB = 25mV, VBUS Voltage > 0.5V	-5	-	+5	%

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
VCONN Mux						
VCONN Switch Rdson	-	-	-	500	-	mΩ
VCONN Switch Turn on Time[2]	-	Time from enable to fully on, with 10µF cap	-	-	1.5	ms
VCONN Discharge Stop Voltage	vVconnDischarge	-	-	-	0.8	V
VCONN Discharge Time[2]	tVconnZero	-	-	-	100	ms
CCx Discharge						
VCONN Mux Discharge Rdson	Rdch	-	-	100	-	Ω
Cable Settings						
Rd Clamp	-	-	0.8	1.1	1.3	V
Rd Resistor	-	-	4.59	5.1	5.61	kΩ
IP Current	-	Default USB Power	64	80	96	µA
	-	1.5A at 5V	166	180	194	µA
	-	3A at 5V	304	330	356	µA
TX						
Bit Rate	fBitRate	-	270	300	330	Kps
Fall Time	tFall	10% and 90% amplitude points, minimum is under an unload condition	300	-	-	ns
Rise Time	tRise	10% and 90% amplitude points, minimum is under an unload condition	300	-	-	ns
Voltage Swing	vSwing	Applies to both no load condition and under the load condition specified in USB-PD Spec	1.05	-	1.2	V
Output Impedance	zDrive	Source output impedance at the Nyquistfrequency of [USB 2.0] low speed (750kHz) while the source is driving the CC line.	33	-	75	Ω
SMBus/I^{2}C, GPIO						
SDA/SCL, GPIO1/2/3/4 Input Low Voltage	VIL	-	-	-	0.5	V
SDA/SCL, GPIO1/2/3/4 Input High Voltage	VIH	-	1.2	-	-	V
SDA/SCL, GPIO1/2/3/4 Input Bias Current	-	-	-	-	1	µA
SDA Output Sink Current	IOL_SDA	VSDA = 0.4V, on	11	-	-	mA
SMBus/I^{2}C Frequency	fSMB	-	10	-	1000	kHz
ALERT#, OCP#, PROCHOT#, GPIO1/2/3/4 Input Leakage Current	-	-	-	-	1	µA
ALERT#, OCP#, PROCHOT#, GPIO1/2/3/4 Output Sink Current	IOL GPIO	Voltage = 0.4V	4	-	-	mA
GPIO1/2/3/4 Output Source Current	IOH_GPIO	-	4	-	-	mA

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
ALERT#, OCP#, PROCHOT#, GPIO1/2/3/4 Output Low Voltage	VOL	-	-	-	0.4	V
GPIO1/2/3/4 Output High Voltage	VOH	-	2.4	-	-	V

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Limits established by characterization are not production tested.

3.5 SMBus Timing Specification

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Bus Free Time[2]	t_{BUF}	-	0.5	-	-	µs
Start Condition Hold Time from SCL[2]	$t_{HD:STA}$	-	0.26	-	-	µs
Start Condition Set-Up Time from SCL[2]	$t_{SU:STA}$	-	0.26	-	-	µs
Stop Condition Set-Up Time from SCL[2]	$t_{SU:STO}$	-	0.26	-	-	µs
SDA Hold Time from SCL[2]	$t_{HD:DAT}$	-	0	-	-	ns
SDA Set-Up Time from SCL[2]	$t_{SU:DAT}$	-	50	-	-	ns
SCL Low Period[2]	t_{LOW}	-	0.5	-	-	µs
SCL High Period[2]	t_{HIGH}	-	0.26	-	50	µs

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Limits established by characterization are not production tested.

4. Typical Performance Graphs

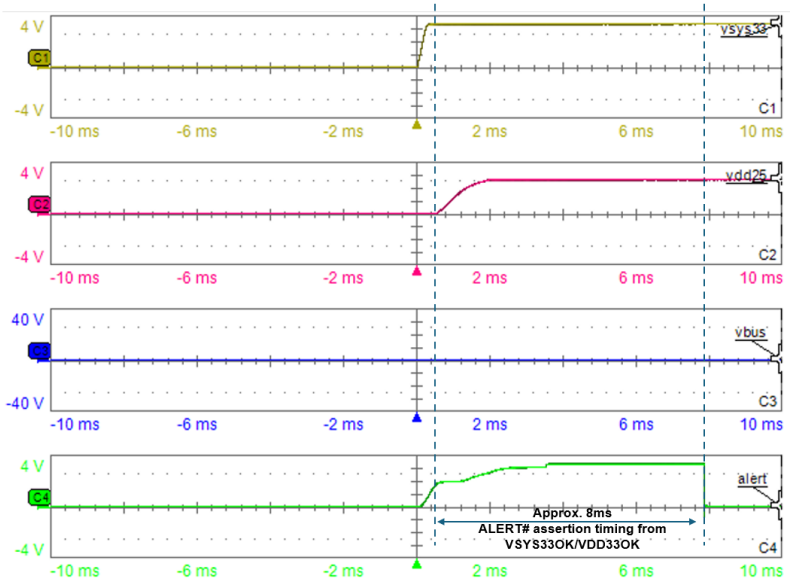


Figure 11. Startup VSYS33 Powered (2.0ms/Div, 2.0V/Div)

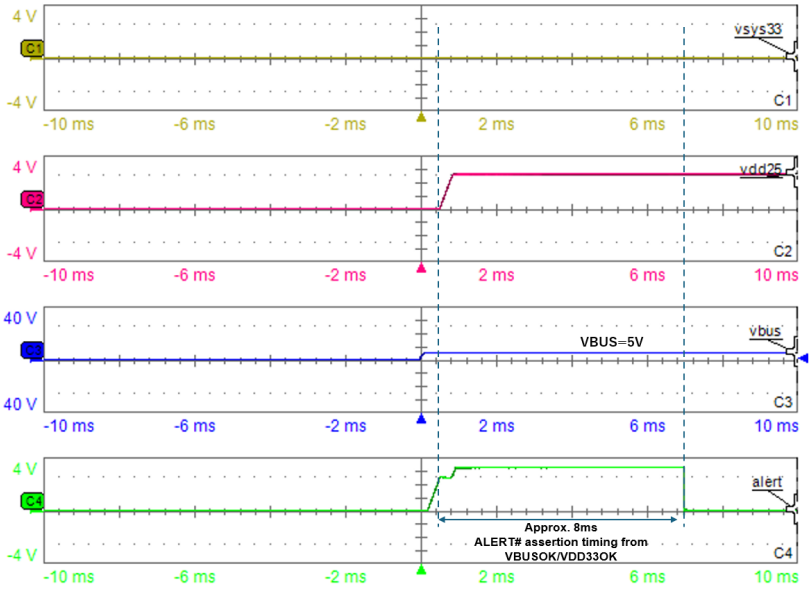


Figure 12. Startup from VBUS (2.0ms/Div on C1 = VSYS33, C2 = VDD25, C4 = ALERT#, 10V/Div on C3 = VBUS

5. Functional Description

5.1 Start-Up

When VSYS33 is supplied, 3.3V is supplied to a 3.3V domain block, VSNK_GATE/VSNK_SRC gate driver, and 2.5V LDO. Also, VSYS33 is passed through VDD33. In this condition, the 3.3V LDO is disabled.

When VSYS33 is not supplied and VBUS is supplied, VBUS is the input to the 3.3V LDO and the VSYS33 switch (VSYS33 SW) is turned off. Also, the 3.3V LDO outputs 3.3V to the 3.3V domain block, VSNK_GATE/VSNK_SRC gate driver, 2.5V LDO, and VDD33. This condition is implemented for when the system does not have any power (for example, dead battery condition).

When the output of the 2.5V LDO rises above a 2.4V POR threshold (VDD2p5_2P4_r), the RAA489400 digital block is activated and starts the TCPC operation.

When VDD33 is supplied but both VSYS33 and VBUS are not supplied, 2.5V LDO is not enabled and the RAA489400 does not start the TCPC operation.

When VCONN_POWER is supplied, 5V is supplied to VCONN Mux, charge pump for VCONN, and charge pump for VSRC_GATE/VSRC_SRC/VSRC_BOOT.

5.2 Programming Resistors

A 1% resistor from the PROG pin to GND programs the configuration of the RAA489400.

Table 1 shows the programming option for the SMBus/I^{2}C slave target address. When VDD33 is powered from either VSYS33 or VBUS, RAA489400 checks the resistance value that is connected to PROG pin with GND, and it configures the SMBus/I^{2}C slave target address based on Table 1.

If the RAA489400 receives I^{2}C access before completing a read to the PROG resistor, the RAA489400 ignores the I^{2}C access.

Table 1. PROG Pin Programming Table

PROG-GND Resistance (Ω)			Slave Target Address (7-bit)
Min	Nominal	Max	
950	1000	1050	0x22
1425	1500	1575	0x23
2090	2200	2310	0x24
3135	3300	3465	0x25
4465	4700	4935	0x26
6460	6800	7140	0x27

5.3 USB Type-C Port Controller Interface

The RAA489400 supports USB Type-C Port Controller Interface specification Revision 2.0 with EPR, which is defined in USB PD specification Revision 3.1. TCPM controls RAA489400 USB Type-C Port Controller through the SMBus/I^{2}C slave target register. Reference the Registers section for details on the TCPC standard and the RAA489400 vendor-defined register information.

5.3.1 USB PD BMC PHY

The RAA489400 supports USB PD BMC (Bi-phase Mark coded) Baseband PHY. The TCPM enables the USB PD BMC PHY when the RAA489400 is in Attached.SNK, Attach.SRC, DebugAccessory with either Source only, Sink only, or the DRP (Dual Role Power) power role, which is configured in ROLE_CONTROL (1Ah). The

RECEIVE_BUFFER (30h) and TRANSMIT_BUFFER (50h) registers are supported to transmit/receive USB PD protocol messages.

5.3.2 USB Type-C Current Mode

The RAA489400 supports the following USB Type-C current options: Default, 1.5A, or 3.0A. This configuration is set in ROLE_CONTROL (1Ah).

5.3.3 VCONN Mux

The VCONN source mux provides 5V power from the VCONN_POWER pin to CC1 or CC2 when Bit0.Enable VCONN in POWER_CONTROL (1Ch) is set to 1b. Bit0.Plug Orientation in TCPC_CONTROL (19h) must be configured for plug orientation when the USB-C device is connected.

When the VCONN fault protection (OV/UV/OT/RV) is enabled and a fault condition is detected, the RAA489400 turns off VCONN Mux.

5V is supplied to VCONN_POWER when the RAA489400 works as a VBUS source.

5.3.4 Source Path Control

RAA489400 supports two options for VBUS source path control. The following options are configured in GPIO1_CTRL Register (82h), GPIO2_CTRL Register (83h), GPIO3_CTRL Register (84h), GPIO4_CTRL Register (85h), VBUS_PATH_CTRL Register (86h), and VBUS_GPIO_CTRL Register (87h).

- VSRC_GATE/VSRC_SRC/VSRC_BOOT for external N-ch MOSFET
- GPIO (VBUS source power switch enable function for external VBUS power switch)

When TCPM sends a command of DisableSourceVbus or SourceVbusDefaultVoltage to the RAA489400 through COMMAND (23h), the RAA489400 turns off/on the VBUS source path.

When the VBUS source fault protection (OC/OV/UV/RV) is enabled and a fault condition is detected, RAA489400 turns the VBUS source path off.

5.3.5 Sink Path Control

The RAA489400 supports two options for the VBUS sink path control. The following options are configured in GPIO1_CTRL Register (82h), GPIO2_CTRL Register (83h), GPIO3_CTRL Register (84h), GPIO4_CTRL Register (85h), VBUS_PATH_CTRL Register (86h), and VBUS_GPIO_CTRL Register (87h).

- VSNK_GATE/VSNK_SRC for external N-ch MOSFET
- GPIO (VBUS sink power switch enable function for external VBUS power switch)

When the TCPM sends a command of DisableSinkVbus or SinkVbus to the RAA489400 through COMMAND (23h), the RAA489400 turns off/on the VBUS sink path.

When the VBUS sink fault protection (OV/UV) is enabled and a fault condition is detected, the RAA489400 turns off VBUS sink path.

5.3.6 Bi-directional VBUS Source and Sink Path Control

The RAA489400 supports one option for a bi-directional VBUS source and sink path control (see Figure 9). The GPIO must be used to control the bi-directional VBUS source and sink path. VBUS_SRC_SEL and VBUS_SNK_SEL must be set with same value with one GPIO pin in VBUS_PATH_CTRL Register.

For example, VBUS_PATH_CTRL Register is set to 0x33 with GPIO1. In this case, when the TCPM sends a command of SourceVbusDefaultVoltage or SinkVbus to RAA489400, GPIO1 is asserted to turn bi-directional VBUS source and sink path on. When the TCPM sends a command of DisableSourceVbus and DisableSinkVbus to the RAA489400, GPIO1 is deasserted to turn bi-directional VBUS source and sink path off. Because of VBUS protection functions, the TCPM must send an appropriate command to control that is based on CC_STATUS Register.

Note: SRC_VBUS_RVP_DIS must be set to 1b to disable the VBUS reverse voltage protection function when VBUS_SRC_SEL and VBUS_SNK_SEL are set to same value for bi-directional VBUS path control.

5.3.7 VBUS Monitoring and Measurement

The RAA489400 supports the VBUS Monitoring and Measurement function for VBUS voltage, VBUS current, Sink Disconnect Detection, and VBUS Discharge to vSafe0V as described in the following sections.

5.3.7.1 VBUS Voltage Measurement

The TCPM can monitor the VBUS voltage measurement status in VBUS_VOLTAGE (70h) when Bit6.VBUS_VOLTAGE Monitor in POWER_CONTROL (1Ch) is enabled.

5.3.7.2 VBUS Current Measurement

The TCPM can monitor VBUS current measurement status in VBUS_CURRENT Register (92h) when the Disabled VBUS_CURRENT monitor is set to 0b in VBUS_CTRL Register (90h).

The TCPM can also monitor a peak current and average current in VBUS_PEAK_CURRENT Register (94h) and VBUS_AVE_CURRENT Register (96h) when Bit4.PEAK_EN and/or Bit7.AVERAGE_EN is enabled in VBUS_CTRL Register (90h).

VBUS_PEAK_CURRENT Register (94h) shows a maximum VBUS peak current.

VBUS_AVE_CURRENT Register (96h) shows an average current over a time period specified in VBUS_CTRL Register (90h). The RAA489400 calculates the average current as the following. Refer to VBUS_CTRL Register (90h) for more information.

y_n = Average Current at Time n, x_n = VBUS Current sampled at Time n, y0 = 0,

$y_{n+1} = y_n + (x_n - y_n) / (N3 * 2^{N4})$

5.3.7.3 VBUS Voltage Alarm

The VBUS voltage alarm function is disabled as a default setting per TCPCi specification. The TCPM can write DisableVoltageAlarms = 0b in POWER_CONTROL (1Ch) to enable the voltage alarms.

The TCPM can write to VBUS_VOLTAGE_ALARM_HI_CFG (76h) to set the high voltage alarm level. The RAA489400 sets VBUSVoltageAlarmHi to 1b in ALERT (10h) when VBUS exceeds the high voltage alarm level in VBUS_VOLTAGE_ALARM_HI_CFG (76h). The RAA489400 re-asserts VBUSVoltageAlarmHi in ALERT (10h) when the high voltage condition on VBUS prevails after the TCPM has cleared VBUSVoltageAlarmHi in ALERT (10h) unless the TCPM disables the voltage alarms by setting DisableVoltageAlarms to 1b in POWER_CONTROL (1Ch).

The TCPM can write to VBUS_VOLTAGE_ALARM_LO_CFG (78h) to set the low voltage alarm level. The RAA489400 sets VBUSVoltageAlarmLo to 1 in ALERT (10h) when VBUS drops below the low voltage alarm level in VBUS_VOLTAGE_ALARM_LO_CFG (78h). The RAA489400 re-asserts VBUSVoltageAlarmLo in ALERT (10h) when the low voltage condition on VBUS prevails after the TCPM has cleared VBUSVoltageAlarmLo in ALERT (10h), unless the TCPM disables the voltage alarms by setting DisableVoltageAlarms to 1b in POWER_CONTROL (1Ch).

5.3.7.4 VBUS Discharge

The RAA489400 supports the automatic VBUS discharge function after a disconnect detection when Bit4.Auto Discharge Disconnect is set to 1b in POWER_CONTROL (1Ch) 1b. The RAA489400 supports force VBUS discharge by setting Bit.2.Force Discharge in POWER_CONTROL (1Ch) so that the TCPM can manually discharge VBUS.

When the RAA489400 starts the VBUS discharge to vSafe0V, the RAA489400 monitors the VBUS voltage and stops the VBUS discharge when VBUS is below vSafe0V (max). When the VBUS discharge is stopped, the RAA489400 does not reapply the VBUS discharge although the VBUS might be higher than vSafe0V (max), but it does reapply the VBUS discharge when another VBUS discharge command or event occurs.

In contrast, when the RAA489400 is the source and the Force Discharge bit of the POWER_CONTROL register is set to 1b, the RAA489400 starts the VBUS discharge and monitors the VBUS voltage to stop the discharging. The discharging VBUS voltage is stopped when the VBUS voltage is below the VBUS_STOP_DISCHARGE_THRESHOLD register.

5.3.8 Internal Sink Path Discharge

The RAA489400 provides an internal Sink discharge function with the SNK_DISCHG pin to discharge an internal sink path, for example, between VBUS sink gate and the battery charger (adapter side).

When a system supports multiple USB-C ports with multiple RAA489400 devices and the first USB-C port (C1) has an EPR Source adapter (up to 240W/48V) and a second USB-C port (C2) has a SPR (up to 100W/20V) source adapter (as in Figure 13), the internal system sink path between the VBUS sink gate and a battery charger (adapter side) has a high voltage (such as 48V). In this case when the EPR source adapter is disconnected, the internal system sink path must be discharged to vSafe5V or 0V for safety before the VBUS sink gate of the second USB-C port is turned on. Otherwise, the SPR source adapter on the second USB-C port might have damage because of a higher voltage than its source capability from the internal sink path.

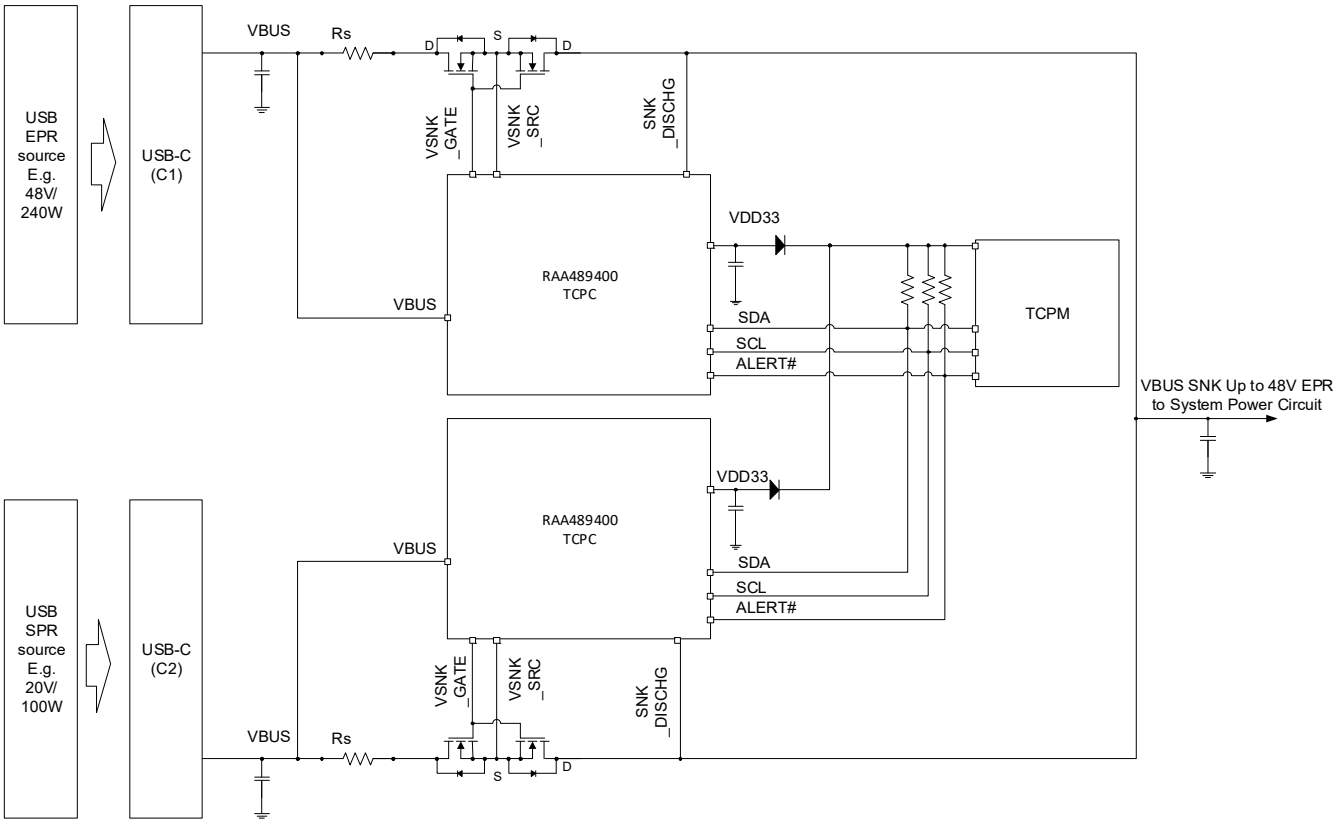


Figure 13. Typical Multiport Sink Only

The RAA489400 provides the following option for the TCPM or system when the RAA489400 works as a sink. The following options can be configured in SINK_PATH_DISCHG Register (9Ah).

- Automatic discharge when RAA489400 receives SinkVbus command.
- Manual discharge with TCPM operation.

5.3.8.1 Automatic Discharge

When DISCHG_MODE of SINK_PATH_DISCHG Register (9Ah) is set to 1b (that is automatic discharge), the RAA489400 receives the SinkVbus command and the internal sink path voltage exceeds the vSafe5V(max); the RAA489400 automatically discharges the internal sink path voltage until the voltage reaches below the

vSafe5V(max). When a voltage is lower than the vSafe5V(max), the RAA489400 stops to discharge and enables VBUS sink gate.

The sink discharge timeout is set to DISCHARGE_TIMEOUT of SINK_PATH_DISCHG Register (9Ah) if the internal sink path voltage is higher than the vSafe5V(max) after the sink discharge timeout setting of receiving the SinkVbus command. Next, the RAA489400 sets a 1b sink path discharge completion bit (Bit 14) and a Sink path discharge timeout bit (Bit15) of VENDOR_STATUS Register (A0h) to notify a discharge failure, and it asserts an ALERT# pin to the TCPM. Afterwards, the RAA489400 discards the SinkVbus command. Also, the TCPM can acknowledge the internal sink path has failed to reach the vSafe5V and can report this failure to the EC and/or CPU.

Note: The RAA489400 does not discharge the internal sink path when it detects a disconnection.

5.3.8.2 Manual Discharge

When DISCHG_MODE of SINK_PATH_DISCHG Register (9Ah) is set to 0b (that is manual discharge) and the TCPM writes 1b to MANUAL_DISCHG of SINK_PATH_DISCHG Register (9Ah), the RAA489400 discharges the internal sink path voltage to vSafe5V(max). When a voltage is lower than the vSafe5V(max), the RAA489400 stops discharge and sets 1b to the sink path discharge completion bit (Bit14) of VENDOR_STATUS Register (A0h) to notify discharge completion and assert ALERT# pin to the TCPM. Next, the TCPM can send the SinkVbus command to the RAA489400 that controls the second USB-C port.

The Sink Discharge Timeout of discharge is set to DISCHARGE_TIMEOUT of SINK_PATH_DISCHG Register (9Ah) if the internal sink path voltage is higher than the vSafe5V(max) after the sink discharge timeout setting of receiving the MANUAL_DISCHG = 1b, and the RAA489400 sets 1b to the sink path discharge completion bit (Bit14) and sink path discharge timeout bit (Bit15) of VENDOR_STATUS Register (A0h) to notify discharge failure and assert the ALERT# pin to TCPM. Finally, the TCPM can acknowledge the internal sink path has failed to reach the threshold setting and can report this failure to the EC and/or CPU.

5.3.9 Initial Sink Fast Role Swap

The RAA489400 supports Initial Sink Fast Role Swap based on the USB PD specification. Fast Role Swap can be enabled in POWER_CONTROL (1Ch).

The RAA489400 turns Sink gate off at first when Fast Role Swap occurs, that is when the RAA489400 receives the Fast Role Swap Signal from a connected USB-C/PD VBUS source device. Next, the RAA489400 turns Source gate on for a new sink device.

Trigger conditions of Sink/Source gate control and timing between those controls are defined in FRS_CTRL Register (98h). Settings of this register are valid only when the Fast Role Swap Enable bit of the POWER_CONTROL (1Ch) is set to 1b.

The TCPM must disable the Fast Role Swap in POWER_CONTROL (1Ch) before the TCPM sends a FR_Swap message.

Note: The RAA489400 does not support Initial Source Fast Role Swap.

Note: The RAA489400 does not consider Fast Role Swap support with Bi-directional VBUS Source and Sink Path Control.

5.4 Protection Features

The RAA489400 supports features for VBUS protection and VCONN Mux protection as described in the following sections. Table 2 and Table 3 clarify the control/status/mask register for each protection.

Table 2. VBUS Protection

Protection	Supported Power Role	Control Register	Status Register	Mask Register
VBUS Overcurrent	Source/Sink	FAULT_CONTROL (1Bh)	FAULT_STATUS (1Fh)	FAULT_STATUS_MASK (15h)
VBUS Overvoltage	Source/Sink	FAULT_CONTROL (1Bh) VBUS_FAULT_CTRL Register (A4h)	FAULT_STATUS (1Fh)	FAULT_STATUS_MASK (15h)
VBUS Undervoltage	Source	VBUS_FAULT_CTRL Register (A4h)	VENDOR_STATUS Register (A0h)	VENDOR_STATUS_ALERT_MASK Register (A2h)
VBUS Reverse Voltage	Source	VBUS_FAULT_CTRL Register (A4h)	VENDOR_STATUS Register (A0h)	VENDOR_STATUS_ALERT_MASK Register (A2h)

Table 3. VCONN Protection

Protection	Control Register	Status Register	Mask Register
VCONN Overcurrent	FAULT_CONTROL (1Bh) VCONN_FAULT_CTRL Register (A6h)	FAULT_STATUS (1Fh)	FAULT_STATUS_MASK (15h)
VCONN Overvoltage	VCONN_FAULT_CTRL Register (A6h)	VENDOR_STATUS Register (A0h)	VENDOR_STATUS_ALERT_MASK Register (A2h)
VCONN Undervoltage	VCONN_FAULT_CTRL Register (A6h)	VENDOR_STATUS Register (A0h)	VENDOR_STATUS_ALERT_MASK Register (A2h)
VCONN Reverse Voltage	VCONN_FAULT_CTRL Register (A6h)	VENDOR_STATUS Register (A0h)	VENDOR_STATUS_ALERT_MASK Register (A2h)
VCONN Over-temperature	VCONN_FAULT_CTRL Register (A6h)	VENDOR_STATUS Register (A0h)	VENDOR_STATUS_ALERT_MASK Register (A2h)

5.4.1 VBUS Overcurrent Protection

If the VBUS Overcurrent Protection Fault is enabled in FAULT_CONTROL (1Bh), the RAA489400 takes the following actions when the VBUS overcurrent is detected either internally with CSIP/CSIN or externally with the overcurrent input from the GPIO function.

- Turns off the VBUS source gate and discharge VBUS to vSafe0V when the RAA489400 works as a VBUS source.
- Turns off the VBUS sink gate when the RAA489400 works as a VBUS sink.
- Sets the VBUS Overcurrent Protection Fault bit in FAULT_STATUS (1Fh).
- Asserts the OCP# pin if VBUS_OCP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- If the RAA489400 works as a VCONN source (that is Enable VCONN = 1b in POWER_CONTROL (1Ch)), the RAA489400 also takes the following actions:
  - Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
  - Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).

The VBUS overcurrent threshold can be configured in VBUS_FAULT_CTRL Register (A4h). The following threshold setting is available: 3.6A (Default), 1.8A, 4.8V, and 6.0A.

5.4.2 VBUS Overvoltage Protection

If the VBUS Overvoltage Protection Fault is enabled in FAULT_CONTROL (1Bh) and/or VBUS_FAULT_CTRL Register (A4h), the RAA489400 takes the following actions when VBUS overvoltage is detected.

- Turns off the VBUS source gate and discharges VBUS to vSafe0V when the RAA489400 works as a VBUS source
- Turn off the VBUS sink gate when the RAA489400 works as a VBUS sink.
- Sets the VBUS Overvoltage Protection Fault bit in FAULT_STATUS (1Fh).
- Asserts the OCP# pin if the VBUS_OVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- If RAA489400 works as VCONN source (that is Enable VCONN = 1b in POWER_CONTROL (1Ch)), the RAA489400 also takes the following actions:
  - Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
  - Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).

Note: The VBUS source overvoltage thresholds are vVbusOv, vSprMax, or vEprMax in the Electrical Specifications. The VBUS sink overvoltage thresholds are vSprMax or vEprMax in the Electrical Specifications. The VBUS overvoltage threshold is configured in VBUS_FAULT_CTRL Register (A4h).

5.4.3 VBUS Source Undervoltage Protection

If VBUS Source Undervoltage Protection is enabled in the VBUS_FAULT_CTRL Register (A4h), the RAA489400 takes the following when VBUS source undervoltage is detected and RAA489400 works as a VBUS Source.

- Turns off the VBUS source gate and discharges VBUS to vSafe0V.
- Sets SRC_VBUS_UVP bit in VENDOR_STATUS Register (A0h).
- Asserts the OCP# pin if SRC_VBUS_UVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- Sets the VBUS Overcurrent Protection Fault bit in FAULT_STATUS (1Fh) if the VBUS Overcurrent Protection Fault bit in FAULT_CONTROL (1Bh) is set to 0b and VBUS_UVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- If the RAA489400 works as a VCONN source (that is Enable VCONN = 1b in POWER_CONTROL (1Ch)), the RAA489400 also takes the following actions:
  - Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
  - Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).

Note: The VBUS source undervoltage detection is not activated from the moment VBUS is enabled to the time specified by UVP_INACTIVE_TIME is elapsed, although the SRC_VBUS_UVP_DIS bit of VBUS_FAULT_CTRL Register (A4h) is 0b and the VBUS voltage is below the vVbusUv threshold.

Note: The RAA489400 does not support the VBUS sink undervoltage when the RAA489400 works as a VBUS sink, because the RAA489400 supports VBUS_SINK_DISCONNECT_THRESHOLD (72h) to detect a disconnection.

5.4.4 VBUS Source Reverse Voltage Protection

If VBUS Source Reverse Voltage Protection is enabled in VBUS_FAULT_CTRL Register (A4h), the RAA489400 takes the following when VBUS RV is detected.

- Turns off VBUS source gate and then discharges VBUS to vSafe0V when the RAA489400 works as a VBUS source.
- Sets the SRC_VBUS_RVP bit in VENDOR_STATUS Register (A0h).
- Asserts the OCP# pin if VBUS_RVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- Sets the VBUS Overcurrent Protection Fault bit in FAULT_STATUS (1Fh), if the VBUS Overcurrent Protection is enabled in FAULT_CONTROL (1Bh) and VBUS_RVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.

- If the RAA489400 works as a VCONN source (that is Enable VCONN = 1b in POWER_CONTROL (1Ch)), the RAA489400 also takes the following actions:
  - Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
  - Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).

Note: When VBUS_SRC_SEL and VBUS_SNK_SEL are set to the same value in VBUS_PATH_CTRL Register for bi-directional VBUS path control, the VBUS source reverse voltage protection must be disabled.

5.4.5 VCONN Overcurrent Protection

If the VCONN Overcurrent Fault is enabled in FAULT_CONTROL (1Bh), the RAA489400 takes the following when the VCONN Overcurrent is detected.

- Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).
- Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
- Sets the VCONN Overcurrent Fault bit in FAULT_STATUS (1Fh).
- Asserts the OCP# pin if VCONN_OCP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.

The VCONN overcurrent threshold is configured in the VCONN_FAULT_CTRL Register (A6h). The following threshold setting is available: 400mA (default), 600mA, and 800mA.

5.4.6 VCONN Overvoltage Protection

The RAA489400 takes the following when VCONN overvoltage is detected.

- Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).
- Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
- Sets the VCONN_OVP bit in VENDOR_STATUS Register (A0h).
- Asserts the OCP# pin if VCONN_OVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- Sets the VCONN Overcurrent Fault in FAULT_STATUS Register, if the VCONN Overcurrent Fault is enabled in FAULT_CONTROL (1Bh) and VCONN_OVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.

5.4.7 VCONN Undervoltage Protection

The RAA489400 takes the following when VCONN UV is detected.

- Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).
- Turns off the VCONN Mux and discharges VCONN to vVconnDischarge.
- Sets the VCONN_UVP bit in VENDOR_STATUS Register (A0h).
- Asserts the OCP# pin if VCONN_UVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.
- Sets the VCONN Overcurrent Fault bit in FAULT_STATUS (1Fh), if the VCONN Overcurrent Fault is enabled in FAULT_CONTROL (1Bh) and VCONN_UVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.

Note: VCONN_UV detection is not activated from the moment VCONN is enabled to the time specified by UVP_INACTIVE_TIME of VCONN_FAULT_CTRL Register (A6h) is elapsed, although, VCONN_UVP_DIS bit of VCONN_FAULT_CTRL Register (A6h) is 0b and VCONN voltage is below the vVconnUv threshold.

5.4.8 VCONN Over-temperature Protection

If the VCONN Overtemperature Fault is enabled in VCONN_FAULT_CTRL Register (A6h), the RAA489400 takes the following when VCONN OT is detected.

- Clears Enable VCONN to 0b in POWER_CONTROL (1Ch).
- Turns off VCONN Mux and discharges VCONN to vVconnDischarge.
- Turns off the VBUS source gate and discharges VBUS to vSafe0V when the RAA489400 works as a VBUS source.
- Turns off the VBUS sink gate when the RAA489400 works as a VBUS sink.

- Sets the VCONN_OTP bit in VENDOR_STATUS Register (A0h).
- Asserts the OCP# pin if VCONN_OTP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.

5.4.9 VCONN Reverse Voltage Protection

RAA489400 takes the following when VCONN RV is detected.

- Clears Enable VCONN to 0b in POWER_CONTROL (1Ch)
- Turns off VCONN Mux and then discharge VCONN to vVconnDischarge.
- Turns off VBUS source gate and then discharge VBUS to vSafe0V when RAA489400 works as VBUS source.
- Turns off VBUS sink gate when RAA489400 works as VBUS sink.
- Sets VCONN_RVP bit in VENDOR_STATUS Register (A0h).
- Asserts OCP# pin if VCONN_RVP of is set to 1b.
- Sets the VCONN Overcurrent Fault bit in FAULT_STATUS (1Fh), if the VCONN Overcurrent Fault is enabled in FAULT_CONTROL (1Bh) and VCONN_RVP of OCP_OUTPUT_CTRL Register (A8h) is set to 1b.

5.5 OCP# Output

When RAA489400 detects a fault condition which is configured in OCP_OUTPUT_CTRL Register (A8h), the RAA489400 asserts the OCP# pin to low. When all fault conditions are removed in FAULT_STATUS (1Fh) and VENDOR_STATUS Register (A0h), the RAA489400 deasserts OCP# pin.

The OCP# function is used for a direct notification signal from the RAA489400 to a system (such as a power management circuit or main system SoC) to notify a fault event.

5.6 PROCHOT#

RAA489400 supports the PROCHOT# function to notify disconnection of a VBUS source device and/or fast role swap event. If the PROCHOT function is enabled in PROCHOT_EN Register (AAh), the RAA489400 asserts PROCHOT# when the RAA489400 detects the following conditions based on the configuration in PROCHOT_EN Register (AAh).

- Disconnection of VBUS source device.
- FRS signal received.

For example, the PROCHOT# function is used for a direct notification signal from the RAA489400 to a system (such as a power management circuit or main system SoC) in the event that a USB-C port loses a power source so that a system starts to reduce a VBUS current drawing.

Table 4. PROCHOT# Assertion Condition for the Event of Disconnection of VBUS Source Device

PROCHOT_EN SNK_DETACH_EN	SNK_DETACH SNK_OPEN	VENDOR_STATUS SNK_DETCH_PROCHOT	PROCHOT# signal
0	Zero	Set to 1b	Deasserted
	Non-Zero	Set to 1b	Deasserted
1	Zero	Set to 1b	Deasserted
	Non-Zero	Set to 1b	Asserted

Table 5. PROCHOT# Assertion Condition for the Event of FRS Signal Received

PROCHOT_EN FRS_EN	POWER_CONTROL Fast Role Swap Enable	ALERT_EXTERNED Sink Fast Role Swap	PROCHOT# signal
0	0b	Set to 0b	Deasserted
	1b	Set to 0b	Deasserted
1	0b	Set to 0b	Deasserted
	1b	Set to 1b	Asserted

5.7 GPIO

The RAA489400 supports the configurable general-purpose input and output with the following functions. The following function can be configured in GPIO1_CTRL Register (82h), GPIO2_CTRL Register (83h), GPIO3_CTRL Register (84h), GPIO4_CTRL Register (85h), VBUS_PATH_CTRL Register (86h), VBUS_GPIO_CTRL Register (87h), and GPIO_OC_EN Register (89h).

1. VBUS source power switch enable function (see Source Path Control).
2. VBUS sink power switch enable function (see Sink Path Control).
3. Overcurrent Input (as STANDARD_INPUT in TCPCI specification). (See Overcurrent Input.)
4. General purpose input.
5. General purpose output (push-pull).
6. General Purpose output (open-drain).

5.7.1 Overcurrent Input

The RAA489400 supports the Overcurrent Input function that is defined in STANDARD_INPUT_CAPABILITIES Register as a TCPCi specification to detect a fault condition from an external VBUS power switch.

An input status is shown in GPIO1_CTRL Register (82h), GPIO2_CTRL Register (83h), GPIO3_CTRL Register (84h), and/or GPIO4_CTRL Register (85h) as well as FAULT_STATUS (1Fh) for the TCPM when a GPIO is enabled as an Overcurrent Input function in GPIO_OC_EN Register (89h).

In addition, if a fault condition is detected from an external VBUS power switch, a GPIO is enabled as an Overcurrent Input function in GPIO_OC_EN Register (89h), and the OCP# output is enabled in OCP_OUTPUT_CTRL Register (A8h), the RAA489400 asserts the OCP# pin to low.

5.8 Clock Management

The RAA489400 supports the integrated oscillators for a 30kHz and 24MHz internal clock. The 30kHz oscillator always works. The 24MHz oscillator can be disabled by the TCPM with the Stop_24MHz_OSC bit in TYPE_C_PRAMETER Register (E2h) when no USB-C device is connected to the RAA489400. When CC1/CC2 status is changed or I^2C access is received, the 24MHz clock is automatically enabled and the Stop_24MHz_OSC bit is automatically cleared in TYPE_C_PRAMETER Register (E2h). The Stop_24MHz_OSC bit in TYPE_C_PRAMETER Register (E2h) reduces power consumption.

6. General SMBus/I²C Architecture

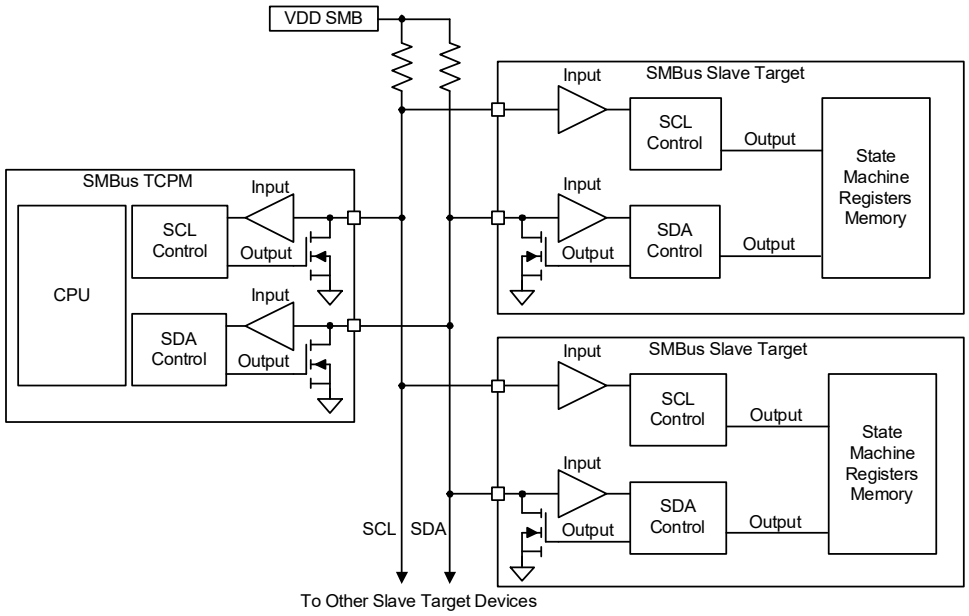


Figure 14. General SMBus Architecture

6.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 15.

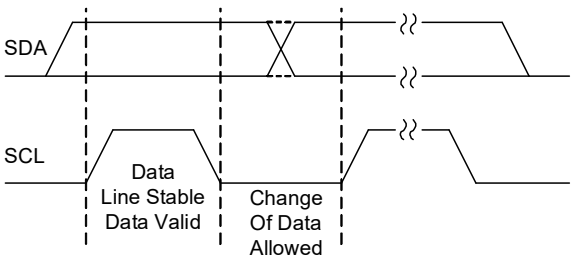


Figure 15. Data Validity

6.2 START and STOP Conditions

Figure 16 shows that the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

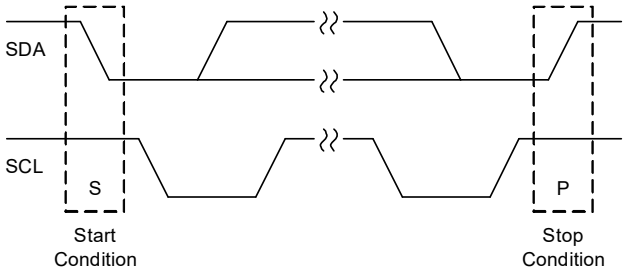


Figure 16. Start and Stop Waveforms

6.3 Acknowledge (ACK)

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the TCPM sends seven slave target address bits and a R/W bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line LOW to acknowledge (see Figure 17). Both the TCPM and slave target use the ACK bit to acknowledge receipt of register addresses and data.

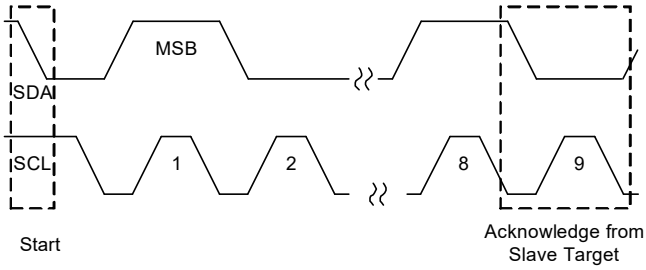


Figure 17. Acknowledge on the SMBus

6.4 Writing Single Byte Registers

When writing to a single byte register, use the following transaction.

Figure 18. Writing Single Byte Registers

6.5 Reading Single Byte Registers

When reading to a single byte register, use the following transaction.

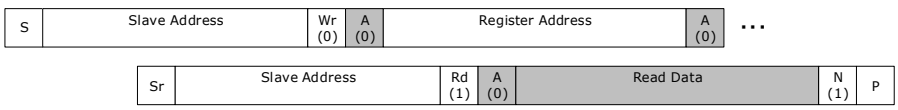


Figure 19. Reading Single Byte Registers

6.6 Writing Two-Byte Registers

When writing to a two-byte register, use the following transaction.

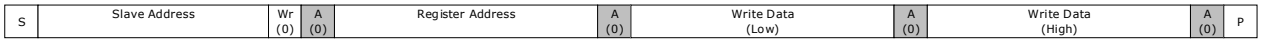


Figure 20. Writing Two-Byte Registers

6.7 Reading Two-Byte Registers

When reading a two-byte register, use the following transaction.

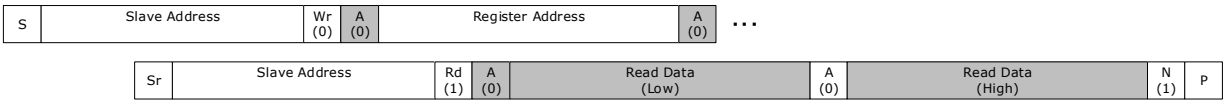


Figure 21. Reading Two-Byte Registers

6.8 Writing the TRANSMIT_BUFFER

When writing to the TRANSMIT_BUFFER register, use the following transaction.

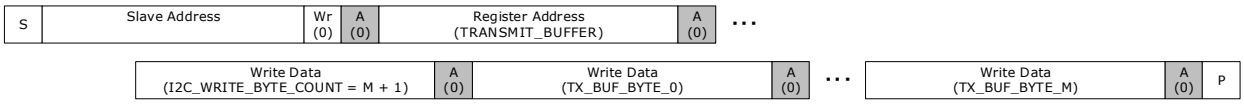


Figure 22. Writing the TRANSMIT_BUFFER

6.9 Reading the RECEIVE_BUFFER

When reading the RECEIVE_BUFFER register, use the following transaction.

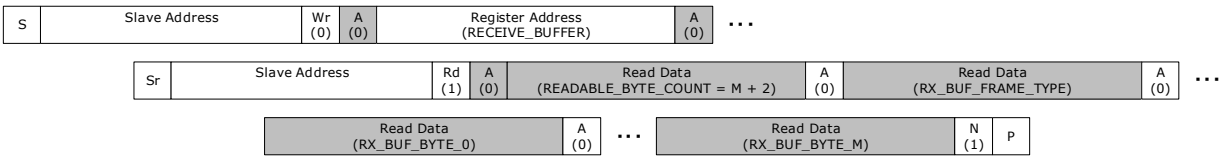


Figure 23. Reading the RECEIVE_BUFFER

6.10 Reading the Alert Response Address

When reading the Alert Response Address register, use the following transaction.

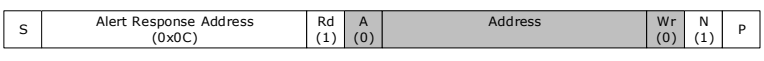


Figure 24. Reading the Alert Response Address

7. Registers

Table 6. Register Attributes

Attribute	Abbreviation	Description
Read/Write	R/W	Read/Write
Read Only	R	Read Only (Write1/0 ignore)
Write Only	W	Write Only
Read. Write 1 Clear	R/W1C	Read. Write 1 Clear (Write 0 ignore)

7.1 Register Map

Table 7. Register Map

Address	Register Name	Register Table	Type	Reset Value
TCPC Standard Registers				
00h...01h	VENDOR_ID	Table 8	R	045Bh
02h...03h	PRODUCT_ID	Table 9	R	026Dh
04h...05h	DEVICE_ID	Table 10	R	0100h
06h...07h	USBTYPEC_REV	Table 11	R	0021h
08h...09h	USBPD_REV_VER	Table 12	R	3115h
0Ah...0Bh	PD_INTERFACE_REV	Table 13	R	2012h
0Ch...0Fh	Reserved as TCPCI specification	-	-	-
10h...11h	ALERT	Table 14	R/W	0200h
12h...13h	ALERT_MASK	Table 15	R/W	6FFFh
14h	POWER_STATUS_MASK	Table 16	R/W	DFh
15h	FAULT_STATUS_MASK	Table 17	R/W	BFh
16h	EXTENDED_STATUS_MASK	Table 18	R/W	01h
17h	ALERT_EXTENDED_MASK	Table 19	R/W	01h
18h	Reserved as TCPCI specification	-	-	-
19h	TCPC_CONTROL	Table 20	R/W	00h
1Ah	ROLE_CONTROL	Table 21	R/W	0Ah or 0Fh
1Bh	FAULT_CONTROL	Table 22	R/W	00h
1Ch	POWER_CONTROL	Table 23	R/W	62h
1Dh	CC_STATUS	Table 24	R	00h
1Eh	POWER_STATUS	Table 25	R	48h
1Fh	FAULT_STATUS	Table 26	R/W	80h
20h	EXTENDED_STATUS	Table 27	R	01h
21h	ALERT_EXTENDED	Table 28	R/W	00h
22h	Reserved as TCPCI specification	-	-	-

Table 7. Register Map (Cont.)

23h	COMMAND	Table 29	W	00h
24h...25h	DEVICE_CAPABILITIES_1	Table 31	R	7EDDh
26h...27h	DEVICE_CAPABILITIES_2	Table 32	R	C2C3h
28h	STANDARD_INPUT_CAPABILITIES	Table 33	R	02h
29h	STANDARD_OUTPUT_CAPABILITIES	Table 34	R	00h
2Ah	Reserved as RAA489400	-	-	-
2Bh	Reserved as TCPCI specification	-	-	-
2Ch...2Dh	Reserved as RAA489400	-	-	-
2Eh	MESSAGE_HEADER_INFO	Table 35	R/W	04h
2Fh	RECEIVE_DETECT	Table 36	R/W	00h
30h	READABLE_BYTE_COUNT	Table 37	R	00h
	RX_BUF_FRAME_TYPE	Table 38	R	00h
	RX_BUF_BYTE_x	Table 39	R	00h
50h	TRANSMIT	Table 40	R/W	00h
51h	I2C_WRITE_BYTE_COUNT	Table 41	W	00h
	TX_BUF_BYTE_x	Table 42	W	00h
70h...71h	VBUS_VOLTAGE	Table 43	R	0000h
72h...73h	VBUS_SINK_DISCONNECT_THRESHOLD	Table 44	R/W	008Ch
74h...75h	VBUS_STOP_DISCHARGE_THRESHOLD	Table 45	R/W	0020h
76h...77h	VBUS_VOLTAGE_ALARM_HI_CFG	Table 46	R/W	0000h
78h...79h	VBUS_VOLTAGE_ALARM_LO_CFG	Table 47	R/W	0000h
7Ah...7Bh	Reserved as RAA489400	-	-	-
7Ch..7Dh	DEVICE_CAPABILITIES_3	Table 48	R	0006h
7Eh...7Fh	Reserved as TCPCI specification	-	-	-
RAA489400 Vendor Defined Registers				
80h	CHIP_REV	Table 49	R	12h
81h	Reserved	-	-	-
82h	GPIO1_CTRL	Table 50	R/W	00h
83h	GPIO2_CTRL	Table 51	R/W	00h
84h	GPIO3_CTRL	Table 52	R/W	00h
85h	GPIO4_CTRL	Table 53	R/W	00h
86h	VBUS_PATH_CTRL	Table 54	R/W	00h
87h	VBUS_GPIO_CTRL	Table 55	R/W	00h
88h	VBUS_CP_CTRL	Table 56	R/W	00h
89h	GPIO_OC_EN	Table 57	R/W	00h
8Ah…8Fh	Reserved	-	-	-
90h…91h	VBUS_CTRL	Table 57	R/W	0001h
92h…93h	VBUS_CURRENT	Table 58	R	0000h

Table 7. Register Map (Cont.)

94h…95h	VBUS_PEAK_CURRENT	Table 60	R	0000h
96h…97h	VBUS_AVE_CURRENT	Table 61	R	0000h
98h	FRS_CTRL	Table 62	R/W	40h
99h	Reserved	-	-	-
9Ah	SINK_PATH_DISCHG_CTRL	Table 63	R/W	00h
9Bh	SNK_DETACH	Table 64	R/W	00h
9Ch…9Fh	Reserved	-	-	-
A0h…A1h	VENDOR_STATUS	Table 65	R/W1C	0000h
A2h…A3h	VENDOR_STATUS_ALERT_MASK	Table 66	R/W	0000h
A4h…A5h	VBUS_FAULT_CTRL	Table 67	R/W	0101h
A6h	VCONN_FAULT_CTRL	Table 68	R/W	01h
A7h	Reserved	-	-	-
A8h…A9h	OCP_OUTPUT_CTRL	Table 69	R/W	0000h
AAh	PROCHOT_EN	Table 70	R/W	00h
ABh…B0h	Reserved	-	-	-
B1h	Control1	Table 71	R/W	0000h
B2h...E1h	Reserved	-	-	-
E2h...E3h	TYPE_C_PARAMETER	Table 72	R/W	0190h
E4h...FFh	Reserved	-	-	-

7.2 Register Descriptions

7.2.1 VENDOR_ID (00h)

Table 8. VENDOR_ID Register

Bit(s)	Name	Type	Reset Value	Description
B15..0	Vendor ID (VID)	R	045Bh	A Vendor ID, or VID, is used to identify the TCPC vendor. The VID is a unique 16-bit unsigned integer assigned by USB-IF.

7.2.2 PRODUCT_ID (03h) and DEVICE_ID (04h)

Table 9. PRODUCT_ID Register

Bit(s)	Name	Type	Reset Value	Description
B15..0	USB Product ID (PID)	R	026Dh	The Product ID, or PID, is used to identify the product. A unique 16-bit unsigned integer assigned uniquely by the Vendor to identify the TCPC.

Table 10. DEVICE_ID Register

Bit(s)	Name	Type	Reset Value	Description
B15..0	bcdDevice	R	0100h	The Device ID, bcdDevice, is used to identify the product release version. A unique 16-bit unsigned integer assigned by the Vendor to identify the version of the TCPC.

7.2.3 USBTYPEC_REV (06h)

Table 11. USBTYPEC_REV Register

Bit(s)	Name	Type	Reset Value	Description
B15..8	Reserved	R	00h	Set to 0
B7..0	bcdUSBTYPEC Release	R	21h	0002 0001 – Release 2.1 This register refers to USB Type-C Cable and Connector Specification Revision, USB Type-C represented by a unique 16-bit unsigned register. The format is packed binary coded decimal.

7.2.4 USBPD_REV_VER (08h)

Table 12. USBPD_REV_VER Register

Bit(s)	Name	Type	Reset Value	Description
B15..8	bcdUSBPD Revision	R	31h	0011 0001 – Revision 3.1 This register refers to USB PD specification Revision, USB PD represented by a unique 16-bit unsigned integer. The format is packed binary coded decimal.
B7..0	bcdUSBPD Version	R	15h	0001 0101 – Version 1.5 This register refers to USB PD specification Version, USB PD represented by a unique 16-bit unsigned integer. The format is packed binary coded decimal.

7.2.5 PD_INTERFACE_REV (0Ah)

Table 13. PD_INTERFACE_REV Register

Bit(s)	Name	Type	Reset Value	Description
B15..8	bcd USB-PD Inter-Block Specification Revision	R	20h	0010 0000 – Revision 2.0 The USB-Port Controller Specification Revision register refers to this Specification Revision and Version represented by a unique 16-bit unsigned integer. The format is packed binary coded decimal.
B7..0	bcd USB-PD Inter-Block Specification Version	R	12h	0001 0010 – Version 1.2 The USB-Port Controller Specification Version register refers to this Specification Revision and Version represented by a unique 16-bit unsigned integer. The format is packed binary coded decimal. *Note:* RAA489400 can transfer/receive USB PD EPR protocol with unchunked message. RAA489400 is also capable for 48V EPR voltage monitor function based on version 1.3 specification.

7.2.6 ALERT (10h)

Table 14. ALERT Register

Bit(s)	Name	Type	Reset Value	Description
B15	Vendor Defined Alert	R/W1C	0b	0b: Cleared 1b: A vendor defined alert has been detected. Defined in VENDOR_STATUS Register (A0h). This bit can be cleared, regardless of the current status VENDOR_STATUS Register (A0h) of the alert source.
B14	Alert Extended	R/W1C	0b	0b: Cleared 1b: An extended interrupt event has occurred. See ALERT_EXTENDED (21h).
B13	Extended Status	R/W1C	0b	0b: Cleared 1b: Extended Status changed
B12	Reserved	R	0b	Set to zero by sender and ignored by receiver.
B11	VBUS Sink Disconnect Detected	R/W1C	0b	0b: Cleared 1b: The TCPC in Attached_Snk state has detected a Sink disconnect. This bit is only asserted when VBUS_SINK_DISCONNECT_THRESHOLD is set and POWER_CONTROL.AutoDischargeDisconnect is set to 1b.
B10	Rx Buffer Overflow	R/W1C	0b	0b: TCPC Rx buffer is functioning properly 1b: TCPC Rx buffer has overflowed. Future GoodCRC is not sent. Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus
B9	Fault	R/W1C	1b	0b: No fault 1b: A fault has occurred in

Table 14. ALERT Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
B8	VBUS Voltage Alarm Lo	R/W1C	0b	0b: Cleared 1b: A low-voltage alarm has occurred This field maintain assert during a low-voltage alarm has occurred. If TCPM needs to disable VBUS voltage alarm function, TCPM needs to set B5 (Disable Voltage Alarms) to 1b in POWER_CONTROL (1Ch).
B7	VBUS Voltage Alarm Hi	R/W1C	0b	0b: Cleared 1b: A high-voltage alarm has occurred This field maintain assert during a high-voltage alarm has occurred. If TCPM needs to disable VBUS voltage alarm function, set B5 (Disable Voltage Alarms) to 1 in POWER_CONTROL (1Ch).
B6	Transmit SOP* Message Successful	R/W1C	0b	0b: Cleared 1b: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission.
B5	Transmit SOP* Message Discarded	R/W1C	0b	0b: Cleared 1b: Reset or SOP* message transmission not sent because of an incoming receive message. Transmit SOP* message buffer registers are empty.
B4	Transmit SOP* Message Failed	R/W1C	0b	0b: Cleared 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
B3	Received Hard Reset	R/W1C	0b	0b: Cleared 1b: Received Hard Reset message
B2	Received SOP* Message Status	R/W1C	0b	0b: Cleared 1b: RECEIVE_BUFFER register changed. READABLE_BYTE_COUNT (30h) being set to 0 does not set this bit.
B1	Power Status	R/W1C	0b	0b: Cleared 1b: Power Status changed
B0	CC Status	R/W1C	0b	0b: Cleared 1b: CC Status changed TCPC does not assert this bit when Looking4Connection changes state in CC_STATUS (1Dh) when EnableLooking4ConnectionAlert is set to TCPC_CONTROL (19h) When TCPM sets EnableLooking4ConnectionAlert set to 0 in TCPC_CONTROL (19h), TCPC does not assert this bit when Looking4Connection has changed in CC_STATUS (1Dh). When TCPM sets DRP to 0, CC1 to Open and CC2 to Open in ROLE_CONTROL (1Ah), TCPC does not assert this bit even when CC1 and CC2 status has changed.

7.2.7 ALERT_MASK (12h)

Table 15. ALERT_MASK Register

Bit(s)	Name	Type	Reset Value	Description
B15	Vendor Defined Alert	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
B14	Alert Extended Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B13	Extended Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B12	Reserved	R	0b	Set to zero by sender and ignored by receiver.
B11	VBUS Sink Disconnect Detected	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B10	Rx Buffer Overflow	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B9	Fault	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B8	VBUS Voltage Alarm Lo	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B7	VBUS Voltage Alarm Hi	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B6	Transmit SOP* Message successful Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B5	Transmit SOP* Message discarded Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B4	Transmit SOP* Message failed Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B3	Received Hard Reset Message Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked (The Hard Reset should generally not be masked)
B2	Receive SOP* Message Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B1	Power Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B0	CC Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked

7.2.8 POWER_STATUS_MASK (14h)

Table 16. POWER_STATUS_MASK Register

Bit(s)	Name	Type	Reset Value	Description
B7	Debug Accessory Connected Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B6	TCPC Initialization Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B5	Sourcing Nondefault Voltage Status Interrupt Mask	R	0b	0b: Interrupt masked 1b: Interrupt unmasked
B4	Sourcing VBUS Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B3	VBUS Detection Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B2	VBUS Present Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B1	VCONN Present Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B0	Sinking VBUS Status Interrupt Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked

7.2.9 FAULT_STATUS_MASK (15h)

Table 17. FAULT_STATUS_MASK Register[1]

Bit(s)	Name	Type	Reset Value	Description
B7	AllRegistersResetTo Default	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked The condition that generates AllRegistersResetToDefault Interrupt also resets this bit; therefore, writing a 0b to this bit does not mask AllRegistersResetToDefault Interrupt.
B6	Reserved	R	0b	Set to zero by sender and ignored by receiver.
B5	Auto Discharge Failed Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B4	Force Discharge Failed Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B3	VBUS Overcurrent Protection Fault Interrupt Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B2	VBUS Overvoltage Protection Fault Interrupt Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B1	Vconn Overcurrent Fault Interrupt Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked
B0	I^2C Interface Error Interrupt Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked

1. VBUS_RVP, VBUS_UVP, VCONN_RVP, VCONN_UVP, VCONN_OVP, and VCONN_OTP are masked in Table 66.

7.2.10 EXTENDED_STATUS_MASK (16h)

Table 18. EXTENDED_STATUS_MASK Register

Bit(s)	Name	Type	Reset Value	Description
B7..1	Reserved	R	0000000b	Set to zero by sender and ignored by receiver.
B0	vSafe0V Status Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked

7.2.11 ALERT_EXTENDED_MASK (17h)

Table 19. ALERT_EXTENDED_MASK Register

Bit(s)	Name	Type	Reset Value	Description
B7...1	Reserved	R	00000b	Set to zero by sender and ignored by receiver.
B0	Sink Fast Role Swap Mask	R/W	1b	0b: Interrupt masked 1b: Interrupt unmasked

7.2.12 TCPC_CONTROL (19h)

Table 20. TCPC_CONTROL Register

Bit(s)	Name	Type	Reset Value	Description
B7	Enable SMBus PEC	R	0b	0b: SMBus PEC is disabled (default)
B6	Enable Looking4Connection Alert	R/W	0b	0b: Disable ALERT.CCStatus assertion when CC_STATUS.Looking4Connection changes (default) 1b: Enable ALERT.CCStatus assertion when CC_STATUS.Looking4Connection changes
B5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
B4	Debug Accessory Control	R/W	0b	0b: Controlled by TCPC (power on default) 1b: Controlled by TCPM. This bit no effect to any function, always it controlled by TCPC.
B3..2	I^2C Clock Stretching Control	R	00b	Clock Stretching Control 00b: Disable clock stretching. TCPC does not perform any clock stretching during I^2C transfers.

Table 20. TCPC_CONTROL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
B1	BIST Test Mode	R/W	0b	Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the TCPC. The TCPM should clear this bit when a disconnect is detected. 0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT (2Fh) passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT (2Fh) result in GoodCRC response but might not be passed to the TCPM through Alert. TCPC does not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
B0	Plug Orientation	R/W	0b	0b: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. TCPM needs to set this bit to oriented position. If TCPM does not set this bit to oriented position, TCPC cannot transmit and receive any messages.

7.2.13 ROLE_CONTROL (1Ah)

Table 21. ROLE_CONTROL Register

Bit(s)	Name	Type	Reset Value	Description
B7	Reserved	R	0b	Set to zero by sender and ignored by receiver.
B6	DRP	R/W	0b	0b: No DRP. Bits B3..0 determine Rp/Rd/Ra or open settings 1b: DRP. The TCPC uses the Rp value defined in B5..4 when a connection is resolved, that is upon entry to Potential_Connect_as_Src in Figure 4-19 of TCPCI specification. The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, TCPC resolves to either an Rp or Rd and report the CC1/CC2 State in CC_STATUS Register The CC pins stay in Potential_Connect_as_Src or Potential_Connect_as_Sink until directed otherwise.
B5..4	Rp Value	R/W	00b	00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved When TCPC connects works as VBUS source, this field can be updated.
B3..2	CC2	R/W	10b or 11b	00b: Not supported 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) If TCPM sets this fields to 00b, it is not effect for CC2. TCPM needs to set this bit based on TCPCI specification. In connected case, TCPC controls CC lines by USB Type-C State. TCPM needs to control USB Type-C state machine correctly, for example, power role swap, error recovery, or others When the TCPC is powered up by VBUS, the reset value of this bit is 10b. When the TCPC is powered up by VSYS33, the reset value of this bit is 11b.
B1..0	CC1	R/W	10b or 11b	00b: Not supported 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) If TCPM sets this fields to 00b, it is not effect for CC1. When the TCPC is powered up by VBUS, the reset value of this bit is 10b. When the TCPC is powered up by VSYS33, the reset value of this bit is 11b.

7.2.14 FAULT_CONTROL (1Bh)

Table 22. FAULT_CONTROL Register[1]

Bit(s)	Name	Type	Reset Value	Description
B7..4	Reserved	R	0000b	Set to zero by sender and ignored by receiver.
B3	VBUS Discharge Fault Detection Timer	R/W	0b	0b: VBUS Discharge Fault Detection Timer enabled 1b: VBUS Discharge Fault Detection Timer disabled This enables the timers for both FAULT_STATUTS.AutoDischargeFailed and FAULT_STATUS.ForceDischargeFailed
B2	VBUS Overcurrent Protection Fault	R/W	0b	0b: Internal OCP circuit enabled 1b: Internal OCP circuit disabled If OCP occurs when this bit is set to 0b, RAA489400 turns off VBUS gate and sets FAULT_STATUS Register. See VBUS Overcurrent Protection for more information.
B1	VBUS Overvoltage Protection Fault	R/W	0b	0b: Internal OVP circuit enabled 1b: Internal OVP circuit disabled If OVP occurs when this bit is set to 0b, RAA489400 turns off VBUS gate and sets FAULT_STATUS (1Fh). See VBUS Overvoltage Protection for more information.
B0	VCONN Overcurrent Fault	R/W	0b	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled If VCONN OCP occurs when this bit is set to 0b, RAA489400 turns off VCONN Mux and sets FAULT_STATUS Register. See VCONN Overcurrent Protection for more information. Regardless of this setting, if RAA489400 detects VCONN overcurrent, RAA489400 turns off VCONN Mux.

1. VBUS_RVP and VBUS_UVP are controlled in Table 67. VCONN_OTP is controlled in Table 68.

7.2.15 POWER_CONTROL (1Ch)

Table 23. POWER_CONTROL Register

Bit(s)	Name	Type	Reset Value	Description
B7	Fast Role Swap Enable	R/W	0b	0b: Disable Fast Role Swap function 1b: Enable Fast Role Swap function Note: When this bit is set to 1b, VSRC_CP_EN is required to set to 1b in VBUS_CP_CTRL Register
B6	VBUS_VOLTAGE Monitor	R/W	1b	0b: VBUS_VOLTAGE Monitoring is enabled 1b: VBUS_VOLTAGE Monitoring is disabled (default) Controls only VBUS_VOLTAGE Monitoring function. VBUS_VOLTAGE (70h) reports all zeroes if disabled.
B5	Disable Voltage Alarms	R/W	1b	0b: Voltage Alarms Power status reporting is enabled 1b: Voltage Alarms Power status reporting is disabled (default) Controls VBUS_VOLTAGE_ALARM_HI_CFG (76h) and VBUS_VOLTAGE_ALARM_LO_CFG (78h).
B4	Auto Discharge Disconnect	R/W	0b	0b: The TCPC does not automatically discharge VBUS based on VBUS voltage (default) 1b: The TCPC automatically discharges. Setting this bit in a Source TCPC triggers the following actions upon a disconnect detection: 1. Disable sourcing power over VBUS 2. VBUS discharge Sourcing power over VBUS is disabled before or at the same time as starting VBUS discharge. Setting this bit in a Sink TCPC triggers the following action upon a disconnect detection: 1. VBUS discharge The TCPC automatically disables discharge (without clearing this bit) once the voltage on VBUS is below vSafe0V (max). TCPC does not re-apply discharge circuit if VBUS rises above vSafe0V.
B3	Enable Bleed Discharge	R/W	0b	0b: Disable bleed discharge of VBUS (default) 1b: Enable bleed discharge of VBUS
B2	Force Discharge	R/W	0b	0b: Disable forced discharge (default) 1b: Enable forced discharge of VBUS. Refer to Section 4.4.5.4.3 in TCPCI specification for more detail.
B1	VCONN Power Supported	R	1b	0b: Deliver at least 1W on VCONN 1b: Deliver at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported. VCONN OCP settings are provided in VCONN_FAULT_CTRL Register (A6h). 00 = 400mA 01 = 600mA 10 = 800mA 11 = Reserved
B0	Enable VCONN	R/W	0b	0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC

7.2.16 CC_STATUS (1Dh)

Table 24. CC_STATUS Register

Bit(s)	Name	Type	Reset Value	Description
B7..6	Reserved	R	00b	Set to zero by sender and ignored by receiver
B5	Looking4Connection	R	0b	0b: TCPC is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found. 1b: TCPC is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)
B4	ConnectResult	R	0b	0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd TCPC updates this bit when Looking4Connection change to 0 from 1.

B3..2	CC2 State	R	00b	If (ROLE_CONTROL.CC2 = Rp) or (ConnectResult = 0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: Reserved
				
				If (ROLE_CONTROL.CC2 = Rd) or (ConnectResult = 1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
				
				If ROLE_CONTROL.CC2 = Ra, this field is set to 00b
				If ROLE_CONTROL.CC2 = Open, this field is set to 00b
				
				This field always returns 00b if (Looking4Connection = 1) or (POWER_CONTROL.EnableVconn = 1 and TCPC_CONTROL.PlugOrientation=0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

Table 24. CC_STATUS Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description

B1..0	CC1 State	R	00b	If (ROLE_CONTROL.CC1 = Rp) or (ConnectResult=0)
				00b: SRC.Open (Open, Rp)
				01b: SRC.Ra (below maximum vRa)
				10b: SRC.Rd (within the vRd range)
				11b: Reserved
				
				If (ROLE_CONTROL.CC1 = Rd) or ConnectResult = 1)
				00b: SNK.Open (Below maximum vRa)
				01b: SNK.Default (Above minimum vRd-Connect)
				10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
				11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
				
				If ROLE_CONTROL.CC1=Ra, this field is set to 00b
				If ROLE_CONTROL.CC1=Open, this field is set to 00b
				
				This field always returns 00b if (Looking4Connection = 1) or (POWER_CONTROL.EnableVconn = 1 and TCPC_CONTROL.PlugOrientation = 1). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

7.2.17 POWER_STATUS (1Eh)

Table 25. POWER_STATUS Register

Bit(s)	Name	Type	Reset Value	Description
B7	Debug Accessory Connected	R	0b	0b: No Debug Accessory connected (default) 1b: Debug Accessory connected TCPC asserts this bit when it transitions to Debug Accessory state. If TCPC detects disconnected, this bit is de-asserted. TCPC detects Rd and Rd or Rp and Rp on Apply State. If the TCPC detects DebugAccessory device with tCCDebounce, it transitions to DebugAccessory.SRC or SNK.
B6	TCPC Initialization Status	R	1b	0b: The TCPC has completed initialization and all registers are valid 1b: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h...0Fh TCPC clears this field and asserts ALERT.POWER_STATUS after TCPC completes initialization of VBUS detection and the first VBUS detection.
B5	Sourcing Nondefault Voltage	R	0b	0b: vSafe5V (Fixed).
B4	Sourcing VBUS	R	0b	0b: Sourcing VBUS is disabled 1b: Sourcing VBUS is enabled This bit does not control the path, just provides a monitor of the status. RAA489400 controls this bit with based on a command and an event (for example, disconnection, and FRS) and indicates that Sourcing VBUS is in progress.
B3	VBUS Detection Enabled	R	1b	0b: VBUS Detection Disabled 1b: VBUS Detection Enabled (default) Indicates whether the TCPC is monitoring for VBUS Present and vSafe0V level. After Power-on reset, VBUS detection is enabled automatically.
B2	VBUS Present	R	0b	0b: VBUS Disconnected 1b: VBUS Connected TCPC asserts VBUS_present when TCPC detects VBUS rises above VBUS_OK_r for more than 1ms. TCPC de-asserts VBUS_present when TCPC detects VBUS falls below VBUS_OK-r – VBUS_OK_h for more than 10µs. In Sink mode, deasserting this bit does not mean Sink Disconnect. Deasserting this bit is independent from VBUS Sink Disconnect which is detected when VBUS voltage is below VBUS_SINK_DISCONNECT_THRESHOLD register.
B1	VCONN Present	R	0b	0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V TCPC de-asserts this bit when TCPC detects VBUS falls below 2.4V. When EnableVCONN is disabled in POWER_CONTROL (1Ch), this bit indicates 0b.
B0	Sinking VBUS	R	0b	0b: Sink is Disconnected 1b: TCPC is sinking VBUS to the system load RAA489400 controls this bit with based on a command and an event (for example, disconnect or FRS) and indicates that Sinking VBUS is in progress.

7.2.18 FAULT_STATUS (1Fh)

Table 26. FAULT_STATUS Register

Bit(s)	Name	Type	Reset Value	Description
B7	AllRegistersResetTo Default	R/W1C	1b	This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.
B6	Reserved	R	0b	Set to zero by sender and ignored by receiver
B5	Auto Discharge Failed	R/W1C	0b	0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.AutoDischargeDisconnect is set, the TCPC reports discharge fails if VBUS is not below vSafe0V within tSafe0V.
B4	Force Discharge Failed	R/W1C	0b	0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.ForceDischarge is set, the TCPC reports a discharge fails if VBUS is not below vSafe0V within tSafe0V.
B3	VBUS Overcurrent Protection Fault	R/W1C	0b	0b: Not in an overcurrent protection state 1b: Overcurrent fault latched If VBUS current exceeds VBUS_OC setting in. See VBUS Overcurrent Protection for more information. This bit remains 1b even if TCPM writes 1b to this bit when VBUS Overcurrent condition still occurs.
B2	VBUS Overvoltage Protection Fault	R/W1C	0b	0b: Not in an overvoltage protection state 1b: Overvoltage fault latched. See VBUS Overvoltage Protection for more information. This bit remains 1b even if TCPM writes 1b to this bit when VBUS Overvoltage condition still occurs.
B1	VCONN Overcurrent Fault	R/W1C	0b	0b: No Fault detected 1b: Overcurrent VCONN fault latched. This bit remains 1b even if TCPM writes 1b to this bit when VCONN Overcurrent condition still occurs.
B0	I^2C Interface Error	R/W1C	0b	0b: No Error 1b: I^2C error has occurred. When the following conditions occur, this bit is asserted TCPM writes to the TRANSMIT register that is not HardReset, CableReset or BIST Carrier Mode 2 when the TRANSMIT_BUFFER is empty has less than 2 bytes I2C_WRITE_BYTE_COUNT is different than the number of bytes written in the TRANSMIT_BUFFER. Main State-Machine has entered Connected_Invalid state TCPM writes an invalid COMMAND DisableVbusDetect command when TCPC sourcing or sinking power over VBUS. SinkVbus command when TCPC is sourcing power over VBUS. SourceVbusDefaultVoltage command when TCPC sinking power over VBUS. SourceVbusNondefaultVoltage command SendFRSwapSignal command Value written to COMMAND register is not defined in the TCPCI spec.

Note: VBUS_RVP, VBUS_UVP, VCONN_RVP, VCONN_UVP, VCONN_OVP, and VCONN_OTP are reported in Table 65.

7.2.19 EXTENDED_STATUS (20h)

Table 27. EXTENDED_STATUS Register

Bit(s)	Name	Type	Reset Value	Description
B7..1	Reserved	R	0000000b	Set to zero by sender and ignored by receiver
B0	vSafe0V	R	1b	0b: VBUS is not at vSafe0V 1b: VBUS is at vSafe0V TCPC reports VBUS is at vSafe0V when TCPC detects VBUS is below 0.8V. This bit is not valid when VbusDetectionEnabled = 0b in POWER_STATUS (1Eh)

7.2.20 ALERT_EXTENDED (21h)

Table 28. ALERT_EXTENDED Register

Bit(s)	Name	Type	Reset Value	Description
B7..1	Reserved	R	00000000b	Set to zero by sender and ignored by receiver
B0	Sink Fast Role Swap	R/W1C	0b	0b: No Fast Role Swap signal received 1b: Fast Role Swap signal received When FRS_EN is set to 1b in PROCHOT_EN register and this bit is set to one, PROCHOT# is asserted Writing one to this bit clears the bit to zero. If bit 0 of this register and bit 1 of Vendor_STATUS register are zero, PROCHOT# is deasserted (Hi-Z).

7.2.21 COMMAND (23h)

Table 29. COMMAND Register

Bit(s)	Name	Type	Reset Value	Description
B7..0	Command	W	00h	Refer to Table 30.

Table 30. COMMAND Register Setting

Register Setting	Description
0001 0001b	**WakeI2C** (no action is taken other than to wake the I^2C interface).
0010 0010b	**DisableVbusDetect.** Disable VBUS present and vSafe0V detection. The TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing or sinking power over VBUS enabled. If the TCPC received this command validly, TCPC clear the POWER_STATUS.VBUS Detection Enable.
0011 0011b	**EnableVbusDetect.** Enable VBUS present and vSafe0V detection. If TCPC received this command, TCPC sets POWER_STATUS.VBUS Detection Enable after update VBUS present and vSafe0V to latest status and it can notify the ALERT for POWER_STATUS.VBUS_present and EXTENDED_STATUS.vSafe0V.

Table 30. COMMAND Register Setting (Cont.)

Register Setting	Description
0100 0100b	**DisableSinkVbus.** Disable sinking power over VBUS but does not discharge VBUS to vSafe0V. If VBUS has not been discharged at Sink detach, for example, Auto Disconnect Discharge is set to 0b, TCPM needs to use Force Discharge in addition to the DisableSinkVbus command. This COMMAND does not disable POWER_STATUS.VBUSPresent detection. The TCPC clears FAULT_STATUS.InternalorExternalOCP, FAULT_STATUS.InternalorExternalOVP, and VENDOR_STATUS register except Bit9.VCONN_0p8V, Bit5.FAULT_STATE, Bit15.Sink path discharge timeout, and Bit14. Sink path discharge complete (B14). The TCPC turn off VBus Sink path gate (Nch-MOSFET with VSNK_GATE or external component with GPIO (Sink Enable function).
0101 0101b	**SinkVbus.** Enable sinking power over VBUS and enable VBus present detection. The TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing power over Vbus enabled. The TCPC turn on VBus Sink path gate (Nch-MOSFET with VSNK_GATE or external component with GPIO (Sink Enable function) and stop VBUS discharge. If TCPC received this command, TCPC completes setting charging and loading of VBUS. When TCPC detects VBUS removed, TCPC controls a discharge circuit If TCPM has set POWER_CONTROL.Auto Discharge Disconnect to 1. Also, when TCPC detects SNK.Open specified in SNK_DETACH register, TCPC controls a discharge circuit If TCPM has set SNK_DETACH.AUTO_DISCHG_SNK_OPEN to 1. So TCPM does not require to write a COMMAND.DisableSinkVbus when TCPC has detect remover the VBUS.
0110 0110b	**DisableSourceVbus.** Disable sourcing power over VBUS. The TCPC clears FAULT_STATUS.InternalorExternalOCP, FAULT_STATUS.InternalorExternalOVP, and VENDOR_STATUS register except Bit9.VCONN_0p8V, Bit5.FAULT_STATE, Bit15.Sink path discharge timeout and Bit14.Sink path discharge complete (B14). This COMMAND does not disable POWER_STATUS.VBUSPresent detection. The TCPC turns off VBus Source path gate (Nch-MOSFET with VSRC_GATE or external component with GPIO (Source Enable function) and discharges VBUS voltage to vSafe0V.
0111 0111b	**SourceVbusDefaultVoltage.** Enable sourcing vSafe5V over VBUS and enable VBus present detection. Source transitions to vSafe5V if at a high voltage. The TCPC ignores this command and assert the FAULT_STATUS.I2CInterfaceError if it has sinking power over Vbus enabled. The TCPC turns on the VBus Source path gate (Nch-MOSFET with VSRC_GATE) or external component with GPIO (Source Enable function) and stops VBUS discharge.
1000 1000b	**SourceVbusNondefaultVoltage.** RAA489400 does not support this command. When RAA489400 receives this command, this command is ignored and the FAULT_STATUS.I2CInterfaceError is set to 1b.
1001 1001b	**Look4Connection.** Start DRP Toggling if ROLE_CONTROL.DRP = 1b. If ROLE_CONTROL.CC1/CC2= 01b start with Rp, if ROLE_CONTROL.CC1/CC2 =10b start with Rd. If ROLE_CONTROL.CC1/CC2 are not both 01b or 10b, then do not start toggling. The TCPM issues COMMAND.Look4Connection to enable the TCPC to restart Connection Detection in cases where the ROLE_CONTROL contents do not change. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case a Source Only or DRP should go back to its Unattached.Src state. This would result in ROLE_CONTROL staying the same.

Table 30. COMMAND Register Setting (Cont.)

Register Setting	Description
1010 1010b	**RxOneMore.** Configure the receiver to automatically clear the RECEIVE_DETECT (2Fh) after sending the next GoodCRC. This is used to shutdown reception of packets at a known point regardless of packet separation or the depth of the receive FIFO in the TCPC.
1100 1100b	**SendFRSwapSignal.** RAA489400 does not support this command. When RAA489400 receives this command, this command is ignored and the FAULT_STATUS.I2CInterfaceError is set to 1b.
1101 1101b	**ResetTransmitBuffer.** The TCPC resets the pointer of the TRANSMIT_BUFFER register to offset 1 and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TCPM. This command is supported by TCPC compliant with USB Port Controller Specification Revision 2.0.
1110 1110b	**ResetReceiveBuffer.** The TCPC resets the pointer of RX_BUFFER when this command is issued by the TCPM. TCPC does not clear the content of the buffer upon receiving this command. The TCPM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x. This command is supported by TCPC compliant with USB Port Controller Specification Revision 2.0.
1111 1111b	I2C Idle RAA489400 does not support. No action is taken.

7.2.22 DEVICE_CAPABILITIES_1 (24h)

Table 31. DEVICE_CAPABILITIES_1 Register

Bit(s)	Name	Type	Reset Value	Description
B15	VBUS Nondefault Target	R	0b	0b: VBUS_NONDEFAULT_TARGET register not implemented 1b: VBUS_NONDEFAULT_TARGET register implemented
B14	VBUS OCP Reporting	R	1b	0b: VBUS OCP is not reported by the TCPC 1b: VBUS OCP is reported by the TCPC
B13	VBUS OVP Reporting	R	1b	0b: VBUS OVP is not reported by the TCPC 1b: VBUS OVP is reported by the TCPC
B12	Bleed Discharge	R	1b	0b: No Bleed Discharge implemented in TCPC 1b: Bleed Discharge is implemented in the TCPC
B11	Force Discharge	R	1b	0b: No Force Discharge implemented in TCPC 1b: Force Discharge is implemented in the TCPC
B10	VBUS Measurement and Alarm Capable	R	1b	0b: No VBUS voltage measurement nor VBUS Alarms 1b; VBUS voltage measurement and VBUS Alarms
B9..8	Source Resistor Supported	R	10b	00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3.0A, 1.5A, and default 11b: Reserved Rp values which can be configured by the TCPM with ROLE_CONTROL (1Ah)
B7..5	Power Roles Supported	R	110b	000b: USB Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP only 101b: Source, Sink, DRP, Adapter/Cable all supported 110b: Source, Sink, DRP 111b: Not valid

Table 31. DEVICE_CAPABILITIES_1 Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
B4	SOP'_DBG/SOP"_DBG Support	R	1b	0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported Configured in RECEIVE_DETECT (2Fh) and TRANSMIT (50h).
B3	Source VCONN	R	1b	0b: TCPC is not capable of switching the VCONN Source 1b: TCPC is capable of switching the VCONN Source
B2	Sink VBUS	R	1b	0b: TCPC is not capable controlling the sink path to the system load 1b: TCPC is capable of controlling the sink path to the system load
B1	Source Nondefault VBUS	R	0b	0b: TCPC is not capable of sourcing nondefault voltages over VBUS 1b: TCPC is capable of sourcing nondefault voltages over VBUS
B0	Source VBUS	R	1b	0b: TCPC is not capable of controlling the source path to VBUS 1b: TCPC is capable of controlling the source path to VBUS

7.2.23 DEVICE_CAPABILITIES_2 (26h)

Table 32. DEVICE_CAPABILITIES_2 Register

Bit(s)	Name	Type	Reset Value	Description
B15	DEVICE_CAPABILITIES_3 Support	R	1b	0b: TCPC does not support the DEVICE_CAPABILITIES_3 register. 1b: TCPC supports the DEVICE_CAPABILITIES_3 register.
B14	Message Disable Disconnect	R	1b	0b: Sink TCPC disables PD message delivery when ALERT.VbusinkDisconnectDetected has been asserted 1b: Sink TCPC disables PD message delivery using the condition as defined in RECEIVE_DETECT.MessageDisableDisconnect
B13	Generic Timer	R	0b	0b: GENERIC_TIMER register is not supported 1b: GENERIC_TIMER register is supported
B12	Long Message	R	0b	0b: RAA489400 does not support long message but RAA489400 can transfer and receive EPR protocol as unchunked message
B11	SMBus PEC	R	0b	0b: TCPC_CONTROL.EnableSMBusPEC not implemented 1b: TCPC_CONTROL.EnableSMBusPEC implemented
B10	Source FR Swap	R	0b	0b: Not capable of sending Fast Role Swap signal as Source when receiving COMMAND.SendFRSwapSignal. 1b: Capable of sending Fast Role Swap signal as Source TCPC when receiving COMMAND.SendFRSwapSignal.
B9	Sink FR Swap	R	1b	0b: POWER_CONTROL.FastRoleSwapEnable not supported as Sink 1b: POWER_CONTROL.FastRoleSwapEnable supported as Sink
B8	Watchdog Timer	R	0b	0b: TCPC_CONTROL.EnableWatchdogTimer not implemented 1b: TCPC_CONTROL.EnableWatchdogTimer implemented

Table 32. DEVICE_CAPABILITIES_2 Register (Cont.)

B7	Sink Disconnect Detection	R	1b	0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented, use POWER_STATUS.VbusPresent=0b to indicate a Sink disconnect. 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented, VBUS falling below VBUS_SINK_DISCONNECT_THRESHOLD is used as indication of Sink disconnect.
B6	Stop Discharge Threshold	R	1b	0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented
B5..4	VBUS Voltage Alarm LSB	R	00b	The TCPC might ignore the number of Least Significant Bits (LSBs) of 4 Threshold and Alarm registers as denoted in this field. Whether or not the TCPC ignores these might be dependent on the instantaneous Voltage of VBus. The TCPM can use this information to round up or down the affected registers as appropriate. The registers affected are: VBUS_SINK_DISCONNECT_THRESHOLD, VBUS_STOP_DISCHARGE_THRESHOLD, VBUS_VOLTAGE_ALARM_HI_CFG, and VBUS_VOLTAGE_ALARM_LO_CFG. 00: TCPC always has 25mV LSB for its voltage alarms and thresholds and uses all bits defined. 01: TCPC might have 50mV LSB for its voltage alarm and might ignore the least significant bit. 10: TCPC might have 100mV LSB for its voltage alarm and might ignore the two least significant bits. 11: Reserved This field is ignored if VBUS_VOLTAGE_ALARM_LO_CFG and VBUS_VOLTAGE_ALARM_HI are not supported.
B3..1	VCONN Power Supported	R	001b	000b: 1.0W 001b: 1.5W 010b: 2.0W 011b: 3W 100b: 4W 101b: 5W 110b: 6W 111b: External
B0	VCONN Overcurrent Fault Capable	R	1b	0b: TCPC is not capable of detecting a VCONN overcurrent fault 1b: TCPC is capable of detecting a VCONN overcurrent fault

7.2.24 STANDARD_INPUT_CAPABILITIES (28h)

Table 33. STANDARD_INPUT_CAPABILITIES Register

Bit(s)	Name	Type	Reset Value	Description
B7..5	Reserved	R	000b	Set to zero by sender and ignored by receiver
B4..3	Source Fast Role Swap	R	00b	00b: Not present in TCPC 01b: Present in TCPC as an input only pin 10b: Present in TCPC as a bidirectional pin, sharing with the STANDARD OUTPUT SIGNAL VBUS Sink Disconnect Detect Indicator. 11b: Reserved
B2	VBUS External Overvoltage Fault	R	0b	0b: Not present in TCPC 1b: Present in TCPC
B1	VBUS External Overcurrent Fault	R	1b	0b: Not present in TCPC 1b: Present in TCPC GPIO1/2/3/4_CTRL, VBUS_PATH_CTRL, VBUS_GPIO_CTRL, and GPIO_OC_EN register need to be set to enable.
B0	Force Off VBUS (Source or Sink)	R	0b	0b: Not present in TCPC 1b: Present in TCPC

7.2.25 STANDARD_OUTPUT_CAPABILITIES (29h)

Table 34. STANDARD_OUTPUT_CAPABILITIES Register

Bit(s)	Name	Type	Reset Value	Description
B7	VBUS Sink Disconnect Detect Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
B6	Debug Accessory Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC RAA489400 does not support Debug Accessory Indicator output pin function. RAA489400 supports Debug Accessory connection status.
B5	VBUS Present Monitor	R	0b	0b: Not present in TCPC 1b: Present in TCPC
B4	Audio Adapter Accessory Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
B3	Active Cable Indicator	R	0b	0b: Not present in TCPC 1b: Present in TCPC
B2	MUX Configuration Control	R	0b	0b: Not present in TCPC 1b: Present in TCPC
B1	Connection Present	R	0b	0b: No Connection 1b: Connection Controlled by the TCPM.
B0	Connector Orientation	R	0b	0b: Not present in TCPC 1b: Present in TCPC

7.2.26 MESSAGE_HEADER_INFO (2Eh)

Table 35. MESSAGE_HEADER_INFO Register

Bit(s)	Name	Type	Reset Value	Description
B7..5	Reserved	R	000b	Set to zero by sender and ignored by receiver.
B4	Cable Plug	R/W	0b	0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
B3	Data Role	R/W	0b	0b: UFP 1b: DFP
B2..1	USB PD Specification Revision	R/W	10b	00b: Revision 1.0 01b: Revision 2.0 10b: Revision 3.0 11b: Reserved
B0	Power Role	R/W	0b	0b: Sink 1b: Source

7.2.27 RECEIVE_DETECT (2Fh)

Table 36. RECEIVE_DETECT Register

Bit(s)	Name	Type	Reset Value	Description
B7	Message Disable Disconnect	R/W	0b	0b: Sink TCPC disables PD message delivery when Auto Discharge Disconnect is set in POWER CONTROL register and VBUS voltage falls below VBUS SINK DISCONNECT THRESHOLD register, that is VBUS Sink disconnect is detected (default) TCPM needs to set 0b in this bit. Regardless of the setting of this bit, Source TCPC always uses SRC.Open as an indication of disconnect to disable PD message delivery. The TCPC clears the RECEIVE_DETECT and READABLE_BYTE_COUNT registers to disable the PD message delivery.
B6	Enable Cable Reset	R/W	0b	0b: TCPC does not detect Cable Reset signaling (default) 1b: TCPC detects Cable Reset signaling
B5	Enable Hard Reset	R/W	0b	0b: TCPC does not detect Hard Reset signaling (default) 1b: TCPC detects Hard Reset signaling
B4	Enable SOP_DBG” message	R/W	0b	0b: TCPC does not detect SOP_DBG” message other than SOP_DBG" GoodCRC messages received by the sending process (default) 1b: TCPC detects SOP_DBG” message
B3	Enable SOP_DBG’ message	R/W	0b	0b: TCPC does not detect SOP_DBG’ message other than SOP_DBG' GoodCRC messages received by the sending process (default) 1b: TCPC detects SOP_DBG’ message
B2	Enable SOP’’ message	R/W	0b	0b: TCPC does not detect SOP’’ message other than SOP" GoodCRC messages received by the sending process (default) 1b: TCPC detects SOP’’ message

Table 36. RECEIVE_DETECT Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
B1	Enable SOP' message	R/W	0b	0b: TCPC does not detect SOP' message other than SOP' GoodCRC messages received by the sending process (default) 1b: TCPC detects SOP' message
B0	Enable SOP message	R/W	0b	0b: TCPC does not detect SOP message other than SOP GoodCRC messages received by the sending process (default) 1b: TCPC detects SOP message

7.2.28 READABLE_BYTE_COUNT (30h)

Table 37. READABLE_BYTE_COUNT

Bit(s)	Name	Type	Reset Value	Description
B7..0	READABLE_BYTE_ COUNT	R	00h	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). The content of this register is undefined when the RECEIVE_BUFFER is cleared. The value in this register is less than or equal to 81 in the case of supporting the proprietary long message or 133 in the case of supporting the TCPCI standard long message.

7.2.29 RX_BUF_FRAME_TYPE

Table 38. RX_BUF_FRAME_TYPE

Bit(s)	Name	Type	Reset Value	Description
B7..3	Reserved	R	00000b	Set to zero by sender and ignored by receiver.
B2..0	Received SOP* Message	R	000b	000b: Received SOP 001b: Received SOP' 010b: Received SOP'' 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved.

7.2.30 RX_BUF_BYTE_x

Table 39. RX_BUFFER_DATA Register

Bit(s)	Name	Type	Reset Value	Description
B7..0	Rx Buffer	R	00h	The TCPM reads the READABLE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_DATA. The TCPM then reads the content of the USB PD message in RX_BUFFER_DATA.

7.2.31 TRANSMIT (50h)

Table 40. TRANSMIT Register

Bit(s)	Name	Type	Reset Value	Description
B7..6	Reserved	R	00b	Set to zero by sender and ignored by receiver.
B5..4	Retry Counter	R/W	00b	00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
B3	Reserved	R	0b	Set to zero by sender and ignored by receiver.
B2..0	Transmit SOP* message	R/W	000b	000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP'' 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (TCPC exit the BIST mode no later than tBISTContMode max)

Note: TCPM needs to set non-zero value to RECEIVE_DETECT register prior to transmit any PD Message, Hard Reset, Cable Reset, or BIST Carrier Mode.

7.2.32 I2C_WRITE_BYTE_COUNT

Table 41. I2C_WRITE_BYTE_COUNT

Bit(s)	Name	Type	Reset Value	Description
B7..0	I2C_WRITE_BYTE_ COUNT	W	00h	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I^2C/SMBus transaction.

7.2.33 TX_BUFFER_BYTE_x

Table 42. TX_BUFFER_DATA Register

Bit(s)	Name	Type	Reset Value	Description
B7..0	Tx Buffer	W	00h	The TCPM writes to this register to transmit a SOP* message where the SOP* message payload (that is the header bytes and the data bytes) was written into the TCPC's internal transmit buffer using the TX_BUFFER_DATA register. The value in this register is less than or equal to 80 in the case of supporting the proprietary long message or 132 in the case of supporting the TCPCI standard long message.

7.2.34 VBUS_VOLTAGE (70h)

Table 43. VBUS_VOLTAGE Register

Bit(s)	Name	Type	Reset Value	Description
B15..12	Reserved	R	0000b	Set to zero by sender and ignored by receiver.
B11..10	Scale Factor	R	00b	00: VBUS measurement not scaled. 01: VBUS measurement divided by 2 10: VBUS measurement divided by 4 11: reserved This fields fixed to 00b.
B9..0	VBUS voltage measurement	R	0000000000b	10-bit measurement of (VBUS / Scale Factor) TCPM multiplies this value by the scale factor to obtain the voltage measurement. All voltages shows ±2% absolute value or ±50mV, whichever is greater. The LSB is 25mV. When VBUS voltage is lower than 25.6V (25mV × 1024), the Scal Factor is 00b. When VBUS voltage is higher or equal to 25.6V and lower than 51.2V (50mV × 1024), the Scale Factor is 01b. When VBUS voltage is higher or equal to 51.2V, the Scale Factor is 10b. This fields fix to 10'h0 if POWER_CONTROL.VBUS_VOLTAGE monitor is one.

7.2.35 VBUS_SINK_DISCONNECT_THRESHOLD (72h)

Table 44. VBUS_SINK_DISCONNECT_THRESHOLD Register

Bit(s)	Name	Type	Reset Value	Description
B15...12	Reserved	R	0000b	Set to 0
B11..0	Voltage trip point	R/W	08Ch (3.5V)	12-bit for voltage threshold with 25mV LSB. (Default 3.5V) ±5% accuracy. A value of zero disables this threshold and Sink Auto VBUS Discharge. If 51.2V (200h) or higher is written, it is treated as 51.15V (1FFh).

7.2.36 VBUS_STOP_DISCHARGE_THRESHOLD (74h)

Table 45. VBUS_STOP_DISCHARGE_THRESHOLD Register

Bit(s)	Name	Type	Reset Value	Description
B15..12	Reserved	R	0000b	Set to 0
B11..0	Voltage trip point	R/W	020h (0.8V)	12-bit for voltage threshold with 25mV LSB. (Default 0.8V) ±5% accuracy.

7.2.37 VBUS_VOLTAGE_ALARM_HI_CFG (76h)

Table 46. VBUS_VOLTAGE_ALARM_HI_CFG Register

Bit(s)	Name	Type	Reset Value	Description
B15..12	Reserved	R	0000b	Set to 0
B11..0	Voltage trip point	R/W	000h (0V)	12-bit for voltage threshold with 25mV LSB. ±5% accuracy.

7.2.38 VBUS_VOLTAGE_ALARM_LO_CFG (78h)

Table 47. VBUS_VOLTAGE_ALARM_LO_CFG Register

Bit(s)	Name	Type	Reset Value	Description
B15..12	Reserved	R	0000b	Set to 0
B11..0	Voltage trip point	R/W	000h (0V)	12-bit for voltage threshold with 25mV LSB. ±5% accuracy.

7.2.39 DEVICE_CAPABILITIES_3 Register (7Ch)

Table 48. DEVICE_CAPABILITIES_3 Register

Bit(s)	Name	Type	Reset Value	Description
B15:3	Reserved	R	0	Set to zero by sender and ignored by receiver.
B2:0	VBUS Voltage Support	R	110b	RAA489400 supports 48V VBUS measurement in the TCPC VBUS Threshold and Alarm registers: VBUS_SINK_DISCONNECT_THRESHOLD, VBUS_STOP_DISCHARGE_THRESHOLD, VBUS_VOLTAGE_ALARM_HI_CFG, and VBUS_VOLTAGE_ALARM_LO_CFG. 000b: 5 Volts* 001b: 9 Volts 010b: 15 Volts 011b: 20 Volts 100b: 28 Volts 101b: 36 Volts 110b: 48 Volts 111b: Reserved. *All voltages are Nominal

7.2.40 CHIP_REVISION register (80h)

Table 49. CHIP_REVISION Register

Bit(s)	Name	Type	Reset Value	Description
7:4	Major Revision Number	R	0001b	Major revision number
3:0	Minor Revision Number	R	0010b	Minor revision number

7.2.41 GPIO1_CTRL Register (82h)

Table 50. GPIO1_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
4	GPIO1_IE	R/W	0b	GPIO1 Input Enable 0b: GPIO1 input is disabled and GPIO1_I is held 0b regardless of GPIO1 pin condition. 1b: GPIO1 input is enabled.
3	GPIO1_OD_N	R/W	0b	GPIO1 Push-pull / Open-drain select 0b: GPIO1 output is open-drain. 1b: GPIO1 output is push-pull.
2	GPIO1_OE	R/W	0b	GPIO1 Output Enable 0b: GPIO1 output is disabled and Hi-Z. 1b: GPIO1 output is enabled and pin state follows setting of GPIO1_O.
1	GPIO1_O	R/W	0b	GPIO1 Output Data 0b: GPIO1 pin is driven low. 1b: GPIO1 pin is driven high (GPIO1_OD_N=1b) or Hi-Z (GPIO1_OD_N=0b).
0	GPIO1_I	R	0b	GPIO1 Input Data 0b: GPIO1 pin input state is low. 1b: GPIO1 pin input state is high. GPIO1_OE should be 0b when reading GPIO1 pin state, which is driven by external device. When GPIO1_OE is 1b, driven data by GPIO1_O can be read back.

7.2.42 GPIO2_CTRL Register (83h)

Table 51. GPIO2_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
4	GPIO2_IE	R/W	0b	GPIO2 Input Enable 0b: GPIO2 input is disabled and GPIO2_I is held 0b regardless of GPIO2 pin. 1b: GPIO2 input is enabled
3	GPIO2_OD_N	R/W	0b	GPIO2 Push-pull / Open-drain select 0b: GPIO2 output is open-drain. 1b: GPIO2 output is push-pull.
2	GPIO2_OE	R/W	0b	GPIO2 Output Enable 0b: GPIO2 output is disabled and Hi-Z. 1b: GPIO2 output is enabled and pin state follows setting of GPIO2_O.

Table 51. GPIO2_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
1	GPIO2_O	R/W	0b	GPIO2 Output Data 0b: GPIO2 pin is driven low. 1b: GPIO2 pin is driven high (GPIO2_OD_N = 1b) or Hi-Z (GPIO2_OD_N = 0b).
0	GPIO2_I	R	0b	GPIO2 Input Data 0b: GPIO2 pin input state is low. 1b: GPIO2 pin input state is high. GPIO2_OE should be 0b when reading GPIO2 pin state, which is driven by external device. When GPIO2_OE is 1b, driven data by GPIO2_O can be read back.

7.2.43 GPIO3_CTRL Register (84h)

Table 52. GPIO3_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
4	GPIO3_IE	R/W	0b	GPIO3 Input Enable 0b: GPIO3 input is disabled and GPIO3_I is held 0b regardless of GPIO3 pin. 1b: GPIO3 input is enabled
3	GPIO3_OD_N	R/W	0b	GPIO3 Push-pull / Open-drain select 0b: GPIO3 output is open-drain. 1b: GPIO3 output is push-pull.
2	GPIO3_OE	R/W	0b	GPIO3 Output Enable 0b: GPIO3 output is disabled and Hi-Z. 1b: GPIO3 output is enabled and pin state follows setting of GPIO3_O.
1	GPIO3_O	R/W	0b	GPIO3 Output Data 0b: GPIO3 pin is driven low. 1b: GPIO3 pin is driven high (GPIO3_OD_N = 1b) or Hi-Z (GPIO3_OD_N = 0b).
0	GPIO3_I	R	0b	GPIO3 Input Data 0b: GPIO3 pin input state is low. 1b: GPIO3 pin input state is high. GPIO3_OE should be 0b when reading GPIO3 pin state which is driven by external device. When GPIO3_OE is 1b, driven data by GPIO3_O can be read back.

7.2.44 GPIO4_CTRL Register (85h)

Table 53. GPIO4_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
4	GPIO4_IE	R/W	0b	GPIO4 Input Enable 0b: GPIO4 input is disabled and GPIO4_I is held 0b regardless of GPIO4 pin. 1b: GPIO4 input is enabled
3	GPIO4_OD_N	R/W	0b	GPIO4 Push-pull / Open-drain select 0b: GPIO4 output is open-drain. 1b: GPIO4 output is push-pull.
2	GPIO4_OE	R/W	0b	GPIO4 Output Enable 0b: GPIO4 output is disabled and Hi-Z. 1b: GPIO4 output is enabled and pin state follows setting of GPIO4_O.
1	GPIO4_O	R/W	0b	GPIO4 Output Data 0b: GPIO4 pin is driven low. 1b: GPIO4 pin is driven high (GPIO4_OD_N = 1b) or Hi-Z (GPIO4_OD_N = 0b).
0	GPIO4_I	R	0b	GPIO4 Input Data 0b: GPIO4 pin input state is low. 1b: GPIO4 pin input state is high. GPIO4_OE should be 0b when reading GPIO4 pin state which is driven by external device. When GPIO4_OE is 1b, driven data by GPIO4_O can be read back.

7.2.45 VBUS_PATH_CTRL Register (86h)

Table 54. VBUS_PATH_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:5	VBUS_SRC_SEL	R/W	000b	VBUS Source Path Control Select 000b: VSRC_GATE 001b: GPIO1 010b: GPIO2 011b: GPIO3 100b: GPIO4 Others: Reserved It is ignored when VBUS_SRC_EN = 0b.
4	VBUS_SRC_EN	R/W	0b	VBUS Source Path Control Enable 0b: VBUS source path control is disabled. 1b: VBUS source path control is enabled.

Table 54. VBUS_PATH_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
3:1	VBUS_SNK_SEL	R/W	000b	VBUS Sink Path Control Select 000b: VSNK_GATE 001b: GPIO1 010b: GPIO2 011b: GPIO3 100b: GPIO4 Others: Reserved It is ignored when VBUS_SNK_EN = 0b.
0	VBUS_SNK_EN	R/W	0b	VBUS Sink Path Control Enable 0b: VBUS sink path control is disabled. 1b: VBUS sink path control is enabled.

7.2.46 VBUS_GPIO_CTRL Register (87h)

Table 55. VBUS_GPIO_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:6	Reserved	R	0b	Set to zero by sender and ignored by receiver.
5	EN_SRC	R/W	0b	GPIOn_O Setting of Enable Source Value of this bit is loaded to GPIOn_O where n is VBUS_SRC_SEL of VBUS_PATH_CTRL register, when VBUS Source Path is enabled, for example, receiving SourceVbusDefaultVoltage command, or detecting FRS VBUS ON condition. GPIOn_OE is set to one and GPIOn_OD_N is unchanged when GPIOn_O is loaded. Loaded values can be read from GPIOn_CTRL register. It is ignored when VBUS_SRC_SEL is 000b.
4	DIS_SRC	R/W	0b	GPIOn_O Setting of Disable Source Value of this bit is loaded to GPIOn_O where n is VBUS_SRC_SEL of VBUS_PATH_CTRL register, when VBUS Source Path is disabled, for example, receiving DisableSourceVbus command or detecting VBUS fault condition. GPIOn_OE is set to one and GPIOn_OD_N is unchanged when GPIOn_O is loaded. Loaded values can be read from GPIOn_CTRL register. It is ignored when VBUS_SRC_SEL is 000b.
3:2	Reserved	R	0b	-

Table 55. VBUS_GPIO_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
1	EN_SNK	R/W	0b	GPIOn_O Setting of Enable Sink Value of this bit is loaded to GPIOn_O where n is VBUS_SNK_SEL of VBUS_PATH_CTRL register, when VBUS Sink Path is enabled, for example, receiving SinkVbus command. GPIOn_OE is set to one and GPIOn_OD_N is unchanged when GPIOn_O is loaded. Loaded values can be read from GPIOn_CTRL register. It is ignored when VBUS_SNK_SEL is 000b.
0	DIS_SNK	R/W	0b	GPIOn_O Setting of Disable Sink Value of this bit is loaded to GPIOn_O where n is VBUS_SNK_SEL of VBUS_PATH_CTRL register, when VBUS Sink Path is disabled, for example, receiving DisableSinkVbus command, detecting VBUS fault condition or detecting FRS VBUS OFF condition. GPIOn_OE is set to one and GPIOn_OD_N is unchanged when GPIOn_O is loaded. Loaded values can be read from GPIOn_CTRL register. It is ignored when VBUS_SNK_SEL is 000b.

7.2.47 VBUS_CP_CTRL Register (88h)

Table 56. VBUS_CP_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:2	Reserved	R	0b	Set to zero by sender and ignored by receiver.
1	VSRC_CP_EN	R/W	0b	VSRC_GATE Charge pump Enable Since it takes tens of ms that the charge pump generates high voltage, TCPM enables the charge pump before turning on VSRC_GATE. TCPM might enable the charge pump in the AttachWait.SRC state, and can disable it when leaving from the Attached.SRC state. 0b: VSRC_GATE charge pump is disabled. 1b: VSRC_GATE charge pump is enabled. *Note:* When Sink FRS is enabled with Fast Role Swap Enable in POWER CONTROL register, TCPM sets this bit.
0	Reserved	R	0b	Set to zero by sender and ignored by receiver.

7.2.48 GPIO_OC_EN Register (89h)

Table 57. GPIO_OC_EN Register

Bit(s)	Name	Type	Reset Value	Description
7:4	Reserved	R	0b	Set to zero by sender and ignored by receiver.
3	GPIO4 OC# EN	R/W	0b	GPIO4 OC# Enable 0b: GPIO4 OC# input is disabled. 1b: GPIO4 OC# input is enabled. When it is set to 1b and GPIO4_OE is set to 0b, GPIO4 pin acts as OC# input. Overcurrent is detected if GPIO4 pin is low. TCPM can manually set GPIO4_OE = 1b, GPIO4_OD_N = 0b and GPIO4_O = 0b to use GPIO4 pin as OC# output.
2	GPIO3 OC# EN	R/W	0b	GPIO3 OC# Enable 0b: GPIO3 OC# input is disabled. 1b: GPIO3 OC# input is enabled. When it is set to 1b and GPIO3_OE is set to 0b, GPIO3 pin acts as OC# input. Overcurrent is detected if GPIO3 pin is low. TCPM can manually set GPIO3_OE = 1b, GPIO3_OD_N = 0b and GPIO3_O = 0b to use GPIO3 pin as OC# output.
1	GPIO2 OC# EN	R/W	0b	GPIO2 OC# Enable 0b: GPIO2 OC# input is disabled. 1b: GPIO2 OC# input is enabled. When it is set to 1b and GPIO2_OE is set to 0b, GPIO2 pin acts as OC# input. Overcurrent is detected if GPIO2 pin is low. TCPM can manually set GPIO2_OE = 1b, GPIO2_OD_N = 0b and GPIO2_O = 0b to use GPIO2 pin as OC# output.
0	GPIO1 OC# EN	R/W	0b	GPIO1 OC# Enable 0b: GPIO1 OC# input is disabled. 1b: GPIO1 OC# input is enabled. When it is set to 1b and GPIO1_OE is set to 0b, GPIO1 pin acts as OC# input. Overcurrent is detected if GPIO1 pin is low. TCPM can manually set GPIO1_OE = 1b, GPIO1_OD_N = 0b and GPIO1_O = 0b to use GPIO1 pin as OC# output.

7.2.49 VBUS_CTRL Register (90h)

Table 58. VBUS_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
15	Reserved	R	0b	Set to zero by sender and ignored by receiver.
14:12	N3	R/W	000b	N3. Refer to VBUS Current Measurement. TCPM should not set zero to N3 or at least MSB of N3 (Bit[14]) when AVERAGE_EN is set to one. Setting zero is undefined when AVERAGE_EN is set to one.
11	Reserved	R	0b	Set to zero by sender and ignored by receiver.
10:8	N4	R/W	0000b	N4. Refer to VBUS Current Measurement.

Table 58. VBUS_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
7	RESET_AVERAGE	W	0b	Reset Stored Average VBUS Current It is write only bit, and zero will be read. When one is written, VBUS_AVE_CURRENT register is cleared to zero, and start to measure new average current value over the TIME_INTERVALif AVERAGE_EN is one. When zero is written, it has no effect.
6	AVERAGE_EN	R/W	0b	Enable Average VBUS Current Measurement 0b: Disabled 1b: Enabled When the AVERAGE_EN = 1, it enables calculating an average of VBUS Current and VBUS_AVE_CURRENT register is kept updated whenever new average value is calculated. When this bit is set to zero, VBUS_AVE_CURRENT register holds the last value until RESET_AVERAGE is set to one or Disable VBUS_CURRENT Monitor is set to one.
5	RESET_PEAK	W	0b	Reset Stored Peak VBUS Current It is write only bit, and zero will be read. When one is written, VBUS_PEAK_CURRENT register is cleared to zero, and start to measure new peak current value if PEAK_EN is one. When zero is written, it has no effect.
4	PEAK_EN	R/W	0b	Enable Peak VBUS Current Measurement 0b: Disabled 1b: Enabled When PEAK_EN = 1, it enables to recode peak VBUS current value, and VBUS_PEAK_CURRENT register is kept updated whenever new peak current value is detected. When this bit is set to zero, VBUS_PEAK_CURRENT register holds the last value until RESET_PEAK is set to one or Disable VBUS_CURRENT Monitor is set to one.

Table 58. VBUS_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
3:2	TIME_INTERVAL	R/W	00b	VBUS ADC Time Interval It selects sampling interval of ADC. Every sampling interval, if both VBUS_VOLTAGE Monitor of POWER_COTNROL register and Disable VBUS_CURRENT Monitor of this register are set to 0b (that is monitor function is enabled), source of ADC is alternating between VBUS voltage and VBUS current at the half of the interval. So that VBUS voltage and VBUS current are sampled every interval which is set to this field. If either one of Disable VBUS_VOLTAGE Monitor or Disable VBUS_CURRENT Monitor is set to 0b, only the enabled one is sampled at the every interval. Between the interval, the ADC function is disabled to save power. The ADC is disabled entirely if both Disable VBUS_VOLTAGE Monitor and Disable VBUS_CURRENT Monitor are set to 1b. Sampled VBUS voltage is read from VBUS_VOLTAGE register, and sampled VBUS current is read from VBUS_CURRENT register. 00b: 5ms 01b: 10ms 10b: 15ms 11b: 20ms
1	Reserved	R	0b	Set to zero by sender and ignored by receiver.
0	Disable VBUS_CURRENT Monitor	R/W	1b	0b: VBUS_CURRENT Monitoring is enabled. VBUS_CURRENT register is updated every interval set by TIME_INTERVAL of this register. 1b: VBUS_CURRENT Monitoring is disabled. When this bit is 1b, all other bits in this register, VBUS_CURRENT, VBUS_AVE_CURRENT and VBUS_PEAK_CURRENTare invalid. VBUS_AVE_CURRENT and VBUS_PEAK_CURRENT can be cleared by setting one to RESET_AVERAGE or RESET_PEAK.

7.2.50 VBUS_CURRENT Register (92h)

Table 59. VBUS_CURRENT Register[1]

Bit(s)	Name	Type	Reset Value	Description
15	Direction	R	0b	0b: Sink 1b: Source
14:10	Reserved	R	0b	Set to zero by sender and ignored by receiver.
9:0	VBUS_CURRENT	R	000000000b	VBUS Current LSB is 11.574mA.

1. This register is cleared when the Disable VBUS_CURRENT Monitor bit of the VBUS_CTRL register is set to 1b.

7.2.51 VBUS_PEAK_CURRENT Register (94h)

Table 60. VBUS_PEAK_CURRENT Register[1]

Bit(s)	Name	Type	Reset Value	Description
15:10	Reserved	R	0b	Set to zero by sender and ignored by receiver.
9:0	VBUS_PEAK_CURRENT	R	000000000b	VBUS Peak Current LSB is 11.574mA.

1. This register is cleared when the Disable VBUS_CURRENT Monitor bit of the VBUS_CTRL register is set to 1b.

7.2.52 VBUS_AVE_CURRENT Register (96h)

Table 61. VBUS_AVE_CURRENT Register[1]

Bit(s)	Name	Type	Reset Value	Description
15:10	Reserved	R	0b	Set to zero by sender and ignored by receiver.
9:0	VBUS_AVE_CURRENT	R	000000000b	VBUS Average Current It shows the Integer part of y_n in 5.3.6.2. Refer to 5.3.6.2 for more detail LSB is 11.574mA.

1. This register is cleared when the Disable VBUS_CURRENT Monitor bit of the VBUS_CTRL register is set to 1b.

7.2.53 FRS_CTRL Register (98h)

Table 62. FRS_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
7:6	VBUS_FRS	R/W	01b	VBUS Voltage Threshold to turn off VBUS Sink Path if SNK_OFF_SEL = 1b and to turn on VBUS Source Path. It does not affect VBUS Sink Path when SNK_OFF_SELECT is set to 0b. 00b: 5.2V 01b: 5.5V 10b: 5.8V 11b: Reserved
5:1	SNK_TO_SRC_TIMER	R/W	00000b	VBUS Sink Off to Source On Timer VBUS Source path, VSRC_GATE or GPIO, is turned on after SNK_TO_SRC_TIMERON × 4µs of turning off VBUS Sink Path, or detecting VBUS < VBUS_FRS whichever comes later. If VBUS Sink Path is already off when FRS signal is received, it is treated as this timer is expired to turn on VBUS Source Path when VBUS < VBUS_FRS is detected. 00000b: 0µs 00001b: 4µs 00010b: 8µs … 11111b: 124µs *Note:* Actual interval time is 0 to 2.67µs longer than the setting, for example, actual time is 4.0 to 6.67µs when set to 4µs.

Table 62. FRS_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
0	SNK_OFF_SEL	R/W	0b	VBUS Sink Off Trigger VBUS Sink Path, VSNK_GATE or GPIO, is turned off when either condition is detected. 0b: FRS Signal is received. 1b: FRS Signal has been received and VBUS < VBUS_FRS_SNK is detected.

7.2.54 SINK_PATH_DISCHG Register (9Ah)

Table 63. SINK_PATH_DISCHG Register

Bit(s)	Name	Type	Reset Value	Description
7:4	Reserved	R	0h	Set to zero by sender and ignored by receiver.
3:2	DISCHG_TIMEOUT	R/W	00b	00b:150ms 01b:200ms 10b:250ms 11b:300ms
1	MANUAL_DISCHG	R/W	0b	Manual Discharge Trigger 0b: Manual Discharge is not triggered. 1b: Start Manual Discharge. Once voltage of SINK_DISCHG pin reaches vSafe5V(max) or DISCHARGE_TIMEOUT is expired, discharging is stopped and this bit is cleared to zero.
0	DISCHG_MODE	R/W	0b	Select a mode of Sink Path Discharge 0b: Manual Discharge. 1b: Automatic Discharge.

7.2.55 SNK_DETACH Register (9Bh)

Table 64. SNK_DETACH Register

Bit(s)	Name	Type	Reset Value	Description
7:5	Reserved	R	000b	Set to zero by sender and ignored by receiver.
4	AUTO_DISCHG_SNK_OPEN	R/W	0b	0b: VBUS is not automatically discharged when Sink Disconnect condition of SNK.Open is detected. TCPM needs to set 0b to this bit.
3:0	SNK_OPEN	R/W	0000b	0000b: PROCHOT# assertion is disabled for Sink Detach detected by CC lines. 0001b to 1111b: PROCHOT# is asserted when this field is set to non-zero value, SNK_DETACH_EN of PROCHOT_EN register is set to 1b, and SNK_DETACH_PROCHOT of VENDOR_STATUS register is set to 1b.

7.2.56 VENDOR_STATUS Register (A0h)

Table 65. VENDOR_STATUS Register

Bit(s)	Name	Type	Reset Value	Description
15	Sink path discharge timeout	R/W1C	0b	0b: Not timed out yet to discharge or not started to discharge 1b: Not completed to discharge internal sink path within a setting in SINK_PATH_DISCHARGE_CTRL.Bit3:2
14	Sink path discharge completion	R/W1C	0b	0b: Not completed to discharge or not started to discharge 1b: Completed to discharge either internal sink path voltage transitions below vSafe5V or the voltage does not transition below vSafe5V after the timeout setting in SINK_PATH_DISCHARGE_CTRL.Bit3:2
13	VCONN_OTP	R/W1C	0b	0b: VCONN_OTP_DIS of VCONN_FAULT_CTRL register is 1b or VCONN OTP has not been occurred. 1b: VCONN_OTP_DIS of VCONN_FAULT_CTRL register is 0b and VCONN OTP has been occurred. This bit remains 1b even if TCPM writes 1b to this bit when VCONN over temperature condition still occurs.
12	VCONN_RVP	R/W1C	0b	0b: VCONN_RVP_DIS of VCONN_FAULT_CTRL register is 1b or VCONN RVP has not been occurred. 1b: VCONN_RVP_DIS of VCONN_FAULT_CTRL register is 0b and VCONN RVP has been occurred. This bit remains 1b even if TCPM writes 1b to this bit when VCONN Reverse voltage condition still occurs.
11	VCONN_UVP	R/W1C	0b	0b: VCONN_UVP_DIS of VCONN_FAULT_CTRL register is 1b or VCONN UVP has not been occurred. 1b: VCONN_UVP_DIS of VCONN_FAULT_CTRL register is 0b and VCONN UVP has been occurred. This bit remains 1b even if TCPM writes 1b to this bit when VCONN Under voltage condition still occurs.
10	VCONN_OVP	R/W1C	0b	0b: VCONN_OVP_DIS of VCONN_FAULT_CTRL register is 1b or VCONN OVP has not been occurred. 1b: VCONN_OVP_DIS of VCONN_FAULT_CTRL register is 0b and VCONN OVP has been occurred. This bit remains 1b even if TCPM writes 1b to this bit when VCONN Overvoltage condition still occurs.
9	VCONN_0p8V	R/W1C	0b	0b: VCONN is has not been changed below 0.8V. 1b: VCONN has been changed below 0.8V. This bit is intended to indicate when VCONN discharge is completed in order to show VCONN status even if the Enable VCONN bit of the POWER_CONTROL register is set to 0b.
8:7	Reserved	R	00b	Set to zero by sender and ignored by receiver.
6	FAULT_STATE_CHANGED	RW1C	0b	0b: FAULT_STATE bit is not changed since last time TCPM wrote 1b to this bit. 1b: FAULT_STATE bit is changed since last time TCPM wrote 1b to this bit.
5	FAULT_STATE	R	0b	0b: RAA489400 is not in the FAULT state. 1b: RAA489400 is in the FAULT state.

Table 65. VENDOR_STATUS Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
4	SRC_VBUS_RVP	R/W1C	0b	0b: SRC_VBUS_RVP_DIS of VBUS_FAULT_CTRL register is 1b or SRC VBUS RVP has not been occurred. 1b: SRC_VBUS_RVP_DIS of VBUS_FAULT_CTRL register is 0b and SRC VBUS RVP has been occurred. This bit remains 1b even if TCPM writes 1b to this bit when Source VBUS Reverse voltage condition still occurs.
3	SRC_VBUS_UVP	R/W1C	0b	0b: SRC_VBUS_UVP_DIS of VBUS_FAULT_CTRL register is 1b or SRC VBUS UVP has not been occurred. 1b: SRC_VBUS_UVP_DIS of VBUS_FAULT_CTRL register is 0b and SRC VBUS UVP has been occurred. This bit remains 1b even if TCPM writes 1b to this bit when Source VBUS Under voltage condition still occurs.
2	Reserved	R	0b	Set to zero by sender and ignored by receiver.
1	SNK_DETACH_PROCHOT	R/W1C	0b	0b: Sink Detach by SNK.Open has not been detected. 1b: Sink Detach by SNK.Open has been detected. Writing one to this bit clears the bit to zero. If bit 0 of ALERT_EXTENDED register and bit 1 of this register are zero, PROCHOT# is deasserted (Hi-Z). Sink Detach is detected when: SNK.Open is detected on the monitored CC for more than 40µs. *Note:* It is different form the method defined in the SNK_DETACH register.
0	SNK_DETACH	R/W1C	0b	TCPM needs to clear this bit when TCPM clears other bit in this register.

7.2.57 VENDOR_STATUS_ALERT_MASK Register (A2h)

Table 66. VENDOR_STATUS_ALERT_MASK Register

Bit(s)	Name	Type	Reset Value	Description
15	Sink path discharge timeout	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
14	Sink path discharge completion	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
13	VCONN_OTP	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
12	VCONN_RVP	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
11	VCONN_UVP	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
10	VCONN_OVP	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
9	VCONN_0p8V	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
8:7	Reserved	R	00b	Set to zero by sender and ignored by receiver.
6	FAULT_STATE_ CHANGED	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
4	SRC_VBUS_RVP	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
3	SRC_VBUS_UVP	R/W	0b	0b: Interrupt masked, 1b: Interrupt unmasked
2	Reserved	R	0b	Set to zero by sender and ignored by receiver.
1	SNK_DETACH_PROCHOT	R/W	0b	0b: Interrupt masked 1b: Interrupt unmasked
0	SNK_DETACH	R/W	0b	TCPM needs to set 0b.

7.2.58 VBUS_FAULT_CTRL Register (A4h)

Table 67. VBUS_FAULT_CTRL Register [1][2][3]

Bit(s)	Name	Type	Reset Value	Description
15:12	Reserved	R	0000b	Set to zero by sender and ignored by receiver.
11:8	UVP_INACTIVE_TIME	R/W	0001b	VBUS_UV/VCONN_UV detection is not activated from when VBUS/VCONN is enabled to when the time specified by this field is elapsed even if SRC_VBUS_UVP_DIS bit of VBUS_FAULT_CTRL register/VCONN_UVP_DIS bit of this register is 0b and VBUS/VCONN voltage is below the vVbusUv/vVconnUv threshold. This inactive time is applied also when turning on SRC Gate or GPIO in the FRS. The inactive time is 10ms multiplied by value of this field if the field is non-zero, and 160ms if the field is 0000b.

Table 67. VBUS_FAULT_CTRL Register (Cont.)[1][2][3]

Bit(s)	Name	Type	Reset Value	Description
7	VBUS_ OVP_TYPE	R/W	0b	Select VBUS Overvoltage Threshold. It selects VBUS OV threshold either vSprMax or vEprMax. It also selects SRC VBUS OV threshold when SRC_VBUS_NonDefault_OVP (bit 6) is one. It is valid only when VBUS Overvoltage Fault bit (B1) is set to 1b in FAULT_CONTROL Register. 0b: VBUS OVP Threshold is vSprMax 1b: VBUS OVP Threshold is vEprMax
6	SRC_VBUS_NonDefault_ OVP	RW	0b	0b: Use vVbusOv for SRC VBUS OVP threshold. 1b: VBUS_OVP_TYPE (bit 7) selects SRC VBUS OVP threshold. It is valid only when both VBUS Overvoltage of FAULT_CONTROL Register and SRC_VBUS_OVP_DIS (bit 2) are set to 0b
5	Reserved	R	0b	Set to zero by sender and ignored by receiver.
4	SRC_VBUS_RVP_DIS	R/W	0b	0b: SRC VBUS RVP is enabled 1b: SRC VBUS RVP is disabled Note: when VBUS_SRC_SEL and VBUS_SNK_SEL are set to same value for bi-directional VBUS path control, this bit needs to be set to 1b to disable VBUS source reverse voltage.
3	SRC_VBUS_UVP_DIS	R/W	0b	0b: SRC VBUS UVP is enabled 1b: SRC VBUS UVP is disabled *Note:* When system supports 5V and higher VBUS source voltage, TCPM might need to set 1b to this bit because of vVbusUv of threshold voltage.
2	SRC_VBUS_ OVP_DIS	R/W	0b	0b: SRC VBUS OVP is enabled as well as SNK_VBUS_OVP 1b: SRC VBUS OVP is disabled When both VBUS Overvoltage of FAULT_CONTROL and this bit are set to 0b, SRC VBUS OVP is enabled. If either bit is set to 1b, SRC VBUS OVP is disabled. If SRC VBUS OVP is enabled and detected, VBUS Overvoltage of the POWER_STATUS register is set to 1b.
1:0	VBUS_OC	R/W	01b	VBUS Overcurrent Threshold Setting of VBUS Overcurrent Threshold. It is valid only when VBUS Overcurrent Fault bit (B2) of FAULT_CONTROL register is set to 1b. 00b: 1.8A 01b: 3.6A 10b: 4.8A 11b: 6.0A

1. Setting of this register (except for UVP_INACTIVE_TIME) and VBUS Overcurrent/Overvoltage of FAULT_CONTROL register are valid only when VBUS is turned on. When VBUS is turned off VBUS_RVP/UVP/OVP/OCP are disabled regardless of settings of this register.
2. SRC_VBUS_RVP and SRC_VBUS_UVP are reported in VENDOR_STATUS register.
3. UVP_INACTIVE_TIME is valid either when VBUS and/or VCONN is turned on or FRS is enabled.

7.2.59 VCONN_FAULT_CTRL Register (A6h)

Table 68. VCONN_FAULT_CTRL Register[1]

Bit(s)	Name	Type	Reset Value	Description
7:6	Reserved	R	0b	Set to zero by sender and ignored by receiver.
5	VCONN_OTP_DIS	R/W	0b	0b: VCONN OTP is enabled. 1b: VCONN_OTP is disabled.
4	VCONN_RVP_DIS	R/W	0b	0b: VCONN RVP is enabled. 1b: VCONN_RVP is disabled.
3	VCONN_UVP_DIS	R/W	0b	0b: VCONN UVP is enabled. 1b: VCONN_UVP is disabled.
2	VCONN_OVP_DIS	R/W	0b	0b: VCONN OVP is enabled. 1b: VCONN_OVP is disabled.
1:0	VCONN_OC	R/W	01b	VCONN Overcurrent Threshold Setting of VCONN Overcurrent Threshold. It is valid only when VCONN Overcurrent Fault bit (B0) of FAULT_CONTROL register is set to 0b. 00b: 400mA 01b: 600mA 10b: 800mA 11b: Reserved

1. Setting of this register is valid only when VCONN is turned on. When VCONN is turned off VCONN_RVP/UVP/OVP/OTP are disabled regardless of settings of this register.

7.2.60 OCP_OUTPUT_CTRL Register (A8h)

Table 69. OCP_OUTPUT_CTRL Register

Bit(s)	Name	Type	Reset Value	Description
15:14	Reserved	R	0b	Set to zero by sender and ignored by receiver.
13	VCONN_OTP	R/W	0b	0b: VCONN OTP does not assert OCP# output. 1b: OCP# is asserted when VCONN_OTP of VENDOR_STATUS register is 1b.
12	VCONN_RVP	R/W	0b	0b: VCONN RVP does not assert OCP# output. 1b: OCP# is asserted when VCONN_RVP of VENDOR_STATUS register is 1b.
11	VCONN_UVP	R/W	0b	0b: VCONN UVP does not assert OCP# output. 1b: OCP# is asserted when VCONN_UVP of VENDOR_STATUS register is 1b.
10	VCONN_OVP	R/W	0b	0b: VCONN OVP does not assert OCP# output. 1b: OCP# is asserted when VCONN_OVP of VENDOR_STATUS register is 1b.
9	Reserved	R	0b	Set to zero by sender and ignored by receiver.
8	VCONN_OCP	R/W	0b	0b: VCONN OCP does not assert OCP# output. 1b: OCP# is asserted when VCONN Overcurrent (B1) of FAULT_STATUS register is 1b.
7:5	Reserved	R	000b	Set to zero by sender and ignored by receiver.

Table 69. OCP_OUTPUT_CTRL Register (Cont.)

Bit(s)	Name	Type	Reset Value	Description
4	VBUS_RVP	R/W	0b	0b: VBUS RVP does not assert OCP# output. 1b: OCP# is asserted when VBUS_RVP of VENDOR_STATUS register is 1b.
3	VBUS_UVP	R/W	0b	0b: VBUS UVP does not assert OCP# output. 1b: OCP# is asserted when VBUS_UVP of VENDOR_STATUS register is 1b.
2	VBUS_OVP	R/W	0b	0b: VBUS OVP does not assert OCP# output. 1b: OCP# is asserted when VBUS Overvoltage (B2) of FAULT_STATUS register is 1b.
1	Reserved	R	0b	Set to zero by sender and ignored by receiver.
0	VBUS_OCP	R/W	0b	0b: VBUS OCP does not assert OCP# output. 1b: OCP# is asserted when VBUS Overcurrent (B3) of FAULT_STATUS register is 1b.

7.2.61 PROCHOT_EN Register (AAh)

Table 70. PROCHOT_EN Register

Bit(s)	Name	Type	Reset Value	Description
7:2	Reserved	R	00000b	Set to zero by sender and ignored by receiver.
1	SNK_DETACH_EN	R/W	0b	0b: Detecting Sink Detach by SNK.Open, that is, setting SNK_DETACH_PROCHOT bit of VENDOR_STATUS register to 1b, does not assert PROCHOT#. 1b: Detecting Sink Detach by SNK.Open, that is, setting SNK_DETACH_PROCHOT of VENDOR_STATUS register to 1b, asserts PROCHOT#. Sink Detach is detected when: SNK.Open is detected on the monitored CC for more than 40µs. Note that it is different form the method defined in the SNK_DETACH register
0	FRS_EN	R/W	0b	0b: Receiving FRS Signal, that is, setting Sink Fast Role Swap bit of ALERT_EXTENDED register to 1b, does not assert PROCHOT#. 1b: Receiving FRS Signal, that is, setting Sink Fast Role Swap bit of ALERT_EXTENDED register to 1b, asserts PROCHOT#.

7.2.62 Control1 Register (B1h)

Table 71. Control1 Register

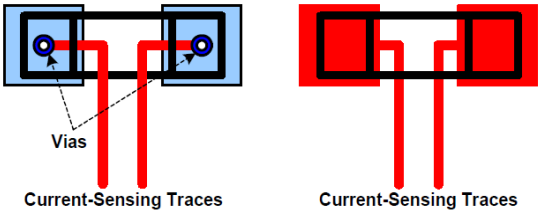
Bit(s)	Name	Type	Reset Value	Description
15:3	Reserved	R/W	0h	Must be set to zero.
2:0	Oscillator Calibration Setting	R/W	000b	Must be set to 001b.

7.2.63 TYPE_C_PRAMETER Register (E2h)

Table 72. TYPE_C_PARAMETER Register

Bit(s)	Name	Type	Reset Value	Description
15	Reserved	R/W	0b	Set to zero.
14	Force Enable 24MHz Clock operation	R/W	0b	0b: Enabled automatic power saving 1b: Disabled automatic power saving Before starts to transmit BIST message, this field must be set to 1b. For other cases, this field must be set to 0b for power saving.
13	Stop 24MHz OSC	R/W	0b	0b: 24MHz OSC is enabled. 1b: 24MHz OSC is disabled. When CC1/CC2 status is changed or I^2C access is received, 24MHz OSC is enabled again automatically and this bit is cleared to 0b.
12:9	Reserved	R	0000b	Set to zero by sender.
8:2	Reserved	R/W	110 0100b	Set to same value as Reset Value.
1:0	Reserved	R	00b	Set to zero by sender.

8. Layout

Pin #	Pin Name	Layout Guidelines
2	CC1	Route the trace with sufficient width. Place decoupling capacitor to filter the noise. Renesas recommends placing the charger CC pins as close to the USB connector as possible, avoid stubs on the CC lines, and route the CC lines with about the same length.
26	CC2	
3	RD1	Connect to CC1, if dead battery Rd needs to be supported.
25	RD2	Connect to CC2, if dead battery Rd needs to be supported.
8	GPIO1	Digital pin, open-drain, push-pull output or input. No special consideration.
7	GPIO2	
6	GPIO3	
5	GPIO4	
9	OCP#	Digital pin, open-drain output. No special consideration.
20	SNK_DISCHG	Run a dedicated trace from the internal sink power rail to the pin.
32	PROCHOT#	Digital pin, open-drain output. No special consideration.
10	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
29	SDA	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
28	SCL	
31	ALERT#	Digital pin, open-drain output. No special consideration.
19	VSNK_SRC	Run this trace with sufficient width in parallel fashion with the VSNK_GATE trace.
18	VSNK_GATE	Run this trace with sufficient width in parallel fashion with the VSNK_SRC trace.
22	VSRC_SRC	Run this trace with sufficient width in parallel fashion with the VSRC_GATE trace.
21	VSRC_GATE	Run this trace with sufficient width in parallel fashion with the VSRC_SRC trace.
23	VSRC_BOOT	Connect to VSRC_SRC through a capacitor.
16	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
15	CSIP	
14	VBUS	Run a dedicated trace from the VBUS to the pin.
12	VSYS33	Run a dedicated trace from the system to the pin.
30	VCONN_POWER	Place the decoupling capacitor in the general proximity of the controller. Route the trace with sufficient width.
13	VDD33	
4	VDD25	
24	GND	Connect this pin to the ground plane.
1, 7, 17, 23	NC	No connection. Although open, soldering is required.

9. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg #	Carrier Type [4]	Temp. Range
RAA489400ARGNP#HA0	400AR	32 Ld 3.0×5.0mm FCQFN	L32.3x5	Reel, 6k	-10 to +100°C
RAA489400ARGNP#MA0				Reel, 1k	
RAA489400A3GNP#HA0	400A3			Reel, 6k	-40 to +105°C
RAA489400A3GNP#MA0				Reel, 1k	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 3. For more information about MSL, see TB363.
3. For the PB-Free Profile, see TB493.
4. See TB347 for details about reel specifications.

11. Revision History

Revision	Date	Description
1.00	Aug 27, 2024	Initial release.

Trademarks

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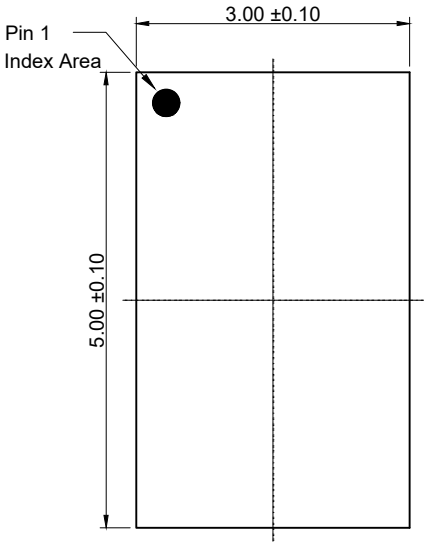
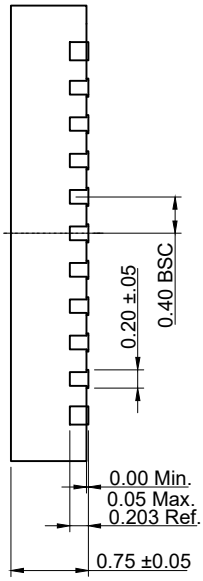
Package Outline Drawing

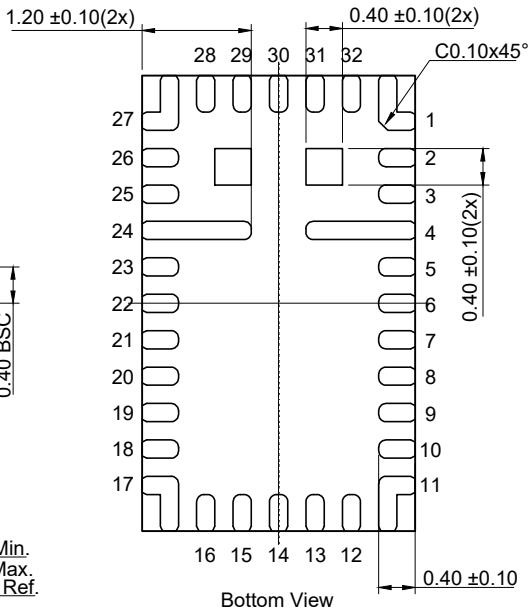
32 Lead Flip Chip Thin Quad Flat No-Lead Package (FCTQFN)
POD Number: L32.3x5, Revision no: 02 Date Created: Feb 1, 2024



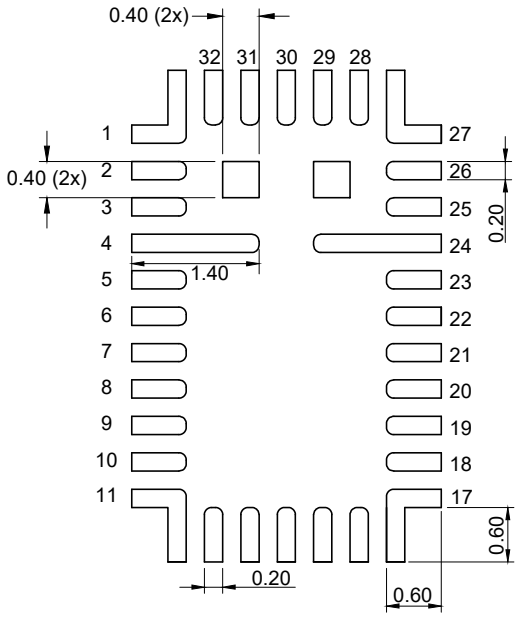
Top View



Side View



Bottom View



Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and toleracing conform to ASME Y14.5M-1994.
3. The configuration of the pin #1 identifier is optional, but must be located in the zone indicated, The pin #1 identifier can be either a mold or a mark feature.
4. Pin1 corner chamfer not required.
5. Unless otherwise specified, tolerance Decimal ±0.05.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

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