RAJ240055 / RAJ240057

2 to 4 Series Li-ion Battery Manager

R01DS0399EJ0101
Rev.1.01
Mar. 13, 2024

CHAPTER 1. INTRODUCTION

1.1 Features

- **Fully integrated battery management solution with battery capacity measurement and programmable protection capability.**
- **Supports up to 4 Li-ion or Li-Polymer battery cells in series.**
- **Supports various self-diagnosis functions for functional safety.**
- **Integrated with Renesas Ultra Low Power RL78 CPU core for multi-function process.**
- **Memory**
  Code flash memory: 64 kB / 128 kB
  Data flash memory (up to 100,000 erase/write cycles): 4 kB
  SRAM: 4 kB / 7 kB
- **Clock generator**
  High speed on-chip oscillator: up to 32 MHz
  Low speed on-chip oscillator: 15 kHz
  AFE high speed on-chip oscillator: 4.194 MHz
  AFE low speed on-chip oscillator: 131.072 kHz
- **General Purpose I/O Ports**
  Total: 12 pins
  CMOS input/output: 6, CMOS input: 1
  N-ch open drain input/output [6 V tolerance]: 3
  High voltage input [30 V tolerance]: 1
  High voltage input/output [VCC tolerance]: 1
- **Serial interface**
  CSI (SPI): 1 channel, UART: 2 channels
  Simplified I2C: 1 channel, I2C: 1 channel
- **Timer**
  MCU 16-bit timer: 6 channels
  MCU 12-bit interval timer: 1 channel
  AFE timer: 2 channels
  - AFE timer A: setting range: 125 ms to 64 s
  - AFE timer B: setting range : 61 us to 2 s
- **Embedded A/D converter**
  AFE 15-bit resolution sigma-delta A/D converter
  - Automatic measurement mode
  - Continuous measurement mode
- **Current integrating circuit**
  18-bit resolution sigma-delta A/D converter
- **Impedance measurement circuit**
  Simultaneous measurement of battery voltage and current
- **Over current detection circuit**
  Short circuit current detection: 2 channels
  Charge overcurrent detection
  Discharge overcurrent detection
  Charge wakeup current detection
  Discharge wakeup current detection
  DBPT current detection
- **Series regulator**
  2.0 V or 3.3 V output can be selected (> 20 mA)
- **Charge and Discharge MOSFET control**
  Supports High-side Nch MOSFET drive (built-in charge pump circuit)
- **Ultra Low Power consumption**
  Power down mode: 1 uA
  Sleep mode1 current: 20 uA (DFET and CFET off)
  Sleep mode2 current: 40 uA (DFET and CFET on)
  In Sleep mode, enable H/W protection function
- **Additional features**
  Internal Cell Balancing Circuit (>10 mA)
  Internal Watchdog Timer (MCU)
  MCU Runaway Detection Circuit (AFE)
  3 Thermistor Sensor Ports with On-chip Pull-up Resistors
  Random cell connection tolerant
- **Voltage and temperature condition**
  Power supply voltage: VCC = 2.2 to 25.0 V
  Operating ambient temperature T_A = -40 to +85°C
- **Package Information**
  32 pin plastic mold QFN
  ([Body] 4.0 mm x 4.0 mm, 0.4 mm pitch)
- **Device Lineup**

Device	Flash ROM	Data Flash	RAM
RAJ240055	64 kB	4 kB	4 kB
RAJ240057	128 kB		7 kB

1.2 Applications

- Notebook PC, Tablet PC

1.3 Description

RAJ24005X is a Renesas battery fuel gauge and management device which combines a separate MCU and AFE blocks in a single package to accomplish various battery protection and management functions. This device incorporates advanced battery management features such as primary and secondary protection, voltage and current measurement, current integrating, and host communication interface. Through user programmable control firmware and configuration data stored in the onboard MCU’s embedded flash memory, the embedded analog and digital hardware circuits offer optimum battery management operations including high accuracy remaining capacity estimation and battery safety.

CHAPTER 2. OUTLINE

2.1 Outline of Functions

(1/2)

Item		Description
Code flash memory		64 kB (RAJ240055) / 128 kB (RAJ240057)
Data Flash memory		4 kB
RAM		4 kB (RAJ240055) / 7 kB (RAJ240057)
Address size		1 MB
Main system clock	High speed on-chip Oscillator clock(f_{IH})	HS (high-speed main) mode: 1 to 32 MHz LS (low-speed main) mode: 1 to 8 MHz
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.03125 usec (Internal high-speed oscillation clock: fIH = 32 MHz)
Instruction set		• Data transmission (8/16 bits) • Addition and subtraction/logical operations (8/16 bits) • Multiplication (8×8 bits,16×16 bits), Division (16÷16 bits,32÷32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.
I/O Port	CMOS I/O	6
	CMOS input	1
	N-ch open-drain I/O [6 V tolerance]	3
	High voltage input [3 0 V tolerance]	1
	High voltage I/O [VCC tolerance]	1
Timer	16-bit timer	6 channels (TAU: 4 channels, Timer RD：2 channels)
	Watchdog timer	1 channel
	12-bit interval timer	1 channel
	Timer output	Timer outputs: 3 channels PWM outputs: 3 channels
Serial interface		• UART: 1 channel • CSI: 1 channel/UART: 1 channel/Simplified I2C: 1 channel
	I^{2}C bus	1 channel
Vector interrupt source	Internal	16
	External	14 (6 sources are connected to AFE in the chip)
Reset		・Reset by RESET pin (reset circuit output of AFE connected to RESETOUT) ・Internal reset by watchdog timer ・Internal reset by power-on-reset ・Internal reset by voltage detector ・Internal reset by illegal instruction execution Note ・internal reset by RAM parity error ・internal reset by illegal memory access
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V (TA = −40 to +85°C) • Power-down-reset: 1.50 ±0.04 V (TA = −40 to +85°C)
Voltage detector		1.63 V to 4.06 V (14 stages)
On-chip debug function		Support

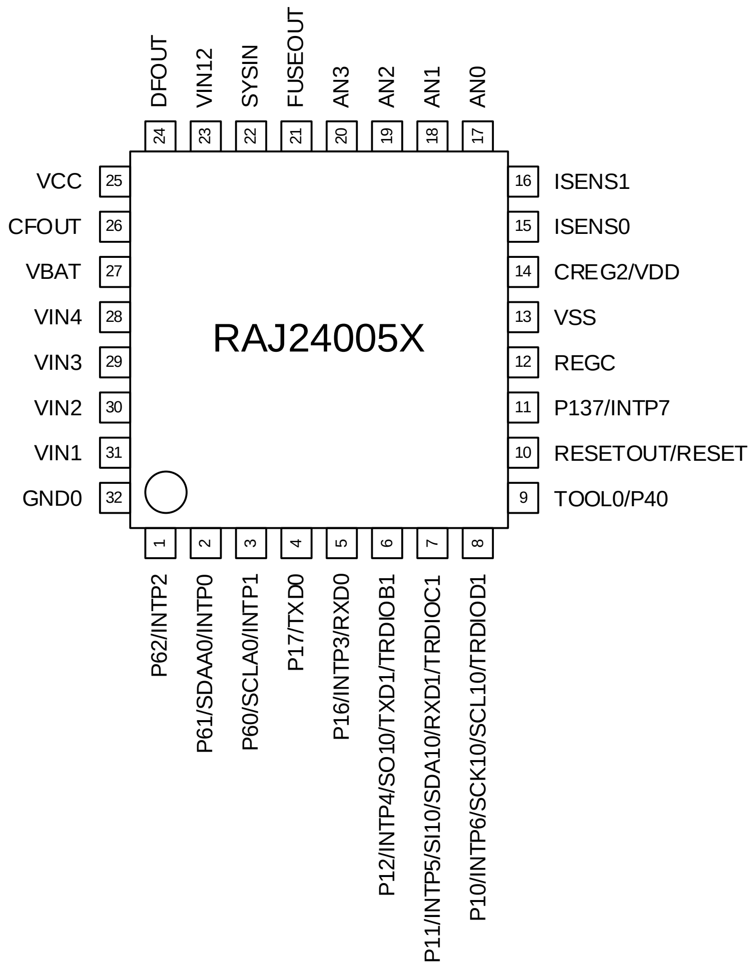
Note The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

Item	Description
Sigma-delta A/D converter	15-bit resolution (sigma-delta method) • Battery Cell voltage (Cell 1 to Cell 4) • Battery Cell total voltage (VBAT pin) • VIN12 pin input voltage • Thermistor sensor port with on-chip pull-up 10 KΩ resistor: 3 channels (AN0, AN1 and AN2) • Analog pin input voltage: 1 channel (AN3) • On-chip simple temperature sensor (temperature range: -40 to 85°C) • Internal reference and supply voltage (AFE)
Current integrating circuit	1 channel:18-bit resolution
Current integrating circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wake up current detection circuit	• Discharge short-circuit current detection: 2 channels • Discharge overcurrent detection • Charge overcurrent detection • Wake up current detection (discharge and charge)
Simple temperature sensor	1 channel
Charge/Discharge High-side FET control circuit	N-ch MOSFET driver for charge control N-ch MOSFET driver for discharge control Programmable MOSFET control by PWM
Power on circuit	Return from power down mode by detecting high voltage input to VIN12 pin
Series regulator	VREG2: power supply for MCU (2.0 V or 3.3 V)
Reset circuit	Series regulator output monitoring (VREG2)
Cell balancing circuit	Support 4 series cells (On-resistor: 200 Ω MAX)
MCU runaway detection circuit	20 bits×1(2 / 4 / 8 / 16 / 32 / 64 [s] to be selected)
AFE On-chip oscillator	4.194 MHz (TYP)
AFE low speed On-chip oscillator	131.072 kHz (TYP)
AFE timer	2 channels • AFE timer A (setting range: 125 ms to 64 s) • AFE timer B (setting range: 61 us to 2 s)
MCU-AFE communication interface(C2C)	AFE to MCU communication (Chip to Chip Interface)
Power supply voltage	VCC = 2.2 to 25.0 V
Operation ambient temperature	-40 to 85°C
Package	32 pin plastic mold QFN([Body] 4.0 mm x 4.0 mm, 0.4 mm pitch)

2.2 Pin Configuration

32 pin plastic mold QFN ([Body] 4.0 mm x 4.0 mm, 0.4 mm pitch)



Caution 1. **CREG2 pin connects to GND0 pin via a capacitor (0.47 uF to 1.0 uF).**

Caution 2. **REGC pin connects to VSS pin via a capacitor (0.47 uF to 1.0 uF).**

Remark Pin name refer to 3.1 Pin Identification.

CHAPTER 3. PIN FUNCTIONS

3.1 Pin Identification

No.	Name	Type	Description
1	P62/INTP2	DIO	Port6 / External Interrupt Input
2	P61/SDAA0/INTP0	DIO	Port6 / I^{2}C Bus data I/O / External Interrupt Input
3	P60/SCLA0/INTP1	DIO	Port6 / I^{2}C Bus clock I/O / External Interrupt Input
4	R17/TXD0	DIO	Port1 / UART Transmit Data
5	P16/INTP3/RXD0	DIO	Port1 / External Interrupt Input / UART Receive Data
6	P12/INTP4/SO10/TXD1/TRDIOB1	DIO	Port1 / External Interrupt Input / Serial Data Output / UART Transmit Data / Timer Output
7	P11/INTP5/SI10/SDA10/RXD1/ TRDIOC1	DIO	Port1 / External Interrupt Input / Serial Data Input / Simplified I2C data I/O / UART Transmit Data / Timer Output
8	P10/INTP6/SCK10/SCL10/TRDIOD1	DIO	Port1 / External Interrupt Input / Serial Clock I/O / Simplified I^{2}C clock I/O / Timer Output
9	TOOL0/P40	DIO	Port4 / Data input/output for Tool
10	RESETOUT/RESET	DIN	Reset input
11	P137/INTP7	DIN	Port13 / External Interrupt Input
12	REGC	P	Regulator Capacitance
13	VSS	P	Ground
14	CREG2/VDD	P	Regulator output
15	ISENS0	AIN	Analog input for current integrating circuit
16	ISENS1	AIN	Analog input for current integrating circuit
17	AN0	AIN	Analog input for Thermistor
18	AN1	AIN	Analog input for Thermistor
19	AN2	AIN	Analog input for Thermistor
20	AN3	AIN	Analog input for Middle voltage (10 V input)
21	FUSEOUT	HVIO	High voltage input/output for Fuse FET control
22	SYSIN	HVIN	High voltage port for system detection
23	VIN12	AIN	High voltage input for power on / charge voltage input
24	DFOUT	HVO	Discharge MOSFET control
25	VCC	P	Power supply
26	CFOUT	HVO	Charge MOSFET control
27	VBAT	AIN	Battery voltage input
28	VIN4	AIN	Battery voltage input
29	VIN3	AIN	Battery voltage input
30	VIN2	AIN	Battery voltage input
31	VIN1	AIN	Battery voltage input
32	GND0	P	Ground

HVO:	**high voltage output**	**DIO:**	**digital I/O**
HVIN:	**high voltage input**	**DIN:**	**digital input**
HVIO:	**high voltage input/output**	**DOUT:**	**digital output**
P:	**power**	**AIN:**	**analog input**

3.2 Pin Functions

3.2.1 Port functions

(1/2)

Function name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P10	8-1-4	I/O	Input port	INTP6/SCK10/SCL10/TRDIOD1	Port 1. 5-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. An input of P10, P11, P12, P16, P17 can be set to TTL input buffer. Output of P10, P11, P12, P16, P17 can be set to N-ch open-drain output (VDD tolerance).
P11	8-1-4			INTP5/SI10/SDA10/RXD1/TRDIOC1	
P12	8-1-4			INTP4/SO10/TXD1/TRDIOB1	
P16	8-1-4			INTP3/RxD0	
P17	8-1-4			TxD0	
P30 Note	7-1-3	I/O	Input port	INTP13	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P31 Note	7-1-3			INTP12	
P32 Note	7-1-3			INTP11	
P33 Note	7-1-3			INTP10	
P40	7-1-3	I/O	Input port	TOOL0	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P40 also can be used for I/O of programmer and debugger.
P60	12-1-6	I/O	Input port	SCLA0/INTP1	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit unit. Output of P60 to P62 can be set to N-ch open-drain output (6 V tolerance).
P61	12-1-6			SDAA0/INTP0	
P62	12-1-5			INTP2	
P70 Note	7-1-3	I/O	Input port	INTP9	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71 Note	7-1-3			INTP8	
P72 Note	7-1-3			(EXBSEL)	
P73 Note	7-1-3			EXBCK	
P74 Note	7-1-3			EXBD0	
P75 Note	7-1-3			EXBD1	
P76 Note	7-1-3			EXBD2	
P77 Note	7-1-3			EXBD3	
P137	2-1-2	input	Input port	INTP7	Port 13. 1-bit input-only port.
RESET	2-1-1	input	Input port	-	Input-only pin for external reset.

Note This pin is internally connected between AFE and MCU.

3.2.2 External Pin Functions

Category	Pin name	I/O	Function
Power supply	VCC	–	Power supply input Apply power supply voltage to VCC pin from a charger or battery.
	GND0	–	Device ground input. Connect the negative input terminal of lithium-ion battery 1 to the GND0 pin
	CREG2	–	Series regulator output port Connect to GND0 via a capacitor (0.47 to 1.0 uF)
	VDD	–	Positive power supply for MCU
	VSS	–	Ground input for MCU Connect the negative input terminal of lithium-ion battery 1 to the GND0 pin
	REGC Note 1	–	Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to VSS via a capacitor (0.47 to 1 uF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
RESET	RESET	Input	This is the active-low system reset input pin for MCU.
	RESETOUT	Output	This is the active-low system reset output pin for AFE.
TOOL0	TOOL0 Note 2	Input	Data I/O for flash memory programmer/debugger. Connect to the VDD via an external pull-up resistor in the on-chip debug mode
Serial interface (UART0, UART1)	RxD0, RxD1	Input	Serial data input pins of serial interface UART0 and UART1
	TxD0, TxD1	Output	Serial data output pins of serial interface UART0 and UART1
Serial interface (CSI10)	SCK10	I/O	Serial clock I/O pins of serial interface CSI10
	SI10	Input	Serial data input pins of serial interface CSI10
	SO10	Output	Serial data output pins of serial interface CSI10
Serial interface (IIC10)	SCL10	Output	Serial clock output pins of serial interface IIC10
	SDA10	I/O	Serial data I/O pins of serial interface IIC10
Serial interface (IICA0)	SCLA0	I/O	Serial clock I/O pins of serial interface IICA0
	SDAA0	I/O	Serial data I/O pins of serial interface IICA0,
A/D converter	AN0 to AN2	Input	AFE A/D converter analog input (Up to 1.8 V input)
	AN3	Input	AFE A/D converter analog input (Up to 10 V input)
Current integrating circuit and overcurrent detection circuit	ISENS0, ISENS1	Input	Analog input for current integrating circuit and over current detection circuit
Timer	TRDIOB1 TRDIOC1 TRDIOD1	I/O	Timer RD input/output
Fuse control input/output	FUSEOUT	I/O	High voltage input/output for fuse control.
System presence input	SYSIN	Input	System presence input
External interrupt input	INTP0 to INTP13	Input	Interrupt request input pin. Only INTP0 and INTP7 pins are connected to the external pin. INTP8 to INTP13 connect interrupt request signal of AFE in the package and do not connect to any pin
Power on circuit	VIN12	Input	Power on input for release from power down state
Cell voltage input	VBAT	Input	The positive input terminal of lithium-ion battery 4
	VIN4	Input	The positive input terminal of lithium-ion battery 4
	VIN3	Input	The negative input terminal of lithium-ion battery 4 and the positive input terminal of lithium-ion battery 3
	VIN2	Input	The negative input terminal of lithium-ion battery 3 and the positive input terminal of lithium-ion battery 2
	VIN1	Input	The negative input terminal of lithium-ion battery 2 and the positive input terminal of lithium-ion battery 1
FET control output	DFOUT	Output	ON/OFF signal output pin for discharge FET
	CFOUT	Output	ON/OFF signal output pin for charge FET.

(Notes are listed on the next page.)

Note 1. REGC is not external power supply pin. (Do not draw current from REGC.)

Note 2. After reset release, the connection between P40/TOOL0 and P137/INTP7 and the operating mode are as follows.

Table 3-1 TOOL0 Pin Operation Mode after Reset Release

P40/TOOL0	P137/INTP7	Operation Mode
VDD	-	Normal operation mode
0 V	VDD	Flash memory programming mode
	0 V	SMBus Boot programming mode

3.2.3 Internal Connection Pins Between AFE and MCU

AFE and MCU are connected with dedicated communication signals which are reference voltage for MCU and interrupt signal from AFE to MCU in the package.

MCU pin	AFE pin	Pin state of AFE	Function
P70/INTP9	INT_AD	Output	ADC completion interrupt output
P71/INTP8	INT_CC	Output	Current Integrating (CC) completion interrupt output
P30/INTP13	INT_TM	Output	AFE Timer underflow interrupt output (AFE timer A or AFE timer B)
P31/INTP12	INT_ANL	Output	Abnormal interrupt output (Over current detection x4, MCU runaway detection, or FUSEOUT pin input edge detection interrupt)
P32/INTP11	INT_WU	Output	Wakeup interrupt output (Wakeup current detection or VIN12 pin input edge detection)
P33/INTP10	INT_SYSIN	Output	SYSIN Pin Input Signal Output
P72	EXBSEL	Input	Control signal of communication between AFE and MCU
P73/EXBCK	EXBCK	Input	Clock signal of communication between AFE and MCU
P74/EXBO0/EXBI0	EXBD0	I/O	Data signal of communication between AFE and MCU
P75/EXBO1/EXBI1	EXBD1	I/O	Data signal of communication between AFE and MCU
P76/EXBO2/EXBI2	EXBD2	I/O	Data signal of communication between AFE and MCU
P77/EXBO3/EXBI3	EXBD3	I/O	Data signal of communication between AFE and MCU

Note EXBSEL, EXBCK and EXBD0 to 3 are connected to GND0 via pull down resistor.

3.3 AFE Pin Block Diagram

Figure 3-1 Pin Block Diagram of VCC Pin

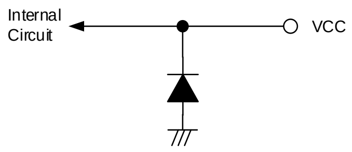


Figure 3-2 Pin Block Diagram of VBAT and CFOUT Pin

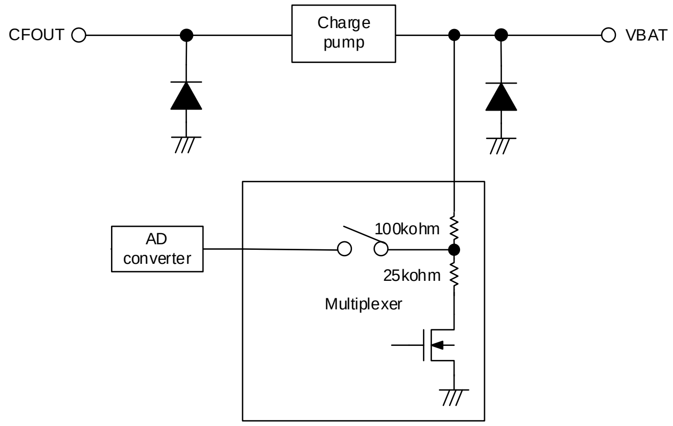


Figure 3-3 Pin Block Diagram of VIN12 and DFOUT Pin

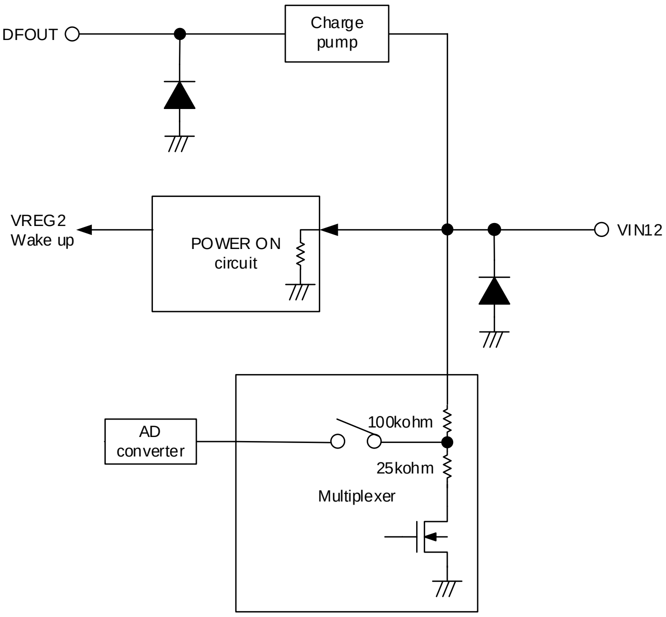


Figure 3-4 Pin Block Diagram of VIN4 to VIN1 Pin

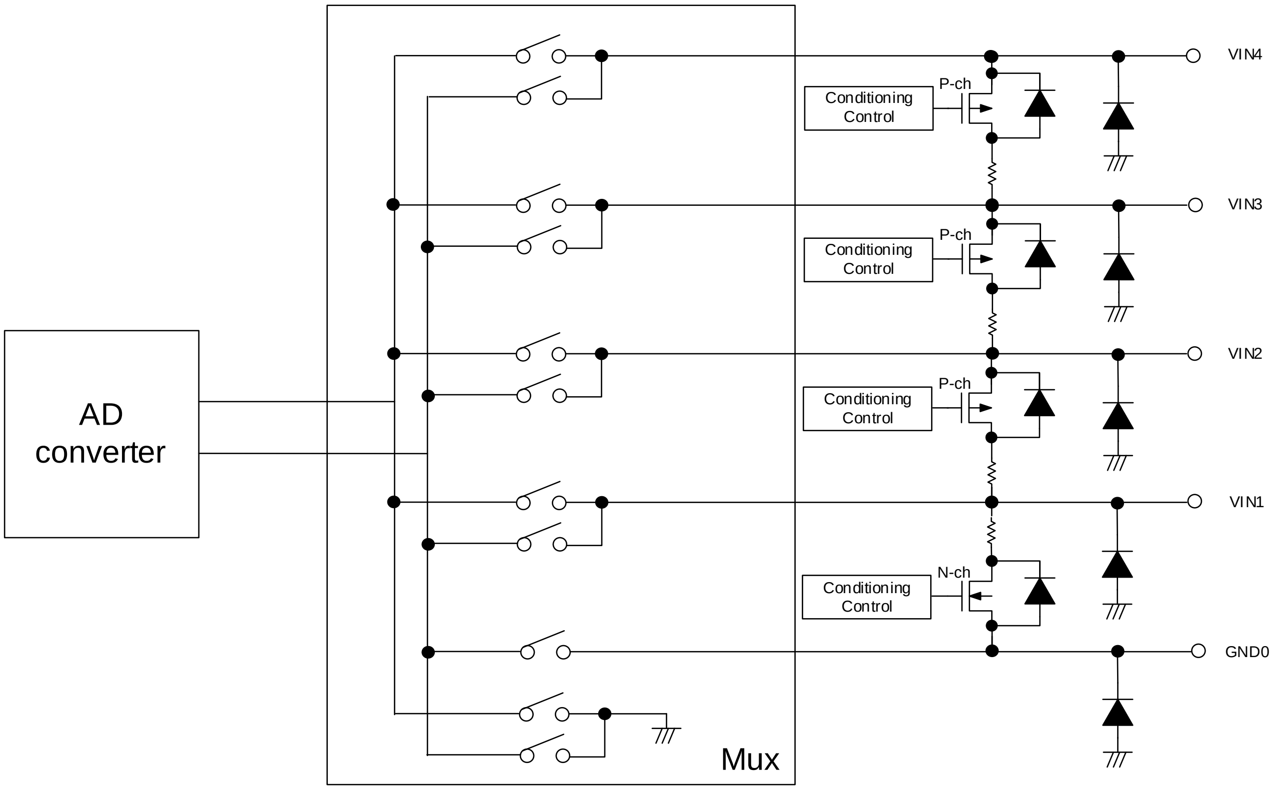


Figure 3-5 Pin Block Diagram of FUSEOUT Pin

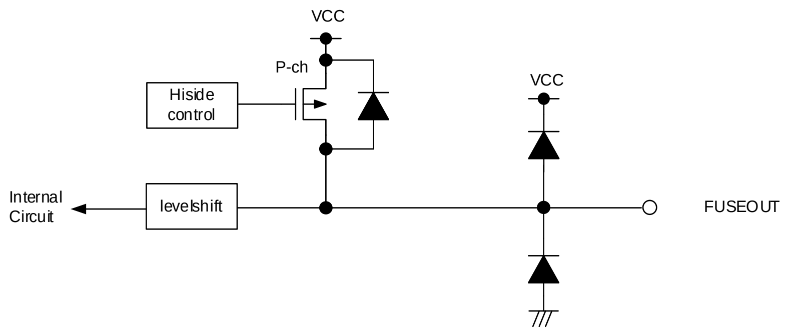


Figure 3-6 Pin Block Diagram of CREG2 Pin

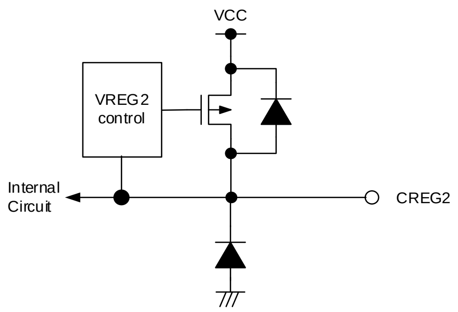


Figure 3-7 Pin Block Diagram of AN0, AN1 and AN2 Pin

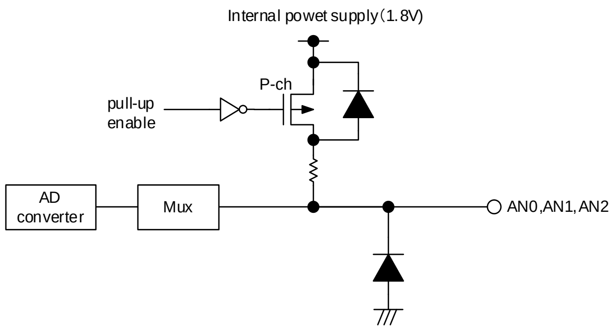


Figure 3-8 Pin Block Diagram of AN3 Pin

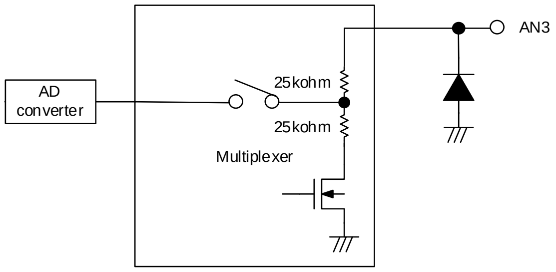


Figure 3-9 Pin Block Diagram of ISENS0 and ISENS1 Pin

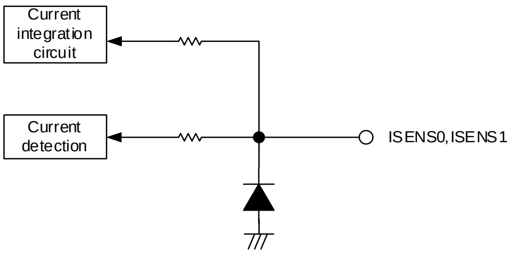


Figure 3-10 Pin Block Diagram of RESETOUT Pin

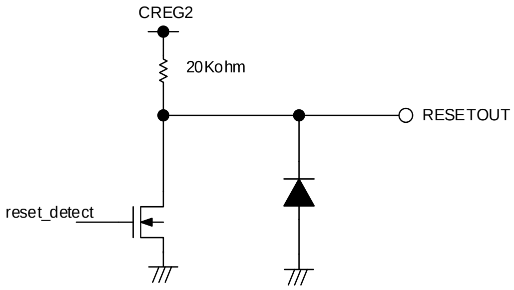
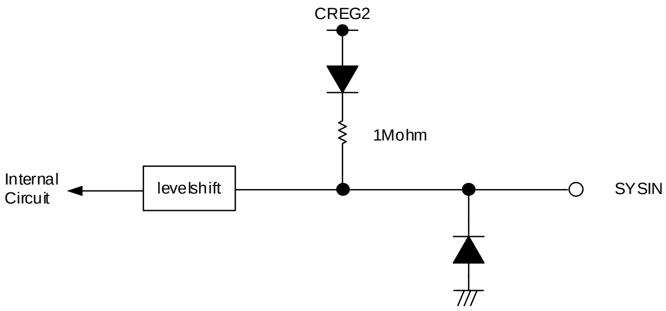
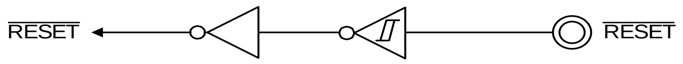


Figure 3-11 Pin Block Diagram of SYSIN Pin



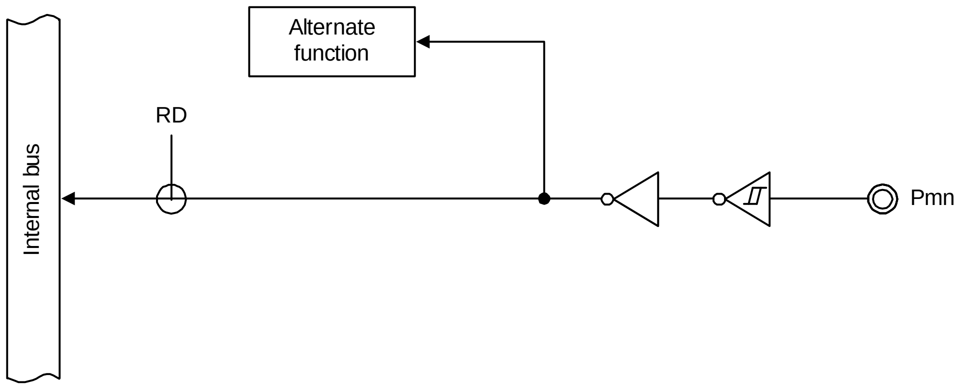
3.4 MCU Pin Block Diagram

Figure 3-12 Pin Block Diagram of Pin type 2-1-1



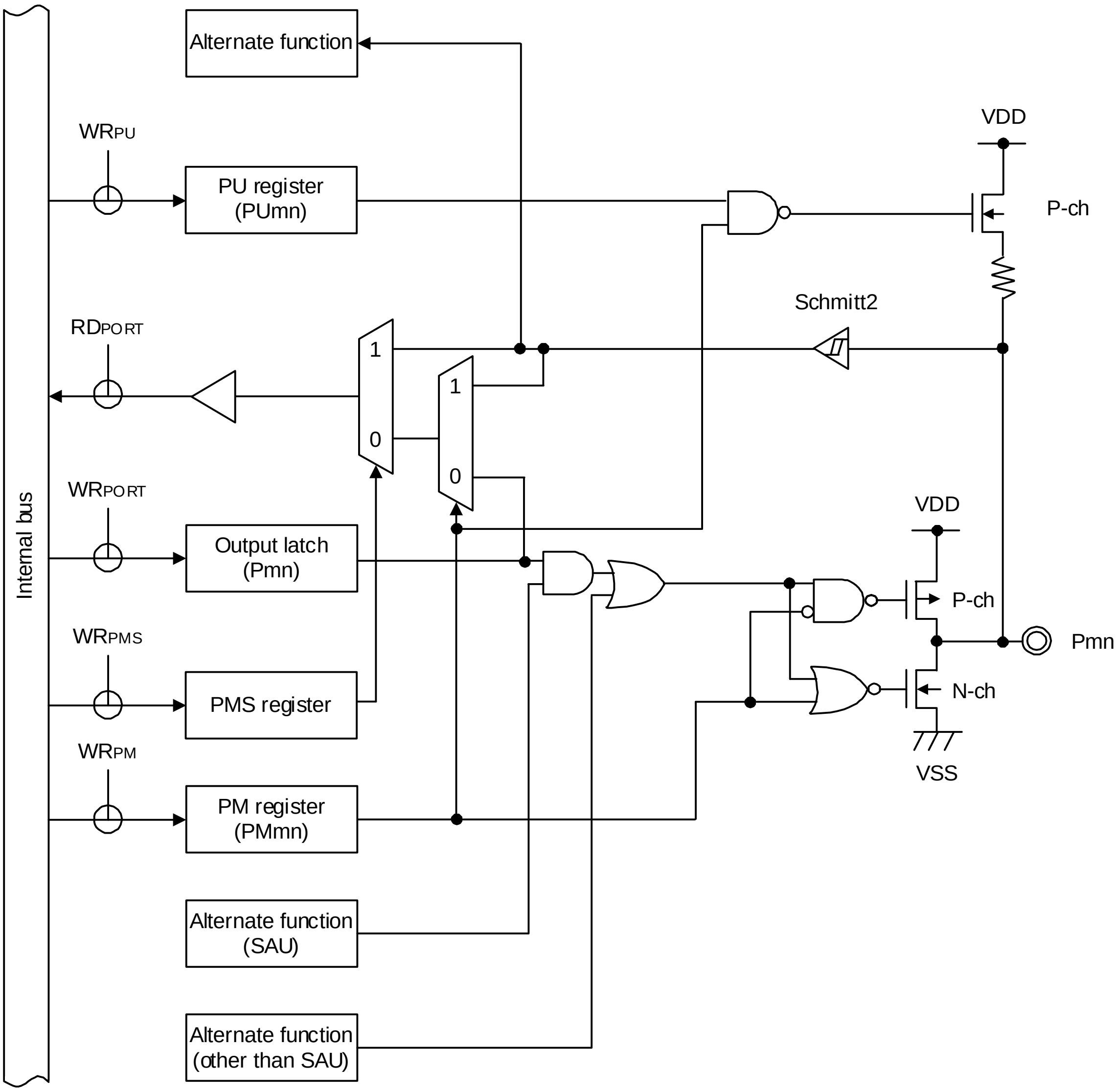
Remark Refer to 3.2.1 Port functions for alternate functions.

Figure 3-13 Pin Block Diagram of Pin type 2-1-2



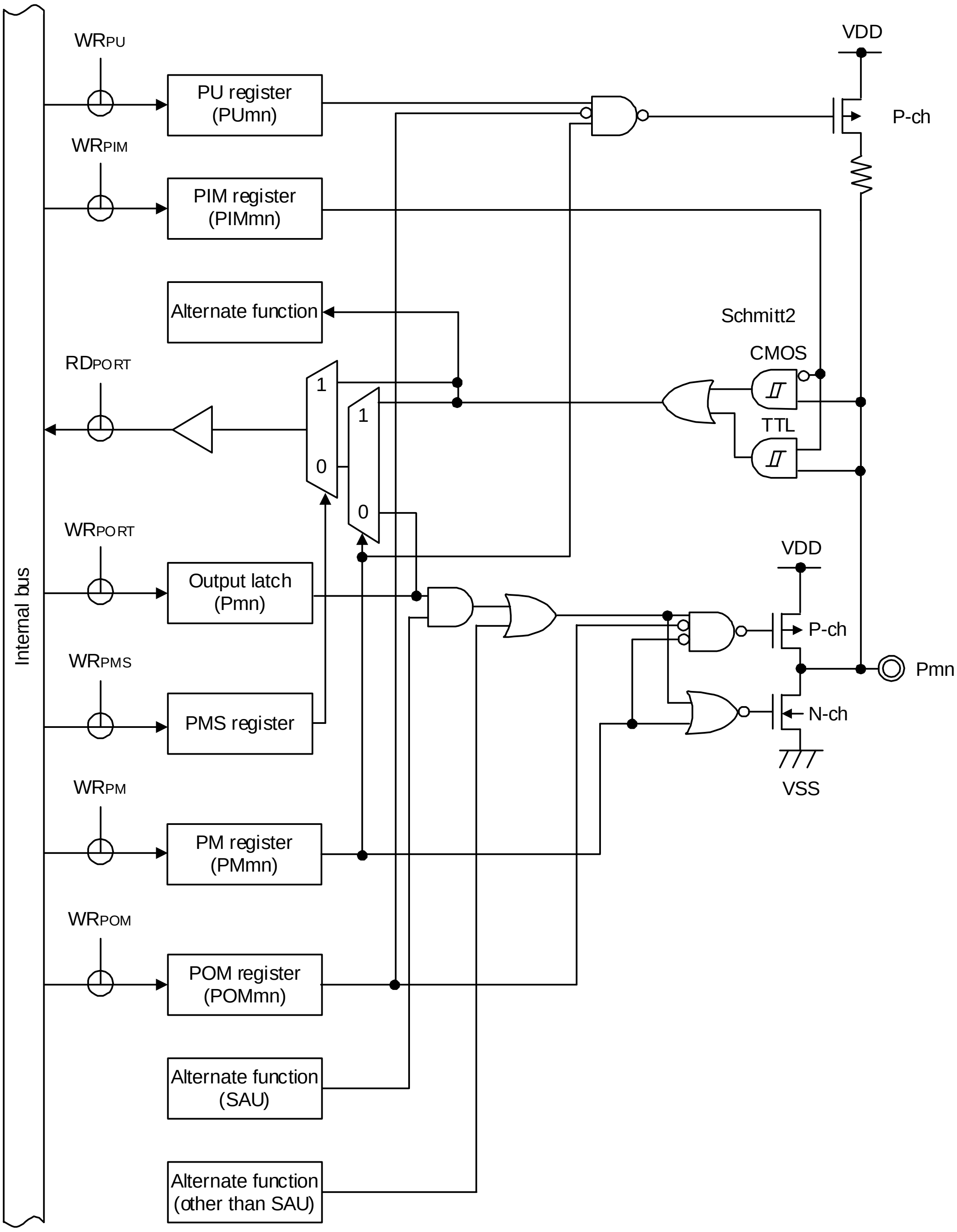
Remark Refer to 3.2.1 Port functions for alternate functions.

Figure 3-14 Pin Block Diagram of Pin type 7-1-3



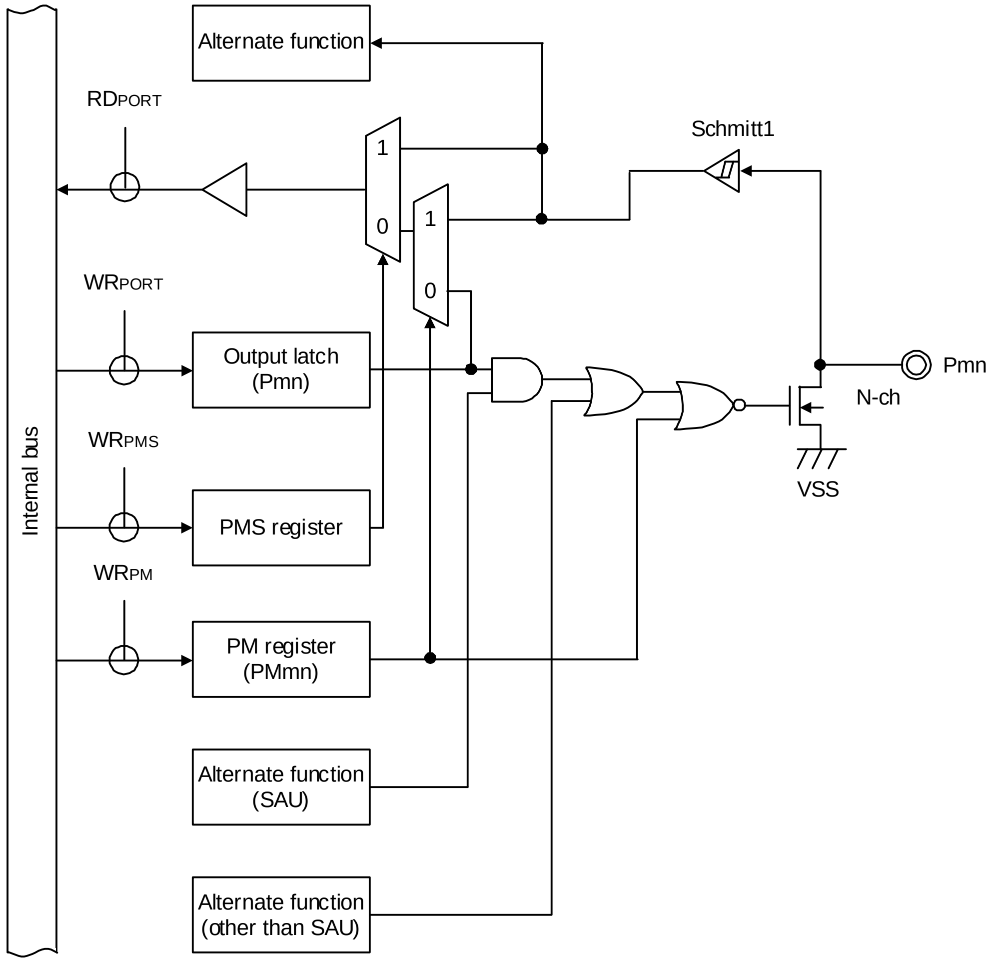
Remark Refer to 3.2.1 Port functions for alternate functions.

Figure 3-15 Pin Block Diagram of Pin type 8-1-4



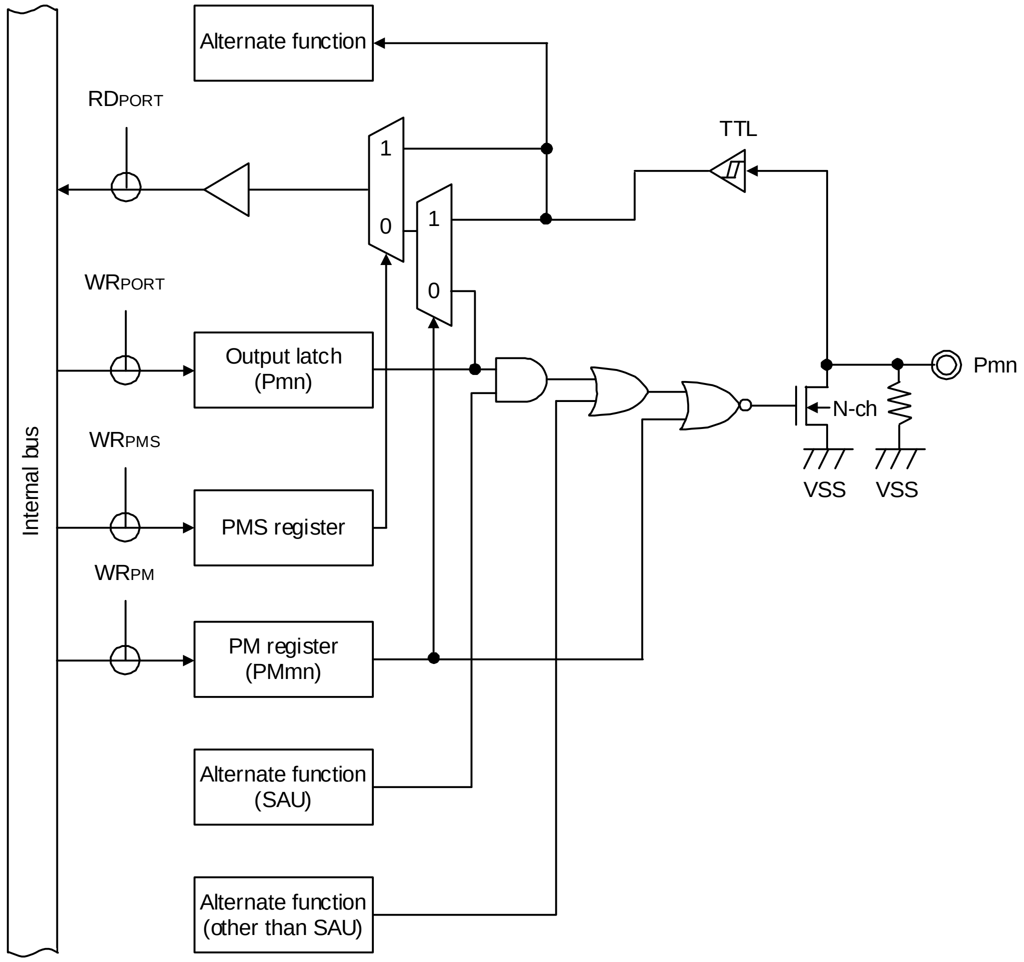
Remark Refer to 3.2.1 Port functions for alternate functions.

Figure 3-16 Pin Block Diagram of Pin type 12-1-5



Remark Refer to 3.2.1 Port functions for alternate functions.

Figure 3-17 Pin Block Diagram of Pin type 12-1-6



Remark Refer to 3.2.1 Port functions for alternate functions.

CHAPTER 4. ELECTRICAL SPECIFICATIONS

Caution This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

4.1 Absolute Maximum Ratings

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	V_{CC}	VCC		-0.5 to +30	V
	GND	GND0, VSS		-0.5 to 0.3	V
CREG2 pin input voltage	V_{ICREG2}	CREG2		-0.3 to +6.5 [Note 1]	V
REGC pin input voltage	V_{IREGC}	REGC		-0.3 to 2.8 and -0.3 to (VDD+0.3) [Note 2]	V
Input voltage	V_{I1}	CMOS port		-0.3 to (VDD+0.3) [Note 3]	V
	V_{I2}	P60 to P62(N-ch open-drain)		-0.3 to +6.5	V
	V_{IN-H1}	VIN4, VIN3, VIN2, VIN1, VBAT, VIN12, SYSIN		-0.5 to + 30	V
	V_{IN-H2}	FUSEOUT		-0.5 to (VCC+0.3) [Note 4]	V
	V_{IN-B}	VIN4 to VIN3, VIN3 to VIN2, VIN2 to VIN1, VIN1 to GND		-0.5 to +6.5	V
	V_{IN-M}	AN3		-0.5 to +12.0	V
	V_{IN-L}	AN0, AN1, AN2, ISENS0, ISENS1		-0.5 to +2.0	V
Output voltage	V_{O1}	CMOS port		-0.3 to (VDD+0.3) [Note 3]	V
	V_{O-H1}	CFOUT, DFOUT		-0.5 to +30.0	V
<R>	V_{O-H2}	FUSEOUT		-0.5 to (VCC+0.3) [Note 4]	V
High-level output current	I_{OH}	Per pin	P10 to P12, P16, P17, P40	-40	mA
		Total of all pins	P10 to P12, P16, P17, P40	-70	mA
Low-level output current	I_{OL}	Per pin	P10 to P12, P16, P17, P40, P60, P61, P62	+40	mA
		Total of all pins	P10 to P12, P16, P17, P40, P60, P61, P62	+70	mA
Cell balancing Input current	I_{CONDI}	VIN4, VIN3, VIN2, VIN1		+40	mA
Cell balancing output current	I_{CONDO0}	VIN3, VIN2, VIN1		+40	mA
	I_{CONDO1}	GND		+50	mA
Power consumption	P_d	Topr = 25°C		300	mW
Operating ambient Temperature	T_A			-40 to +85	°C
Storage temperature	Tstg	-		-65 to +150	°C

Note 1. Connect the CREG2 pin to GND0 via a capacitor (0.47 uF to 1.0 uF). This value regulates the absolute maximum rating of the CREG2 pin.

Note 2. Connect the REGC pin to VSS via a capacitor (0.47 to 1.0 uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 3. Must be 6.5 V or lower.

Note 4. Must be 30 V or lower.

Caution Product quality may degrade if the absolute maximum rating has been exceeded. The absolute maximum ratings are rated values where the product is on the verge of suffering physical damage, therefore the product must be used within that ensure the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. GND (GND0 and VSS): Reference voltage.

4.2 Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply	VCC	CREG2 = 2.0 V setting	2.2	-	25.0	V
		CREG2 = 2.7 V default setting	3.0	-	25.0	V
		CREG2 = 3.3 V setting	4.0	-	25.0	V
	GND	GND0, VSS	-	0.0	-	V

Caution To ensure the stable transition from Power down mode to Normal mode, VCC pin voltage must be 3.0 V or more.

4.3 Supply current characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power down mode current 1	I_{PD}	VCC = 14.0 V	-	-	2.0	uA
Power down mode current 2 (Low voltage)	I_{PDL}	VCC = 4.0 V	-	-	1.0	uA
Sleep mode current 1	I_{SLP1}	MCU operation mode: STOP mode AFE operation mode: Low power operation mode Note ALOCO = ON, AOCO = OFF CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = L, DFOUT = L, AD(AFE) = OFF, CC = OFF	-	20.0	40.0	uA
Sleep mode current 2	I_{SLP2}	MCU operation mode: STOP mode AFE operation mode: Low power operation mode Note ALOCO = ON, AOCO = OFF CD = ALL ON, AFE timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = OFF, CC = OFF	-	40.0	80.0	uA
Normal mode current	I_{NOM}	MCU operation mode: LS (Low-Speed main) mode, f_{HOCO} = 8 MHz AFE operation mode: Normal operation mode ALOCO = ON, AOCO = ON CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = ON, CC = ON	-	2.0	3.0	mA

Note "Sleep mode current 1 and 2" is the current consumption when PCON register value is set to "63H".

Caution After trimming.

4.4 Oscillator Characteristics

4.4.1 MCU On-chip oscillator characteristics

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1, 2	f_{IH}		1	-	32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20°C ≤ T_A ≤ 85°C	-1.0	-	+1.0	%
		-40°C ≤ T_A ≤ 85°C	-1.5	-	+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}		-	15	-	kHz
Low-speed on-chip oscillator clock frequency accuracy			-15	-	+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.4.2 AFE On-chip oscillator characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AFE on-chip oscillator clock frequency	f_{AOCO}		-	4.194	-	MHz
AFE on-chip oscillator clock frequency accuracy			-2	-	+2	%
AFE Low-speed on-chip oscillator clock frequency	f_{ALOCO}		-	131.072	-	kHz
AFE Low-speed on-chip oscillator clock frequency accuracy			-5	-	+5	%

Caution After trimming.

Remark Values in brackets are design value.

4.5 Pin characteristics

(1/5)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P10 to P12, P16, P17, P40		-	-	-10.0 Note 2	mA
		Total of P10 to P12, P16, P17, P40 (When duty ≤70% Note 3)	CREG2 = 3.3 V setting	-	-	-19.0	mA
			CREG2 = 2.0 V setting	-	-	-10.0	mA
		Total of all pins (When duty ≤70% Note 3)		-	-	-100.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current from pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

Total output current from pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.
A current higher than the absolute maximum rating must not flow into any one pin.

Caution **P10 to P12, P16 and P17 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/5)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P10 to P12, P16, P17, P40		-	-	20.0 Note 2	mA
		Per pin for P60, P61, P62		-	-	15.0 Note 2	mA
		Total of P10 to P12, P16, P17, P40, P60, P61, P62 (When duty ≤ 70% Note 3)	CREG2 = 3.3 V setting	-	-	35.0	mA
			CREG2 = 2.0 V setting	-	-	20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)		-	-	150.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/5)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P12, P16, P17, P40	Normal input buffer	0.8 VDD	-	VDD	V
	V_{IH2}	P10 to P11, P16, P17	TTL input buffer	1.5	-	VDD	V
	V_{IH3}	P60, P61		1.35	-	VDD	V
	V_{IH4}	P62		0.7 VDD	-	VDD	V
	V_{IH5}	P137, RESET		0.8 VDD	-	VDD	V
Input voltage, low	V_{IL1}	P10 to P12, P16, P17, P40	Normal input buffer	0	-	0.2 VDD	V
	V_{IL2}	P10 to P12, P16, P17	TTL input buffer	0	-	0.32	V
	V_{IL3}	P60, P61		0	-	0.54	V
	V_{IL4}	P62		0	-	0.3 VDD	V
	V_{IL5}	P137, RESET		0	-	0.2 VDD	V

Caution The maximum value of VIH of pins P10 to P12, P16 and P17 is VDD, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(4/5)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P10 to P12, P16, P17, P40	IOH1 = -1.5 mA	VDD - 0.5	-	-	V
Output voltage, low	V_{OL1}	P10 to P12, P16, P17, P40	CREG2 = 3.3 V setting IOL1 = 3.0 mA	-	-	0.6	V
			CREG2 = 3.3 V setting IOL1 = 1.5 mA	-	-	0.4	V
			CREG2 = 2.0 V setting IOL1 = 0.6 mA	-	-	0.4	V
	V_{OL2}	P60, P61, P62	CREG2 = 3.3 V setting IOL2 = 3.0 mA	-	-	0.4	V
			CREG2 = 2.0 V setting IOL2 = 2.0 mA	-	-	0.4	V

Caution P10 to P12, P16 and P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(5/5)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P10 to P12, P16, P17, P40, P137	VI = VDD	-	-	1	uA
Input leakage current, low	I_{LIL1}	P10 to P12, P16, P17, P40, P137	VI = VSS	-	-	-1	uA
On-chip pull-up resistance	R_U	P10 to P12, P16, P17, P40	VI = VSS, In input port	10	20	100	kΩ
	R_{UA0}	AN0, AN1, AN2		7.5	10	12.5	kΩ
	R_{UA1}	RESET/RESETOUT		-	20	-	kΩ
On-chip pull-down resistance	R_D	P60, P61		-	1	-	MΩ

Remark 1. Unless specified, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. Regarding pin characteristics of CFOUT, DFOUT, refer to Section 4.8.7 Charge/discharge FET control circuit characteristics.

Remark 3. Regarding pin characteristics of VIN1 to VIN4 refer to Section 4.8.2 Multiplexer.

Remark 4. Regarding pin characteristics of FUSEOUT and SYSIN refer to Section 4.8.1 High-voltage port characteristics.

4.6 AC Characteristics

(1/2)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

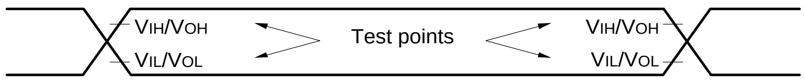
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125	-	1	us
				2.4 V ≤ VDD ≤ 5.5 V	0.0625	-	1	us
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125	-	1	us
			LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.25	-	1	us
		Subsystem clock (f_{SUB}) operation			28.5	30.5	31.3	us
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125	-	1	us
				2.4 V ≤ VDD ≤ 5.5 V	0.0625	-	1	us
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125	-	1	us
			LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 5.5V	0.25	-	1	us

(2/2)

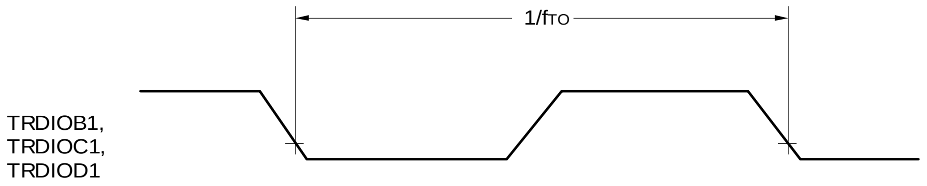
(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

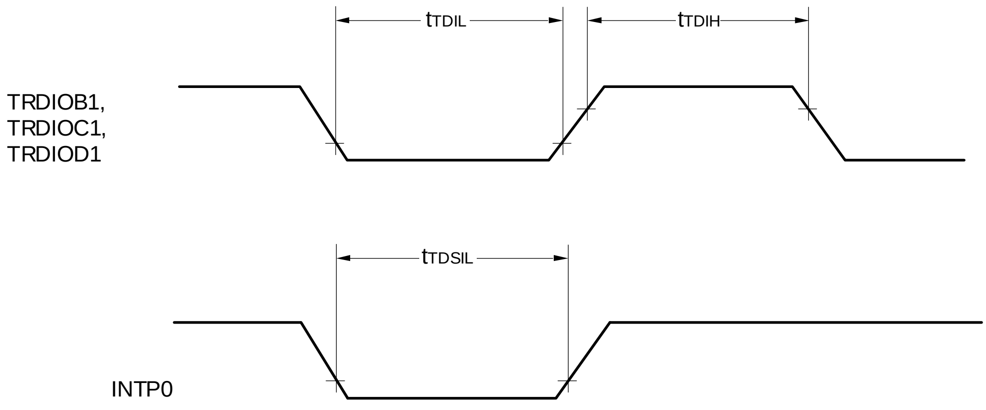
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOB1, TRDIOC1, TRDIOD1		$3/f_{CLK}$	-	-	ns
Timer RD forced cutoff signal input low-level width	t_{TDSIL}	P61/INTP0	2 MHz < f_{CLK} ≤ 32 MHz	1	-	-	us
			f_{CLK} ≤ 2 MHz	$1/f_{CLK}$ + 1	-	-	
TRDIOB1, TRDIOC1, TRDIOD1 output frequency	f_{TO}	HS (high-speed main) mode		-	-	8	MHz
		LS (low-speed main) mode		-	-	4	MHz
		LV(low-voltage main) mode		-	-	2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP13		1	-	-	us
RESET low-level width	t_{RSL}			10	-	-	us

AC Timing Test Points

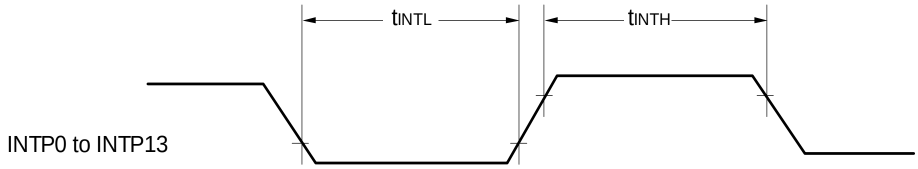


TI/TO Timing

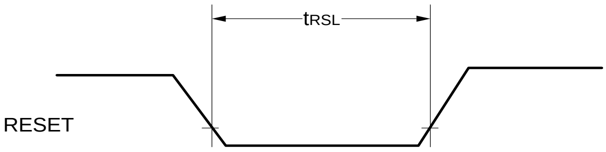




Interrupt Request Input Timing



RESET Input Timing



4.7 MCU peripheral circuit characteristics

AC Timing Test Points

4.7.1 Serial array unit

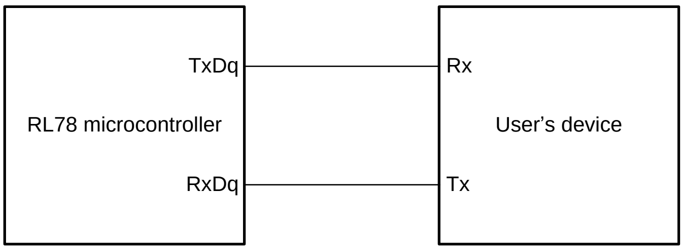
(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

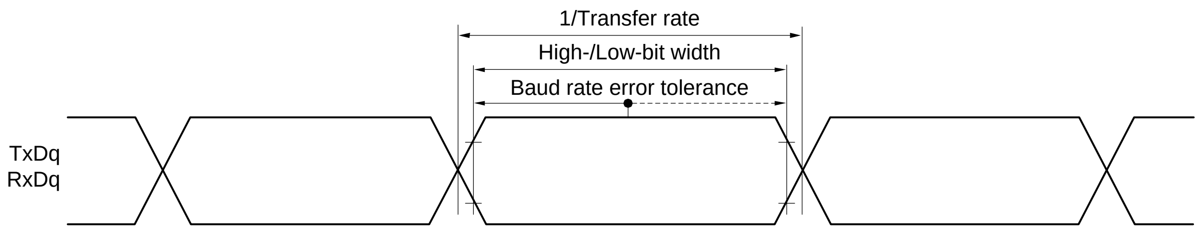
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note			-	$f_{MCK}/6$	-	$f_{MCK}/6$	-	$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$	-	5.3	-	1.3	-	0.6	Mbps

Note Transfer rate in the SNOOZE mode is only 4800 bps.

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).



UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

Remark 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	125	-	500	-	1000	-	ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2$ - 18	-	$t_{KCY1}/2$ - 50	-	$t_{KCY1}/2$ - 50	-	ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}		44	-	110	-	110	-	ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		19	-	19	-	19	-	ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	-	25	-	25	-	25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution. Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 10), m: Unit number (m = 0), n: Channel number (n = 2), g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 02))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	1 MHz < f_{MCK}	8/f_{MCK}	-	—	-	—	-	ns
		f_{MCK} ≤ 16 MHz	6/f_{MCK}	-	6/f_{MCK}	-	6/f_{MCK}	-	ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2 - 8	-	t_{KCY2}/2 - 8	-	t_{KCY2}/2 - 8	-	ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}		1/f_{MCK} + 20	-	1/f_{MCK} + 30	-	1/f_{MCK} + 30	-	ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}		1/f_{MCK} + 31	-	1/f_{MCK} + 31	-	1/f_{MCK} + 31	-	ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30pF Note 4	-	2/f_{MCK} + 44	-	2/f_{MCK} + 110	-	2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

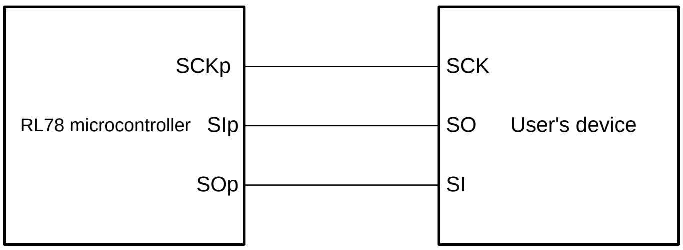
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution. Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 10), m: Unit number (m = 0), n: Channel number (n = 2),
g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 02))

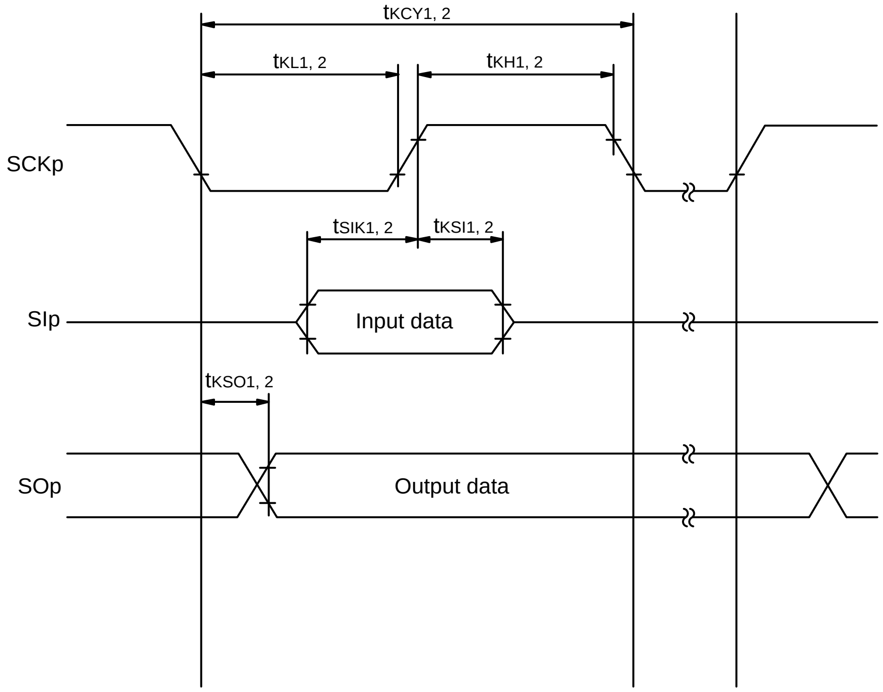


CSI mode connection diagram (during communication at same potential)

Remark 1. p: CSI number (p = 10)

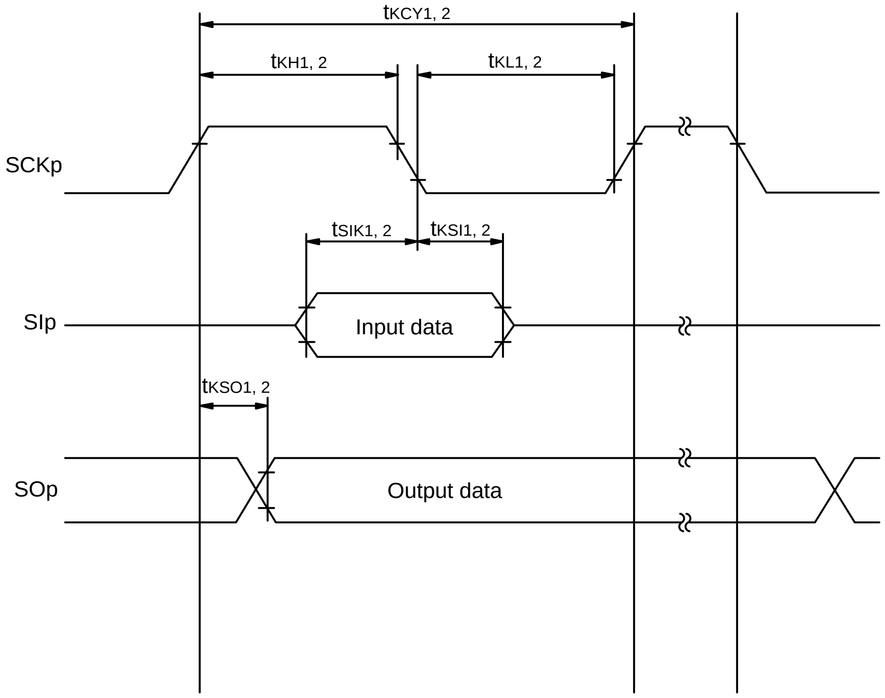
Remark 2. m: Unit number, n: Channel number (mn = 02)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



CSI mode serial transfer timing (during communication at same potential)

Remark 1. p: CSI number (p = 10)

Remark 2. m: Unit number, n: Channel number (mn = 02)

(4) During communication at same potential (simplified I²C mode)

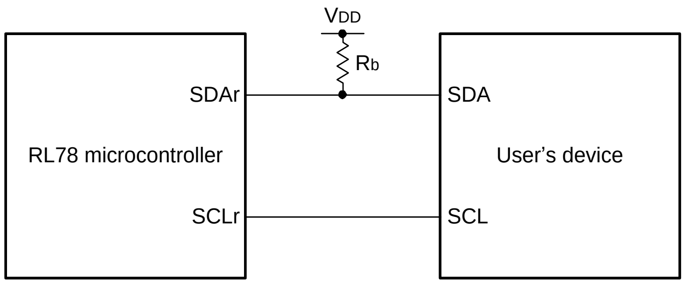
(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	Cb = 50pF, Rb = 2.7kΩ	-	1000 Note 1	-	400 Note 1	-	400 Note1	kHz
Hold time when SCLr = “L”	t_{LOW}	Cb = 50pF, Rb = 2.7kΩ	475	-	1150	-	1150	-	ns
Hold time when SCLr = “H”	t_{HIGH}	Cb = 50pF, Rb = 2.7kΩ	475	-	1150	-	1150	-	ns
Data setup time (reception)	$t_{SU:DAT}$	Cb = 50pF, Rb = 2.7kΩ	$1/f_{MCK}$ + 85 Note 2	-	$1/f_{MCK}$ + 145 Note 2	-	$1/f_{MCK}$ + 145 Note2	-	ns
Data hold time (transmission)	$t_{HD:DAT}$	Cb = 50pF, Rb = 2.7kΩ	0	305	0	305	0	305	ns

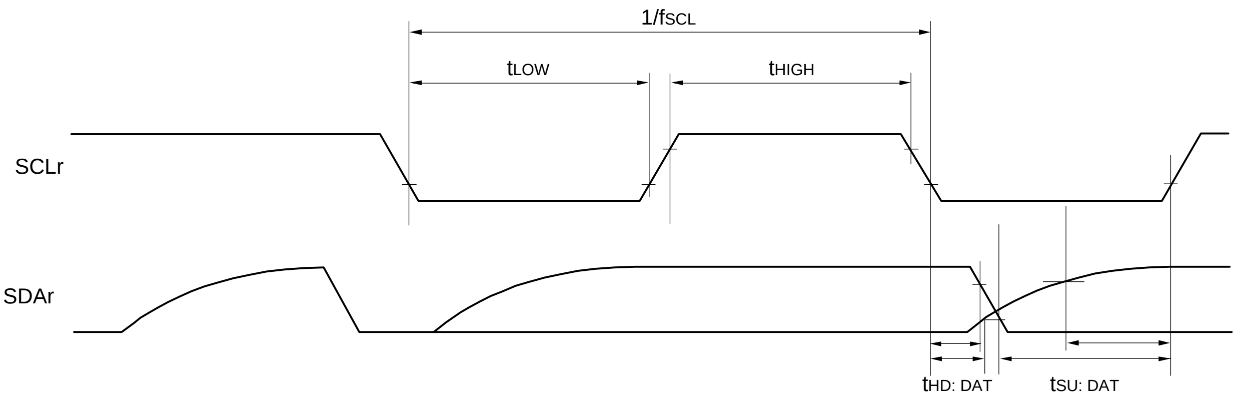
Note 1. The value must also be equal to or less than $f_{MCK}/4$.

Note 2. Set the f_{MCK} value not to over the hold time of SCLr = “L” and SCLr = “H”.

Caution. Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)

Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 10), g: PIM number (g = 1), h: POM number (h = 1)

Remark 3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 2), mn = 02)

4.7.2 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: $f_{CLK} \geq$ 1MHz	0	100	0	100	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7	-	4.7	-	4.7	-	us
Hold time Note 1	$t_{HD: STA}$		4.0	-	4.0	-	4.0	-	us
Hold time when SCLA0 = “L”	t_{LOW}		4.7	-	4.7	-	4.7	-	us
Hold time when SCLA0 = “H”	t_{HIGH}		4.0	-	4.0	-	4.0	-	us
Data setup time (reception)	$t_{SU: DAT}$		250	-	250	-	250	-	ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	3.45	0	3.45	us
Setup time of stop condition	$t_{SU: STO}$		4.0	-	4.0	-	4.0	-	us
Bus-free time	t_{BUF}		4.7	-	4.7	-	4.7	-	us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400pF, Rb = 2.7kΩ

(2) I²C fast mode

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: fCLK ≥ 3.5 MHz	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$		0.6	-	0.6	-	0.6	-	us
Hold time[Note1]	$t_{HD: STA}$		0.6	-	0.6	-	0.6	-	us
Hold time when SCLA0 = “L”	t_{LOW}		1.3	-	1.3	-	1.3	-	us
Hold time when SCLA0 = “H”	t_{HIGH}		0.6	-	0.6	-	0.6	-	us
Data setup time (reception)	$t_{SU: DAT}$		100	-	100	-	100	-	ns
Data hold time (transmission) Note2	$t_{HD: DAT}$		0	0.9	0	0.9	0	0.9	us
Setup time of stop condition	$t_{SU: STO}$		0.6	-	0.6	-	0.6	-	us
Bus-free time	t_{BUF}		1.3	-	1.3	-	1.3	-	us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: Cb = 320pF, Rb = 1.1kΩ

(3) I^2C fast mode plus

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

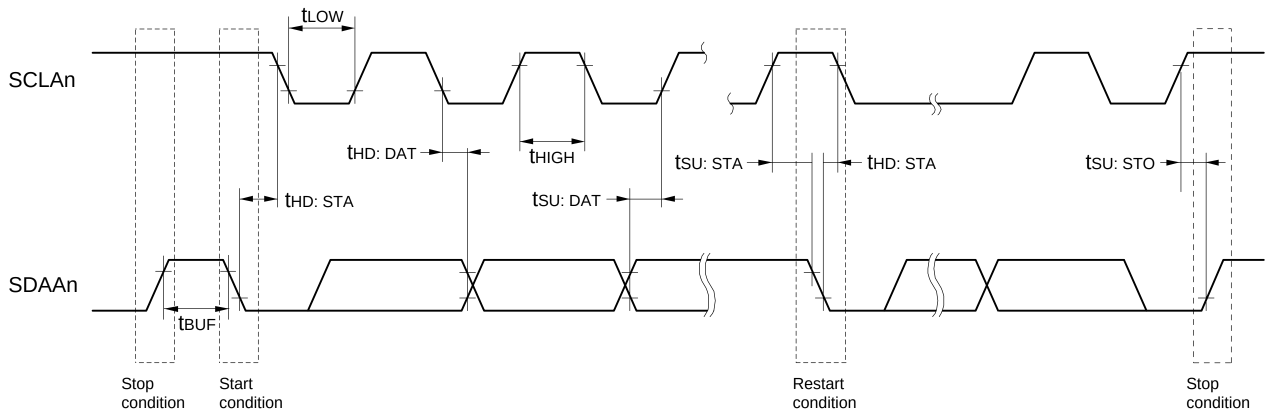
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: $f_{CLK} \geq 10$ MHz	0	1000	-		-		kHz
Setup time of restart condition	$t_{SU: STA}$		0.26	-	-		-		us
Hold time Note 1	$t_{HD: STA}$		0.26	-	-		-		us
Hold time when SCLA0 = "L"	t_{LOW}		0.5	-	-		-		us
Hold time when SCLA0 = "H"	t_{HIGH}		0.26	-	-		-		us
Data setup time (reception)	$t_{SU: DAT}$		50	-	-		-		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	0.45	-		-		us
Setup time of stop condition	$t_{SU: STO}$		0.26	-	-		-		us
Bus-free time	t_{BUF}		0.5	-	-		-		us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: Cb = 120pF, Rb = 1.1kΩ



IICA serial transfer timing

Remark n = 0

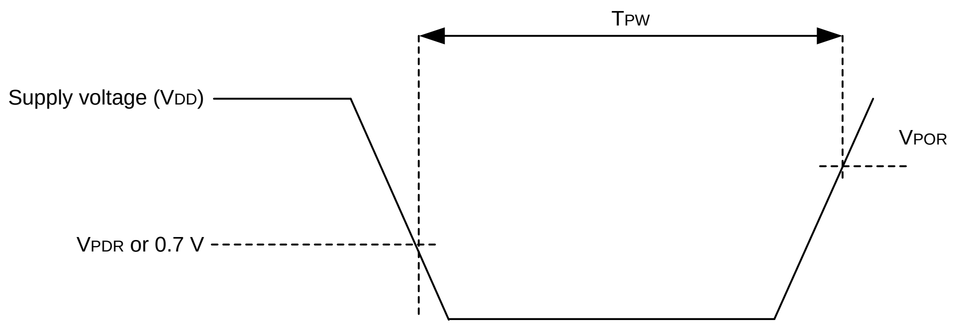
4.7.3 POR circuit characteristics (MCU)

(T_A = -40 to +85°C, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	V_{PDR}	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW}		300	-	-	us

Note 1. However, when operating voltage drops when LVD is off, it enters STOP mode, or enable the reset status using external reset pin before the voltage drops below the operating voltage range shown in Section 4.6 AC Characteristics.

Note 2. Minimum time required for POR to reset when VDD is below VPDR. This is also the minimum time required for a POR reset when VDD exceeds VPOR after VDD is below 0.7 V during STOP mode or while the main system clock is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.7.4 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T_A= -40 to +85°C, VPDR ≤ CREG2 = VDD ≤ 5.5 V, GND0 = VSS= 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVI0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVI1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVI2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVI3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVI4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVI5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVI6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVI7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVI8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVI9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVI10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVI11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVI12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVI13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300	-	-	us
Detection delay time		t_{LD}		-	-	300	us

(2) Interrupt & Reset Mode

(T_A= -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, GND0 = VSS= 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V_{LVDA0}	VPOC2, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V_{LVDA1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

4.8 Analog front end peripheral circuit characteristics

4.8.1 High-voltage port characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH0}	FUSEOUT	2.0	-	VCC	V
	V_{IH1}	SYSIN	1.2	-	-	V
Input voltage, low	V_{IL0}	FUSEOUT	0.0	-	0.6	V
	V_{IL1}	SYSIN	0.0	-	0.5	V
Output voltage, high	V_{OH0}	FUSEOUT, IOH = -1mA	VCC-0.7	-	VCC	V
Pin leakage current	I_{LK}	FUSETOUT, VI=VCC, GND	-	-	±1	uA

4.8.2 Multiplexer characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain VIN(n)-VIN(n-1)	GAIN1	VIN4,VIN3 ≥ 2.0 V VIN2,VIN1 ≥ 0 V Note	-	1.0	-	V/V
Gain VBAT, VIN12	GAIN2		-	0.2	-	V/V
Gain AN0,1,2	GAIN3		-	1.0	-	V/V
Gain AN3	GAIN4		-	0.5	-	V/V
Input voltage range VIN(n)-VIN(n-1)	VRA1		-0.1	-	5.1	V
Input voltage range VBAT, VIN12	VRA2		0.0	-	25.0	V
Input voltage range AN0, 1, 2	VRA3		0.0	-	1.8	V
Input voltage range AN3	VRA4		0.0	-	10	V
Pin input current VBAT, VIN12	I_{IN0}	VBAT and VIN12 pins = 25.0 V when target pin selected	-	200 (125)	-	uA (KΩ)
Pin input current AN3	I_{IN1}	AN3 pin = 5.0 V when target pin selected	-	100 (50)	-	uA (KΩ)
Pin leakage current	I_{LKV1}	VIN1=5.0 V	-	-	1	uA
		VIN2=10.0 V	-	-	1	uA
		VIN3=15.0 V	-	-	1	uA
		VIN4=20.0 V	-	-	1	uA

Note Reference voltage is GND0

4.8.3 Simple temperature sensor characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output	V_{TEMP}	T_A = 25°C	-	0.74	-	V
Temperature coefficient	F_{VTEMP}		-	-1.57	-	mV/°C

Note Reference voltage is GND0

4.8.4 Sigma-delta A/D converter characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution Note1	RESAD	Conversion time = 8 ms	-	-	15	bits
		Conversion time = 4 ms	-	-	14	bits
		Conversion time = 2 ms	-	-	13	bits
		Conversion time = 1 ms	-	-	12	bits
		Conversion time = 0.5 ms	-	-	11	bits
		Conversion time = 0.25 ms	-	-	10	bits
Input voltage range	VINAD		-0.1	-	5.1	V
Integral nonlinearity	INLAD	Input range -0.1 V to 5.1 V, End fit	-27	-	27	LSB
Conversion result in zero input	ADZERO	VIN=0 V	-	3275 Note 2	-	LSB
Temperature dependency In zero input	dTADZERO	VIN=0 V	-0.24	-	+0.24	LSB/°C
Conversion result in full-scale input	ADFS	VIN=5.1 V	-	31002 Note 2	-	LSB
Temperature dependency in full-scale input	dTADFS	VIN=5.1 V	-0.24	-	+0.24	LSB/°C
Input resistance	RINAD		-	(1.0)	-	MΩ
Battery cell voltage measurement error	ERRCELL1	T_A = +25°C After calibration	-	-	±5	mV
	ERRCELL2	-20°C ≤ T_A ≤ 85°C After calibration	-	-	±10	mV
	ERRCELL2L	-40°C ≤ T_A ≤ 85°C After calibration	-	-	±12	mV

Note 1. AD conversion result is output in 15-bit.

Note 2. This value is before subtracting the offset voltage.

Caution 1. Except for Battery cell voltage measurement error (ERRCELL), these parameters are sigma-delta converter circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in brackets are design value.

4.8.5 Current integrating circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RESCC		-	-	18	bits
Conversion time	TCC		-	250	-	ms
Input voltage range	VINCC	±25 mV mode ISENS1 to ISENS0	-25	-	+25	mV
		±50mV mode ISENS1 to ISENS0	-50	-	+50	mV
Integral nonlinearity	INLCC	End fit	-	-	0.02	%FSR
Input resistance	RINCC	ISENS0, ISENS1	-	(1.0)	-	MΩ

Caution 1. These parameters are current integration circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in brackets are design value.

4.8.6 Overcurrent detection / wakeup current detection circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current detection 0 setting voltage step	dSVSC0	50 mV to 300 mV	-	25.0	-	mV
Discharge short-circuit current detection 0 voltage error	dVSC0	50 mV to 300 mV setting	-	-	±25.0	mV
Discharge short-circuit current detection 1 setting voltage step	dSVSC1	15 mV to 50 mV	-	5.0	-	mV
		50 mV to 100 mV	-	10.0	-	mV
		100 mV to 200 mV	-	25.0	-	mV
Discharge short-circuit current detection 1 voltage error Note 1	dVSC1	15 mV to 50 mV setting	-	-	±5.0	mV
		60 mV to 100 mV setting			±10.0	mV
		125 mV to 200 mV setting	-	-	±25.0	mV
Discharge overcurrent detection setting voltage step	dSVDOC	10 mV to 70 mV	-	2.5	-	mV
Discharge overcurrent detection voltage error Note 1	dVDOC	10 mV to 70 mV setting	-	-	±5.0	mV
Charge overcurrent detection setting voltage step	dSVCOC	-50 mV to -15 mV	-	5.0	-	mV
		-100 mV to -50.0 mV	-	10.0	-	mV
		-200 mV to -100 mV	-	25.0	-	mV
Charge overcurrent detection voltage error Note 1	dVCOC	-50 mV to -15 mV setting	-	-	±5.0	mV
		-100 mV to -60.0 mV setting			±10.0	mV
		-200 mV to -125 mV setting	-	-	±25.0	mV
Discharge wakeup current detection setting voltage step	dSVDWU	0 mV to 140 mV	-	1.25	-	mV
Charge wakeup current detection setting voltage step	dSVCWU	-140 mV to 0 mV	-	1.25	-	mV
DBPT current detection setting voltage step	dSVDBPT	0 mV to 140 mV	-	1.25	-	mV
Discharge wakeup current detection voltage error Note 1	dVDWU	20 times mode ISENS1 to ISENS0: 0.25mV	-0.20	0.0	+0.15	mV
		20 times mode ISENS1 to ISENS0: 0.3125mV to 2.5mV	-0.30	0.0	+0.15	mV
Charge wakeup current detection voltage error Note 1	dVCWU	20 times mode ISENS1 to ISENS0: -0.25mV	-0.15	0.0	+0.20	mV
		20 times mode ISENS1 to ISENS0: -0.3125mV to -2.5mV	-0.15	0.0	+0.30	mV
DBPT current detection voltage error Note 1	dVDBPT	20 times mode ISENS1 to ISENS0: 0.25mV	-0.20	0.0	+0.15	mV
		20 times mode ISENS1 to ISENS0: 0.3125mV to 2.5mV	-0.30	0.0	+0.15	mV
Discharge short-circuit current detection 0 time error Note 2	dTSC0	0 us to 916 us (61 us step)	0.0	-	30.5	us
Discharge short-circuit current detection 1 time error Note 2	dTSC1	0 us to 1892 us (61 us step)	0.0	-	30.5	us
Discharge overcurrent detection time error Note 2	dTDOC	0.916 ms to 61.462 ms (1.952 ms step)	0.0	-	30.5	us
Charge overcurrent detection time error	dTCOC	0 us to 1892 us (61 us step)	0.0	-	30.5	us
Discharge wakeup current detection time error Note 2	dTDWU	3.91 ms to 62.56 ms (3.91 ms step)	-3.91	-	0	ms
Charge wakeup current detection time error Note 2	dTCWU	3.91 ms to 62.56 ms (3.91 ms step)	-3.91	-	0	ms
DBPT current detection time error Note 2	dTDBPT	0 us to 916 us (61 us step)	0.0	-	30.5	us

Note 1. This is the specification after zero-calibration is executed.

Note 2. The frequency error of On-chip oscillator (AOCO and ALOCO) is excluded from these detection time error.

4.8.7 Charge/discharge FET control circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-side Charge FET control Output voltage, CFOUT=H	CFON1	2.2 V ≤ VCC < 5.0 V Load between CFOUT to VBAT = 4.7nF/10MΩ Based on VBAT pin	4.0	(10.0)	12.0	V
	CFON2	5.0 V ≤ VCC Load between CFOUT to VBAT = 4.7nF/10MΩ Based on VBAT pin	9.0	(10.0)	12.0	V
High-side Charge FET control Output voltage, CFOUT=L	CFOFF	Load between CFOUT to VBAT = 4.7nF/10MΩ Based on VBAT pin	-	0.0	+0.2	V
High-side Charge FET control CFOUT rise Time	CFTR1	2.2 V ≤ VCC < 5.0 V Load between CFOUT to VBAT = 4.7nF/10MΩ Lo(VBAT)→Hi(VBAT + 3 V)	-	1.5	3.0	ms
	CFTR2	5.0 V ≤ VCC Load between CFOUT to VBAT = 4.7nF/10MΩ Lo(VBAT)→Hi(VBAT + 4 V)	-	(0.2)	0.6	ms
High-side Charge FET control CFOUT fall Time	CFTF	Load between CFOUT to VBAT = 4.7nF/10MΩ Hi(VBAT+CFON1)→Lo(VBAT + 1 V)		(0.08)	0.2	ms
High-side Discharge FET control Output voltage, DFOUT=H	DFON1	2.2 V ≤ VCC < 5.0 V Load between DFOUT to VIN12 = 4.7nF/10MΩ Based on VIN12 pin	4.0	(10.0)	12.0	V
	DFON2	5.0 V ≤ VCC Load between DFOUT to VIN12 = 4.7nF/10MΩ Based on VIN12 pin	9.0	(10.0)	12.0	V
High-side Discharge FET control Output voltage, DFOUT=L	DFOFF	Load between DFOUT to VIN12 = 4.7nF/10MΩ Based on VIN12 pin	-	0.0	+0.2	V
High-side Discharge FET control DFOUT rise Time	DFTR1	2.2 V ≤ VCC < 5.0 V Load between DFOUT to VIN12 = 4.7nF/10MΩ Lo(VIN12)→Hi(VIN12 + 3 V)	-	1.5	3.0	ms
	DFTR2	5.0 V ≤ VCC Load between DFOUT to VIN12 = 4.7nF/10MΩ Lo(VIN12)→Hi(VIN12 + 4 V)	-	(0.2)	0.6	ms
High-side Discharge FET control DFOUT fall Time	DFTF	Load between DFOUT to VIN12 = 4.7nF/10MΩ Hi(VIN12+CFON1)→Lo(VIN12 + 1 V)		(0.08)	0.2	ms

Caution. After trimming.

4.8.8 Power on circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, High	V_{IH}	VIN12 pin	3.0	-	VCC	V
Input voltage, Low	V_{IL}	VIN12 pin	0.0	-	1.0	V
Pull-down resistance	Rdpon1	After Power down mode release and VIN12PDEN bit of PINSEL register = 0	-	12.36	-	MΩ
	Rdpon2	Power down mode and VIN12PDEN bit of PINSEL register = 1	-	100	-	KΩ

Caution. To entry power down mode, it is necessary to input power down command while VIN12 port is L.

4.8.9 Series regulator circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	VR2O	CREG2 = 3.3 V setting, 4.0 V ≤ VCC, Io=50 uA to 20 mA	3.20	3.30	3.40	V
		CREG2 = 2.7 V Wakeup setting, 3.0 V ≤ VCC, Io=50 uA to 20 mA	2.55	2.7	2.8	V
		CREG2 = 2.0 V setting, 2.2 V ≤ VCC, Io=50 uA to 20 mA	1.9	2.0	2.05	V
Load drive capability Note	IOMAX	CREG2 = 3.3 V setting, 4.0 V ≤ VCC < 4.5 V, 3.20 V ≤ CREG2 ≤ 3.40 V	20.0	-	-	mA
		CREG2 = 3.3 V setting, 4.5 V ≤ VCC < 25.0 V, 3.20 V ≤ CREG2 ≤ 3.40 V	30.0	-	-	mA
		CREG2 = 2.0 V setting, 2.2 V ≤ VCC < 2.7 V, 1.90 V ≤ CREG2 ≤ 2.05 V	20.0	-	-	mA
		CREG2 = 2.0 V setting 2.7 V ≤ VCC < 25.0 V, 1.90 V ≤ CREG2 ≤ 2.05 V	30.0	-	-	mA

Note In case of using load drive, total power consumption must be under the maximum ratings power consumption (Pd).

Caution. After trimming.

4.8.10 AFE reset circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 release voltage	V_{REL}		1.85	-	-	V
VREG2 detection voltage	V_{DET}	After trimming	1.75	-	-	V

4.8.11 Cell balancing circuit characteristics

(T_A = -40 to +85°C, 2.2 V ≤ VCC ≤ 25.0 V, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
1st cell on resistance	R_{COND1}	VCC ≥ 5 V VIN1 – GND0 = 3.5 V Note	-	100	200	Ω
2nd cell on resistance	R_{COND2}	VIN2 ≥ 5 V VIN2 – VIN1 = 3.5 V Note	-	100	200	Ω
3rd cell on resistance	R_{COND3}	VIN3 ≥ 5 V VIN3 – VIN2 = 3.5 V Note	-	100	200	Ω
4th cell on resistance	R_{COND4}	VIN4 ≥ 5 V VIN4 – VIN3 = 3.5 V Note	-	100	200	Ω

Note This is the voltage before the cell conditioning switch is turned on.

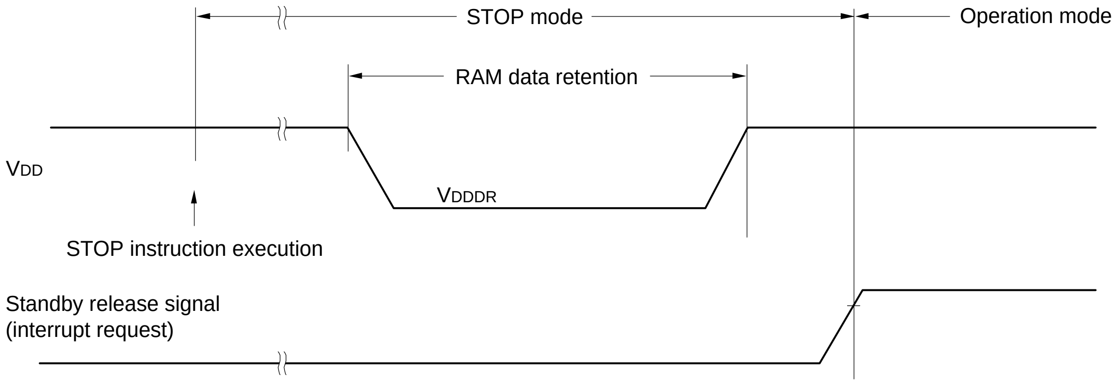
Caution This is the specification when a 100 Ω resistor is placed between each battery cell and VIN4 to VIN1 in series, and one cell conditioning switch is turned on.

4.9 RAM Data Retention Characteristics

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note	-	5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



4.10 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1	-	32	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C	1,000	-	-	Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 year T_A = 25 C	-	1,000,000	-	
		Retained for 5 years T_A = 85°C	100,000	-	-	
		Retained for 20 years T_A = 85°C	10,000	-	-	

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retained years are until next rewrite completion.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4.11 Dedicated Flash Memory Programmer Communication (UART)

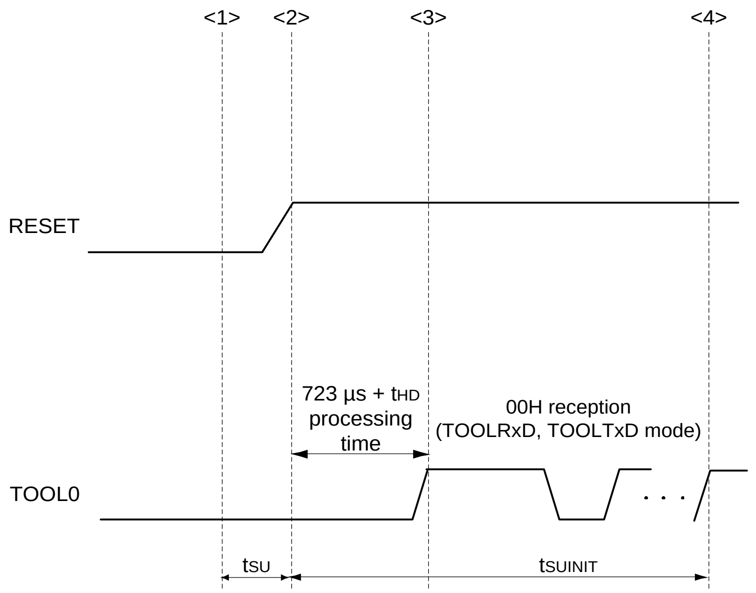
(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200	-	1,000,000	bps

4.12 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, VDD = CREG2, GND0 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
The time needed when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.	-	-	100	ms
The time needed from when the TOOL0 pin is placed at low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10	-	-	us
The time needed for the TOOL0 pin must be kept at low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1	-	-	ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tSUINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tSU: Time needed for the TOOL0 pin is placed at low level until the pin reset ends

tHD: Time needed for the TOOL0 pin at low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

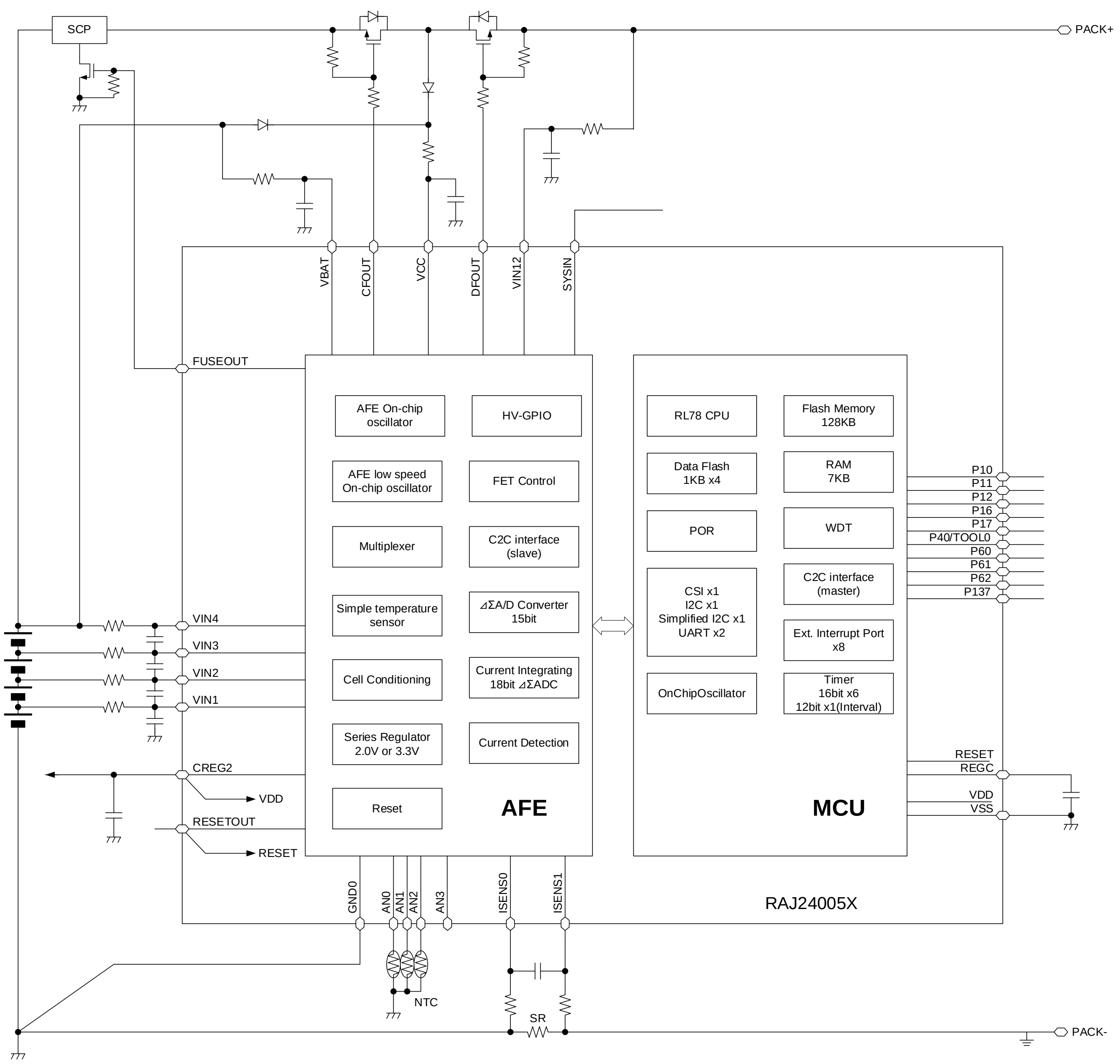
CHAPTER 5. DETAILED DESCRIPTION

5.1 Overview

RAJ24005X is a Renesas Li-ion battery fuel gauge IC (FGIC) which consists of an MCU device and an AFE device in a single package. These devices integrate a variety of battery management features.

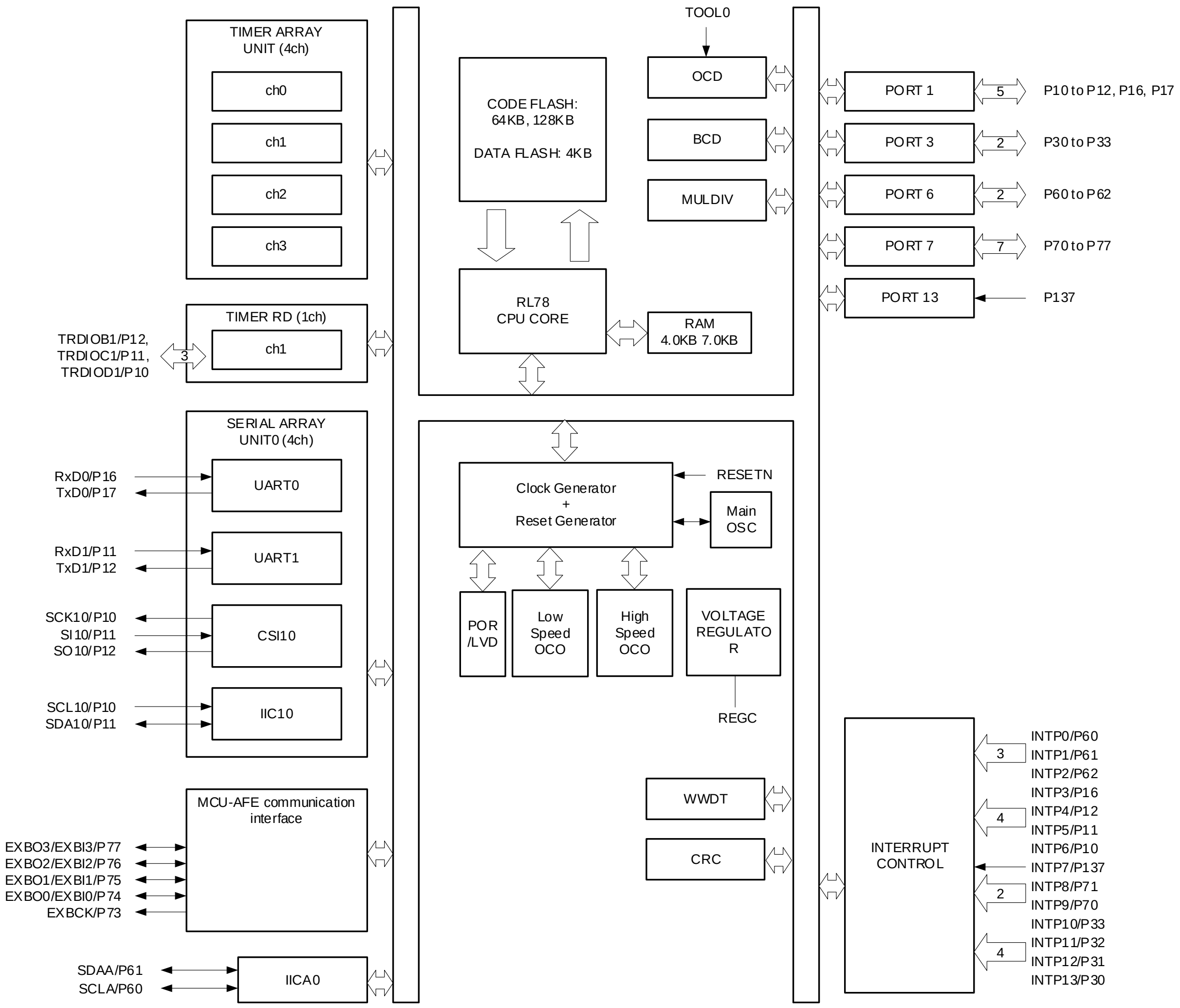
5.2 Block diagram

5.2.1 System block diagram



Caution **This example of a peripheral circuit does not guarantee the operation of this device. Evaluate the operation adequately with actual applications, and then determine the circuits and constants.**

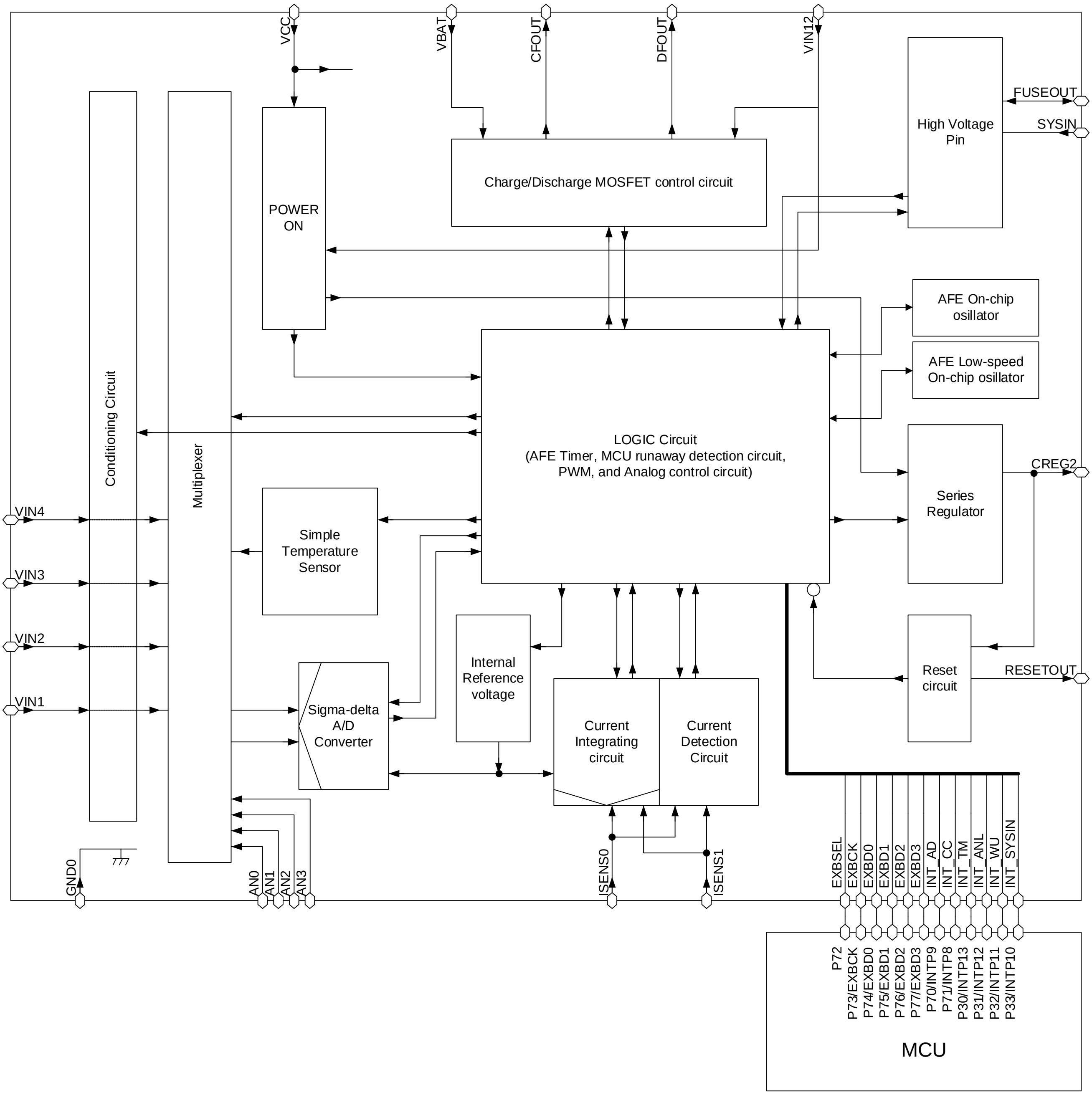
5.2.2 MCU block diagram



Caution 1. **P30 to P31, P70 to P77 are connected to AFE chip in the package and not connected to the package external pin.**

Caution 2. **Each interrupt request of AFE is assigned to P71/INTP8, P70/INTP9, P33/INTP10, P32/INTP11, P31/INTP12, P30/INTP13.**

5.2.3 AFE block diagram



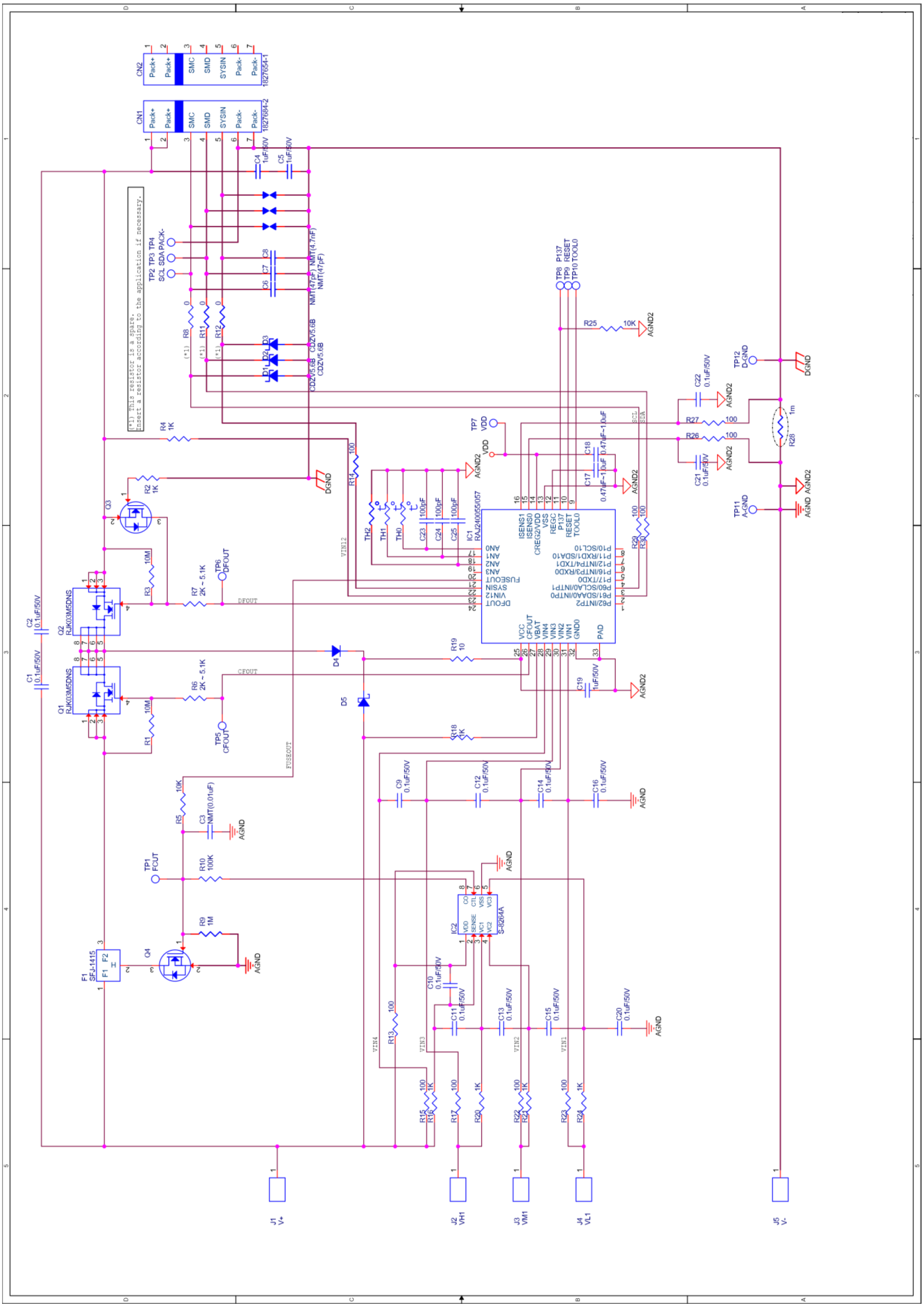
CHAPTER 6. APPLICATION GUIDELINE

6.1 Typical Application Specification

A typical specification example of Li-ion battery management unit as shown below.
From the next page, the typical application guideline is explained for RAJ240055/57.

Battery cell assembly	4S1P	
Host Interface	System Management Bus (SMBus) Specification, version 3.0.	
	UART (* Regarding UART, there is no typical application specification in this section)	
Primary protection	Charge FET and Discharge FET	
Secondary protection	Fuse blow by FGIC or a secondary protection device.	
Connect pins	Pack+	Positive battery pack terminal
	SMC	SMBus clock
	SMD	SMBus data
	SYSIN	Battery insertion detection
	Pack-	Negative battery pack terminal
Additional Features	External reverse charge protection circuit	
	Battery and charge/discharge MOSFET temperature measurement with three thermistors	

<R> 6.2 Typical Application Circuit

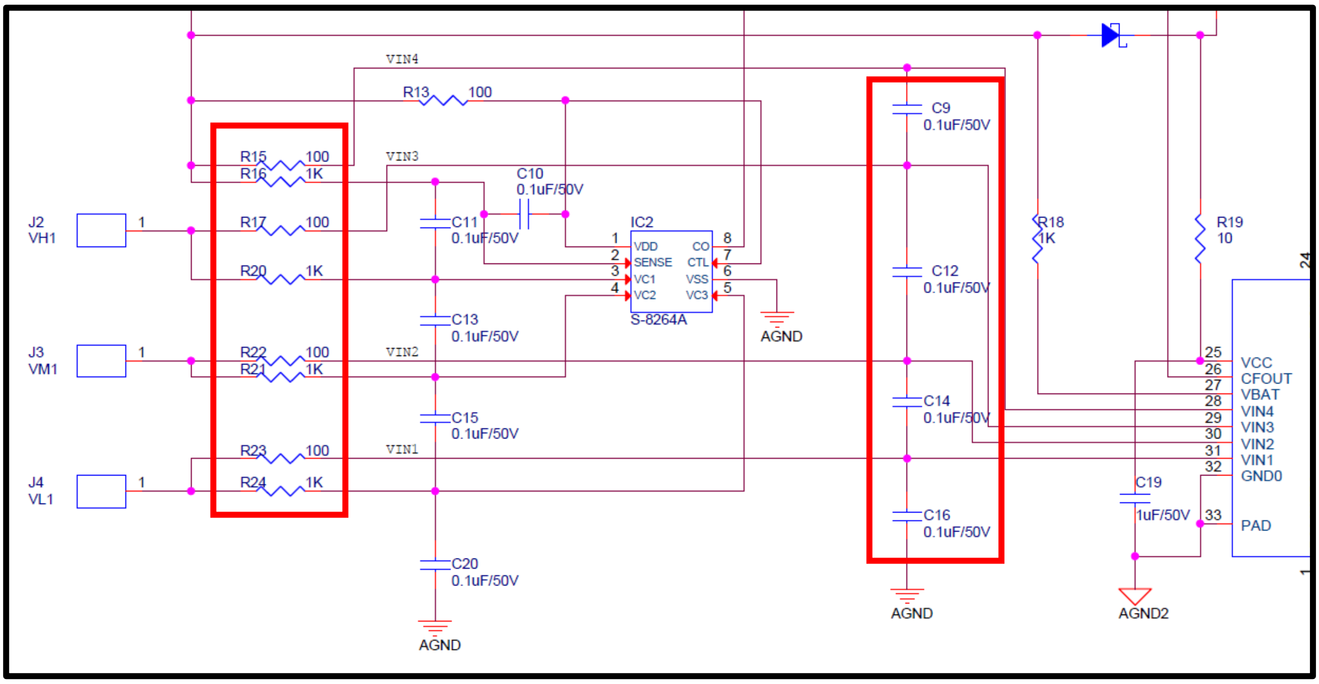


6.3 Circuit Design Guideline

6.3.1 Cell voltage monitor circuit

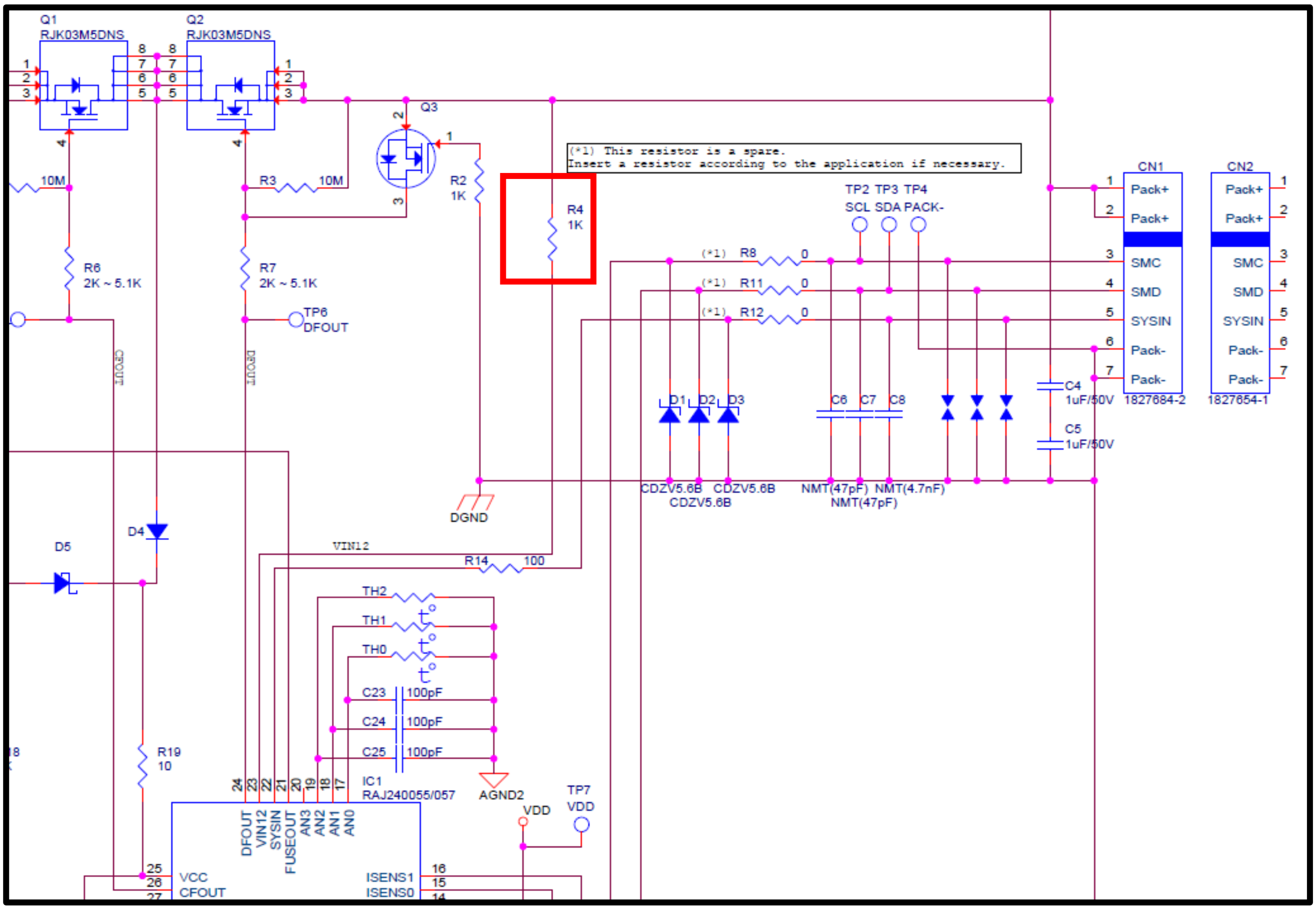
- Place an input filter between FGIC's VIN pins and each of the cells.
- Place resistors valued 100 Ω and capacitors valued 0.1 uF to VIN1 – VIN4 pins for surge protection.

  It is necessary to calculate the cut-off frequency and use correct resistance and capacitance value based on application.



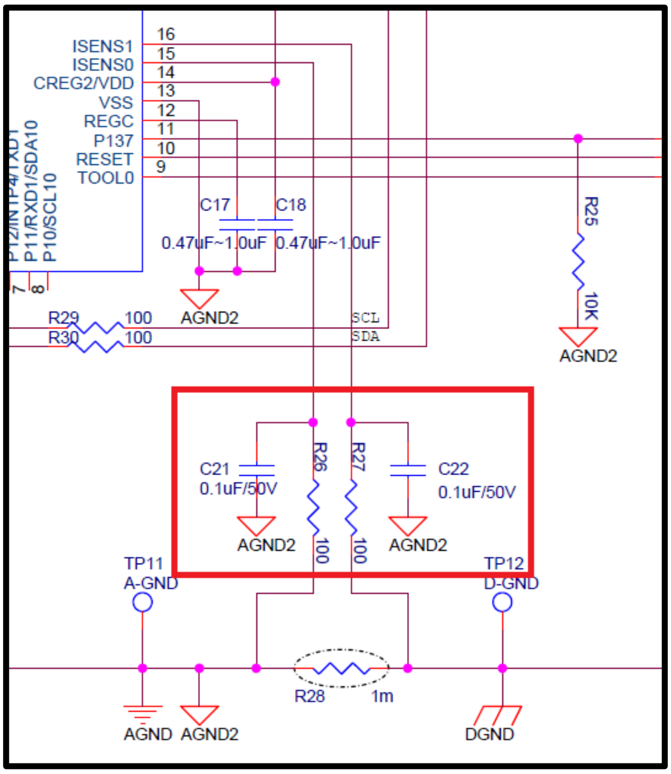
6.3.2 Charger connect detection circuit

- VIN12 pin is source voltage of DFOUT pin (D-FET gate control signal). R4 limits a current when charger is connected reversely. Recommended resistance is 1 kΩ. If it is too large, it will affect D-FET turn off speed.
- Basically, VIN12's capacitor is not mount. It works for stable voltage measurement of VIN12 pin.



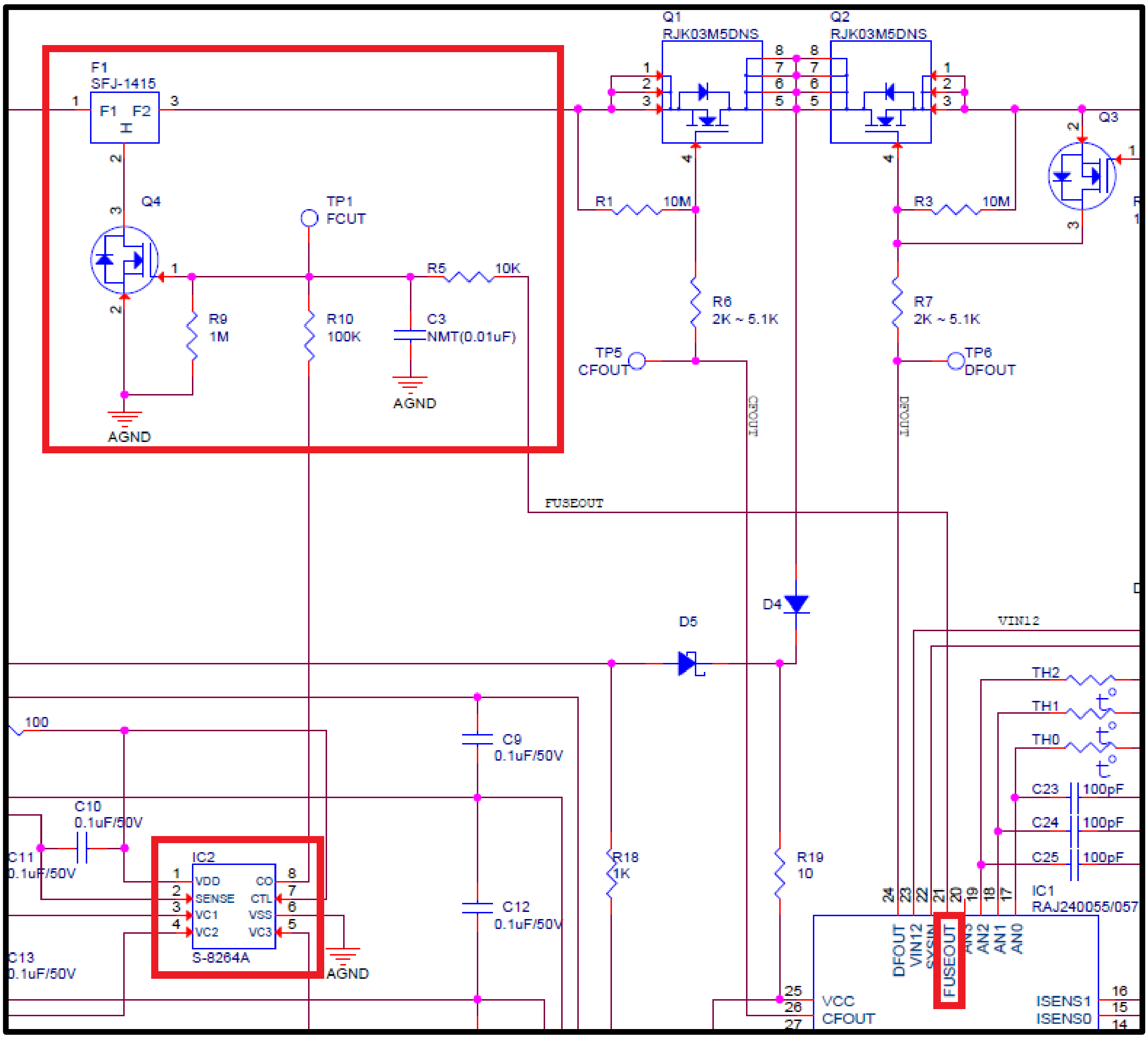
6.3.3 Current monitor

- Potential difference on the sense resistor is monitored by current integrating circuit.
- Place a Low Pass Filter (100 Ω, 0.1 uF) at input stage.
- Sense lines should be shielded if small voltage difference is detected to ensure high accurate current sensing.



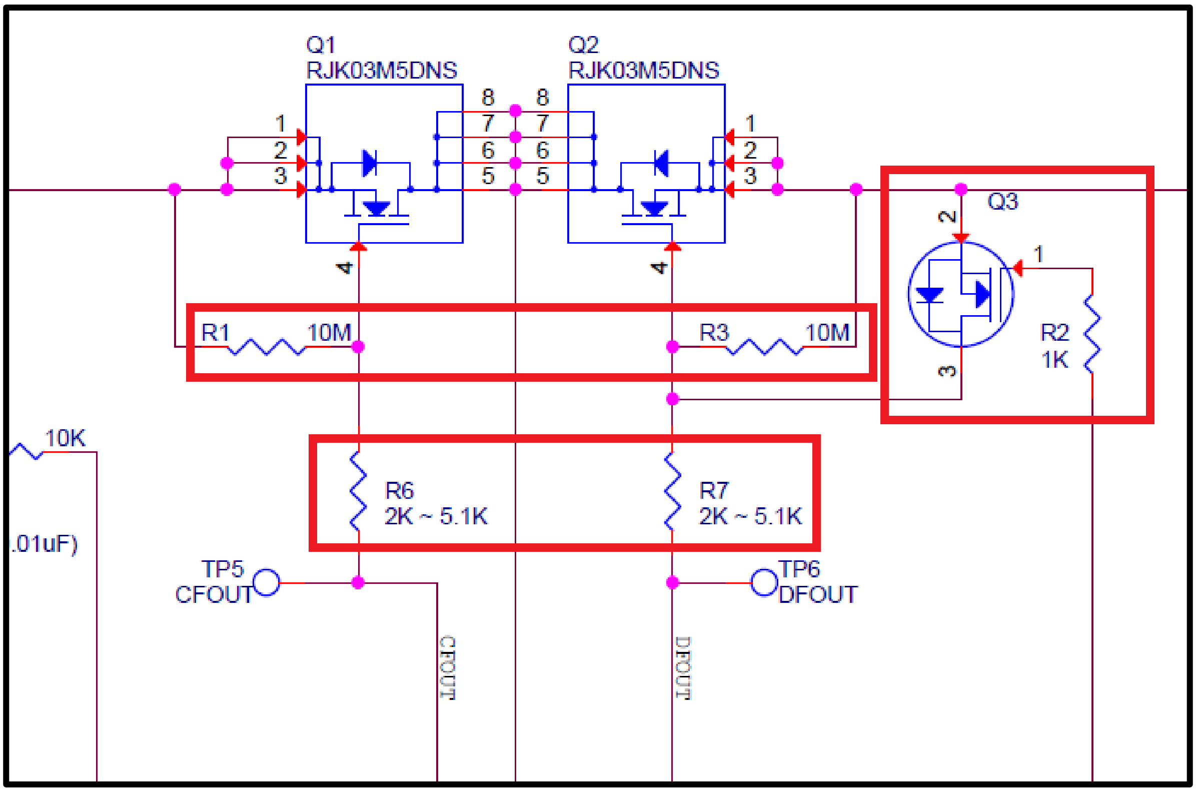
6.3.4 Fuse control

- Self-control protector (SCP) is used for fuse in reference circuit.
- The fuse will blow when RAJ24005X drives FUSEOUT pin high to make Q4 ON.
- The fuse will blow when overcurrent exceeds the limit of SCP.
- The fuse will blow when 2nd protection IC (S-8264A) drives CO pin high to make Q4 ON by detecting overcharge voltage.



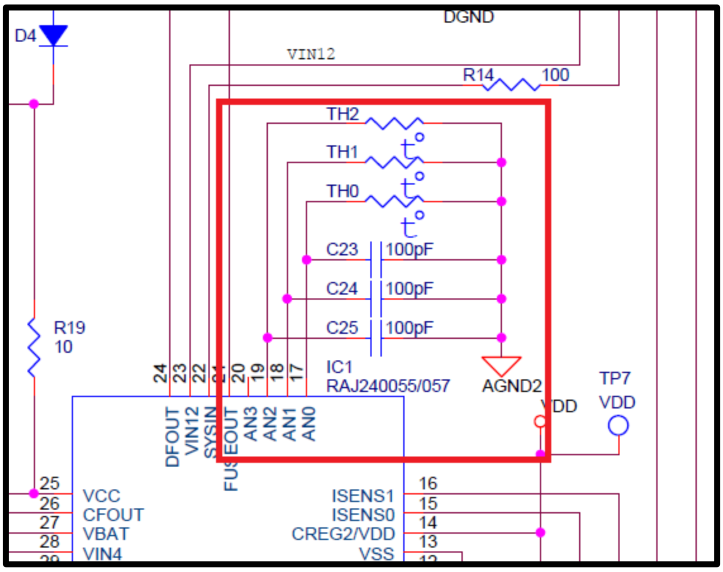
6.3.5 C-FET and D-FET control

- R6 and R7 are placed for gate protection and C-FET/D-FET noise reduction. 2~5.1 kΩ is recommended.
- R1 and R3 are placed to fix C-FET/D-FET gate voltage in order to keep stable off when FET state is off. 10MΩ is recommended to prevent voltage drop.
- Q3 is placed between gate and source of Q2 to turn off D-FET when charger is reversely connected.
- R2 is placed for Q3 gate protection. 1 kΩ is recommended.



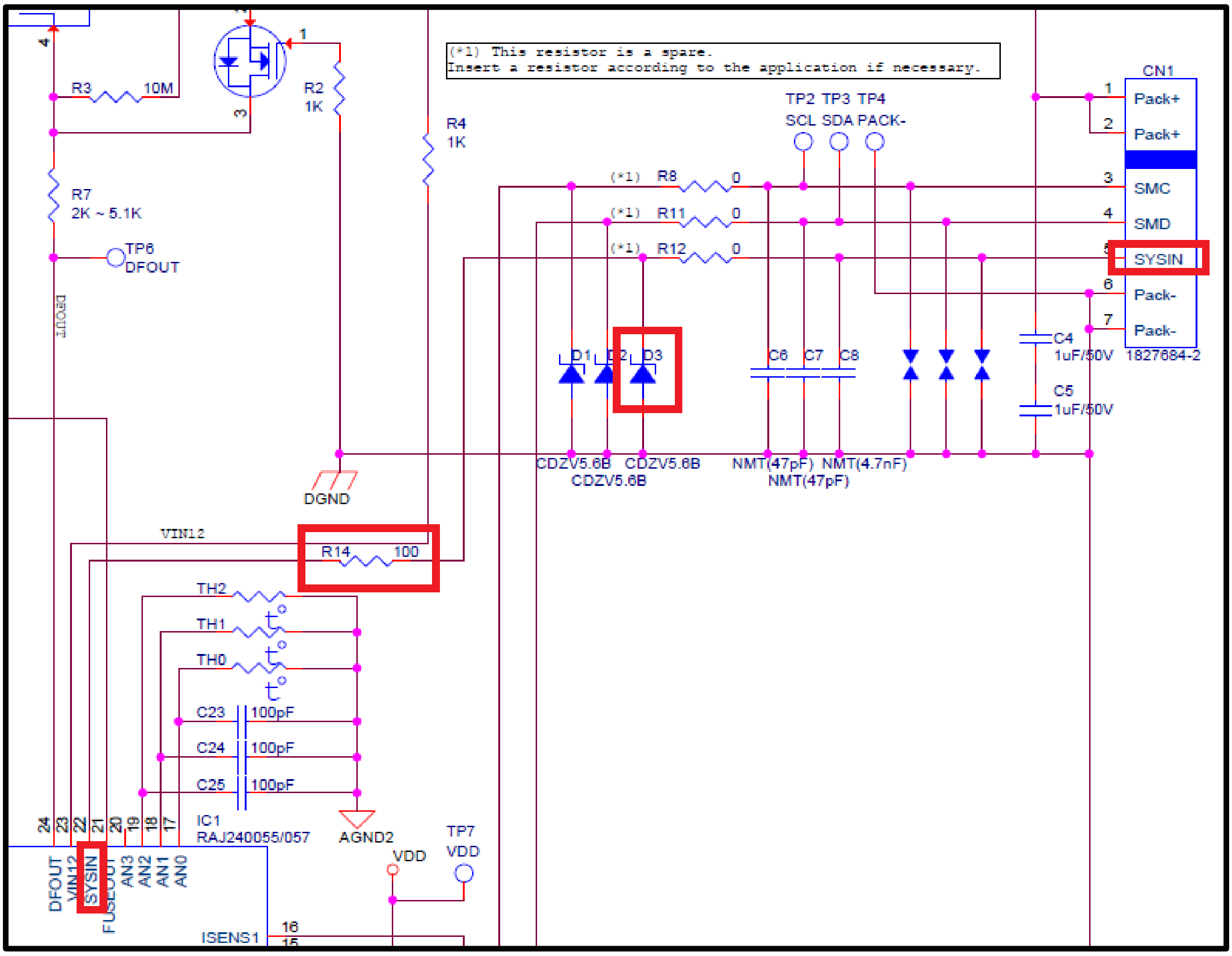
<R> ### 6.3.6 Thermistor

- ADC voltage measurement pins (AN0, AN1, AN2 and AN3) are assigned for thermistor. To prevent EMC noise issue, additional 100pF capacitor is recommended.



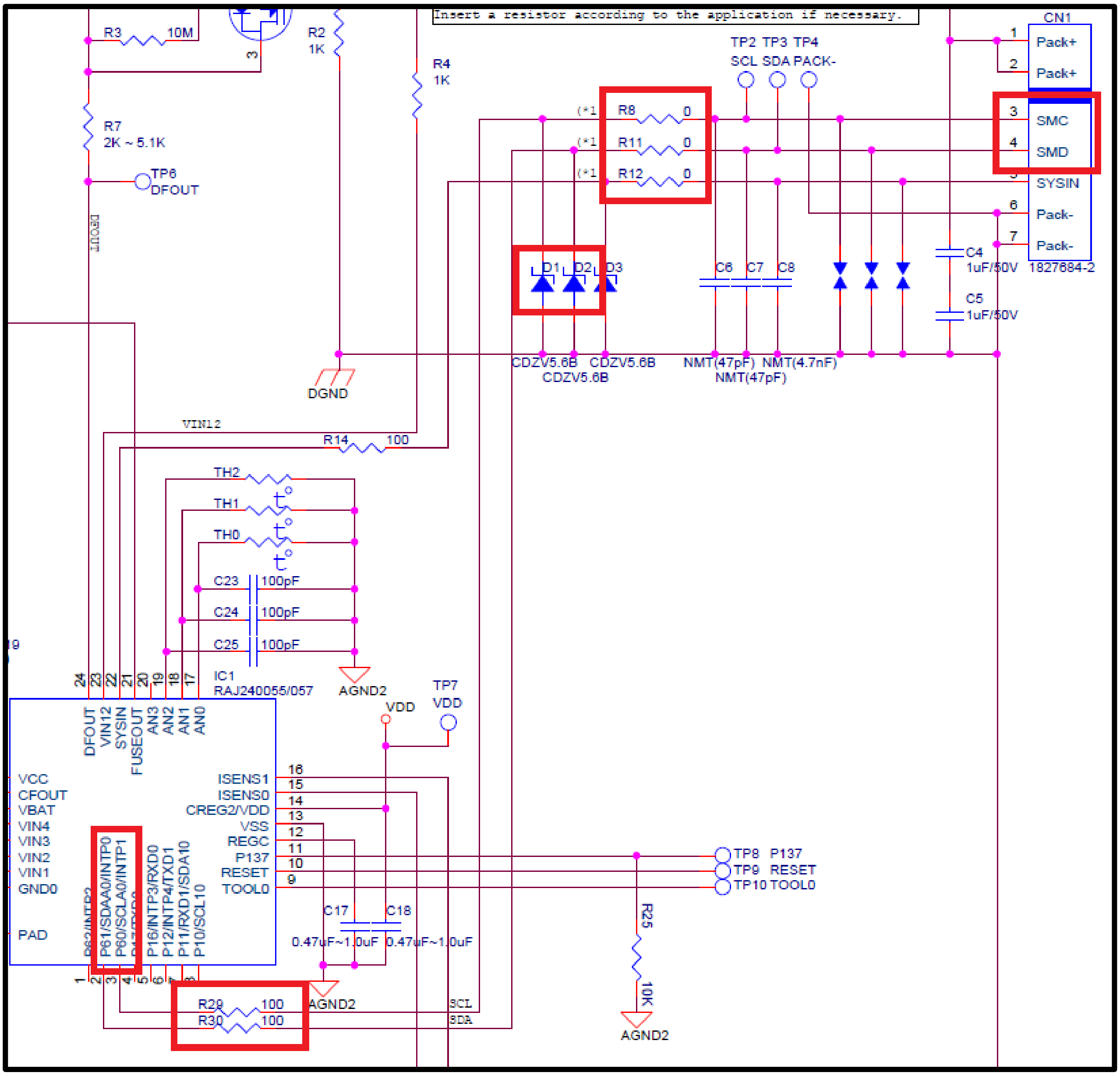
6.3.7 System presence

- Connect R14 (100 Ω) for ESD protection at SYSIN input from SYSIN terminal of connector.
- Zener diode (D3) is for ESD protection. The zener voltage must be less than 30 V, an absolute maximum rating of SYSIN pin.



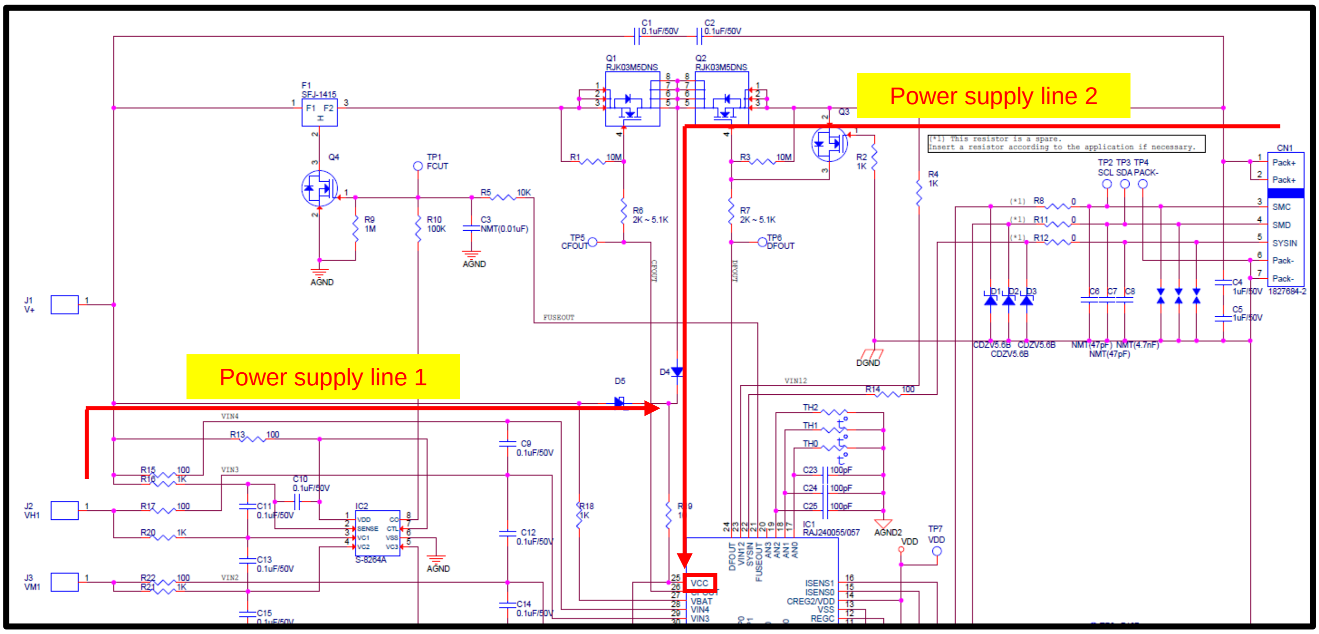
6.3.8 Communication line

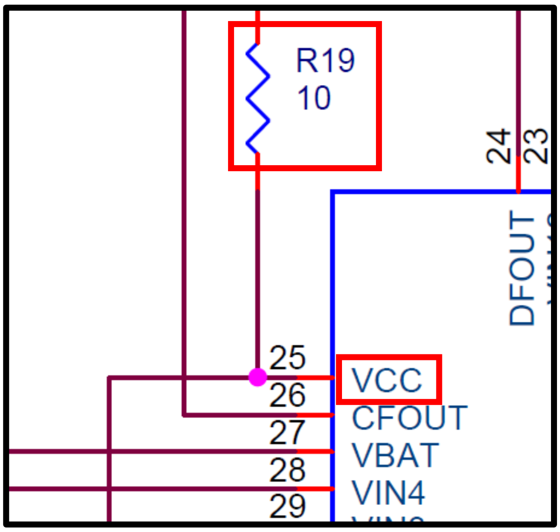
- RAJ24005X supports SMBus communication.
- For electrical over stress countermeasure, input 100 Ω resistor (R29, R30) and Zener diode (D1, D2) are recommended in SMBus communication line. The zener voltage must be less than 6.5V, an absolute maximum rating of SCL and SDA pins.



6.3.9 Power supply path

- Power is supplied to VCC pin through the following two paths depending on circumstance.
- Power is supplied from battery side when Pack+/- is not connected to a charger or the fuse is blown. See power supply line 1.
- Higher output voltage from battery and charger is used as power supply. See power supply line 2.
- R19 is placed for VCC pin protection to limit current. 10 Ω is recommended.





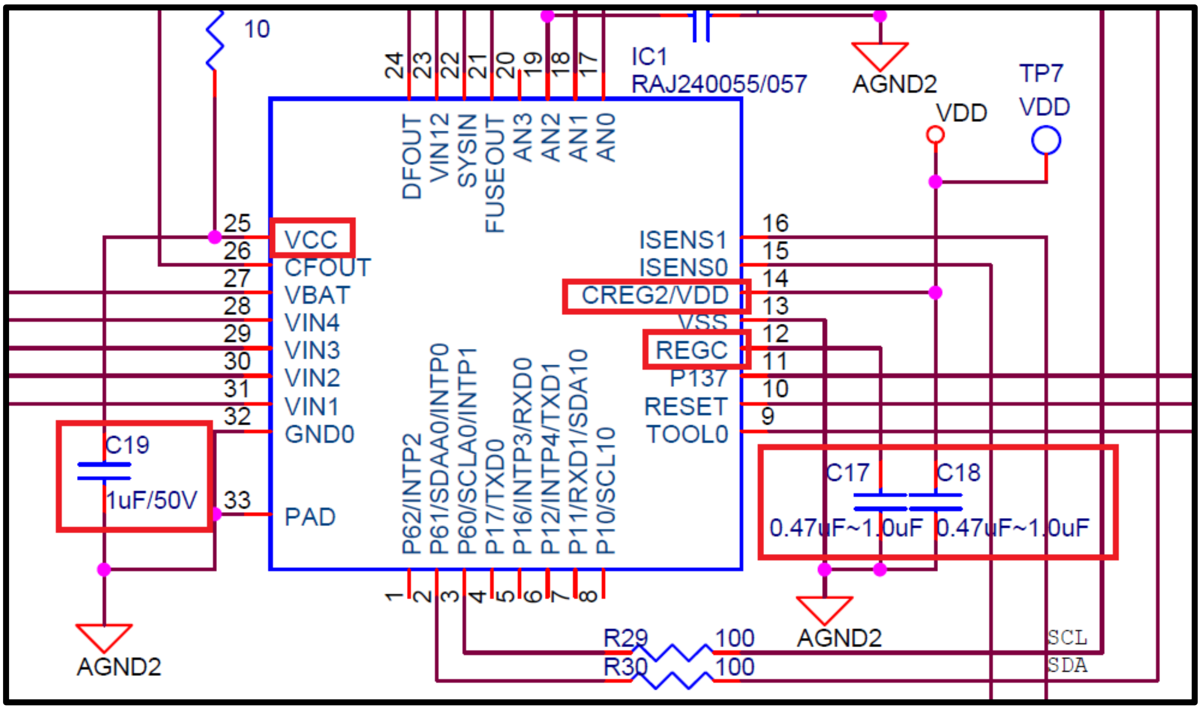
6.3.10 VCC, CREG2, REGC capacitance

- The following decoupling capacitors must be placed adjacent to each pin.

  C19: VCC to AGND2 (1.0 uF is recommended.)

  C18: CREG2 to AGND2 (0.47 to 1.0 uF is recommended.)

  C17: REGC to AGND2 (0.47 to 1.0 uF is recommended.)



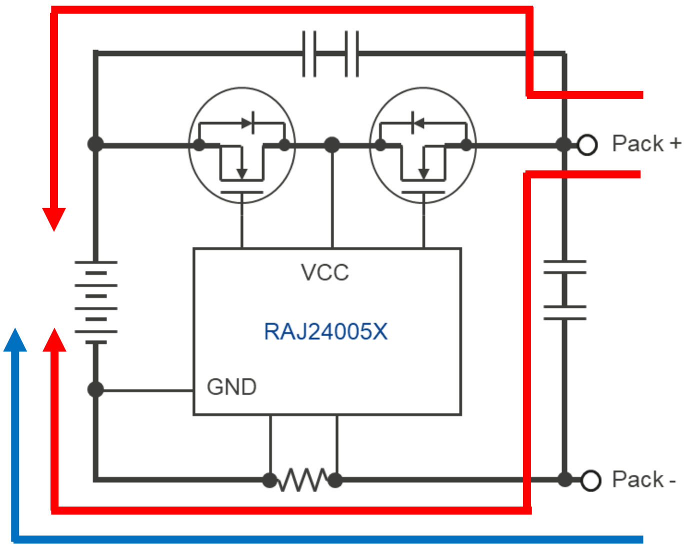
6.4 Layout Guidelines

6.4.1 Summary

- Large current pattern should be wide and short to minimize voltage drop and heat generation.
- Decoupling capacitor must be placed as close as possible to the device VCC and GND pins to prevent erroneous operation due to noise from power supply.
- Capacitors for voltage regulators must be placed close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- To decrease parasitic PCB impedance and improve tolerance against noise, it is preferred to enhance ground pattern as much as possible.
- FGIC (RAJ24005X) must be placed away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.

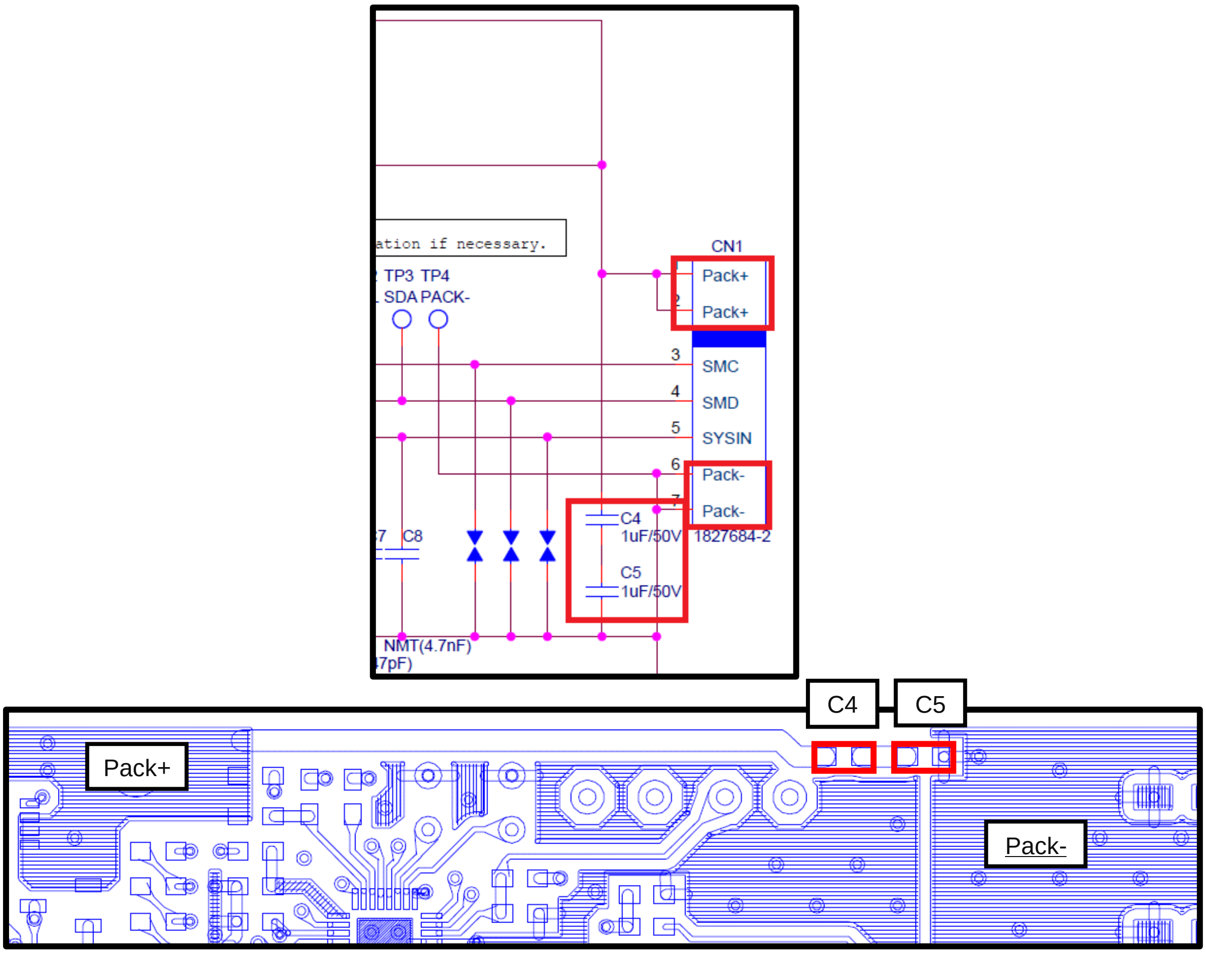
6.4.2 ESD protections on each terminal (basic policy)

- ESD on Pack+ terminal must be discharged to the top side of the cell or to Pack- terminal through a capacitor.
- ESD on Pack- terminal must be discharged to the GND side of the cell.
- ESD on communication terminals and other GPIOs must be discharged to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- terminal must be discharged to the battery cells so that it will not interfere with FGIC functions and measurements.
- Sufficient current capacity in the power line is required to effectively discharge ESD noise.
  Power line: Pack+ terminal to the top side of the cell, Pack- terminal to the GND side of the cell, etc.



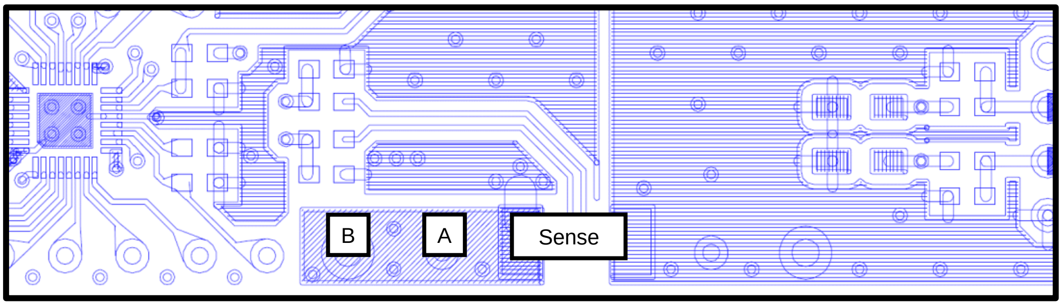
6.4.3 Pack+, Pack- (Noise protection element)

- Bypass capacitors must be placed across Pack+ and Pack- terminals. (Countermeasure against ESD)
- Bypass capacitors must be placed adjacent to Pack+ and Pack- terminals. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don’t use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)



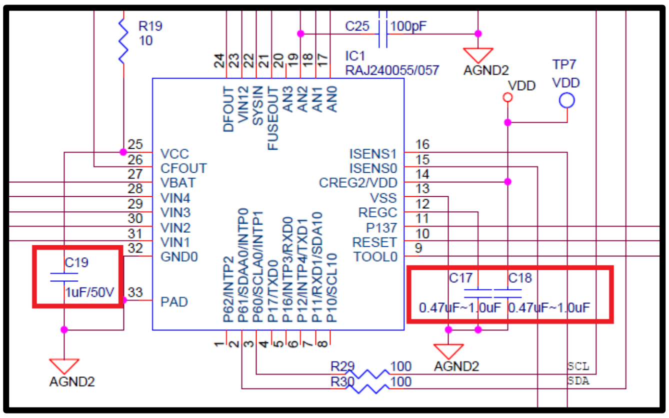
6.4.4 GND connection

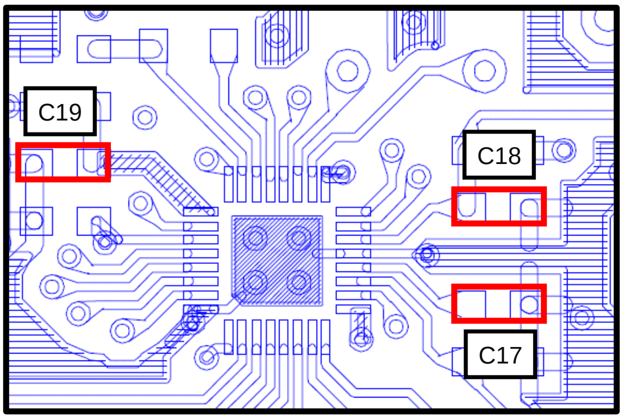
- Each analog GND of FGIC should be connected to the point (B) of the cell- side by the pattern with an adequate width. (Prevent potential variation by large current.)
- Minimize parasitic impedance between point (A) and (B).
- The pattern from GND0 and VSS pins to AGND and AGND2 should not be diverged on the way, nor be connected to the other GND. (Keeping the GND potential of MCU and AFE equal)



6.4.5 Bypass capacitor between VCC/CREG2/REGC and GND0/VSS

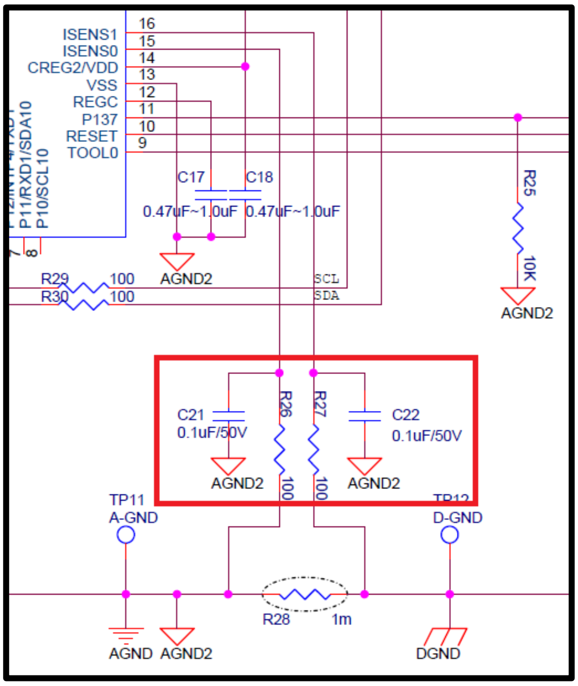
- The patterns between VCC pin and GND0 pin, and between CREG2/REGC pin and VSS pin, a bypass capacitor is connected and the path must be as short as possible. (Countermeasure for ESD, EMC noise and etc.)
  The FGIC and bypass capacitors must be placed on the same side of the PCB without through-holes.
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)



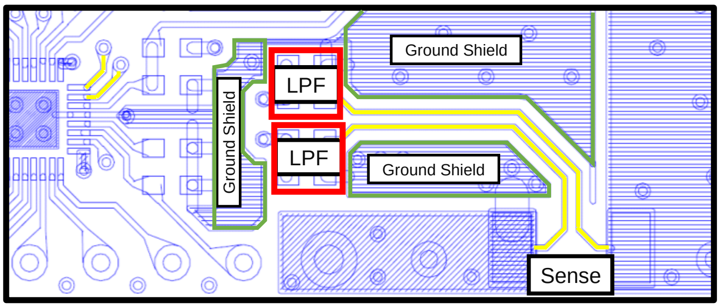


6.4.6 Current Monitor (ISENS0, ISENS1)

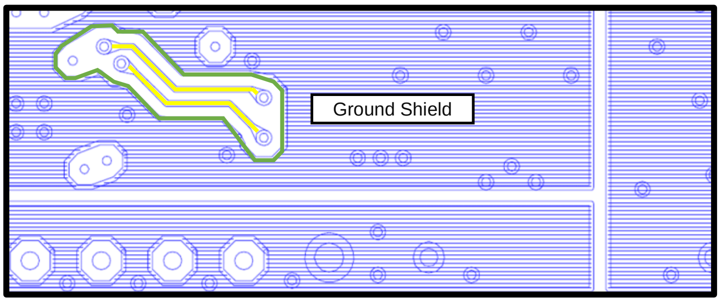
- Two lines from current sense resistor to ISENS0, ISENS1 pins must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise).
- Both sides of the 2 lines from the sense resistor should be protected by the shield pattern which is connected with GND. (Prevention of erroneous detections due to noise)
- Minimizing wire length and its number of branches between current sense resistors and ISENS0/ISENS1 pins to suppress incoming noise from unnecessary pattern.
- LPF (100 Ω and 0.1 uF) to suppress noise should be placed as close as possible to the ISENS0/ISENS1 pins.



L1 Pattern (Top layer)

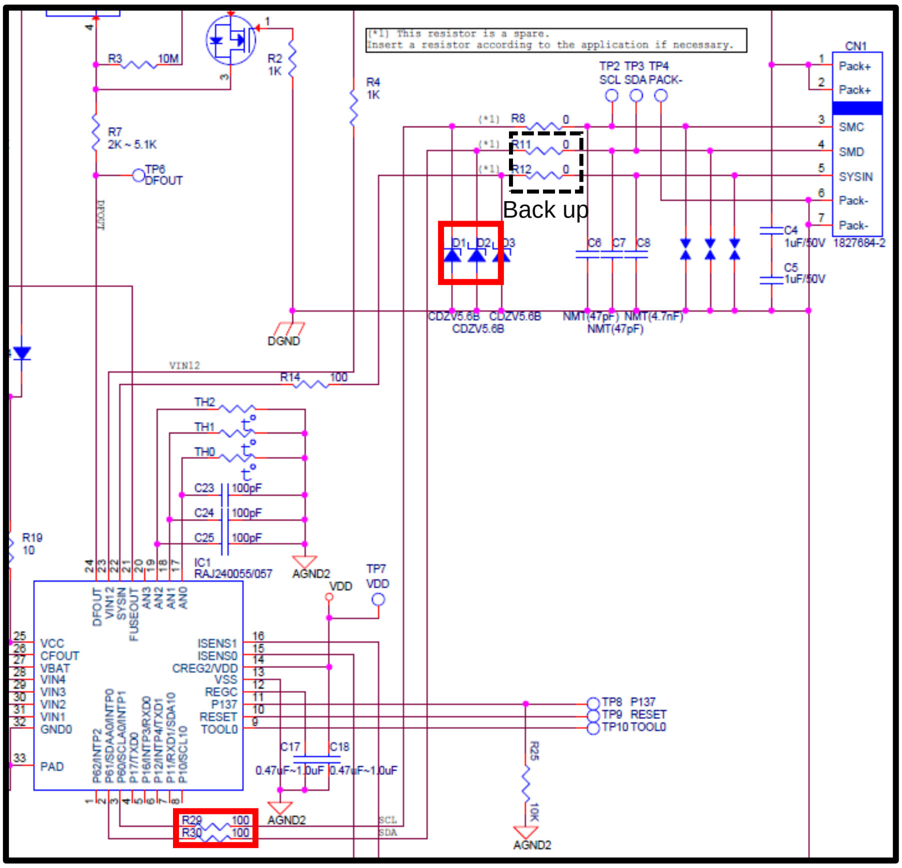


L3 Pattern (Inner layer)



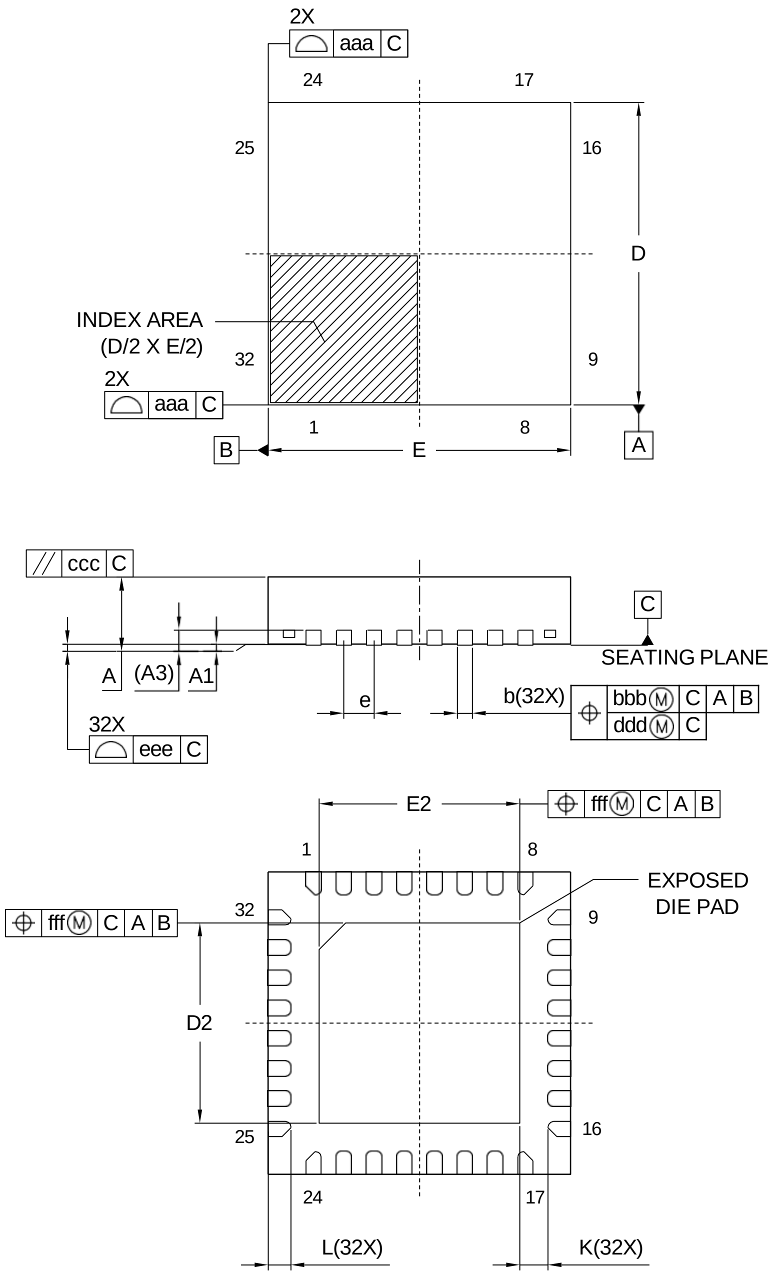
6.4.7 Communication line (SMBus)

- Zener diodes must be placed to SMBus lines. And it is necessary to place resistors on the side of FGIC. (Zener diode and the resistor are for surge countermeasures and noise countermeasure.)
- The resistor on the side of the FGIC must be placed as close to the FGIC as possible.



CHAPTER 7. PACKAGE OUTLINE

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HVQFN032-4x4-0.40	PVQN0032LE-A	0.04



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.90
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
L	0.20	0.30	0.40
K	0.20	—	—
D_2	2.60	2.65	2.70
E_2	2.60	2.65	2.70
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

REVISION HISTORY

Rev.	Date	Page	Description
1.00	Dec. 29, 2022		First release
1.01	Mar. 13, 2024	P20	4.1 Absolute Maximum Ratings Updated the Note for FUSEOUT of Output voltage
		P56	6.2 Typical Application Circuit Updated the figure
		P61	6.3.6 Thermistor Updated the figure and description (recommend adding a capacitor to ANx pins)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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