RAJ240080
2 to 5 Series Li-ion Battery Manager

R01DS0299EJ0100
Rev.1.00
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# 1. Introduction

## 1.1 Features

- **Fully integrated battery management solution with battery capacity measurement and programmable protection capability.**
- **Supports up to 5 Li-ion or Li-Polymer battery cells in series.**
- **Integrated with Renesas Ultra Low Power RL78 CPU core for multi-function process**
- **Memory**
  Code flash memory: 64KB
  Data flash memory (up to 100,000 erase/write cycles): 4 KB
  SRAM: 5.5KB
- **Clock generator**
  High speed on-chip oscillator: up to 32 MHz
  Low speed on-chip oscillator: 32 KHz
  AFE on-chip oscillator: 4.194MHz
- **General Purpose I/O Ports**
  Total: 22 pins
  CMOS input/output: 16
  CMOS input: 2
  High voltage input [VCC tolerance]: 1
  High voltage input/output [VCC tolerance]: 1
- **Serial interface**
  CSI (SPI): 1 channel
  I2C: 1 channel
  UART: 2 channels
  Simplified I2C: 1 channel
- **Timer**
  MCU 16-bit timer: 5 channels
  MCU 12-bit interval timer: 1 channel
  AFE timer: 2 channels
    - AFE timer A: setting range: 125 ms to 64 s
    - AFE timer B: setting range：30.52 us to 125 ms
- **Embedded A/D converter**
  AFE 15-bit resolution sigma-delta A/D converter
- **Current integration circuit**
  18-bit resolution sigma-delta A/D converter
- **Impedance measurement circuit**
  Simultaneous measurement of battery voltage and current
- **Over current detection circuit**
  Short circuit current detection
  Charge overcurrent detection
  Discharge overcurrent detection
  Charge wakeup current detection
  Discharge wakeup current detection
- **Series regulator**
  3.3V CREG2
  1.8V CREG1
- **Charge and Discharge MOSFET control**
  High side Nch MOSFET drive circuit embedded
  Programmable MOSFET control by 8-bit PWM
- **Fuse control**
  FUSEOUT pin can support fuse blow function.
- **Intel® Dynamic Battery Power Technology support**
- **Voltage and temperature condition**
  Power supply voltage: VCC = 4.0 to 28 V
  Operating ambient temperature: Ta = -20 to +85°C
- **Package Information**
  48 pin plastic mold QFP
  ([Body] 9.0 mm x 9.0 mm, 0.5 mm pitch)

## 1.2 Applications

- E-Bike, E-Scooter, Pedal-Assist Bicycle
- Power Tool, Vacuum Cleaner, Drone
- Battery Backup System, Energy Storage System (ESS)

## 1.3 Description

RAJ240080 is Renesas Li-ion battery fuel gauge IC (FGIC) which consists of a MCU device and an AFE device in a single package. Pack with a variety of battery management features and Renesas RL78 CPU core which has multiple low power modes and capable of achieving high performance in ultra-low power operation. RAJ240080 fuel gauge IC has control firmware stored in embedded flash memory to control attached embedded analog and digital circuits to execute battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

# Table of Contents

# 2. OUTLINE

## 2.1 Outline of Functions

**Caution** **This outline describes the functions at the time when Peripheral I/O redirection register 0 (PIOR0) is set to “00H”.**

(1/2)

| Item | | Description |
|---|---|---|
| Code flash memory | | 64 KB |
| Data Flash memory | | 4 KB |
| RAM | | 5.5 KB |
| Address size | | 1MB |
| Main system clock | High speed on-chip Oscillator clock(fIH) | HS (high-speed main) mode: 1 to 32 MHz<br>LS (low-speed main) mode: 1 to 8 MHz , |
| Low speed on-chip oscillator clock | | 15 kHz (TYP.) |
| General purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) |
| Minimum instruction execution time | | 0.03125 us(Internal high speed oscillation clock: fIH = 32 MHz) |
| Instruction set | | • Data transmission (8/16 bits)<br>• Addition and subtraction/logical operations (8/16 bits)<br>• Multiplication (8×8 bits,16×16 bits),Division (16÷16 bits,32÷32 bits)<br>• Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc. |
| I/O Port | CMOS I/O | 16 |
| | CMOS input | 2 |
| | N-ch open-drain I/O [6V tolerance) | 2 |
| | High voltage I/O | 2 |
| Timer | 16-bit timer | 6 channels<br>(TAU : 4 channels, Timer RD : 2 channels) |
| | Watchdog timer | 1 channel |
| | 12-bit interval timer | 1 channel |
| Serial interface | | CSI: 1 channel / UART: 2 channels / simplified I2C: 1 channel |
| | I$^2$C bus | 1 channel |
| Vector interrupt source | Internal | 10 |
| | External | 9 (6 sources is connected to AFE in the chip) |
| Reset | | ・Reset by RESET pin (reset circuit output of AFE connected to RESETOUT)<br>・Internal reset by watchdog timer<br>・Internal reset by illegal instruction execution Note<br>・internal reset by RAM parity error<br>・internal reset by illegal memory access |
| On-chip debug function | | Support |

**Note** The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

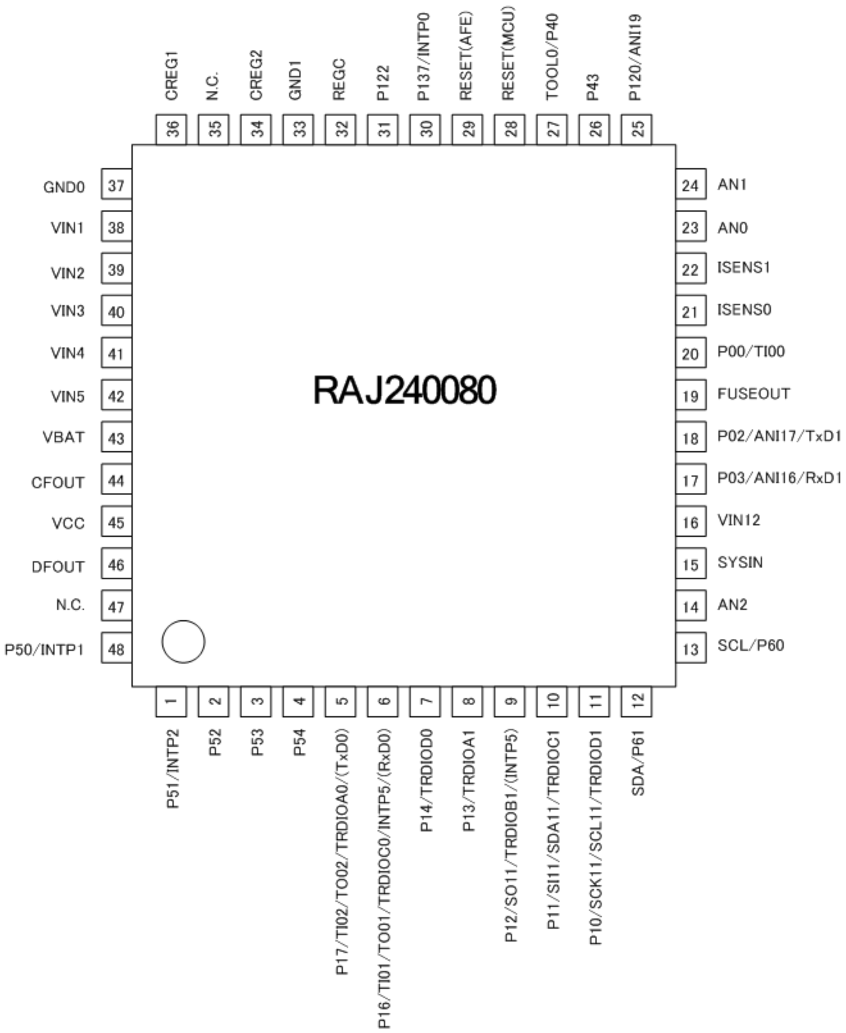
| Item | Description |
|---|---|
| PWM | 8 bits ×1 for FET control |
| Sigma-delta A/D converter | 15-bit resolution (sigma-delta method)<br>• Each battery Cell voltage<br>• Battery Cell total voltage<br>• VIN12 pin input voltage<br>• Thermistor sensor port with on-chip pull-up 10kohm resistor: 3 channels<br>• On-chip simple temperature sensor (temperature range: -20 to 85C) |
| Current integrating circuit | 1 channel:18-bit resolution |
| Current integrating circuit for impedance measurement | 1 channel:11-bit resolution |
| Overcurrent detection circuit and wake up current detection circuit | • Discharge short-circuit current detection<br>• Discharge overcurrent detection<br>• Charge overcurrent detection,<br>• Wake up current detection (discharge and charge)<br>• Intel® Dynamic Battery Power Technology current detection |
| Simple temperature sensor | 1 channel |
| Charge/Discharge FET control circuit | NchFET driver for charge control<br>NchFET driver for discharge control |
| Power on reset circuit | Return from power down mode by detecting voltage and connecting charger |
| Series regulator Note1 | CREG2: Power supply for MCU (3.3 V)<br>CREG1: Reference voltage for AFE A/D converter and current integration circuit (1.8V) |
| Reset circuit | Series regulator output monitoring (CREG2) |
| Cell balancing circuit | 5 series cells support (On-resistor: 500ohm TYP) |
| MCU runaway detection circuit | 20 bits×1(2 / 4 / 8 [s] to be selected) |
| AFE On-chip oscillator Note2 | 4.194 MHz (TYP) |
| AFE timer | 2 channels<br>• AFE timer A (setting range：125 ms to 64 s)<br>• AFE timer B (setting range：30.52 us to 125 ms) |
| MCU-AFE communication interface(C2C) | AFE ~ MCU communication (Chip to Chip Interface) |
| Power supply voltage | VCC = 4.0 to 28 V |
| Operation ambient temperature | -20 to 85C |
| Package | 48 pin plastic mold QFP([Body] 9.0mm x 9.0mm , 0.5 mm pitch, 1.4 mm thickness) |

**Note 1.** Series regulator stabilization time is 10ms after AFE power on.

**Note 2.** 2ms wait is need for stabilization after On-chip oscillator is started.

## 2.2 Pin Configuration

・48 pin plastic mold QFP ([Body] 9.0mm x 9.0mm , 0.5 mm pitch)



**Caution 1.** **REGC pin connects to GND1 pin through a capacitor (0.47 to 1 uF)**

**Caution 2.** **CREG1 pin connects to GND0 pin through a capacitor (1 uF).**

**Caution 3.** **CREG2 pin connects to GND1 pin through a capacitor (2.2 uF).**

**Remark 1.** Pin name refer to [3.1 Pin identification].

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

# 3. PIN FUNCTIONS

## 3.1 Pin identification

(1/2)

| No. | Name | Type | Description |
|---|---|---|---|
| 1 | P51/INTP2 | DIO(8-R) | Port 51 Leave open in output mode if not used. |
| 2 | P52 | DIO(8-R) | Port 52 Leave open in output mode if not used. |
| 3 | P53 | DIO(5-AN) | Port 53 Leave open in output mode if not used. |
| 4 | P54 | DIO(5-AN) | Port 54 Leave open in output mode if not used. |
| 5 | P17/TI02/TO02/TRDIOA0/(TxD0) | DIO(5-BC) | Port 17 Leave open in output mode if not used. |
| 6 | P16/TI01/TO01/TRDIOC0/INTP5/(RxD0) | DIO(5-BC) | Port 16 Leave open in output mode if not used. |
| 7 | P14/TRDIOD0 | DIO(5-AN) | Port 14 Leave open in output mode if not used. |
| 8 | P13/TRDIOA1 | DIO(5-BB) | Port 13 Leave open in output mode if not used. |
| 9 | P12/SO11/TRDIOB1/(INTP5) | DIO(5-BB) | Port 12 Leave open in output mode if not used. |
| 10 | P11/SI11/SDA11/TRDIOC1 | DIO(8-R) | Port 11 Leave open in output mode if not used. |
| 11 | P10/SCK11/SCL11/TRDIOD1 | DIO(5-AN) | Port 10 Leave open in output mode if not used. |
| 12 | SDA/P61 | DIO(13-R) | I2C Bus data I/O Input/Output |
| 13 | SCL/P60 | DIO(13-R) | I2C Bus data I/O Input/Output |
| 14 | AN2 | AIN | Analog Input |
| 15 | SYSIN | HVIN | System detection pin |
| 16 | VIN12 | AIN | Charger connection monitoring |
| 17 | P03/ANI16/RxD1 | DIO(11-V) | Port 03 Leave open in output mode if not used. |
| 18 | P02/ANI17/TxD1 | DIO(11-U) | Port 02 Leave open in output mode if not used. |
| 19 | FUSEOUT | HVIO | Fuse FET control |
| 20 | P00/TI00 | DIO(8-R) | Port 00 Leave open in output mode if not used. |
| 21 | ISENS0 | AIN | Analog input for current integration circuit |
| 22 | ISENS1 | AIN | Analog input for current integration circuit |
| 23 | AN0 | AIN | Analog Input |
| 24 | AN1 | AIN | Analog Input |
| 25 | P120/ANI19 | DIO(11-U) | Port 120 Leave open in output mode if not used. |
| 26 | P43 | DIO(5-AN) | Port 43 Leave open in output mode if not used. |
| 27 | TOOL0/P40 | DIO(8-R) | Data Input/Output for tools |
| 28 | RESET(MCU) | DIN (2) | Reset Input |
| 29 | RESET(AFE) | OUT | Reset Output |
| 30 | P137/INTP0 | DIN (2) | Port 137 Connect to GND1 through a resistor if not used. |
| 31 | P122 | DIN (37-C) | Port 122 Connect to GND1 through a resistor if not used. |
| 32 | REGC | P | Regulator capacitor connection |
| 33 | GND1 | P | Ground |
| 34 | CREG2 | P | Regulator capacitor connection |
| 35 | NC | NC | No connect |
| 36 | CREG1 | P | Regulator capacitor connection |

(2/2)

| No. | Name | Type | Description |
|---|---|---|---|
| 37 | GND0 | P | Ground |
| 38 | VIN1 | AIN | Battery voltage input |
| 39 | VIN2 | AIN | Battery voltage input |
| 40 | VIN3 | AIN | Battery voltage input |
| 41 | VIN4 | AIN | Battery voltage input |
| 42 | VIN5 | AIN | Battery voltage input |
| 43 | VBAT | AIN | Battery voltage input |
| 44 | CFOUT | HVO | Charge FET control |
| 45 | VCC | P | Power supply |
| 46 | DFOUT | HVO | Discharge FET control |
| 47 | NC | NC | No connect |
| 48 | P50/INTP1 | DIO(5-AN) | Port 50 Connect to GND1 through a resistor |

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

**HVO: high voltage output**
**HVIN: high voltage input**
**HVIO: high voltage input/output**
**P: power**

**DIO: digital I/O**
**DIN: digital input**
**AIN: analog input**

## 3.2 Pin Functions

(1/2)

| Category | Pin name | I/O | Function |
|---|---|---|---|
| Power supply | VCC | − | Power supply input<br>Apply power supply voltage to VCC pin from a charger or battery. |
| | GND0, GND1 | − | Device ground input. Connect the negative input terminal of lithium-ion battery 1 to the GND0 and GND1 pins |
| | CREG1 | − | 1.8V series regulator for AFE A/D converter<br>Connect this pin to VSS via a capacitor (1.0 uF). |
| | CREG2 | − | 3.3V series regulator and power supply for MCU<br>Connect this pin to VSS via a capacitor (2.2 uF). |
| | REGC Note 1. | − | Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to VSS via a capacitor (0.47 to 1 uF).<br>Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage. |
| RESET | RESET(MCU) | Input | This is the active-low system reset input pin for MCU. |
| | RESET(AFE) | output | This is the active-low system reset output pin for AFE. |
| TOOL0 | TOOL0 **Note 3** | input | Data I/O for flash memory programmer/debugger.<br>Connect to the CREG2 via an external pull-up resistor in the on chip debug mode |
| Serial interface (UART0, UART1) | RxD0, RxD1 | input | Serial data input pins of serial interface UART0 to UART1 |
| | TxD0, TxD1 | output | Serial data output pins of serial interface UART0 to UART1 |
| Serial interface (CSI11) | SCK11 | I/O | Serial clock I/O pin of serial interface CSI11 |
| | SI11 | input | Serial data input pin of serial interface CSI11 |
| | SO11 | output | Serial data output pin of serial interface CSI11 |
| Serial interface (IIC11) | SCL11 | output | Serial clock output pin of serial interface IIC11 |
| | SDA11 | I/O | Serial data I/O pin of serial interface IIC11 |
| Serial interface (IICA0) | SCL | I/O | Serial clock I/O pins of serial interface IICA0 |
| | SDA | I/O | Serial data I/O pins of serial interface IICA0, |
| A/D converter | AN0, AN1, AN2 | input | AFE A/D converter analog input |
| | ANI16, ANI17, ANI19 | input | MCU A/D converter analog input |
| Current integration circuit and overcurrent detection circuit | ISENS0、ISENS1 | input | Analog input for current integration circuit and over current detection circuit |
| Timer | TI01, TI02 | input | The pins for inputting an external count clock/capture trigger to 16-bit timers 01 and 02 |
| | TO01, TO02 | output | Timer output pins of 16-bit timers 01 and 02 |
| | TRDIOA0,<br>TRDIOA1,<br>TRDIOB1,<br>TRDIOC0,<br>TRDIOC1,<br>TRDIOD0,<br>TRDIOD1 | I/O | Timer RD input/output |

**Note 1.** CREG1 is not external power supply pin. (Do not draw current from CREG1.)

**Note 2.** REGC is not external power supply pin. (Do not draw current from REGC.)

**Note 3.** After reset release, the connection between P40/TOOL0 and the operating mode are as follows.

**Table 3-1 TOOL0 Pin Operation Mode after Reset Release**

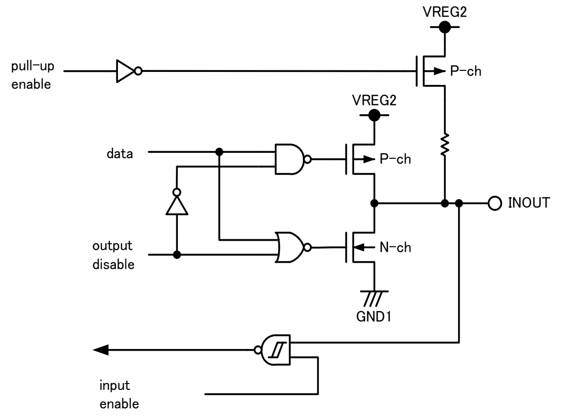
| P40/TOOL0 | Operation Mode |
|---|---|
| CREG2 | Normal operation mode |
| 0V | Flash memory programming mode |

(2/2)

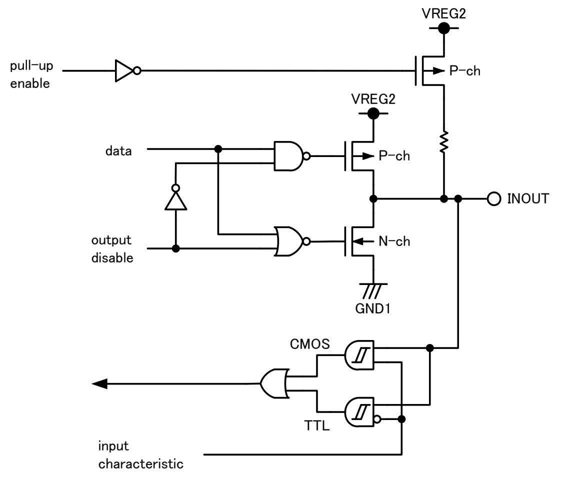
| Category | Pin name | I/O | Function |
|---|---|---|---|
| External interrupt input | INTP0 to INTP2, INTP5 | input | Interrupt request input pin. |
| Charger connection detect | VIN12 | Input | Charger voltage input and source voltage of discharge FET drive port (DFOUT) |
| Battery connection detect | VBAT | input | Sense voltage input pin for most positive cell and source voltage for charge FET drive port (CFOUT) |
| Battery voltage detection circuit | VIN5 | input | The positive input terminal of lithium-ion battery 5. |
| | VIN4 | Input | The negative input terminal of lithium-ion battery 5 and the positive input terminal of lithium-ion battery 4 |
| | VIN3 | Input | The negative input terminal of lithium-ion battery 4 and the positive input terminal of lithium-ion battery 3 |
| | VIN2 | Input | The negative input terminal of lithium-ion battery 3 and the positive input terminal of lithium-ion battery 2 |
| | VIN1 | Input | The negative input terminal of lithium-ion battery 2 and the positive input terminal of lithium-ion battery 1 |
| FET control output | DFOUT | Output | ON/OFF signal output pin for discharge FET. |
| | CFOUT | Output | ON/OFF signal output pin for charge FET. |

## 3.3 Pin Block Diagram

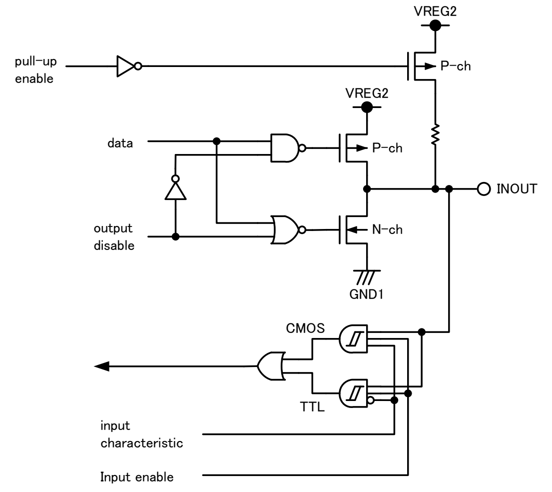
**DIO (Type 5-BB)**



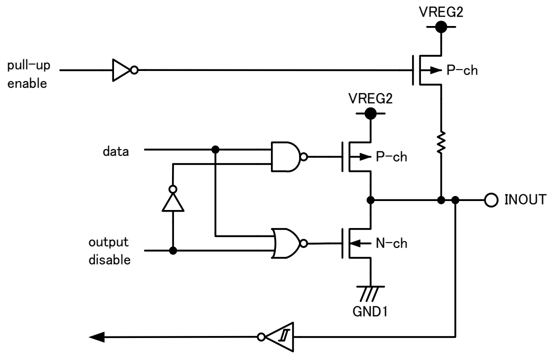
**DIO (Type 5-AN)**



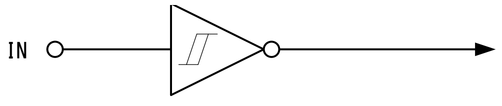
**DIO (Type 5-BC)**



**DIO (Type 8-R)**

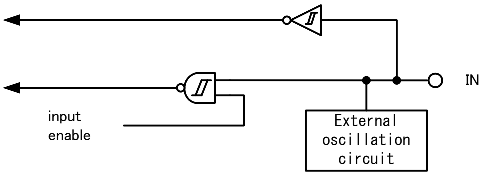


**DIN (Type 2)**



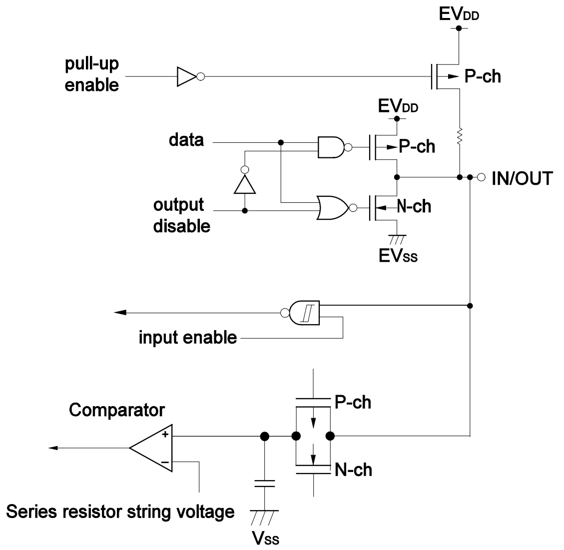
Schmitt-triggered input with histeresis characteristics

**DIN (Type 37-C)**

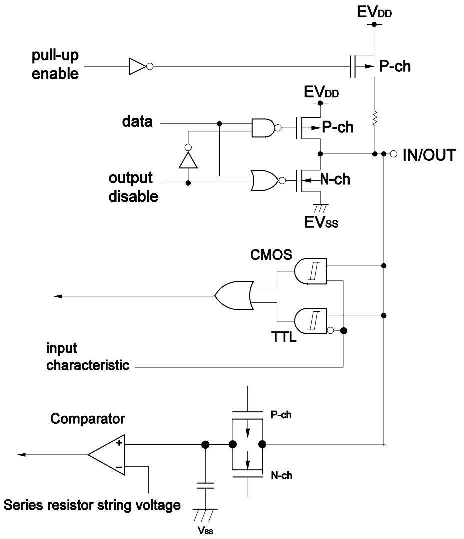


External oscillation circuit:can not be used with this product.

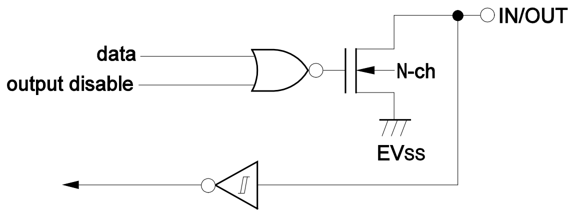
**DIO (11-U)**



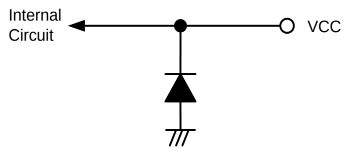
**DIO (11-V)**



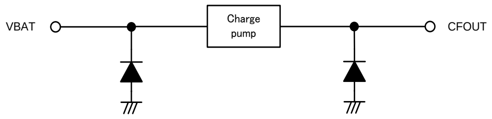
**DIO (13-R)**



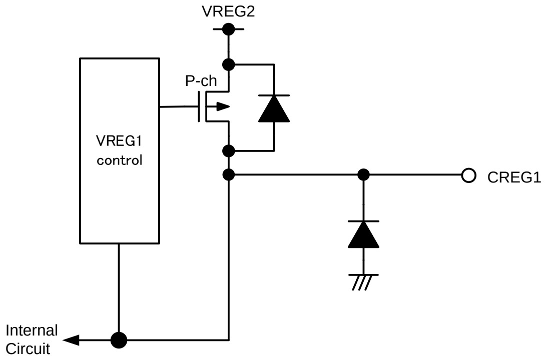
**VCC**



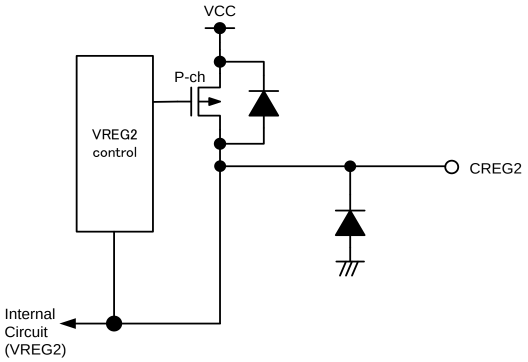
**VBAT, CFOUT**



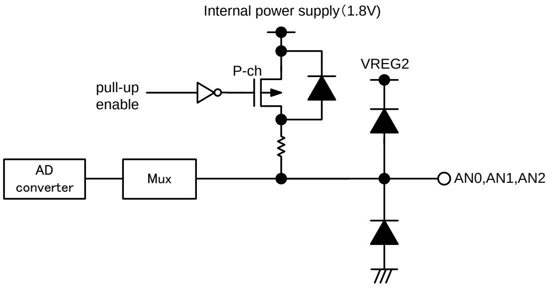
**CREG1**



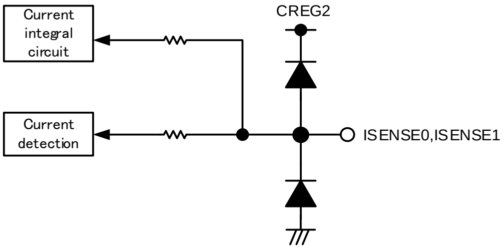
**CREG2**



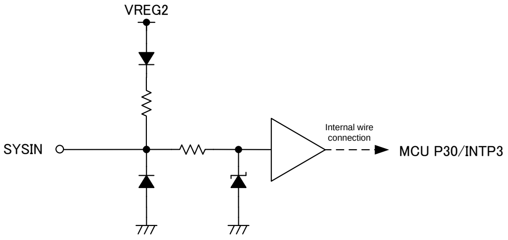
**AN0 / AN1 / AN2**



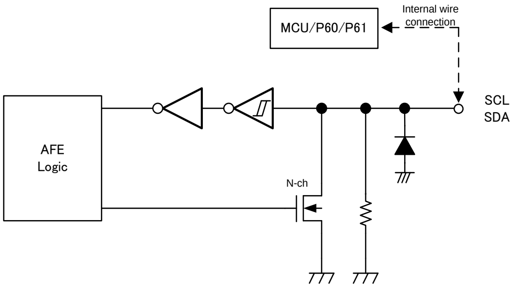
**ISENS0 / ISENS1**



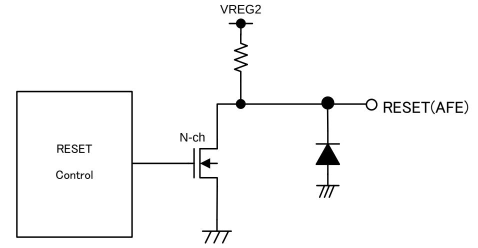
**SYSIN**



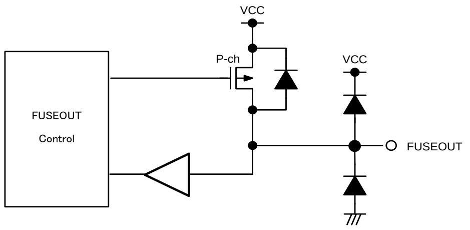
**SCL / SDA**



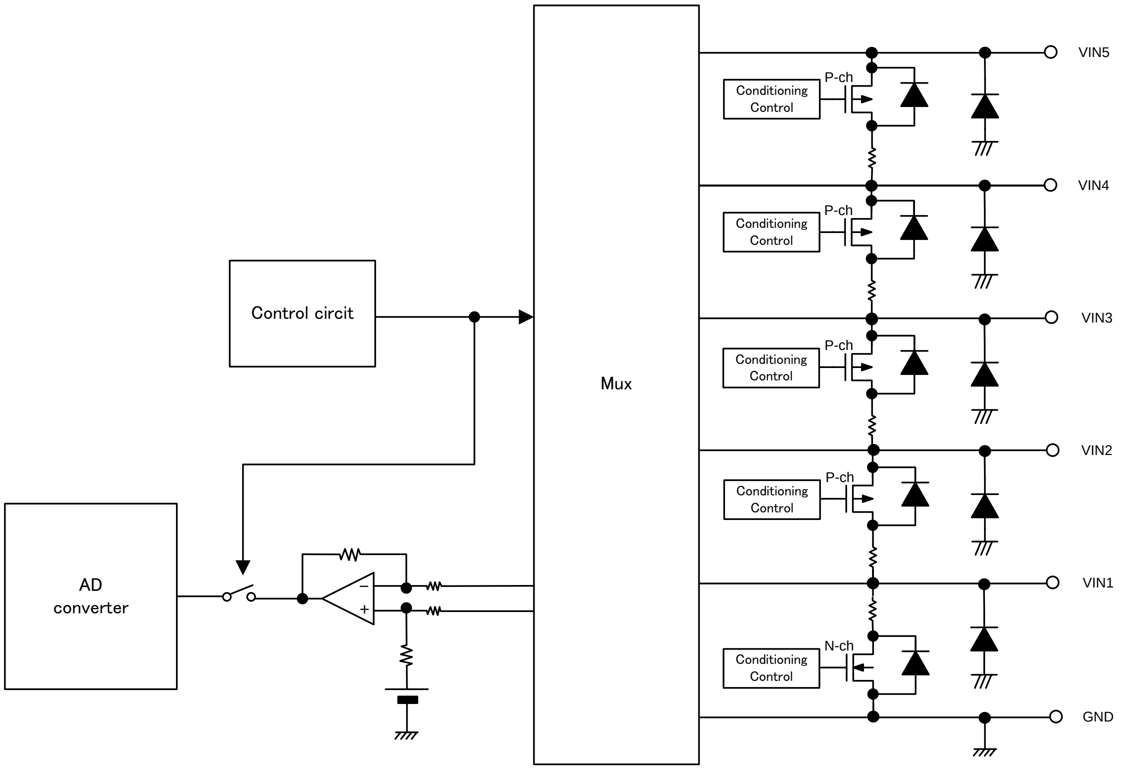
**RESET (AFE)**



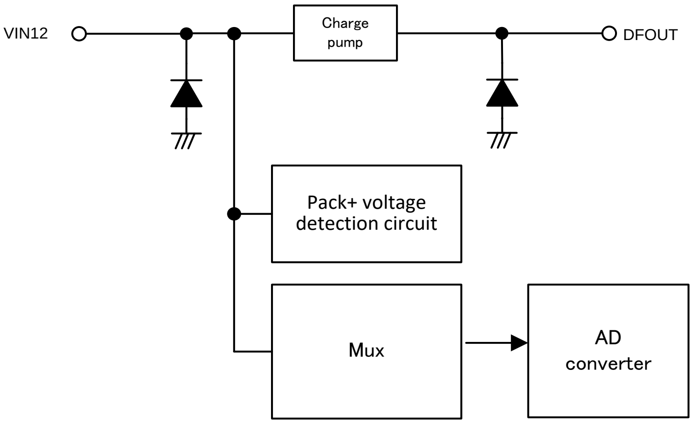
**FUSEOUT**



**VIN1, VIN2, VIN3, VIN4, VIN5**



**VIN12, DFOUT**



# 4. ELECTRICAL SPECIFICATIONS

**Caution This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used..**

## 4.1 Absolute Maximum Ratings

Absolute Maximum Ratings

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | VCC | | -0.5 to +35 | V |
| | GND | GND0, GND1 | | -0.5 to 0.3 | V |
| CREG1 pin input voltage | $V_{CREG1}$ | CREG1 | | -0.3 to +2.0 Note 1 | V |
| CREG2 pin input voltage | $V_{CREG2}$ | CREG2 | | -0.3 to +5.5 Note 3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | | -0.3 to 2.8 and -0.3 to (CREG2+0.3) Note 2 | V |
| Input voltage | $V_{I1}$ | P00, P02, P03, P10 to P14, P16, P17, P40 (TOOL0), P43, P50 to P54, P120, P122, P137, RESET(MCU) | | -0.3 to (CREG2+0.3) Note 4 | V |
| | $V_{I2}$ | SCL(P60), SDA(P61) (N-ch open-drain) | | -0.3 to +5.5 | V |
| | $V_{IN-H}$ | VIN5, VIN4, VIN3, VIN2, VIN1, VBAT, VIN12, SYSIN | | -0.5 to +35 | V |
| | $V_{IN-B}$ | VIN5 to VIN4, VIN4 to VIN3, VIN3 to VIN2, VIN2 to VIN1, VIN1 to GND0 | | -0.5 to +7 | V |
| | $V_{IN-L}$ | AN0, AN1, AN2, ISENS0, ISENS1 | | -0.3 to +2.0 | V |
| | $V_{AI}$ | ANI16, ANI17, ANI19 | | -0.3 to CREG2 +0.3 and -0.3 to AVREF(+) +0.3 Note 5 | V |
| Output voltage | $V_{O1}$ | P00, P02, P03, P10 to P14, P16, P17, P40 (TOOL0), P43, P50 to P54, P120, SCL(P60), SDA(P61) | | -0.3 to (CREG2+0.3) Note 4 | V |
| | $V_{O-H}$ | CFOUT, DFOUT | | -0.5 to +35 | V |
| | $V_{O-FH}$ | FUSEOUT | | -0.3 to VCC+0.3 and -0.5 to 30 | V |
| High-level output current | $I_{OH}$ | Per pin | P02, P03, P10 to P17, P43, P50 to P54, P120 | -40 | mA |
| | | Total of all pins | P02, P03, P10 to P17, P43, P50 to P54, P120 | -100 | mA |
| | $I_{OH-FH}$ | FUSEOUT | | -10 | mA |
| Low-level output current | $I_{OL}$ | Per pin | P02, P03, P10 to P17, P43, P50 to P54, P120 | +40 | mA |
| | | Total of all pins | P02, P03, P10 to P17, P43, P50 to P54, P120 | +100 | mA |
| Power consumption | Pd | Topr = 25 C | | 300 | mW |
| Operating ambient Temperature | TA | - | | -20 to +85 | C |
| Storage temperature | Tstg | - | | -65 to +150 | C |

**Note 1.** Connect the CREG1 pin to GND0 via a capacitor (1uF). This value regulates the absolute maximum rating of the CREG1 pin. Do not applied direct voltage to this pin.

**Note 2.** Connect the REGC pin to GND1 via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of the REGC pin. Do not applied direct voltage to this pin.

**Note 3.** Connect the CREG2 pin to GND1 via a capacitor (2.2uF). This value regulates the absolute maximum rating of the CREG2 pin. Do not applied direct voltage to this pin.

**Note 4.** Must be 6.5V or lower.

**Note 5.** Do not exceed AVREF (+) + 0.3V in case of A/D conversion target pin.

**Caution** **Product quality may degrade if the absolute maximum rating has been exceeded. The absolute maximum ratings are rated values where the product is on the verge of suffering physical damage, therefore the product must be used within conditions that ensure the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** GND (GND0, GND1): Reference voltage.

## 4.2 Power supply voltage condition

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply | VCC, VBAT | | 4.0 | - | 28.0 | V |
| | GND0, GND1 | | - | 0.0 | - | V |

## 4.3 Supply current characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2 = 3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. Note2 | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power down mode current Note 1 | ICC3 | VCC≦14V<br>AFE: Power down mode | - | (0.5) | 1.0 | uA |
| Sleep mode current Note 1 | ICC2 | TA=25C<br>MCU operation mode: STOP mode<br>AOCO = ON<br>CD = ALL ON, AFE timer = ON,<br>AFE WDT = ON, CFOUT = H, DFOUT = H,<br>ADC = OFF, CC = OFF | - | (150) | - | uA |
| Normal mode current Note 1 | ICC1 | MCU operation mode: LS (Low-Speed main) mode, $f_{HOCO}$=8MHz, fIH=8MHz<br>AOCO = ON<br>CD = ALL ON, AFE Timer = ON,<br>AFE WDT = ON, CFOUT = H, DFOUT = H,<br>ADC = ON, CC = ON | - | (2.0) | - | mA |

**Note 1.** This is the current which flows in VCC pin.

**Note 2.** Temperature condition of the TYP. value is TA=25 C.

**Caution After trimming.**

**Remark 1.** AOCO: AFE On-chip oscillator, CD: Overcurrent detection circuit, ADC: A/D converter circuit, CC: Current integrating circuit

**Remark 2.** fHOCO: high-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 3.** fIH: high-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** The numerical value in a parenthesis is a reference value.

## 4.4 Oscillator Characteristics

### 4.4.1 MCU On-chip oscillator characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, GND0 = GND1 = 0V )

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Note | $f_{IH}$ |  | - | 8 | - | MHz |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ |  | - | 15 | - | kHz |

**Note** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

### 4.4.2 AFE On-chip oscillator characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, GND0 = GND1 = 0V )

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| AFE on-chip oscillator clock frequency Note | $f_{AOCO}$ |  | - | 4.194 | - | MHz |
| AFE on-chip oscillator clock frequency accuracy |  |  | -2 | - | +2 | % |

**Note** This value is when it writes trimming data stored in flash memory to the OCOTRIM0 to OCOTRIM2 register.

**Caution After trimming.**

## 4.5 Pin characteristics

(1/3)

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH}$ | Per pin for P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120 | | | -10.0 Note 2 | mA |
| | | Total of P00, P02, P03, P40, P43, P120<br>(When duty ≤ 70% Note 3) | | | -10.0 | mA |
| | | Total of P10 to P14, P16, P17, P50 to P54<br>(When duty ≤ 70% Note 3) | | | -19.0 | mA |
| | | Total of all pins (When duty ≤70% Note 3) | | | -135.0 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the CREG2 pin to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current from pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA

Total output current from pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

**Caution** **P00, P02, P03, P10 to P14, P16 and P17 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/3)

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Output current, low [Note 1] | $I_{OL}$ | Per pin for P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120 | | | 20.0 [Note 2] | mA |
| | | Per pin for P60, P61 | | | 15.0 [Note 2] | mA |
| | | Total of P00, P02, P03, P40, P43, P120 (When duty ≤ 70% [Note 3]) | | | 15.0 | mA |
| | | Total of P10 to P14, P16, P17, P50 to P54, P60, P61 (When duty ≤ 70% [Note 3]) | | | 35.0 | mA |
| | | Total of all pins (When duty ≤70% [Note 3]) | | | 150 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the GND pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/3)

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00, P02, P03, P10 to P14, P16, P17, P43, P50 to P54, P120, P122, P137, P40/TOOL0, RESET(MCU) $^{\text{Note1}}$ (normal input buffer) | | 0.8 CREG2 | | CREG2 | V |
| | $V_{IH2}$ | SCL(P60), SDA(P61) | | 2.1 | | CREG2 | V |
| | $V_{IH3}$ | SYSIN | | 0.7 CREG2 | | 6.0 | V |
| | $V_{IH4}$ | FUSEOUT | | 2 | | VCC | V |
| | $V_{IH5}$ | P03, P04, P10, P16, P17, P43, P50, P53, P54 (TTL Input buffer) | | 2 | | CREG2 | V |
| Input voltage, low | $V_{IL1}$ | P00, P02, P03, P10 to P14, P16, P17, P43, P50 to P54, P120, P122, P137, P40/TOOL0, RESET(MCU) $^{\text{Note1}}$ (normal input buffer) | | 0 | | 0.2 CREG2 | V |
| | $V_{IL2}$ | SCL(P60), SDA(P61) | | 0 | | 0.8 | V |
| | $V_{IL3}$ | SYSIN | | 0 | | 0.3 CREG2 | V |
| | $V_{IL4}$ | FUSEOUT | | 0 | | 0.5 | V |
| | $V_{IL5}$ | P03, P04, P10, P16, P17, P43, P50, P53, P54 (TTL Input buffer) | | 0 | | 0.5 | V |
| Output voltage High | $V_{OH1}$ | P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120 $^{\text{Note2}}$ | IOH = -1.5mA | CREG2 - 0.5 | - | CREG2 | V |
| Output voltage Low | $V_{OL1}$ | P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120 $^{\text{Note2}}$ | IOL = 1.5mA | - | - | 0.4 | V |
| | $V_{OL2}$ | SCL(P60), SDA(P61) | IOL = 3.0 mA | - | - | 0.4 | V |
| FUSEOUT Output High Voltage | $V_{OH\text{-}FUSE}$ | External Pulldown 100 kΩ | | VCC - 0.5 | - | - | V |
| Input leak current High | $I_{LIH1}$ | P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120, P122, P137, P40/TOOL0, RESET(MCU) | VI = CREG2 | - | - | 1 | µA |
| Input leak current Low | $I_{LIL1}$ | P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120, P122, P137, P40/TOOL0, RESET(MCU) | VI = GND1 | - | - | -1 | µA |
| Pull-up resistor | $R_U$ | P00, P02, P03, P10 to P14, P16, P17, P40, P43, P50 to P54, P120 | VI = GND1, When input port | 10 | 20 | 100 | kΩ |
| | $R_{UA}$ | AN0, AN1, AN2 | VI = GND1 | 7.5 | (10) | 12.5 | kΩ |
| | $R_{UAR}$ | RESET (AFE) | VI = GND1 | - | (20) | - | kΩ |

**Note 1.** The maximum value of VIH of pins P00, P02, P03, P10, P11, P13, P14, P17, P43 and P50 to P54 are CREG2, even in N-ch open drain mode.

**Note 2.** P00, P02, P03, P10, P11, P13, P14, P17, P43, and P50 to P54 do not output a high-level in N-ch open drain mode.

**Remark 1.** Unless specified, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** Regarding pin characteristics of CFOUT, DFOUT, refer to Section 4.8.5 Charge/discharge FET control circuit characteristics.

**Remark 3.** Regarding pin characteristics of VIN1 to VIN5 refer to Section 4.8.1 Multiplexer characteristics.

**Remark 4.** The parenthetical values are for reference.

## 4.6 AC Characteristics

(1/2)

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 0.03125 | | 1 | us |
| | | | LS (low-speed main) mode | 0.125 | | 1 | us |
| | | | LV (low-voltage main) mode | 0.25 | | 1 | us |
| | | In the self-programming mode | HS (high-speed main) mode | 0.03125 | | 1 | us |
| | | | LS (low-speed main) mode | 0.125 | | 1 | us |
| | | | LV (low-voltage main) mode | 0.25 | | 1 | us |
| TI00 to TI02 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | $1/f_{MCK}$ +10 | | | ns |

**Remark** $f_{MCK}$ : Timer array unit operation clock frequency

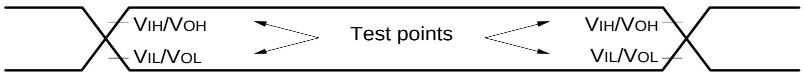
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

(2/2)

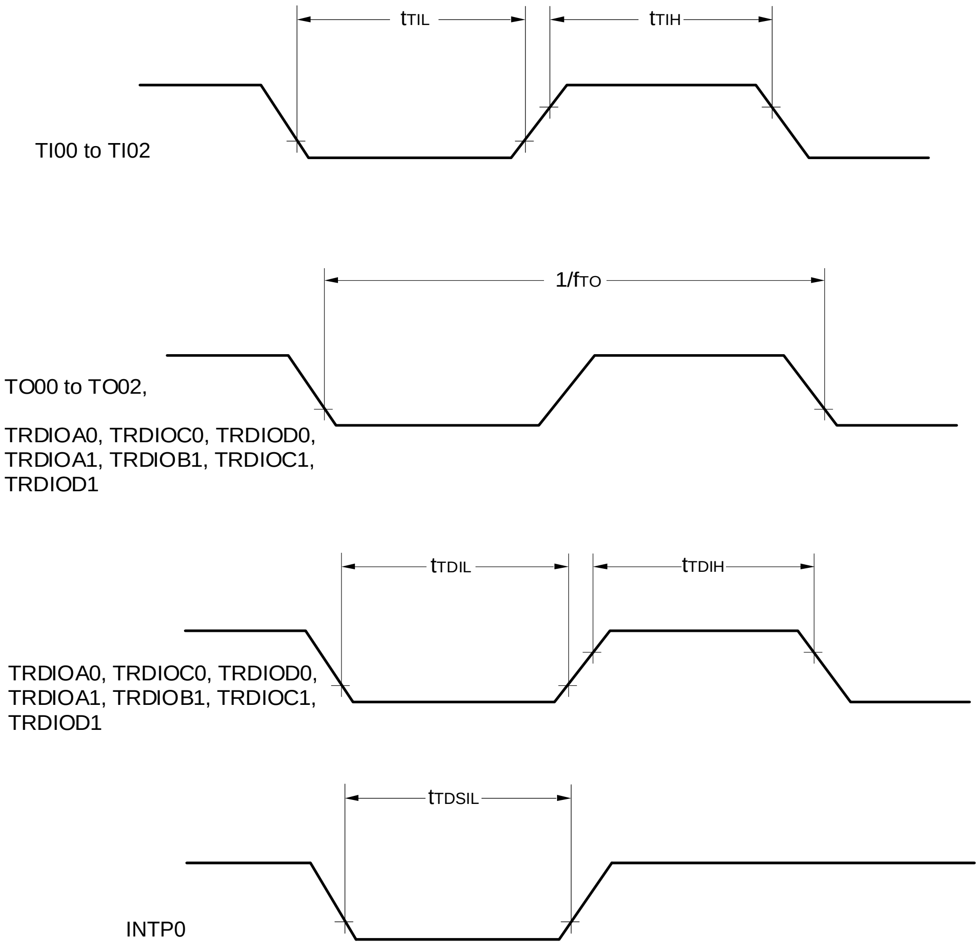
(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Timer RD input high-level width, low-level width | $t_{TDIH}$,<br>$t_{TDIL}$ | TRDIOA0, TRDIOC0, TRDIOD0<br>TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1 | $3/f_{CLK}$ | | | ns |
| TO00 to TO02, TRDIOA0, TRDIOC0, TRDIOD0 TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1 output frequency | $f_{TO}$ | HS (high-speed main) mode | | | 8 | MHz |
| | | LS (low-speed main) mode | | | 4 | MHz |
| | | LV(low-voltage main) mode | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$,<br>$t_{INTL}$ | INTP0 to INTP2, INTP5 | 1 | | | us |
| RESET low-level width | $t_{RSL}$ | | 10 | | | us |

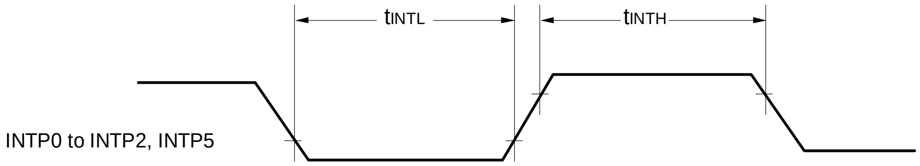
## AC Timing Test Points



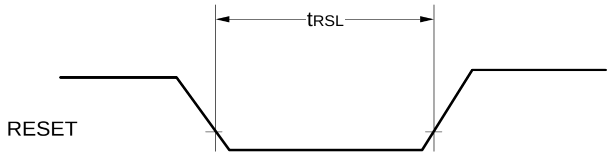
## TI/TO Timing



### Interrupt Request Input Timing



### RESET Input Timing



## 4.7 MCU peripheral circuit characteristics

### AC Timing Test Points

### 4.7.1 Serial array unit

(1) During communication at same potential (UART mode)

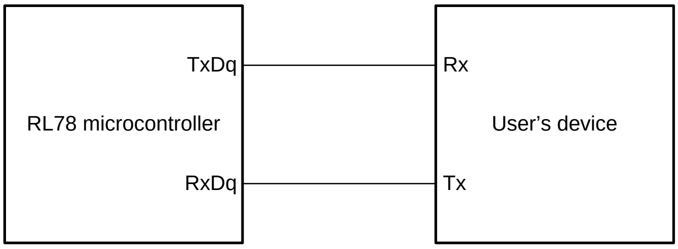
($T_A$ = -20 to +85C, 4.0V ≤ $V_{CC}$ ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | | | $f_{MCK}$/6 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate<br>$f_{MCK} = f_{CLK}$ Note2 | | 5.3 | | 1.3 | | 0.6 | Mbps |

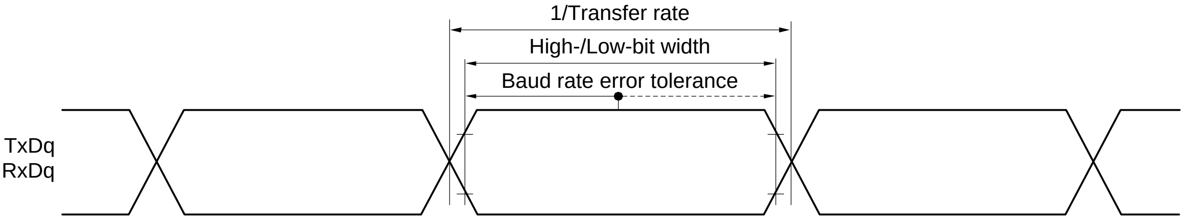
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**Note 2.** The maximum operating frequencies of the CPU/pripheral hardware clock ($f_{CLK}$) are:
HS mode: 32MHz, LS mode: 8MHz, LV mode: 4MHz

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**



**UART mode connection diagram (during communication at same potential)**



**UART mode bit width (during communication at same potential) (reference)**

**Remark 1.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

**Remark 2.** $f_{CK}$: Serial array unit operation clock frequency
Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 125 | | 500 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | | $t_{KCY1}/2 - 18$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | | 44 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | | 25 | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 11), m: Unit number (m = 0), n: Channel number (n = 3), g: PIM number (g = 1)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 03)

### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

($T_A$ = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 1 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | — | | ns |
| | | $f_{MCK}$ ≤ 16MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$,<br>$t_{KL2}$ | | tKCY2/2 - 8 | | tKCY2/2 - 8 | | tKCY2/2 - 8 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | | 1/fMCK + 20 | | 1/fMCK + 30 | | 1/fMCK + 30 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | 1/fMCK + 31 | | 1/fMCK + 31 | | 1/fMCK + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30pF Note 4 | | 2/fMCK + 44 | | 2/fMCK + 110 | | 2/fMCK + 110 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

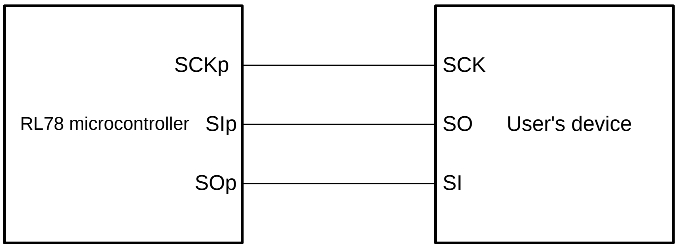
**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution** **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 11), m: Unit number (m = 0), n: Channel number (n = 3), g: PIM number (g = 1)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 03)

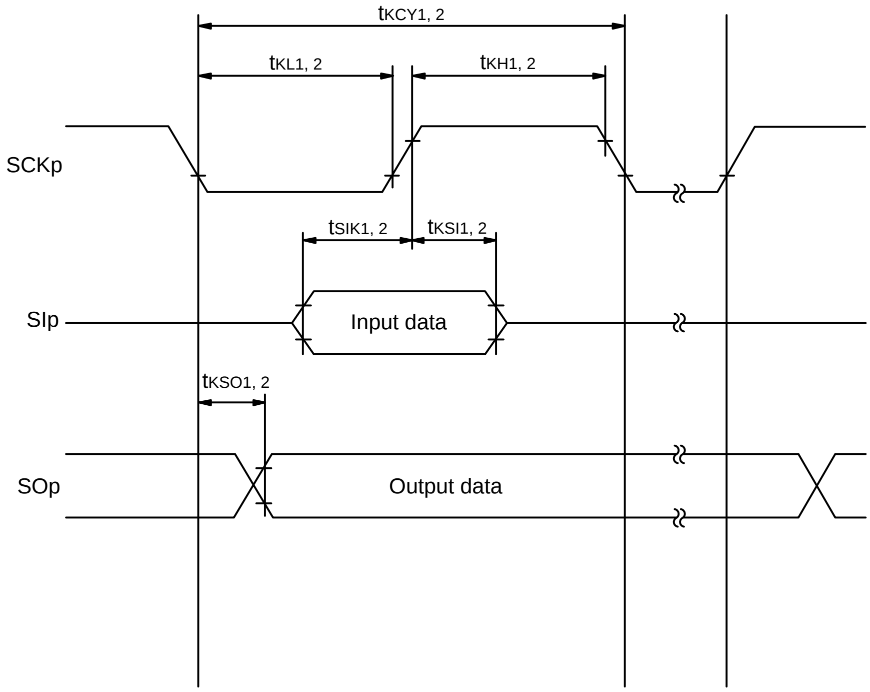


**CSI mode connection diagram (during communication at same potential)**

**Remark 1.** p: CSI number (p = 11)

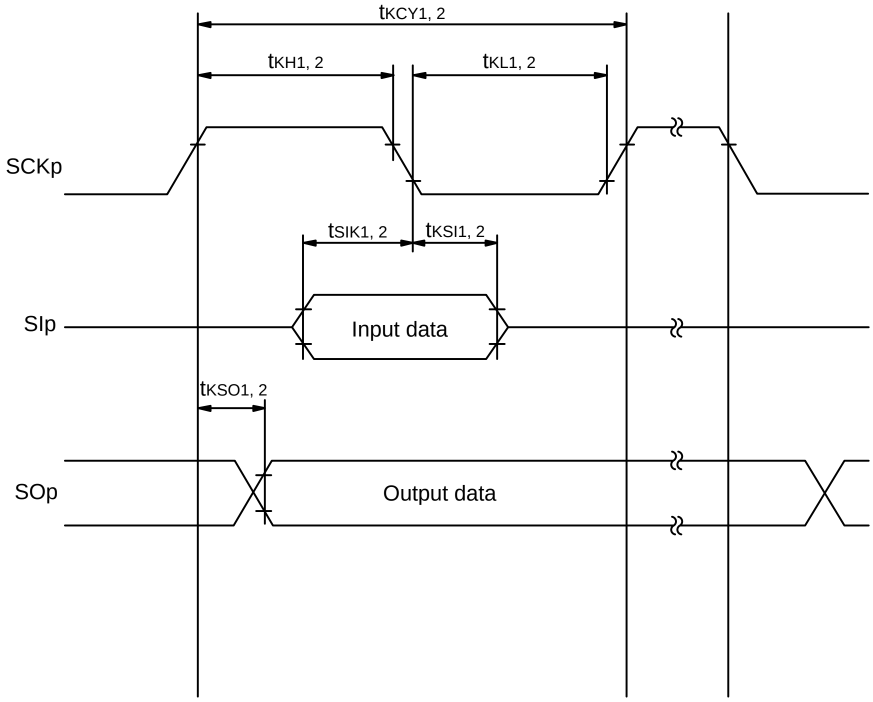
**Remark 2.** m: Unit number, n: Channel number (mn = 03)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



CSI mode serial transfer timing (during communication at same potential)

**Remark 1.** p: CSI number (p = 11)

**Remark 2.** m: Unit number, n: Channel number (mn = 03)

### (4) During communication at same potential (simplified I$^2$C mode)

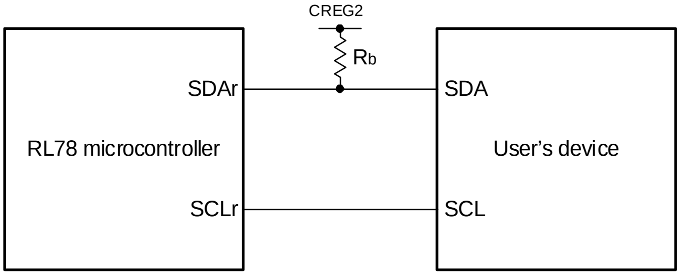
(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS ( high-speed main ) mode | | LS ( low-speed main ) mode | | LV ( low-voltage main ) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | Cb = 50pF, Rb = 2.7kΩ | | 1000[Note 1] | | 400[Note 1] | | 400[Note1] | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | Cb = 50pF, Rb = 2.7kΩ | 475 | | 1150 | | 1150 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | Cb = 50pF, Rb = 2.7kΩ | 475 | | 1150 | | 1150 | | ns |
| Data setup time (reception) | $t_{SU:\ DAT}$ | Cb = 50pF, Rb = 2.7kΩ | $1/f_{MCK}$ + 85[Note 2] | | $1/f_{MCK}$ + 145[Note 2] | | $1/f_{MCK}$ + 145[Note2] | | ns |
| Data hold time (transmission) | $t_{HD:\ DAT}$ | Cb = 50pF, Rb = 2.7kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |

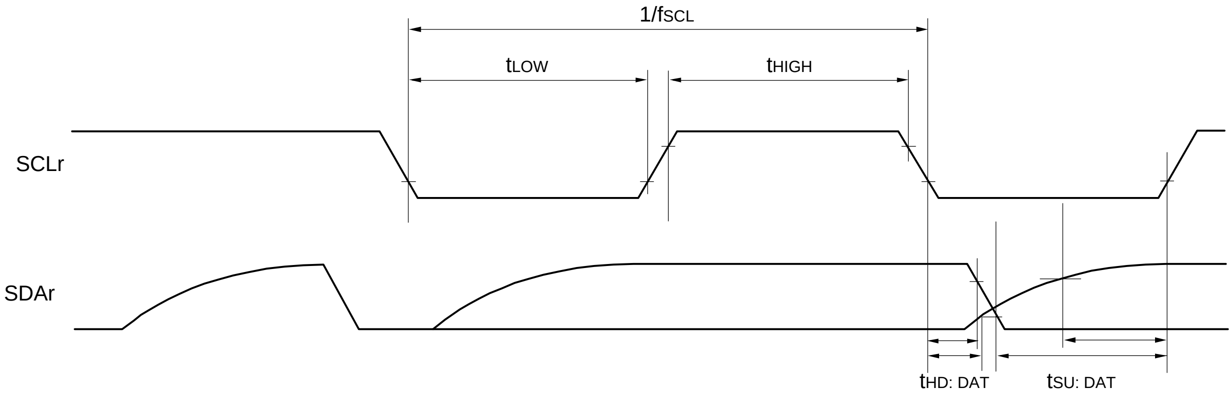
**Note 1.** The value must also be equal to or less than $f_{MCK}/4$.

**Note 2.** Set the $f_{MCK}$ value not to over the hold time of SCLr = “L” and SCLr = “H”.

**Caution** **Select the normal input buffer and the N-ch open drain output (CREG2 tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**



**Simplified I$^2$C mode connection diagram (during communication at same potential)**



**Simplified I$^2$C mode serial transfer timing (during communication at same potential)**

**Remark 1.** Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 11), g: PIM, POM number (g = 1)

**Remark 3.** fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 03)

### 4.7.2 Serial interface IICA

(1) $I^2C$ standard mode

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode:<br>$f_{CLK} \geq$ 1MHz | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | | 4.7 | | 4.7 | | 4.7 | | us |
| Hold time Note 1 | $t_{HD: STA}$ | | 4.0 | | 4.0 | | 4.0 | | us |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | | 4.7 | | 4.7 | | 4.7 | | us |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | | 4.0 | | 4.0 | | 4.0 | | us |
| Data setup time (reception) | $t_{SU: DAT}$ | | 250 | | 250 | | 250 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | us |
| Setup time of stop condition | $t_{SU: STO}$ | | 4.0 | | 4.0 | | 4.0 | | us |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 4.7 | | 4.7 | | us |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400pF, Rb = 2.7kΩ

(2) $I^2C$ fast mode

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode:<br>fCLK ≥ 3.5 MHz | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:\ STA}$ | | 0.6 | | 0.6 | | 0.6 | | us |
| Hold time[Note1] | $t_{HD:\ STA}$ | | 0.6 | | 0.6 | | 0.6 | | us |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 1.3 | | 1.3 | | 1.3 | | us |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 0.6 | | 0.6 | | 0.6 | | us |
| Data setup time (reception) | $t_{SU:\ DAT}$ | | 100 | | 100 | | 100 | | ns |
| Data hold time (transmission) Note2 | $t_{HD:\ DAT}$ | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | us |
| Setup time of stop condition | $t_{SU:\ STO}$ | | 0.6 | | 0.6 | | 0.6 | | us |
| Bus-free time | $t_{BUF}$ | | 1.3 | | 1.3 | | 1.3 | | us |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: Cb = 320pF, Rb = 1.1kΩ

### (3) $I^2C$ fast mode plus

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus:<br>fCLK ≥ 10 MHz | 0 | 1000 | | | | | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | | 0.26 | | | | | | us |
| Hold time[Note 1] | $t_{HD: STA}$ | | 0.26 | | | | | | us |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | | 0.5 | | | | | | us |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | | 0.26 | | | | | | us |
| Data setup time (reception) | $t_{SU: DAT}$ | | 50 | | | | | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD: DAT}$ | | 0 | 0.45 | | | | | us |
| Setup time of stop condition | $t_{SU: STO}$ | | 0.26 | | | | | | us |
| Bus-free time | $t_{BUF}$ | | 0.5 | | | | | | us |

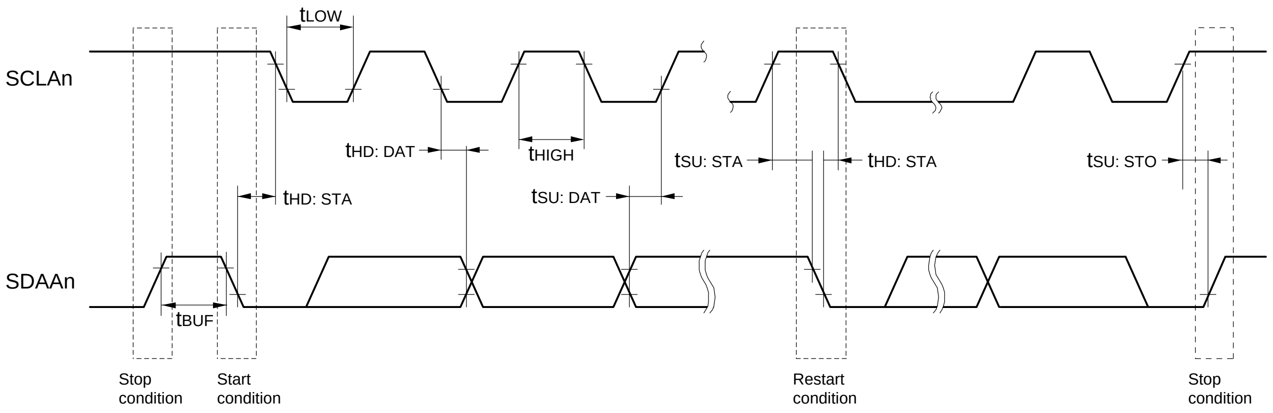
**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected

**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: Cb = 120pF, Rb = 1.1kΩ



**IICA serial transfer timing**

**Remark** n = 0

### 4.7.3 Interrupt

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Item | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Interrupt input high-level width, low-level width | $t_{INTH}$,<br>$t_{INTL}$ | INTP0, INTP5 | 1 | - | - | us |

### 4.7.4 A/D converter characteristics

When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) =Vss (ADREFM = 0), target pin: ANI16, ANI17, ANI19

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V, Reference voltage (+) = VBGR, Reference voltage (-) = AVREFM = 0V

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | RES | | 8 | | bits | |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 17 | | 39 | us |
| Zero-scale error Note 1, 2 | $E_{ZS}$ | 8-bit resolution | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Reference voltage (+) | $V_{BGR}$ | | 1.38 | 1.45 | 1.5 | V |
| Reference voltage (-) | $AV_{REFM}$ | | VSS | | | V |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

## 4.8 AFE peripheral circuit characteristics

### 4.8.1 Multiplexer characteristics

(TA = 25C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Offset voltage | Voff | VCC=VIN5≥2.0 V x (number of Battery cells) | - | (100) | - | mV |
| Gain<br>VIN(n)-VIN(n-1) | GAIN1 | VCC=VIN5≥2V x (number of series cells)<br>VIN5,VIN4,VIN3,VIN2,VIN1>0V Note | | (0.28) | | V/V |
| Gain<br>VIN12 | GAIN2 | VCC≥2V x (number of series cells) | | (0.06) | | V/V |
| Gain AN0,1,2 | GAIN3 | | | 1.0 | | V/V |
| Input voltage range<br>VIN(n)-VIN(n-1) | VRA1 | VIN5,VIN4,VIN3,VIN2,VIN1>0V Note | 0.0 | | 5.0 | V |
| Input voltage range<br>VIN12 | VRA2 | | 0.0 | | 25.0 | V |
| Input voltage range<br>VIN5 | VRA3 | | 0.0 | | 28.0 | V |
| Input voltage range<br>AN0, 1, 2 | VRA4 | | 0.0 | | CREG1 | V |

**Note** Reference voltage is GND0 and GND1.

**Remark** Values in brackets are design value.

### 4.8.2 Sigma-delta A/D converter characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, CREG1=1.8V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution Note1 | - | Conversion time = 8ms | | | 15 | bits |
| | | Conversion time = 4ms | | | 14 | bits |
| | | Conversion time = 2ms | | | 13 | bits |
| | | Conversion time = 1ms | | | 12 | bits |
| Input voltage range | - | | 0 | | CREG1 | V |
| Integral nonlinearity | - | Endfit | -16 | | 16 | LSB |
| Conversion result in zero input | - | VIN=GND0 | | 3266 Note 2 | | LSB |
| Temperature dependency In zero input | - | VIN=GND0 | -0.24 | | +0.24 | LSB/C |
| Conversion result in full-scale input | - | VIN=CREG1 | | 29453 Note 2 | | LSB |
| Temperature dependency in full-scale input | - | VIN=CREG1 | -0.24 | | +0.24 | LSB/C |

**Note 1.** AD conversion result is output in 15-bit.

**Note 2.** This value is before subtracting the offset voltage and design value.

**Caution Calibration is needed to keep high accuracy in system.**

### 4.8.3 Current integrating circuit characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, CREG1=1.8V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | - | | | | 18 | bits |
| Conversion time | - | f1=4,194,304 Hz | | (250) | | ms |
| Input voltage range | - | ISENS1 to ISENS0 | -100 | | +100 | mV |
| Integral nonlinearity | - | Endfit | | | 0.02 | %FSR |
| Input resistance | IICC | ISENS0, ISENS1 | | (0.2) | | uA |

**Caution Calibration is needed to keep high accuracy in system.**

**Remark** Values in brackets are design value.

### 4.8.4 Overcurrent detection / wakeup current detection circuit characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, CREG1=1.8V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Discharge short-circuit current detection 1 setting voltage step | - | 0.1V to 0.8V | | 0.1 | | V |
| Discharge short-circuit current detection 2 setting voltage step | - | 25mv to 100mV | | 12.5 | | mV |
| | | 100mV to 250mV | | 25 | | mV |
| Discharge short-circuit current detection 1 voltage error | - | 0.1V to 0.8V | | | ±50 | mV |
| Discharge short-circuit current detection 2 voltage error | - | 25mv to 100mV setting | | | ±10 | mV |
| | | 125mV to 250mV setting | | | ±25.0 | mV |
| Discharge overcurrent detection setting voltage step | - | 25mV to 50mV | | 2.5 | | mV |
| | | 50mV to 100mV | | 5 | | mV |
| Discharge overcurrent detection voltage error Note 1 | - | 25mV to 50mV setting | | | ±10 | mV |
| | | 55mV to 100mV setting | | | ±25 | mV |
| Charge overcurrent detection setting voltage step | - | -100mV to -25mV | | 12.5 | | mV |
| | | -250mV to -100mV | | 25 | | mV |
| Charge overcurrent detection voltage error Note 1 | - | -100mV to -25mV setting | | | ±10 | mV |
| | | -250mV to -125mV setting | | | ±25 | mV |
| Discharge wakeup current detection setting voltage step | - | 0mV to 145mV | | 2.5 | | mV |
| Charge wakeup current detection setting voltage step | - | -145mV to 0mV | | 2.5 | | mV |
| Discharge wakeup current detection voltage error Note 1 | - | 10 times mode 1A detection sense resistance 5mΩ | 4.0 | 5.0 | 6.0 | mV |
| Charge wakeup current detection voltage error Note 1 | - | 10 times mode -1A detection sense resistance 5mΩ | -6.0 | -5.0 | -4.0 | mV |
| DBPT current detection voltage error Note 1 | - | 10 times mode 1A detection sense resistance 5mΩ | 4.0 | 5.0 | 6.0 | mV |
| Discharge short-circuit current detection 1 time error Note 2 | - | 0us to 427us (61us step | 0.0 | | 30.5 | us |
| Discharge short-circuit current detection 2 time error Note 2 | - | 0us to 915us (61us step | 0.0 | | 30.5 | us |
| Discharge overcurrent detection time error Note 2 | - | 0.916ms to 30.212ms (1.95ms step) | 0.0 | | 30.5 | us |
| Charge overcurrent detection time error | - | 0us to 915us (61us step) | 0.0 | | 30.5 | us |
| Discharge wakeup current detection time error Note 2 | - | - | 58.6 | | 62.5 | ms |
| Charge wakeup current detection time error Note 2 | - | - | 58.6 | | 62.5 | ms |
| DBPT current detection time error Note 2 | - | - | 58.6 | | 62.5 | ms |

**Note 1.** This is the specification after zero-calibration is executed.

**Note 2.** The frequency error of On-chip oscillator and the error due to the temperature characteristics of the detection circuit are excluded from these detection time error.

### 4.8.5 Charge/discharge FET control circuit characteristics

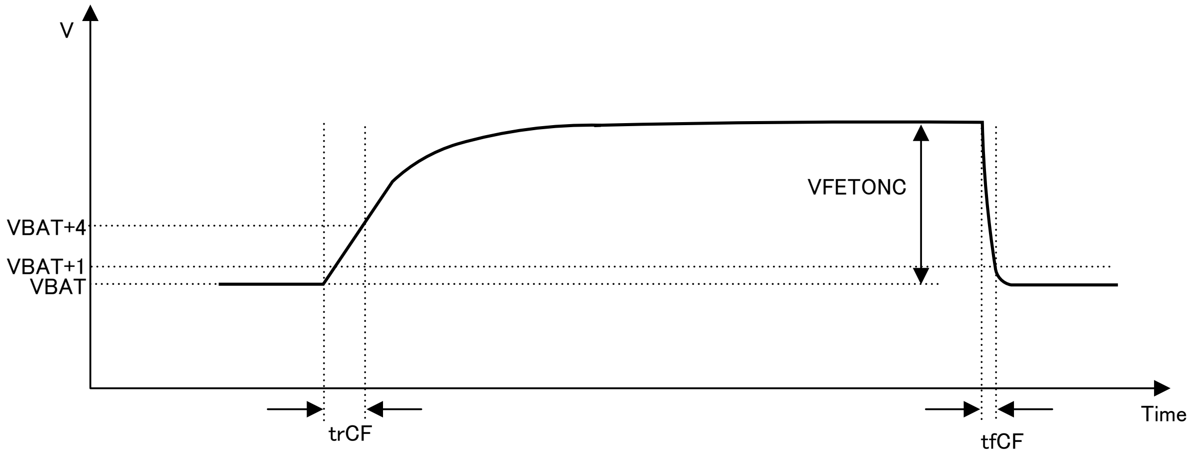
(TA = 25C, 4.0V ≤ VCC ≤ 25V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-side Charge FET control Output voltage, CFOUT=H | VFETONC1 | 4.0V ≤ VCC < 6.0V<br>Load between CFOUT to VBAT = 4700pF/10MΩ<br>Based on VBAT pin | 4.0 | (7.0) | 12.0 | V |
| | VFETONC2 | 6.0V ≤ VCC<br>Load between CFOUT to VBAT = 4700pF/10MΩ<br>Based on VBAT pin | 9.0 | (10.0) | 12.0 | V |
| High-side Charge FET control Output voltage, CFOUT=L | VFETOFFC | Load between CFOUT to VBAT = 4700pF/10MΩ<br>Based on VBAT pin, VBAT=14V | - | (0.0) | 0.2 | V |
| High-side Charge FET control CFOUT rise Time | trCF1 | 4.0V ≤ VCC < 6.0V<br>Load between CFOUT to VBAT = 4700pF/10MΩ<br>Lo(VBAT)→Hi(VBAT+4V) | - | (1.0) | 3.0 | ms |
| | trCF2 | 6.0V ≤ VCC<br>Load between CFOUT to VBAT = 4700pF/10MΩ<br>Lo(VBAT)→Hi(VBAT+4V) | - | (0.2) | 0.6 | ms |
| High-side Charge FET control CFOUT fall Time | tfCF | Load between CFOUT to VBAT = 4700pF/10MΩ<br>Hi(VBAT+4V)→Lo(VBAT+1V) | - | (0.08) | 0.2 | ms |
| High-side Discharge FET control Output voltage, DFOUT=H | VFETOND1 | 4.0 ≤ VCC < 6.0V<br>Load between DFOUT to VIN12 = 4700pF/10MΩ<br>Based on VIN12 pin | 4.0 | (7.0) | 12.0 | V |
| | VFETOND2 | 6.0 ≤ VCC<br>Load between DFOUT to VIN12 = 4700pF/10MΩ<br>Based on VIN12 pin | 9.0 | (10.0) | 12.0 | V |
| High-side Discharge FET control Output voltage, DFOUT=L | VFETOFFD | Load between DFOUT to VIN12 = 4700pF/10MΩ<br>Based on VIN12 pin | - | (0.0) | 0.2 | V |
| High-side Discharge FET control DFOUT rise Time | trDF1 | 4.0V ≤ VCC < 6.0V<br>Load between DFOUT to VIN12 = 4700pF/10MΩ<br>Lo(VIN12)→Hi(VIN12+4V) | - | (1.0) | 3.0 | ms |
| | trDF2 | 6.0V ≤ VCC<br>Load between DFOUT to VIN12 = 4700pF/10MΩ<br>Lo(VIN12)→Hi(VIN12+4V) | - | (0.2) | 0.6 | ms |
| High-side Discharge FET control DFOUT fall Time | tfDF | Load between DFOUT to VIN12 = 4700pF/10MΩ<br>Hi(VIN12+4V)→Lo(VIN12)<br>External constant of VIN12: C=0.01uF, R=10kΩ | - | (0.25) | 0.4 | ms |

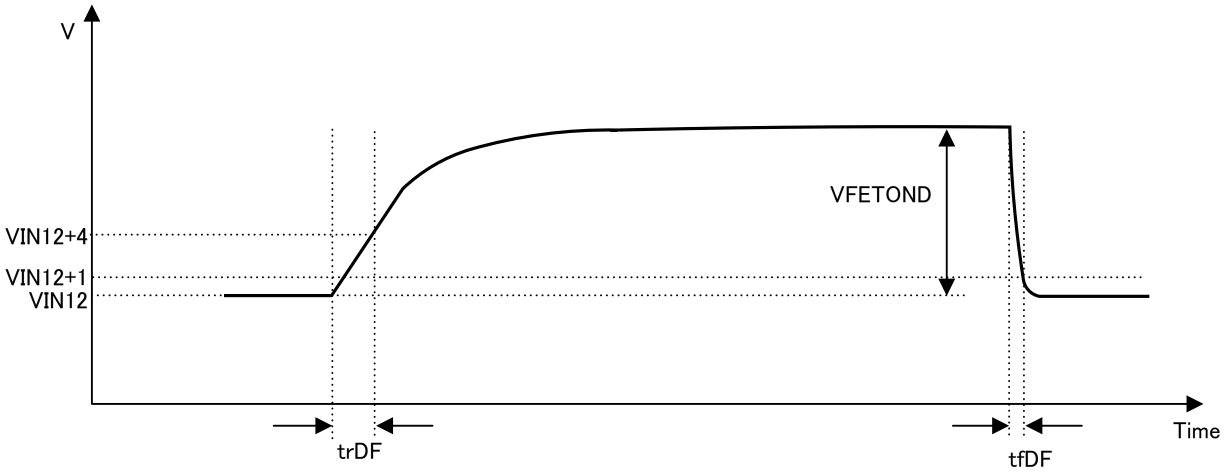
**Caution After trimming.**

**Remark** Values in brackets are design value.

### CFOUT output timing characteristic



### DFOUT output timing characteristic



### 4.8.6 Series regulator circuit characteristics

(TA = 25C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CREG2 output voltage | Vreg2o | VCC=14V, Io=50uA after triming | - | (3.3) | - | V |
| CREG2 Load drive capability Note | VR2d | 4.0V ≤ VCC=VIN5m, 3.0V ≤ CREG2 | 20.0 | - | - | mA |
| CREG1 output voltage | Vreg1o | VCC=14V, Io=10uA after triming | 1.755 | - | 1.845 | V |

**Note** In case of using load drive, total power consumption must be under the maximum ratings power consumption (Pd).

**Caution** **After trimming**.

**Remark** Values in brackets are design value.

### 4.8.7 Cell balancing circuit characteristics

(TA = 25C, VCC=17.5V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| 1st cell on resistance | $R_{ON1}$ | VCC=VBAT=VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V, 1cell balancing SW: ON | - | (500) | - | Ω |
| 2nd cell on resistance | $R_{ON2}$ | VCC=VBAT=VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V, 2cell balancing SW: ON | - | (500) | - | Ω |
| 3rd cell on resistance | $R_{ON3}$ | VCC=VBAT=VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V, 3cell balancing SW: ON | - | (500) | - | Ω |
| 4th cell on resistance | $R_{ON4}$ | VCC=VBAT=VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V, 4cell balancing SW: ON | - | (500) | - | Ω |
| 5th cell on resistance | $R_{ON5}$ | VCC=VBAT=VIN5=17.5 V, VIN4=14V, VIN3=10.5 V, VIN2=7 V, VIN1=3.5 V, 5cell balancing SW: ON | - | (500) | - | Ω |

**Remark** Values in brackets are design value.

## 4.9 Flash Memory Programming Characteristics

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | | 1 | | 32 | MHz |
| Number of code flash rewrites Note 1, 2, 3 | $C_{erwr}$ | Retained for 20 years<br>$T_A$ = 85 C | 1,000 | | | Times |
| Number of data flash rewrites Note 1, 2, 3 | | Retained for 1 year<br>$T_A$ = 25 C | | 1,000,000 | | |
| | | Retained for 5 years<br>$T_A$ = 85 C | 100,000 | | | |
| | | Retained for 20 years<br>$T_A$ = 85 C | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retained years are until next rewrite completion.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 4.10 Dedicated Flash Memory Programmer Communication (UART)

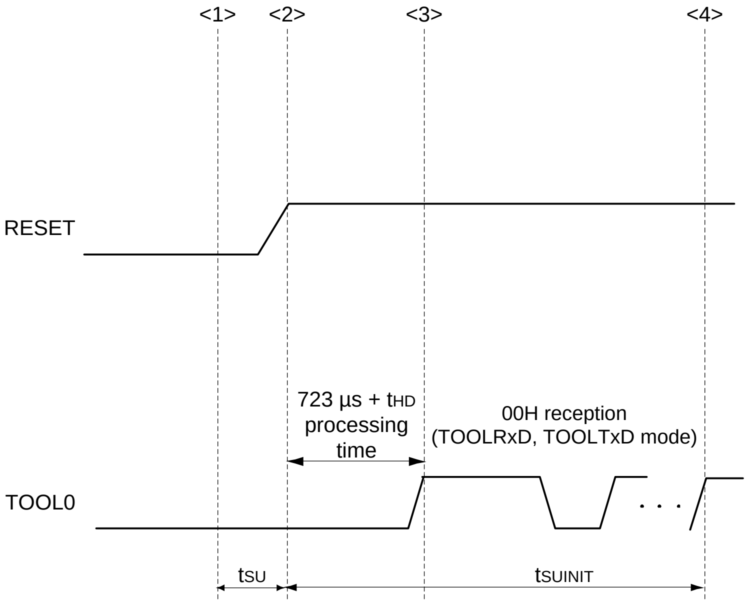
(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 4.11 Timing of Entry to Flash Memory Programming Modes

(TA = -20 to +85C, 4.0V ≤ VCC ≤ 28V, CREG2=3.3V, GND0 = GND1 = 0V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| The time needed when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| The time needed from when the TOOL0 pin is placed at low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | us |
| The time needed for the TOOL0 pin must be kept at low level after an external reset ends<br>(excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** tSUINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tSU: Time needed for the TOOL0 pin is placed at low level until the pin reset ends

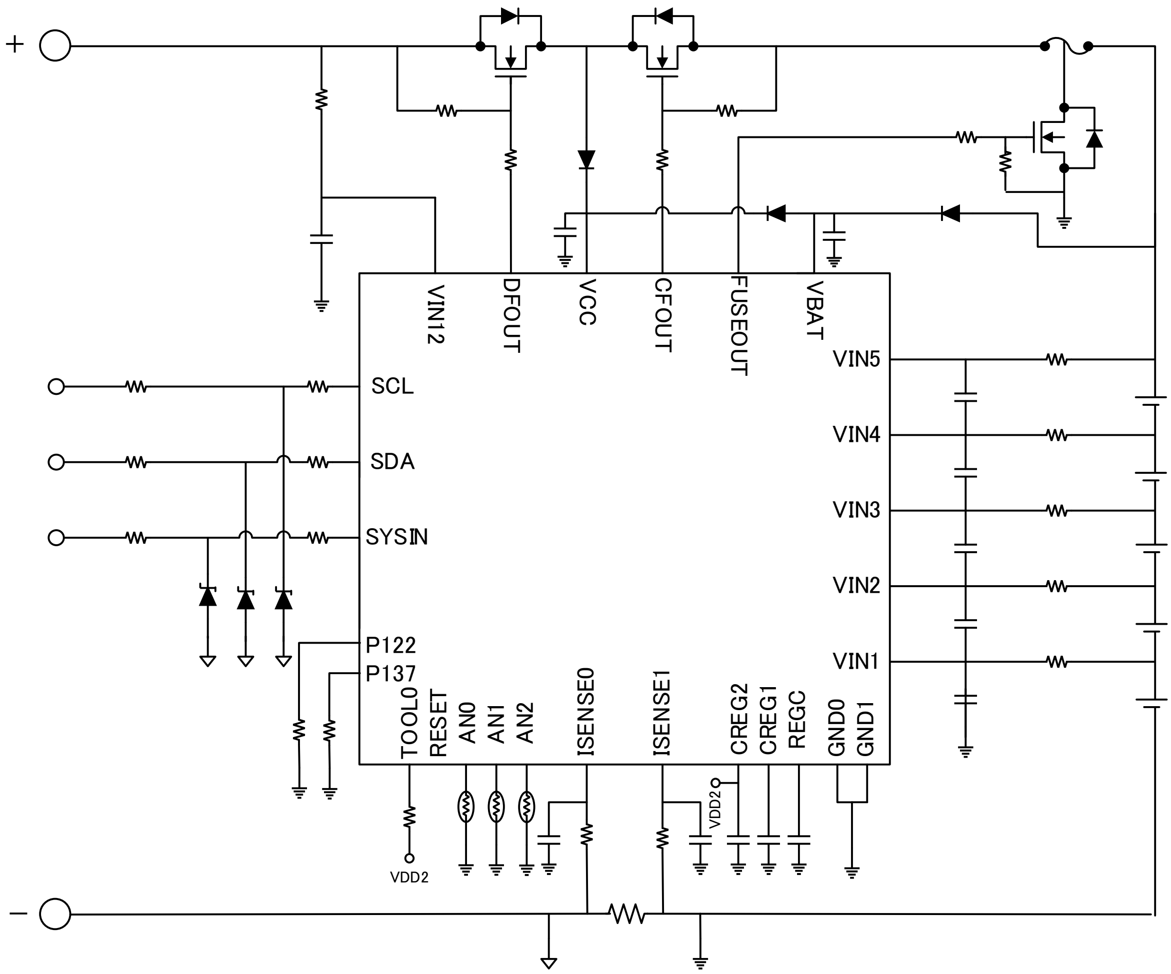
tHD: Time needed for the TOOL0 pin at low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

# 5. Detailed description

## 5.1 Overview

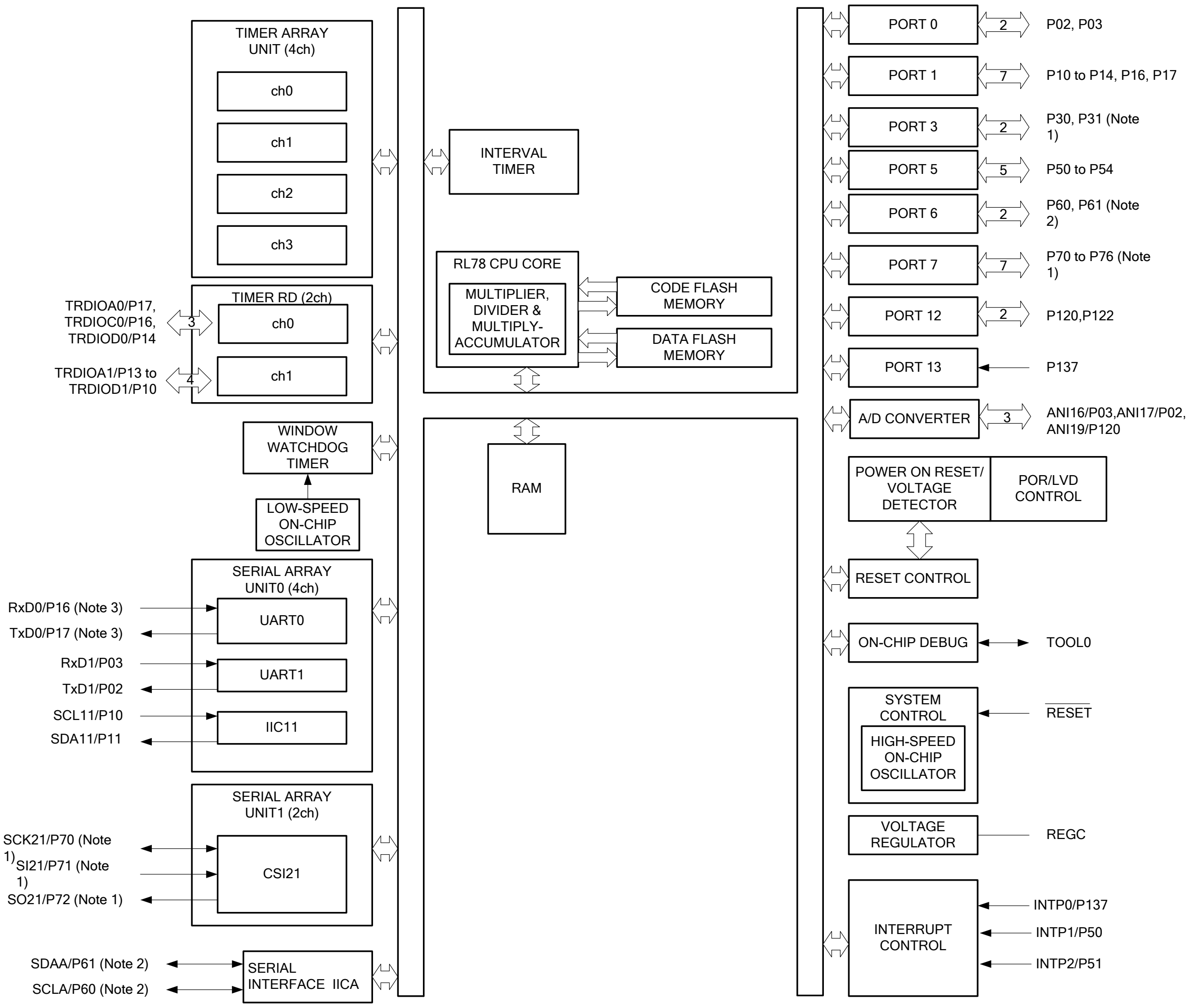
RAJ240080 is Renesas fuel gauge ICs which consists of a MCU block and an AFE block in a single package and accomplish various protection mechanisms. This IC's incorporates advanced battery management features such as primary and secondary protection, voltage and current measurement, current integration, host communication interface. By using the battery management controlled firmware and data are stored in the embedded flash memory to control the embedded analog and digital hardware circuits, optimum battery management operation including high accuracy remaining capacity estimation and battery safety can be achieved.

## 5.2 System block diagram



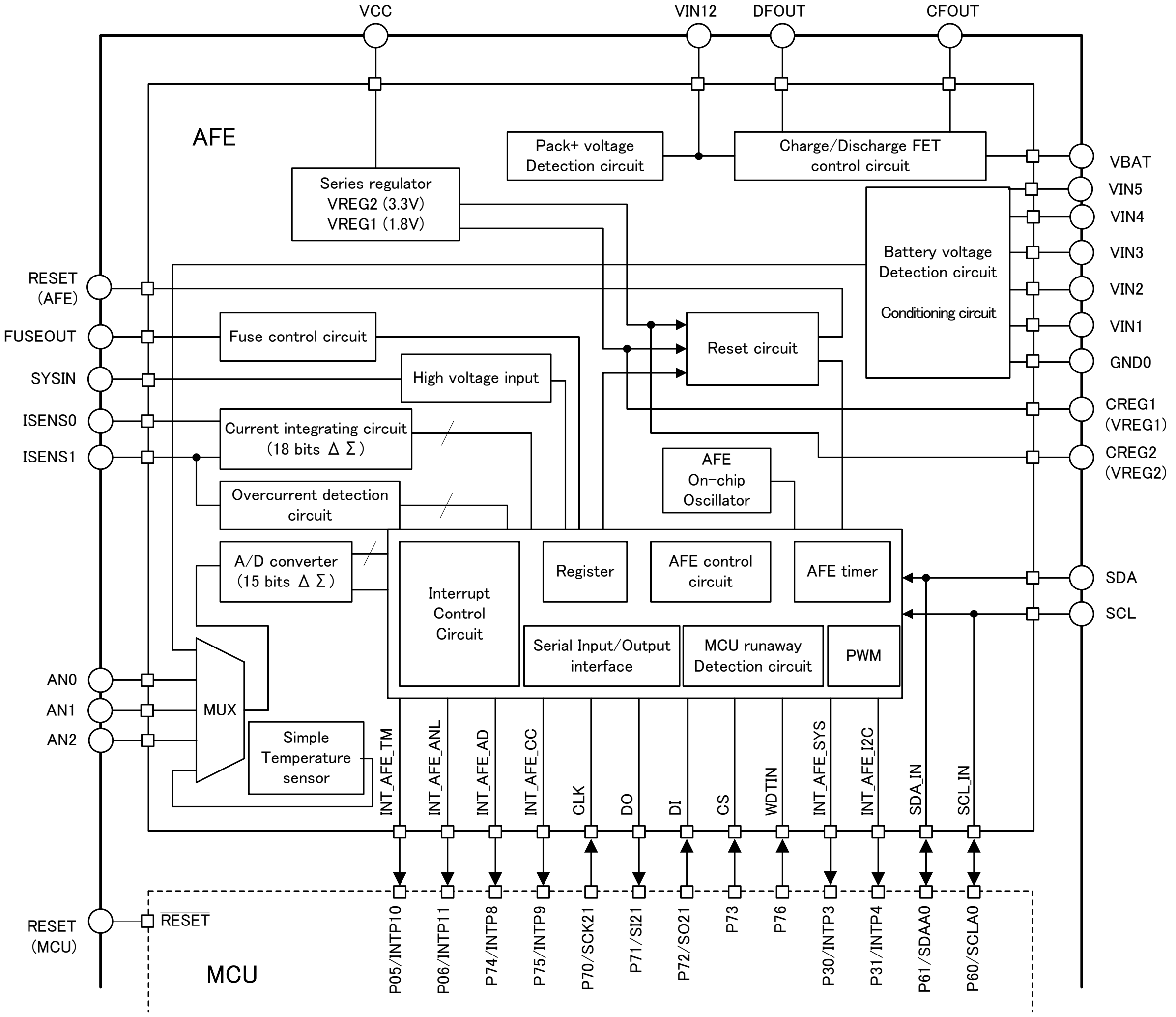
**Caution The example peripheral circuit does not guarantee proper operation. Please perform sufficient evaluation using the actual application to determine the circuits and peripherals.**

## 5.3 MCU block diagram



Notes 1. P30,P31,P70 to P76 are connected to AFE chip in the package.And do not connected to any pin.
2. P60/SDAA0 is connected to SDA pin and P61/SCLA0 is connected to SCL pin respectively.
3. Each interrupt request of AFE are assigned P05/INTP10,P06/INTP11. To use external interrupt function of P05,P06(INTP10,INTP11),it set the PIOR01 bit in the PIOR0 register to 1 and it's enabled peripheral I/O re-direction function. When setting the PIOR01 bit to 1,P16,P17 can be used as UART function(RxD0,TxD0)

## 5.4 AFE block diagram



# 6. Application Guideline

## 6.1 Typical Application Specification

A typical specification example of Li-ion battery management unit as shown below.

Battery cell assembly : 5S1P (5 cells in series and 1 cell in parallel)
Host interface : System Management Bus (SMBus) Specification, version 1.1.
: UART
Primary protection : charge FET and discharge FET
Secondary protection : Fuse blow by FGIC (RAJ240080) or a secondary protection device.

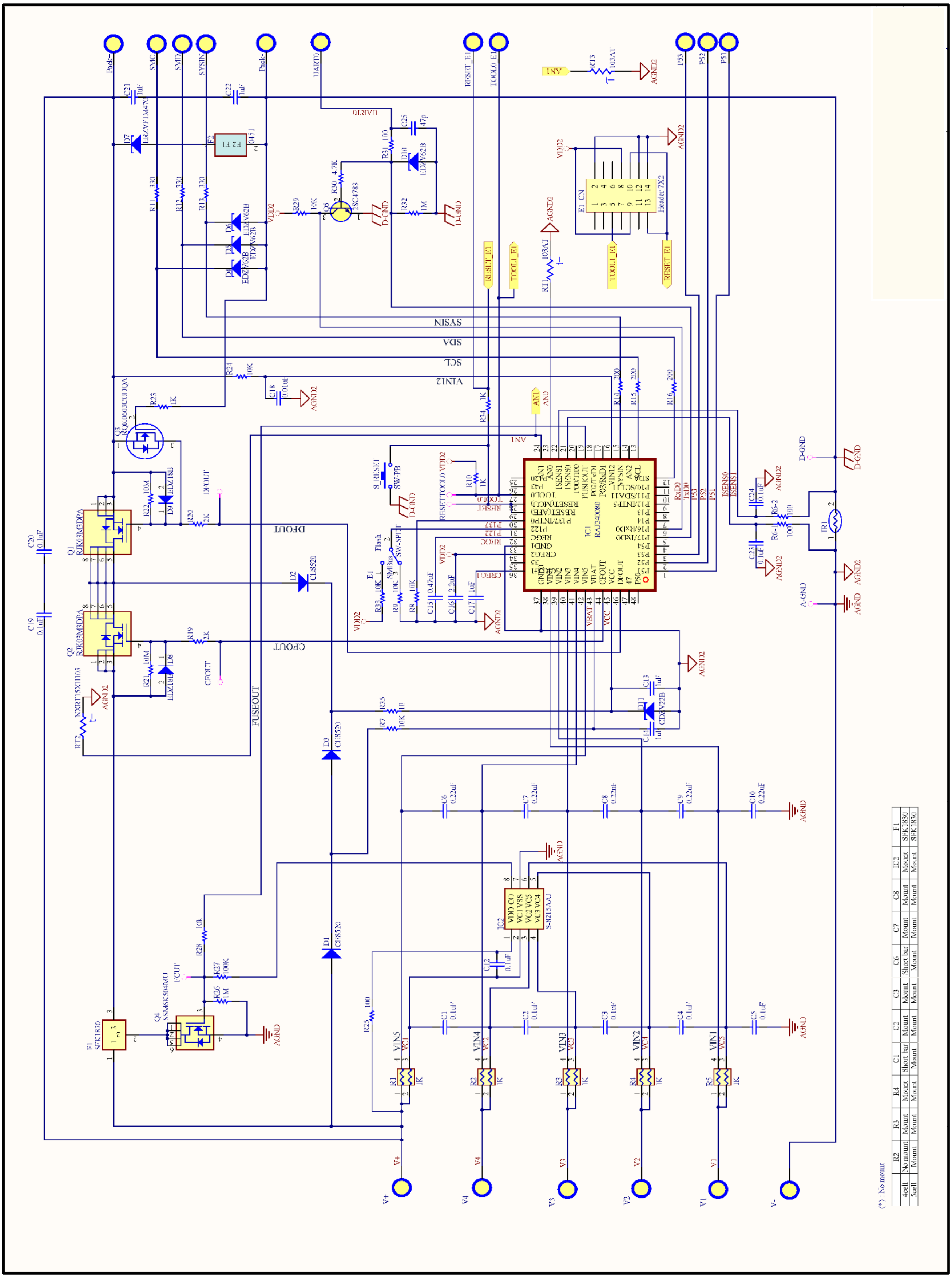
Connector pins:

| | |
|---|---|
| Pack+ | Positive battery pack terminal |
| SMC | SMBus clock |
| SMD | SMBus data |
| UART0 | UART communication port |
| SYSIN | Battery insertion detection |
| Pack- | Negative battery pack terminal |

External reverse charge protection circuit

Battery and charge/discharge MOSFET temperature measurement with three thermistors

## 6.2 Typical Application Circuit



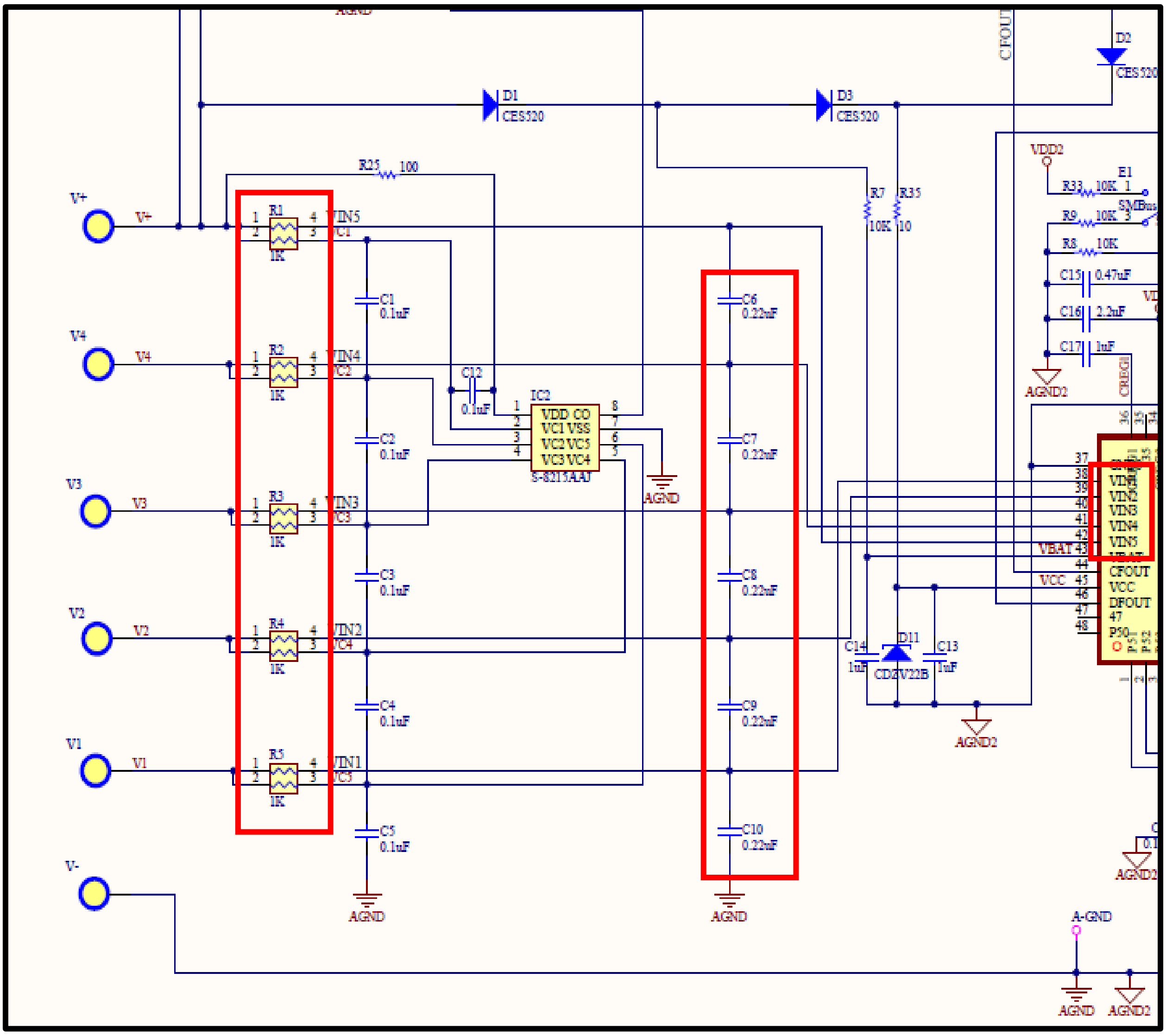
| | R2 | R3 | R4 | C1 | C2 | C3 | C6 | C7 | C8 | IC2 | F1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 4cell | No mount | Mount | Mount | Short bar | Mount | Mount | Short bar | Mount | Mount | Mount | SFK1830 |
| 5cell | Mount | Mount | Mount | Mount | Mount | Mount | Mount | Mount | Mount | Mount | SFK1830 |

**Typical Application Circuit Schematic**

## 6.3 Circuit Design Guideline

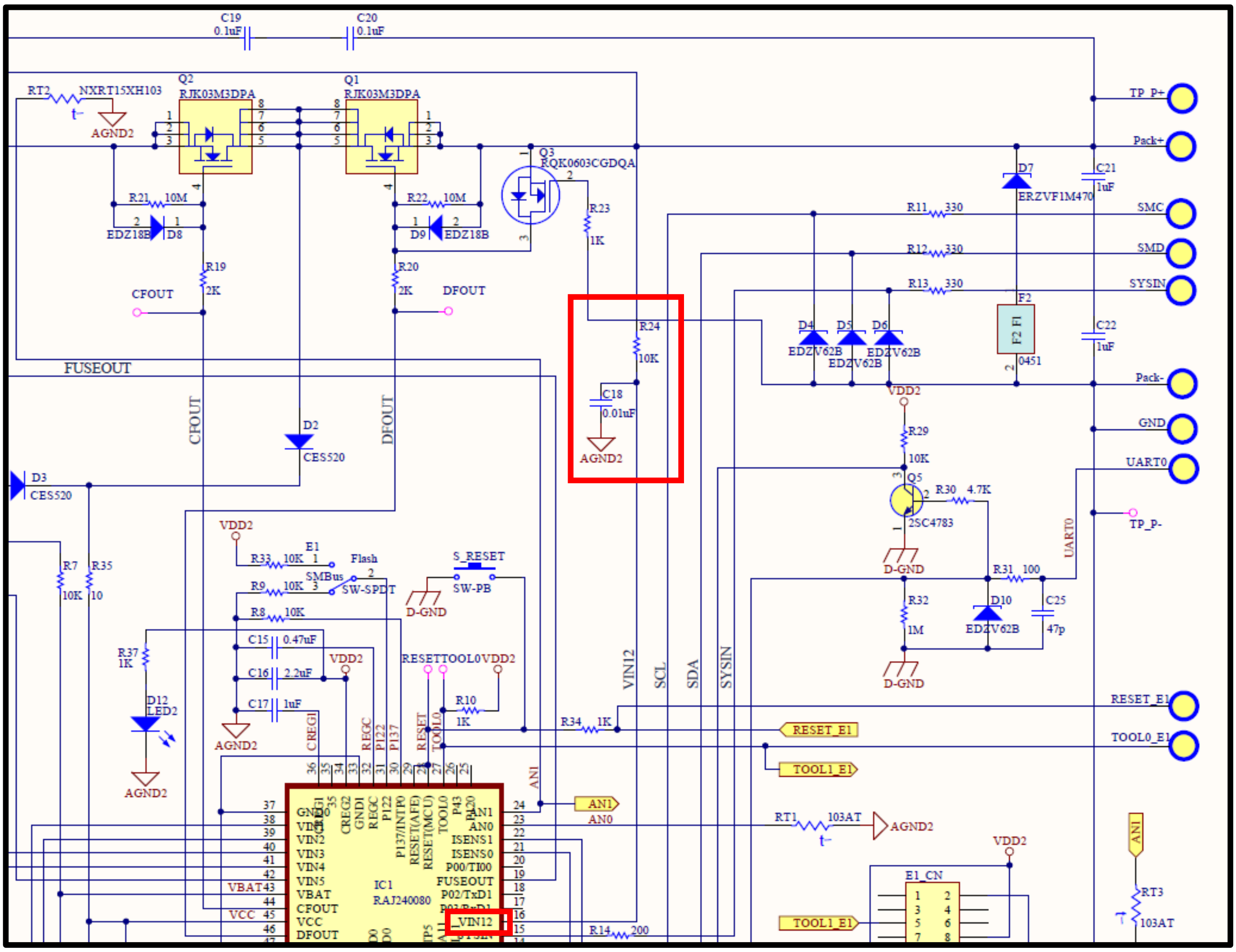
### 6.3.1 Cell voltage monitor circuit

- Place an input filter between FGIC's VIN port and each of the cells independently for FGIC and 2nd protection IC.
- Place resistors valued around 1kΩ and capacitors valued around 0.22uF to VIN1 – VIN5 for surge protection, so cut-off frequency become 0.7 kHz with 1kΩ. It is necessary to calculate the cut-off frequency and use correct resistance and capacitance value based on application.



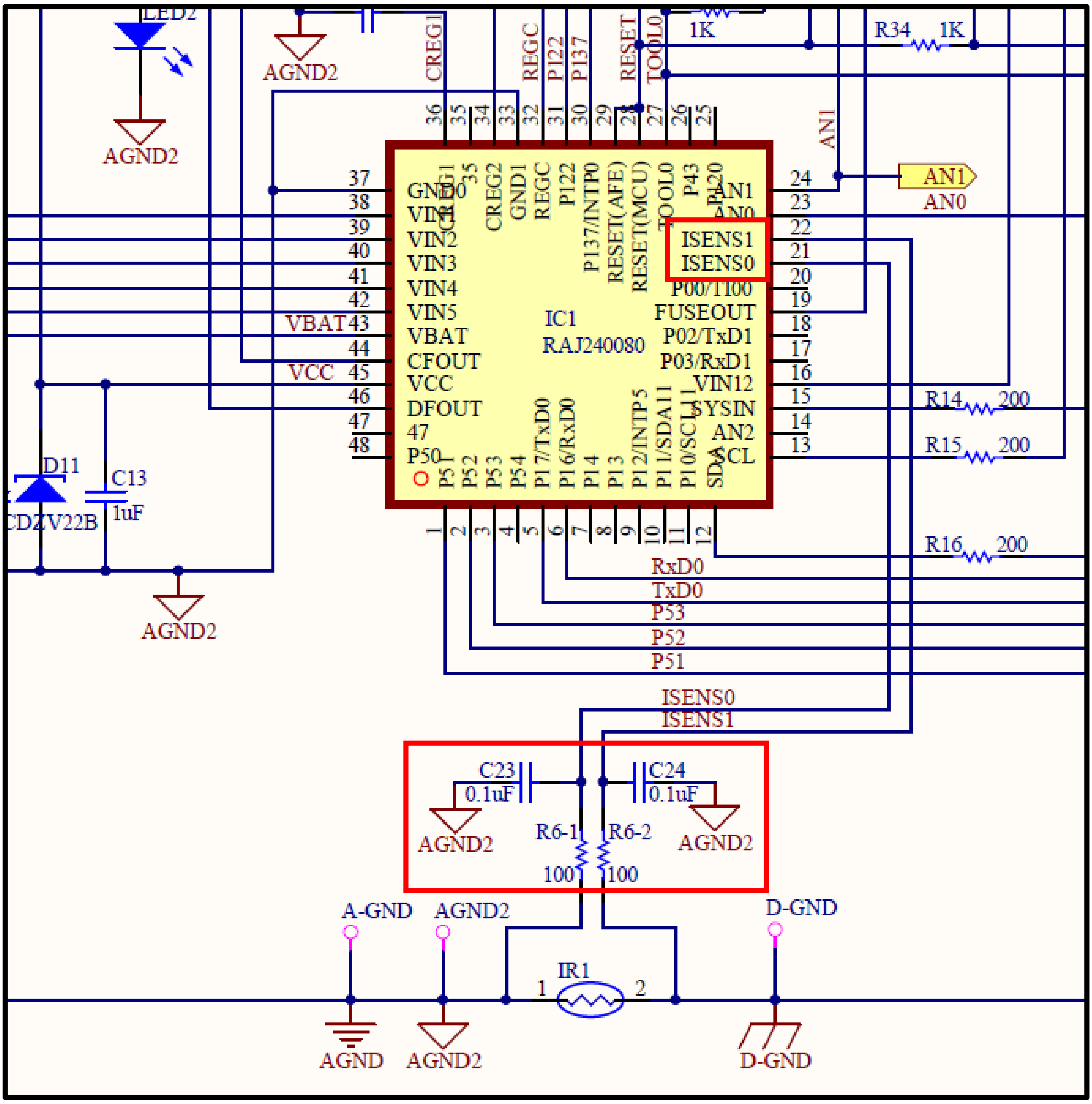
### 6.3.2 Charger connect detection circuit

- VIN12 port is source voltage of DFOUT (D-FET gate control signal). R24 plays a role in limiting the current limit when charger is reverse-charged. 1kΩ is recommended, if it is too large, the D-FET turn off speed will become too slow.
- C18 helps provide stable D-FET boost operation. 0.01μF is recommended. If it is too large, the D-FET turn off speed will becomes too slow.



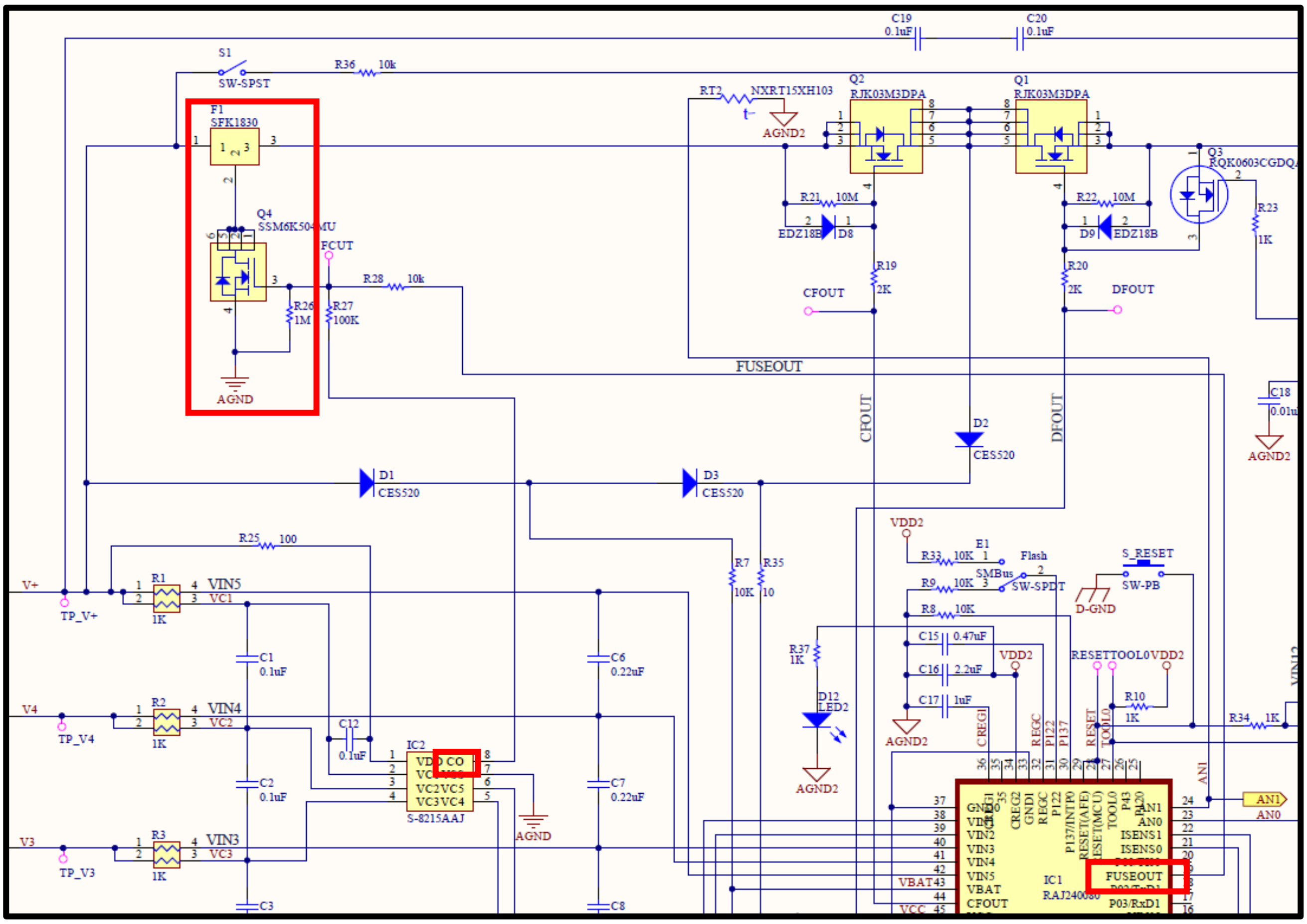
### 6.3.3 Current monitor

- Potential difference on the sense resistor is monitored by current integration circuit.
- Place a Low Pass Filter (100 Ω, 0.1μF) at input stage.
- Sense lines should be shielded if small voltage difference is detected to ensure high accurate current sensing.



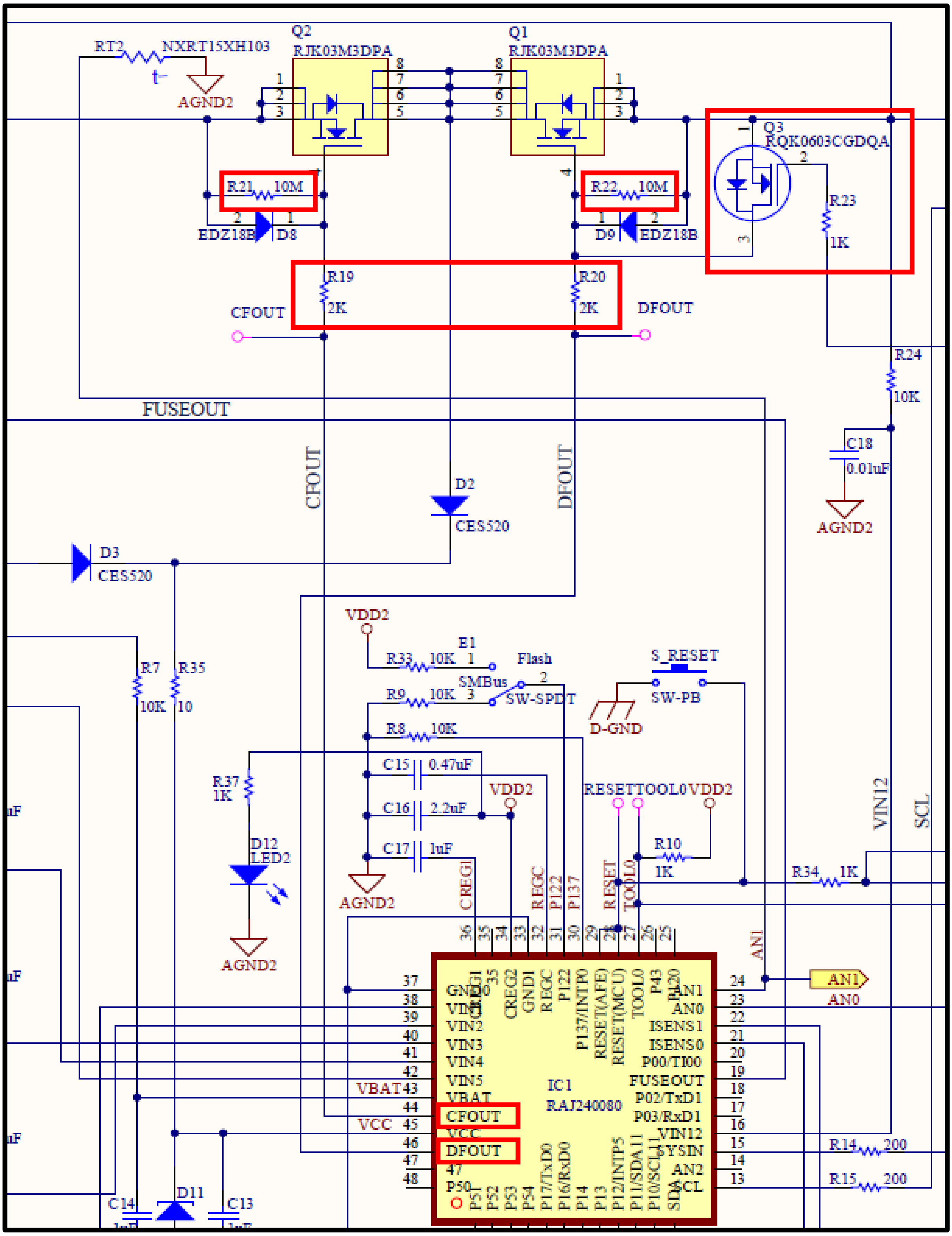
### 6.3.4 Fuse control

- Self-control protector (SCP) is used for fuse in reference circuit.
- The fuse will blow when RAJ240080 drives FUSEOUT pin high to make Q4 ON.
- The fuse will blow when overcurrent exceeds the limit of SCP.
- When 2nd protection IC detects overcharge voltage, CO becomes high to make Q4 ON.



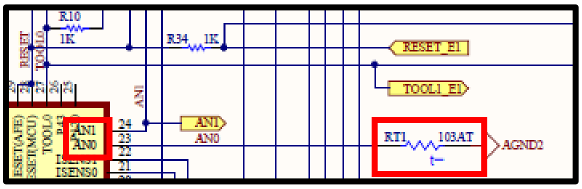
### 6.3.5 C-FET and D-FET control

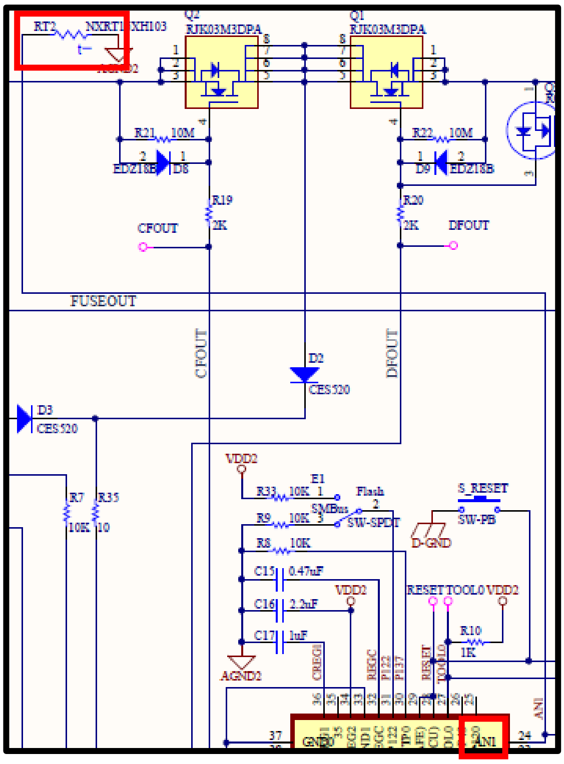
- Q3 is located between gate and source of D-FET(Q1) to make D-FET turn off when charger is reverse connected.
- R23 is for Q3 gate protection. (1kΩ is recommended.)
- R19 and R20 are used as gate protection and C-FET/D-FET noise reduction. (2kΩ is recommended.)
- R21 and R22 are use to fix C-FET/D-FET gate voltage in order to keep stable off state when both FETs are turn off. 10MΩ is recommended to prevent voltage drop.



### 6.3.6 Thermistor

- ADC voltage measurement pins (AN0, AN1, AN2) are assigned for thermistor. AN2 is OPEN in the reference circuit.





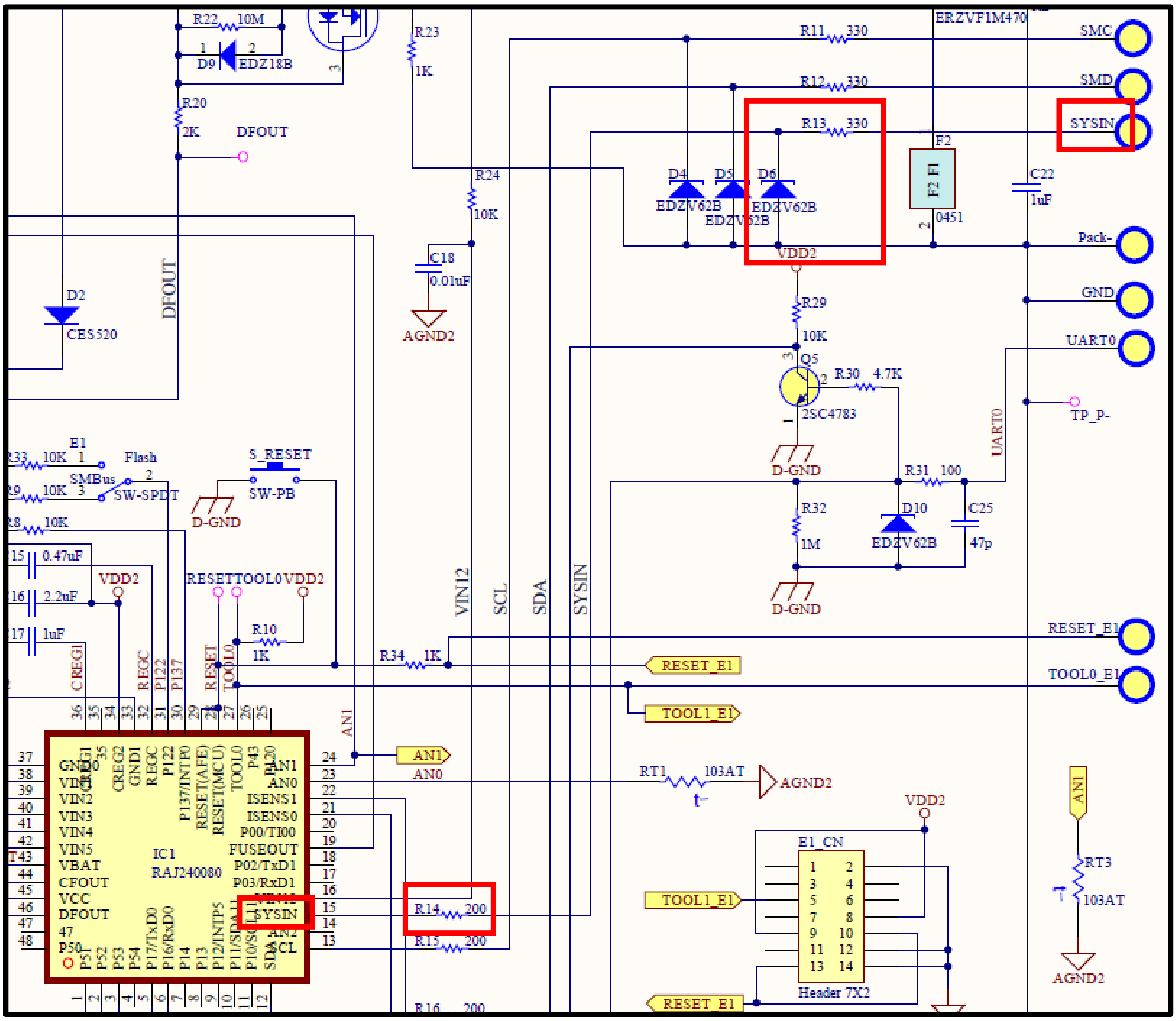
### 6.3.7 System presence

Connect R13 (330 Ω) and R14 (200 Ω) for ESD protection at SYSIN input.

Connect zener diode to protect against short-circuit with Pack+.

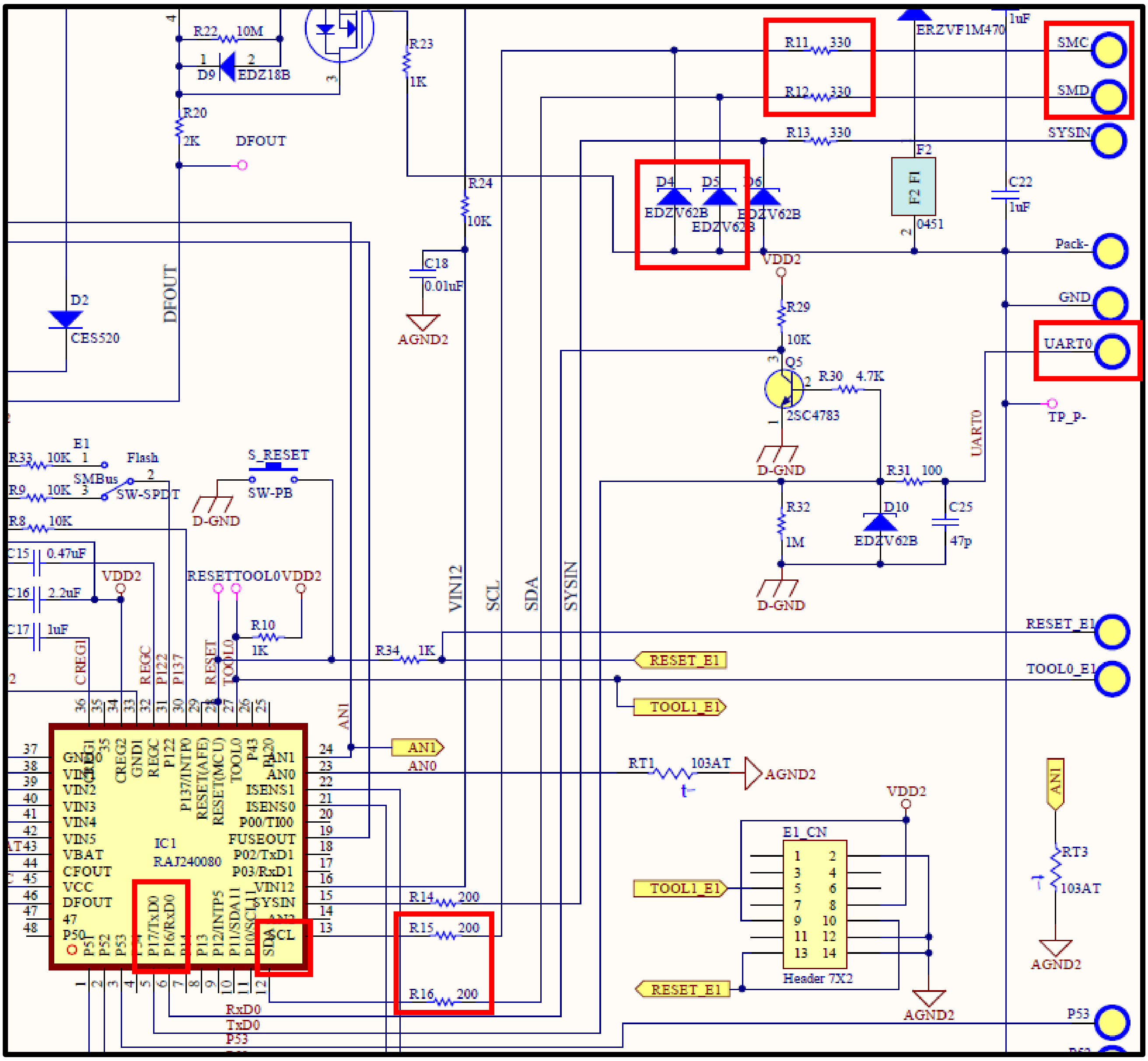
Zener diode must be the one with its zener voltage less than 6.5V, an absolute maximum rating of CREG2.

Recommended: EDZV6.2B (Rohm)



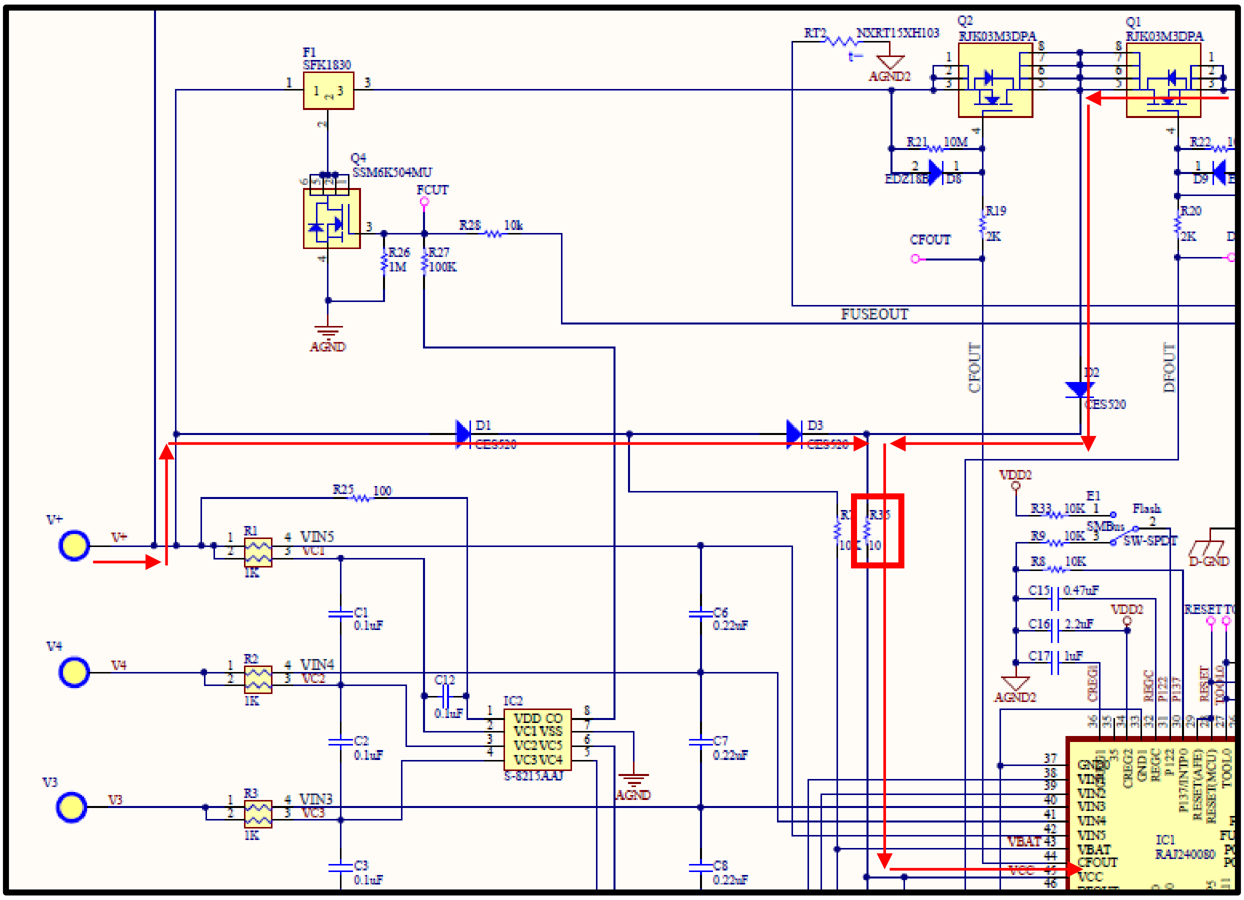
### 6.3.8 Communication line

- RAJ240080 support 2 kinds of communication, SMBus, UART.
- For electrical over stress countermeasure, input 200 Ω, 330 Ω resistance and zener diode are recommended in SMBus communication line. Regarding fast mode, these resistance value should be changed.
- For UART communication, P16 and P17 pins have CREG2 output circuit, therefore RXD/TXD line pull up voltage should be the same as CREG2.



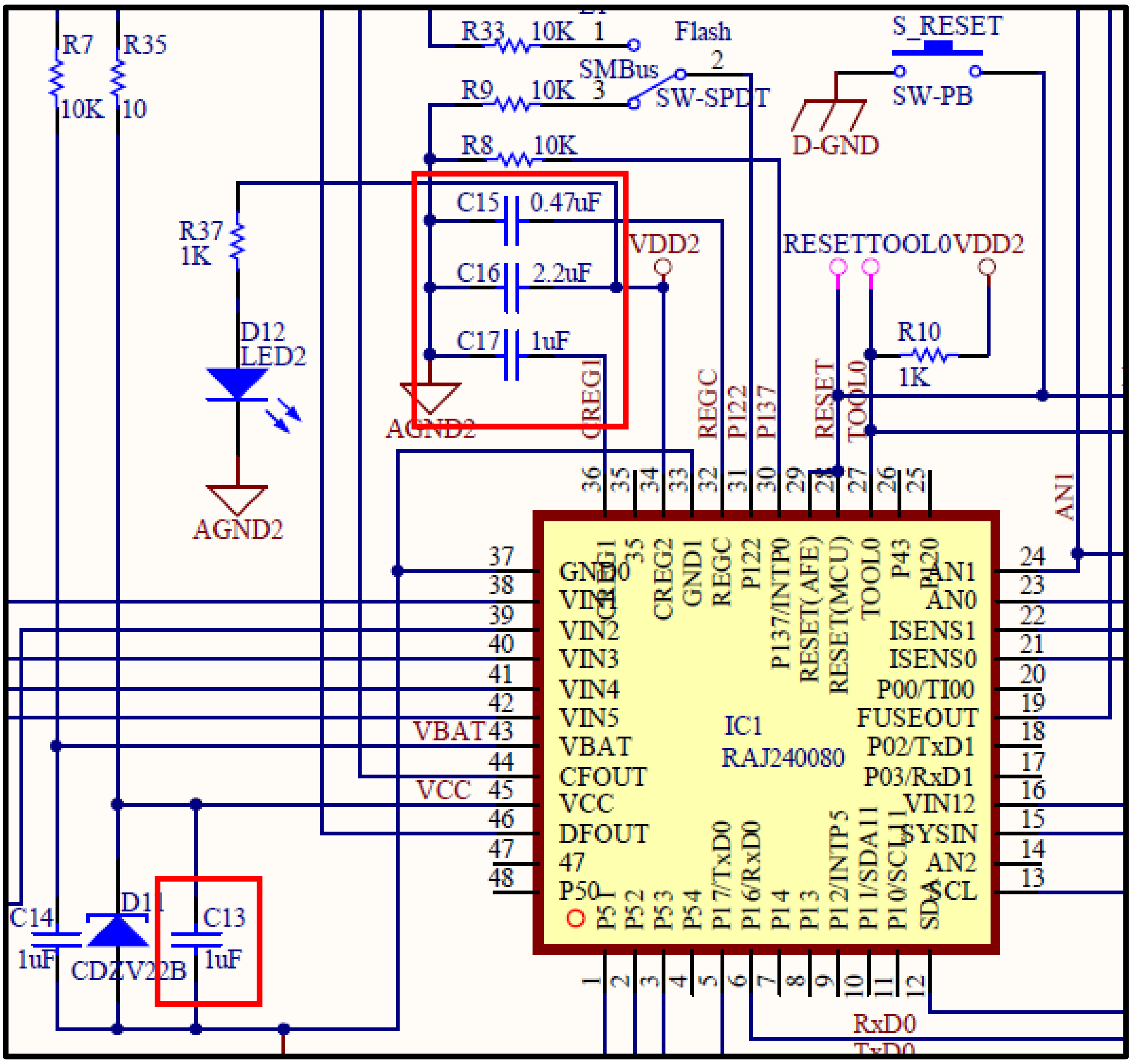
### 6.3.9 Power supply path

- Power is supplied to VCC through the following two paths depending on circumstance.
- Power supplied from battery side when fuse is blown.
- Higher output voltage from battery and charger is used as power supply.
- For protection of the VCC pin, it is recommended to add resistor for current limit.



### 6.3.10 VCC, CREG2, CREG1 and REGC capacitance

- The following decoupling capacitors must be located adjacent to each terminal.
- C13: VCC (1µF is recommended.)
- C16: CREG2 (2.2µF is recommended.)
- C17: CREG1 (1µF is recommended.)
- C15: REGC (0.47µF is recommended.)



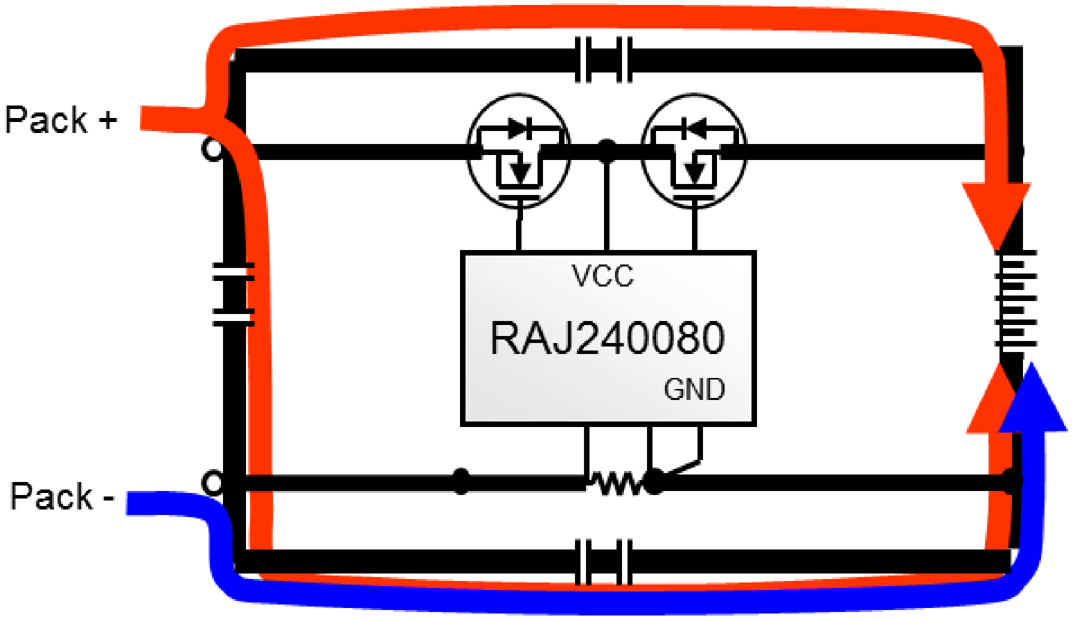
## 6.4 Layout Guidelines

### 6.4.1 Summary

- Large current patterns must be wide and short to minimize voltage drop and heat generation.
- Bypass capacitors must be mounted as close as possible to the device VCC / VBAT and GND pins to prevent erroneous operation due to noise from power supply.
- Capacitors for voltage regulators must be located close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- FGIC (RAJ240080) must be located away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.

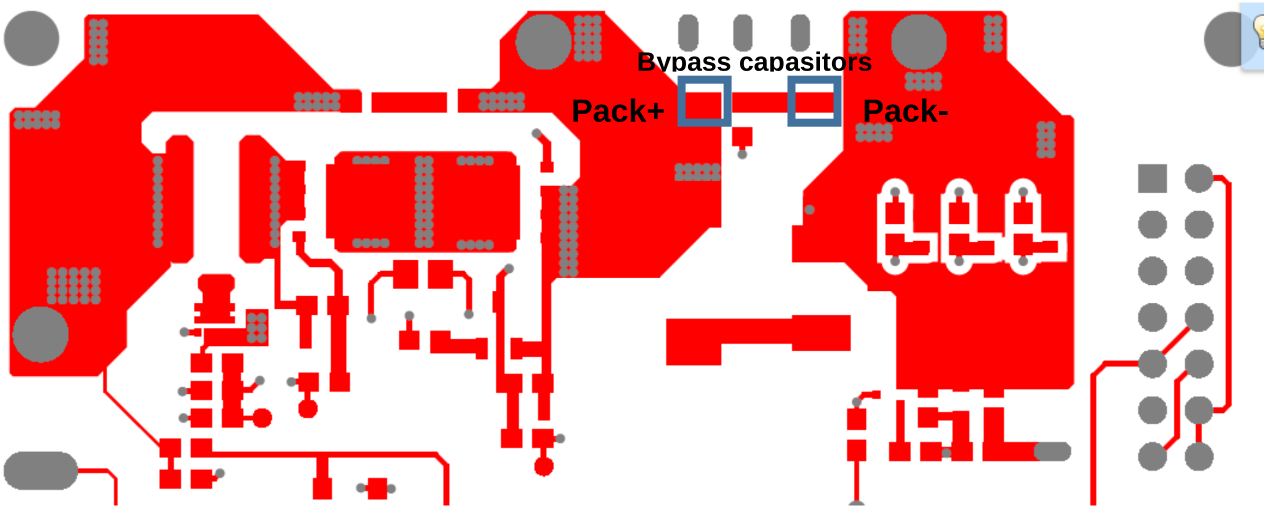
### 6.4.2 ESD protections on each terminal (basic policy)

- ESD on Pack+ terminal must be discharged to the top side of the cell or to Pack- terminal through a capacitor.
- ESD on Pack- terminal must be discharged to the GND side of the cell.
- ESD on communication terminals and other GPIOs must be discharged to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- must be discharged to the battery cells so that it will not interfere with FGIC functions and measurements.



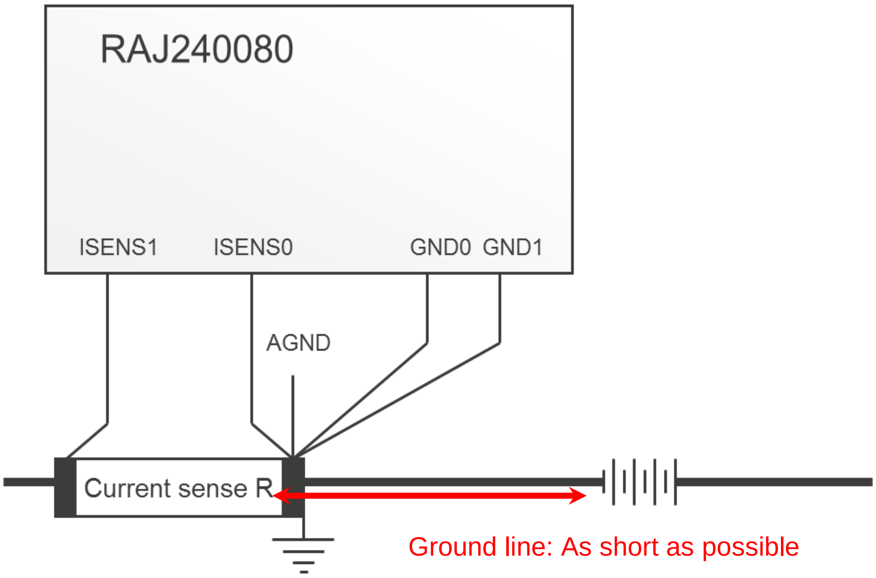
### 6.4.3 Pack+, Pack- (Noise protection element)

- A bypass capacitor must be placed between Pack+ and Pack-. (Countermeasure against ESD)
- A bypass capacitor must be located adjacent to Pack+, Pack-. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don’t use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)
- For the terminal protection against noise and overvoltage, It is recommended that it carries varistor (D7) or TVS diode.
- It is recommended to add Fuse to prevent short circuit.(F2)
- C21, C22, D7, F2 must be placed as short as possible between Pack + and Pack-. However, be careful not to narrow the distance between Pack + and Pack-.



### 6.4.4 GND connection

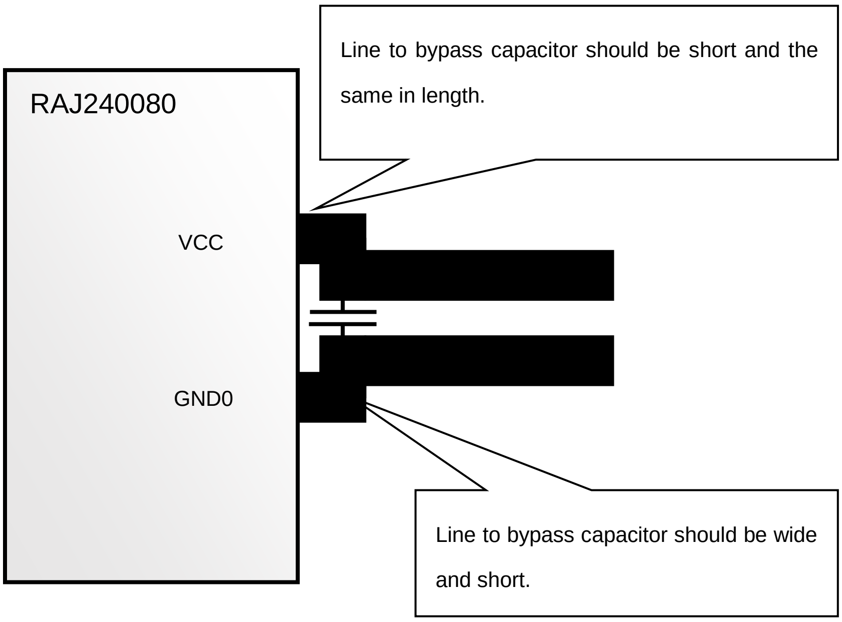
- AGND and AGND2 of RAJ240080 must be connected to the one point of current detection resistor of the cell side by the pattern with an adequate width. (Prevent potential variation by large current.)
- The patterns between AGND and AGND2 must not be divided. (Keeping the GND potential of MCU and AFE equal)
- The lines from cell GND to current sensing resistor must be wide and as short as possible to avoid potential difference generated between cell GND and RAJ240080 when current flows.



### 6.4.5 Bypass capacitor between VCC and GND0

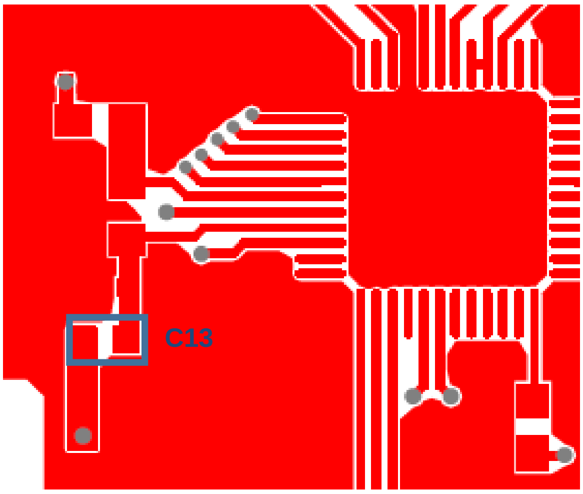
- The patterns between VCC pin and GND1 pin, a bypass capacitor is connected and the path must be as short as possible and of equal length . (Countermeasure for ESD)

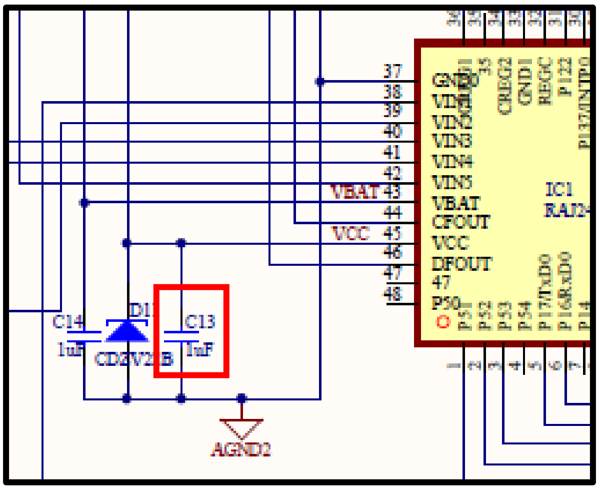
  FGIC and bypass capacitors must be placed on the same side of PCB without any through-hole.
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)



Line to bypass capacitor should be short and the same in length.

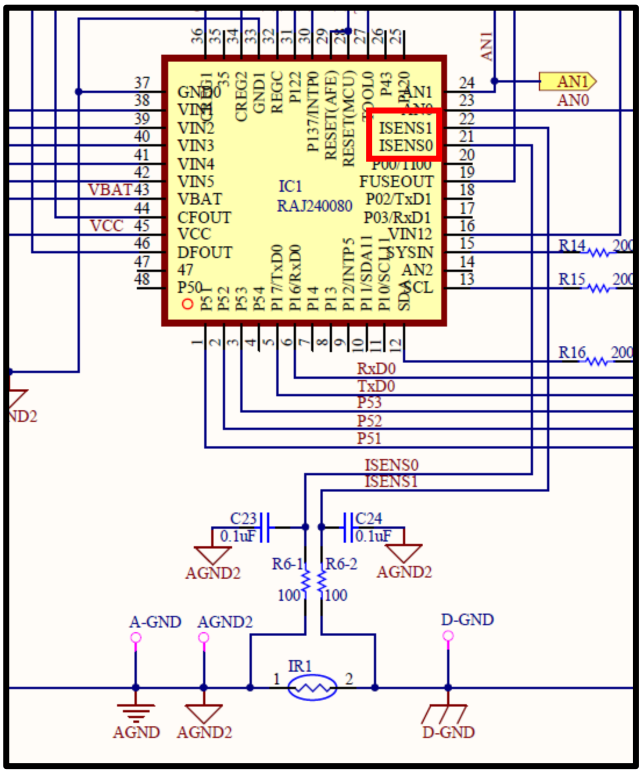
Line to bypass capacitor should be wide and short.

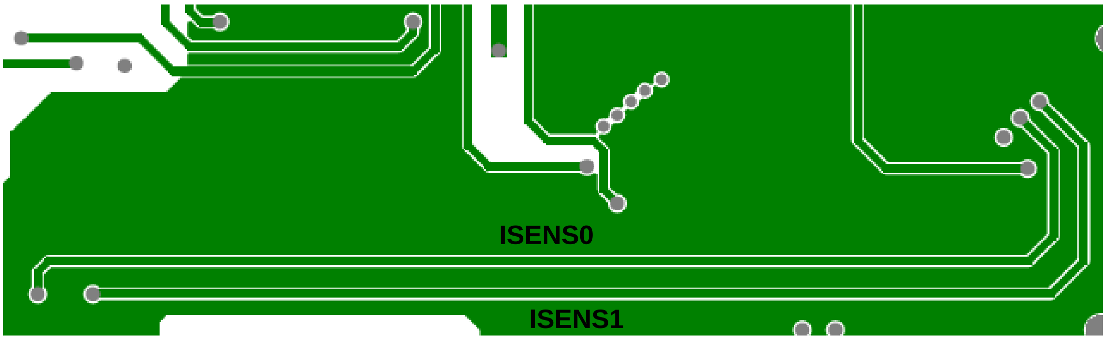




### 6.4.6 Current Monitor (ISENS0, ISENS1)

- Two lines from current sense resistor to ISENS0, ISENS1 must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise)
- LPF (100 ohm and 0.1 uF) and a shield pattern should be placed to ISENS0/1 lines. (Countermeasure against noise)
- There must be no unnecessary divergence between current sense resistors to ISENS0 and ISENS1. (Incoming noise from the pattern unnecessarily divergence.)
- Capacitors connected to shielding pattern are recommended to be located adjacent to RAJ240080. (Countermeasure against noise)





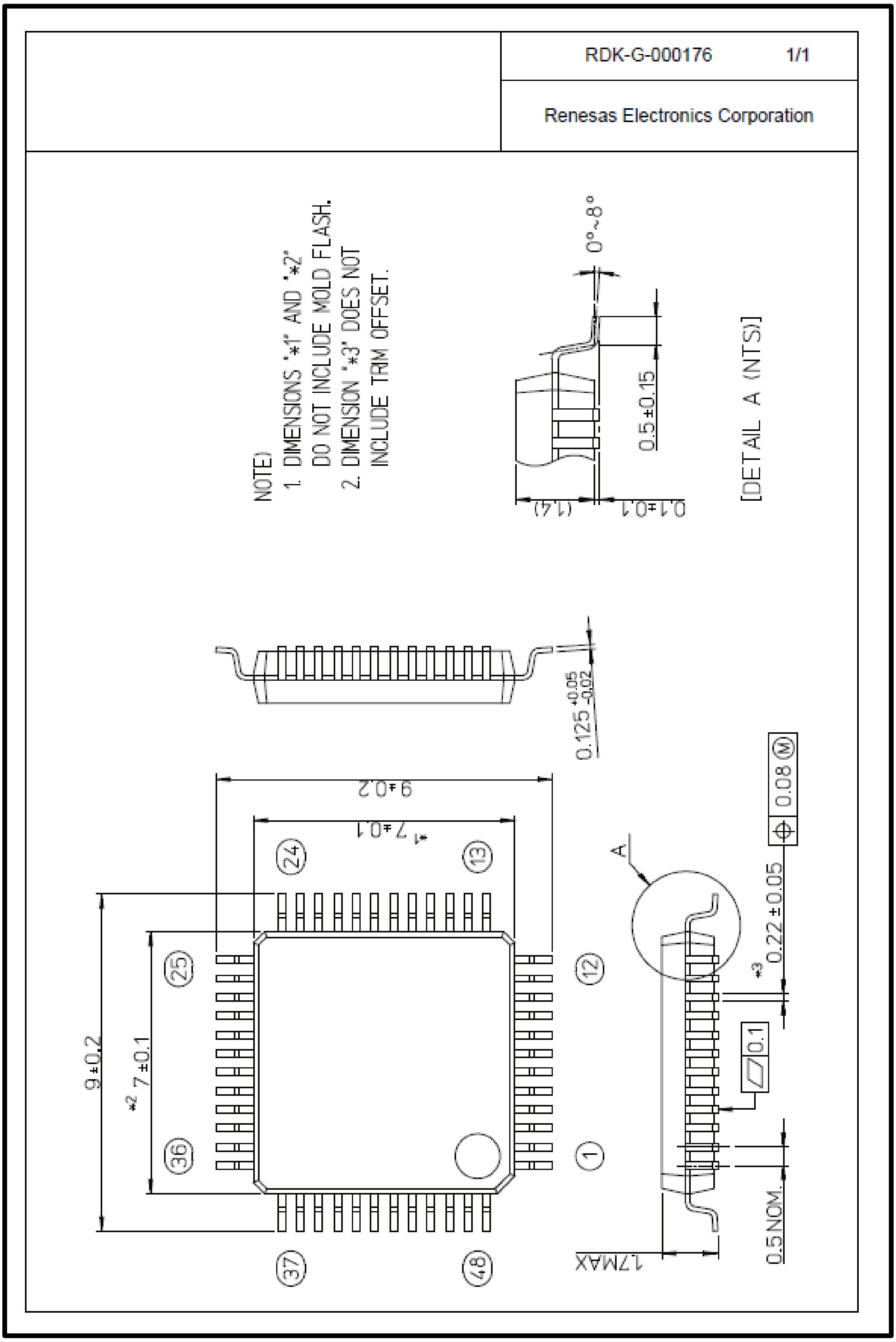
### 6.4.7 Communication line (SMBus)

- SMBus lines must be equipped with zener diodes. And it is necessary to mount resistors on the side of FGIC and pack connecter. (Zener diode and the resistor on the side of connector are for surge countermeasures, the resistor on the side of FGIC for noise countermeasure.)
- The resistor on the side of the FGIC must be located as close to the FGIC as possible

### 6.4.8 Unused Pins

- Unused pins are recommended to be connected to GND via resistors as ESD countermeasure. (Setting low output by software prevents the terminal from becoming indefinite).

# 7. PACKAGE DRAWINGS



**Caution** Package outline is tentative version. All parameters are expressed in milimator.

# REVISION HISTORY

| Rev. | Date | Page | Description |
|---|---|---|---|
| 1.00 | Dec. 27, 2017 | | First Version |

# General cautions for Handling Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on Processing during Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate undetermined and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states state of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for possible future expansion of functions only. Do not access these addresses; the correct operation of LSI will not guaranteed if they are accessed.
4. Clock Signals

   After applying a reset, the reset line will only be released after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, system-evaluation test needs to be implemented for the given product.

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(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.3.0-1 November 2016)

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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