RC32012A

FemtoClock Jitter Attenuator and Clock Generator

The RC32012A is a fully integrated, low-power, high-performance jitter attenuator and clock generator. The device supports JEDEC JESD204B/C for converter synchronization and SyncE for network-based synchronization.

The RC32012A is ideal for providing reference clocks for high-speed serial links up to 28Gbps Ethernet in modular switch line cards and fabric cards in data center equipment, and for clocking data converters in small cell wireless equipment. The device is a member of Renesas' high-performance FemtoClock family and radio clock family.

Applications

- Switches / Routers
- Jitter attenuation for 10 / 25 / 40 / 100 / 200 / 400 Gbps Ethernet PHYs in Switch Line Cards
- Clock generation for 10 /25 / 40 / 100 / 200 / 400 Gbps Ethernet PHYs in Switch Fabric Cards
- Small Cell for 4.5G and 5G
- Medical Imaging
- Professional Audio and Video

Product Options

- 10 × 10 × 0.9 mm 72-QFN package
- 12 differential or 24 single-ended outputs

Features

- Can be configured as clock generator or jitter attenuator/synchronizer
- Low power, less than 1.2W typical
- Low jitter, less than 100 fs-RMS
- Compliant with ITU-T G.8262 and G.8262.1 option 1 and 2 for synchronous Ethernet Equipment Clock (EEC/eEEC) without degrading output jitter
- PCIe Gen 1-6 CC, SRIS and SRNS support
- Jitter attenuation with programmable loop bandwidth from 0.1Hz to 12kHz
- Up to four fractional output dividers and 12 integer output dividers
  - Each fractional output divider can be slaved with DPLL or SYS-DPLL or free-run locked to APLL
- DPLL can be configured as DCO and each fractional output divider can be configured as NCO or DCO
- Combo bus allows frequency sharing between DPLL, System DPLL, and each of the four fractional output dividers
- LVCMOS, LVPECL, LVDS, HCSL, CML, SSTL, HSTL output modes supported with programmable output swing and common mode voltage
- JESD204B/C support on differential or single ended outputs with DC-coupling or AC-coupling
- Up to seven single-ended or two differential clock inputs, one crystal/XO input, and one XO/TCXO/OCXO input
- Up to nine GPIO pins programmable to device select or system monitor options
- Supports 1MHz I^2C, 400kHz SMBus, or 50MHz SPI serial port
- Internal non-volatile memory (up to 16 different configurations), or external serial I^2C EEPROM provide default device settings on power-up.
- 2.5V and 3.3V core and 1.8V, 2.5V, and 3.3V output operation
- -40° to +85°C industrial temperature operation

Contents

1. Overview

1.1 Block Diagram

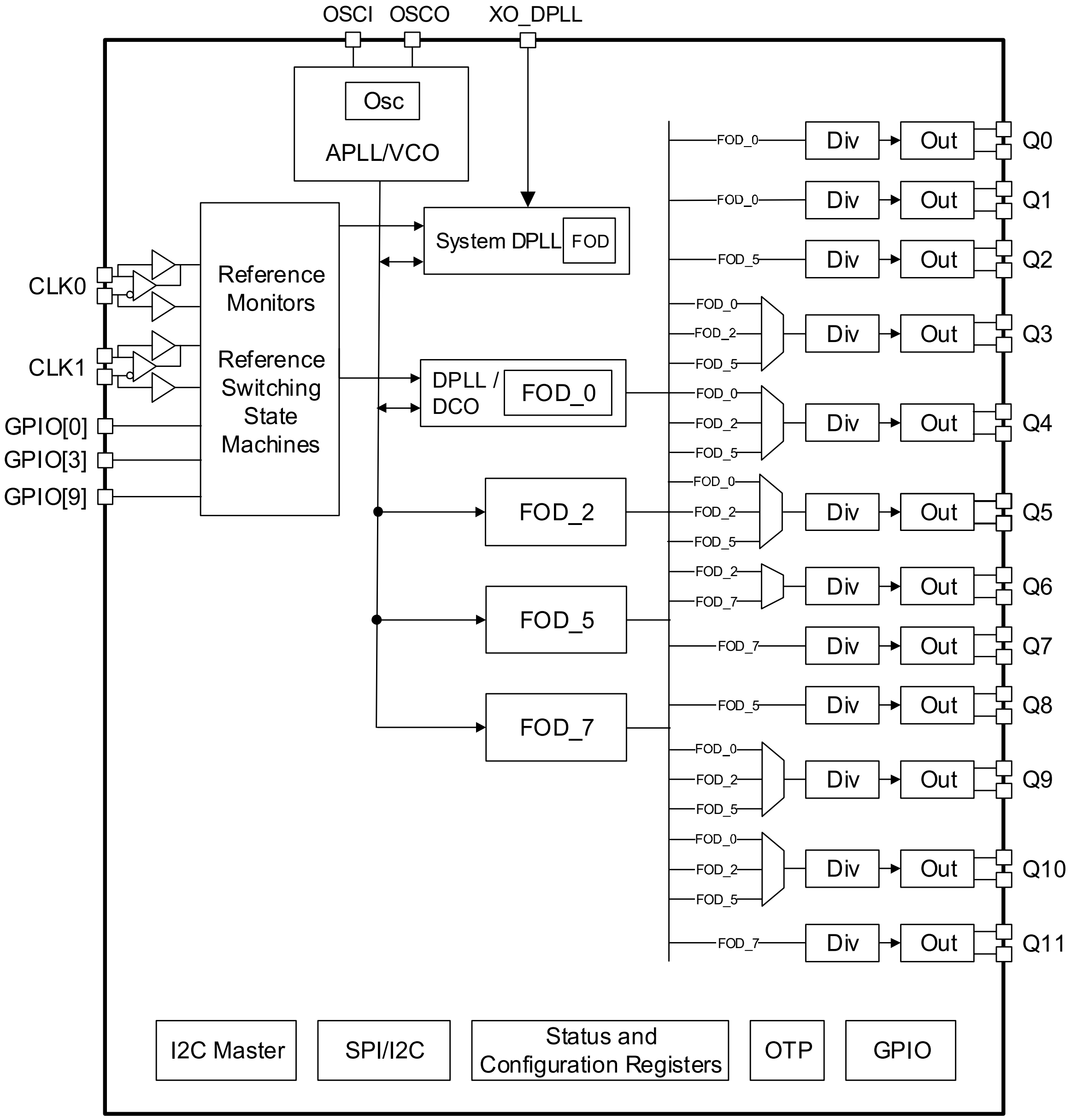


Figure 1. Block Diagram

1.2 Typical Application

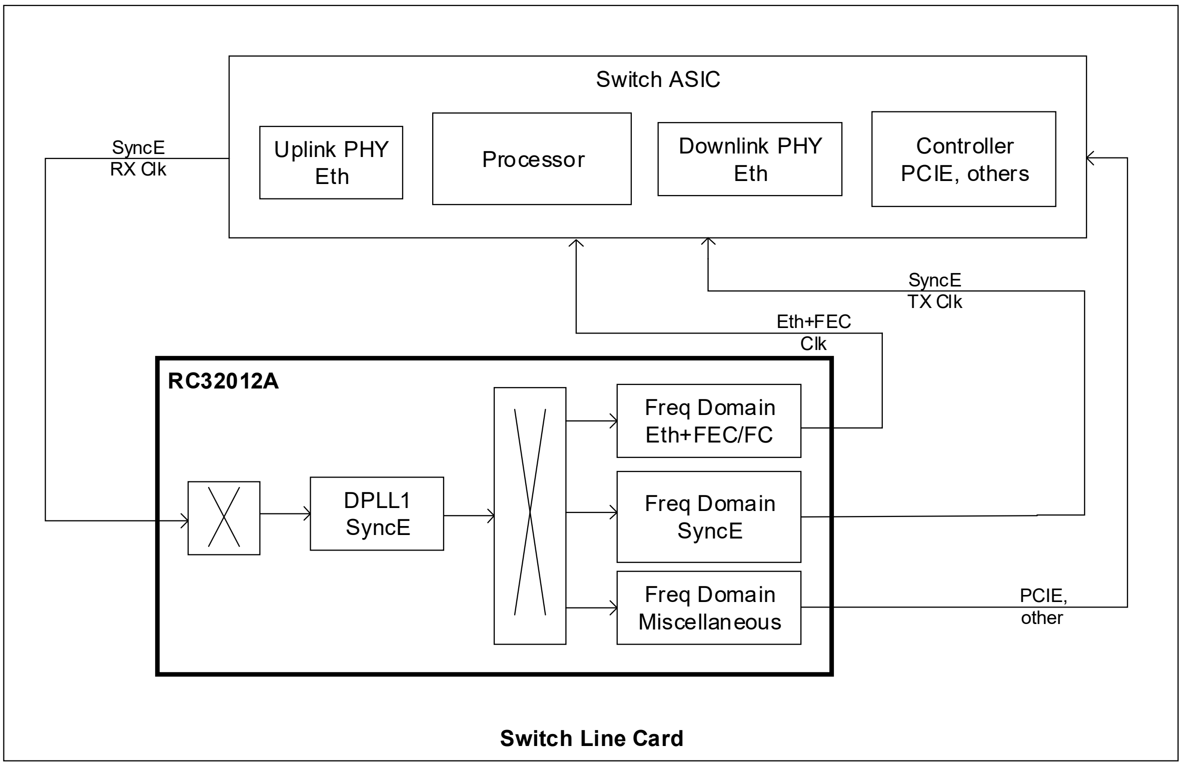


Figure 2. Switch Line Card Use Case

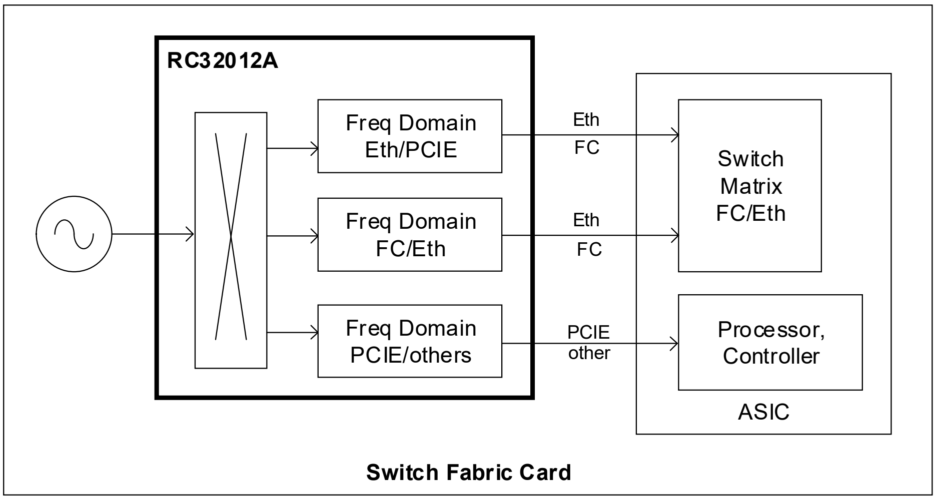
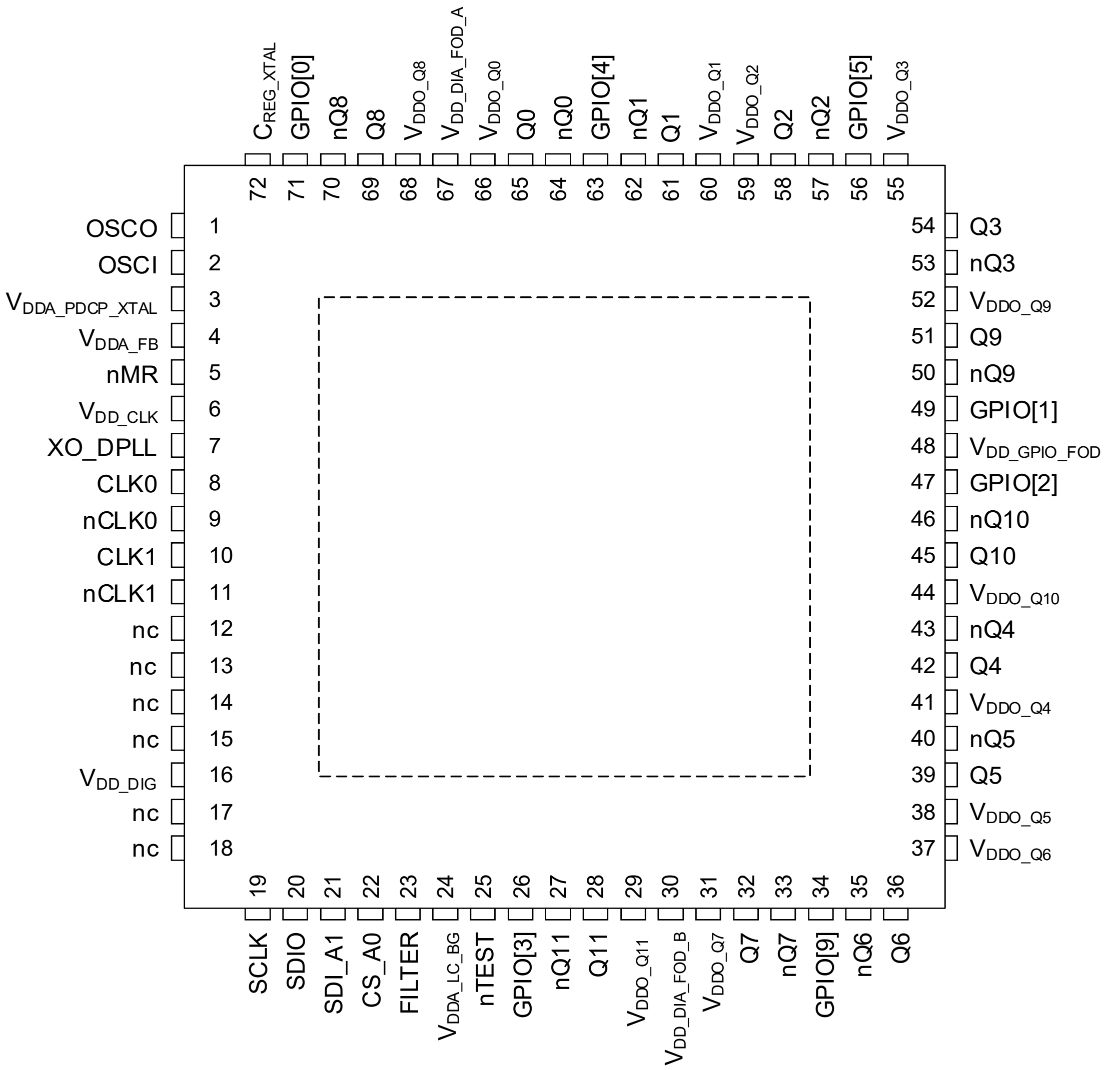


Figure 3. Switch Fabric Card Use Case

2. Pin Information

2.1 Pin Assignments[1]



2.2 Pin Descriptions

Table 1. Pin Descriptions [1]

Number	Name	Type		Description
1	OSCO	Output		Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to the OSCI pin, this pin should be left unconnected.
2	OSCI	Input		Crystal Input. Accepts a reference from a clock oscillator or a fundamental mode parallel-resonant crystal.
3	$V_{DDA\_PDCP\_XTAL}$	Power		Analog power supply voltage for System Analog PLL's phase detector and charge pump, as well as the oscillator circuit associated with OSCI / OSCO pins. 2.5V or 3.3V operation supported.[2]

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1. Indexed signals (e.g., GPIO[5]) are not necessarily numbered sequentially (i.e., some indexes may be skipped). This is to maintain software compatibility with other members of the family of devices.

Table 1. Pin Descriptions [1] (Cont.)

Number	Name	Type		Description
4	V_{DDA_FB}	Power		Analog power supply voltage for System Analog PLL's feedback divider, 1.8V required.
5	nMR	Input	Pull-up	Master Reset input (see Power-Up, Configuration and Serial Interfaces).
6	V_{DD_CLK}	Power		Power supply for input clock buffers and dividers. Supports 1.8V, 2.5V, or 3.3V as appropriate for the input clock swing.
7	XO_DPLL	Input		Single-ended crystal oscillator input for System Digital PLL.
8	CLK0	Input	Pull-down	Positive input for differential input Clock 0 or single-ended input for Clock 0.
9	nCLK0	Input	Pull-up	Negative input for differential input Clock 0 or single-ended input for Clock 8.
10	CLK1	Input	Pull-down	Positive input for differential input Clock 1 or single-ended input for Clock 1.
11	nCLK1	Input	Pull-up	Negative input for differential input Clock 1 or single-ended input for Clock 9.
12	nc	Unused		No connect.
13	nc	Unused		No connect.
14	nc	Unused		No connect.
15	nc	Unused		No connect.
16	VDD_DIG	Power		Power supply for digital logic. 1.2V or 1.8V supported.
17	nc	Unused		No connect.
18	nc	Unused		No connect.
19	SCLK	I/O	Pull-up	Main serial port clock input. Used in both SPI and I^2C modes as the clock. This pin can also be used when device boots as I^2C Clock Output for I^2C Master Operation. External pull-up recommended in I^2C mode.
20	SDIO	I/O	Pull-up	Main serial port bi-directional data pin. Used as a bi-directional data pin in I^2C and 3-wire SPI modes. Used as Serial Data Output pin in 4-wire SPI mode. This pin can also be used when device boots as I^2C Bi-directional Data for I^2C Master Operation. External pull-up recommended in I^2C mode.
21	SDI_A1	Input	Pull-up	Main serial port input. Used as Serial Data In in 4-wire SPI mode and optionally as an Address Bit 1 select input in I^2C mode. Unused in 3-wire SPI mode.
22	CS_A0	Input	Pull-up	Main serial port input. Used as a Chip Select input in SPI mode and optionally as an Address Bit 0 select input in I^2C mode.
23	FILTER	Analog		Reference capacitor for System Analog PLL Loop Filter. Requires a 2.2nF capacitor to ground.
24	$V_{DDA\_LC\_BG}$	Power		Analog power supply voltage for System Analog PLL's LC Resonator and bandgap regulator, 3.3V or 2.5V supported.[2]
25	nTEST	Input	Pull-up	Test Mode enable pin. Must be high for normal operation
26	GPIO[3]	I/O	Pull-up [3]	General Purpose Input / Output 3.
27	nQ11	Output		Q11 clock negative output.
28	Q11	Output		Q11 clock positive output.

Table 1. Pin Descriptions [1] (Cont.)

Number	Name	Type		Description
29	V_{DDO_Q11}	Power		Power supply for Q11/nQ11 output buffers.[4]
30	$V_{DD\_DIA\_FOD\_B}$	Power		Power Supply for FOD control logic for FOD_2 and FOD_7. Also powers FOD_2 and FOD_7. 1.8V supply required.
31	V_{DDO_Q7}	Power		Power supply for Q7/nQ7 output buffers.[4]
32	Q7	Output		Q7 clock positive output.
33	nQ7	Output		Q7 clock negative output.
34	GPIO[9]	I/O	Pull-up [3]	General Purpose Input / Output 9.
35	nQ6	Output		Q6 clock negative output.
36	Q6	Output		Q6 clock positive output.
37	V_{DDO_Q6}	Power		Power supply for Q6/nQ6 output buffers.[4]
38	V_{DDO_Q5}	Power		Power supply for Q5/nQ5 output buffers.[4]
39	Q5	Output		Q5 clock positive output.
40	nQ5	Output		Q5 clock negative output.
41	V_{DDO_Q4}	Power		Power supply for Q4/nQ4 output buffers.[4]
42	Q4	Output		Q4 clock positive output.
43	nQ4	Output		Q4 clock negative output.
44	V_{DDO_Q10}	Power		Power supply for Q10/nQ10 output buffers.[4]
45	Q10	Output		Q10 clock positive output.
46	nQ10	Output		Q10 clock negative output.
47	GPIO[2]	I/O	Pull-up [3]	General Purpose Input / Output 2.
48	$V_{DD\_GPIO\_FOD}$	Power		Combined Power Supply input for all the digital pins, including GPIO pins and serial ports pins as well as FOD_5. Only 1.8V supported.
49	GPIO[1]	I/O	Pull-up [3]	General Purpose Input / Output 1.
50	nQ9	Output		Q9 clock negative output.
51	Q9	Output		Q9 clock positive output.
52	V_{DDO_Q9}	Power		Power supply for Q9/nQ9 output buffers.[4]
53	nQ3	Output		Q3 clock negative output.
54	Q3	Output		Q3 clock positive output.
55	V_{DDO_Q3}	Power		Power supply for Q3/nQ3 output buffers.[4]
56	GPIO[5]	I/O	Pull-up [3]	General Purpose Input / Output 5.
57	nQ2	Output		Q2 clock negative output.
58	Q2	Output		Q2 clock positive output.
59	V_{DDO_Q2}	Power		Power supply for Q2/nQ2 output buffers.[4]
60	V_{DDO_Q1}	Power		Power supply for Q1/nQ1 output buffers.[4]
61	Q1	Output		Q1 clock positive output.
62	nQ1	Output		Q1 clock negative output.
63	GPIO[4]	I/O	Pull-up [3]	General Purpose Input / Output 4.
64	nQ0	Output		Q0 clock negative output.
65	Q0	Output		Q0 clock positive output.

Table 1. Pin Descriptions [1] (Cont.)

Number	Name	Type		Description
66	V_{DDO_Q0}	Power		Power supply for Q0/nQ0 output buffers. [4]
67	$V_{DD\_DIA\_FOD\_A}$	Power		Power supply for FOD control logic for FOD_0 and FOD_5. Also powers FOD_0. 1.8V supply required.
68	V_{DDO_Q8}	Power		Power supply for Q8/nQ8 output buffers. [4]
69	Q8	Output		Q8 clock positive output.
70	nQ8	Output		Q8 clock negative output.
71	GPIO[0]	I/O	Pull-up [3]	General Purpose Input / Output 0.
72	C_{REG_XTAL}	Power		Filter capacitor for voltage regulator for oscillator circuit associated with OSCI / OSCO pins. Requires a 10µF filter capacitor to ground.
ePad	V_{SS}	Power		Device ePad must be connected to Ground.

1. Pull-up and pull-down refer to internal input resistors (see Table 2, Pin Characteristics, for typical values).
2. $V_{DDA\_PDCP\_XTAL}$ and $V_{DDA\_LC\_BG}$ can be driven with either 2.5V or 3.3V, however, both must use the same voltage level. Register programming is required to configure the device for either 2.5V or 3.3V operation. For more information, see the *8A3xxxx Family Programming Guide*.
3. GPIO pins can be configured via EEPROM and/or OTP with a pull-up or a pull-down. Pull-up is the default configuration.
4. For voltages supported, see Clock Outputs.

2.3 Pin Characteristics

Table 2. Pin Characteristics

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance	OSCI, OSCO			9		pF
		All Other pins			2		
R_{PULLUP}	Input Pull-up Resistor	nCLK[1:0]			50		kΩ
$R_{PULLDOWN}$	Input Pull-down Resistor	CLK[1:0]			50		kΩ
C_{PD}	Power Dissipation Capacitance (per output pair)	LVCMOS	V_{DDO_Qx} [1] = 3.465V		9		pF
			V_{DDO_Qx} = 2.625V		8.8		
			V_{DDO_Qx} = 1.89V		8.8		
			V_{DDO_Qx} = 1.575V		9.2		
			V_{DDO_Qx} = 1.26V		8.7		
		Differential	V_{DDO_Qx} = 3.465V		1.4		
			V_{DDO_Qx} = 2.625V		3.5		
			V_{DDO_Qx} = 1.89V		5		
R_{OUT} [2]	Output Impedance	GPIO[9,5:0]	$V_{DD\_GPIO\_FOD}$ = 1.8V		32		Ω
		SDIO, SCLK	$V_{DD\_GPIO\_FOD}$ = 1.8V		38		

1. V_{DDO_Qx} denotes: V_{DDO_Q0}, V_{DDO_Q1}, V_{DDO_Q2}, V_{DDO_Q3}, V_{DDO_Q4}, V_{DDO_Q5}, V_{DDO_Q6}, V_{DDO_Q7}, V_{DDO_Q8}, V_{DDO_Q9}, V_{DDO_Q10}, or V_{DDO_Q11}
2. Output impedance values for the Qx / nQx outputs are provided in Table 26.

3. Specifications

3.1 Abbreviations Used

Many signals will be concatenated for simplicity in the specification tables that follow. Table 3 shows a list of abbreviations used and will be referred to in footnotes for the various other tables.

Table 3. Abbreviated Signal Names and the Detailed Signal Names Referenced by Them

Abbreviation	Signals Referenced by this Abbreviation
V_{DD_CLKx}	V_{DD_CLK}
Input CLK	CLK[1:0], nCLK[1:0]
Output Q	Q[11:0], nQ[11:0]
Status Outputs	GPIO[9,5:0], SDIO
GPIO	GPIO[9,5:0]
V_{DDx}	$V_{DDA\_PDCP\_XTAL}$, V_{DD_CLK}, V_{DDA_FB}, $V_{DDA\_BG\_LC}$, V_{DD_DIG}, $V_{DD\_GPIO\_FOD}$, $V_{DDA\_DIA\_FOD\_A}$, $V_{DDA\_DIA\_FOD\_B}$, V_{DDO_Q0}, V_{DDO_Q1}, V_{DDO_Q2}, V_{DDO_Q3}, V_{DDO_Q4}, V_{DDO_Q5}, V_{DDO_Q6}, V_{DDO_Q7}, V_{DDO_Q8}, V_{DDO_Q9}, V_{DDO_Q10}, V_{DDO_Q11},
V_{DDO_Qx}	V_{DDO_Q0}, V_{DDO_Q1}, V_{DDO_Q2}, V_{DDO_Q3}, V_{DDO_Q4}, V_{DDO_Q5}, V_{DDO_Q6}, V_{DDO_Q7}, V_{DDO_Q8}, V_{DDO_Q9}, V_{DDO_Q10}, V_{DDO_Q11}

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC32012A at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
V_{DDx}[1]	Any voltage supply		-0.5	3.63	V
V_{IN}	Voltage on any input	OSCI [2], OSCO, FILTER, C_{REG_XTAL}	0	2.75	V
		All other inputs	-0.5	3.63	V
I_{IN}	Differential Input Current	Input CLK [1]		±50	mA
I_O	Output Current - Continuous	Output Q [1]		30	mA
		Status Outputs [1]		25	mA
	Output Current - Surge	Output Q		60	mA
		Status Outputs		50	mA
T_{JMAX}	Maximum Junction Temperature			150	°C
T_S	Storage temperature		-65	150	°C
-	ESD - Human Body Model			2000	V
-	ESD - Charged Device Model			1500	V

1. For information on the signals referenced by this abbreviation, see Table 3.
2. This limit only applies to the OSCI input when being over-driven by an external signal. No limit is implied when this is connected directly to a crystal.

3.3 Recommended Operating Conditions

Table 5. Recommended Operating Conditions [1]

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_A	Ambient air temperature	-40		85	°C
T_C	Case temperature [2]	-40		105	°C

1. It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.
2. Measured at solder connection to Printed Circuit Board on any signal, voltage, or ePad.

3.4 Supply Voltage Characteristics

Table 6. Power Supply DC Characteristics[1][2]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{DD_CLK}	Supply Voltage for Input Clock Buffers and Dividers		1.71	[3]	3.465	V
I_{DD_CLKx} [4]	Supply Current for V_{DD_CLKx}	V_{DD_CLKx} = 3.465V, PMOS mode		3		mA
		V_{DD_CLKx} = 3.465V, NMOS mode		6		
		V_{DD_CLKx} = 3.465V, CMOS mode		1.5		
		V_{DD_CLKx} = 2.625V, PMOS mode		2.6		
		V_{DD_CLKx} = 2.625V, NMOS mode		6		
		V_{DD_CLKx} = 2.625V, CMOS mode		1		
		V_{DD_CLKx} = 1.89V, PMOS mode		2.5		
		V_{DD_CLKx} = 1.89V, NMOS mode		5		
		V_{DD_CLKx} = 1.89V, CMOS mode		1		
$V_{DDA\_PDCP\_XTAL}$	Analog Supply Voltage for oscillator and for APLL Phase detector and Charge Pump		2.375	[5]	3.465	V
$I_{DDA\_PDCP\_XTAL}$	Supply Current for $V_{DDA\_PDCP\_XTAL}$	$V_{DDA\_PDCP\_XTAL}$ = 3.3V		48		mA
		$V_{DDA\_PDCP\_XTAL}$ = 2.5V		33		mA
V_{DDA_FB}	Analog Supply Voltage for APLL Feedback Divider		1.71	1.8	1.89	V
I_{DDA_FB}	Supply Current for V_{DDA_FB}	V_{DDA_FB} = 1.89V		22		mA
$V_{DDA\_BG\_LC}$	Analog Supply Voltage for APLL Bandgap reference and LC Resonator		2.375	[5]	3.465	V
$I_{DDA\_BG\_LC}$	Supply Current for $V_{DDA\_BG\_LC}$	$V_{DDA\_BG\_LC}$ = 3.465V		125		mA
		$V_{DDA\_BG\_LC}$ = 2.625V		88		mA
V_{DD_DIG}	Digital Supply Voltage		1.14	[6]	1.89	V

Table 6. Power Supply DC Characteristics[1][2]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
I_{DD_DIG}	Supply Current for V_{DD_DIG}	V_{DD_DIG} = 1.89V		190		mA
		V_{DD_DIG} = 1.26V		180		mA
$V_{DD\_GPIO\_FOD}$	Power Supply Voltage for FOD blocks FOD_5, GPIO and other status / control signals		1.71	1.8	1.89	V
$I_{DD\_GPIO\_FOD}$ [7]	Supply Current for $V_{DD\_GPIO\_FOD}$ [8]	$V_{DD\_GPIO\_FOD}$ = 1.89V Base current (FOD Off) $I_{DD(FODBASE)}$		30		mA
		Adder for FOD at 500MHz $I_{DD(FODPERFOD)}$		27		mA
		Adder per 1MHz over 500MHz on FOD $I_{DD(FODPERMHZ)}$		0.012		mA/MHz
$V_{DD\_DIA\_FOD\_A}$	Supply Voltage for FOD control logic for FOD_0 and FOD_5 and for FOD_0		1.71	1.8	1.89	V
$I_{DD\_DIA\_FOD\_A}$	Supply Current for $V_{DD\_DIA\_FOD\_A}$ [9]	$V_{DDA\_DIA\_FOD\_A}$ = 1.89V		45		mA
		Adder per FOD at 500MHz		30		mA
		Adder per FOD per 1MHz over 500MHz		0.012		mA/MHz
$V_{DD\_DIA\_FOD\_B}$	Supply Voltage for FOD control logic for FOD_2 and FOD_7 and for FOD_2 and FOD_7		1.71	1.8	1.89	V
$I_{DDA\_DIA\_FOD\_B}$ [10]	Supply Current for $V_{DDA\_DIA\_FOD\_B}$ [9]	$V_{DDA\_DIA\_FOD\_B}$ = 1.89V		69		mA
		Adder per FOD at 500MHz		30		mA
		Adder per FOD per 1MHz over 500MHz		0.012		mA/MHz
V_{DDO_Qx}[11]	Output Clock Q Supply Voltage [12]		1.14		3.465	V

1. V_{SS} = 0V, T_A = -40°C to 85°C.
2. Current consumption figures represent a worst-case consumption with all functions associated with the particular voltage supply being all enabled and running at full capacity. This information is provided to allow for design of appropriate power supply circuits that will support all possible register-based configurations for the device.
3. Supports 1.8V ±5%, 2.5V ±5%, or 3.3V ±5% operation, not a continuous range.
4. I_{DD_CLKx} denotes the current consumed by the appropriate V_{DD_CLKx} supply voltage.
5. Supports 2.5V ±5% or 3.3V ±5% operation, not a continuous range.
6. Supports 1.2V ±5% or 1.8V ±5% operation, not a continuous range.
7. $I_{DD\_DCO\_Qx}$ denotes the current consumed by the appropriate $V_{DD\_DCO\_Qx}$ supply voltage. This is the current consumption for each supply, not the total for all $V_{DD\_DCO\_Qx}$.

8. The $I_{DD\_GPIO\_FOD}$ current consumed is dependent on the number of FODs attached to the voltage rail that are supported and the frequency of operation of those FODs. For information on which FODs are supported by which power supply, see Pin Descriptions and Pin Characteristics. A calculation needs to be performed using the formula below, where f_{FOD} is the operating frequency of each FOD, NumFOD is the number of FODs on that supply that are enabled. Note that only the base current is needed if all FODs are disabled.

$$I_{DD(FOD)} = I_{DD(FODBASE)} + NumFOD \times I_{DD(FODPERFOD)} + \sum_{operatingDCO} (f_{FOD} - 500) \times I_{DD(FODPERMHZ)}$$

9. The I_{DDA_DIA} current consumed is dependent on the number of FODs attached to the voltage rail that are supported and the frequency of operation of those FODs. For information on which FODs are supported by which power supply, see Pin Descriptions and Pin Characteristics. A calculation needs to be performed using the formula below, where f_{FOD} is the operating frequency of each FOD, NumFOD is the number of FODs on that supply that are enabled. Note that only the base current is needed if all FODs are disabled.

$$I_{DD(DIA)} = I_{DD(DIABASE)} + NumFOD \times I_{DD(DIAPERFOD)} + \sum_{operatingDCO} (f_{FOD} - 500) \times I_{DD(DIAPERMHZ)}$$

10. $V_{DDA\_DIA\_FOD\_B}$ consumes higher current than $V_{DDA\_DIA\_FOD\_A}$ because it has some additional circuitry, besides the FODs on it.
11. For information on the signals referenced by this abbreviation, see Table 3.
12. Currents for the outputs are shown in Table 7 or Table 8 as appropriate for the mode the individual output is operating in.

Table 7. Output Supply Current (Output Configured as Differential) [1][2][3]

Symbol	Parameter	Test Condition	SWING [4] = 00	SWING = 01	SWING = 10	SWING = 11	Unit
I_{DDO_Qx} [5]	Qx / nQx Supply Current [6]	V_{DDO_Qx} [7] = 3.465V	15	17	19	20	mA
		V_{DDO_Qx} = 2.625V	14	16	18	19	mA
		V_{DDO_Qx} = 1.89V	14	15	16	16	mA

1. Output current consumption is not affected by any of the core device power supply voltage levels.
2. Internal dynamic switching current at maximum f_{OUT} is included.
3. V_{DDO_Qx} = 3.3V ±5% or 2.5V ±5%, or 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
4. Refers to the output voltage (swing) setting programed into device registers for each output.
5. I_{DDO_Qx} denotes the current consumed by each V_{DDO_Qx} supply.
6. Measured with outputs unloaded.
7. For information on the signals referenced by this abbreviation, see Table 3.

Table 8. Output Supply Current (Output Configured as LVCMOS) [1][2][3]

Symbol	Parameter	Test Condition	TERM [4] = 00		TERM = 01		TERM = 10		TERM = 11		Unit
			Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{DDO_Qx}[5]	Qx, nQx Supply Current [6] Qx and nQx Both Enabled	V_{DDO_Qx}[7] = 3.465V	24	32	25	35	25	37	25	39	mA
		V_{DDO_Qx} = 2.625V	18	25	19	27	19	29	20	30	
		V_{DDO_Qx} = 1.89V	12	20	14	21	15	22	15	23	
		V_{DDO_Qx} = 1.575V	9	17	11	18	11	19	12	20	
		V_{DDO_Qx} = 1.26V	6	13	6	13	6	14	6	14	
	Qx, nQx Supply Current [8] Qx enabled and nQx Tri-stated	V_{DDO_Qx} = 3.465V	14	23	14	24	14	25	14	26	mA
		V_{DDO_Qx} = 2.625V	11	19	11	20	11	20	11	21	
		V_{DDO_Qx} = 1.89V	9	16	10	17	10	17	10	18	
		V_{DDO_Qx} = 1.575V	8	15	8	16	9	16	9	16	
		V_{DDO_Qx} = 1.26V	5	12	5	12	5	12	5	12	

1. Output current consumption is not affected by any of the core device power supply voltage levels.
2. Internal dynamic switching current at maximum f_{OUT} is included.
3. V_{SS} = 0V, T_A = -40°C to 85°C.
4. Refers to the LVCMOS output drive strength (termination) setting programed into device registers for each output.
5. I_{DDO_Qx} denotes the current consumed by each V_{DDO_Qx} supply.
6. Measured with outputs unloaded.
7. For information on the signals referenced by this abbreviation, see Table 3.
8. Measured with outputs unloaded.

3.5 DC Electrical Characteristics

Table 9. LVCMOS/LVTTL DC Characteristics [1][2][3][4][5]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	nMR, nTEST, GPIO[9,8,5:0], SCLK, SDIO, SDI_A1, CS_A0, SDA_M	V_{DD_GPIO} = 1.8V ±5%	0.65 × V_{DD_GPIO}		V_{DD_GPIO} + 0.3	V
V_{IH}	Input High Voltage	XO_DPLL	V_{DD_DIG} = 1.8V ±5%	1.17		3.465	V
			V_{DD_DIG} = 1.2V ±5%	1.17		3.465	V
V_{IH}	Input High Voltage	CLK[1:0], nCLK[1:0][5]	V_{DD_CLK} = 3.3V ±5%	2		V_{DD_CLK} + 0.3	V
			V_{DD_CLK} = 2.5V ±5%	1.7		V_{DD_CLK} + 0.3	V
			V_{DD_CLK} = 1.8V ±5%	0.65 × V_{DD_CLK}		V_{DD_CLK} + 0.3	V
V_{IL}	Input Low Voltage	nMR, nTEST, GPIO[9,5:0], SCLK, SDIO, SDI_A1, CS_A0, SDA_M	V_{DD_GPIO} = 1.8V ±5%	-0.3		0.35 × V_{DD_GPIO}	V
V_{IL}	Input Low Voltage	XO_DPLL	V_{DD_DIG} = 1.8V ±5%	-0.3		0.35 × V_{DD_DIG}	V
			V_{DD_DIG} = 1.2V ±5%	-0.3		0.35 × V_{DD_DIG}	V

Table 9. LVCMOS/LVTTL DC Characteristics [1][2][3][4][5] (Cont.)

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
V_{IL}	Input Low Voltage	CLK[1:0], nCLK[1:0][5]	V_{DD_CLK} = 3.3V ±5%	-0.3		0.8	V
			V_{DD_CLK} = 2.5V ±5%	-0.3		0.7	
			V_{DD_CLK} = 1.8V ±5%	-0.3		0.35 × V_{DD_CLK}	
I_{IH}	Input High Current	nMR, nTEST, GPIO[9,5:0], SDA_M, SCLK, SDIO, SDI_A1, CS_A0	V_{IN} = V_{DD_GPIO} = V_{DD_GPIO} (max)			5	μA
I_{IH}	Input High Current	XO_DPLL	V_{IN} = 3.465V V_{DD_DIG} = V_{DD_DIG} (max)			150	μA
I_{IH}	Input High Current	CLK[1:0]	V_{IN} = V_{DD_CLK} = V_{DD_CLK} (max)			150	μA
		nCLK[1:0]				5	
I_{IL}	Input Low Current	nMR, nTEST, GPIO[9,5:0], SDA_M, SCLK, SDIO, SDI_A1, CS_A0	V_{IN} = 0V, V_{DD_GPIO} = V_{DD_GPIO} (max)	-150			μA
I_{IL}	Input Low Current	XO_DPLL	V_{IN} = 0V V_{DD_DIG} = V_{DD_DIG} (max)	-5			μA
I_{IL}	Input Low Current	CLK[1:0]	V_{IN} = 0V, V_{DD_CLK} = V_{DD_CLK} (max)	-5			μA
		nCLK[1:0]		-150			
V_{OH}	Output High Voltage	GPIO[9,5:0], SDA_M, SCL_M, SCLK, SDIO	V_{DD_GPIO} = 1.8V ±5%, I_{OH} = -100μA	V_{DD_GPIO} - 0.2			V
			V_{DD_GPIO} = 1.8V ±5%, I_{OH} = -2mA	V_{DD_GPIO} - 0.45			
V_{OL}	Output Low Voltage	GPIO[9,5:0], SDA_M, SCL_M, SCLK, SDIO	V_{DD_GPIO} = 1.8V ±5%, I_{OL} = 100μA			0.2	V
			V_{DD_GPIO} = 1.8V ±5%, I_{OL} = 2mA			0.45	

1. V_{IL} should not be less than -0.3V.
2. 3.3V characteristics in accordance with JESD8C-01, 2.5V characteristics in accordance with JESD8-5A.01, 1.8V characteristics in accordance with JESD8-7A, 1.5V characteristics in accordance with JESD8-11A.01, 1.2V characteristics in accordance with JESD8-12A.01
3. V_{SS} = 0V, T_A = -40°C to 85°C.
4. When Output Q are configured as LVCMOS, their output characteristics are specified in Table 15.
5. Input pair used as two single-ended clocks rather than as a differential clock.

Table 10. Low-swing Mode Single-ended Input DC Characteristics[1][2][3][4][5]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{PP}	Peak-to-Peak Voltage		0.15		1.3	V

1. V_{IL} should not be less than -0.3V.
2. V_{IH} should not be higher than V_{DD_CLK}.
3. V_{SS} = 0V, T_A =-40°C to 85°C.
4. Input pair used as two single-ended clocks rather than a differential clock.
5. Input must be AC coupled.

Table 11. Differential Input DC Characteristics[1]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	CLK[1:0]	$V_{IN} = V_{DD\_CLK} = V_{DD\_CLK}$ (max)			150	μA
		nCLK[1:0]				5	
I_{IL}	Input Low Current	CLK[1:0]	V_{IN} = 0V, $V_{DD\_CLK} = V_{DD\_CLK}$ (max)	-5			μA
		nCLK[1:0]		-150			
V_{PP}	Peak-to-Peak Voltage[2][3]		Any input protocol	0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[2][4]	CLK[1:0], nCLK[1:0]	Input protocol = HCSL, HSTL, SSTL	0.1		V_{DD_CLK} - 1.2	V
			Input protocol = LVDS, LVPECL, CML	0.7		V_{DD_CLK}	

1. V_{SS} = 0V, T_A = -40°C to 85°C.
2. V_{IL} should not be less than -0.3V.
3. V_{PP} is the single-ended amplitude of the output signal. The differential specs is 2 * V_{PP}.
4. Common mode voltage is defined as the cross-point.

Table 12. Differential Output DC Characteristics (V_{DDO_Qx} = 3.3V +5%, V_{SS} = 0V, T_A = -40°C to 85°C)[1][2][3][4]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
V_{OVS}[5]	Output Voltage Swing	Output Q[1]	SWING = 00[6]	336	402	462	mV
			SWING = 01	478	605	698	
			SWING = 10	658	791	910	
			SWING = 11	739	870	997	
V_{CMR}[7]	Output Common Mode Voltage	Output Q[1]	CENTER = 000[8]	0.86	0.95	1.07	V
			CENTER = 001	0.98	1.14	1.28	
			CENTER = 010	1.13	1.33	1.51	
			CENTER = 011	1.30	1.53	1.73	
			CENTER = 100	1.46	1.73	1.95	
			CENTER = 101	1.63	1.93	2.17	
			CENTER = 110	1.80	2.12	2.39	
			CENTER = 111	1.96	2.30	2.59	

1. For information on the signals referenced by this abbreviation, see Table 3.
2. Terminated with 100Ω across Qx and nQx.
3. If LVDS operation is desired, select SWING = 00 and CENTER = 001 or 010.
4. If LVPECL operation is desired, select SWING = 10 and CENTER = 101 or 110 for 3.3V LVPECL, and SWING = 10 and CENTER = 001 or 010 for 2.5V LVPECL operation.
5. V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2 * V_{OVS}.
6. Refers to the differential voltage swing setting programed into device registers for each output.
7. Not all V_{CMR} selections can be supported with particular V_{DDO_Qx} and V_{OVS} settings.
8. Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.

Table 13. Differential Output DC Characteristics (V_{DDO_Qx} = 2.5V +5%, V_{SS} = 0V, T_A = -40°C to 85°C)[1][2][3][4]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
V_{OVS}[5]	Output Voltage Swing	Output Q[1]	SWING = 00[6]	295	393	448	mV
			SWING = 01	457	591	677	
			SWING = 10	587	761	881	
			SWING = 11	733	835	943	
V_{CMR}[7]	Output Common Mode Voltage	Output Q[1]	CENTER = 000[8]	0.85	0.93	1.03	V
			CENTER = 001	0.94	1.10	1.23	
			CENTER = 010	1.09	1.28	1.44	
			CENTER = 011	1.24	1.46	1.65	
			CENTER = 100	1.39	1.65	1.86	
			CENTER = 101	Not Supported			
			CENTER = 110				
			CENTER = 111				

1. For information on the signals referenced by this abbreviation, see Table 3.
2. Terminated with 100Ω across Qx and nQx.
3. If LVDS operation is desired, select SWING = 00 and CENTER = 001 or 010.
4. If LVPECL operation is desired, select SWING = 10 and CENTER = 001 or 010 for 2.5V LVPECL operation. For V_{DDO} = 2.5V, 3.3V LVPECL levels cannot be generated.
5. V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2 * V_{OVS}.
6. Refers to the differential voltage swing setting programed into device registers for each output.
7. Not all V_{CMR} selections can be supported with particular V_{DDO_Qx} and V_{OVS} settings.
8. Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.

Table 14. Differential Output DC Characteristics (V_{DDO_Qx} = 1.8V +5%, V_{SS} = 0V, T_A = -40°C to 85°C)[1][2][3]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
V_{OVS}[4]	Output Voltage Swing	Output Q[1]	SWING = 00[5]	299	411	485	mV
			SWING = 01	470	586	700	
			SWING = 10	582	713	852	
			SWING = 11	612	750	899	
V_{CMR}[6]	Output Common Mode Voltage	Output Q[1]	CENTER = 000[7]	0.84	0.91	0.99	V
			CENTER = 001	0.91	1.05	1.18	
			CENTER = 010	1.05	1.21	1.36	
			CENTER = 011	Not Supported			
			CENTER = 100				
			CENTER = 101				
			CENTER = 110				
			CENTER = 111				

1. For information on the signals referenced by this abbreviation, see Table 3.
2. Terminated with 100Ω across Qx and nQx.
3. If LVDS operation is desired, select SWING = 00 and CENTER = 010.
4. V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2 * V_{OVS}.

5. Refers to the differential voltage swing setting programed into device registers for each output.
6. Not all V_{CMR} selections can be supported with particular V_{DDO_Qx} and V_{OVS} settings.
7. Refers to the differential voltage crossing point (center voltage) setting programed into device registers for each output.

Table 15. LVCMOS Clock Output DC Characteristics[1][2]

Symbol	Parameter	Test Condition	TERM[3] = 00			TERM = 01			TERM = 10			TERM = 11			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output High Voltage	V_{DDO_Qx} = 3.3V ±5%	0.74 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			V
		V_{DDO_Qx} = 2.5V ±5%	0.70 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			
		V_{DDO_Qx} = 1.8V ±5%	0.65 × V_{DDO_Qx}			0.71 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			0.75 × V_{DDO_Qx}			
		V_{DDO_Qx} = 1.5V ±5%	0.61 × V_{DDO_Qx}			0.66 × V_{DDO_Qx}			0.70 × V_{DDO_Qx}			0.72 × V_{DDO_Qx}			
		V_{DDO_Qx} = 1.2V ±5%	0.56 × V_{DDO_Qx}			0.59 × V_{DDO_Qx}			0.63 × V_{DDO_Qx}			0.66 × V_{DDO_Qx}			
V_{OL}	Output Low Voltage	V_{DDO_Qx} = 3.3V ±5%			0.29 × V_{DDO_Qx}			0.25 × V_{DDO_Qx}			0.25 × V_{DDO_Qx}			0.25 × V_{DDO_Qx}	V
		V_{DDO_Qx} = 2.5V ±5%			0.32 × V_{DDO_Qx}			0.27 × V_{DDO_Qx}			0.25 × V_{DDO_Qx}			0.25 × V_{DDO_Qx}	
		V_{DDO_Qx} = 1.8V ±5%			0.39 × V_{DDO_Qx}			0.33 × V_{DDO_Qx}			0.30 × V_{DDO_Qx}			0.26 × V_{DDO_Qx}	
		V_{DDO_Qx} = 1.5V ±5%			0.44 × V_{DDO_Qx}			0.38 × V_{DDO_Qx}			0.35 × V_{DDO_Qx}			0.31 × V_{DDO_Qx}	
		V_{DDO_Qx} = 1.2V±5%			0.50 × V_{DDO_Qx}			0.46 × V_{DDO_Qx}			0.42 × V_{DDO_Qx}			0.38 × V_{DDO_Qx}	
Z_{OUT}	Output Impedance	V_{DDO_Qx} = 3.3V±5%		35			25			21			18		Ω
		V_{DDO_Qx} = 2.5V±5%		31			23			20			17		
		V_{DDO_Qx} = 1.8V±5%		42			31			25			21		
		V_{DDO_Qx} = 1.5V±5%		71			47			35			29		
		V_{DDO_Qx} = 1.2V±5%		101			86			66			49		

1. V_{SS} = 0V, T_A = -40°C to 85°C.
2. V_{DDO_Qx} is used to refer to the appropriate V_{DDO_Qx} power supply voltage for each output. For more information, see Table 3 and Table 2.
3. This refers to the register settings for the LVCMOS output drive strength within the device.

Table 16. Input Frequency Characteristics[1]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
f_{IN}	Input Frequency	OSCI, OSCO	Using a Crystal[2]	25		54	MHz
			Over-driving Crystal Input Doubler Logic Enabled[3]	25		62.5	
			Over-driving Crystal Input Doubler Logic Disabled	50		125	
		Input CLK[4][5]	Differential Mode			1000	
			Single-ended Mode			250	
		GPIO	Used as Clock Input			150	
f_{IN}	Input Frequency	XO_DPLL		1		150[6] [f]	MHz
f_{SCLK}	Serial Port Clock SCLK (Slave mode)	I^2C Operation		100		1200	kHz
		SPI Operation		0.1		50	MHz

1. V_{SS} = 0V, T_A = -40°C to 85°C.
2. For crystal characteristics, see Table 17.
3. Refer to Overdriving the XTAL Interface.
4. For information on the signals referenced by this abbreviation, see Table 3.
5. For proper device operation, the input frequency must be divided down to 150MHz or less (DPLL Phase Detector maximum frequency = 150MHz).
6. If the System DPLL needs to be driven with a higher frequency, one of the CLKx / nCLKx inputs can be routed via register settings to the System DPLL instead of using XO_DPLL.

Table 17. Crystal Characteristics[1]

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Mode of Oscillation		Fundamental			
Frequency		25		54	MHz
Equivalent Series Resistance (ESR)	C_L= 18pF, crystal frequency $\leq$ 40MHz			50	Ω
	C_L= 18pF, crystal frequency > 40MHz			25	
	C_L= 12pF			50	
Load Capacitance (C_L)			12		pF

1. V_{SS} = 0V, T_A = -40°C to 85°C.

3.6 AC Electrical Characteristics

Table 18. AC Characteristics[1][2]

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Unit
f_{VCO}	Analog PLL VCO Operating Frequency		V_{DDA_X}[3] = 3.3V ±5%		13.4		13.8	GHz
			V_{DDA_X}[3] = 2.5V ±5%		13.5		13.9	
f_{FOD}	Fractional Output Divider Operating Frequency		Measured with output divider set to /1		500		1000	MHz
f_{OUT}	Output Frequency	Differential Output			0.0000005		1000	MHz
		LVCMOS Output			0.0000005		250	
Δf_{OUT}	Output Frequency Accuracy[4]					0		ppb
	Initial Frequency Offset[5]		Switchover or Entering Holdover State			1		ppb
	Output Phase Change in Fully Hitless Switching[6]		Input references with phase difference < 100μs			350		ps
			Input references with phase difference ≥ 100μs			1000		
t_{SK}	Output-to-Output Skew[7][8]		Any two differential outputs[9]	V_{DDO_Qx} = 3.3V ±5%		65	150	ps
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%				
			Any two outputs configured as LVCMOS in-phase[10]	V_{DDO_Qx} = 3.3V ±5%		100	255	
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%				
				V_{DDO_Qx} = 1.5V ±5%[11]				
				V_{DDO_Qx} = 1.2V ±5%[11]				
			Q to nQ of same output pair, configured as LVCMOS, in-phase[10]	V_{DDO_Qx} = 3.3V ±5%		20	90	
				V_{DDO_Qx} = 2.5V ±5%		20	130	
				V_{DDO_Qx} = 1.8V ±5%				
				V_{DDO_Qx} = 1.5V ±5%[11]				
				V_{DDO_Qx} = 1.2V ±5%[11]				

Table 18. AC Characteristics[1][2] (Cont.)

Symbol	Parameter	Test Condition			Minimum	Typical	Maximum	Unit
$t_{SK(B)}$	Output-to-Output Skew within a Bank[12]	Bank 1: Q0/nQ0(FOD4), Q1/nQ1(FOD4), Q2/nQ2(FOD4), Q3/nQ3(FOD2), Q8/nQ8(FOD5), Q9/nQ9(FOD2)	Differential[9]	V_{DDO_Qx} = 3.3V ±5%		30	65	ps
				V_{DDO_Qx} = 2.5V ±5%		30	72	
				V_{DDO_Qx} = 1.8V ±5%				
			LVCMOS [10]	V_{DDO_Qx} = 3.3V ±5%		75	150	
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%				
		Bank 2: Q4/nQ4(FOD0), Q10/nQ10(FOD0)	Differential[9]	V_{DDO_Qx} = 3.3V ±5%		22	50	ps
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%				
			LVCMOS [10][11]	V_{DDO_Qx} = 3.3V ±5%		45	130	
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%				
		Bank 3: Q5/nQ5(FOD0), Q6/nQ6(FOD7), Q7/nQ7(FOD7), Q11/nQ11(FOD7)	Differential[9]	V_{DDO_Qx} = 3.3V ±5%		35	90	ps
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%				
			LVCMOS [10][11]	V_{DDO_Qx} = 3.3V ±5%		55	130	
				V_{DDO_Qx} = 2.5V ±5%				
				V_{DDO_Qx} = 1.8V ±5%		55	160	
Δt_{SK}	Temperature Variation[13] Output-Output						4	ps/°C
t_{ALIGN}	Input - Output Alignment Variation[14]	Delay variation as shown in Figure 6 for any CLK/CLKn input pair to any Q/Qn output pair in differential mode when using internal loopback.			-500		500	ps
Δt_{ALIGN}	Temperature Variation[13] Input-Output						4	ps/°C

Table 18. AC Characteristics[1][2] (Cont.)

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Unit
t_R / t_F	Output Rise and Fall Times 20% to 80%	Differential Output[15] [16]	V_{DDO_Qx}[17] = 3.3V ±5%, 2.5V±5% or 1.8V ±5%	SWING[18] = 00	100		400	ps
				SWING = 01	100		450	
				SWING = 10				
				SWING = 11				
		LVCMOS Output[19]	V_{DDO_Qx} = 3.3V ±5%	TERM[20] = 00	100	254	380	ps
				TERM = 01	100	262	400	
				TERM = 10	110	275	460	
				TERM = 11	115	268	510	
			V_{DDO_Qx} = 2.5V ±5%	TERM = 00	115	285	405	ps
				TERM = 01	120	293	470	
				TERM = 10	120	315	525	
				TERM = 11	140	347	565	
			V_{DDO_Qx} = 1.8V ±5%	TERM = 00	205	417	590	ps
				TERM = 01	205	458	715	
				TERM = 10	230	459	800	
				TERM = 11	235	482	880	
			V_{DDO_Qx} = 1.5V ±5%[21]	TERM = 00	415	558	730	ps
				TERM = 01	545	747	985	
				TERM = 10	615	890	1145	
				TERM = 11	690	1011	1305	
			V_{DDO_Qx} = 1.2V ±5%[21]	TERM = 00	800	986	1250	ps
				TERM = 01	1180	1416	1835	
				TERM = 10	1415	1715	2195	
				TERM = 11	1650	1980	2520	
odc	Output Duty Cycle	Differential Output	PULSE = 50%	f_{OUT} < 500MHz	47	50	53	%
				500MHz ≤ f_{OUT} < 800MHz	45	50	55	%
				f_{OUT} ≥ 800MHz	40	50	60	%
		LVCMOS	PULSE = 50%	V_{DDO_Qx} = 3.3V or 2.5V	47	50	53	%
				V_{DDO_Qx} = 1.8V or 1.5V	45	50	55	
				V_{DDO_Qx} = 1.2V	42	50	58	
t_{LOCK}	1PPS Locking Time		17mHz loop bandwidth, phase and frequency snap enabled				20	S
$t_{STARTUP}$	Start-up Time[22]	Regulators Ready[23]				3		µs
		Internal OTP Start-up	Synthesizer mode			7	10	ms
			DPLL mode, with a loop bandwidth setting of 300Hz[24]			1.5		s

Table 18. AC Characteristics[1][2] (Cont.)

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
PSNR	Power Supply Noise Rejection[25][26][27][28]	VDDA_LC_BG	50mVpp		-85		dBc
			100mVpp		-80		
		VDDA_PDCP_XTAL	50mVpp		-75		
			100mVpp		-70		
		VDDO_Qx	50mVpp		-70		
			100mVpp		-70		

1. V_{SS} = 0V, T_A = -40°C to 85°C.
2. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
3. V_{DDA_X} refers to V_{DDA_PDCP}, V_{DDA_XTAL}, V_{DDA_LC}, and V_{DDA_BG}.
4. Long-term frequency error with respect to the DPLL input reference. The typical value shown assumes the DPLL has been phase-locked to a stable input reference for at least 306 minutes (based on a 0.1mHz advanced holdover filter setting) before going into an advanced holdover state on disqualification of the input reference.
5. This parameter will vary with the quality of the reference to the system DPLL. The typical value shown assumes an ideal reference used for the system DPLL.
6. This parameter will vary with the quality of the TDC and system DPLL references. The typical value shown assumes an ideal reference is used as input to the TDC and system DPLL.
7. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage
8. This parameter is defined in accordance with JEDEC Standard 65.
9. Measured at the differential cross points.
10. Measured at V_{DDO_Qx} / 2.
11. Using LVCMOS with V_{DDO_Qx} = 1.5V or 1.2V will result in much larger skews and is not recommended for skew-sensitive applications.
12. Banks are defined as a list of outputs driven by a specific FOD. Results do not apply if the output is driven by a different FOD.
13. This parameter is measured across the full operating temperature range and the difference between the slowest and fastest numbers is the variation.
14. Measured from the differential cross point of the input to the differential cross point of the associated output after device is locked and input is stable. Measured using integer-related input and output frequencies.
15. Rise and fall times on differential outputs are independent of the power supply voltage on the output.
16. Measured with outputs terminated with 50Ω to GND.
17. For information on the signals referenced by this abbreviation, see Table 3.
18. Refers to the differential voltage swing setting programed into device registers for each output.
19. Measured with outputs terminated with 50Ω to V_{DDO_Qx} / 2.
20. Refers to the LVCMOS output drive strength (termination) setting programed into device registers for each output.
21. This parameter has been characterized with F_{OUT} = 50MHz.
22. Measured from the rising edge of nMR after all power supplies have reached > 80% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked analog or digital PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected.
23. At power-up, the nMR signal must be asserted for at least this period of time.
24. Start-up time will depend on the actual configuration used. For more information on estimating start-up time, contact Renesas technical support.
25. Noise spur amplitude measured relative to 156.25MHz carrier.
26. Typical PSNR values specified over the modulation frequency range of 10kHz to 1MHz.
27. Injected as sinusoidal noise to the specified power rail only.
28. 0.1uF capacitor placed on modulated power rail.

Table 19. Phase Jitter and Phase Noise

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
tjit(Φ)	Random Phase Jitter (12kHz to 20MHz, 50MHz Crystal, Clock Generator Mode, 13750MHz APLL VCO Frequency)	156.25MHz (IOD)	-	107	130	fs (RMS)
		312.5MHz (IOD)	-	103	120	
		106.25MHz (FOD)	-	147	165	
		100MHz (FOD)	-	176	192	
tjit(Φ)	Random Phase Jitter (12kHz to 20MHz, 54MHz Crystal, Jitter Attenuator Mode with 10Hz loop bandwidth, 25MHz input from SMA-100)	156.25MHz	-	108	133	fs (RMS)
		312.5MHz	-	108	133	
ΦSSB(1k)	Single Sideband Phase Noise (50MHz Crystal, Clock Generator Mode, 13750MHz APLL VCO Frequency, one IOD output enabled at 156.25MHz	1kHz Offset	-	-129	-	dBc/Hz
ΦSSB(10k)		10kHz Offset	-	-136	-	
ΦSSB(100k)		100kHz Offset	-	-145	-	
ΦSSB(1M)		1MHz Offset	-	-153	-	
ΦSSB(10M)		10MHz Offset	-	-157	-	
ΦSSB(20M)		20MHz Offset	-	-158	-	
ΦSSB(1k)	Single Sideband Phase Noise (50MHz Crystal, Clock Generator Mode, 13750MHz APLL VCO Frequency, one FOD output enabled at 106.25MHz	1kHz Offset	-	-127	-	dBc/Hz
ΦSSB(10k)		10kHz Offset	-	-134	-	
ΦSSB(100k)		100kHz Offset	-	-143	-	
ΦSSB(1M)		1MHz Offset	-	-155	-	
ΦSSB(10M)		10MHz Offset	-	-158	-	
ΦSSB(20M)		20MHz Offset	-	-159	-	
ΦSSB(1k)	Single Sideband Phase Noise (54MHz Crystal, Jitter Attenuator Mode with 10Hz loop bandwidth,25MHz input from SMA-100, one output enabled at 156.25MHz)	1kHz Offset	-	-126	-	dBc/Hz
ΦSSB(10k)		10kHz Offset	-	-134	-	
ΦSSB(100k)		100kHz Offset	-	-145	-	
ΦSSB(1M)		1MHz Offset	-	-152	-	
ΦSSB(10M)		10MHz Offset	-	-156	-	
ΦSSB(20M)		20MHz Offset	-	-157	-	
-	Output-output Isolation	Measured on 156.25MHz LVDS victim with 100MHz HCSL aggressor	-	-75	-	dB

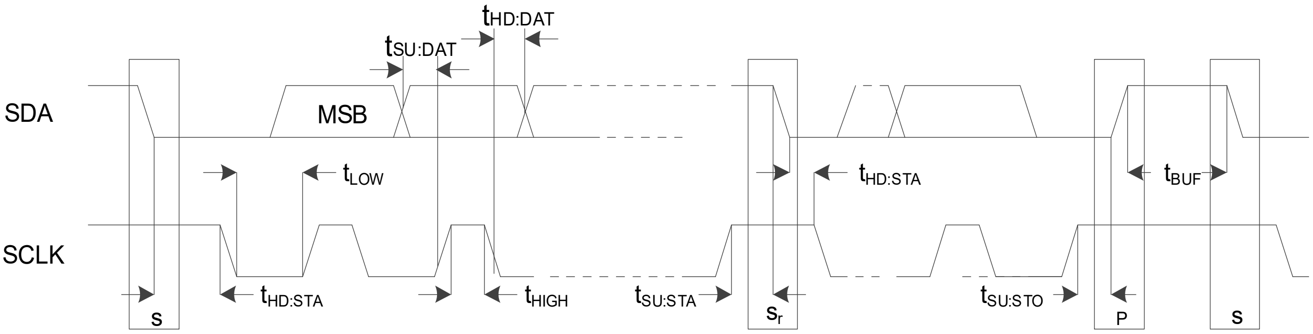


Figure 4. I^{2}C Slave Timing Diagram

Table 20. I^{2}C Slave Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
f_{SCLK}	SCLK Operating Frequency			1	MHz
t_{LOW}	SCLK Pulse Width Low		130		ns
t_{HIGH}	SCLK Pulse Width High		9		ns
$t_{SU:STA}$	Start or Repeat Start Setup Time to SCLK		6		ns
$t_{HD:STA}$	Start or Repeat Start Hold Time from SCLK		18		ns
$t_{SU:DAT}$	Data Setup Time to SCLK rising edge		5		ns
$t_{HD:DAT}$	Data Hold Time from SCLK rising edge		0		ns
$t_{SU:STO}$	Stop Setup Time to SCLK		12		ns
t_{BUF}	Minimum Time from Stop to Next Start		0.5		ns

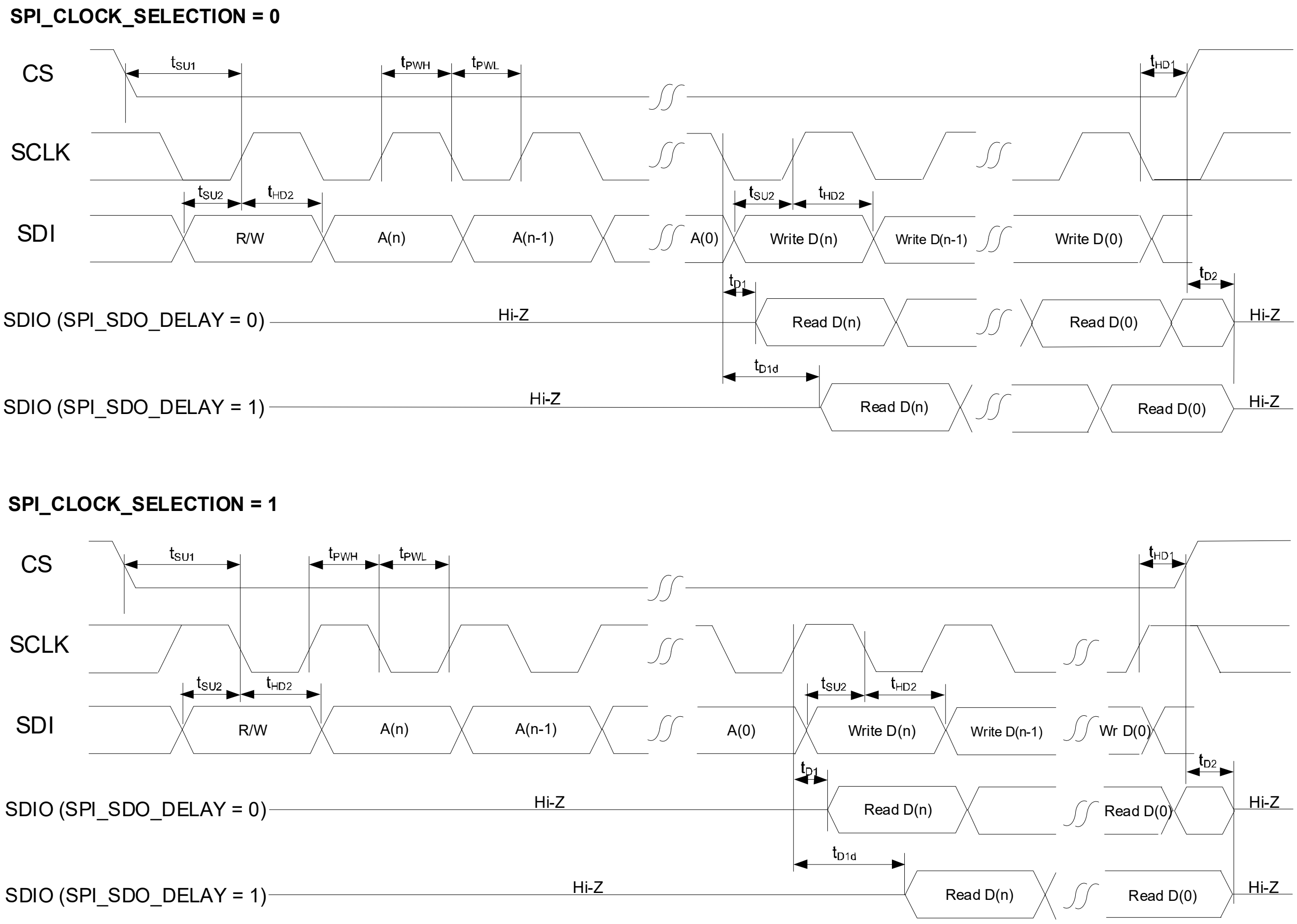


Figure 5. SPI Timing Diagram

Table 21. SPI Timing

Parameter	Description		Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency when performing only writes				50	MHz
	Maximum operating frequency when performing mixed reads and writes				40	MHz
t_{PWH}	SCLK Pulse Width High			5		ns
t_{PWL}	SCLK Pulse Width Low			6		ns
t_{SU1}	CS Setup Time to SCLK rising or falling edge			3		ns
t_{HD1}	CS Hold Time from SCLK rising or falling edge			1		ns
t_{SU2}	SDIO Setup Time to SCLK rising or falling edge			4		ns
t_{HD2}	SDIO Hold Time from SCLK rising or falling edge			1		ns
t_{D1}[1]	Read Data Valid Time from SCLK rising or falling edge with no data delay added	V_{CCCS} = 3.3V		6		ns
		V_{CCCS} = 2.5V		6		ns
		V_{CCCS} = 1.8V		6		ns

Table 21. SPI Timing (Cont.)

Parameter	Description		Minimum	Typical	Maximum	Unit
t_{D1d}[1]	Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing[2]	V_{CCCS} = 3.3V		6 + half SCLK period		ns
		V_{CCCS} = 2.5V		6 + half SCLK period		ns
		V_{CCCS} = 1.8V		6 + half SCLK period		ns
t_{D2}	SDIO Read Data Hi-Z Time from CS High[3]			10		ns

1. Measurement performed approximately 1cm away from device pad. Observing at a greater distance on a heavily loaded trace may show slower edge rates and longer delays. This is highly dependent on PCB loading.
2. Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.
3. This is the time until the RC32012A releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

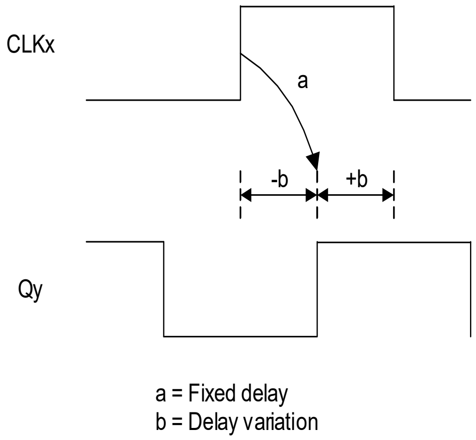


Figure 6. Input-Output Delay

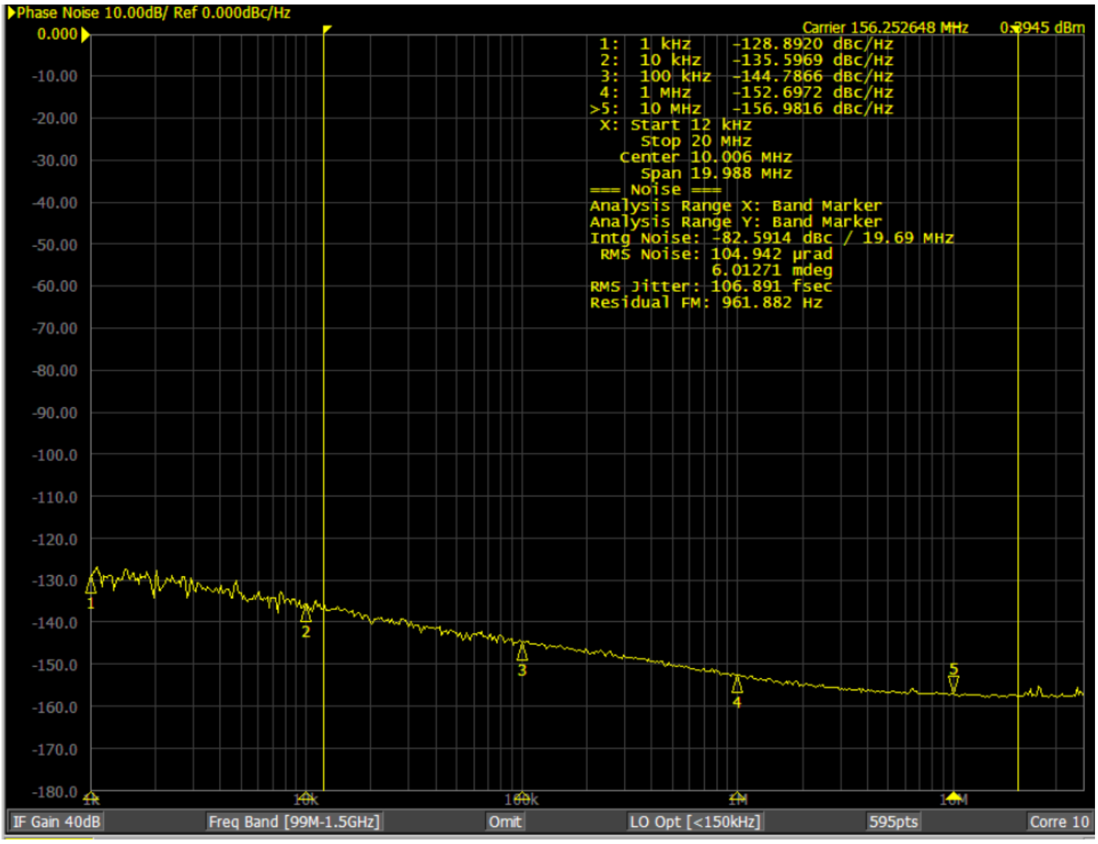
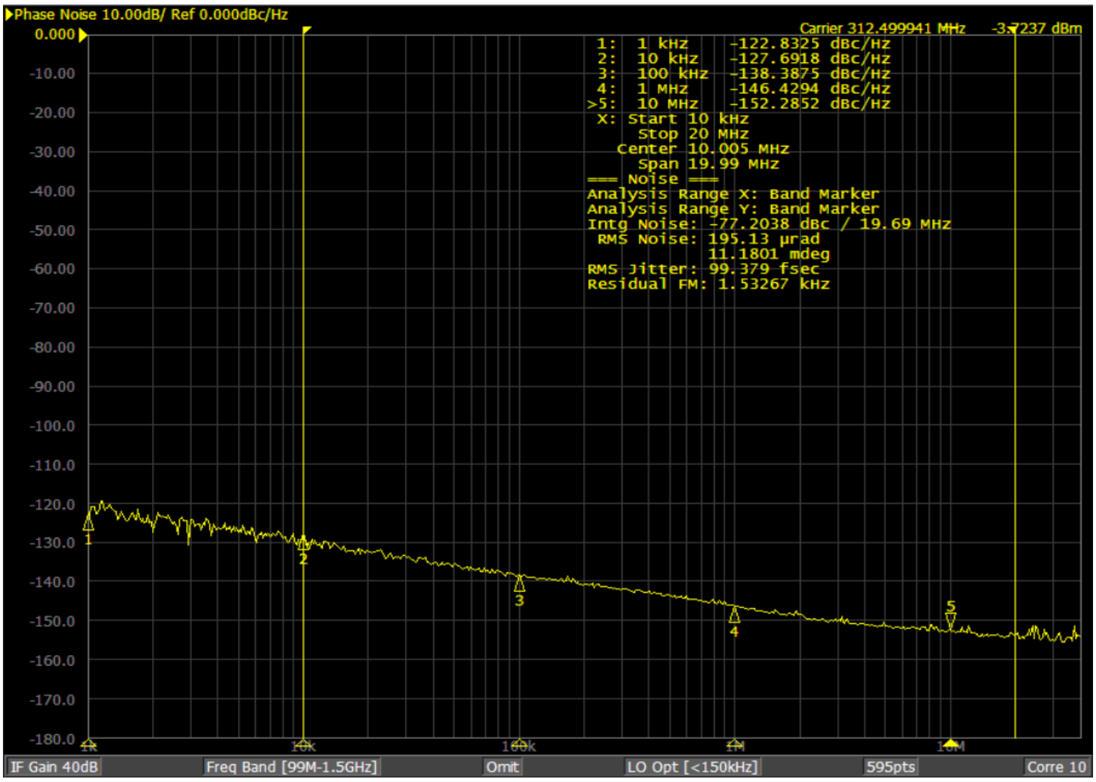

```
Carrier 156.252648 MHz     0.3945 dBm
 1:  1 kHz     -128.8920 dBc/Hz
 2:  10 kHz    -135.5969 dBc/Hz
 3:  100 kHz   -144.7866 dBc/Hz
 4:  1 MHz     -152.6972 dBc/Hz
>5:  10 MHz    -156.9816 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -82.5914 dBc / 19.69 MHz
 RMS Noise: 104.942 µrad
            6.01271 mdeg
RMS Jitter: 106.891 fsec
Residual FM: 961.882 Hz
```

Figure 7. Phase Noise of 156.25MHz Output in Clock Generator Mode


```
Carrier 106.251806 MHz     0.3311 dBm
 1:  1 kHz     -127.4422 dBc/Hz
 2:  10 kHz    -133.9275 dBc/Hz
 3:  100 kHz   -142.5945 dBc/Hz
 4:  1 MHz     -154.6148 dBc/Hz
>5:  10 MHz    -158.0295 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -82.9883 dBc / 19.69 MHz
 RMS Noise: 100.254 µrad
            5.7441 mdeg
RMS Jitter: 150.17 fsec
Residual FM: 833.12 Hz
```

Figure 8. Phase Noise of 106.25MHz Output in Clock Generator Mode



```
 1:  1 kHz     -122.8325 dBc/Hz
 2:  10 kHz    -127.6918 dBc/Hz
 3:  100 kHz   -138.3875 dBc/Hz
 4:  1 MHz     -146.4294 dBc/Hz
>5:  10 MHz    -152.2852 dBc/Hz
 X: Start 10 kHz
      Stop 20 MHz
    Center 10.005 MHz
      Span 19.99 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -77.2038 dBc / 19.69 MHz
 RMS Noise: 195.13 µrad
            11.1801 mdeg
RMS Jitter: 99.379 fsec
Residual FM: 1.53267 kHz
```

Figure 9. Phase Noise of 312.5MHz Output in Jitter Attenuator Mode

4. Functional Description

The RC32012A is a fully integrated, low-power, high-performance frequency synthesizer with jitter attenuation and network synchronization capabilities. The device can be set up as either of the following:

- Clock generator, that is locked to the external crystal or oscillator and providing free-run clock outputs
- Jitter attenuator, that is locked to an external reference and providing low-jitter clock outputs when used with an external crystal or oscillator

The device is optimized to deliver excellent phase noise as required for driving up to 28Gbps Ethernet PHYs, ASICs or FPGAs in 10G, 25G, 40G, 100G, 200G, or 400G switch line cards and switch fabric cards. The RC32012A supports JEDEC JESD204B/C for converter synchronization and SyncE for network-based synchronization.

4.1 Clock Generator Mode

The RC32012A can be set in Clock Generator mode by completing the following steps:

1. DPLL/DCO and System DPLL are powered down.
2. CLK0, CLK1 and GPIO0, GPIO3, GPIO9 are unused for reference clock inputs.
3. APLL is locked to external crystal or oscillator and provides high-frequency clocks to FOD_0, FOD_2, FOD_5, and FOD_7.
4. Free-run clock outputs are generated from FOD_0, FOD_2, FOD_5, or FOD_7, and each FOD can be independently set to integer or fractional divide values.

Note: Up to four unrelated clock frequency domains can be achieved.

4.2 Jitter Attenuator or Synchronizer Mode

The RC32012A can be set in Jitter Attenuator or Synchronizer mode by completing the following steps:

- CLK0, CLK1 and GPIO0, GPIO3, GPIO9 are used for reference clock inputs.
- APLL is locked to external crystal or oscillator and provides high-frequency clocks to SYS_DPLL and FOD_0, FOD_2, FOD_5, FOD_7.
- System DPLL locks to external oscillator or TCXO or OCXO.
- DPLL/DCO uses FOD_0 to be synchronized and locked to the chosen reference clock input.
- Clock outputs, generated from synchronized DPLL/DCO, are generated from FOD_0
- Clock outputs, generated from free-run APLL or from System DPLL or from synchronized DPLL/DCO, are generated from FOD_2, FOD_5, and FOD_7, which can be set to integer or fractional divider values

Note: Up to four unrelated clock frequency domains can be achieved

4.3 Power-Up, Configuration and Serial Interfaces

The RC32012A can be powered up and configured in three ways:

- From internal non-volatile memory using OTP user configurations (UserCfgs)
- From its slave serial interface
- From an external I2C EEPROM

The RC32012A supports three slave serial interfaces: I2C, SPI, and SMBUS, and one serial master interface (I2C). These interfaces share the same pins, so only one is available at a time. Additionally, all of the device GPIO pins are sampled at the rising edge of the nMR (master reset) signal and some of them can be used in setting the initial configuration.

4.4 Input Clocks

The RC32012A supports one crystal/reference input that is used as a reference to the analog PLL (APLL). Up to two differential or seven single-ended clock inputs can be used as a reference to the digital PLL (DPLL) and support hitless reference switching. GPIO0, GPIO3, and GPIO9 can alternately be set as reference clock inputs in Jitter Attenuator mode.

4.4.1 Crystal/Oscillator Input

The crystal input supports crystal frequencies of 25MHz to 54MHz with a recommended load capacitance of 12pF. The crystal input can be over-driven with differential or single-ended inputs with proper external terminations. The supported frequency range is 25MHz to 62.5MHz when doubler logic for APLL is enabled, and 50Mz to 125MHz when doubler logic for APLL is disabled. An available LOS monitor detects the loss of signal on crystal input.

4.4.2 XO_DPLL Input

The XO_DPLL input supports frequencies of 1MHz to 150MHz when driven by an external oscillator, TCXO, or OCXO. An available LOS monitor detects the loss of signal on XO_DPLL input.

4.4.3 Reference Clock Inputs

There are two differential reference clock inputs that support differential or single-ended CMOS logic levels without external terminations. If set to single-ended type, each differential input turns into two single-ended inputs. Additionally, GPIO0, GPIO3, and GPIO9 can each be individually programmed to act as a single-ended input. Internal biasing is available for AC-coupled applications. The two clock inputs can be left floating when unused. An available LOS monitor detects the loss of signal on reference clock inputs.

4.5 Clock Input Monitors

There are two types of reference clock monitors: one to monitor the APLL input and the other to monitor the DPLL inputs. The APLL input is monitored for Loss of Signal (LOS). While the DPLL clock inputs (CLKIN0, CLKIN0B, CLKIN1, CLKIN1B, GPIO0, GPIO3, and GPIO9) each have LOS, activity and frequency monitoring.

- The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least eight times that of the measuring clock period.
- The frequency monitor can be configured to measure the reference over a nominal 5ms time window in order to achieve ~1ppm granularity.
- The frequency monitor can be configured to measure the reference over a nominal 0.4s time window in order to achieve ~12ppb granularity.

4.6 Clock Input Monitor

The APLL input is monitored for Loss of Signal (LOS). The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least eight times that of the measuring clock period.

4.7 APLL

The APLL is an integer LC-VCO based PLL with an operating range from 13.4GHz to 13.9GHz. The crystal or oscillator input clock is used to drive the APLL, and can be frequency doubled for increased performance. The APLL is temperature compensated for utmost frequency stability. The high-frequency clock output from the APLL is provided to each of the four fractional output dividers (FOD_0, FOD_2, FOD_5, FOD_7).

4.7.1 APLL Lock Detector

The APLL lock detector indicates whether the APLL is locked to a functioning crystal or reference input by monitoring the phase errors. Lock status is available on a GPIO pin or in the register map.

4.8 System DPLL

The System DPLL uses a high-frequency clock input from the APLL and forms a fractional-N DPLL architecture that is locked to the oscillator, or TCXO or OCXO. The System DPLL generates an internal system clock that is used by the reference monitors and other digital circuitry in the device. If the reference provided to the System APLL meets the stability and accuracy requirements of the intended application then the System DPLL can free run and a System DPLL reference is not required. Alternatively, the System DPLL can be locked to an external reference that meets the stability and accuracy requirements of the intended application. The System DPLL can accept a reference from the XO_DPLL. The frequency information from the System DPLL can be shared with the DPLL and with each of the four fractional output dividers (FOD_0, FOD_2, FOD_5, and FOD_7).

4.9 DPLL

To operate in Jitter Attenuator or Synchronizer mode, FOD_0, which receives its high-frequency clock input from the APLL, is used as a DCO and forms a fractional-N DPLL architecture that is locked to the chosen reference clock input. The APLL locks to an input clock from a crystal or a crystal oscillator and generates an output clock in the range of 13.4GHz to 13.9GHz, and FOD_0 generates an output clock in the range of 500MHz to 1GHz. The FOD_0 acts as a digital controlled oscillator (DCO) and is dynamically controlled by the DPLL. The DPLL also uses the FOD_0 output clock to generate the fractional divided DPLL feedback clock. The DPLL fractional feedback divider, which is comprised of 48-b numerator and 48-b denominator, is static during normal operation.

4.10 DPLL Operating Modes

All DPLLs within RC32012A are exactly the same. The only difference with the System DPLL channel is that it is not connected directly to any output stages. One channel of the DPLL is shown in Figure 10.

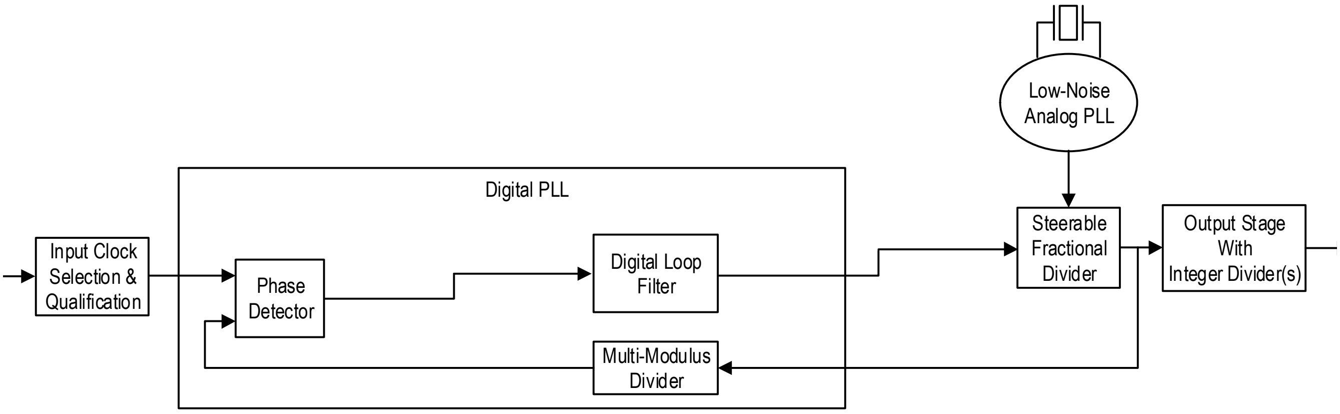


Figure 10. DPLL Channel

The DPLL operating mode operation can be set to automatic, forced locked, forced free-run and forced holdover. They can be controlled by setting the appropriated bits in the DPLL mode register. When the DPLL is set to automatic, then an internal state machine will control the states automatically. The automatic state machine is shown in n Figure 11.

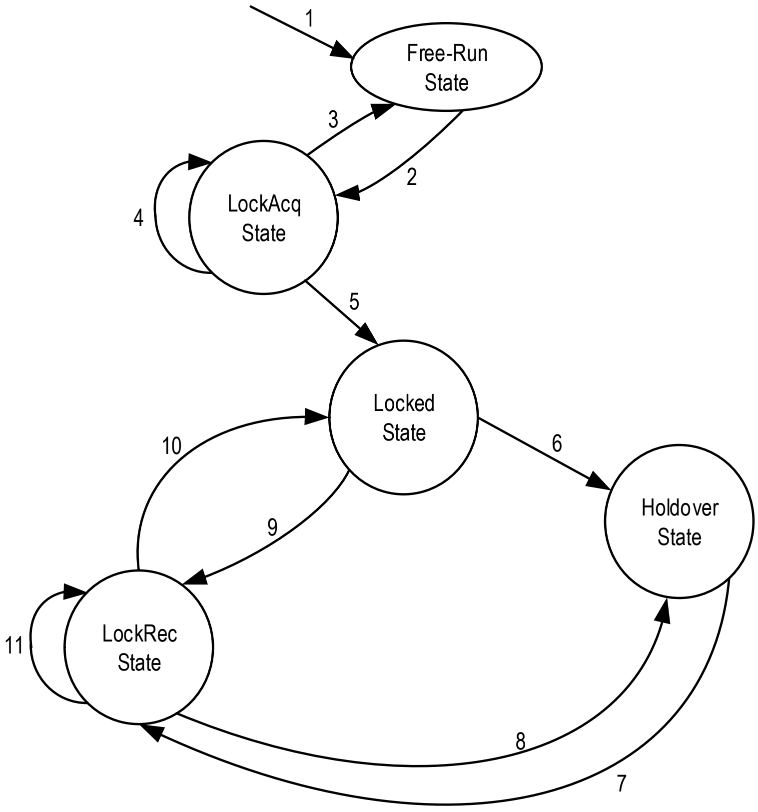


Figure 11. DPLL Automatic State Machine

In Figure 11, the changes of state are based on:

1. Reset, the device enters Free-Run State
2. Once an input clock is qualified and it is selected: enter the LockAcq State
3. If the DPLL selected input clock is disqualified AND no qualified input clock is available: go back to Free-Run State
4. DPLL switches to another qualified clock: remain in LockAcq State
5. The DPLL locks to the selected input clock: enter Locked State.
6. The DPLL selected input clock is disqualified AND No qualified input clock is available: enter Holdover State.
7. A qualified input clock is now available: enter LockRec State.
8. If the DPLL selected input clock is disqualified AND no qualified input clock is available: go back to Holdover State.
9. The DPLL switches to another qualified clock: enter LockRec State
10. The DPLL locks to the selected input clock: go to Locked State
11. The DPLL switches to another qualified clock: remain in LockRec State

In items 4, 9, and 11, the DPLL switches to another qualified clock due to the selected input clock being disqualified, or the device is set to revertive mode and a qualified input clock with a higher priority becomes valid, or the device is set to Forced selection to another input clock.

4.10.1 Free-Run Mode

In Free-Run mode the DPLL synthesizes clocks based on the system clock (crystal oscillator) and has no influence from a current or a previous input clock.

Combo mode can be used with Free-Run mode. In that case the input clock of the combo master affects the combo slave's free-Run frequency.

4.10.2 Locked Mode

In Locked mode, the DPLL is synchronized to an input clock. The frequency and phase of the output clock track the DPLL selected input clock. The bandwidth (BW) and damping factor are programmable and are used by the DPLL when locked to an input reference. Table 22 includes some common BW settings and their associated applications.

Table 22. DPLL Bandwidth

DPLL BW (Hz)[1]	Description
92.6 m	GR-253 stratum 3, SMC and G.8262 EEC-option 2 BW<0.1Hz G.8273.2 0.5≤BW≤0.1
278 m	
556 m	
1.11	G.8262 EEC-option 1 1≤BW≤10, GR-1244 stratum 3 BW<3Hz
2.22	G.8262 EEC-option 1 1≤BW≤10, GR-1244 stratum 3 BW<3Hz
4.45	G.8262 EEC-option 1 1≤BW≤10
8.89	G.8262 EEC-option 1 1≤BW≤10
17.8	
35.6	
71.2	
94.4	
142	
285	G.8251 (OTN)
333	
571	
11.4 k	
12.1 k	Jitter attenuators and Clock generators

[1] Values shown are the nominal loop bandwidths that will be provided by the DPLL. Data entry via registers uses a different format and will result in the nearest value in this table that is less than the requested value in the registers.

4.10.3 Holdover Mode

If all the input clocks for a particular DPLL become invalid, then that DPLL will enter holdover state.

In holdover mode, the DPLL uses stored frequency data acquired in Locked mode to control its output clocks. There are several programmable modes for the frequency offset acquisition method; it can use the frequency offset just before it entered holdover state (simple holdover), or a previously stored post-filtered frequency offset (advanced holdover).

For the advanced holdover mode, the holdover value can be post filtered and is stored in two registers at a programmable rate while the DPLL is in locked state. When the DPLL enters the advanced holdover mode, the oldest register value is restored into the integrator inside the DPLL. The rate at which the holdover registers are updated is programmable between 0 and 63 s in steps of 1s.

Note: For the advanced holder function to operate correctly, the DPLL must have been in a locked state for multiples of the update rate before a holdover occurs or the advanced holdover values will not have settled to accurate values before being used.

The DPLL can also be forced into the holdover mode. If the forced holdover mode is used, then the DPLL will stay in holdover even if there are valid references available for the DPLL to lock to.

4.10.4 Manual Holdover Mode

In Manual Holdover mode, the DPLL state machine is forced into the Holdover state, but frequency offset is set by the DPLL manual holdover value register bits under user control.

4.11 DPLL Input Clock Qualification and Selection

The Digital PLL (DPLL) may use any of the inputs as its reference. Several options exist to control how the DPLL selects which input to use at any moment in time. Whether a particular input is qualified for use at any time is based on the reference monitors. The DPLL_REF_MODE registers allow the DPLL to be set in any of the modes shown in Table 23. There is an independent reference selection process for the DPLL.

Table 23. DPLL Reference Mode

DPLL_ref_mode[3:0]	Description
0000	Automatic input clock selection
0001	Manual input clock selection
0010	GPIO
0011	Slave
0100	GPIO_Slave
0101 - 1111	Reserved

4.11.1 Automatic Input Clock Selection

If automatic input clock selection is used, then the input clock selection is determined by the input clock being valid, the priority of each input clock, and the input clock configuration.

Each input can be enabled or disabled by setting register bits. If the input is enabled and reference monitors declare that input valid, then that input is qualified to be used by the DPLL. Within all the qualified inputs, the one with the highest priority is selected by the DPLL. The input clock priority is set by setting the appropriate bits in the DPLL_REF_PRIORITY registers. If a user wished to designate several inputs as having the same priority, then an additional table allows several outputs to be placed in a group of equal priority.

4.11.2 Manual Input Clock Selection via Register or GPIO

If manual input clock selection is chosen then the DPLL will lock to the input clock indicated by register bits or by selected GPIO pins. The results of input reference monitoring do not affect the clock selection in manual selection mode.If the DPLL is locked to an input clock that becomes invalid, then the DPLL will go into holdover even in the case where there are other input clocks that are valid.

4.11.3 Slave or GPIO Slave Selection

This mode of clock selection is used when the RC32012A is acting as an inactive, redundant clock source to another timing device. The other device is the master and this device is the slave. When Slave mode is selected via registers, a specific input (from the master timing device) is also indicated. That input and only that input is used in this mode. GPIO Slave mode involves the same configuration settings as if the part were a master, but a GPIO input is used to tell this device that it is now the slave and to switch to and monitor the designated input only.

4.12 DPLL Switchover Management

4.12.1 Revertive and Non-Revertive Switching

All DPLLs supports revertive and non-revertive switching, the default being non-revertive. During the reference selection process, a DPLL selects the valid reference with the highest priority then the DPLL locks to that input clock. In case of non-revertive switching, the DPLL only switches to another, higher priority reference if the current reference becomes invalid. Non-revertive switching minimizes the amount of reference switches and therefore is the recommended mode.

If revertive switching is enabled and a higher priority clock becomes valid, then the DPLL will switch to that higher priority input clock unless that higher priority clock is designated as part of the same group (i.e. should be considered of equal priority).

4.12.2 Hitless Reference Switching

All DPLLs support Hitless Reference Switching (HS). HS is intended to minimize the phase change on the output clock when switching between input sources that may have different phases. When a DPLL switches input with HS enabled, it will first go into an internal holdover state (but not signal that externally), then the phase offset of the newly selected input clock with respect to the previous clock will be measured. The device then automatically compensates for the measured phase offset resulting in minimal disruption to the phase of the DPLL output clock.

The HS operation for a particular DPLL is triggered if any one of the following conditions occurs:

- DPLL is locked to an input clock and switches to a different input clock
- DPLL exits from Holdover mode
- There are several additional cases where hitless reference switching can be used in synchronization applications with physical and/or packet clocks. For more information about the particular application, contact Renesas.

For the two conditions, the maximum phase transient on the DPLL output clock with HS on is 250ps. Hitless reference switching can be enabled or disabled through register settings.

For 1PPS input clocks, if they have up to 100 ms of phase difference between them, then the maximum phase transient on the DPLL output 1PPS clock is 250 ps with HS on. If they have between 100 ms and 0.5 s of phase difference between them, then the maximum phase transient on the DPLL output 1PPS clock is 1 ns with HS selected.

4.12.3 Phase Slope Limiting

Phase Slope Limiting (PSL) can be enabled and independently programmed for each of the DPLLs. PSL is particularly useful in the initial locking to an input or during switchover between clock inputs. If PSL is enabled, then the rate of change of phase of the output clock is limited by the DPLL. The PSL settings for the device are very flexible, allowing any slope from 1ns/s to 65.536ms/s with a granularity of 1ns/s, including the values needed to meet Telecom standards as shown in Table 24.

Table 24. Some Key DPLL Phase-Slope Limits Supported

DPLL PSL	Description
unlimited	Limited by DPLL loop bandwidth setting
61 µs/s	Telcordia GR-1244 ST3
7.5 µs/s	G.8262 EEC option 1, G.813 SEC option 1
885 ns/s	Telcordia GR-1244 ST2, ST3E, and ST3 (objective)

4.12.4 DPLL Frequency Offset Limit Setting

Each DPLL has an independent setting to limit its maximum frequency range This setting is used in conjunction with the advanced reference monitoring to provide pull-in / hold-in limit enforcement as required in many telecom standards. It will also limit the frequency deviation during locking, during holdover and while performing switchovers. This limit must be set wide enough to cover the expected frequency range of the input when locking.

4.12.5 DPLL Fast Lock Operation

Each DPLL also has the ability to support a Fast Lock function. There are two options the user can choose from to perform the fast lock:

- Frequency Snap
- Phase Snap
- Open-loop phase pull-in (mutually exclusive with Phase Snap)
- Wide Acquisition Bandwidth

Any of the options can be independently enabled or disabled, and selected to be applied when the DPLL is in either the LOCKACQ state or the LOCKREC state. Although the options are mutually exclusive, the order of precedence is as listed (with frequency snap being the highest).

The frequency and phase snap options are recommended for locking to mid-kHz-range input clocks or lower. For frequency snap, the RC32012A will measure the input clock from the current DPLL operating frequency, determine an approximate frequency offset and digitally write that directly to the steerable FOD block, causing the output frequency to snap directly to the correct output frequency. The frequency snap can be optionally limited using a Frequency Slope Limit (FSL). For the phase snap and the open loop phase pull-in options, the measurement is used to determine the phase offset. With phase snap, the phase is snapped to the correct value; with open loop pull-in, the DPLL's PFD & LPF are temporarily isolated to allow for an unfiltered phase pull-in to the correct value. The combination of these methods will achieve lock very quickly, but there may be severe disruptions on the output clock while locking occurs; mainly due to the frequency/phase snaps.

The wide acquisition bandwidth option uses the DPLL in a normal operating mode, but with temporary relaxation of items like DPLL loop bandwidth, phase slope limits (PSL) or damping factor until lock is achieved. At that point, the normal DPLL limits are resumed. The user is able to control what limits are to be applied. In addition, for LOCKACQ state only, the DPLL's bandwidth may be temporarily opened to its maximum for a short duration of time (in ms); with the temporary phase slope limit still being applied. This pre-acquisition option is applied before the wide acquisition bandwidth option. These methods are recommended for higher frequency signals since it results in fewer perturbations on the output clock. It also allows the user to trade-off the level of changes on the clock during the locking process versus the speed of locking.

4.13 Digitally-Controlled Oscillator Operation via External Control

The DPLL channel may be operated as an externally-controlled DCO. There are several different control methods that can be used depending on the application needs. Each is described individually in the following sub-sections. Phase and/or frequency updates will be calculated using external methods and written into the RC32012A over the serial port.

4.13.1 Write-Frequency Mode

For the DPLL channel in this mode a Frequency Control Word (FCW) is used to adjust the frequency output of the DCO (by steering the FOD) and the phase detector and loop filter are essentially bypassed. All the filtering is done by an external device and the frequency offset written into the Write Frequency Configuration register is passed on directly to the output clocks. This is shown in Figure 12. When applied, the FCW will not cause any missing pulses or glitches in the output clock, although a large frequency jump may cause issues with devices receiving this clock. The output will remain at this frequency until a new FCW is written.

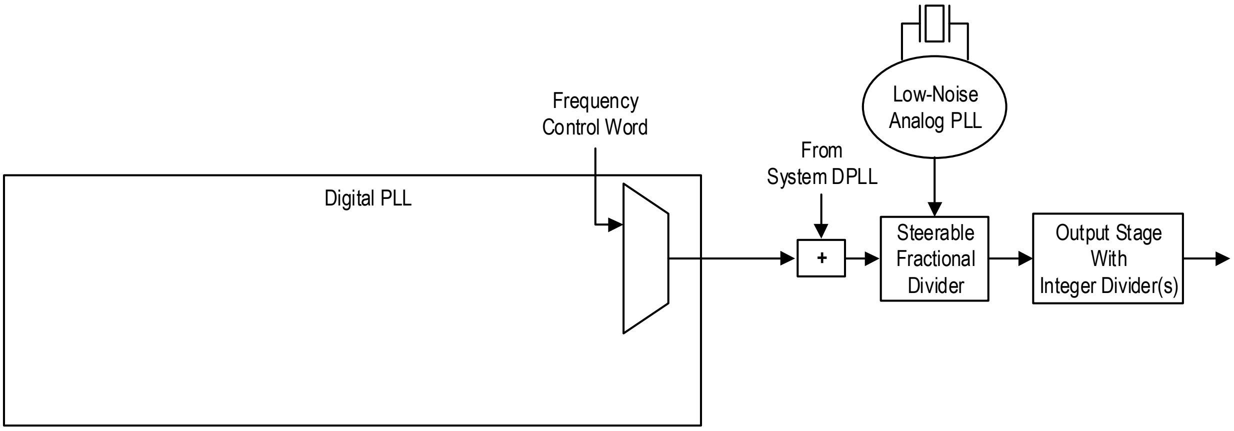


Figure 12. External DCO Control via Frequency Control Word

The FCW is a 42-bit 2's-complement value. The FCW has a granularity of 1.11x10^{-10}ppm and a full range of +244.20ppm to -244.08 ppm of the nominal DCO frequency. A positive value will increase the output frequency and a negative one will decrease the output frequency. The formula for calculation of the FCW from the fractional frequency offset (FFO) is:

$$FCW = \left(1 - \frac{1}{\left(1 + \frac{FFO}{10^6}\right)}\right) \times 2^{53}$$

Where,

FFO = Fractional Frequency Offset, in ppm
FCW = Frequency Control Word (Positive or Negative Integer)

The value resulting from the above calculation must be converted to a 42-bit 2's complement value and then sign-extended to 48-bits to be written into the register.

Write frequency mode may be used to make phase changes on the output. For fine resolution, phase changes are done by controlling the DCO's frequency. Coarse phase adjustments should be done by snap-alignment method by using the Phase Offset registers. Using the Phase Offset registers is referred to as the snap-alignment method since the output will snap directly to that new phase rather than moving smoothly to it over time. The snap-alignment method provides fast coarse phase alignments and therefore it should be used to bring the phase close to the desired value and then use the DCO in write frequency mode to fine tune it. Since write frequency mode is changing the frequency, the phase will move smoothly over time without any jumps.

4.13.2 Increment / Decrement Registers and Pins

The DCO frequency update can also be done by applying a preset frequency offset value to be added or to be subtracted from a cumulative FCW value. The cumulative FCW value behaves as described in the previous section.

Once the individual frequency offset values are configured for all applicable DCOs, then a single 16-bit register can be written over the serial port and cause an increment or decrement frequency offset to be applied to one or more DCOs with a single register access. Subsequent accesses to this register can apply additional frequency offsets to any or all DCOs.

Alternatively, one or more GPIO pins can be configured to perform the increment or decrement frequency offset function on a specific DCO. For information on how to configure the GPIOs, see General Purpose Input/Outputs (GPIOs).

4.13.3 Write-Phase Mode

In this mode of operation for the DPLL channel, shown in Figure 13, the Phase Control Word (PCW) is written by the external control logic over the serial port to directly control the DCO phase with hardware controlled bandwidth (e.g. 0.1Hz per G.8273.2) and phase slope limiting. In this mode, the DPLL loop bandwidth and the phase slope limiting are programmable and will affect the output phase as it is adjusted.

The PCW applied to the Digital Loop Filter is equivalent to applying a phase error measured by the on-chip Phase / Frequency Detector to the Digital Loop Filter when the DPLL is operating in closed loop. The update rate needs to be at least 60 times the loop filter bandwidth. As an example, for 0.1Hz, the update should be greater than 6Hz.The rate of adjustment of phase on the DCO output is controlled by Digital Loop Filter settings. For information on configuring related DPLL parameters such as loop bandwidth and phase slope limiting, see DPLL Operating Modes. This method allows a better control of the output clock since all parameters are controlled in hardware. This makes it easier to meet telecom specifications such as G.8273.2 (G.8273.2 specifies the T-BC bandwidth to be between 0.05Hz and 0.1Hz). This change will not cause any missing pulses or glitches in the output clock. Also, because the output frequency is changed only at a rate determined by the loop filter, this should not cause any issues, if properly configured, with devices receiving this clock.

Note that the PCW must be reduced over time or the DPLL will continue to adjust the DCO frequency to remove the “phase error”. This can be adjusted by external software.

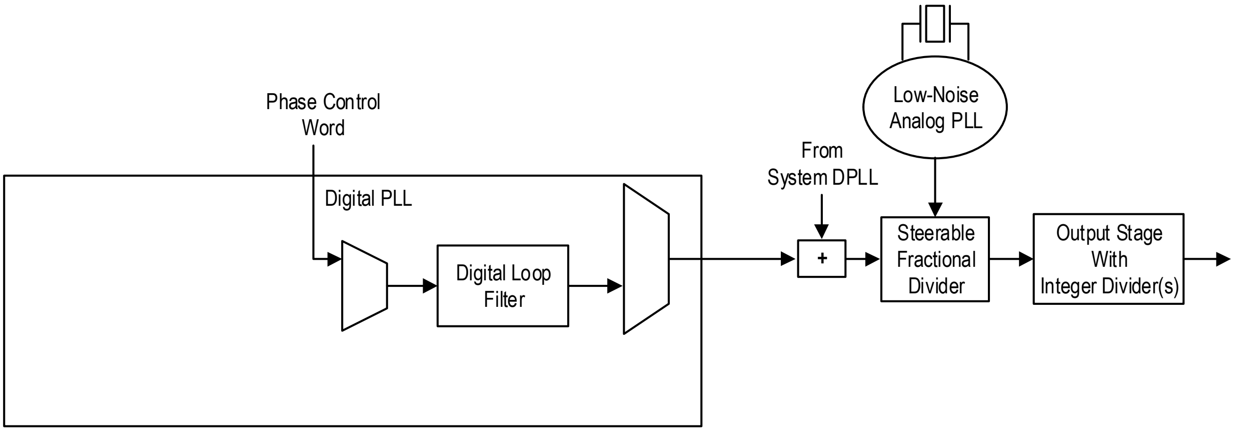


Figure 13. External DCO Control via Phase Control Word

To assist in the above, there is an optional timer associated with the PCW. This allows a phase control word to be applied for a limited period of time after which it will automatically be reset to zero or be placed into holdover by the RC32012A, and therefore it will avoid the DCO continuing to apply the phase adjustment indefinitely until it reaches its tuning range limits. The timer value is a 16-bit integer that has a granularity of 1 millisecond and a full range of up to 65.535 seconds.

The PCW is a 32-bit 2’s-complement value. The resolution of the PCW is 50 ps and the range is ±107.3741824 ms. Writing a positive value will result in the output frequency getting faster. This will shorten the clock periods, moving the clock edges to the left as seen on an oscilloscope. A negative value will slow the output frequency.

4.13.4 Adjusting Phase while in Closed Loop Operation

There may be usage scenarios that require adding a phase offset from an external software-controlled process to an output clock that is locked to an input clock. That function can also be supported as shown in Figure 14. In this mode, the amount of phase offset needed consists of two components. The first is dependent on which input the DPLL is locked to. So a phase offset register is provided for each input to allow individual offsets to be specified per-input. The second part of the phase offset configuration is for each DPLL. There is a register for each DPLL that allows for another offset value to be specified that is independent of which input is active. The actual Phase Offset Value applied will be calculated by the RC32012A using the per-input phase offset value for the currently active input summed with the phase offset value for the DPLL channel. During input reference switching, this value will be automatically recalculated at any switchover and applied as shown. Note that if an input is used on multiple DPLL channels, it may not be possible to maintain unique values per-input-per-DPLL. The calculated offset value is then summed with the measured phase error for that channel (phase difference between input reference and feedback value) to drive the DPLL to the desired phase.

The Phase Offset Value applied to the Digital Loop Filter is equivalent to applying a phase error measured by the on-chip Phase / Frequency Detector to the Digital Loop Filter when the DPLL is operating in closed loop.

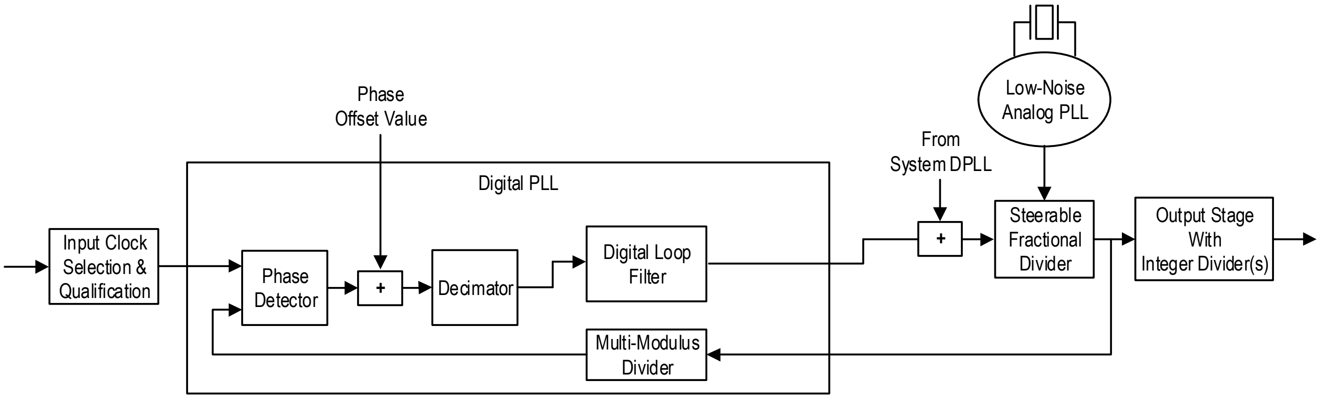


Figure 14. Phase Control in Closed Loop Operation

4.14 DPLL Lock Detector

The DPLL lock detector declares lock when the phase from the phase detector remains within a programmable range for a programmable time interval both of which are set in the register map. This indicates that the DPLL is locked to the reference clock input. If the phase detector output is below the lock threshold for half of the programmed lock interval, the internal lock signal is asserted and the normal loop filter bandwidth and damping applied to the DPLL's loop filter instead of the acquire filter settings.

4.15 Output Dividers

The RC32012A provides four fractional output dividers (FOD) and 12 integer output dividers (IOD).

4.15.1 Integer Output Dividers

All 12 IODs are identical and derive their input clock from the output of either of the four FODs. Each IOD uses a 32-bit divider to provide output frequencies from 0.5Hz to 1GHz. Changing IOD values results in an immediate change to the new frequency. Glitch-less squelch and release of the IOD clock is supported. When enabled, this mimics a gapped clock behavior when an IOD frequency is changed.

4.15.1.1 SYSREF Generation

The RC32512A supports continuous mode SYSREF generation within each IOD. Additional coarse delay adjust is available per IOD channel with a step size of one FOD output clock period.

4.15.2 Fractional Output Dividers

There are four fractional output dividers (FOD) with FOD_0 as a part of DPLL/DCO in Jitter Attenuator mode. Each FOD can divide down either the APLL VCO clock or the DPLL output clock to provide frequencies of 500MHz to 1GHz. The fractional divide value involves two unsigned integer values, representing the integer (INT) and fraction (FRAC) portion of the divide ratio. The fraction portion is an integer representing the 43-bit numerator of a fraction, where the denominator of that fraction is fixed at 2^{43}. The equation for the FOD output frequency is as follows.

$$f_{FOD} = \frac{f_{APLL}}{\left(INT + \frac{FRAC}{2^{43}}\right)}$$

Note: Fractions that approach 0, 1, or 1/2 can result in increased phase noise on the output signal due to integer-boundary spurs. It is recommended that APLL frequency and FOD divider settings be coordinated to avoid such fractions.

4.15.2.1 Output Phase Adjustment

Fine phase adjustments of the FOD output can be performed by increasing or decreasing the frequency of operation of the FOD for a period of time. This results in the clock edges of the FOD output clock being advanced (increased FOD output frequency will move edges to the left as seen on an oscilloscope relative to some fixed reference point) or delayed (decreased FOD output frequency moves edges to the right) by some amount.

Coarse phase adjustments of the IOD output can be performed, and is the same as FOD phase adjustment but with a step size of one FOD output clock period.

4.15.2.2 Digital Controlled Oscillator (DCO) Mode

In DCO mode, a frequency control word (FCW) is passed directly from an external processor or FPGA to the DPLL with a step size of 1.11×10^{-10}ppm and a full range of +244.20ppm to -244.08 ppm of the nominal DCO frequency. A positive value will increase the output frequency and a negative one will decrease the output frequency. The formula for the calculation of the FCW from the fractional frequency offset (FFO) is as follows:

$$FCW = \left(1 - \frac{1}{\left(1 + \frac{FFO}{10^6}\right)}\right) \times 2^{53}$$

Where,

FFO = Fractional Frequency Offset, in ppm
FCW = Frequency Control Word (Positive or Negative Integer)

4.15.2.3 Numerically Controlled Oscillator (NCO) Mode

In NCO mode, each FOD in open-loop, except for FOD_0 in Jitter Attenuator mode, can adjust its output clock frequency with a step size of $(1/2^{43})/N$ where N is the nominal fractional output divide value, and is based on incrementing the numerator where the denominator of that fraction is fixed at 2^{43}. This frequency change at the output clock is gradual without glitches. The device can be in either Clock Generator mode or in Jitter Attenuator mode.

4.16 Clock Outputs

The RC32012A supports up to 12 differential or 24 single-ended clock outputs or any combination of differential and single-ended clock outputs. Every differential clock output can be programmed as two single-ended clock outputs.

4.16.1 Output Buffer in Single-Ended Mode

When used as a single-ended output buffer, two copies of the same output clock are created with LVCMOS output levels. Each clock will have the same frequency, phase, voltage, and current characteristics. The only exception is that the user can program the clock from the nQx output pad to be inverted in phase relative to the one coming from the Qx output pin. The non-inverted setting can result in greater noise on these outputs and increased coupling to other output clocks in the device, so it should be used with caution.

In this mode of operation, the output buffer supports 1.8V, 2.5V, or 3.3V V_{DDO_Qx} voltages. An output swing of 1.2V or 1.5V is supported from the V_{DDO_Qx} voltage of 1.8V. For each output voltage, there are four impedance options that can be selected from.

4.16.2 Output Buffer in Differential Mode

When used as a differential output buffer, the user can control the output voltage swing (V_{OVS}) and common mode voltage (V_{CMR}) of the buffer. Which V_{OVS} and V_{SWING} settings can be used with a particular V_{DDO_Qx} voltage are listed in Table 25. Note that V_{DDO_Qx} options of 1.5V or 1.2V cannot be used in differential mode.

Table 25. Configurable Output Mode Options

V_{DDO_Qx}	V_{OVS} Options Supported	V_{CMR} Options Supported
3.3V	410mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V
	600mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V, 2.3V
	750mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V, 2.1V
	900mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V, 1.9V
2.5V	410mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V
	600mV	0.9V, 1.1V, 1.3V, 1.5V, 1.7V
	750mV	0.9V, 1.1V, 1.3V, 1.5V
	900mV	0.9V, 1.1V, 1.3V
1.8V	410mV	0.9V, 1.1V, 1.3V
	600mV	0.9V, 1.1V, 1.3V
	750mV	0.9V, 1.1V, 1.3V
	900mV	0.9V, 1.1V

4.16.3 Output Banks

The RC32012A maps the internal and external frequency sources to output banks, that can be programmed in the register map, according to Table 26. There are up to 12 clock outputs that can be derived from each of the four FODs.

Table 26. Output Bank Assignment

Output Pins	FODs that can Drive this Stage
Q0 / nQ0, Q1 / nQ1	FOD_0
Q2 / nQ2, Q8 / nQ8	FOD_5
Q3 / nQ3, Q4 / nQ4, Q5 / nQ5, Q9 / nQ9, Q10 / nQ10	FOD_0, FOD_2, FOD_5
Q6 / nQ6	FOD_2, FOD_7
Q7 / nQ7, Q11 / nQ11	FOD_7

4.17 General Purpose Input/Outputs (GPIOs)

The GPIO signals are intended to provide a user with a flexible method to manage the control and status of the part via pins without providing dedicated pins for each possible function that may be wasted in a lot of applications. The GPIOs are fully configurable so that any GPIO can perform any function on any target logic block.

4.17.1 GPIO Modes

Each of the GPIO pins may be individually configured to operate in one of the following modes. Note that these modes are effective only once the RC32012A has completed its reset sequence. During the reset sequence one or more of these pins may have different functions as outlined in the Use of GPIO Pins at Reset section:

- General Purpose Input - in this mode of operation, the GPIO pin will act as an input whose logic level will be monitored and reflected in an internal register that may be read over the serial port. This is the default mode if no other option is programmed in OTP or EEPROM.
- General Purpose Output - in this mode of operation, the GPIO pin will act as an output that is driven to the logic level specified in an internal register. That register may be written over the serial port.
- Alarm output - In this mode of operation, the GPIO pin will act as a single-purpose alarm or Alert (aggregated alarm) output. For information on when an alarm output will be asserted or released and alarm sources, see Alarm Output Operation. Note that each GPIO can be independently configured and so if multiple GPIOs are configured the same way, they will all have the same output values.
  - Loss-of-Signal status - in this mode of operation, the GPIO pin will act as an active-high Loss-of-Signal output. When the GPIO output is asserted, that indicates the selected input reference monitor is indicating an alarm condition. The related reference monitor and the associated GPIO pin are configured via registers. Configuration of the reference monitor will determine what constitutes an alarm. Note that the GPIO output reflects the actual state of the alarm signal from the selected reference monitor. This is not a latched or ‘sticky’ signal. Note that this is different than the other alarm sources below.
  - Loss-of-Lock status - in this mode of operation, the GPIO pin will act as an active-high Loss-of-Lock output. When the GPIO output is asserted, that indicates the System APLL or DPLL has lost lock. The related PLL channel and associated GPIO pin are configured via registers. Note that the GPIO output reflects the ‘sticky’ state of the alarm signal from the selected PLL channel. This is a latched or ‘sticky’ signal and so must be cleared by register access to the ‘sticky’ bit clear register to remove the alarm signal.
  - Holdover status - in this mode of operation, the GPIO pin act as an active-high Holdover status. When the GPIO output is asserted, that indicates the DPLL for the selected PLL channel has lost all its input references and is in a holdover state. The related PLL channel and associated GPIO pin are configured via registers. Note that the GPIO output reflects the ‘sticky’ state of the alarm signal from the selected PLL channel. This is a latched or ‘sticky’ signal and so must be cleared by register access to the ‘sticky’ bit clear register to remove the alarm signal.
  - Alert (aggregated alarm) status - In this mode of operation, the GPIO will act as the logical OR of all alarm indicators that are enabled to drive this output. Only ‘sticky’ bits are available to drive the GPIO in this mode. This output will be asserted if any of the ‘sticky’ bits are asserted and enabled to cause the Alert (aggregated alarm). To clear this output, all contributing ‘sticky’ bits must be individually cleared This output will be active-high to indicate one or more alarms are asserted.
- Output Disable control - in this mode of operation, the GPIO pin will act as a control input. When the GPIO input is high, the selected output clock(s) will be disabled, then placed in high-impedance state. When the GPIO pin is low, the selected output clock(s) will be enabled and drive their outputs as configured. Selection of which output(s) are controlled by which GPIO(s) is configured via registers over the serial port or by OTP or EEPROM at reset. Each GPIO can be configured to control any or all outputs (or none). So all combinations can be setup from a single GPIO controlling all outputs, to all outputs responding to individual GPIO signals and any grouping in between.
- Single-ended Input Clock - in this mode of operation a single-ended input clock may be applied to certain GPIOs that map to specific input stages. This may be used if extra single-ended inputs are needed due to all

input reference clock pins are taken-up by differential input references. This mode can not be used if an input stage already has two single-ended input references from the CLKx/nCLKx input pins.

- Manual Clock Selection control - in this mode of operation, the GPIO pin acts as an input that will manually select between one of two inputs for a specific DPLL channel. The specific input references and the PLL channel must be pre-configured via registers. Assertion of the GPIO will select the higher priority input and de-assertion will select the lower priority input.
- DCO Increment - in this mode of operation, the GPIO pin will act as an increment command input pin for a specific channel configured as a DCO. The rising edge of the GPIO pin will cause an increment function on the indicated DCO. The amount of the increment and the related DCO to increment must be previously configured via registers.
- DCO Decrement - in this mode of operation, the GPIO pin will act as an decrement command input pin for a specific channel configured as a DCO. The rising edge of the GPIO pin will cause an decrement function on the indicated DCO.The amount of the decrement and the related DCO to decrement must be previously configured via registers.

4.17.2 GPIO Pin Configuration

The GPIO pins are all powered off a single voltage supply that only supports 1.8V operation. An internal register must be set to indicate 1.8V. This setting is a global one for all GPIOs.

In addition, each GPIO can be enabled or disabled under register control. If enabled and configured in an operating mode that makes it an output, the user can choose if the GPIO output will behave as an open-drain output or a CMOS output. The open-drain output drives low, but is pulled high by a pull-up resistor. There is a very weak pull-up internal to the RC32012A, but an external pull-up is strongly recommended. In CMOS mode, the output voltage will be driven actively both high and low as needed. Register control may also enable a pull-up (default) or pull-down.

4.17.3 Alarm Output Operation

There are many internal status and alarm conditions within the RC32012A that can be monitored over the serial port by polling registers. Several of these can be directed to GPIO pins. In addition there is the ability to designate one of the GPIOs as an Alert (aggregated alarm) output signal called an Alert output.

The RC32012A provides both a ‘live’ and a ‘sticky’ status for each potential alarm condition. A ‘live’ bit shows the status of that alarm signal at the moment it is read over the serial port. A ‘sticky’ bit will assert when an alarm condition changes state and will remain asserted until the user clears it by writing to the appropriate clear bit over the serial port. When a GPIO is configured to show the status of a specific alarm, it will show the ‘live’ or sticky status of that alarm, depending on the specific alarm, where a high output on the GPIO indicates the alarm is present.

The Alert (aggregated alarm) output logic only uses the ‘sticky’ status bit for alarms. This ensures when a software routine reads the RC32012A there will be an indication of what caused the alarm in the first place. Note that there can be multiple sticky bits asserted. Table 27 shows the alarm conditions possible within the RC32012A. Note that the reference monitor, the DPLL, and the System DPLL blocks can generate the indicated alarms.

Table 27. Alarm Indications

Logic Bloc	Specific Alarm	Conditions for Live Alarm[1] to Assert	Conditions for Live Alarm[1] to Negate[2]
Reference Monitoring	Frequency Offset Limit Exceeded	When reference monitor indicates reference frequency above the rejection range.	When reference monitor indicated reference frequency within acceptance range.
	Loss-of-Signal	When reference monitor indicates reference period above the threshold.	When reference monitor indicates reference period below the threshold.
	Activity Alarm	When reference monitor indicates reference frequency above the threshold. NOTE: Activity alarm is not as accurate as frequency offset limit monitor but is quicker to report.	When reference monitor indicates reference frequency below the threshold. NOTE: Activity alarm is not as accurate as frequency offset limit monitor but is quicker to report.
DPLL[3][4]	Holdover	DPLL has entered / is in the Holdover state	DPLL no longer in Holdover state
	Locked	DPLL has entered / is in the Locked state and System APLL is in the Locked state	DPLL and/or System APLL no longer in the Locked state

1. ‘Sticky’ alarm bits are set whenever the associated live alarm changes state. So there will be a new ‘sticky’ alarm on both assertion and negation of the appropriate live alarm indication.
2. Only the ‘live’ status will negate by itself. The ‘sticky’ needs to be explicitly cleared by the user.
3. For the Digital PLL, ‘sticky’ alarms are raised when the state machine transitions into specific states and ‘live’ status indicates that the Digital PLL is currently in a specific state. The user is able to read the current state of the Digital PLL state machine from status registers over the serial port.
4. This includes the System DPLL, as well as all Digital PLL.

For each of the alarm types in each of the logic blocks that can generate them, there is a ‘live’ status, a ‘sticky’ status, a ‘sticky’ clear control and a series of control bits that indicate what effects the alarm will have. When the ‘live’ status asserts, the ‘sticky’ status will also assert. If so configured via registers, that alarm may generate and external signal via GPIO. That signal may be an individual alarm output or an Alert (aggregated alarm). Once external software responds, it is expected to read the sticky status bits to determine the source(s) of the alarm and any other status information it may need to take appropriate action. The ‘sticky’ clear control may be used to clear any or all of the bits that contributed to the alarm output being asserted.

In addition to the above controls and status, each potential alarming logic block has its own controls and status. Each of the reference monitors has a ‘sticky’ status bit, a ‘sticky’ clear bit and various control bits. The DPLL and system DPLL each have a ‘sticky’ status bit, a ‘sticky’ clear bit, control bits and a PLL state status field. These functions behave as described in the previous paragraph. Note that both the individual alarm ‘sticky’ status and the logic block ‘sticky’ status must be cleared to fully remove the source of the alarm output. Individual ‘sticky’ alarms should be cleared first so that all individual alarms associated with a logic block won’t cause a re-assertion of the block ‘sticky’ alarm.

There are also several configuration bits that act on the alarm output logic as a whole. There is a global alarm enable control that will enable or disable all alarm sources. This may be used during alarm service routines to prevent new alarms while that handler is executing in external software. There is also the ability to designate a GPIO as an Alert (aggregated alarm) output and determine which individual alarms will be able to drive it.

4.18 Device Initial Configuration

During its reset sequence, the RC32012A will load its initial configuration, enable internal regulators, establish and enable internal clocks, perform initial calibration of the Analog PLL and lock it to the reference on the OSCI / OSCO pins. Depending on the initial configuration it may also bring-up Digital PLLs, lock to input references including any OCXO/TCXOs and generate output clocks.

There are four mechanisms that may be used to establish the initial configuration during the reset sequence:

- State of certain GPIO pins (see Table 28) at the rising edge of the nMR signal,
- Configuration previously stored in One-Time Programmable memory,
- Configuration stored in an external I^2C EEPROM,
- Default values for internal registers.

Each of these will be discussed individually in the following sections and then integrated into the reset sequence.

4.18.1 Use of GPIO Pins at Reset

Several of the device GPIO pins are sampled at the rising edge of the nMR (master reset) signal and used in setting the initial configuration. Table 28 shows which pins are used to control what aspects of the initial configuration. All of these register settings can be over-written later via serial port accesses.

Table 28. GPIO Pin Usage at Start-Up

GPIO Number	Function	Internal Pull-up or Pull-down
9	0 = Device uses SPI protocol 1 = Device uses I^2C protocol	Pull-up
4 pins user selectable[1]	Identifies which stored configuration in OTP to use for initial configuration (has no effect with “-000” unprogrammed devices). See details just below this table	Pull-up
1 pin user selectable[1]	Disables EEPROM accesses during start-up sequence By default, no GPIO is used for this purpose, so the device will attempt to find an external EEPROM to check for additional start-up information by default. See details just below this table	Pull-up
1 pin user selectable[1]	Provides pin control for I^2C slave serial port (for serial port selected by GPIO[9] as I^2C) default base address bit A2. Has no effect on serial port selected as SPI. By default no GPIO is used for this purpose, so the default I^2C slave port base address will have a 0 for bit A2. See details just below this table	Pull-up

1. Selection of this mode for a GPIO is performed using the Device Information block in the OTP memory, which is programmed by Renesas at the factory for dash codes that are non-zero. “-000” dash code devices are considered unprogrammed and so will have the default behavior indicated above.

Any of the available GPIOs may be used as:

- I^2C base address bit A2

  This is for the serial port, whichever is selected as I^2C during the start-up sequence using GPIO[9]. If no GPIOs are configured in this mode, bit A2 of the slave serial port base address will be zero. The value of the I^2C base address and the serial port configuration can be over-written by SCSR configuration data or serial port accesses later in the start-up sequence. If more than one GPIO is programmed with this functionality, only the one with the highest index will be used.

- EEPROM Access Disable control

  A high input value on a GPIO programmed with this function prevents device from attempting to read device update information or SCSR configuration data from an external I^2C EEPROM. This will speed-up device reset time, but prevents access to updated information that may be stored in EEPROM. If no GPIOs are configured in this mode, then the device will attempt to locate an external EEPROM at the appropriate point in the start-up sequence. If multiple GPIOs are configured to perform this function, then any one of them being active will disable EEPROM accesses, so it is recommended that no more than one GPIO be programmed for this function.

- Default Configuration Select control

  If no GPIOs are selected then GPIO[3:0] will be assumed and the value on those pins at the rising edge of the nMR signal will be used to select which of the SCSR configurations in OTP memory is to be used. Note that since a GPIO is pulled-up by default, unless these pins are pulled or driven low during the reset period, this will select SCSR Configuration 15.

  If one or more GPIOs are selected for this function, then the value on those pins at the rising edge of nMR will be used to select the SCSR configuration to be loaded. The Device Information block of the OTP may be configured to select any of up to four GPIO pins to be used for this purpose if the default GPIOs are not convenient. The GPIOs chosen do not have to be sequential, but whichever ones are chosen, the one with the lowest index number will be the LSB and so on in order of the index until the GPIO with the highest index is the MSB. No GPIO that appears elsewhere in this table should be used for this purpose.

  If less than four GPIO pins are selected, then the selected GPIOs will be used as the least-significant bits of a 4-bit selection value, with the upper bits set to zero. If more than four GPIOs are programmed for this function, then the GPIOs will form a larger bit-length word for selection of internal configuration.

4.18.2 Default Values for Registers

All registers are defined so that the default state (without any configuration data from OTP or EEPROM being loaded) will cause the device to power-up with none of the outputs enabled and all GPIO signals in General-Purpose Input mode. Users can then program any desired configuration data over the serial port once the reset sequence has completed.

4.19 One-Time Programmable (OTP) Memory

The RC32012A contains a 32KB One-Time Programmable (OTP) memory block. The term “one-time programmable” refers to individual blocks within the memory structure. Different blocks can be programmed at different times, but each block can only be programmed once. The data structure within the OTP is designed to facilitate multiple updates and multiple configurations being stored, up to the limit of the physical memory space. At this time, OTP can only be programmed within Renesas.

After reset of the RC32012A, all internal registers are reset to their default values, then OTP contents are loaded into the device’s internal registers. A Device Information block programmed by Renesas at Final Test will always be loaded. This provides information that is specific to the device, including product ID codes and revision information. In addition there are zero or more device configurations stored in the OTP by Renesas at the factory if a special dash-code part number is requested. Certain GPIO pins are sampled at the rising edge of the external nMR input signal. The state of those pins at that time will be used by the RC32012A to determine which of up to 16 configurations stored in the OTP to load into the device registers. For information on how to select a configuration, see Use of GPIO Pins at Reset.

Storage of configuration data in OTP does not require having a value stored for every register in the device. Register default values are defined to ensure that most functions will be disabled or otherwise made as neutral as possible. This allows only features that are being used in any particular configuration (and their associated trigger registers as defined in the 8A3xxxx Family Programming Guide) to need to be stored in OTP for that configuration. The intent of this is to minimize the size a configuration takes in OTP to allow more configurations to be stored there. For this reason, the exact number of configurations store-able in OTP can't be predetermined. There will be a minimum of 2 configurations and a maximum of 16 configuration capacity in the OTP.

Part numbers with -000 as the dash code number are considered 'unprogrammed' parts, but will come with at least a Device Information block pre-programmed with Renesas-proprietary information including parameters needed to successfully boot the device to the point where it can read its configuration data. One Device Update block may also be programmed if determined to be appropriate by Renesas.

Custom user configurations indicated with non-zero dash code part numbers will in addition have one or more SCSR Configuration sections pre-programmed as indicated in the datasheet addendum document for that particular dash code part number.

Note that a programmed configuration, Device Information block or Device Update block may be invalidated via the OTP programming interface and if sufficient OTP space remains a new one added to replace it. Note that this does not erase or remove the original data and the space it consumes. It just marks it to be ignored by the device. This allows for a limited ability to update a device in the field either from a device functional update or configuration data perspective. This is a purely software-driven process handled over the serial port. For support if this type of in-field upgrade / change is desired, contact Renesas. Note that the ability to perform this type of in-field update is highly dependent on the size of the change versus the remaining space in OTP, so will not be possible in all cases.

4.19.1 Configuration Data in OTP

Users are able to program multiple configurations into the internal One-Time Programmable memory. The Timing Commander GUI Software can perform this function. Please contact Renesas for sample code if this needs to be performed in another way by the end-user. By using the GPIO pins at start-up as outlined in the Use of GPIO Pins at Reset, one of those configurations can be chosen for use as the initial values in the device registers after reset. Register values can be changed at any time over the serial port, but any such changes are not stored in OTP and will be lost on reset or power-down.

The OTP is organized so that only configuration data that changes from the register default values needs to be stored. This saves OTP space and allows the potential for more configurations to be stored in the OTP.

If the indicated configuration in OTP has a checksum error, it will not be loaded and registers will be left at their default values.

4.19.2 Configuration Data in External I^{2}C EEPROM

As a final option, the initial configuration may be read from one or more external I^{2}C EEPROMs. The Timing Commander GUI Software can generate the necessary EEPROM load information as an Intel HEX file for this purpose. The RC32012A will search each EEPROM for a valid configuration data block (valid header and checksum). The first valid block found will be loaded into internal registers after checksum validation. The search will terminate after the first valid block is found and loaded. This means that only a single valid configuration block can be stored via the EEPROM method.

The RC32012A will look for EEPROMs at I^{2}C base addresses of 1010xxx (binary), and search each EEPROM from the lowest address to the highest. When the device searches for an EEPROM configuration, it will check for a valid block at address offsets 0x0000 and 0xF000 within an EEPROM. If using this configuration method, see the warning in Step 5 – Search for Configuration in External EEPROM.

4.20 Reset Sequence

Figure 15 shows the relationship between the master reset signal (nMR) and the supply voltages for the RC32012A. There are no power sequencing requirements between the power rails, so V_{DD} in the diagram represents any of the supply voltages. To ensure there is no anomalous behavior from the device as it powers-up, it is recommended that the nMR signal be asserted (low) before any voltage supply reaches the minimum voltage shown in the figure. nMR should remain asserted until a short hold time (t_{HOLD} ~10nsec) after all supply voltages reach the operating window of 95% of nominal voltage. nMR must be asserted or the device will not function correctly after power-up.

One additional consideration is that once minimum voltage is reached on all voltage supplies, internal regulators and voltage references will take up to 3µsec to reach stability. If the time t_{RAMP} shown in the figure is less than the voltage regulator startup time of 3µsec, then release of nMR should be delayed.

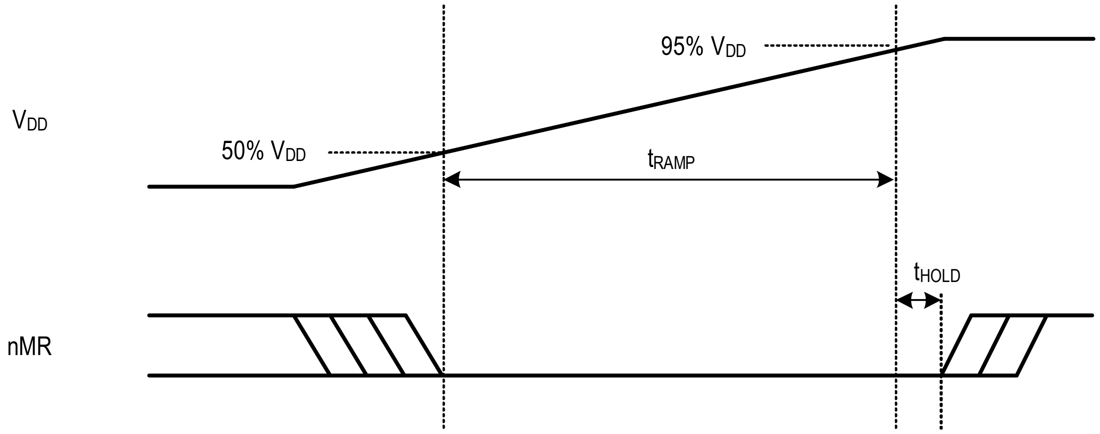


Figure 15. Power-Up Reset Sequencing

In cases where the device is not powering-up and just being reset, a low pulse on nMR of 20 ns will be sufficient to reset the device.

The reset sequence discussed below will begin from the rising (negating) edge of the nMR (master reset) signal.

4.20.1 Step 0 – Reset Sequence Starting Condition

Once power rails reach nominal values and the nMR signal has been asserted, the RC32012A will be in the following state:

- All Qx / nQx outputs will be in a high-impedance state
- All GPIO pins will be set to General-Purpose Inputs, so none will be driving the output
- The serial port protocols are not set at this point in the reset sequence, so the ports will not respond.
- OTP will be checked for any device patch information and if any is found, it will be loaded and the device reinitialized.
- Device Information block loaded from internal OTP to configure what GPIOs will be used for what start-up functions in Step 1.

4.20.2 Step 1 – Negation of nMR (Rising Edge)

At the rising edge of the nMR signal, the state on the GPIO pins at that time is latched. After a short hold time, the GPIOs can release their reset levels and assume their normal operation modes. The latched values will be used in later stages of the reset sequence.

4.20.3 Step 2 – Internally Set Default Conditions

An internal image of all the device registers will be created in internal RAM with all registers set to their default values. This will not result in any changes to the GPIO or output clock signals from their Step 0 condition.

Based on the serial port protocol selection made via the GPIO pin in Step 1, serial port configuration will be completed as indicated by the GPIO input pin. If SPI mode is selected by the GPIO, the register default values will configure it to use 4-wire SPI mode.

4.20.4 Step 3 – Scan for Device Updates in EEPROM

Unless a GPIO is configured to control this in Step 0 and in Step 1 is sampled in the state requesting no EEPROM read, this step will be performed by the RC32012A. The RC32012A will use the I^{2}C Master port (if available) to check for device functional update information. If such information is found, it will be loaded, the device functionality updated and then the part will reinitialize to Step 0.

4.20.5 Step 4 – Read Configuration from OTP

Using the GPIO values latched in Step 1, the device will search the internal One-Time Programmable memory for the indicated configuration number. If no such configuration is found or the configuration has an invalid checksum, the device will skip to Step 6. Any errors in this process will be reported. If loading from OTP was successful, which configuration number was loaded will be reported.

If the requested configuration is found and is valid, the device will load the registers indicated in the configuration data with the stored data values in the internal register image. Any register not included in the configuration data set will remain at its default value in the register image.

Note: Many register modules have explicitly defined trigger registers that when written will cause the other register settings in that module to take effect. Users must ensure that the configuration in OTP will cause a write to all applicable trigger registers, even if that register's contents would be all zero. Multi-byte register fields also require all bytes of the field to be written to ensuring triggering. For information about which trigger registers are associated with which other registers, see the *8A3xxxx Family Programming Guide*.

The contents of several of the registers will be used to guide the remainder of the reset sequence.

- If the APLL feedback divider value was programmed in this step, perform APLL calibration in parallel with remaining reset activities.
- Re-configure serial ports to use I^{2}C or SPI protocols as indicated (for information, see the I2C Slave Operation or SPI Operation).

4.20.6 Step 5 – Search for Configuration in External EEPROM

Unless a GPIO is configured to control this in Step 0 and in Step 1 is sampled in the state requesting no EEPROM read, this step will be performed by the RC32012A.

The device will use its I^{2}C Master Port to attempt to access an external I^{2}C EEPROM at base address 1010000 (binary) at an I^{2}C frequency of 1MHz. If there is no response, this will be repeated at base address 1010001 (binary) at 1MHz. This will repeat up to address 1010111 (binary) at 1MHz. If there are still no responses, the search will be repeated at 400kHz and then again at 100kHz. If no response is received after this whole sequence, the device will proceed to Step 6. Any errors in the process will be reported in status registers.

If at any point in the above search sequence a response is received from an EEPROM, the device will read data from the EEPROM at address offsets 0x0000 and 0xF000 in the EEPROM. If a valid configuration data block is found, it will be read, its checksum validated and if that passes, loaded into internal the internal register image similarly to OTP configuration data described in Step 4. If the data found is not of the correct format or the data block fails a checksum comparison, it will be ignored. The search will continue through the EEPROM and on to the next EEPROM address until the whole range has been searched or a valid configuration block has been found and applied to the internal register image. Then the sequence will proceed to Step 6.

Warning: Since OTP and EEPROM configuration data rarely consists of a full register image, reading of configuration data from OTP and then from one or more configuration blocks stored in EEPROM may result in internal registers being loaded with conflicting settings drawn partially from each of the configuration data sets being loaded. It is strongly recommended that a configuration block placed in EEPROM only be used when no valid configuration is being pointed to in OTP by GPIO signals (or there is no valid configuration in OTP at all).

If multiple configurations are to be used then the user must ensure all registers are set to the desired values by the final configuration block to be loaded.

4.20.7 Step 6 – Complete Configuration

The RC32012A will complete the reset and initial configuration process at this point and begin normal operations. Completion steps include:

- Calibrate the System APLL and lock it to the reference clock on the OSCI input,
- Perform a temperature sensor cycle to establish an initial value in internal registers,
- Enable serial port operation as configured,
- Apply configuration settings from the internal register image to the actual registers and enable output clocks and GPIOs as configured.
- Begin operation on input reference monitors and PLL state machine alarms / status,
- Enable alarm operation as configured.

Note that there are several scenarios in which the reset sequence will reach this point without retrieving any configuration data and with all registers in the default state. This may be intentional for users who wish to configure only via the serial port or the result of a problem in the loading of a configuration. Users may read appropriate status bits to determine what failures, if any, occurred during the reset sequence.

4.21 Clock Gating and Logic Power-Down Control

The RC32012A has the ability to disable the clocks to many logic blocks inside the device. It also has the ability to turn-off internal power regulators, disabling individual power domains within the part. Because of the potentially complex interactions of the logic blocks within the device, logic within the part will handle the decision-making of what will be powered-off versus clock-gated versus fully operational at any time. By default, the device will configure itself with functions in the lowest power-consuming state consistent with powering-up the part and reading a user configuration. User configurations, whether stored in internal OTP, external EEPROM or manually adjusted over the serial port, should make use of register bits to only turn-on functions that are needed. Also if a function is no longer needed, register bits should be used to indicate it is no longer required. Internal logic will reduce its power-consumption state in reaction to these indicators to the greatest extent possible.

4.22 Serial Port Functions

The RC32012A supports 1 serial port. The signals on the port share the functions of an I^2C Master port used for loading configuration data at reset and a configurable slave I^2C or SPI port that can be used at any time after the reset sequence is complete to monitor and/or configure the device. Note that the I^2C master port can only be used when the slave port is configured in I^2C mode. Since I^2C master operation only occurs immediately after reset, while configuration or other data is being loaded from an external I^2C serial EEPROM, I^2C mode for the serial port can be selected via GPIOs as indicated in Use of GPIO Pins at Reset.

The operation of the serial port when in I^2C master operation (during self-configuration only) is described in I2C Master. The SCL and SDIO pins are used for this purpose.

For details on the operation of the master I^2C and slave I^2C or SPI ports, see the appropriate section below.

A slave serial port can be reconfigured at any time by accessing the appropriate registers within a single burst write. This includes configuration options with each protocol or switching between protocols (I^2C to SPI or vice versa). However it is recommended that the full operating mode configuration, including page sizes for registers, for a serial port be set in the initial configuration data read from OTP or external EEPROM (see Device Initial Configuration for details).

Note on Signal Naming in the Remainder of the Serial Port Sections

The pin names indicated in the Pin Description table are meant to indicate the function of that signal when used in SPI mode and also the function when in I^{2}C mode. In the remainder of the Serial Port Functions descriptions, the SPI descriptions will refer to the signals by their function in the selected mode, as shown in Table 29.

Table 29. Serial Port Pin to Function Mapping

SPI Mode Signal Name	Function	I^{2}C Mode Signal Name	Function	Package Pin Name
SCLK	SPI Clock Input	SCLK	I^{2}C Clock Input	SCLK
CS	SPI Chip Select (active low)	A0	I^{2}C Slave Address Bit 0	CS_A0
SDI	SPI Data Input (unused in 3-wire mode)	A1	I^{2}C Slave Address Bit 1	SDI_A1
SDIO	SPI Data Out (4-wire mode) SPI Data In/Out (3-wire mode)	SDA	I^{2}C Data In/Out	SDIO

4.22.1 Addressing Registers within the RC32012A

The address space that is externally accessible within the RC32012A is 64kbytes in size and so needs 16-bits of address offset information to be provided during slave serial port accesses. Of that 64kbytes, only the upper 32kbytes contains user accessible registers.

The user may choose to operate the serial port providing the full offset address within each burst or to operate in a paged mode where part of the address offset is provided in each transaction and part comes from an internal page register in each serial port. Figure 16 shows how page register and offset bytes from each serial transaction interact to address a register within the RC32012A.

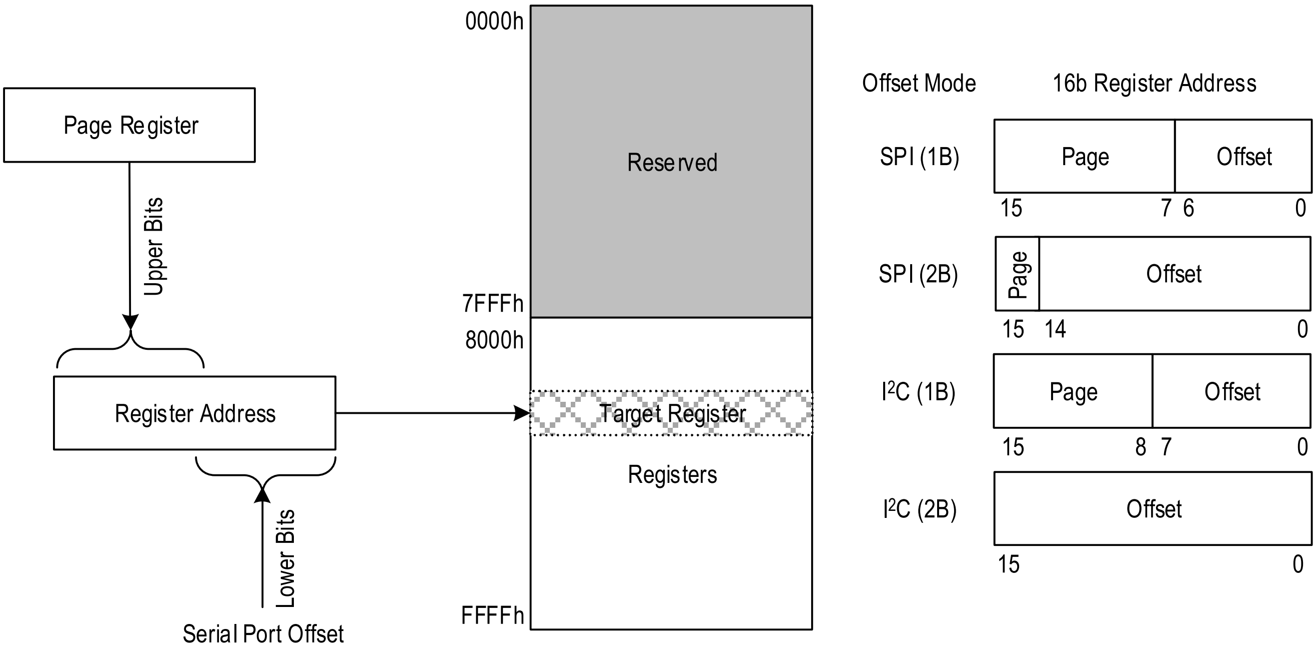


Figure 16. Register Addressing Modes via Serial Port

4.22.2 I²C Slave Operation

The I²C slave protocol of the RC32012A complies with the I²C specification version UM10204 Rev.6 – 4 April 2014. Figure 17 shows the sequence of states on the I²C SDA signal for the supported modes of operation.

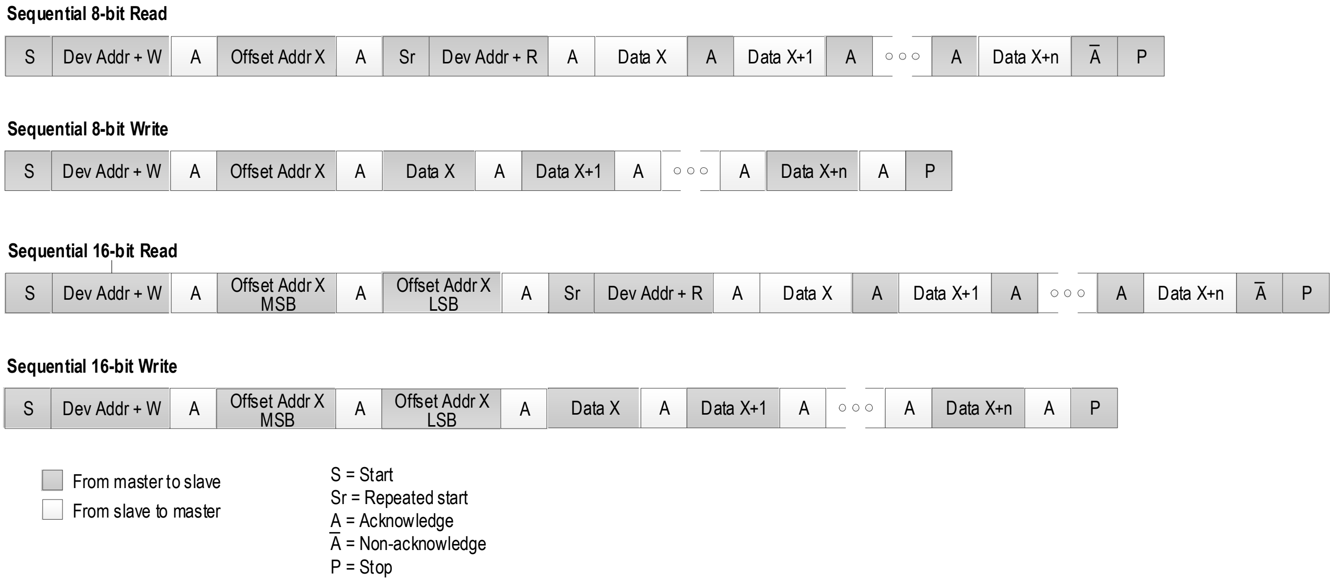


Figure 17. I²C Slave Sequencing

The Dev Addr shown in the figure represents the base address of the RC32012A device. This 7-bit value can be set in an internal register which can have a user-defined value loaded at reset from internal OTP memory or an external EEPROM. The default value if those methods are not used is 1011000b. Note that the levels on the A0 and A1 signals can be used to control Bit 0 and Bit 1 (respectively) of this address. There is also an option as defined in the Use of GPIO Pins at Reset section to designate the reset state of a GPIO pin to set the default value of the A2 bit of the I²C slave port base address. In I²C operation these inputs are expected to remain static. They have different functions when the part is in SPI mode. The resulting base address is the I²C bus address that this device will respond to.

When I²C operation is selected for a slave serial port, the selection of 1-byte (1B) or 2-byte (2B) offset addressing must also be configured. These offsets are used in conjunction with the page register for each serial port to access registers internal to the device. Because the I²C protocol already includes a read/write bit with the Dev Addr, all bits of the 1B or 2B offset field can be used to address internal registers.

- In 1B mode, the lower 8-bits of the register offset address come from the Offset Addr byte and the upper 8-bits come from the page register.
  The page register can be accessed at any time using an offset byte value of FCh. This 4-byte register must be written in a single burst write transaction.
- In 2B mode, the full 16-bit register address can be obtained from the Offset Addr bytes, so the page register only needs to be setup once after reset via a 4-byte burst access at offset FFFCh.

Note: I²C burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single I²C burst access. Bursts may be of greater length if desired, but must not extend beyond the end of the register page (Offset Addr FFh in 1B mode, no limit in 2B mode). An internal address pointer is incremented automatically as each data byte is written or read.

4.22.2.1 I^{2}C 1-byte (1B) Addressing Examples

RC32012A I^{2}C 7-bit I^{2}C address is 0x5B with LSB = R/W

Example write “0x50” to register 0xCBE4:

```
   B6* FC 00 CB 10 20  #Set Page Register, *I2C Address is left-shifted one bit.
   B6 E4 50            #Write data 5B to CB E4
```

Example read from register 0xC024:

```
   B6* FC 00 C0 10 20  #Set Page Register, *I2C Address is left-shifted one bit.
   B6 24*              #Set I2C pointer to 0xC024, *I2C instruction should use “No
Stop”
   B7 <read back data> #Send address with Read bit set.
```

4.22.2.2 I^{2}C 2-byte (2B) Addressing

RC32012A I^{2}C 7-bit I^{2}C address is 0x5B with LSB = R/W

Example write “50” to register 0xCBE4:

```
   B6* FF FD 00 10 20  #Set Page Register, *I2C Address is left-shifted one bit.
   B6 CB E4 50         #Write data to CB E4
```

Example read from register 0xC024:

```
   B6* FF FD 00 10 20  #Set Page Register (*I2C Address is left-shifted one bit.)
   B6 C0 24*           #Set I2C pointer to 0xC024, *I2C instruction should use “No
Stop”
   B7 <read back data> #Send address with Read bit set.
```

4.22.3 I^{2}C Master

The RC32012A has the ability to load its register configuration from an external I^{2}C EEPROM during its reset sequence, but only if the serial port is configured in I^{2}C mode. For information on what accesses occur under what conditions, see Reset Sequence.

As needed during the reset sequence, the RC32012A will arbitrate for the I^{2}C bus and attempt to access an external I^{2}C EEPROM using the access sequence shown in Figure 18. The I^{2}C master protocol of the RC32012A complies with the I^{2}C specification version UM10204 Rev.6 – 4 April 2014. As can be seen in the figure, the I^{2}C master port may be configured to support I^{2}C EEPROMs with either 1-byte or 2-byte offset addressing. The I^{2}C master logic will negotiate with any EEPROMs found to use the highest speed of 1MHz, 400kHz or 100kHz.

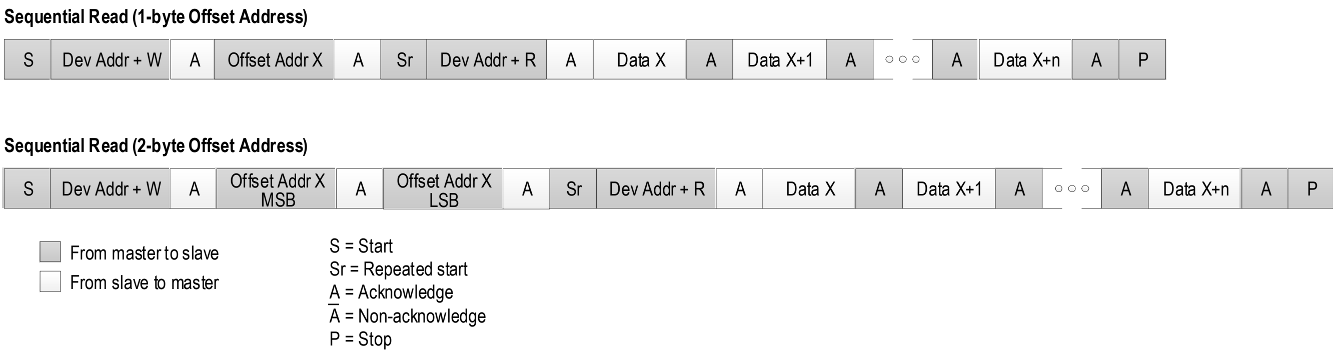


Figure 18. I^{2}C Master Sequencing

4.22.4 SPI Operation

The RC32012A supports SPI operation as a selectable protocol on the serial port. The port may be configured for either 3-wire or 4-wire operation. In 4-wire mode, there are separate data in (to the RC32012A) and data out signals (SDI and SDIO respectively). In 3-wire mode, the SDIO signal is used as a single, bidirectional data signal. Figure 19 shows the sequencing of address and data on the serial port in both 3-wire and 4-wire SPI mode. 4-wire SPI mode is the default. The R/W bit is high for Read Cycles and low for Write Cycles.

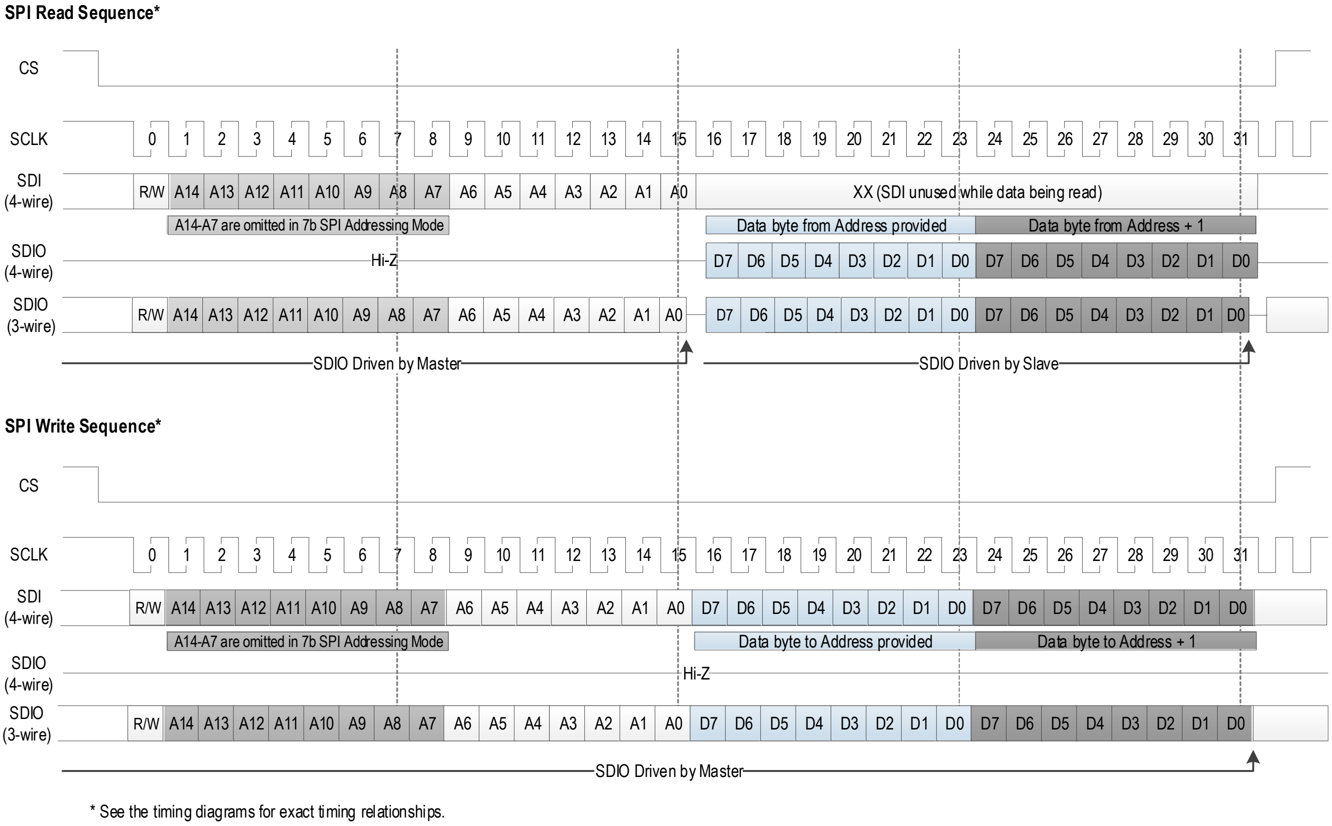


Figure 19. SPI Sequencing

A serial port can be configured for the following settings. These settings can come from register defaults or from an internal OTP or external EEPROM configuration loaded at reset:

- 1-byte (1B) or 2-byte (2B) offset addressing (see Figure 16)
  - In 1B operation, the 16-bit register address is formed by using the 7-bits of address supplied in the SPI access and taking the upper 9-bits from the page register. The page register is accessed using an Offset Address of 7Ch with a 4-byte burst access.
  - In 2B operation, the 16-bit register address is formed by using the 15-bits of address supplied in the SPI access and taking the upper 1-bit from the page register. Note that this bit will always be ‘1’ for register accesses, so the page register only needs to be set once in 2B operation. The page register can be accessed using a 3-byte burst access Offset Address of 7FFDh. It should be accessed in a single burst write transaction to set it.
- Data sampling on falling or rising edge of SCLK
- Output (read) data positioning relative to active SCLK edge
- 4-wire (SCLK, CS, SDIO, SDI) or 3-wire (SCLK, CS, SDIO) operation
- In 3-wire mode, SDIO is a bi-directional data pin.
- Output signal protocol compatibility / drive strength and termination voltage

Note: SPI burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts may be of greater length if desired, but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

4.22.4.1 SPI 1-byte (1B) Addressing Example

Example write to “50” to register 0xCBE4

```
  7C 80 CB 10 20      #Set Page register
  64* 50              #*MSB is 0 for write transactions
```

Example read from 0xC024:

```
  7C 00 C0 10 20      #Set Page register
  A4* 00              #*MSB is set, so this is a read command
```

4.22.4.2 SPI 2-byte (2B) Addressing Example

Example write to “50” to register 0xCBE4

```
  7F FD 80 10 20      #Set Page register
  4B E4* 50           #*MSB is 0 for write transactions
```

Example read from 0xC024:

```
7F FD 80 10 20        #Set Page register
C0* 24 00             #*MSB is set, so this is a read command
```

5. Applications Information

5.1 Recommendations for Unused Input and Output Pins

5.1.1 Inputs

5.1.1.1 CLKx / nCLKx Input

For applications that do not require the use of the reference clock input, both CLK and nCLK should be left floating. If the CLK/nCLK input is connected but not used by the device, it is recommended that CLK and nCLK not be driven with active signals.

5.1.1.2 LVCMOS Control Pins

LVCMOS control pins have internal pull-ups. Additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

5.1.2 Outputs

5.1.2.1 LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached. The mode of the output buffer should be set to tri-stated to avoid any noise being generated.

5.1.2.2 Differential Outputs

All unused differential outputs can be left floating. Renesas recommends that there is no trace attached. Both sides of the differential output pair should be left floating or terminated.

5.1.3 Power Connections

The power connections of the RC32012A can be grouped as shown if all members of the groups are using the same voltage level:

- V_{DD_DIG}
- V_{DDA_FB}
- V_{DDO_Qn} (can share supplies if output frequencies are the same, otherwise keep separated to avoid spur coupling)
  - If all outputs Qn/nQn associated with any particular V_{DDO_Qn} pin are not used, the power pin can be left floating

5.2 Clock Input Interface

The RC32012A accepts both single-ended and differential inputs. For information on input terminations, see Quick Guide - Output Terminations (AN-953).

If you have additional questions on input types not covered in the application discussion, or if you require information about register programming sequences for changing the differential inputs to accept LVCMOS inputs levels, see Termination - AC Coupling Clock Receivers (AN-844) or contact Renesas technical support.

5.3 Overdriving the XTAL Interface

The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCI input is internally biased at 1V. The OSCO pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 1.8V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 20. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise.

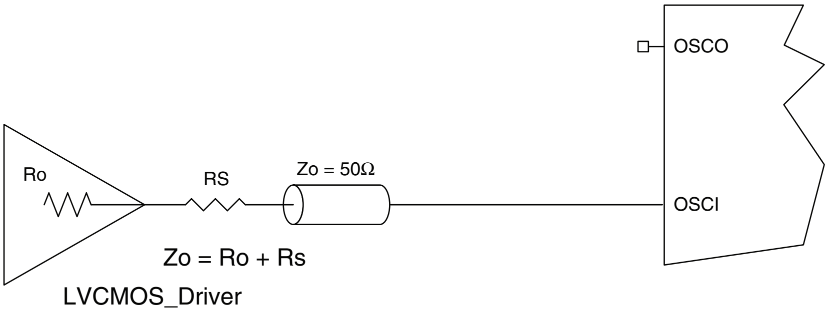


Figure 20. 1.8V LVCMOS Driver to XTAL Input Interface

Figure 21 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

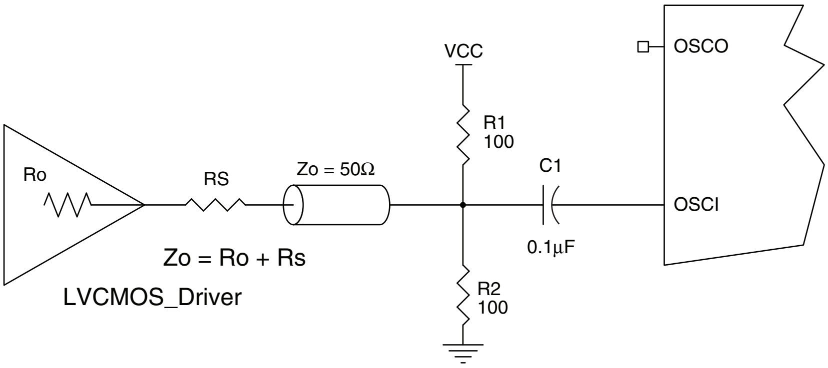


Figure 21. LVCMOS Driver to XTAL Input Interface

Figure 22 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and guaranteed using a quartz crystal as the input.

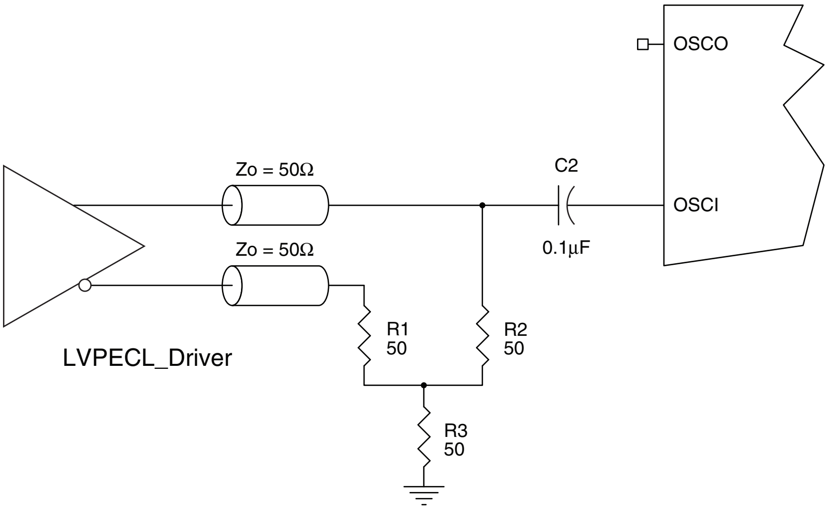


Figure 22. LVPECL Driver to XTAL Input Interface

5.4 Wiring the Differential Input to Accept Single-Ended Levels

For information, see Differential Input to Accept Single-ended Levels Application Note (AN-836).

5.5 Differential Output Termination

For all types of differential protocols, the same termination schemes are recommended (see Figure 23 and Figure 24). These schemes are the same as normally used for an LVDS output type.

The recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_{Diff}) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. To avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

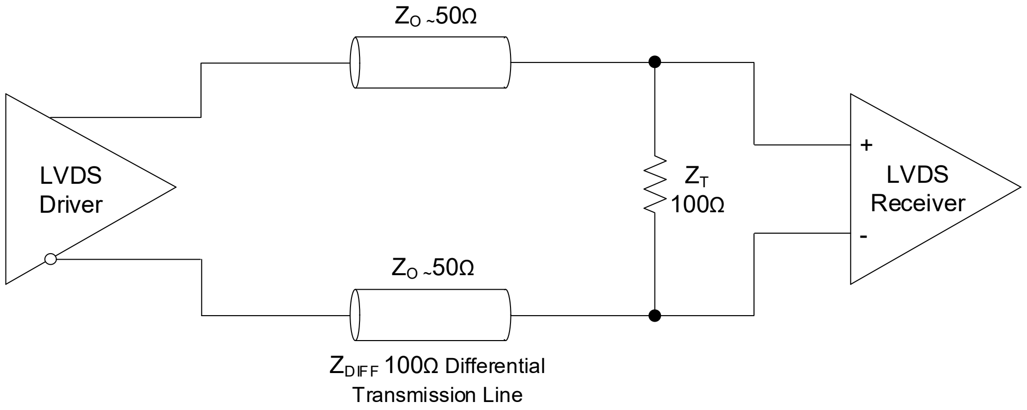


Figure 23. Standard LVDS Termination

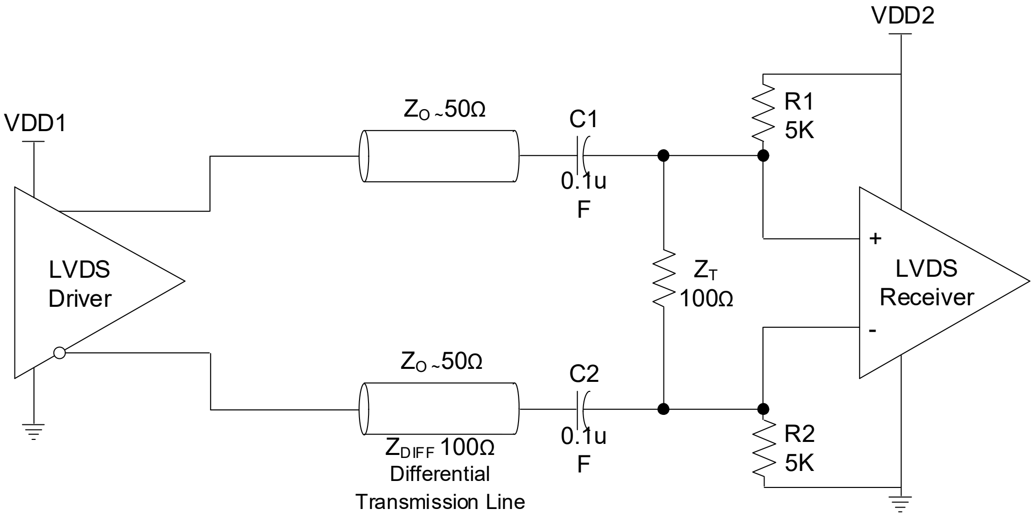


Figure 24. AC Coupled LVDS Termination

For alternate termination schemes, see “LVDS Termination” in Quick Guide - Output Terminations (AN-953), or contact Renesas for support.

5.6 External I²C Serial EEPROM Recommendation

An external I²C EEPROM can be used to store configuration data and/or to contain device update data. An EEPROM with 8Kbit capacity is sufficient to store a full configuration. However, the recommendation is to use an EEPROM with a 1Mbit capacity in order to support future device updates. Renesas has validated and recommends the use of the Microchip 24FC1025 or OnSemi CAT24M01 1Mbit EEPROM.

5.7 Schematic and Layout Information

The RC32012A requires external load capacitors to ensure the crystal will resonate at the proper frequency. For recommendations on crystal vendors, contact Renesas. For recommended values for external tuning capacitors, see Table 30.

Table 30. Recommended Tuning Capacitors for Crystal Input

Crystal Nominal C_L Value (pF)	Recommended Tuning Capacitor Value (pF)[1]	
	OSCI Capacitor (pF)	OSCO Capacitor (pF)
8	2.7	2.7
10	13	3.3
12	27	3.3
18[2]	27	3.3

1. Recommendations are based on 4pF stray capacitance on each leg of the crystal. Adjust according to the PCB capacitance.
2. This will tune the crystal to a CL of 12pF, which is fine when channels are running in Jitter attenuator mode or referenced to an XO. It will present a positive ppm offset for channels running exclusively in Synthesizer mode and referenced only to the crystal.

5.8 Power Considerations

For power and current consumption calculations, see the Renesas Timing Commander tool.

6. Thermal Information

6.1 VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 25. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e., “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern (Note: These recommendations are to be used as a guideline only). For additional information, see the application note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

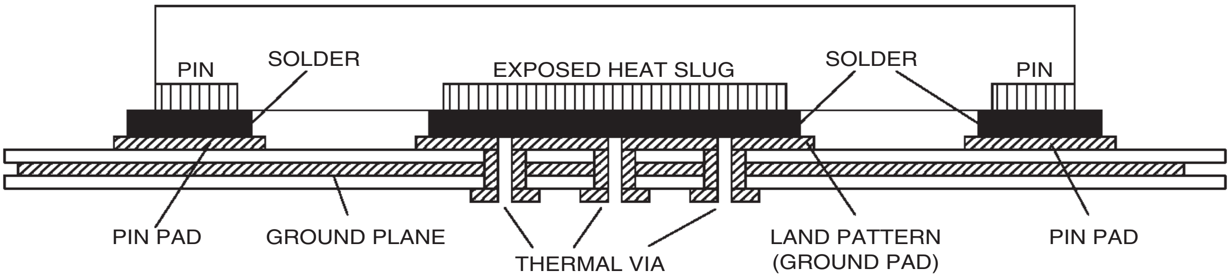


Figure 25. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)

6.2 Thermal Characteristics

Table 31. Thermal Characteristics

Symbol	Parameter		Value	Unit
θ_{JA}	Theta J_A. Junction to Ambient Air Thermal Coefficient[1][2]	0 m/s air flow	13.71	°C/W
		1 m/s air flow	10.67	°C/W
		2 m/s air flow	9.46	°C/W
θ_{JB}	Theta J_B. Junction to Board Thermal Coefficient[1]		0.702	°C/W
θ_{JC}	Theta J_C. Junction to Device Case Thermal Coefficient[1]		12.87	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)		3	

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePAD is connected to a ground plane using a grid of 9x9 thermal vias.

7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

8. Marking Diagram

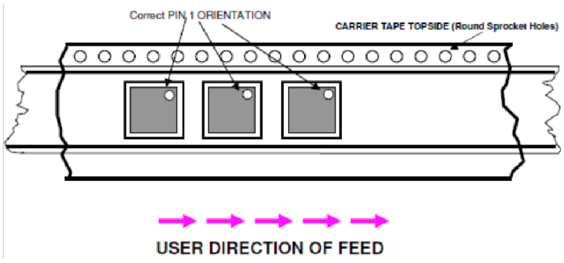
- Lines 2 and 3 are the part number.
  - “000” denotes dash code; “GN2” denotes the package code.
- Line 4:
  - “#” denotes stepping; “YYWW” is the last digits of the year and week that the part was assembled; “$” denotes mark code.
- “LOT” denotes the lot code; “COO” denotes country of origin

9. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RC32012AdddGN2#BB0[1]	10 × 10 × 0.9 mm, 72-VFQFN	3	Tray	-40° to +85°C
RC32012AdddGN2#KB0	10 × 10 × 0.9 mm, 72-VFQFN	3	Tape and Reel, Pin 1 Orientation: EIA-481-D	-40° to +85°C

1. Replace “ddd” with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use “000” for unprogrammed parts.

Table 32. Pin 1 Orientation in Tape and Reel Packaging

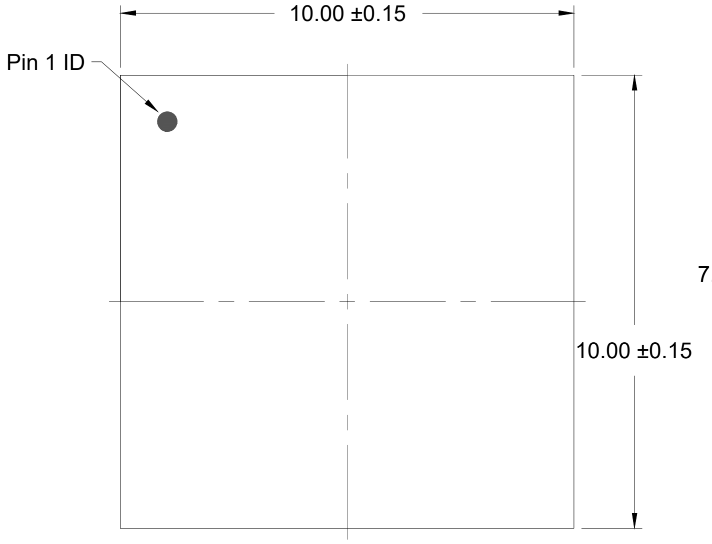
Part Number Suffix	Pin 1 Orientation	Illustration
NK#K	Quadrant 2 (EIA-481-D)	

10. Revision History

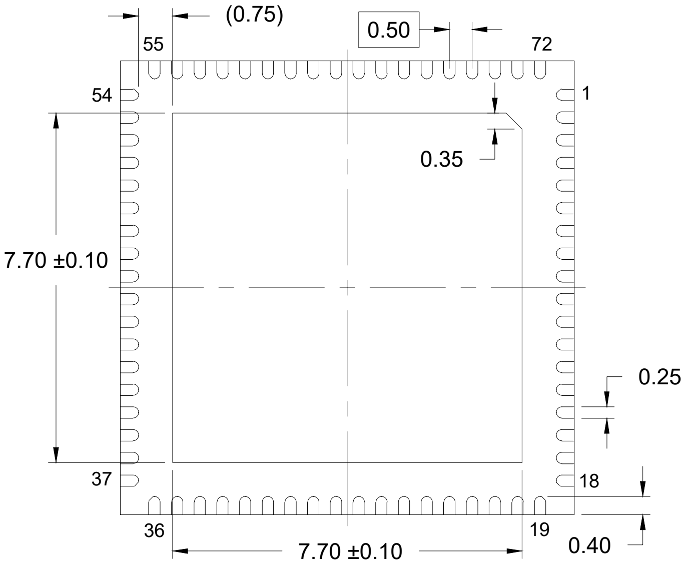
Revision	Date	Description
1.03	Sep 15, 2022	▪ Updated the differential output parameter for t_R / t_F in Table 18
1.02	May 6, 2022	▪ Deleted the “Temperature Sensor” section ▪ Updated One-Time Programmable (OTP) Memory ▪ Completed other minor changes
1.01	Nov 1, 2021	▪ Updated the Functional Description section. ▪ Updated the Marking Diagram section.
1.00	Aug 13, 2021	Initial release.

Package Outline Drawing

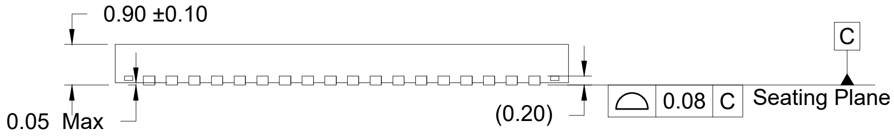
Package Code:NLG72P4
72-VFQFPN 10.0 x 10.0 x 0.90 mm Body, 0.50 mm Pitch
PSC-4208-04, Revision: 05, Date Created: Jul 6, 2023



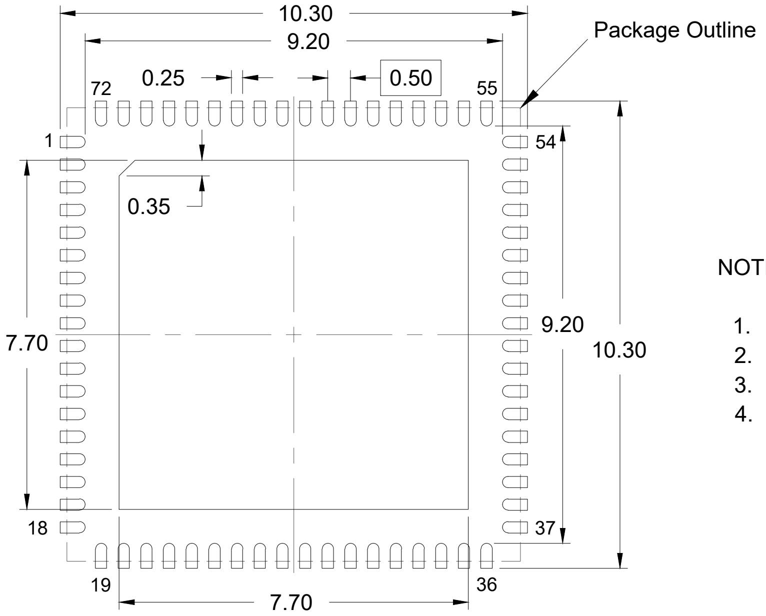
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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