READ2656J

High Drivability & High Slew Rate, Output Full Range High Voltage, Low Power Consumption CMOS Dual Operational Amplifier

Description

The READ2656J is dual CMOS Operational Amplifier with AEC-Q100 compliant, which is the features the same performance as the Bipolar products (UPC842) about the voltage resistance (power supply voltage: 36V Max.) and high slew rate (8V/µs Typ.). This IC is the output full-range product with greatly reduced power consumption and input bias current compared to bipolar products.

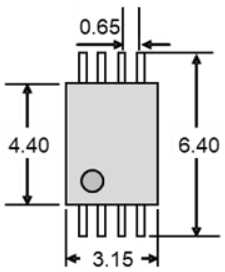
Features

— AEC-Q100 Compliant
— Output full range (Rail-to-Rail output)
— Absolute Maximum Ratings
- Power Supply Voltage V_{DD} = -0.1 to +36V
- Operating Ambient Temperature Range T_A= -40 to +125 ˚C

— Electrical Characteristics
- Power Supply Voltage V_{DD} = +4.5V to +32V
- Input Offset Voltage V_{IO} ≤ ±9mV
- Input Bias Current I_B ≤ (1pA)
- Supply current (per channel) I_{DD} = 0.7 mA Typ., 1.0 mA Max. (@V_{DD}=5.0V T_A=-40˚C to +125˚C)
- Slew Rate SR = 8 V/µs Typ.

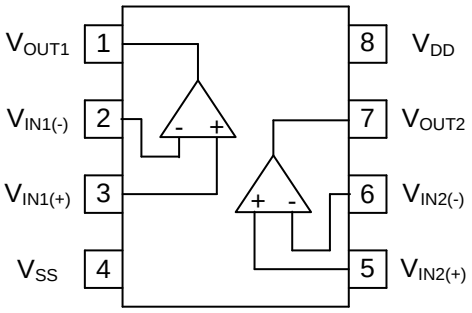
( ) reference value of design

Product Line-up

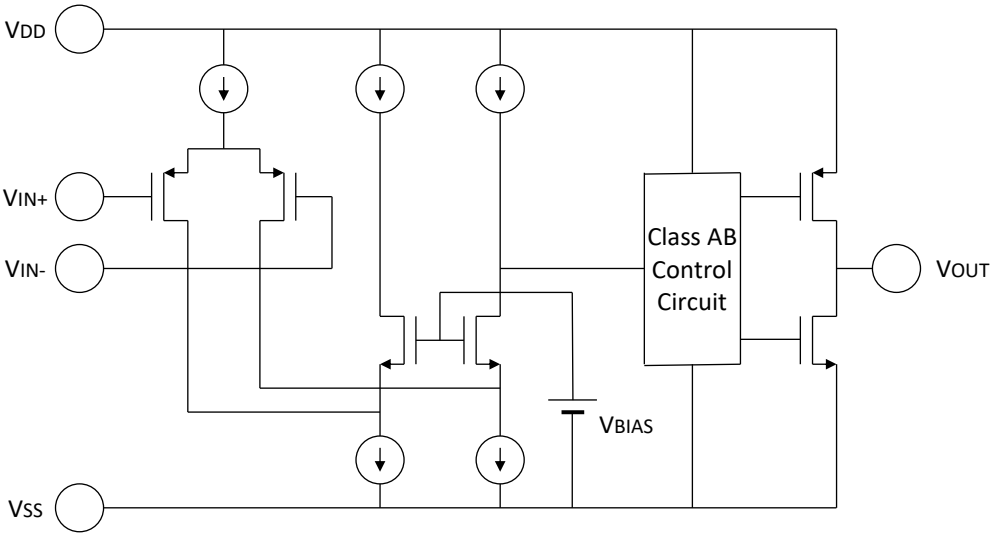
Package	TSSOP
Product Name(1)	READ2656JSP#GC1 READ2656JSP#HC1
Quality Level	High Quality Level
Outline	**Unit : mm** 

(1). The taping direction is different for GC and HC. Please refer to the delivery specifications for details.

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<T_A=-40 to +125 ˚C >

Items	Symbol	Ratings	Unit
Supply voltage Note.1	V_{DD}	-0.1 to +36	V
Differential input voltage	V_{ID}	±2	V
Input voltage Note.2	V_I	V_{SS} -0.1 to V_{DD} +0.1	V
Maximum output current	I_O	20	mA
Power dissipation Note.3	P_T	440	mW
Junction temperature	T_j	-40 to +150	˚C
Operating temp. range	T_A	-40 to +125	˚C
Storage temp. range	T_{stg}	-55 to +150	˚C

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of V_{SS} (GND)-0.1V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm x 100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ2656JSP: Derate at -5.5 mW/˚C when T_A > 69 ˚C

(Junction – ambient thermal resistance $R_{th(J-A)}$ = 183 ˚C/W)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (V_{SS} = GND)	V_{DD}	+4.5		+32	V
Power Supply Voltage (Dual Supply)	V_{DD} – V_{SS}	±2.25		±16	V

Electrical Characteristics

< T_A=25˚C, V_{DD}=5.0V, V_{SS}=GND>

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V_{IO}		±3	±9	mV	
Input offset current	I_{IO}			(±1)	pA	
Input bias current	I_B			(±1)	pA	
Output high voltage	V_{OH}	V_{DD}-0.3			V	I_L = 10mA
Output low voltage	V_{OL}			V_{SS}+0.3	V	I_L = 10mA
Voltage gain	A_V	60	90		dB	R_L≥100kΩ
Channel supply current	I_{DD}/ch		0.7	1	mA	R_L=∞, I_O=0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		V_{DD}-2	V	
Gain bandwidth product	GBW		6		MHz	C_L=20pF
Slew rate	SR		8		V/μs	C_L=20pF
Channel Separation			80		dB	f = 20 Hz to 20 kHz

< T_A=25˚C, $V_{DD,SS}$=±15 V >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V_{IO}		±3	±12	mV	
Input offset current	I_{IO}			(±1)	pA	
Input bias current	I_B			(±1)	pA	
Output high voltage	V_{OH}	V_{DD}-0.3			V	I_L = 10mA
Output low voltage	V_{OL}			V_{SS}+0.3	V	I_L = 10mA
Voltage gain	A_V	60	90		dB	R_L≥100kΩ
Channel supply current	I_{DD}/ch		0.7	1	mA	R_L=∞, I_O=0
Common mode rejection ratio	CMRR	55	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		V_{DD}-2	V	
Gain bandwidth product	GBW		6		MHz	C_L=20pF
Slew rate	SR		8		V/μs	C_L=20pF
Channel Separation			80		dB	f = 20 Hz to 20 kHz

< T_A= -40 to +125˚C, V_{DD}=5.0V, V_{SS}=GND>

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V_{IO}		±3	±9	mV	
Input offset current	I_{IO}		±3	±20	nA	
Input bias current	I_B		±3	±20	nA	
Output high voltage	V_{OH}	V_{DD}-0.45			V	I_L = 10 mA
Output low voltage	V_{OL}			V_{SS}+0.45	V	I_L = 10 mA
Voltage gain	A_V	60	90		dB	R_L≥100kΩ
Channel supply current	I_{DD}/ch		0.7	1.0	mA	R_L=∞, I_O=0
Common mode rejection ratio	CMRR	50	80		dB	
Supply voltage rejection ratio	SVRR	50	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		V_{DD}-2	V	
Gain bandwidth product	GBW		6		MHz	C_L=20pF
Slew rate	SR		8		V/μs	C_L=20pF
Channel Separation			80		dB	f = 20 Hz to 20 kHz

( ) reference value of design

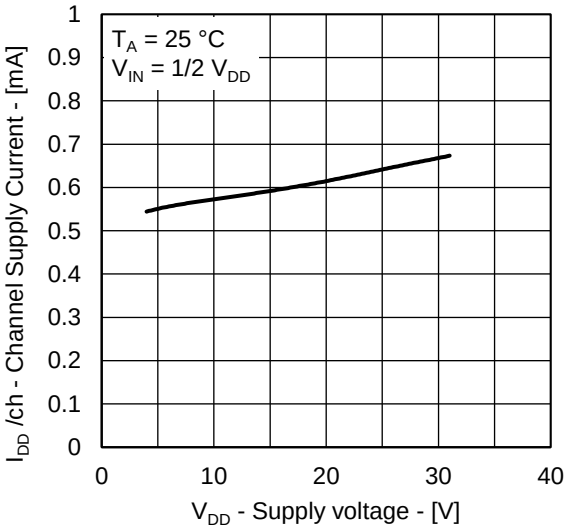
Notes

Output terminal: The over-current protection feature is not built in the output terminal of this product. Therefore, if the output is short circuit (from output to V_{DD} or from output to V_{SS}) or the forward clamp circuit using the diode at the output pin, the excessive output current may flow. Please insert the series resistor in the output pin to limit the current.

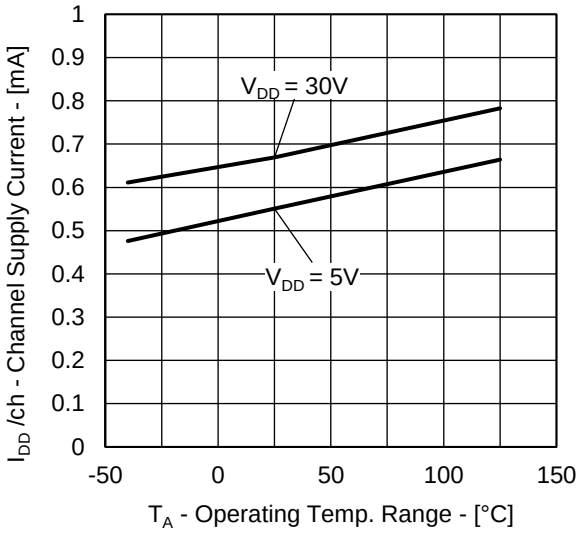
Application circuit: Please keep V_{ID} within ±2V during stationary operation and design the closed-loop operation composed feedback system: Voltage Follower, Inverting Amplifier and Non-inverting Amplifier.

Characteristics Curve (T_A = 25 °C) (Reference Value)

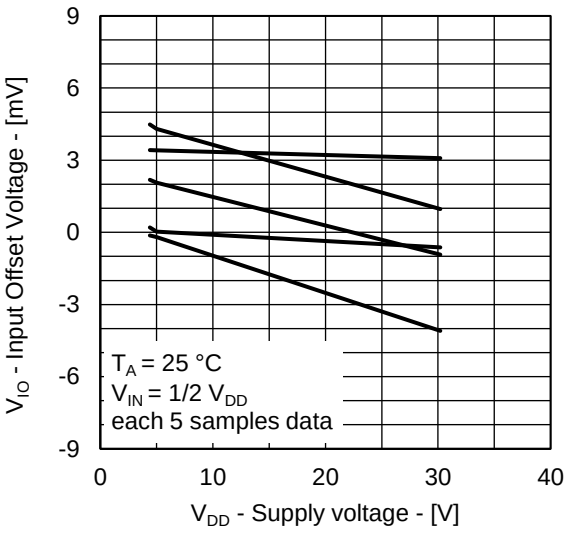
I_{DD} /ch vs. V_{DD}



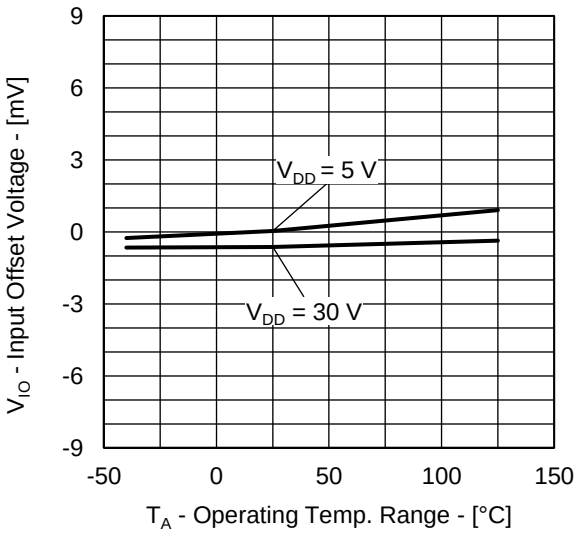
I_{DD} /ch vs. T_A



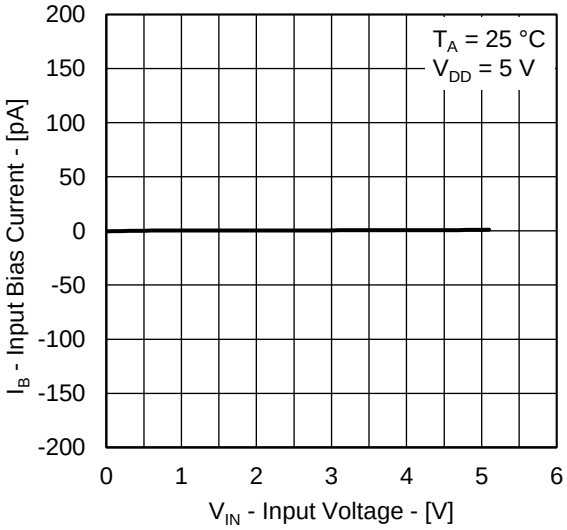
V_{IO} vs. V_{DD}



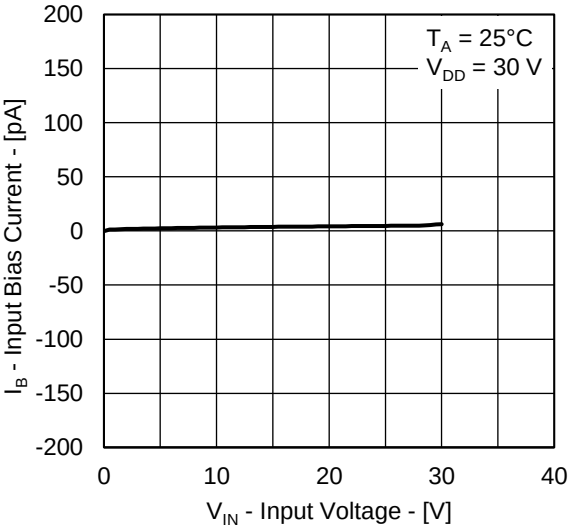
V_{IO} vs. T_A



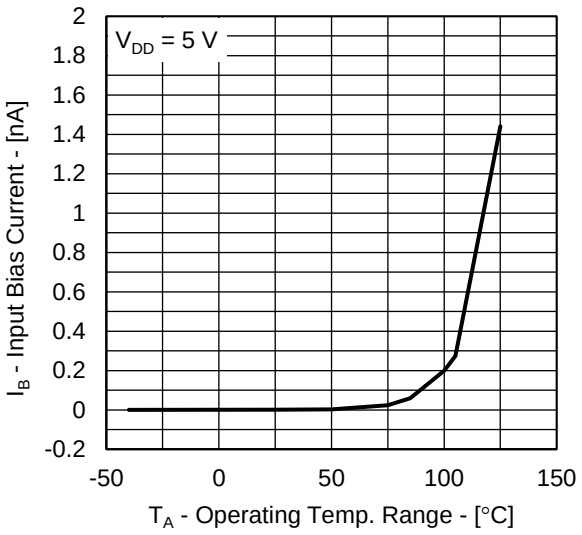
I_B vs. V_{IN}



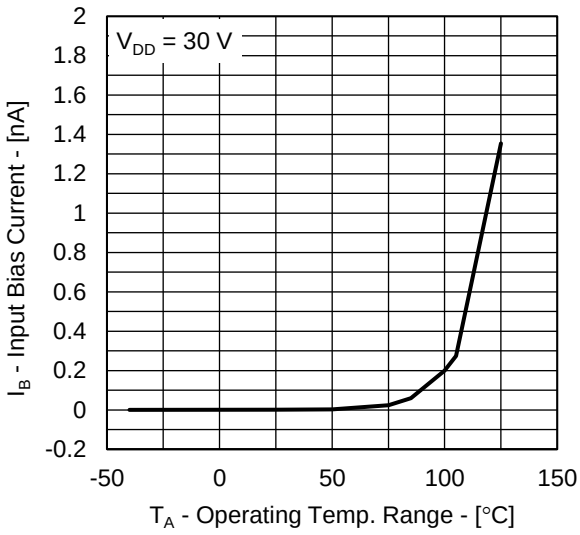
I_B vs. V_{IN}



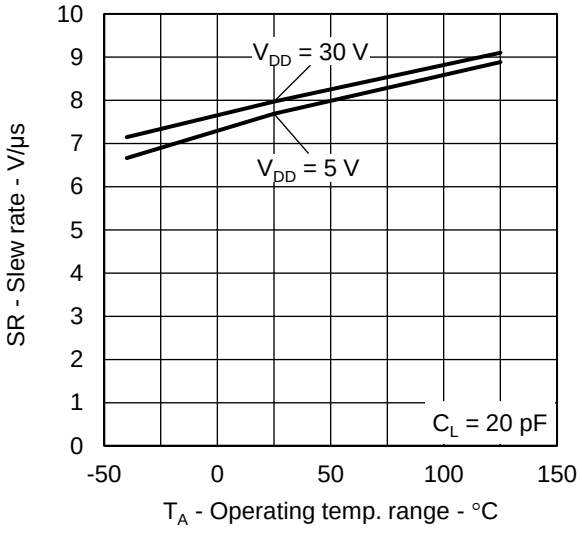
I_B vs. T_A



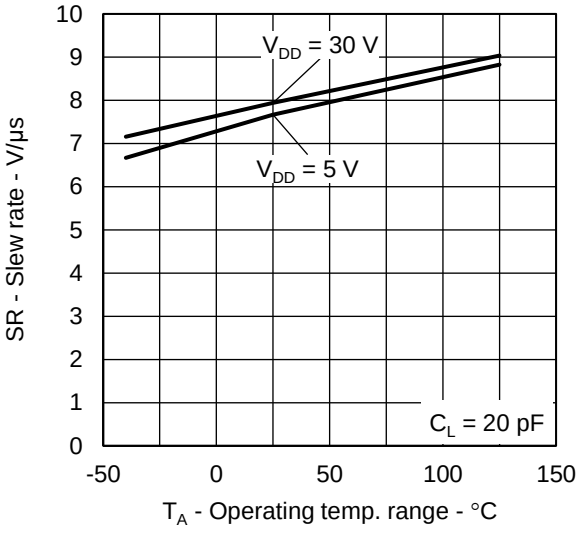
I_B vs. T_A



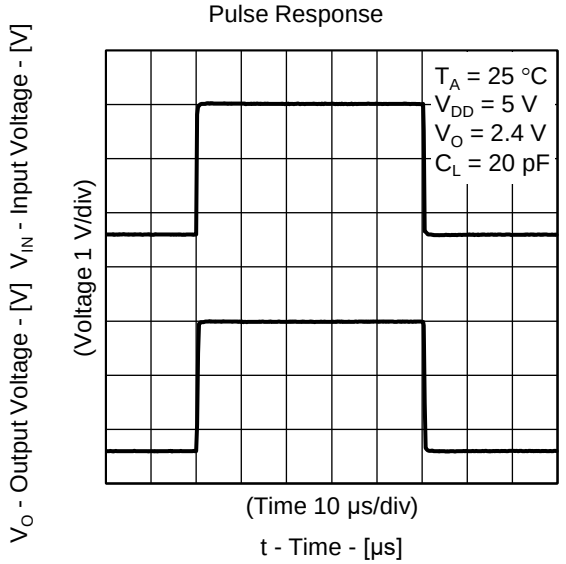
SR vs. T_A (Output rise time)



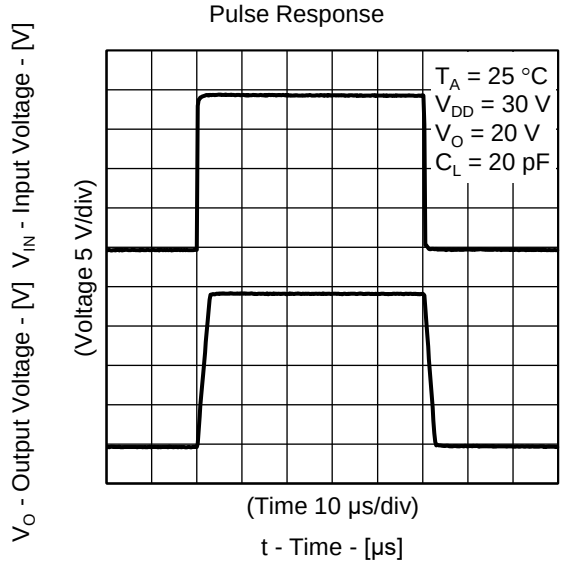
SR vs. T_A (Output fall time)

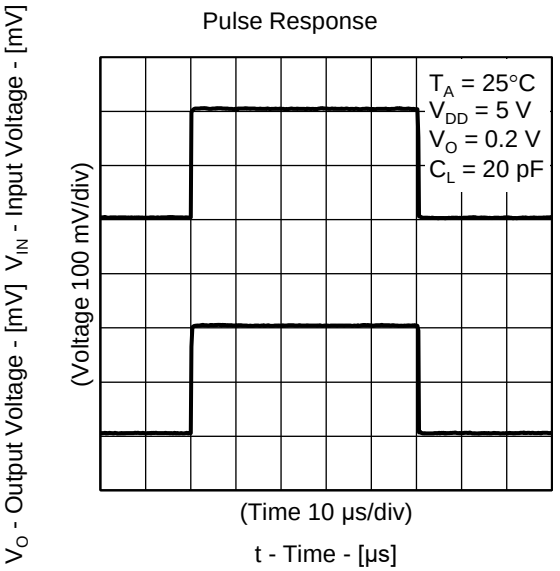


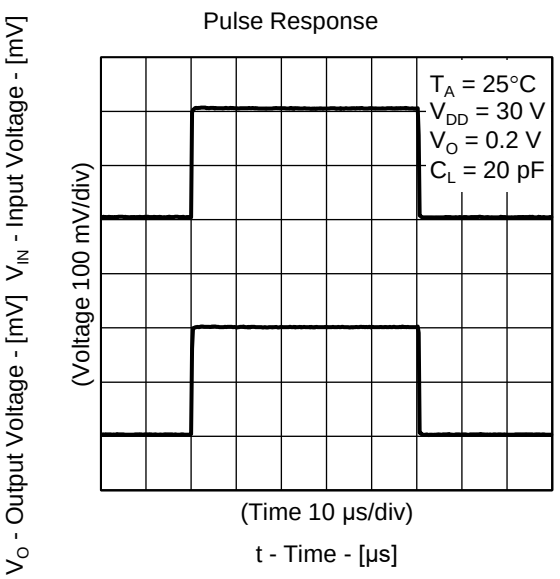
Pulse Response

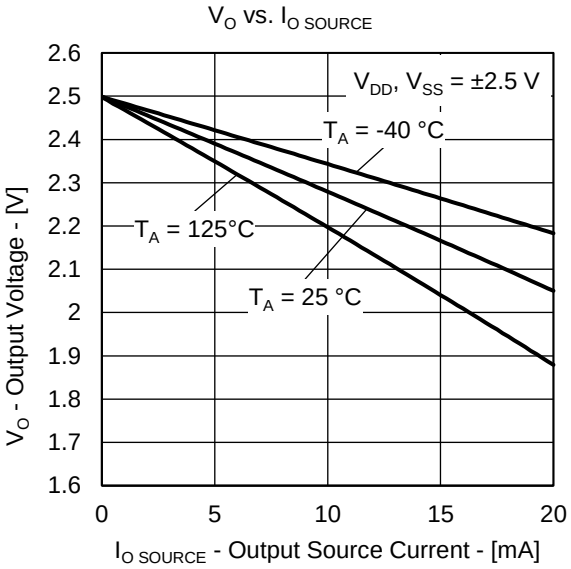


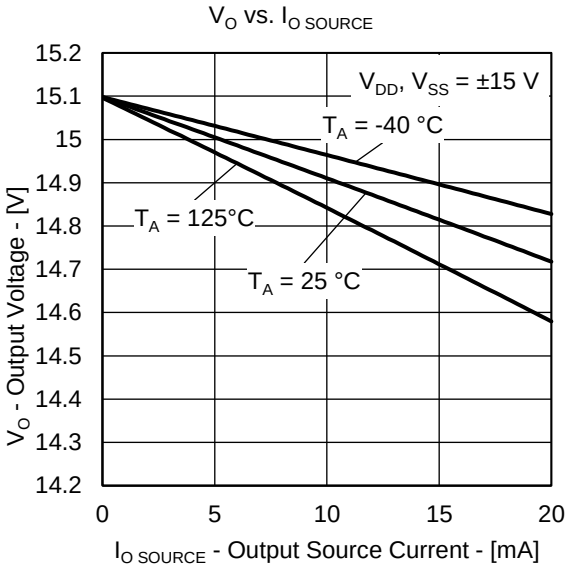
Pulse Response

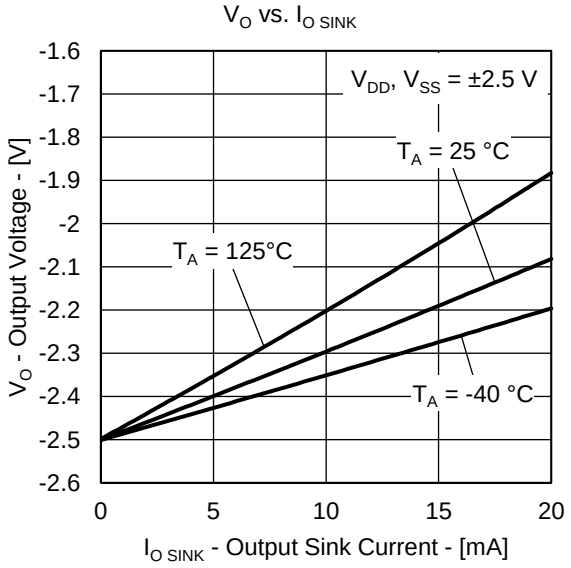


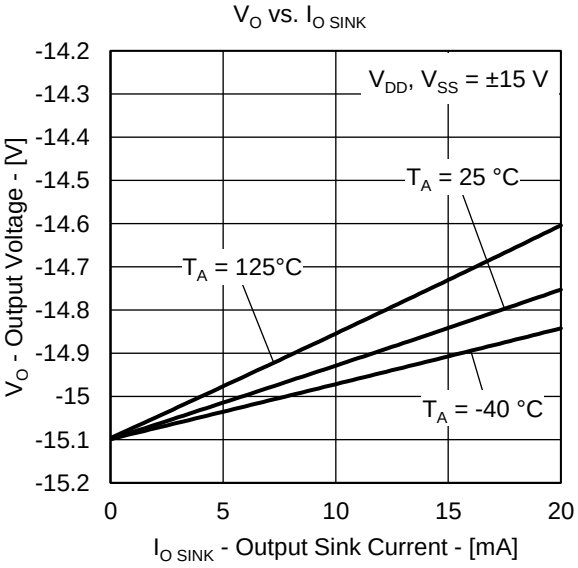

Pulse Response
T_A = 25°C
V_{DD} = 5 V
V_O = 0.2 V
C_L = 20 pF
(Voltage 100 mV/div)
V_O - Output Voltage - [mV] V_{IN} - Input Voltage - [mV]
(Time 10 µs/div)
t - Time - [µs]


Pulse Response
T_A = 25°C
V_{DD} = 30 V
V_O = 0.2 V
C_L = 20 pF
(Voltage 100 mV/div)
V_O - Output Voltage - [mV] V_{IN} - Input Voltage - [mV]
(Time 10 µs/div)
t - Time - [µs]

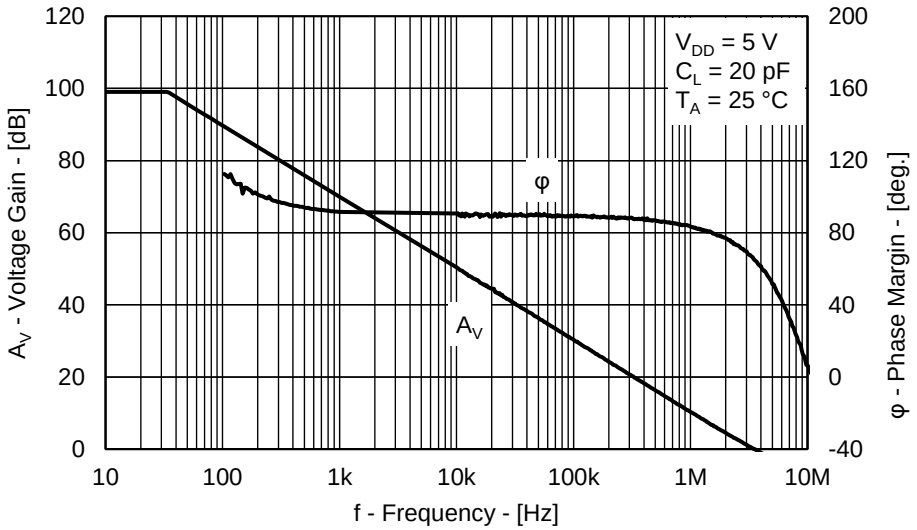

V_O vs. $I_{O\ SOURCE}$
V_{DD}, V_{SS} = ±2.5 V
T_A = -40 °C
T_A = 125°C
T_A = 25 °C
V_O - Output Voltage - [V]
$I_{O\ SOURCE}$ - Output Source Current - [mA]


V_O vs. $I_{O\ SOURCE}$
V_{DD}, V_{SS} = ±15 V
T_A = -40 °C
T_A = 125°C
T_A = 25 °C
V_O - Output Voltage - [V]
$I_{O\ SOURCE}$ - Output Source Current - [mA]

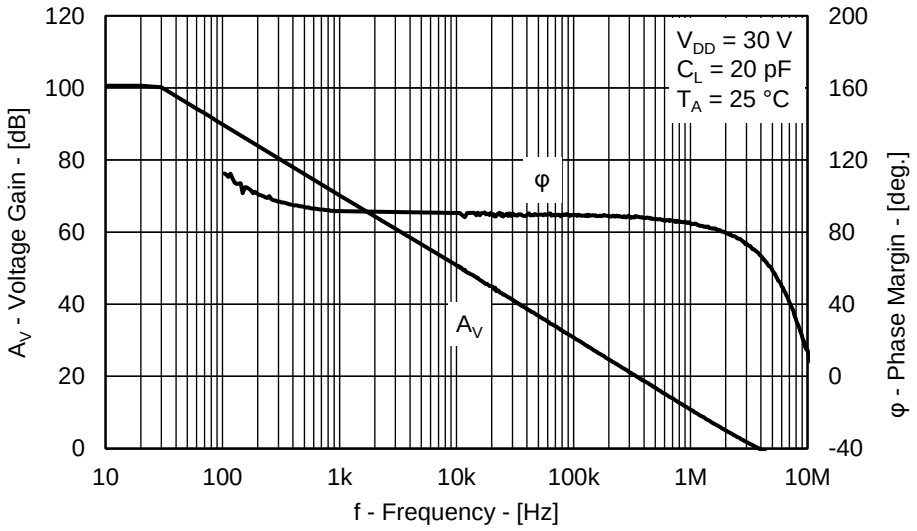

V_O vs. $I_{O\ SINK}$
V_{DD}, V_{SS} = ±2.5 V
T_A = 25 °C
T_A = 125°C
T_A = -40 °C
V_O - Output Voltage - [V]
$I_{O\ SINK}$ - Output Sink Current - [mA]


V_O vs. $I_{O\ SINK}$
V_{DD}, V_{SS} = ±15 V
T_A = 25 °C
T_A = 125°C
T_A = -40 °C
V_O - Output Voltage - [V]
$I_{O\ SINK}$ - Output Sink Current - [mA]

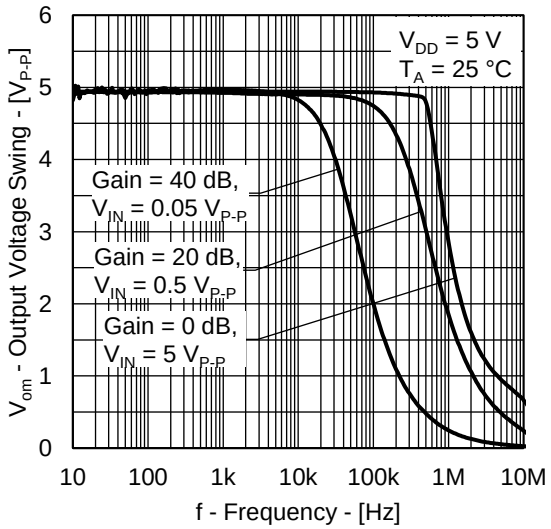
A_V, φ vs. f



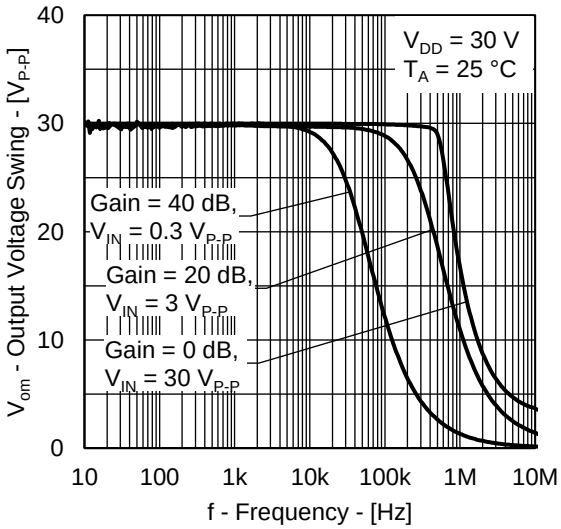
A_V, φ vs. f



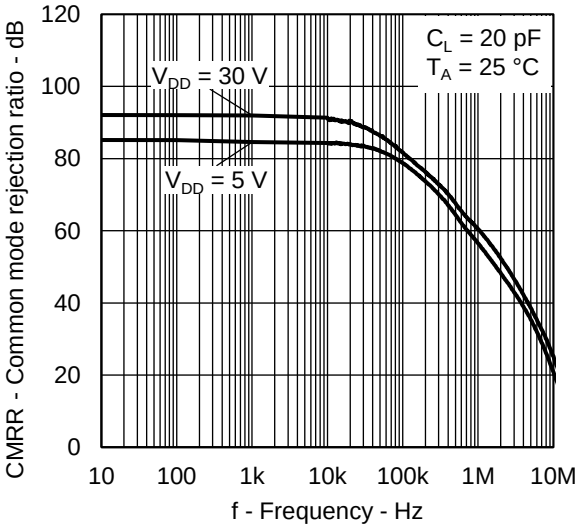
V_{om} vs. f



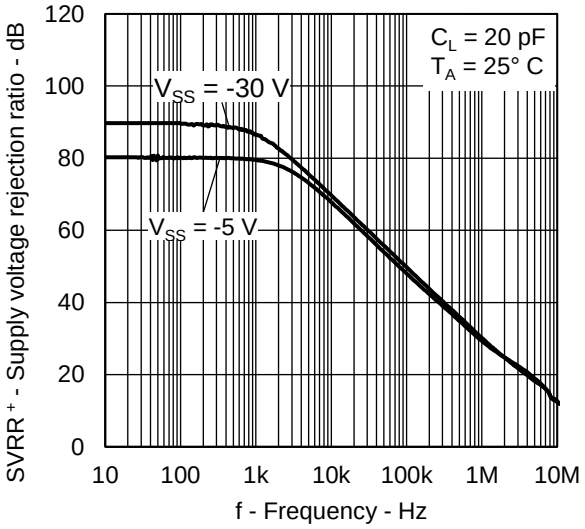
V_{om} vs. f



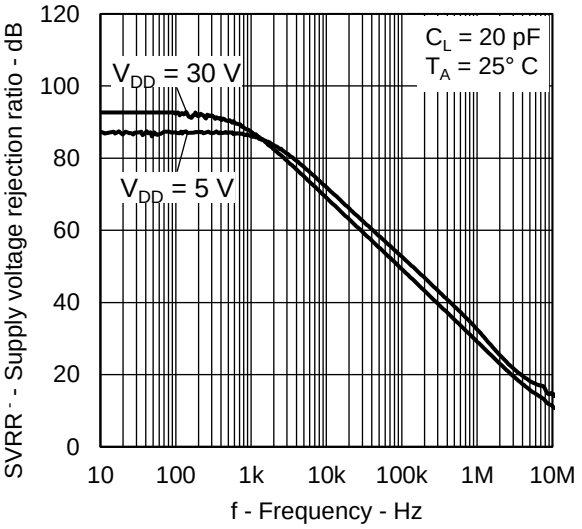
CMRR vs. f



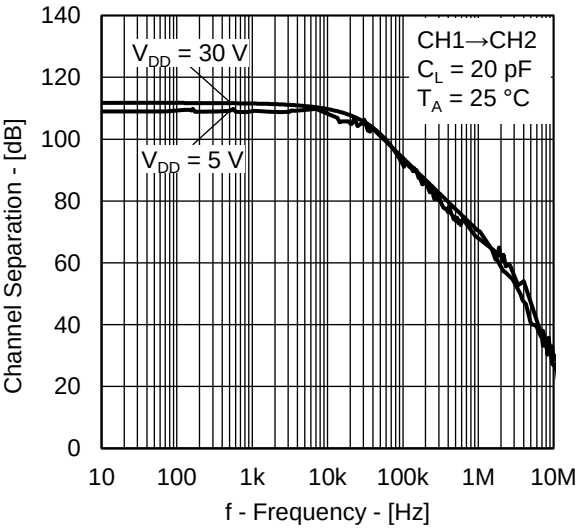
SVRR⁺ vs. f



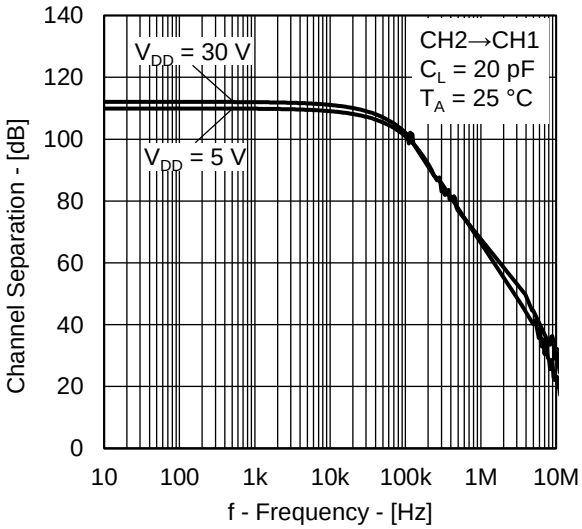
SVRR⁻ vs. f

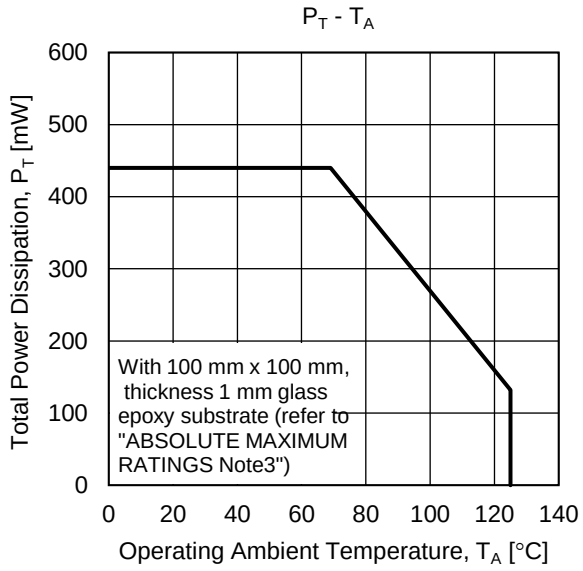


Channel Separation vs. f



Channel Separation vs. f



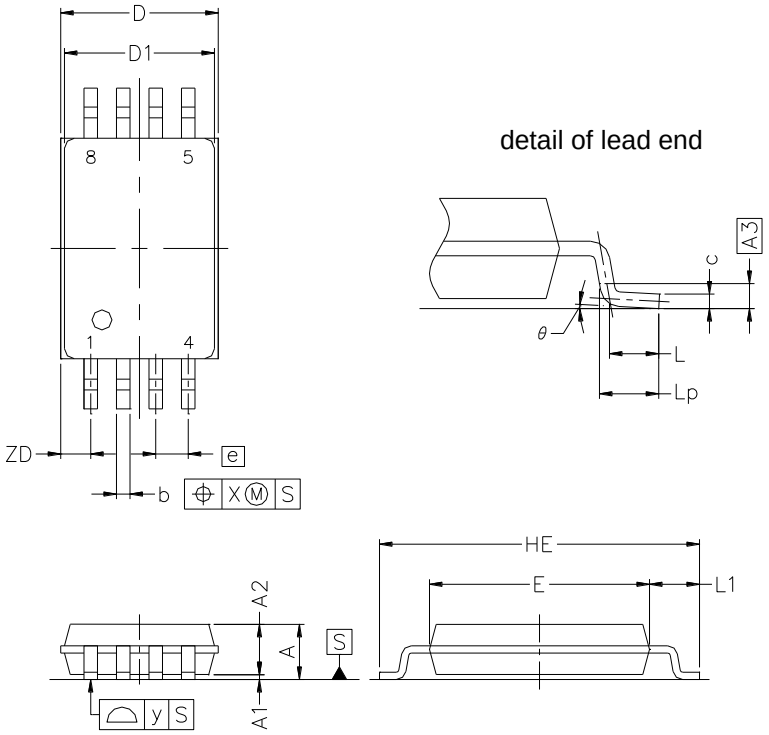

P_T - T_A
600
500
400
300
200
100
0
Total Power Dissipation, P_T [mW]
With 100 mm x 100 mm, thickness 1 mm glass epoxy substrate (refer to "ABSOLUTE MAXIMUM RATINGS Note3")
0
20
40
60
80
100
120
140
Operating Ambient Temperature, T_A [°C]

Package Dimensions

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—

Unit : mm



NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 +0.06 -0.05
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° +5° -3°
e	0.65
x	0.10
y	0.10
ZD	0.60

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