REAR56957A,BG

Voltage Detecting, System Resetting IC Series

R03DS0170EJ0100
Rev.1.00
2021.10.4

Description

REAR56957A,B are semiconductor integrated circuits for resetting of all types of logic circuit such as CPUs, and have the feature of setting the detection voltage by adding external resistance.

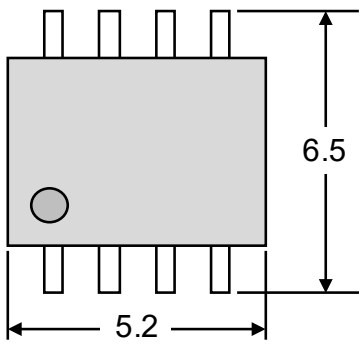
They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor.

They fined extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

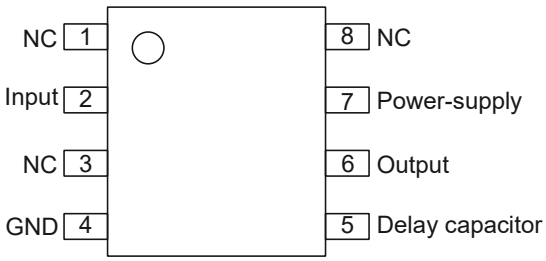
Features

- Few external parts
- Large delay time with a capacitor of small capacitance (td ≈ 100ms, at 0.33μF)
- Low threshold operating voltage (Supply voltage to keep low-state at low supply voltage): 0.6V (Typ.) at RL = 22kΩ
- Wide supply voltage range: 2V to 17V
- Wide application range

Ordering Information

Package Type	SOP	
Part Name	REAR56957AGSM	REAR56957BGSM
Product Type Quality Level	Normal Quality Level	
Outline	Unit : mm 	

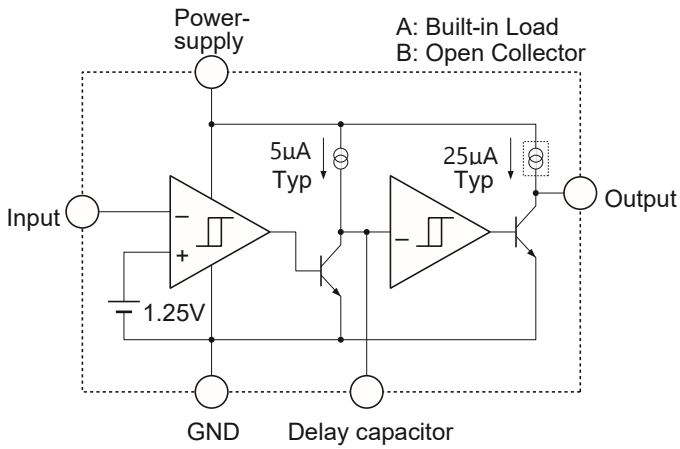
Pin Arrangement



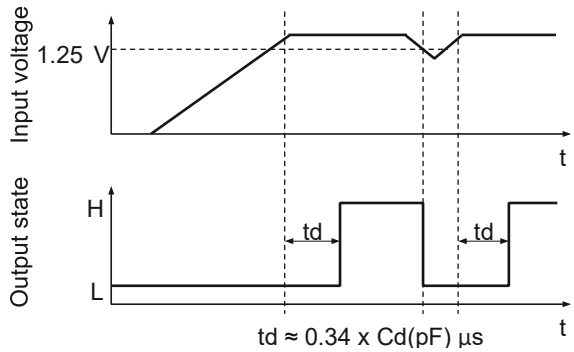
(Top view)

NC: No Connection

Block Diagram



Operating Waveform



Absolute Maximum Ratings

(T_a=25˚C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply Voltage	V_{CC}	-0.3 to +18	V	
Output Sink Current	I_{SINK}	6	mA	
Output Applied Voltage	V_O	-0.3 to V_{CC}	V	Type A (output with constant current load)
		-0.3 to +18		Type B (open collector output)
Total Power Dissipation	Pd	440	mW	
Thermal Derating	Kθ	4.4	mW/˚C	Refer to the thermal derating curve.
Operating Temperature	T_{opr}	-40 to +85	˚C	
Storage Temperature	T_{stg}	-55 to +125	˚C	
Input Voltage Range	V_{IN}	-0.3 to V_{CC}	V	V_{CC} ≤ 7V
		-0.3 to +7		V_{CC} > 7V

Recommended Operating Condition

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2		17	V

Electrical Characteristics

(T_a=25˚C, unless otherwise noted)

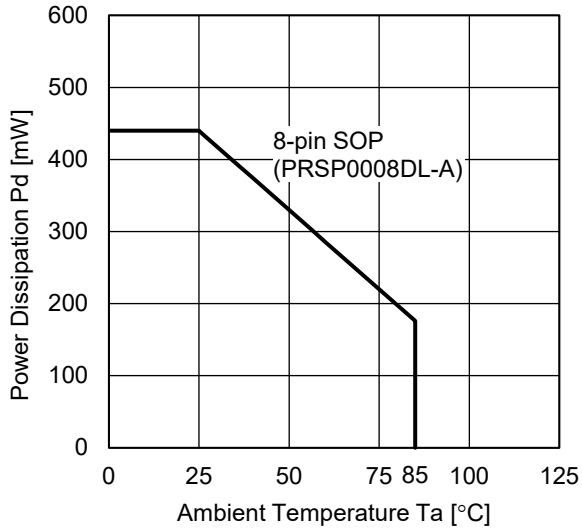
- “L” reset type

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Detecting Voltage	V_S	1.20	1.25	1.30	V		
Hysteresis Voltage	ΔV_S	9	15	23	mV	V_{CC} = 5V	
Detecting Voltage Temperature Coefficient	$V_S/\Delta T$		0.01		%/˚C		
Supply Voltage Range	V_{CC}	2		17	V		
Input Voltage Range	V_{IN}	-0.3		V_{CC}	V	V_{CC} ≤ 7V	
		-0.3		7.0		V_{CC} > 7V	
Input Current	I_{IN}		100	500	nA	V_{IN} = 1.25V	
Circuit Current	I_{CC}		390	590	μA	Type A, V_{CC} = 5V	
			360	540		Type B, V_{CC} = 5V	
Delay Time	t_{pd}	1.6	3.4	7.0	ms	Cd = 0.01μF Note.1	
Constant Current	I_{pd}	-8	-5	-3	μA	V_{CC} = 5V	
Output Saturation Voltage	V_{sat}		0.2	0.4	V	V_{CC} = 5V, V_{IN} < 1.2V, I_{SINK} = 4mA	
Threshold Operating Voltage	V_{OPL}		0.67	0.9	V	L reset type minimum supply voltage for IC operation	R_L = 2.2kΩ, V_{sat} ≤ 0.4V
			0.55	0.8			R_L = 100kΩ, V_{sat} ≤ 0.4V
Output Leakage Current	I_{OH}			30	nA	Type B, V_{out} ≤ 17V	
Output Load Current	I_{OC}	-40	-25	-17	μA	Type A, V_{CC}=5V, V_{IN} > 1.35V, V_O=1/2 × V_{CC}	
Output High Voltage	V_{OH}	V_{CC}-0.2	V_{CC}-0.06		V	Type A	

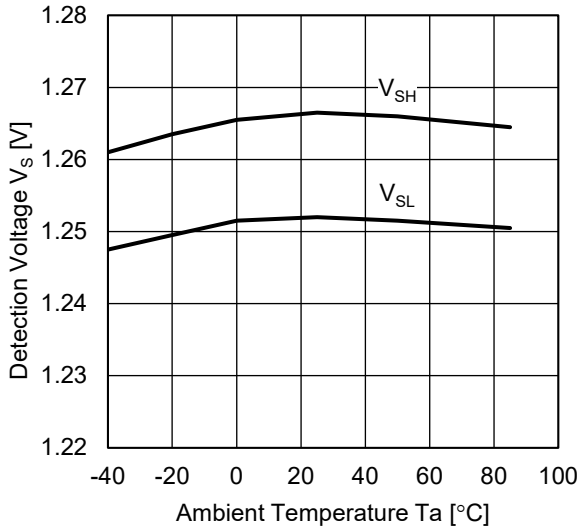
【Note】1. Please set the desired delay time by attaching capacitor of the range between 4700pF and 10μF

Typical Characteristics

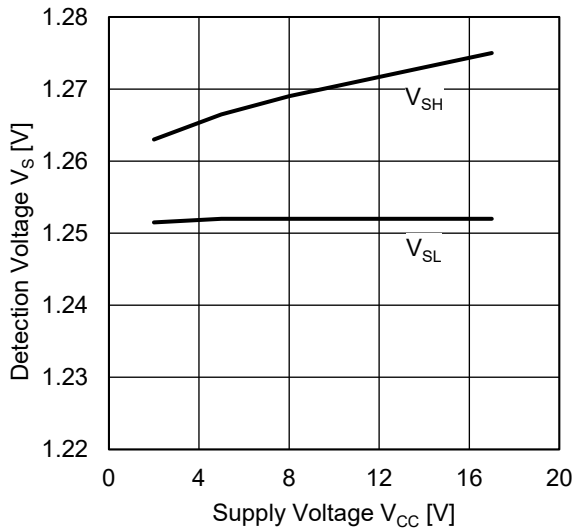
Thermal Derating



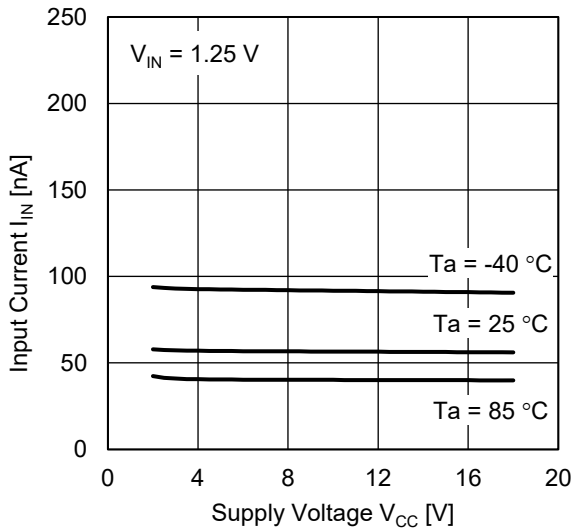
Detection Voltage vs. Ambient Temperature



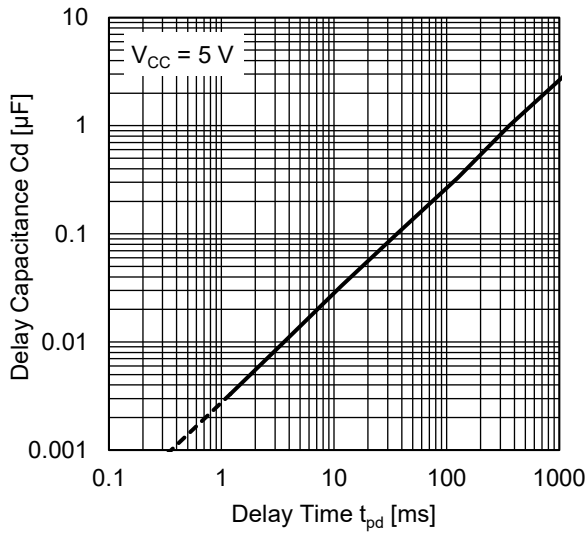
Detection Voltage vs. Supply Voltage



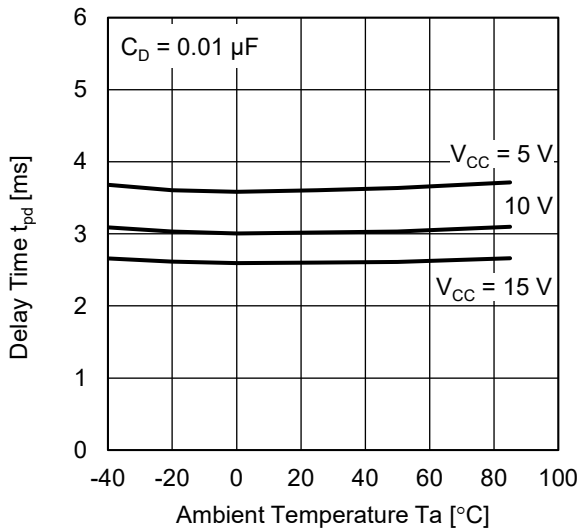
Input Current vs. Supply Voltage



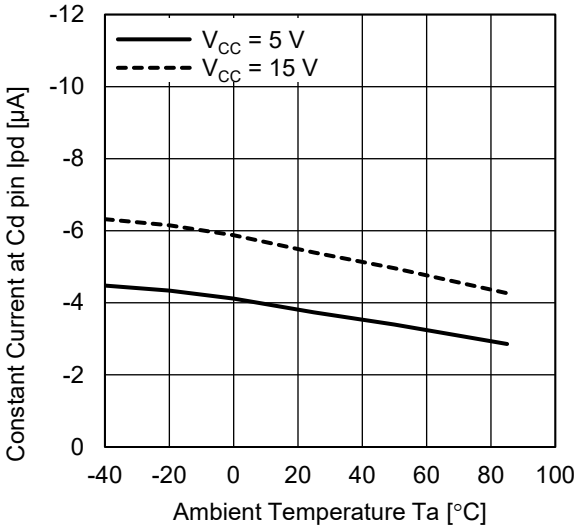
Delay Capacitance vs. Delay Time



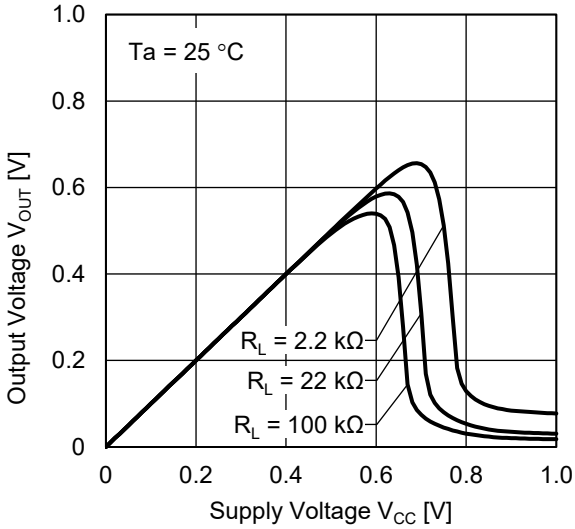
Delay Time vs. Ambient Temperature



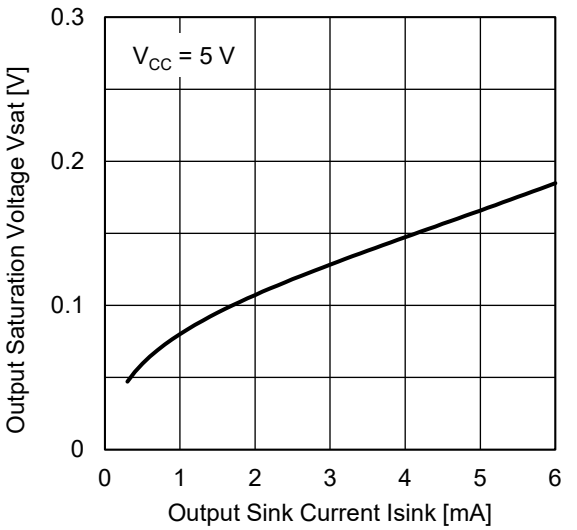
Constant Current at Cd pin vs. Ambient Temperature



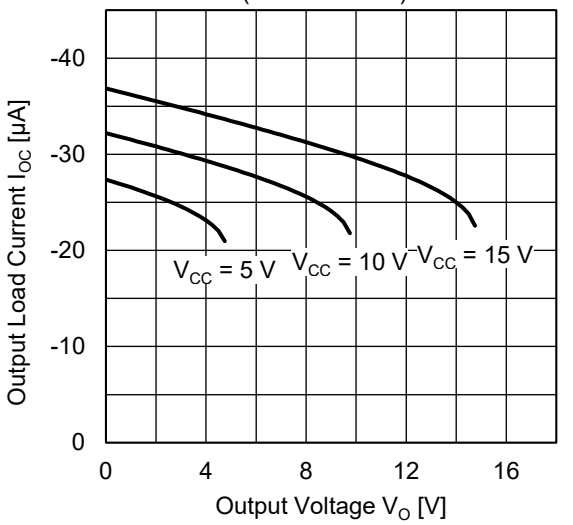
Threshold Operating Voltage



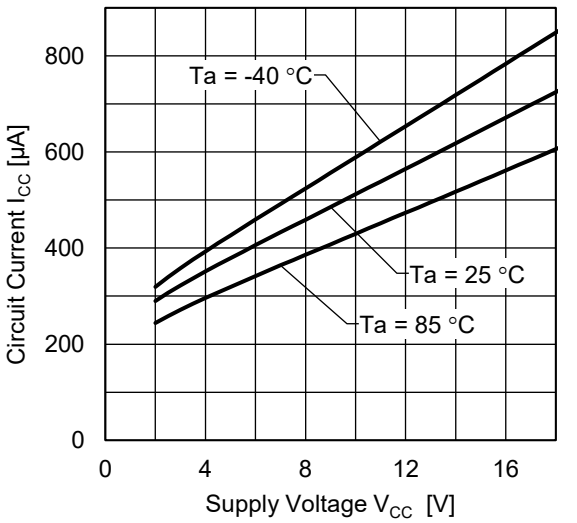
Output Saturation Voltage vs. Output Sink Current



Output Load Current vs. Output Voltage (REAR56957A)



Circuit Current vs. Supply Voltage (REAR56957B)

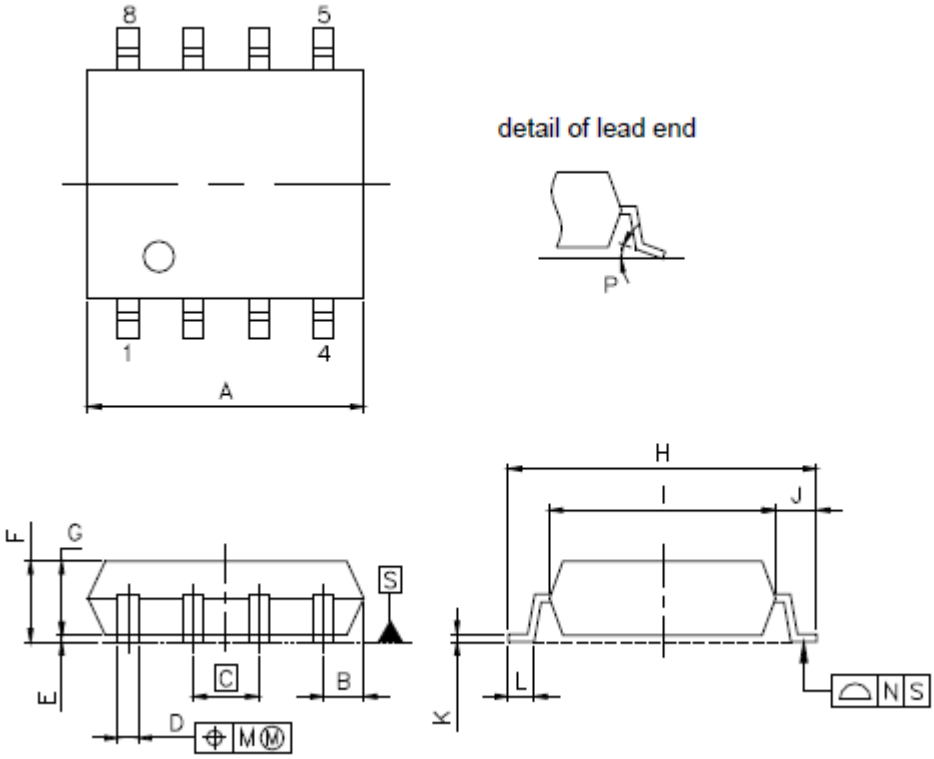


Package Drawing

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-SOP8-0225-1.27	PRSP0008DL-A	S8GM-50-225B	0.08

Unit: mm



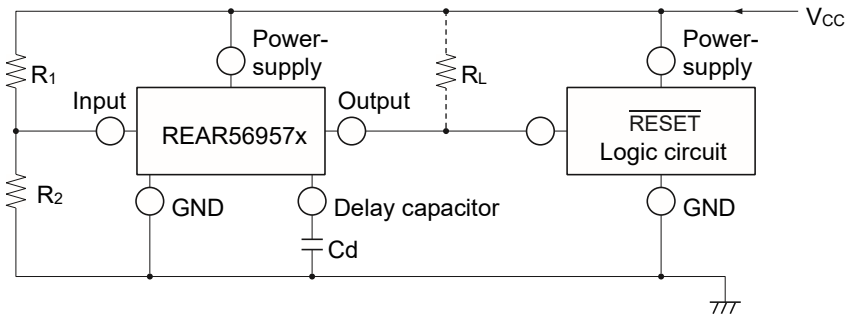
NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 +0.17 -0.20
B	0.78 MAX
C	1.27 (T.P)
D	0.42 +0.08 -0.07
E	0.1 ±0.1
F	1.59 ±0.21
G	1.49
H	6.5 ±0.3
I	4.4 ±0.15
J	1.1 ±0.2
K	0.17 +0.08 -0.07
L	0.6 ±0.2
M	0.12
N	0.10
P	3° +7° -3°

Example of Application Circuit

Reset Circuit of REAR56957



Reset Circuit of REAR56957

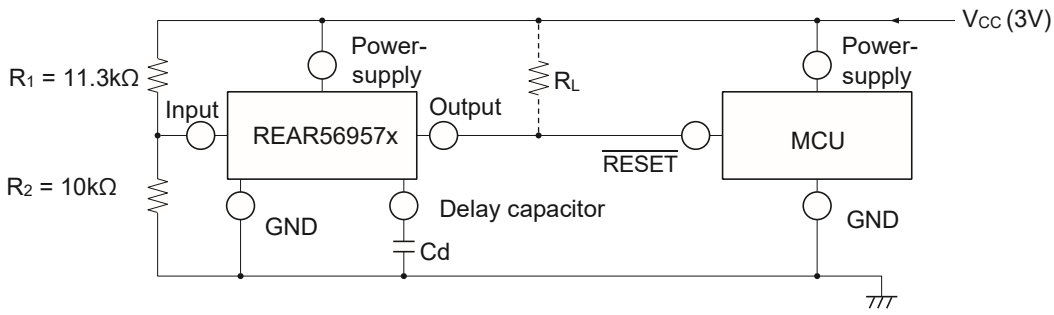
Notes : 1. The detecting supply voltage is $V_S \times (R_1 + R_2)/R_2$ (V) approximately. V_S = 1.25 V (Typ)
The detecting supply voltage can be set between 2 V and 15 V
2. The delay time is about 0.34 × Cd (pF) µs.
3. If the REAR56957 and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
4. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor R_L to overcome the pull-down resistor.
5. When a negative supply voltage is used, the supply voltage side of REAR56957 and the GND side are connected to negative supply voltage respectively.

Application Example on 3V Microcontroller System

The input voltage detection type can be used for voltage monitoring of 3V microcontroller system as shown on Figure .

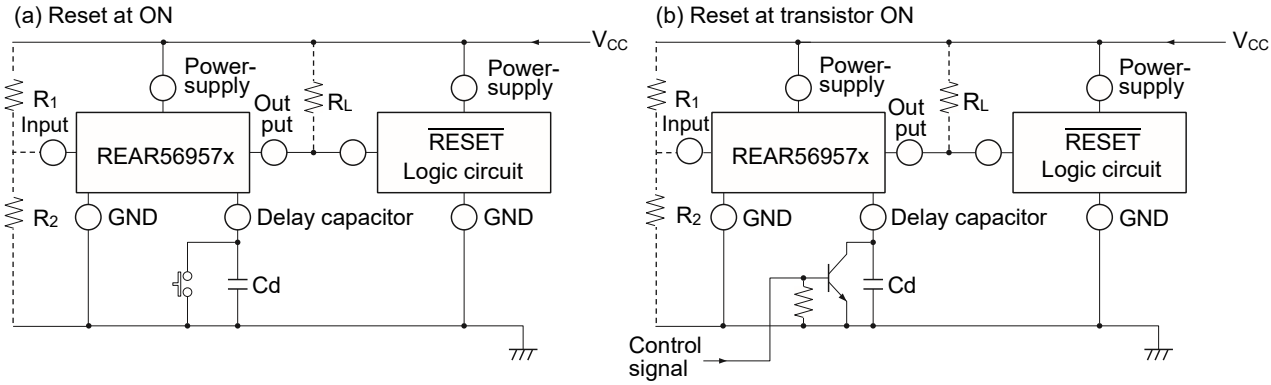
The constant in Figure sets the detection voltage to 2.66V (TYP). However, the detection voltage can be adjusted by changing R_1 or R_2.

The detection accuracy of the IC alone is ±4%.



Application Example on 3V Microcontroller System

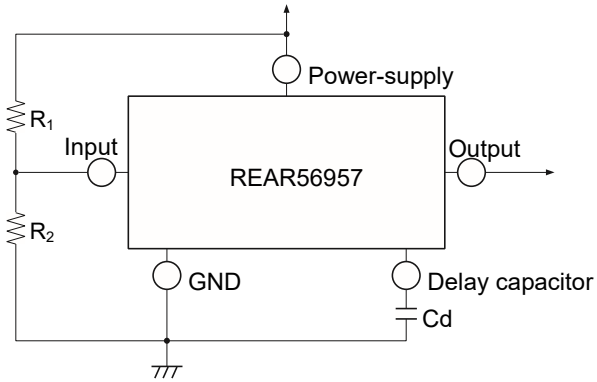
Case of Using Reset Signal except Supply Voltage in the REAR56957



Case of Using Reset Signal except Supply Voltage in the REAR56957

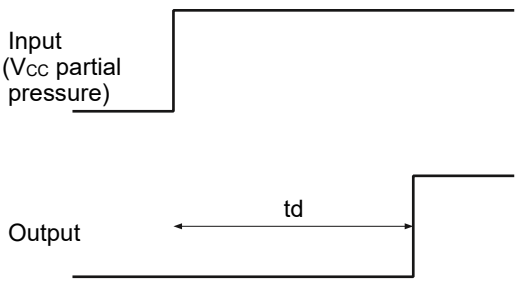
Delay Waveform Generating Circuit

When REAR56957 are used, a waveform with a large delay time can generate only by adding a small capacitor.



Delay Waveform Generating Circuit

Operating Waveform



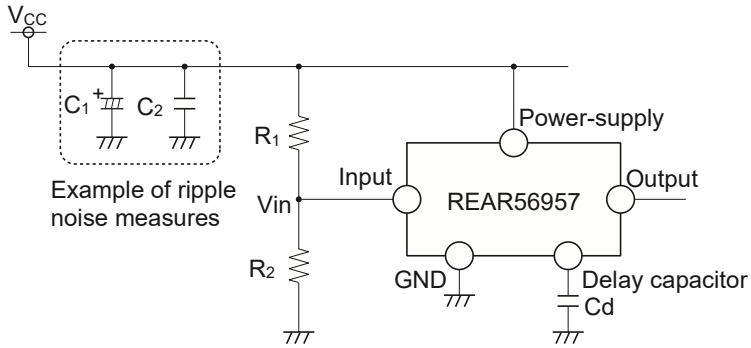
$td \approx 0.34 \times Cd(pF)\ \mu s$

Operating Waveform

Notice for use

About the Power Supply Line

1. About bypass capacitor
   Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.
   Therefore, please install C_1 and C_2 for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure.



Example of Ripple Noise Measures

2. The sequence of voltage impression
   Please do not impress the voltages to the input terminals earlier than the power supply terminal. Moreover, please do not open the power supply terminal with the voltage impressed to the input terminal. (The setting of the bias of an internal circuit collapses, and a parasitic element might operate.)

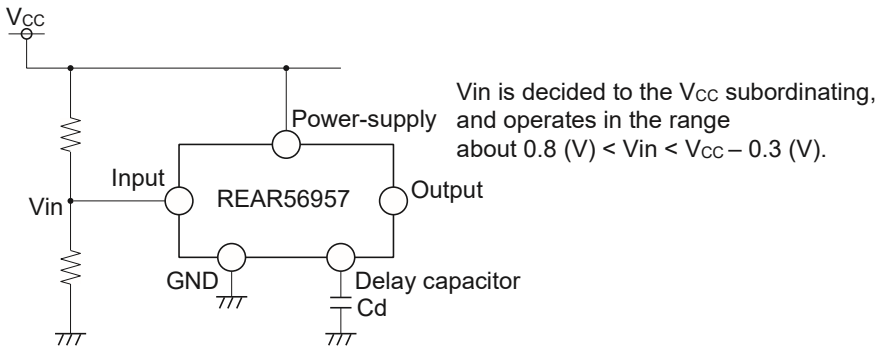
About the Input Terminal

1. Setting range of input voltage
   The following voltage is recommended to be input to the input terminal (pin 2).

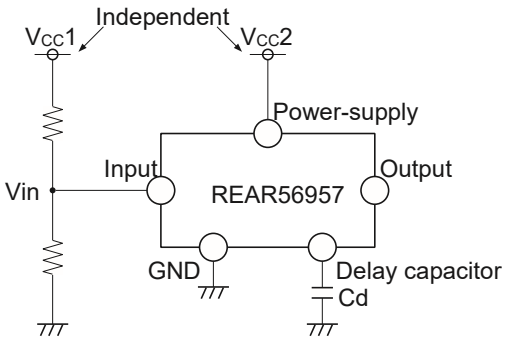
   about 0.8 (V) < Vin < V_{CC} – 0.3 (V) ... at V_{CC} ≤ 7 V

   about 0.8 (V) < Vin < 6.7 (V) ..... at V_{CC} > 7 V

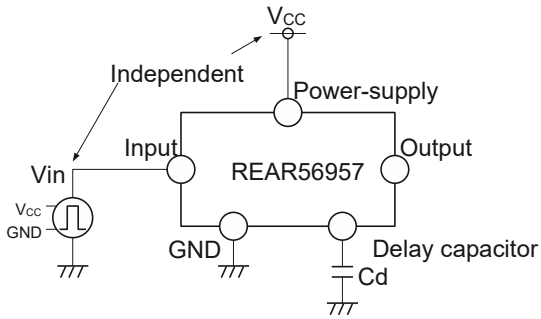
2. About using input terminal
   Please do an enough verification to the transition characteristic etc. of the power supply when using independent power supply to input terminal (pin 2).



Recommended Example of Circuit



Example 1. Independent power supply system
Please do enough verifying about transition characteristic of $V_{CC}1$ and $V_{CC}2$

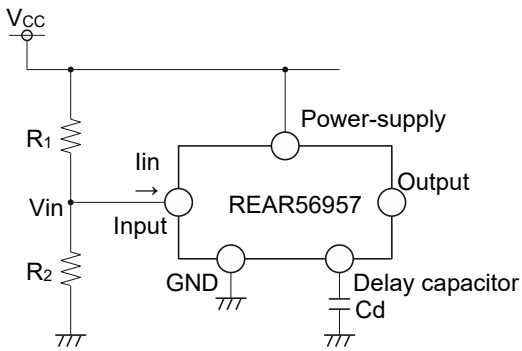


Example 2. Logic pulse input
(not recommended)

3. Calculation of detecting voltage

Detecting voltage Vs can be calculated by the following expression.
However, the error margin is caused in the detecting voltage because input current Iin (standard 100 nA) exists if it sets too big resistance.
Please set the constant to disregard this error margin.

$$V_S = 1.25 \times \left(\frac{R_1 + R_2}{R_2} \right) + \underbrace{Iin \times R_1}_{\text{error margin}}$$



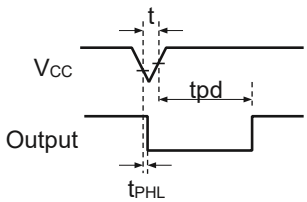
Influence of Input Current

4. About the voltage input outside ratings

Please do not input the voltage outside ratings to the input terminal.
An internal protection diode becomes order bias, and a large current flows.

Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 µF or less.
When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.



Time Chart at Momentary Voltage-Decrease

(1) The difference at delay time becomes remarkable.
A long delay setting of tens of seconds is fundamentally possible. However, when set delay time is lengthened, the range of the difference relatively grows, too. When a set value is assumed to be 'tpd', the difference occurs in the range from 0.47 × tpd to 2.05 × tpd. For instance, 34 seconds can be calculated at 100 µF. However, it is likely to vary within the ranges of 16-70 seconds.

(2) Difficulty to react to a momentary voltage decrease.
For example, the reaction time t_{PHL} is 10 µs when delay capacitor Cd = 0.1 µF.

The momentary voltage-decrease that is longer than such t_{PHL} are occurs, the detection becomes possible. When the delay capacitance is enlarged, t_{PHL} also becomes long. For instance, it becomes about 100 to 200 µs in case of circuit constant C1 = 100 µF.

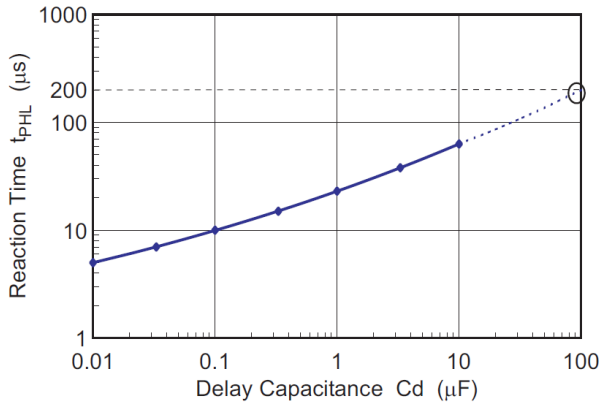
(Characteristic graph 1 is used and extrapolation in case of Cd = 100 µF.)

Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

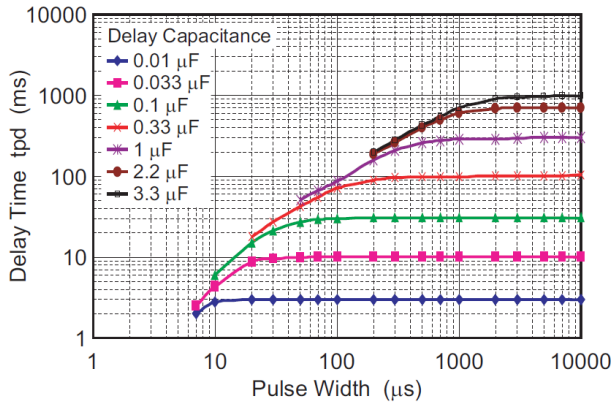
(3) Original delay time is not obtained.
When the momentary voltage-decrease time 't' is equivalent to t_{PHL}, the discharge becomes insufficient and the charge starts at that state. This phenomenon occurs at large capacitance. And, original delay time tpd is not obtained.

Please refer to characteristic graph 2. (Delay time versus input pulse width)

Characteristic Graph 1
Reaction Time vs. Delay Capacitance
(Example data)



Characteristic Graph 2
Delay Time vs. Momentary Voltage Decrease Pulse Width
(Example data)

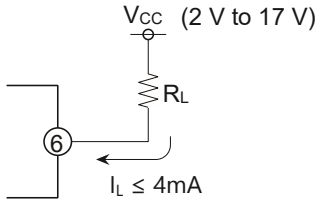


Characteristic Graph

Setting of Output Load Resistance (REAR56957B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation. Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance) R_L so that the output current (output inflow current I_L) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).



Output Load Resistance R_L

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