

Product Introduction

Concept

The RH850/F1x microcontroller focus on low power and low cost for the body application.

The device is a high-end microcontroller with a 32-bit RH850G3M core for car body control. The features of this device are the low power consumption, the high processing power and the variable peripheral function.

In particular, Low power consumption is achieved by supporting wide stand-by control and the power supply insulation using the port polling, stand-by control of AD conversion and LIN communication which considered body control application.

This device supports the security and safety function. And the local area network has been strengthened by upgrading each module of CAN, LIN master/slave.

Function overview

Refer to *the RH850/F1H User's manual: Hardware*.

Block diagram

Refer to *the RH850/F1H User's manual: Hardware*.

Pin map

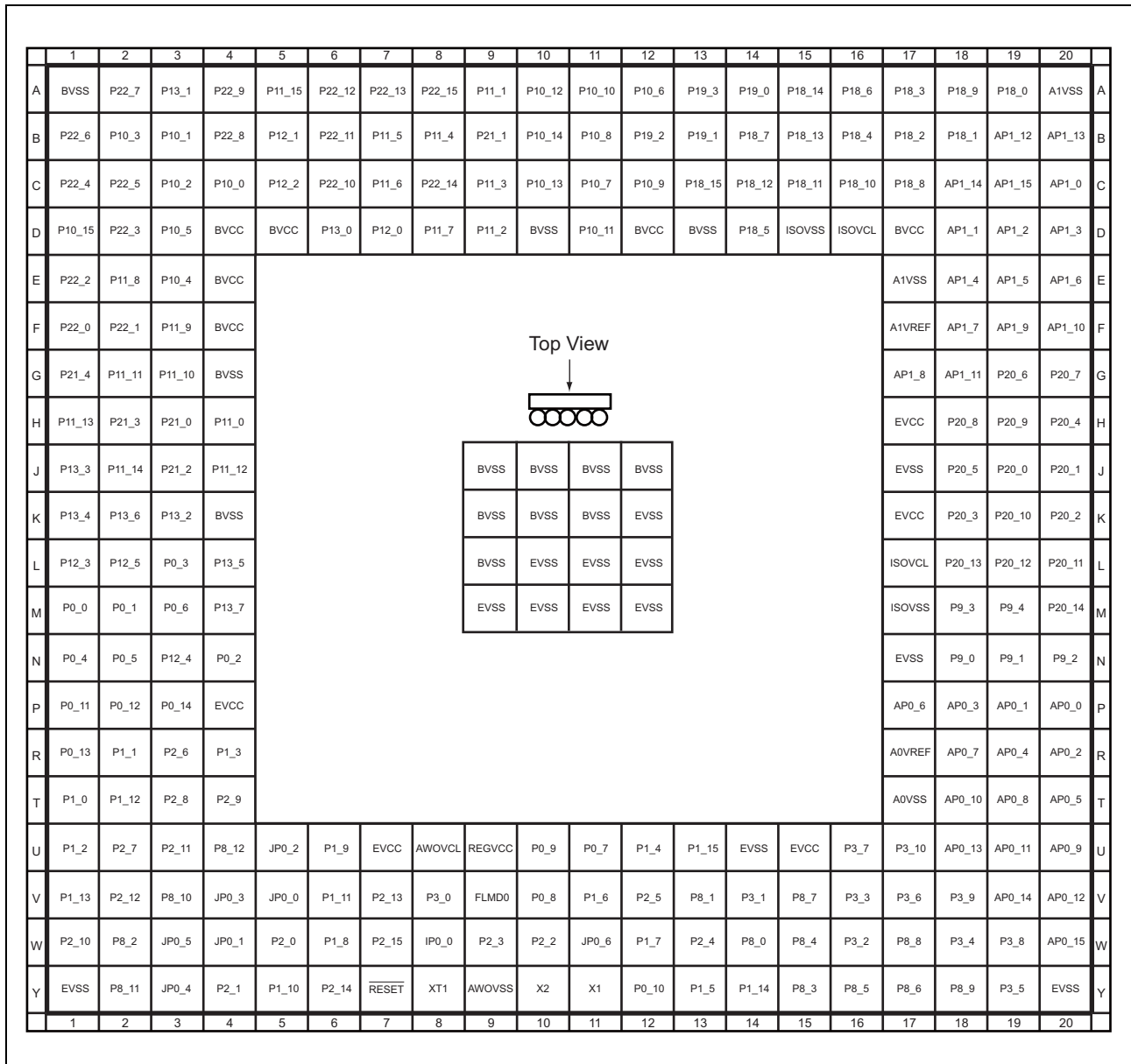


Figure 1.1 Pin Connection Diagram (272 pin FPBGA)

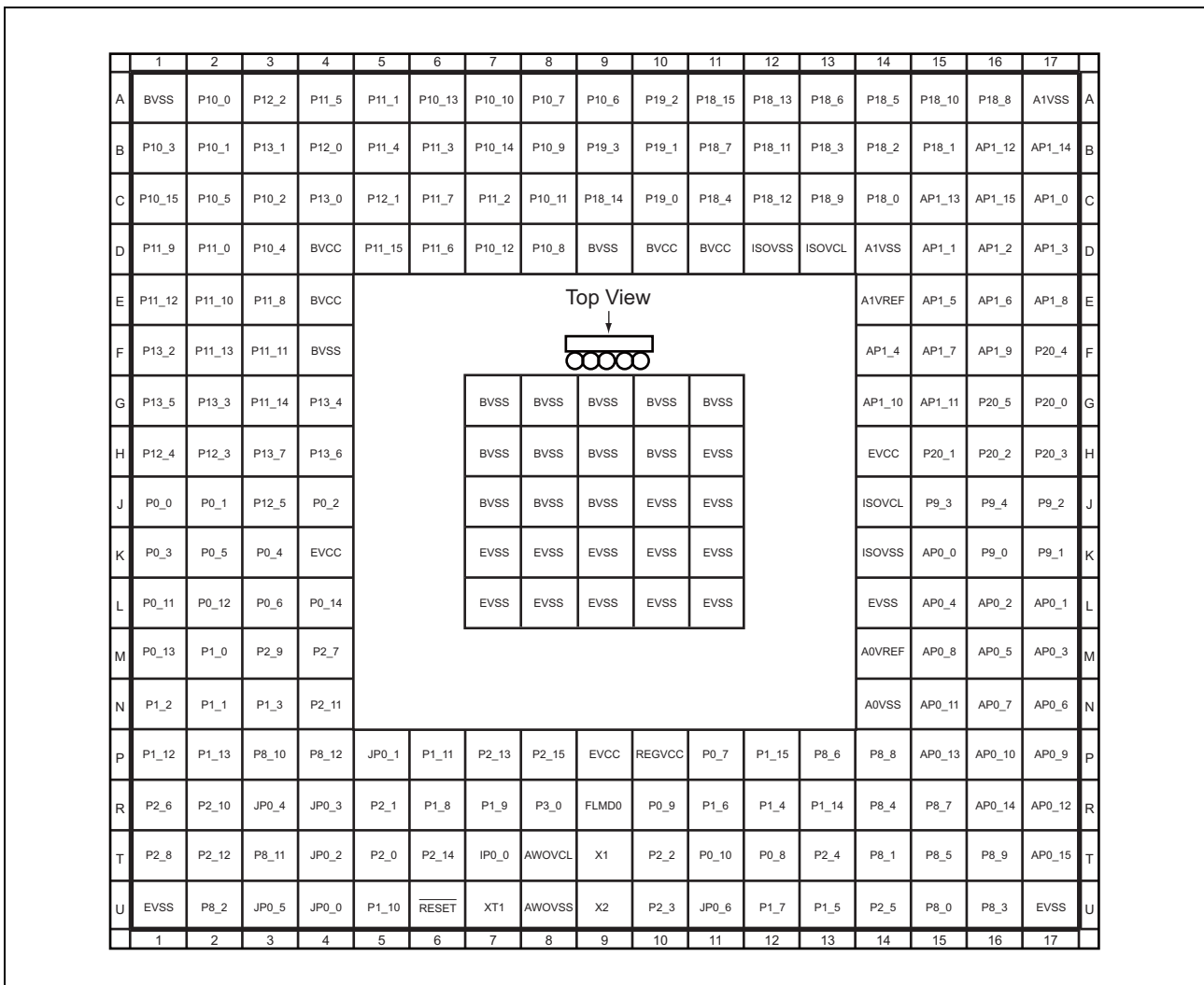


Figure 1.2 Pin Connection Diagram (233 pin FPBGA)

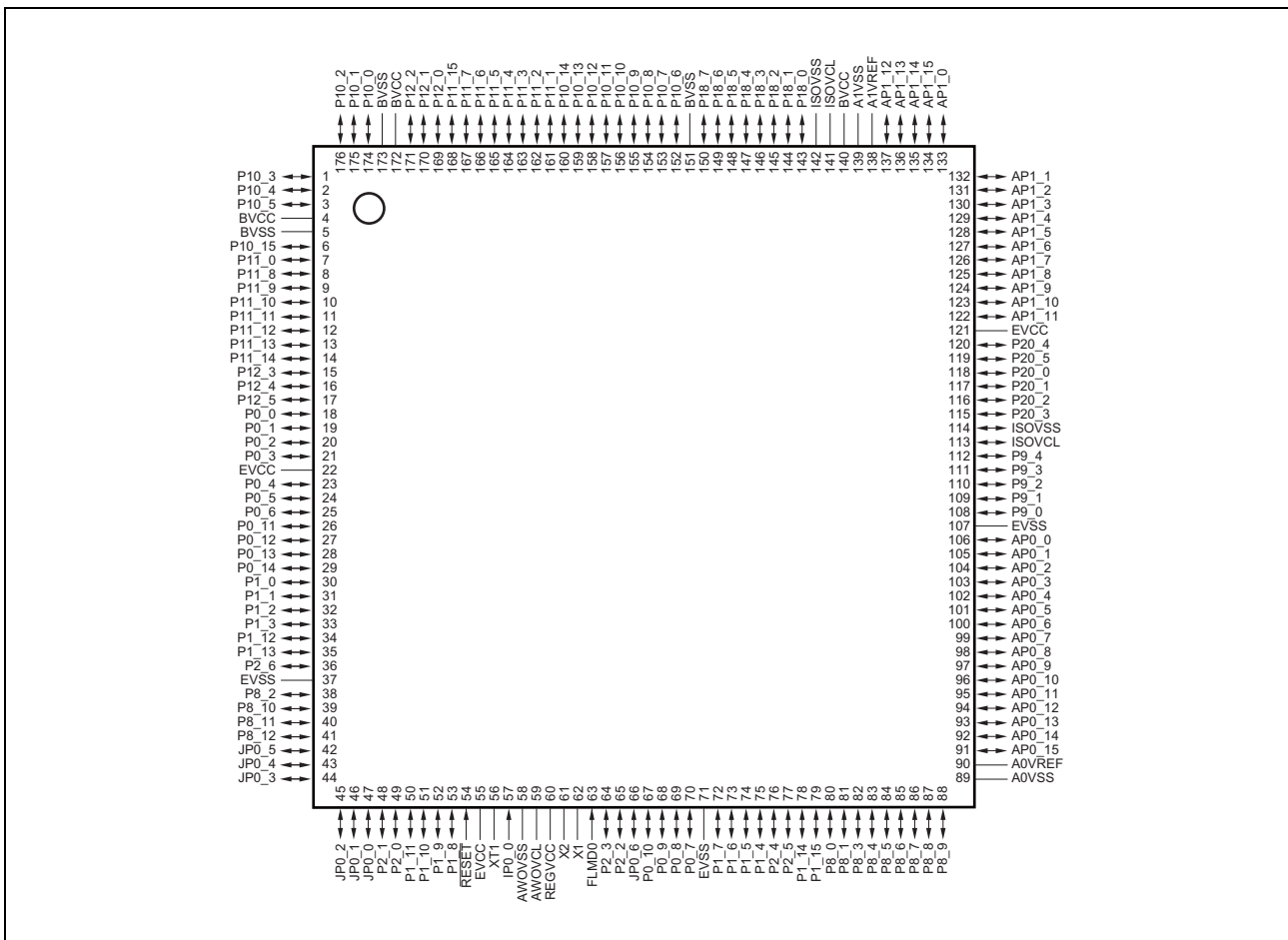


Figure 1.3 Pin Connection Diagram (176 pin LQFP)

Product Lineup

Pin Count	Memory						Part Name		Line Name
	Code Flash	CPU1 (Core #1)	CPU2 (Core #2)	Global Memory			Operating Temperature (Ta)		
		Local RAM	Local RAM	Data Flash	Global RAM	Retention RAM (RRAM)	-40°C to +105°C	-40°C to +125°C	
176 pin	3 MB	112 KB	112 KB	64 KB	32 KB	64 KB	R7F7015013AFP	R7F7015014AFP	ECO
	4 MB	128 KB	128 KB		64 KB	64 KB	R7F7015023AFP	R7F7015024AFP	ECO
	6 MB	192 KB	192 KB		64 KB	128 KB	R7F7015033AFP	R7F7015034AFP	ECO
233 pin	3 MB	112 KB	112 KB	64 KB	32 KB	64 KB	R7F7015063ABG	R7F7015064ABG	ECO
	4 MB	128 KB	128 KB		64 KB	64 KB	R7F7015073ABG	R7F7015074ABG	ECO
	6 MB	192 KB	192 KB		64 KB	128 KB	R7F7015083ABG	R7F7015084ABG	ECO
272 pin	3 MB	112 KB	112 KB	64 KB	32 KB	64 KB	R7F7015113ABG	R7F7015114ABG	ECO
	4 MB	128 KB	128 KB		64 KB	64 KB	R7F7015123ABG	R7F7015124ABG	ECO
	6 MB	192 KB	192 KB		64 KB	128 KB	R7F7015133ABG	R7F7015134ABG	ECO
176 pin	3 MB	192 KB	192 KB	64 KB	64 KB	128 KB	R7F7015213AFP	R7F7015214AFP	Gateway
	4 MB	256 KB	256 KB		96 KB	128 KB	R7F7015223AFP	R7F7015224AFP	Gateway
233 pin	3 MB	192 KB	192 KB	64 KB	64 KB	128 KB	R7F7015243ABG	R7F7015244ABG	Gateway
	4 MB	256 KB	256 KB		96 KB	128 KB	R7F7015253ABG	R7F7015254ABG	Gateway
176 pin	3 MB	112 KB	112 KB	64 KB	32 KB	64 KB	R7F7015263AFP	R7F7015264AFP	PREMIUM
	4 MB	128 KB	128 KB		64 KB	64 KB	R7F7015273AFP	R7F7015274AFP	PREMIUM
233 pin	3 MB	112 KB	112 KB	64 KB	32 KB	64 KB	R7F7015283ABG	R7F7015284ABG	PREMIUM
	4 MB	128 KB	128 KB		64 KB	64 KB	R7F7015293ABG	R7F7015294ABG	PREMIUM

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj (**Section 1.2.4, Temperature Condition**) and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Section 1 Electrical Specifications

1.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

1.1.1 Pin Groups

1.1.1.1 272 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
Pg R	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
Pg E	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20 Related pins: RESET,
Pg B	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19, P21, P22
Pg A0	A0VREF, A0VSS	Related port: AP0
Pg A1	A1VREF, A1VSS	Related port: AP1

1.1.1.2 233 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
Pg R	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
Pg E	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20 Related pins: RESET, FLMD0
Pg B	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19
Pg A0	A0VREF, A0VSS	Related port: AP0
Pg A1	A1VREF, A1VSS	Related port: AP1

1.1.1.3 176 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
Pg R	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
Pg E	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P8, P9, P20 Related pins: RESET, FLMD0
Pg B	BVCC, BVSS	Related ports: P10, P11, P12, P18
Pg A0	A0VREF, A0VSS	Related port: AP0
Pg A1	A1VREF, A1VSS	Related port: AP1

1.1.2 General Measurement Conditions

1.1.2.1 Common Conditions

Power supply

- REGVCC = EVCC = VPOC*¹ to 5.5 V
- BVCC = VPOC*¹ to REGVCC
- A0VREF = 3.0 V to 5.5 V
- A1VREF = 3.0 V to 5.5 V
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Capacitance on internal regulator

- CAWOVCL: 0.1 μ F +/- 30%
- CISOVCL: 0.1 μ F +/- 30% per pin
- Operating temperature
Ta:
–40 to (depend on the product) $^{\circ}$ C
Tj:
R7F7015xx3AFP: –40 to 130 $^{\circ}$ C
R7F7015xx4AFP: –40 to 150 $^{\circ}$ C
R7F7015xx3ABG: –40 to 130 $^{\circ}$ C
R7F7015xx4ABG: –40 to 150 $^{\circ}$ C

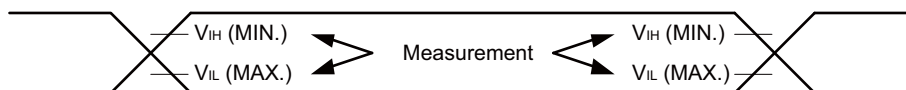
Load conditions

- CL = 30 pF

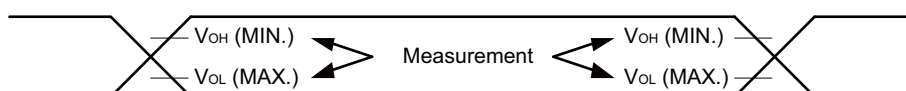
Note 1. “VPOC” means POC (power on clear) detection voltage. For more detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics.**

1.1.2.2 AC Characteristic Measurement Condition

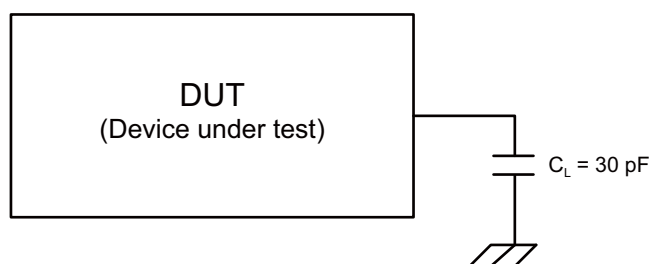
AC test input measurement points



AC test output measurement points



Load conditions



CAUTION

If the load capacitance exceeds 30 pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance till less than 30 pF.

1.2 Absolute Maximum Ratings

CAUTIONS

1. Do not directly connect the output (or input/output) pins to each other, power supply and ground.
2. Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.
3. When designing an external circuit ensure that the connections do not conflict with the port state of this device.

1.2.1 Supply Voltages

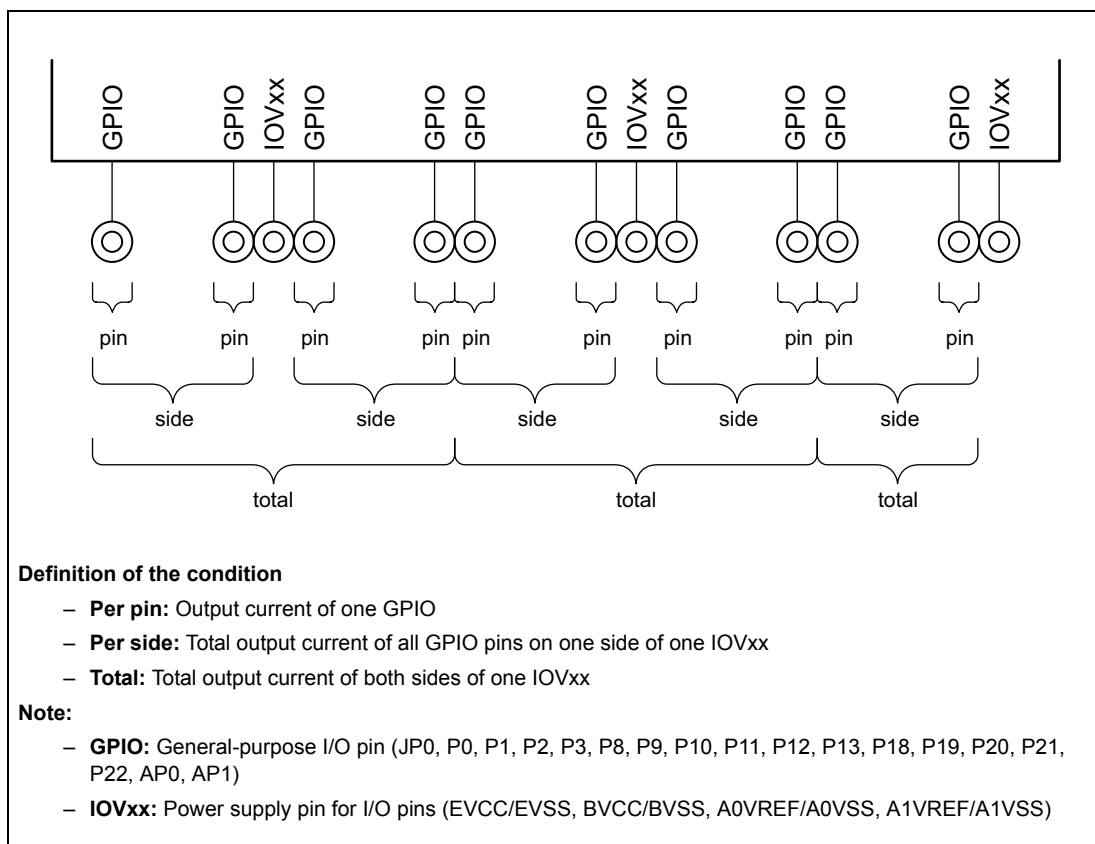
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		-0.5		6.5	V
	AWOVSS		-0.5		0.5	V
	ISOVSS		-0.5		0.5	V
Port supply voltage	EVCC		-0.5		6.5	V
	BVCC		-0.5		6.5	V
	EVSS		-0.5		0.5	V
	BVSS		-0.5		0.5	V
A/D-converter supply voltage	A0VREF		-0.5		6.5	V
	A1VREF		-0.5		6.5	V
	A0VSS		-0.5		0.5	V
	A1VSS		-0.5		0.5	V

1.2.2 Port Voltages

Item	Pin Group ^{*1}	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR	VI		-0.5		REGVCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			-0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgB			-0.5		BVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			-0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V
	PgA1			-0.5		A1VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.2.3 Port Current



1.2.3.1 272 pin

Table 1.1 Port Current (272 pin) (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit		
High level output current	IOH	PgE	Per pin			-10	mA	
			Per side (total of P9_0 to P9_4, P20_10 to P20_14)			-48	mA	
			Per side (total of P20_0 to P20_9)			-48	mA	
			Per side (total of P0_0 to P0_3)			-40	mA	
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			-48	mA	
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0)			-48	mA	
			Per side (total of JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P3_1 to P3_2, P8_0 to P8_1, P8_3 to P8_7)			-48	mA	
			Per side (total of P3_3 to P3_10, P8_8 to P8_9)			-48	mA	
			Total (EVCC)			-60	mA	
		PgB	Per pin				-10	mA
			Per side (total of P18_0 to P18_7)				-48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)				-48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1)				-48	mA
			Per side (total of P10_0 to P10_2)				-30	mA
			Per side (total of P10_3 to P10_5)				-30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7)				-48	mA
			Per side (total of P21_0, P21_2 to P21_4, P22_0 to P22_2)				-48	mA
			Per side (total of P22_3 to P22_8)				-48	mA
			Per side (total of P21_1, P22_9 to P22_15)				-48	mA
Total (BVCC)				-60	mA			
High level output current	IOH	PgA0	Per pin			-10	mA	
			Total (A0VREF)			-48	mA	
		PgA1	Per pin				-10	mA
			Total (A1VREF)			-48	mA	

Table 1.1 Port Current (272 pin) (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Low level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_10 to P20_14)			48	mA
			Per side (total of P20_0 to P20_9)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2 to P2_3)			48	mA
			Per side (total of P1_4 to P1_7, P2_4 to P2_5)			48	mA
			Per side (total of P1_14 to P1_15, P3_1 to P3_2, P8_0 to P8_1, P8_3 to P8_7)			48	mA
			Per side (total of P3_3 to P3_10, P8_8 to P8_9)			48	mA
			Total (EVCC)			60	mA
Low level output current	IOL	PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7)			48	mA
			Per side (total of P21_0, P21_2 to P21_4, P22_0 to P22_6)			48	mA
			Per side (total of P21_1, P22_7 to P22_15)			48	mA
Total (BVCC)			60	mA			
Low level output current	IOL	PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VREF)			48	mA

1.2.3.2 233 pin

Table 1.2 Port Current (233 pin) (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit		
High level output current	IOH	PgE	Per pin			-10	mA	
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			-48	mA	
			Per side (total of P0_0 to P0_3)			-40	mA	
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			-48	mA	
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0)			-48	mA	
			Per side (total of JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			-48	mA	
			Total (EVCC)			-60	mA	
		PgB	Per pin				-10	mA
			Per side (total of P18_0 to P18_7)				-48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)				-48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1)				-48	mA
			Per side (total of P10_0 to P10_2)				-30	mA
			Per side (total of P10_3 to P10_5)				-30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7)				-48	mA
		Total (BVCC)				-60	mA	
		PgA0	Per pin				-10	mA
			Total (A0VREF)				-48	mA
		PgA1	Per pin				-10	mA
			Total (A1VREF)				-48	mA

Table 1.2 Port Current (233 pin) (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit			
Low level output current	IOL	PgE	Per pin			10	mA		
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA		
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12)			48	mA		
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA		
			Per side (total of JP0_6, P0_7 to P0_10, P2_2 to P2_3)			48	mA		
			Per side (total of P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			48	mA		
			Total (EVCC)			60	mA		
			PgB	Per pin				10	mA
				Per side (total of P18_0 to P18_7)				48	mA
				Per side (total of P18_8 to P18_15, P19_0 to P19_3)				48	mA
		Per side (total of P10_6 to P10_14, P11_1 to P11_2)					48	mA	
		Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1)					48	mA	
		Per side (total of P10_0 to P10_2)					30	mA	
		Per side (total of P10_3 to P10_5)					30	mA	
		Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7)					48	mA	
		Total (BVCC)					60	mA	
		PgA0		Per pin				10	mA
			Total (A0VREF)				48	mA	
		PgA1	Per pin				10	mA	
			Total (A1VREF)				48	mA	

1.2.3.3 176 pin

Table 1.3 Port Current (176 pin) (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit		
High-level output current	IOH	PgE	Per pin			-10	mA	
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			-48	mA	
			Per side (total of P0_0 to P0_3)			-40	mA	
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6, P8_2, P8_10 to P8_12)			-48	mA	
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1)			-48	mA	
			Per side (total of JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			-48	mA	
			Total (EVCC)			-60	mA	
		PgB	Per pin				-10	mA
			Per side (total of P10_6 to P10_9, P18_0 to P18_7)				-48	mA
			Per side (total of P10_10 to P10_14, P11_1 to P11_7, P11_5, P12_0 to P12_2)				-48	mA
			Per side (total of P10_0 to P10_2)				-30	mA
			Per side (total of P10_3 to P10_5)				-30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5)				-48	mA
			Total (BVCC)				-60	mA
		PgA0	Per pin				-10	mA
			Total (A0VREF)				-48	mA
		PgA1	Per pin				-10	mA
			Total (A1VREF)				-48	mA

Table 1.3 Port Current (176 pin) (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2 to P2_3)			48	mA
			Per side (total of P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5)			48	mA
		Total (BVSS)			60	mA	
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VSS)			48	mA

1.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		-55		170	°C
Junction temperature	Tj	R7F7015xx3AFP	-40		130	°C
		R7F7015xx4AFP	-40		150	°C
		R7F7015yy3ABG	-40		130	°C
		R7F7015yy4ABG	-40		150	°C

xx = 01, 02, 03, 21, 22
yy = 11, 12, 13, 24, 25, 63, 73, 83

Regarding operation temperature of each product, refer to “**Product Lineup**”.

1.3 Capacitance

Condition: REGVCC = EVCC = BVCC = A0VREF = A1VREF = AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz			10	pF
Input/Output capacitance	CIO*2	0 V for non measurement pins			10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

1.4 Operational Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f _{CPUCLK}	for CPU1 PLL mode (Fixed frequency mode) SSCG mode (Dithered frequency mode) for CPU2			120	MHz
Peripheral clock frequency	f _{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f _{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
	f _{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f _{CKSCLK_AADCA}	for ADCA0			40	MHz
	f _{CKSCLK_AFOUT}	for CSCXFOUT			30	MHz
	f _{CKSCLK_IPERI1}	for TAUD0 for TAUJ1 for ENCA0 for TAPA for PIC			80	MHz
	f _{CKSCLK_IPERI2}	for TAUBn for PWM-diag,			60	MHz
	f _{CKSCLK_ILIN}	for RLIN2n for RLIN3n			60	MHz
	f _{CKSCLK_AADCA}	for ADCA1			40	MHz
	f _{CKSCLK_ICAN}	for RS-CANn (pclk)			80	MHz
	f _{CKSCLK_ICANOSC}	for RS-CANn (clk_xincan)			24	MHz
	f _{CKSCLK_ICSI}	for CSIGn for CSIHn			80	MHz
	f _{RL}	for WDTA1 for WDTA2			240*2	kHz
	f _{CPUCLK2}	for FLXA (hclk) for Ether for OSTMn for MEMC*4			60	MHz
	f _{PPLLCLK}	for FLXA (clk)			80	MHz
f _{CPUCLK4}	for RIIC			30	MHz	
f _{EMCLK}	for LPS			8	MHz	
Power supply range	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	BVCC		VPOC*3		REGVCC	V
	A0VREF		3.0		5.5	V
	A1VREF					

- Note 1. For clock specification of peripherals, refer to *Section 11, Clock Controller*, in the *RH850/F1H Group User's Manual: Hardware*.
- Note 2. This frequency depends on the internal oscillator (LS IntOSC).
- Note 3. "VPOC" means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on). For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**. In addition, the guaranteed operation in DC characteristic. And AC characteristic is guaranteed when more than 3.0 V. When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.
- Note 4. Divided by 2 on MEMC internal.

1.5 Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC}	Crystal/Ceramic	8		24	MHz
MainOSC Current consumption	I_{MOSC}	Crystal/Ceramic After stabilization		1.9*3	2.3*3	mA
MainOSC oscillation start point	V_{MOSCSP}	Crystal/Ceramic	VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}	Crystal/Ceramic		0.5xREGVCC*3		V
MainOSC oscillation amplitude	V_{MOSCAP}	Crystal/Ceramic	0.4xREGVCC-0.2*3			V
MainOSC oscillation stabilization time	t_{MSTB}	Crystal/Ceramic		*1		ms
SubOSC frequency	f_{SOSC}	Crystal	30	32.768	38	kHz
SubOSC Current consumption	I_{SOSC}	After stabilization		1.5*3	4*3	μ A
SubOSC DC operating point	$V_{SOSDCOP}$			0.65*3		V
SubOSC oscillation stabilization time	t_{SSTB}			*2		s

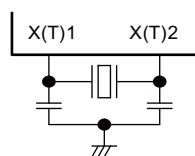
- Note 1. Oscillator stabilization time is time until being set ("1") in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written "1", and depends on the setting value of MOSCST register and EMCLK (8 MHz/240 kHz). Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.
- Note 2. Oscillator stabilization time is time until being set ("1") in SOSCS.SOSCCLKACT bit after SOSCE.SOSCENTRG bit is written "1", and depends on the setting value of SOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.
- Note 3. This is reference value.

CAUTION

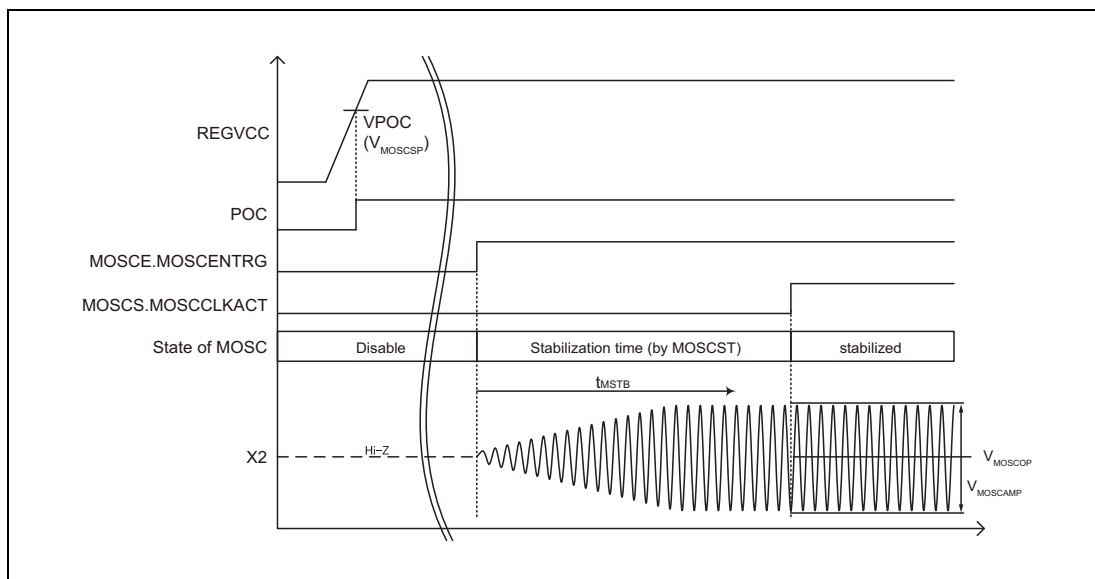
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

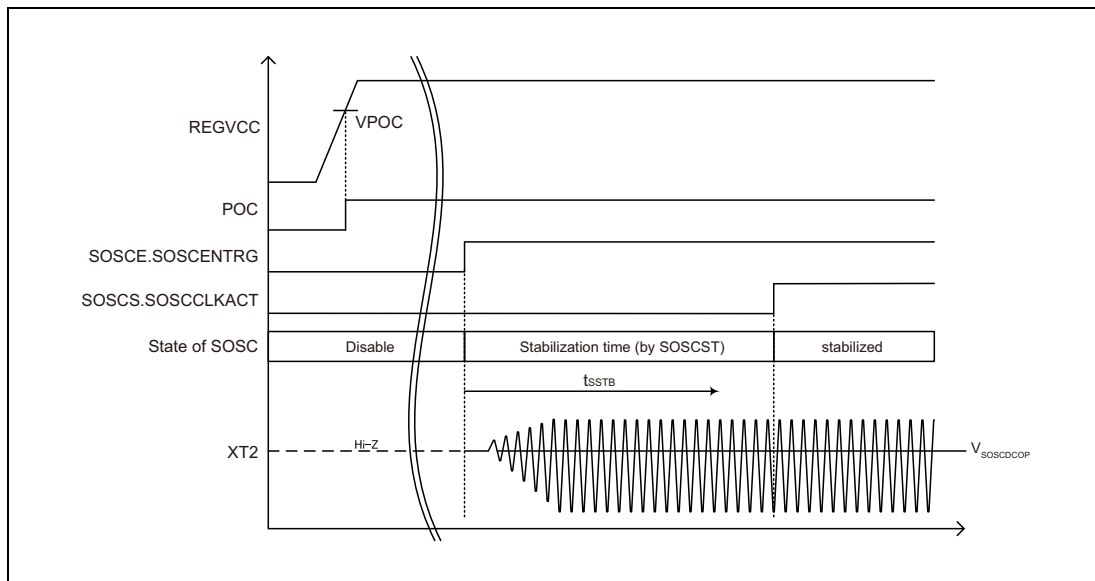
Recommended oscillator circuit is shown below.



MainOSC



SubOSC



1.6 Internal Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/-30%, CISOVCL: 0.1 μ F +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency	f_{RH}		7.36	8	8.64	MHz
		Ta = 25°C	7.6	8	8.4	MHz
HS IntOSC Current consumption	I_{RH}	After stabilization			25* ¹	μ A
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	μ s

Note 1. This is reference value.

1.7 PLL Characteristics

1.7.1 PLL0 (for CPU) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input frequency	f _{SSCGICLK}		8		24	MHz	
Output frequency	f _{SSCGP}	PLL mode	25		120	MHz	
	f _{SSCGS}	SSCG mode	25		120	MHz	
Modulation frequency	f _{MOD}		20		100	kHz	
Frequency dithering range*4	f _{DIT}		±0.82	±1.0	±1.18	%	
			±1.64	±2.0	±2.36	%	
			±2.46	±3.0	±3.54	%	
			±3.28	±4.0	±4.72	%	
			±4.1	±5.0	±5.9	%	
Output period jitter*1	t _{CPJS}	pr = 4*2	-150		150	ps	
		pr = 8*2	-200		200	ps	
		pr = 16*2	-300		300	ps	
Lock time*3	t _{LCKSP}	PLL mode	PLL0ST = 0000 0AA0 _H	314.9	340	369.6	μ s
	t _{LCKS}	SSCG mode	PLL0ST = 0000 1B80 _H	814.9	880	956.6	μ s

Note 1. This is reference value.

Note 2. The following parameters are set by PLL0C register.
- pr: PLL0C.PLL0P2-0 bits

Note 3. Lock time is time until being set ("1") in PLL0S.PLL0CLKACT bit after PLL0E.PLL0ENTRG bit is written "1".

Note 4. "Frequency dithering range" is set by PLL0ADJ[2:0] bits of PLL0C registers.

1.7.2 PLL1 (for Peripheral) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Input frequency	f_{PLLICK}		8		24	MHz	
Output frequency	f_{PLL}		25		80	MHz	
Output period jitter*1	t_{CPJP}	PLL1.OUTBSEL = 0	par = 4^{*2}		150	ps	
			par = 6^{*2} [($f_{\text{PLLICK}} / \text{mr} \times \text{nr}$) = 480 MHz]	-150		150	ps
			par = 6^{*2} [($f_{\text{PLLICK}} / \text{mr} \times \text{nr}$) < 480 MHz]	-200		200	ps
			par = 8^{*2}	-250		250	ps
			par = 16^{*2}	-300		300	ps
		PLL1.OUTBSEL = 1	($f_{\text{PLLICK}} / \text{mr} \times \text{nr}$) = 480 MHz	-150		150	ps
			($f_{\text{PLLICK}} / \text{mr} \times \text{nr}$) < 480 MHz	-200		200	ps
Long term jitter*1	t_{LTJ}	term = 1 μ s	-500		500	ps	
		term = 10 μ s	-1		1	ns	
		term = 20 μ s	-2		2	ns	
Lock time*3	t_{LCKP}		104.0	112.3	122.1	μ s	

Note 1. This is reference value.

Note 2. The following parameters are set by PLL1C register.

- par: PLL1C.PA2-0 bits
- mr: PLL1C.M1-0 bits
- nr: PLL1C.N5-0 bits

Note 3. Lock time is time until being set ("1") in PLL1S.PLL1CLKACT bit after PLL1E.PLL1ENTRG bit is written "1".

1.8 Power Management Characteristics

1.8.1 Regulator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC* ¹		5.5	V
Normal operation voltage	V _{OP}	AWOVCL pin, ISOVCL pin	1.10	1.25	1.35	V
Limited operation voltage	V _{LOP}	AWOVCL pin, ISOVCL pin	1.35		1.43* ³	V
Regulator output voltage	V _{RO}	AWOVCL pin, ISOVCL pin	1.15	1.25	1.35	V
Output voltage	AWOVCL	AWOVCL pin	1.1	1.25	1.35	V
	ISOVCL	ISOVCL pin	1.1	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.1	0.13	μF
	CISOVCL	ISOVCL pin	0.07	0.1	0.13	μF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40* ²	mΩ
	RVRISO	for CISOVCL			40* ²	mΩ
Inrush current during power-on					200* ²	mA

Note 1. "VPOC" means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on).

For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics.**

Note 2. This is reference value.

Note 3. Reliability restrictions from 1.35 V to 1.43 V.

1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/-30%, CISOVCL: 0.1 μ F +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Detection voltage (REGVCC)	VPOC	POC	At power-on (Rise)	2.8	2.95	3.1	V
			After power-on (Fall)	2.8	2.9	3.0	V
	VLVI0	LVI	Rise	3.87	4.0	4.13	V
			Fall	3.9	4.0	4.1	V
	VLVI1		Rise	3.57	3.7	3.83	V
			Fall	3.6	3.7	3.8	V
	VLVI2		Rise	3.37	3.5	3.63	V
			Fall	3.4	3.5	3.6	V
VVLVI	VLVI		1.8	1.9	2.0	V	
Detection voltage (AWOVCL, ISOVCL)	VCMH	CVM	High voltage	1.40	1.50	1.60	V
	VCVML ^{*8}		Low voltage	1.1	1.15	1.20	V
Response time	t _{D_POC1} ^{*6}	POC	At power-on (Rise)	^{*1}		2	ms
				^{*2}		6.3	ms
			After power-on (Rise)	^{*3}		2	ms
				^{*4}		5	ms
	t _{D_POC2} ^{*7}		After power-on (Fall)	^{*5}		5	μ s
	t _{D_LVI}	LVI				2	ms
	t _{D_VLVI}	VLVI		^{*3}		2	ms
				^{*4}		5	ms
t _{D_CVM}	CVM		0.2		10	μ s	
Setup time	t _{S_LVI}	LVI	LVICNT0, 1 bits are set to 1 (except 00 _B), then LVI is ready to operate			80	μ s
REGVCC minimum width	t _{W_POC}	POC		0.2			ms
	t _{W_LVI}	LVI		0.2			ms
	t _{W_VLVI}	VLVI		0.2			ms

Note 1. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms

Note 2. Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms

Note 3. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms

Note 4. Voltage slope (t_{VS}): 20 V/ms < t_{VS} ≤ 500 V/ms

Note 5. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms

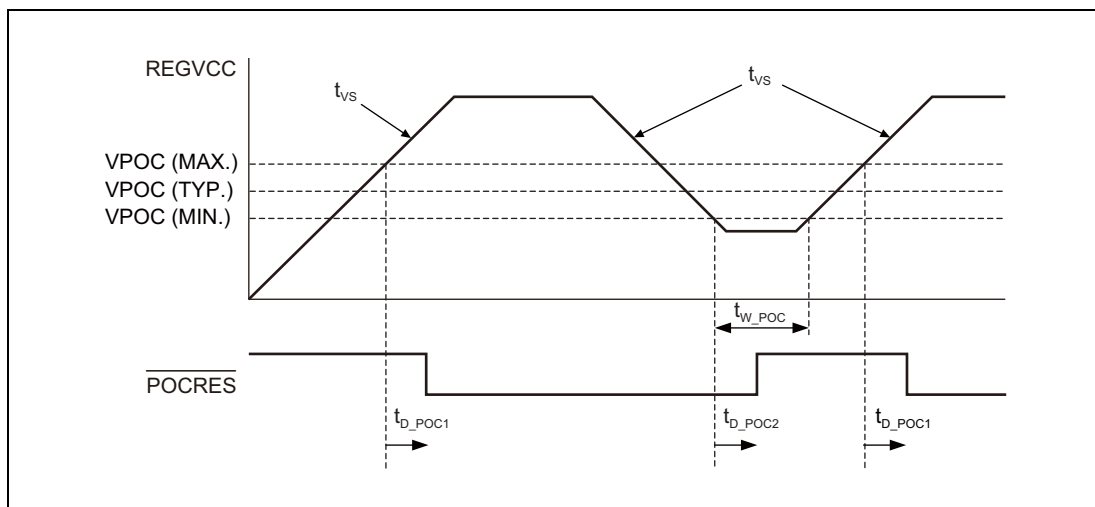
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.

Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.

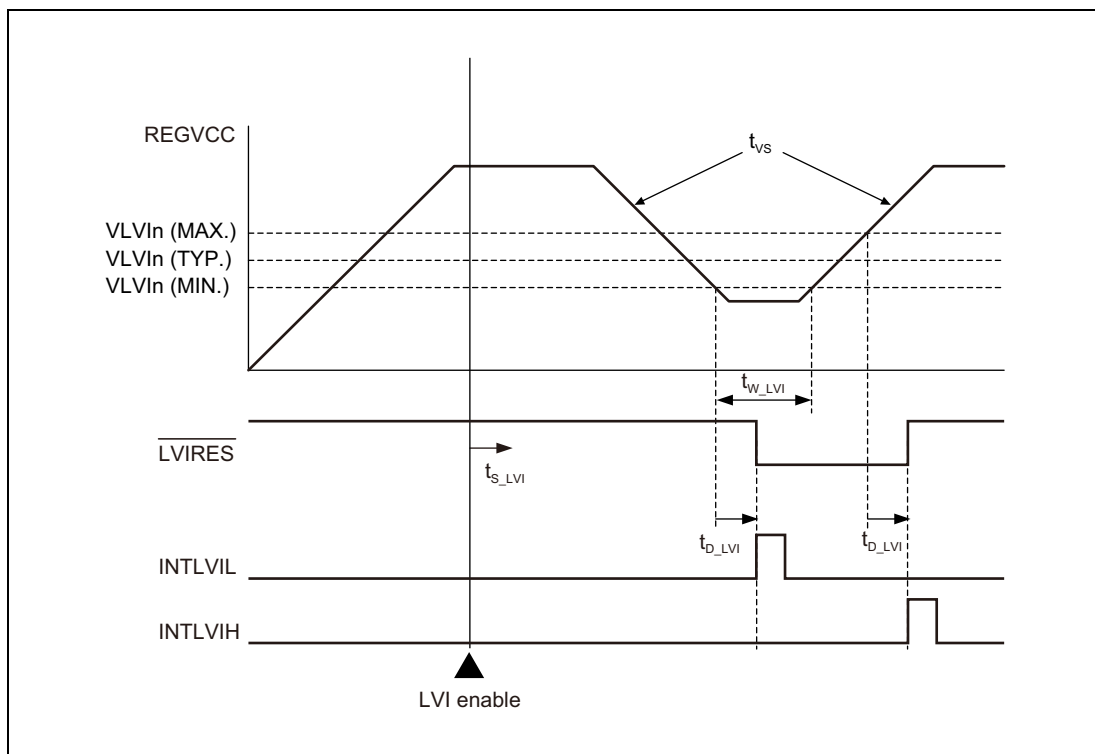
Note 8. The CVM monitors the internal voltage regulator output to ensure that AWOVCL/ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage AWOVCL or ISOVCL outside the specified level of VCMH and VCML is not ensured by CVM.

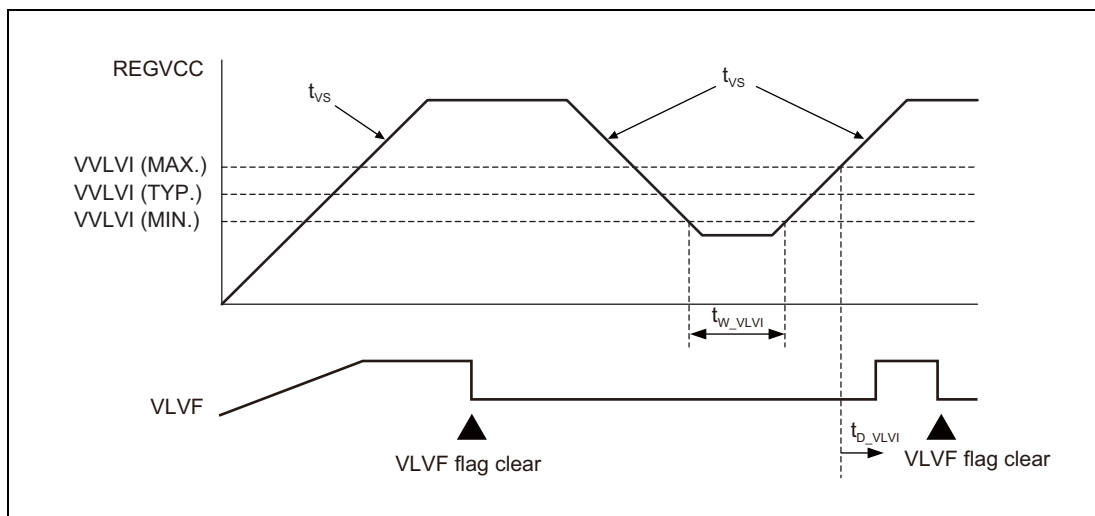
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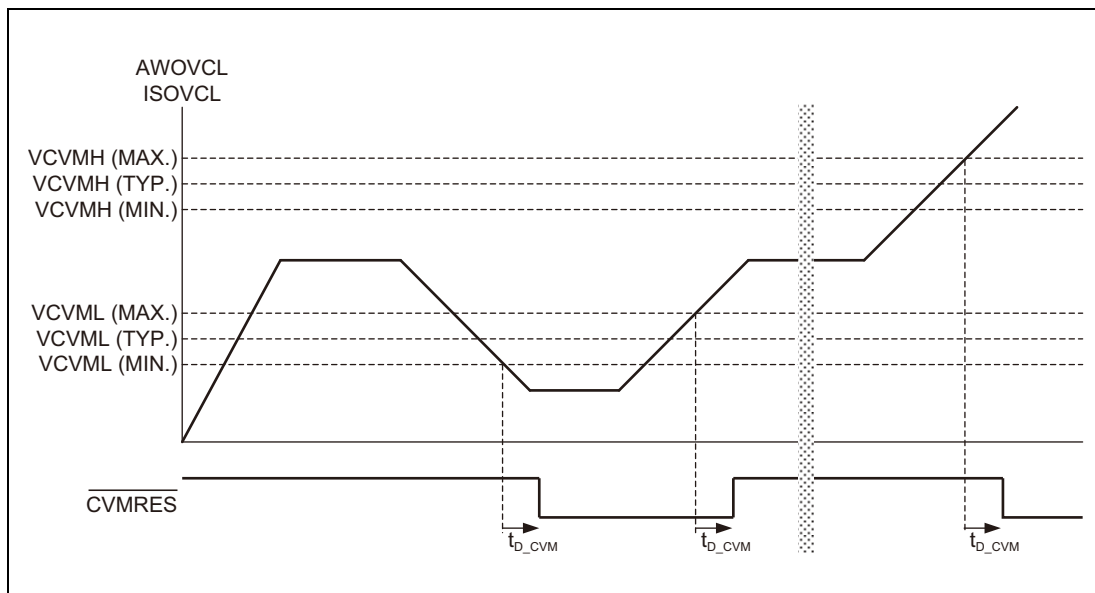
<LVI>



<VLVI>



<CVM>

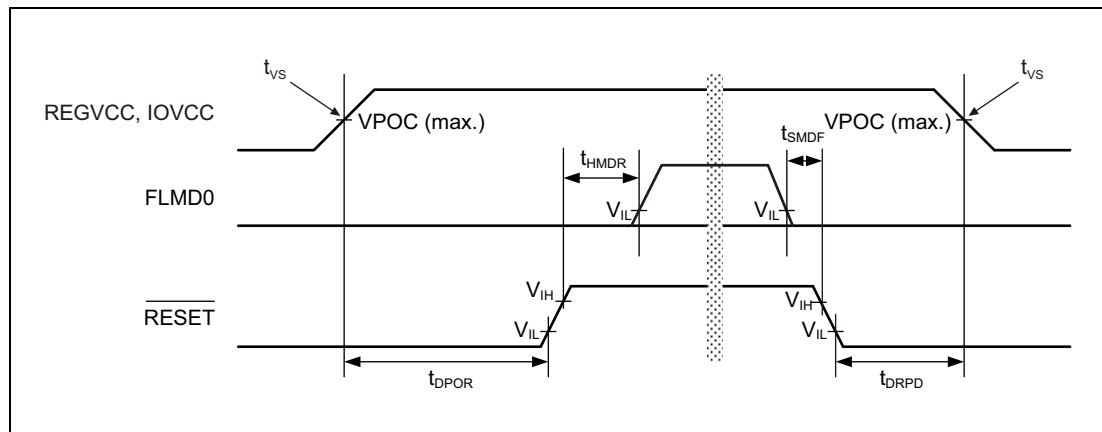


1.8.3 Power Up/Down Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Table 1.4 In case the $\overline{\text{RESET}}$ pin is used (except Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 μ s/V)	V/ms
REGVCC \uparrow and IOVCC*1 \uparrow to $\overline{\text{RESET}}$ \uparrow delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms $\leq t_{VS} \leq$ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms $< t_{VS} \leq$ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ \uparrow)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ \downarrow)	t_{SMDF}		0*2			μ s
$\overline{\text{RESET}}$ \downarrow to REGVCC \downarrow and IOVCC*1 \downarrow delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

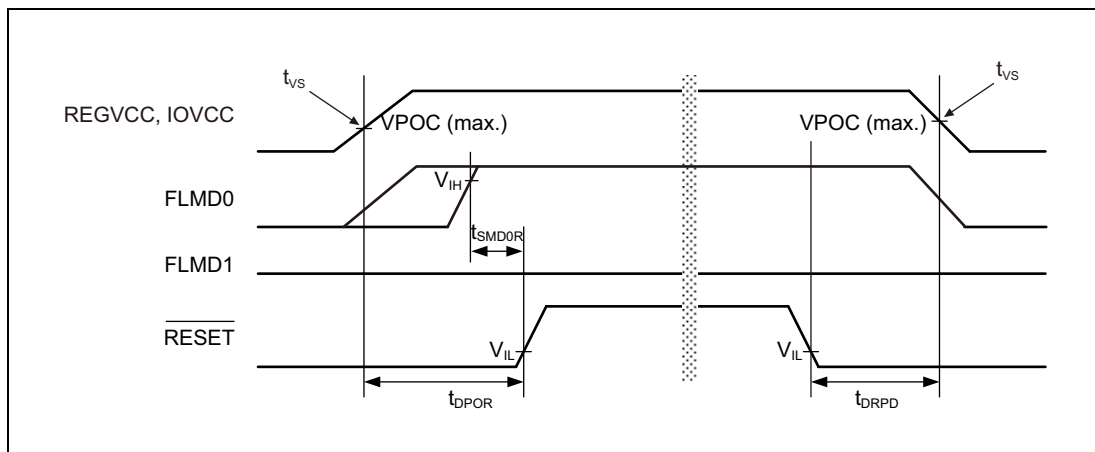
Note 2. When the $\overline{\text{RESET}}$ and FLMD0 pin input low level at same time ($t_{SMDF} = 0\mu$ s) in the device enters on-chip debug mode and operates self-programming, following pins have a possibility to unstable level output for less than 23ns.

JP0_6, P10_0, P0_0, P10_5, P8_1

So, when the device was used in the device entries on-chip debug mode and operates self-programming, please input low level in FLMD0 before $\overline{\text{RESET}}$ pin input.

Table 1.5 In case the $\overline{\text{RESET}}$ pin is used (for Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 $\mu\text{s/V}$)	V/ms
REGVCC \uparrow and IOVCC*1 \uparrow to $\overline{\text{RESET}}$ \uparrow delay time	t_{DPOR}	Voltage slope (t_{VS}): $0.02 \text{ V/ms} \leq t_{VS} \leq 0.5 \text{ V/ms}$	2			ms
		Voltage slope (t_{VS}): $0.5 \text{ V/ms} < t_{VS} \leq 500 \text{ V/ms}$	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ \uparrow)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ \downarrow to REGVCC \downarrow and IOVCC*1 \downarrow delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

Table 1.6 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 $\mu\text{s/V}$)	V/ms
REGVCC \uparrow and IOVCC \uparrow to $\overline{\text{RESET}}$ \uparrow delay time	t_{DPOR}	Voltage slope (t_{VS}): $0.02 \text{ V/ms} \leq t_{VS} \leq 0.5 \text{ V/ms}$	2			ms
		Voltage slope (t_{VS}): $0.5 \text{ V/ms} < t_{VS} \leq 500 \text{ V/ms}$	6.3			ms
FLMD0, FLMD1, MODE0, MODE1 setup time (vs $\overline{\text{RESET}}$ \uparrow)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ \downarrow to REGCC \downarrow and IOVCC \downarrow delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ \uparrow)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ \downarrow)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

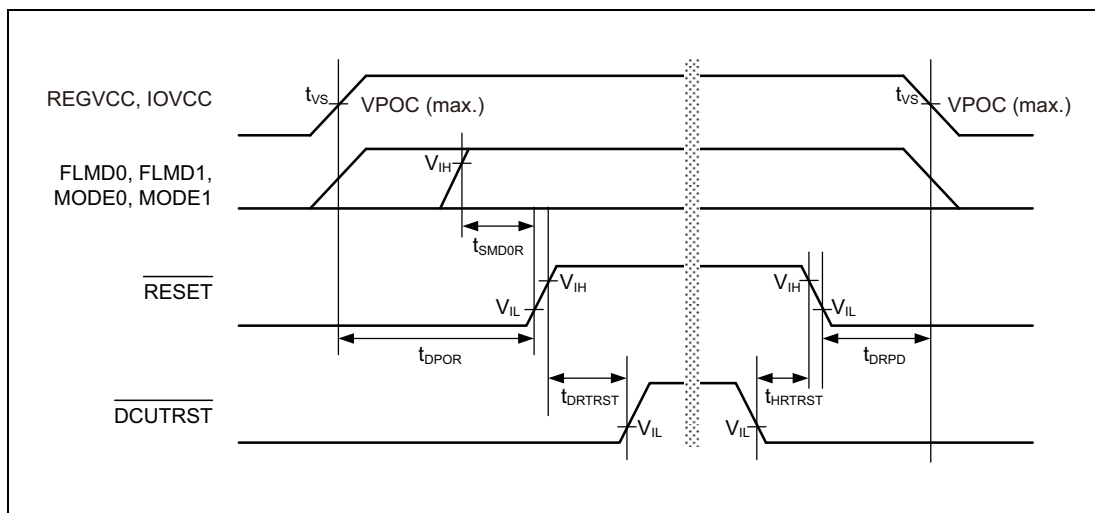
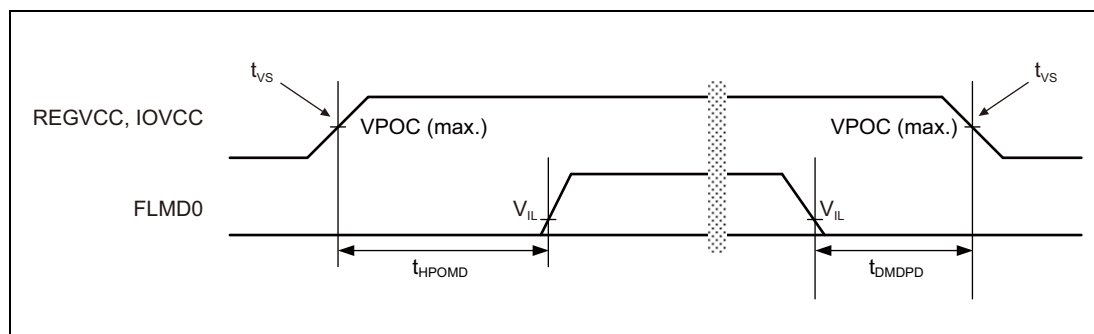


Table 1.7 In case the RESET pin is not used and fixed to high level by pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 μ s/V)	V/ms
REGVCC \uparrow and IOVCC*2 \uparrow to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}): $0.02 \text{ V/ms} \leq t_{VS} \leq 0.5 \text{ V/ms}$	2			ms
		Voltage slope (t_{VS}): $0.5 \text{ V/ms} < t_{VS} \leq 500 \text{ V/ms}$	6.3			ms
FLMD0 \downarrow to REGVCC \downarrow and IOVCC*2 \downarrow delay time	t_{DMDPD}		1			μ s

Note 1. This operating condition is available only in normal operation mode (include self-programming mode).
When the device is used in except single chip mode, please use the RESET pin.

Note 2. IOVCC means EVCC, BVCC, A0VREF and A1VREF.



1.8.4 CPU Reset Release Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1μF +/- 30%, CISOVCL: 0.1μF +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Table 1.8 In case the $\overline{\text{RESET}}$ pin is not used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}): $0.02 \text{ V/ms} \leq t_{\text{VS}} \leq 0.5 \text{ V/ms}$			2.58	ms
		Voltage slope (t_{VS}): $0.5 \text{ V/ms} < t_{\text{VS}} \leq 500 \text{ V/ms}$			8.38	ms

Note 1. This is reference value.

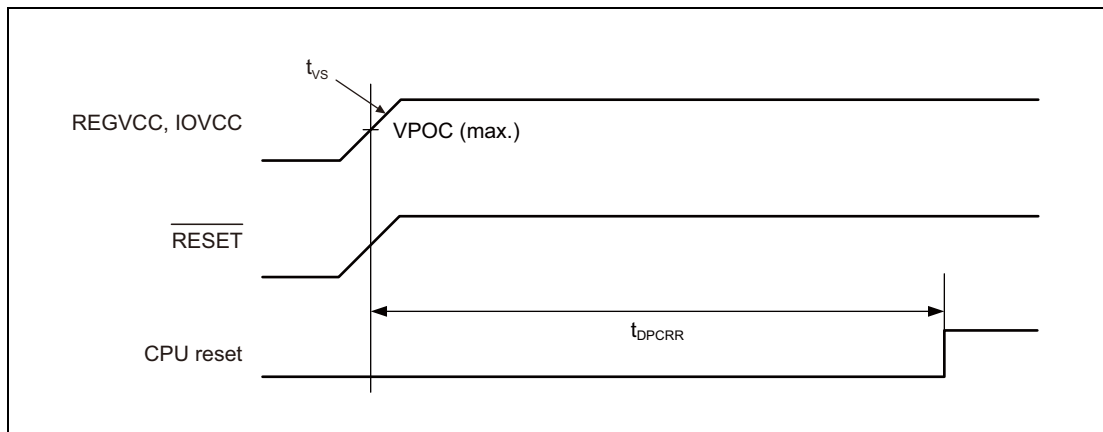
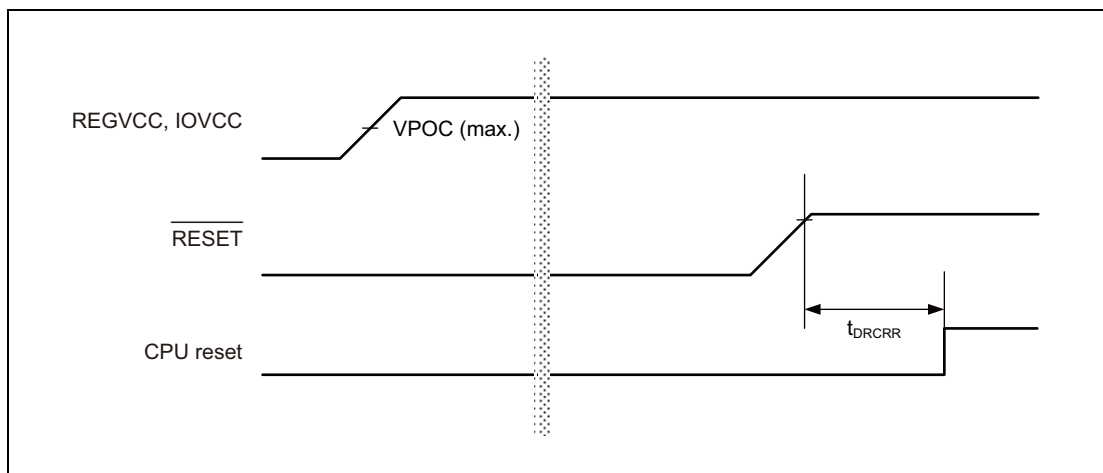


Table 1.9 In case the $\overline{\text{RESET}}$ pin is used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				14×2	μs

Note 1. This is reference value.

Note 2. At least t_{DPCRR} time is necessary reaching from VPOC (max) even if power up sequence is kept shown on **Section 1.8.3, Power Up/Down Timing.**



1.9 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

(1/5)

Pin Name	176 pin	233 pin	272 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
RESET	√	√	√	—	—	√	—	—	—	—	—	— ⁴
FLMD0	√	√	√	—	√	—	—	—	—	—	√	√
P21_0	—	—	√	—	—	—	√	—	—	Slow	√	—
P21_1	—	—	√	—	—	—	√	—	—	Slow	√	—
P21_2	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P21_3	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P21_4	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_0	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_1	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_2	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_3	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_4	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_5	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_6	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_7	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_8	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_9	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_10	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_11	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_12	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_13	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_14	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P22_15	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
IP0_0	√	√	√	—	—	—	—	—	—	—	—	—
JP0_0	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_1	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
JP0_2	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_3	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_4	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_5	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
JP0_6	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P0_0	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_1	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_2	√	√	√	—	√	—	√	—	—	Slow/Fast ²	√	√
P0_3	√	√	√	—	√	—	√	—	—	Slow/Fast ²	√	√
P0_4	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_5	√	√	√	—	√	—	√	—	—	Slow/Fast ³	√	√
P0_6	√	√	√	—	√ ¹	—	√	—	—	Slow/Fast ³	√	√
P0_7	√	√	√	—	√	—	√	—	—	Slow/Fast ⁷	√	√
P0_8	√	√	√	—	—	—	√	—	—	Slow	√	√
P0_9	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_10	√	√	√	—	—	—	√	—	—	Slow	√	√
P0_11	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_12	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_13	√	√	√	—	√	—	√	—	—	Slow/Fast	√	—
P0_14	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—

(2/5)

Pin Name	176 pin	233 pin	272 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P1_0	√	√	√	—	√ ⁶	—	√	—	—	Slow	√	—
P1_1	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_2	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_3	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_4	√	√	√	—	√ ⁶	—	√	—	—	Slow	√	—
P1_5	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_6	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_7	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_8	√	√	√	—	√ ⁶	—	√	—	—	Slow	√	—
P1_9	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_10	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_11	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_12	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_13	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_14	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_15	√	√	√	—	—	—	√	—	—	Slow	√	—
P2_0	√	√	√	—	√	—	√	—	—	Slow	√	—
P2_1	√	√	√	—	—	—	√	—	—	Slow	√	—
P2_2	√	√	√	—	√	—	√	—	—	Slow	√	—
P2_3	√	√	√	—	—	—	√	—	—	Slow	√	—
P2_4	√	√	√	—	√	—	√	—	—	Slow	√	—
P2_5	√	√	√	—	—	—	√	—	—	Slow	√	—
P2_6	√	√	√	—	—	—	√	—	—	Slow	√	—
P2_7	—	√	√	—	√ ⁶	—	√	—	—	Slow	√	—
P2_8	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_9	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_10	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_11	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_12	—	√	√	—	√ ⁶	—	√	—	—	Slow	√	—
P2_13	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_14	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_15	—	√	√	—	—	—	√	—	—	Slow	√	—
P3_0	—	√	√	—	—	—	√	—	—	Slow	√	—
P3_1	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_2	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_3	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_4	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_5	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_6	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_7	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_8	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_9	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_10	—	—	√	—	—	—	√	—	—	Slow	√	—
P8_0	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P8_1	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P8_2	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P8_3	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P8_4	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P8_5	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P8_6	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵

(3/5)

Pin Name	176 pin	233 pin	272 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P8_7	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ¹
P8_8	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ¹
P8_9	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ¹
P8_10	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ¹
P8_11	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ¹
P8_12	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ¹
P20_0	√	√	√	—	√	—	√	—	—	Slow	√	—
P20_1	√	√	√	—	—	—	√	—	—	Slow/Fast ⁷	√	—
P20_2	√	√	√	—	√	—	√	—	—	Slow/Fast ⁷	√	—
P20_3	√	√	√	—	—	—	√	—	—	Slow	√	—
P20_4	√	√	√	—	√	—	√	—	—	Slow	√	—
P20_5	√	√	√	—	—	—	√	—	—	Slow	√	—
P20_6	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_7	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_8	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_9	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_10	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_11	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_12	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_13	—	—	√	—	—	—	√	—	—	Slow	√	—
P20_14	—	—	√	—	—	—	√	—	—	Slow	√	—
P9_0	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P9_1	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P9_2	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P9_3	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P9_4	√	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P10_0	√	√	√	—	√	—	√	√	—	Slow/Fast	√	√
P10_1	√	√	√	—	—	—	√	√	—	Slow/Fast ³	√	√
P10_2	√	√	√	—	√	—	√	√	—	Slow/Fast ³	√	√
P10_3	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_4	√	√	√	—	√	—	√	√	—	Slow/Fast ⁷	√	√
P10_5	√	√	√	—	—	—	√	√	—	Slow/Fast ⁷	√	√
P10_6	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_7	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P10_8	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P10_9	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_10	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_11	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_12	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_13	√	√	√	—	√ ⁶	—	√	—	—	Slow/Fast	√	√
P10_14	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_15	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P11_0	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P11_1	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P11_2	√	√	√	—	—	—	√	—	—	Slow/Fast ³	√	√
P11_3	√	√	√	—	√	—	√	—	—	Slow/Fast ³	√	√
P11_4	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P11_5	√	√	√	—	√	—	√	—	—	Slow/Fast	√	—
P11_6	√	√	√	—	√ ⁶	—	√	—	—	Slow/Fast ³	√	—
P11_7	√	√	√	—	—	—	√	—	—	Slow/Fast ³	√	—

(4/5)

Pin Name	176 pin	233 pin	272 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P11_8	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P11_9	√	√	√	—	√ ⁶	—	√	—	—	Slow/Fast	√	—
P11_10	√	√	√	—	—	—	√	√	—	Slow/Fast	√	—
P11_11	√	√	√	—	—	—	√	√	—	Slow/Fast	√	—
P11_12	√	√	√	—	√	—	√	—	—	Slow	√	—
P11_13	√	√	√	—	√	—	√	√	—	Slow/Fast	√	—
P11_14	√	√	√	—	—	—	√	√	—	Slow/Fast	√	—
P11_15	√	√	√	—	√	—	√	—	—	Slow/Fast	√	—
P12_0	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P12_1	√	√	√	—	√ ⁶	—	√	—	—	Slow/Fast	√	—
P12_2	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P12_3	√	√	√	—	√	—	√	√	—	Slow	√	—
P12_4	√	√	√	—	—	—	√	√	—	Slow/Fast	√	—
P12_5	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P13_0	—	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P13_1	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
	—	√	—	—	—	—	—	—	—	Slow	—	—
P13_2	—	√	√	—	—	—	√	√	—	Slow	√	—
P13_3	—	√	√	—	—	—	√	√	—	Slow	√	—
P13_4	—	√	√	—	—	—	√	—	—	Slow	√	—
P13_5	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
	—	√	—	—	—	—	—	—	—	Slow	—	—
P13_6	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
	—	√	—	—	—	—	—	—	—	Slow	—	—
P13_7	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
	—	√	—	—	—	—	—	—	—	Slow	—	—
P18_0	√	√	√	—	—	—	√	√	ADC	Slow	√	√ ⁵
P18_1	√	√	√	—	—	—	√	—	ADC	Slow/Fast	√	√ ⁵
P18_2	√	√	√	—	—	—	√	—	ADC	Slow/Fast	√	√ ⁵
P18_3	√	√	√	—	—	—	√	—	ADC	Slow/Fast	√	√ ⁵
P18_4	√	√	√	—	—	—	√	—	ADC	Slow/Fast	√	√ ⁵
P18_5	√	√	√	—	—	—	√	—	ADC	Slow/Fast	√	√ ⁵
P18_6	√	√	√	—	—	—	√	—	ADC	Slow/Fast	√	√ ⁵
P18_7	√	√	√	—	—	—	√	√	ADC	Slow	√	√ ⁵
P18_8	—	√	√	—	—	—	√	√	ADC	Slow	√	√ ⁵
P18_9	—	√	√	—	—	—	√	√	ADC	Slow	√	√ ⁵
P18_10	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P18_11	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P18_12	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P18_13	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P18_14	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P18_15	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P19_0	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P19_1	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P19_2	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
P19_3	—	√	√	—	—	—	√	—	ADC	Slow	√	√ ⁵
AP0_0	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ¹
AP0_1	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ¹
AP0_2	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ¹
AP0_3	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ¹

(5/5)

Pin Name	176 pin	233 pin	272 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
AP0_4	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_5	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_6	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_7	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_8	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_9	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_10	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_11	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_12	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_13	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_14	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP0_15	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_0	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_1	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_2	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_3	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_4	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_5	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_6	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_7	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_8	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_9	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_10	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_11	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_12	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_13	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_14	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}
AP1_15	√	√	√	√	—	—	—	—	ADC	Slow	—	√ ^{†1}

- Note 1. Pull-down resistor for ADC diagnostic purpose. Control via ADC self-diagnostic register.
- Note 2. Supports Cload: 100 pF, it can be set for CSIH0SO and CSIH0SC with fast mode
- Note 3. Supports Cload: 50 pF, it can be set for CSIHnSO and CSIHnSC with fast mode. (n = 1 to 3)
- Note 4. At a power-on clear reset, an on-chip pull-down resistor at the RESET pin is enabled until the flash sequence is completed.
- Note 5. Pull-down resistors for ADC diagnostic and internal pull-down purposes. For ADC diagnostic, control via ADC self-diagnostic register. For internal pull-down, control via PD register.
- Note 6. Available in devices other than the RH850/F1H for Gateway product.
- Note 7. Fast mode is available in devices other than the RH850/F1H for Gateway product.

Caution: Regarding external pull-up resistor of RESET pin, please connect less than 6.6 kΩ.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
High level input voltage	VIH	CMOS	0.65 × IOVCC		IOVCC + 0.3	V	
		SHMT1 (except FLMD0 pin)	0.7 × IOVCC		IOVCC + 0.3	V	
		SHMT1 (FLMD0 pin) ^{*3}	0.66 × EVCC		EVCC + 0.3	V	
		SHMT2	0.75 × IOVCC		IOVCC + 0.3	V	
		SHMT4	0.8 × IOVCC		IOVCC + 0.3	V	
		TTL	IOVCC = VPOC to 3.6 V	2.0		IOVCC + 0.3	V
			IOVCC = 3.6 V to 5.5 V	2.2		IOVCC + 0.3	V
Low level input voltage	VIL	IP0_0 pin	0.7 × REGVCC		REGVCC	V	
		CMOS	-0.3		0.35 × IOVCC	V	
		SHMT1	-0.3		0.3 × IOVCC	V	
		SHMT2	-0.3		0.25 × IOVCC	V	
		SHMT4	-0.3		0.5 × IOVCC	V	
		TTL	-0.3		0.8	V	
		IP0_0 pin	0		0.3 × REGVCC	V	
Input hysteresis for Schmitt	VH	SHMT1	0.3			V	
		SHMT2	0.2 × IOVCC			V	
		SHMT4	0.1			V	
Input leakage current	ILIH	IP0_0 pin, VI = REGVCC			0.5	μ A	
		RESET, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 pin, VI = EVCC ^{*2}			0.5	μ A	
		P10, P11, P12, P13, P18, P19, P21 pin, VI = BVCC			0.5	μ A	
		AP0 pin, VI = A0VREF ^{*2}			0.5	μ A	
		AP1 pin, VI = A1VREF ^{*2}			0.5	μ A	
	ILIL	IP0_0 pin, VI = 0 V			-0.5	μ A	
		RESET, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 pin, VI = 0 V ^{*2}			-0.5	μ A	
		P10, P11, P12, P13, P18, P19, P21 pin, VI = 0 V ^{*2}			-0.5	μ A	
		AP0 pin, VI = 0 V ^{*2}			-0.5	μ A	
		AP1 pin, VI = 0 V ^{*2}			-0.5	μ A	
Internal pull-up resistance	RU	except FLMD0 pin	20	40	100	k Ω	
		FLMD0 ^{*3}	4	12	36	k Ω	
Internal pull-down resistance	RD	except FLMD0 pin	20	40	100	k Ω	
		FLMD0	4	12	36	k Ω	
High level output voltage	VOH	Fast mode	IOH = -5 mA (6 pins) ^{*4}	IOVCC - 1.0		V	
			IOH = -3 mA (10 pins) ^{*4}	IOVCC - 1.0		V	
			IOH = -1 mA (16 pins) ^{*4}	IOVCC - 0.5		V	
			IOH = -0.1 mA (16 pins) ^{*4}	IOVCC - 0.5		V	
		Slow mode	IOH = -1 mA (16 pins) ^{*4}	IOVCC - 0.5		V	
			IOH = -0.1 mA (16 pins) ^{*4}	IOVCC - 0.5		V	
Low level output voltage	VOL	Fast mode	IOL = 5 mA (6 pins) ^{*4}		0.4	V	
			IOL = 3 mA (10 pins) ^{*4}		0.4	V	
			IOL = 1 mA (16 pins) ^{*4}		0.4	V	
		Slow mode	IOL = 1 mA (16 pins) ^{*4}		0.4	V	

(2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)* ⁵	CL = 30 pF		7	ns
			CL = 50 pF		12	ns
			CL = 100 pF		24	ns
		Fast mode (P18_1 to P18_6)* ⁶	CL = 15 pF		2.1	ns
			CL = 50 pF		6	ns
		Fast mode (P0_5, P0_6, P10_1, P10_2, P11_2, P11_3, P11_6, P11_7)* ⁶	CL = 50 pF		6	ns
			CL = 100 pF		6.15	ns
		Slow mode* ⁵	CL = 30 pF		37	ns
			CL = 50 pF		62	ns
CL = 100 pF			124	ns		
Output frequency	f_O	Fast mode	CL = 30 pF		40	MHz
			CL = 50 pF		10	MHz
		Slow mode	CL = 30 pF		10	MHz
			CL = 50 pF		6	MHz
			CL = 100 pF		3	MHz

Note 1. "IOVCC" means the pins are assigned to the power supply (EVCC, BVCC, A0VREF and A1VREF).

Note 2. Not select the analog input function of ADCn.

Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 86 kΩ or more as external pull-down resistor.

Note 4. The number of pin indicates simultaneous ON.

Note 5. Measurement point: $0.1 \times IOVCC$ to $0.9 \times IOVCC$

Note 6. Measurement point: $0.2 \times IOVCC$ to $0.8 \times IOVCC$

1.9.1 Output Current

1.9.1.1 272 pin

Table 1.10 Output Current (272 pin) (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
High level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_10 to P20_14		-11	mA
				P20_0 to P20_9		-18	mA
				P0_0 to P0_3		-12	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12		-30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15 P3_0		-14	mA
				JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P3_1 to P3_2, P8_0 to P8_1, P8_3 to P8_7		-28	mA
				P3_3 to P3_10, P8_8 to P8_9		-10	mA
				Total (EVCC)		-60	mA
PgB	Per side	PgB	Per side	P18_0 to P18_7		-30	mA
				P18_8 to P18_15, P19_0 to P19_3		-12	mA
				P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1		-30	mA
				P10_0 to P10_2		-15	mA
				P10_3 to P10_5		-15	mA
				P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7		-30	mA
				P21_0, P21_2 to P21_4 P22_0 to P22_2		-7	mA
				P22_3 to P22_8		-6	mA
				P21_1, P22_9 to P22_15		-8	mA
				Total (BVCC)		-60	mA
PgA0	Total (A0VREF)		-16	mA			
PgA1	Total (A1VREF)		-16	mA			

Table 1.10 Output Current (272 pin) (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit					
Low level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_10 to P20_14		11	mA				
				P20_0 to P20_9		18	mA				
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12		30	mA				
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15 P3_0, P8_2, P8_10 to P8_12		20	mA				
				JP0_6, P0_7 to P0_10, P2_2 to P2_3		11	mA				
				P1_4 to P1_7, P2_4 to P2_5		6	mA				
				P1_14 to P1_15, P3_1 to P3_2, P8_0 to P8_1, P8_3 to P8_7		10	mA				
				P3_3 to P3_10, P8_8 to P8_9		10	mA				
				Total (EVCC)						60	mA
						PgB	Per side	P18_0 to P18_7		30	mA
P18_8 to P18_15, P19_0 to P19_3		12	mA								
P10_6 to P10_14, P11_1 to P11_2		30	mA								
P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1		30	mA								
P10_0 to P10_2		15	mA								
P10_3 to P10_5		15	mA								
P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7		30	mA								
P21_0, P21_2 to P21_4 P22_0 to P22_6		-11	mA								
P21_1, P22_7 to P22_15		-10	mA								
Total (BVCC)									60	mA	
Pg A0	Total (A0VREF)					16	mA				
Pg A1	Total (A1VREF)					16	mA				

Note 1. For detail of the definition of "side" and "total", refer to **Section 1.2.3, Port Current**.

1.9.1.2 233 pin

Table 1.11 Output Current (233 pin) (1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit			
High level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5		-11	mA			
				P0_0 to P0_3		-12	mA			
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12		-30	mA			
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15 P3_0		-14	mA			
				JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9		-28	mA			
				Total (EVCC)		-60	mA			
				PgB	Per side		P18_0 to P18_7		-30	mA
							P18_8 to P18_15, P19_0 to P19_3		-12	mA
							P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1		-30	mA
							P10_0 to P10_2		-15	mA
P10_3 to P10_5		-15	mA							
P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7		-30	mA							
Total (BVCC)		-60	mA							
PgA0	Total (A0VREF)		-16	mA						
PgA1	Total (A1VREF)		-16	mA						
Low level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5		11	mA			
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12		30	mA			
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15 P3_0, P8_2, P8_10 to P8_12		20	mA			
				JP0_6, P0_7 to P0_10, P2_2 to P2_3		11	mA			

Table 1.11 Output Current (233 pin) (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit							
Low level output current	IOL	PgE	Per side	P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9		17	mA						
					Total (EVCC)				60	mA			
					Pg B	Per side	P18_0 to P18_7		30	mA			
							P18_8 to P18_15, P19_0 to P19_3		12	mA			
							P10_6 to P10_14, P11_1 to P11_2		30	mA			
							P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1		32	mA			
							P10_0 to P10_2		15	mA			
							P10_3 to P10_5		15	mA			
							P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7		30	mA			
							Total (BVCC)				60	mA	
							Pg A0	Total (A0VREF)				16	mA
							Pg A1	Total (A1VREF)				16	mA

Note 1. For detail of the definition of "side" and "total", refer to **Section 1.2.3, Port Current**.

1.9.1.3 176 pin

Table 1.12 Output Current (176 pin) (1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit			
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5		-11	mA			
				P0_0 to P0_3		-12	mA			
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6, P8_2, P8_10 to P8_12		-30	mA			
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1		-9	mA			
				JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9		-28	mA			
			Total (EVCC)					-60	mA	
			PgB	Per side		P10_6 to P10_9, P18_0 to P18_7			-28	mA
						P10_10 to P10_14, P11_1 to P11_7, P11_5, P12_0 to P12_2			-30	mA
						P10_0 to P10_2			-15	mA
						P10_3 to P10_5			-15	mA
P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5						-30	mA			
Total (BVCC)					-60	mA				
PgA0	Total (A0VREF)				-16	mA				
PgA1	Total (A1VREF)				-16	mA				
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5		11	mA			
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6		30	mA			
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P8_2, P8_10 to P8_12		16	mA			
				JP0_6, P0_7 to P0_10, P2_2 to P2_3		11	mA			
				P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9		17	mA			
				Total (EVSS)					60	mA

Table 1.12 Output Current (176 pin) (2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PGB	Per side	P18_0 to P18_7		8	mA
				P10_6 to P10_14, P11_1 to P11_2		30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2		30	mA
				P10_0 to P10_2		15	mA
				P10_3 to P10_5		15	mA
				P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5		30	mA
				Total (BVSS)		60	mA
				PgA0	Total (A0VSS)		16
PgA1	Total (A1VSS)		16	mA			

Note 1. For detail of the definition of "side" and "total", refer to **Section 1.2.3, Port Current**.

1.10 Power Supply Currents

Condition: REGVCC, EVCC, BVCC, A0VREF and A1VREF total current. But, the I/O buffer is stopped.

Item	Symbol	Condition				MIN.	TYP.* ¹	MAX.	Unit	
		CPU1/CPU2	PLL	Ta	Peripheral					
RUN mode current	IDDR1	RUN (120 MHz)	RUN	-40 to 125°C	Run(#1)	82	144	mA		
				25°C	Stop(#1)				70	mA
RUN mode current (During data/code flash programming)	IDDR3	RUN (120 MHz)	RUN	-40 to 125°C	Run(#2)	94	161	mA		
HALT mode current	IDDH	RUN	RUN	-40 to 125°C	Run(#3)	47	115	mA		
STOP mode current	IDDS	Stop	Stop	-40 to 85°C	Stop(#2)	0.75	15	mA		
				105°C	Stop(#2)				25	mA
				125°C	Stop(#2)				42	mA
DeepSTOP mode current	IDDDS	Power off	Power off	-40 to 85°C	Stop(#3)	50	540	μA		
				105°C	Stop(#3)				950	μA
				125°C	Stop(#3)				1600	μA
Cyclic RUN mode current	IDDCR	RUN (HS IntOSC)	Stop	-40 to 85°C	Run(#4)	4	25	mA		
				105°C	Run(#4)				40	mA
				125°C	Run(#4)				72	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	-40 to 85°C	Run(#5)	2	22	mA		
				105°C	Run(#5)				38	mA
				125°C	Run(#5)				70	mA

Note 1. The condition of "TYP." shows the specification with the following conditions. Also, the value is just for reference only. RUN mode current of TYP condition shows the value when ICUMB is stop.

- Ta = 25°C
- REGVCC = EVCC = BVCC = A0VREF = A1VREF = 5.0 V
- AWOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Caution: It must be ensured that the junction temperature in the Ta range remains below $T_j \leq 150^\circ\text{C}$ and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

(1/2)

Power Domain	Function	Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Stop	Stop
	SubOSC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Stop	Stop
	FOUT	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read / Write	Read / Write	No access	Fetch	No access	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	RTCA0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Stop	Stop	Stop
	ADCA0	Run* ¹	Run* ¹	Run* ¹	Stop	Stop	Stop	Stop	Stop

(2/2)

Power Domain	Function	Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
ISO	CPU1 (PE1)	Run (PLL)	Run (PLL)	Halt (PLL)	Run (HS IntOSC)	Stop	Run (PLL)	Stop	Power off
	CPU2 (PE2)	Run (PLL)	Run (PLL)	Halt (PLL)	Stop	Stop	Run (PLL)	Stop	
	ICUMB	Run	Run	Stop	Stop	Stop	Stop	Stop	
	DMA	Run	Run	Run	Stop	Stop	Stop	Stop	
	PLL0	Run	Run	Run	Stop	Stop	Run	Stop	
	PLL1	Run	Run	Run	Stop	Stop	Run	Stop	
	Code Flash (FLI0)	Fetch	No access	No access	No access	No access	Fetch	No access	
	Code Flash (FLI1)	Stop	No access	No access	No access	No access	Fetch	No access	
	Code Flash (FLI2)	Fetch	No access	No access	No access	No access	Fetch	No access	
	Data Flash	Read	Write / Erase	No access	No access	No access	Read	No access	
	LRAM (PE1)	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	LRAM (PE2)	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	GRAM	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	OSTMn	Run	Run	Run	Stop	Stop	Stop	Stop	
	WDTAn	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUBn	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUJ1	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAPA, PIC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	ENCA0	Run	Run	Run	Stop	Stop	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN3n	Run (115.2kbps)	Run (115.2kbps)	Run (115.2kbps)	Stop	Stop	Stop	Stop	
	RLIN2n	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	RS-CANn	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CSIGn	Run	Run	Run	Stop	Stop	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Stop	Stop	
	RIIC0	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
Flexray	Run	Run	Run	Stop	Stop	Stop	Stop		
EternetAVB	Wait	Wait	Wait	Stop	Stop	Stop	Stop		
KR	Wait	Wait	Wait	Stop	Stop	Stop	Stop		
CLMA2	Run	Run	Run	Stop	Stop	Stop	Stop		
ADCA1	Run	Run	Run	Stop	Stop	Stop	Stop		

Note 1. T&H used.

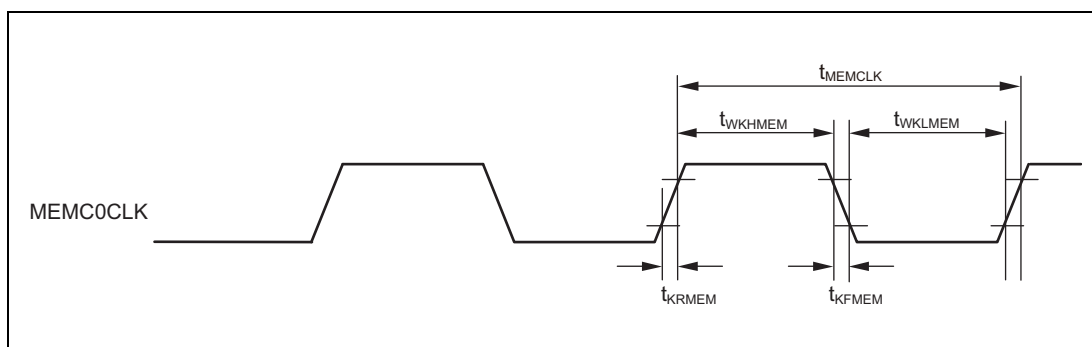
1.11 MEMC0CLK Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μF +/- 30%, CISOVCL: 0.1 μF +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0CLK pin: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MEMC0CLK output cycle	t_{MEMCLK}		33.4 (max.30 MHz)			ns
MEMC0CLK high / low level width	t_{WKHMEM} / t_{WKLMEM}		$t_{MEMCLK} / 2 - 10$			ns
MEMC0CLK rise / fall time	t_{KRMEM} / t_{KFMEM}				10	ns



1.12 External Bus Timing

1.12.1 MEMC0CLK Asynchronous

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V,
A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C,
CL = 30 pF

<Output driver strength>

MEMC0AD0-15, MEMC0A16-19, MEMC0CS3-0, MEMC0BEN1-0, MEMC0ASTB, MEMC0WR, MEMC0RD pin:
Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max.30 MHz)			ns
Address ^{*6} setup time to MEMC0ASTB ↓	t _{SAST}	<1>	(1 + ASW) × T - 15			ns
Address (MEMC0AD15-0) hold time from MEMC0ASTB ↓	t _{HSTA}	<2>	(1 + AHW) × T - 15			ns
Address (MEMC0AD15-0) float delay time from MEMC0RD ↓	t _{FRDA}	<3>		9		ns
Address ^{*7} hold time from MEMC0RD ↑	t _{HRDA}	<4>	-1.5			ns
Data (MEMC0AD15-0) input delay time from MEMC0RD ↓	t _{DRDID}	<5>	9		(1 + w) × T - 35	ns
Data (MEMC0AD15-0) input hold time from MEMC0RD ↑	t _{HRDID}	<6>	0			ns
Delay time from MEMC0ASTB ↓ to MEMC0RD ↓	t _{DSTRD}	<7>	(1 + AHW) × T - 15			ns
Delay time from MEMC0ASTB ↓ to MEMC0WR ↓	t _{DSTWR}	<8>	(1 + AHW) × T - 15			ns
MEMC0RD, MEMC0WR low level width	t _{WRDST}	<9>	(1 + w) × T - 10			ns
Data (MEMC0AD15-0) output delay time from MEMC0WR ↓	t _{DWROD}	<10>		11		ns
Address ^{*7} hold time from MEMC0WR ↑	t _{HWRA}	<11>	(1 + DHW) × T - 15			ns
Data (MEMC0AD15-0) output setup time to MEMC0WR ↑	t _{SODWR}	<12>	(1 + w) × T - 15			ns
Data (MEMC0AD15-0) output hold time from MEMC0WR ↑	t _{HWROD}	<13>	(1 + DHW) × T - 15			ns
MEMC0WAIT setting delay from MEMC0ASTB ↓	t _{SSTWT1}	<14>			(2 + AHW) × T - (4 × t _{CPUCLK} + 35)	ns
	t _{SSTWT2}	<15> w ≥ 1			(2 + w + AHW) × T - (4 × t _{CPUCLK} + 35)	ns
MEMC0WAIT hold time from MEMC0ASTB ↓	t _{HSTWT1}	<16> w ≥ 1	(1 + w + AHW) × T - (4 × t _{CPUCLK} + 20)			ns
	t _{HSTWT2}	<17> w ≥ 1	(2 + w + AHW) × T - (4 × t _{CPUCLK} + 20)			ns

Note 1. ASW means the number of address setup wait for multiplex bus.

Note 2. AHW means the number of address hold wait for multiplex bus.

Note 3. "w" means the number of data wait.

Note 4. t_{CPUCLK}: CPU clock period.

Note 5. DHW means the number of data hold wait for multiplex bus.

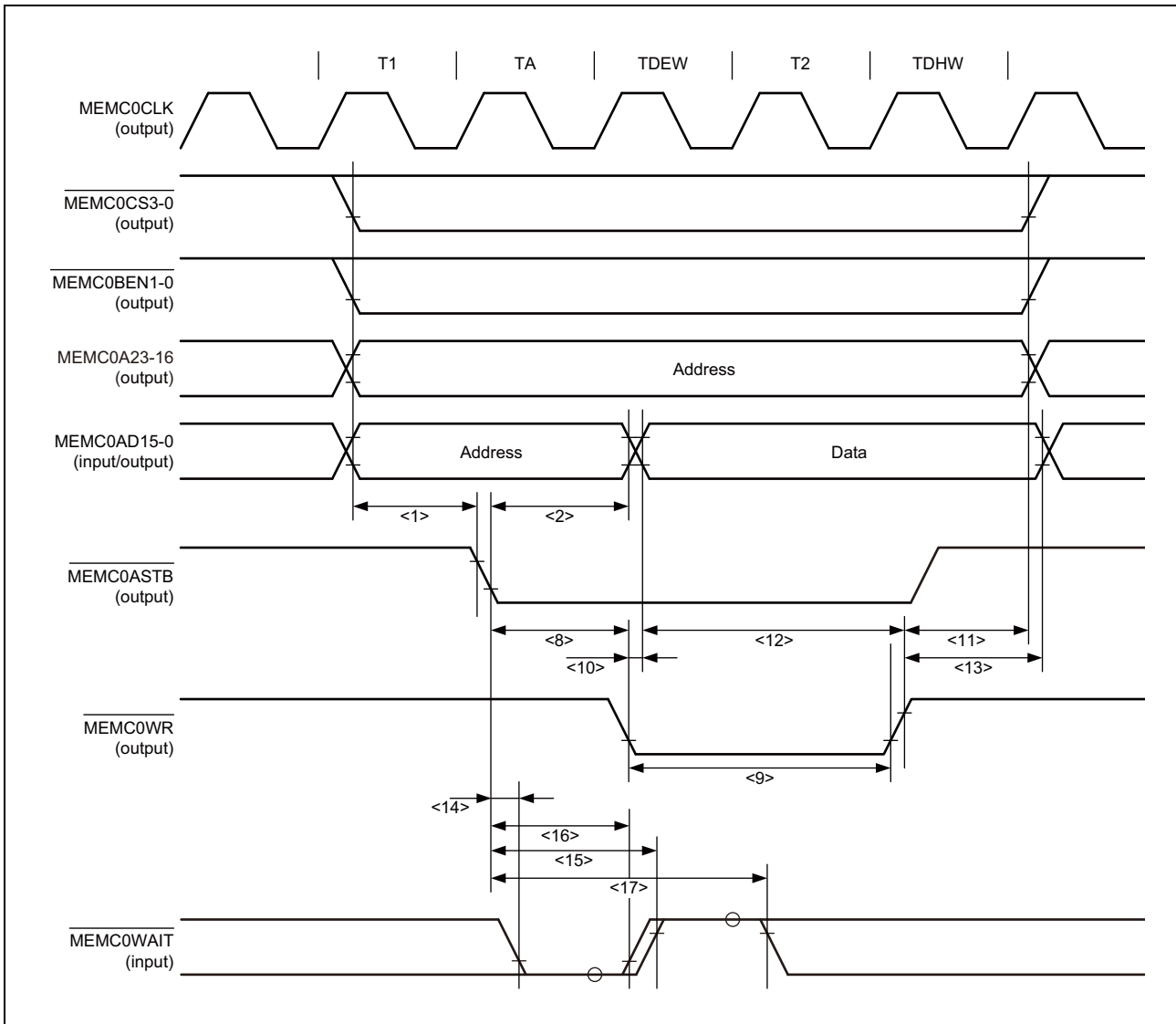
Note 6. Address means MEMC0AD15-0, MEMC0A23-16, MEMC0CS3-0 and MEMC0BEN1-0.
272 pin product supports 24 bit address. 233 pin and 176 pin products support 20 bit address.

Note 7. Address means MEMC0A23-16, MEMC0CS3-0, MEMC0BEN1-0 and MEMC0ASTB.
272 pin product supports 24-bit address. 233 pin and 176 pin products support 20 bit address.

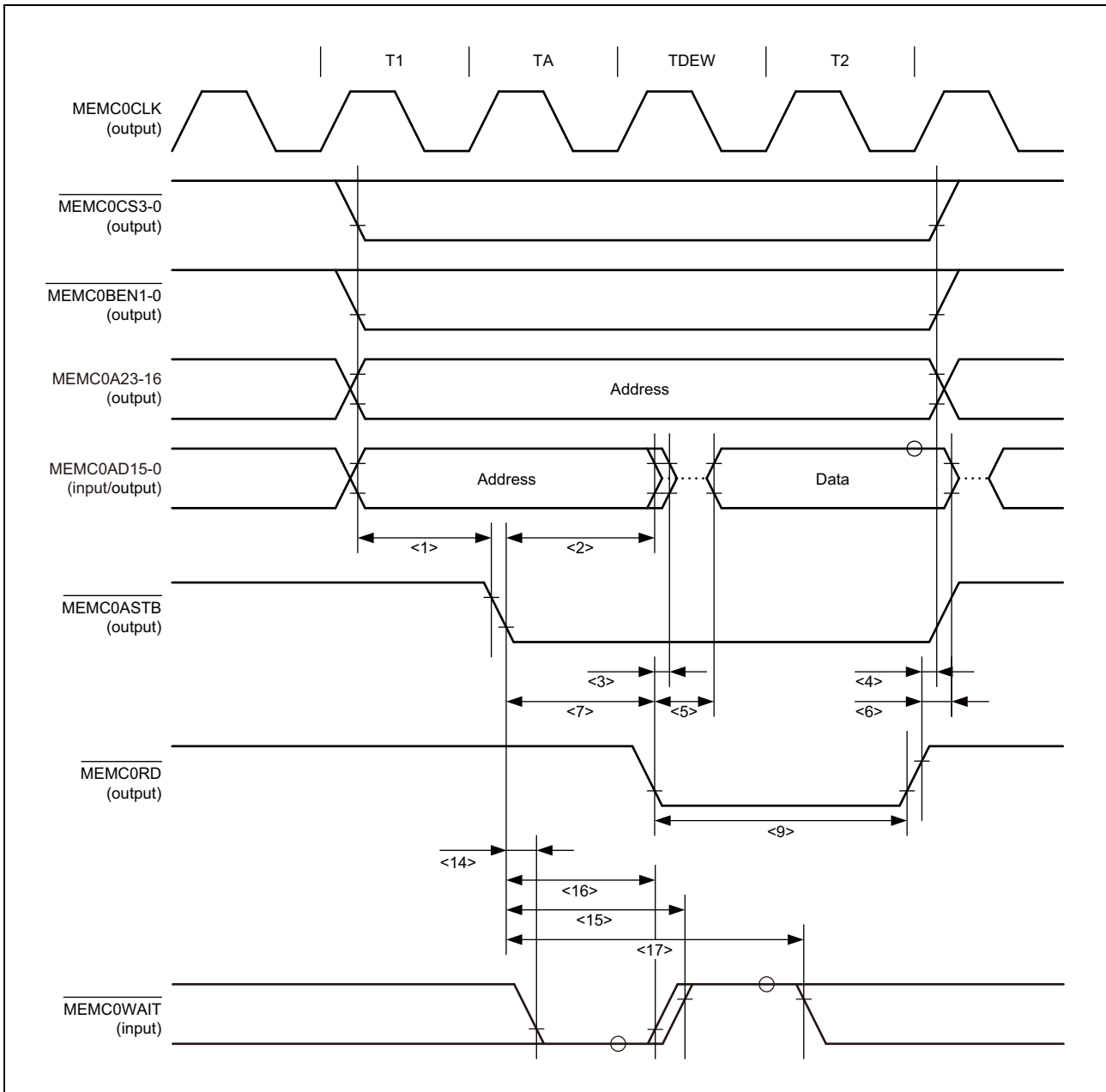
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1 data wait. (w = 1)

(1) Multiplex Write Cycle (Asynchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Asynchronous; 1 Data Wait)



1.12.2 MEMC0CLK Synchronous

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V,
A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C,
CL = 30 pF

<Output driver strength>

MEMC0CLK, MEMC0AD0-15, MEMC0A16-19, MEMC0CS3-0, MEMC0BEN1-0, MEMC0ASTB, MEMC0WR,
MEMC0RD pin: Fast mode

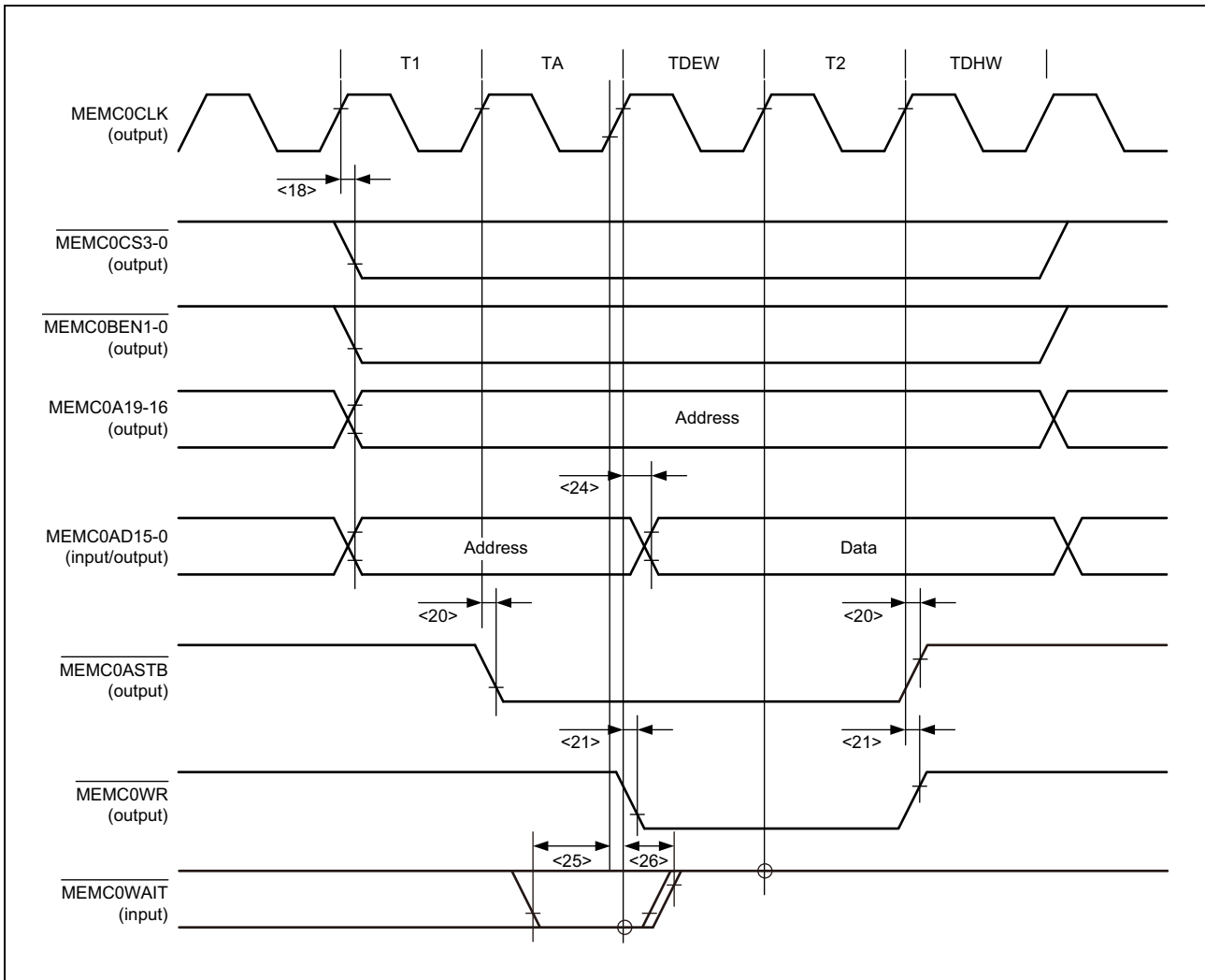
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max.30MHz)			ns
Delay time from MEMC0CLK \uparrow to address*1	t_{DKA}	<18>	-0.5		15	ns
Delay time from MEMC0CLK \uparrow to address (MEMC0AD15-0) float	t_{FKA}	<19>	0		12	ns
Delay time from MEMC0CLK \uparrow to $\overline{\text{MEMC0ASTB}}$	t_{DKST}	<20>	0		11	ns
Delay time from MEMC0CLK \uparrow to $\overline{\text{MEMC0RD}}$ and $\overline{\text{MEMC0WR}}$	t_{DKRDWR}	<21>	-2.5		6	ns
Data (MEMC0AD15-0) input setup time (from MEMC0CLK \uparrow)	t_{SIDK}	<22>	10			ns
Data (MEMC0AD15-0) input hold time (from MEMC0CLK \uparrow)	t_{HKID}	<23>	2.5			ns
Data (MEMC0AD15-0) output delay time (from MEMC0CLK \uparrow)	t_{DKOD}	<24>			15	ns
$\overline{\text{MEMC0WAIT}}$ setup time (to MEMC0CLK \uparrow)	t_{SWTK}	<25>	22 + 4 \times t_{CPUCLK}			ns
$\overline{\text{MEMC0WAIT}}$ hold time (from MEMC0CLK \uparrow)	t_{HKWT}	<26>	-5 - 4 \times t_{CPUCLK}			ns

Note 1. Address means MEMC0AD15-0, MEMC0A23-16, MEMC0CS3-0 and MEMC0BEN1-0.
272 pin product supports 24 bit address. 233 pin and 176 pin products support 20 bit address.

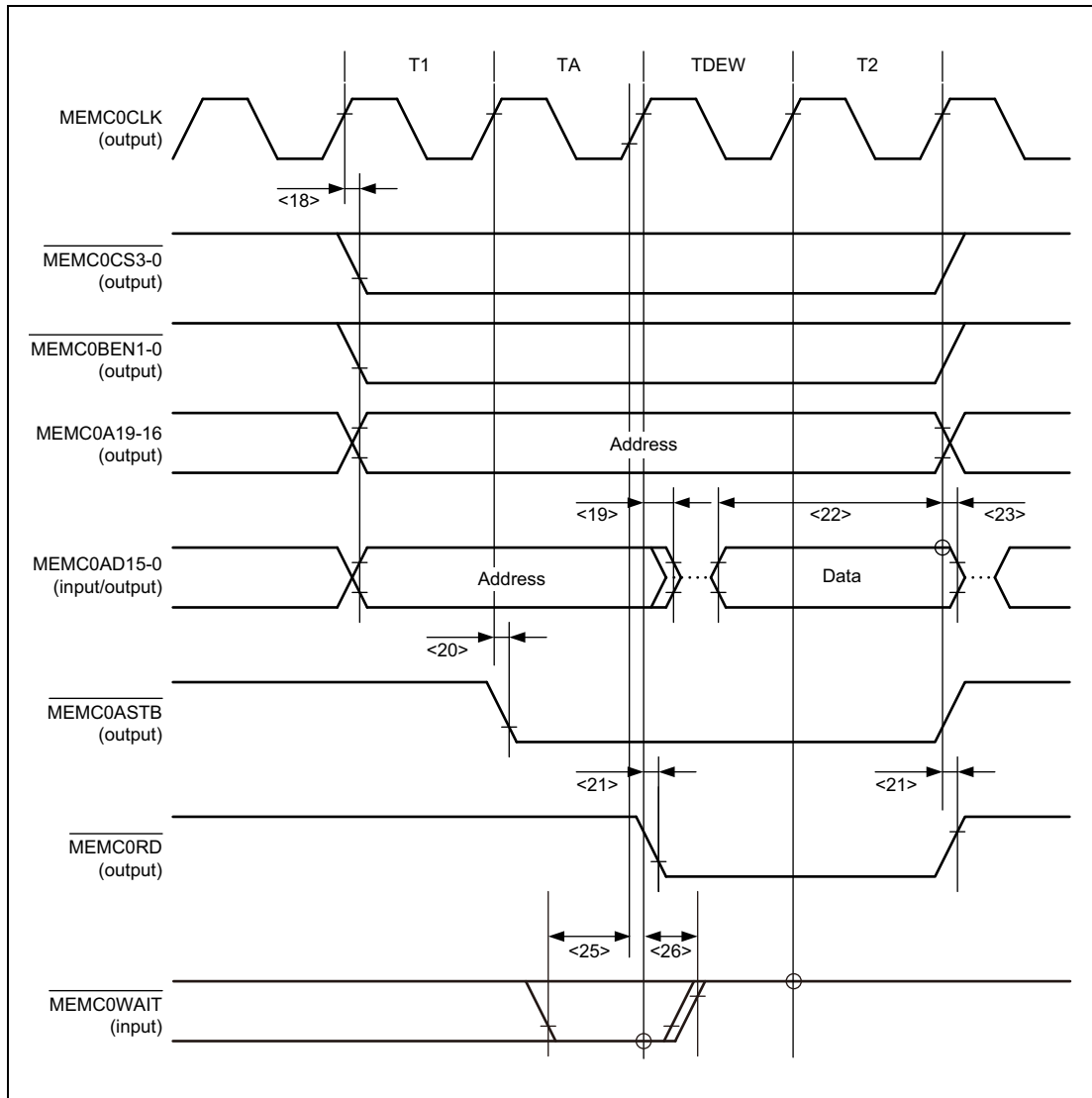
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1 data wait. (w = 1)

(1) Multiplex Write Cycle (Synchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Synchronous; 1 Data Wait)

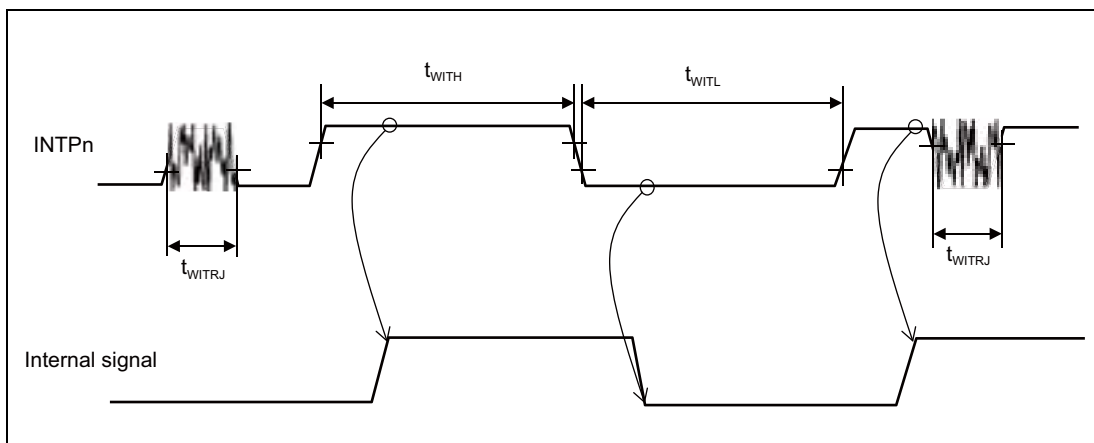
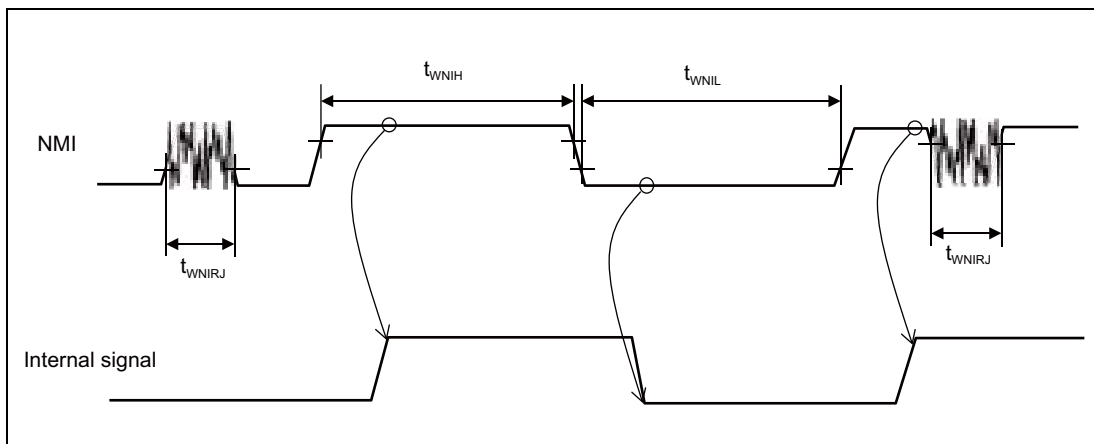


1.13 Interrupt Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μF +/- 30%, CISOVCL: 0.1 μF +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high / low level width*1	t_{WNIH} / t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			μs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high / low level width*1	t_{WITh} / t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			μs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

- Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.
- Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



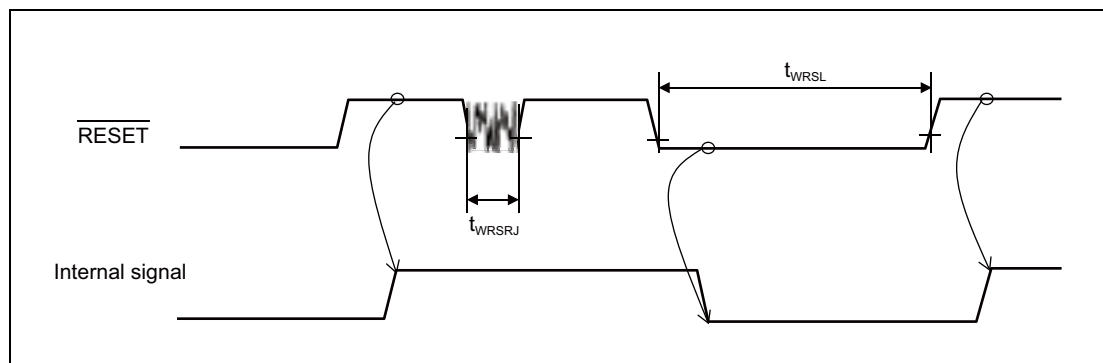
1.14 $\overline{\text{RESET}}$ Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μF +/- 30%, CISOVCL: 0.1 μF +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	*3	0.6			μs
		*4	5.0			μs
		*5	600			μs
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		0.1			μs

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



Note 3. After $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600 μs will become Hi-z. (figure (a))

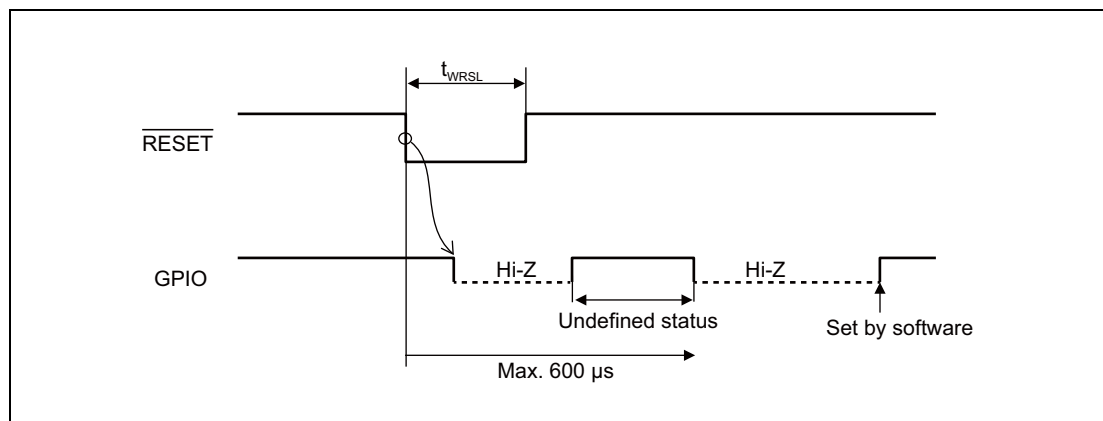
Note 4. If during RUN mode or HALT mode, after $\overline{\text{RESET}}$ is asserted GPIO pin will become Hi-z. For other modes, after $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600 μs will become Hi-z. (figure (a) and (b))

Note 5. GPIO output states will become Hi-z after $\overline{\text{RESET}}$ is asserted. (figure (b))

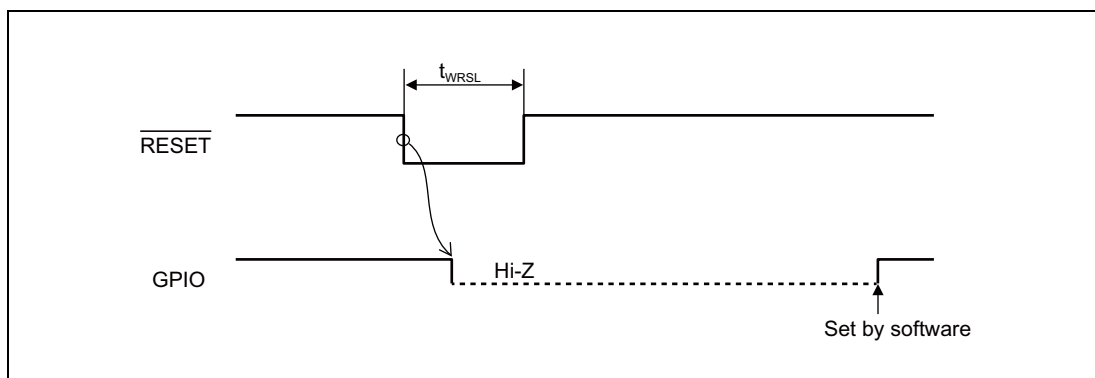
(a) In case of either

$t_{\text{WRSL}} < 5 \mu\text{s}$, any mode or

$t_{\text{WRSL}} < 600 \mu\text{s}$, any mode except for RUN and HALT mode.



- (b) In case of either
 - $5 \mu\text{s} \leq t_{\text{WRSL}}$, RUN and HALT mode or
 - $600 \mu\text{s} \leq t_{\text{WRSL}}$, any mode.

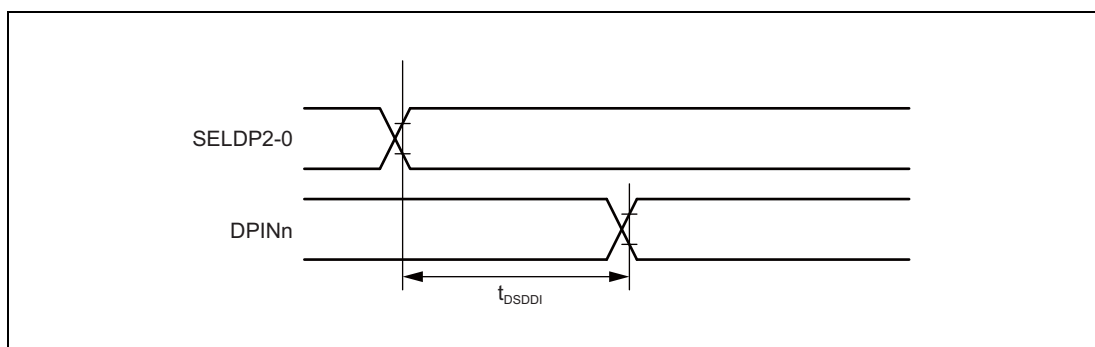


1.15 Low Power Sampler (DPIN Input) Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μF +/- 30%, CISOVCL: 0.1 μF +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note 1. n = 7 to 0



1.16 CSCXFOUT Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

CSCXFOUT: Slow or fast mode (refer to the condition in the following table)

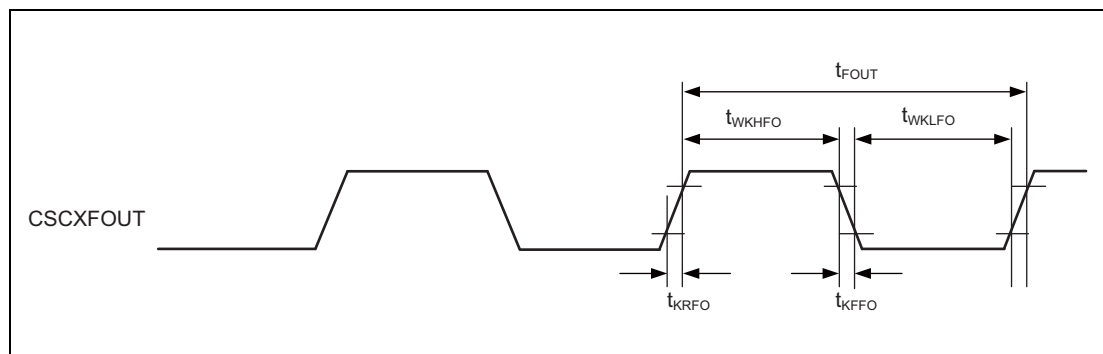
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	Slow mode	100 (max.10MHz)			ns
		Fast mode (Except JP0_3 pin)*1	33.4 (30MHz)			ns
CSCXFOUT high level width	t_{WKHFO}	Slow mode	N: 1*2 or even value*3	$t_{FOUT} / 2 - 37$		ns
			N: Odd value (N ≥ 5)*3, *4	$t_{FOUT} \times (N+1) / 2N - 37$		ns
		Fast mode (Except JP0_3 pin)*1	N: 1*2 or even value*3	$t_{FOUT} / 2 - 10$		ns
			N: Odd value (N ≥ 3)*3	$t_{FOUT} \times (N+1) / 2N - 10$		ns
CSCXFOUT low level width	t_{WKLFO}	Slow mode	N: 1*2 or even value*3	$t_{FOUT} / 2 - 37$		ns
			N: Odd value (N ≥ 5)*3, *4	$t_{FOUT} \times (N-1) / 2N - 37$		ns
		Fast mode (Except JP0_3 pin)*1	N: 1*2 or even value*3	$t_{FOUT} / 2 - 10$		ns
			N: Odd value (N ≥ 3)*3	$t_{FOUT} \times (N-1) / 2N - 10$		ns
CSCXFOUT rise / fall time	t_{KRFO} / t_{KFFO}	Slow mode			37	ns
		Fast mode (Except JP0_3 pin)*1			10	ns

Note 1. JP0_3 does not support fast mode.

Note 2. When MainOSC, HS IntOSC, LS IntOSC or SubOSC is selected as source clock with the condition of N=1, the characteristics of output signal depends on the selected source clock. It is recommended to use output signal after evaluation on an actual environment.

Note 3. "N" is the value of "Clock divisor N" defined by FOUTDIV register.

Note 4. The selection of N = 3 is prohibited when slow mode is used.



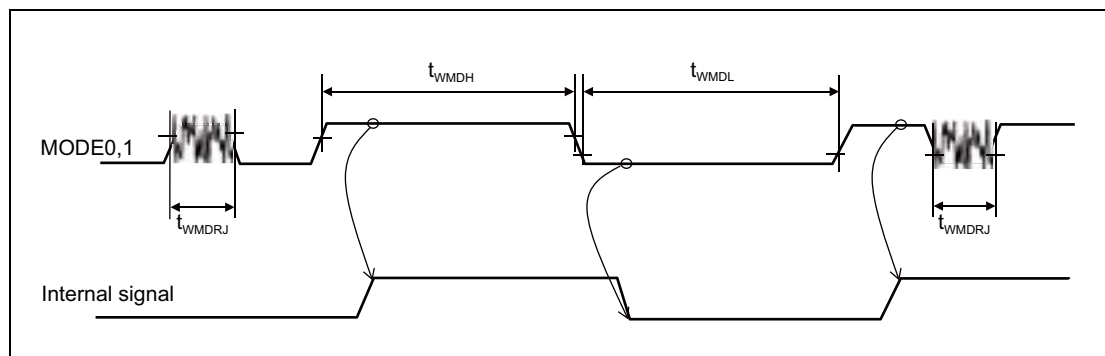
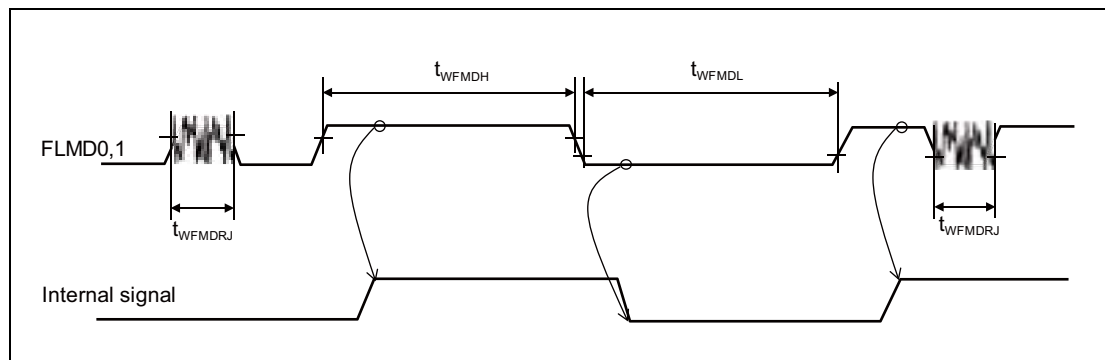
1.17 Mode Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0,1 input high / low level width*1	t_{WFMDH} / t_{WFMDL}		600			ns
FLMD0, 1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0,1 input high / low level width*1	t_{WMDH} / t_{WMDL}		600			ns
MODE0, 1 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0,1 and MODE0,1 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.

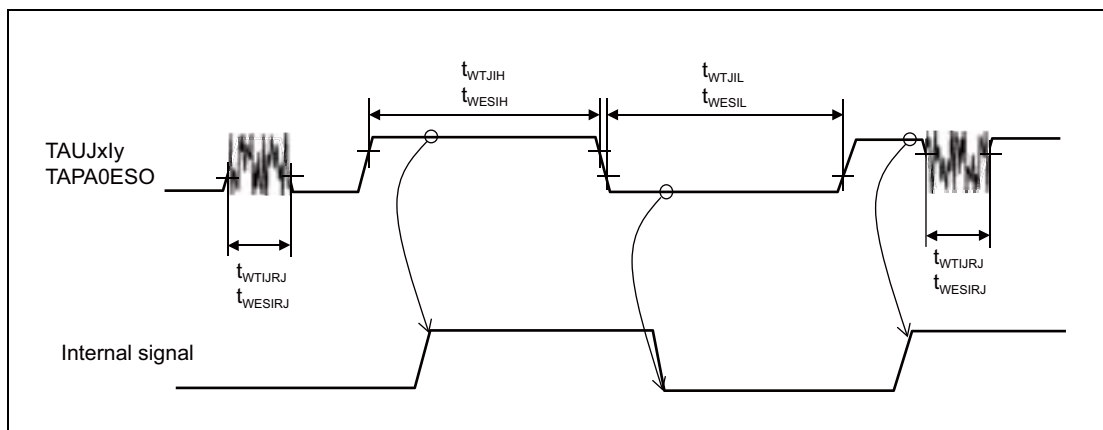
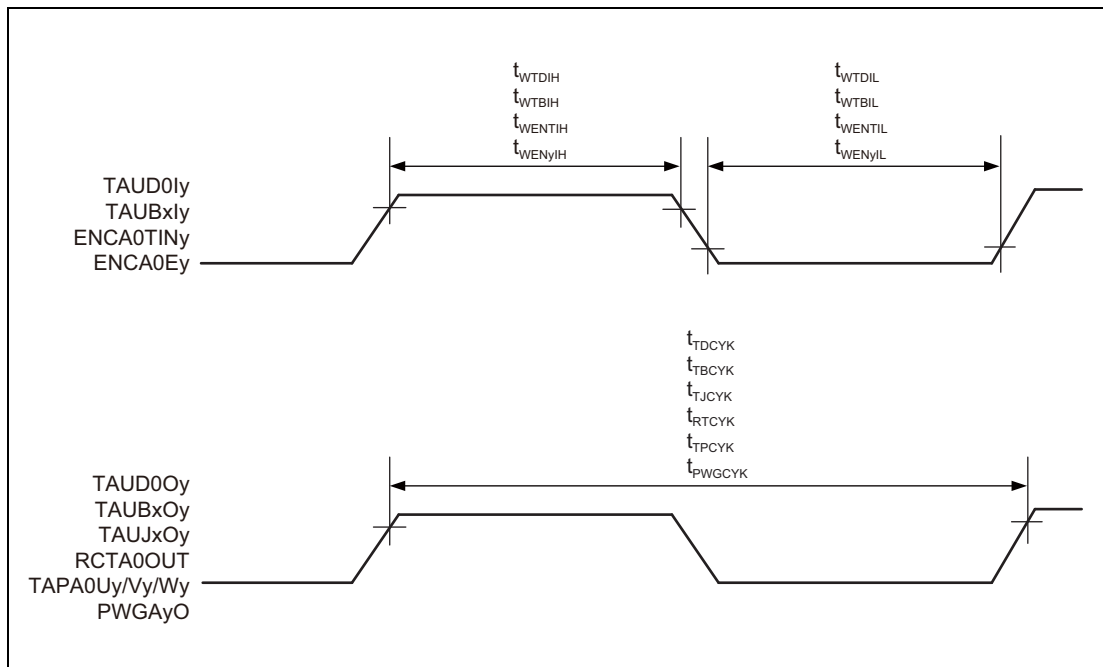


1.18 Timer Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1uF +/-30%, CISOVCL: 0.1uF +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0ly input high/low level width (y = 0 to 15)	t _{WTDIH} / t _{WTDIL}		n × Tsamp + 20 ^{*1, *2}			ns
TAUD0Oy output cycle (y = 0 to 15)	t _{TDCYK}	Slow mode			10	MHz
TAUBxly input high/low level width (x = 0, 1, y = 0 to 15)	t _{WTBIH} / t _{WTBIL}		n × Tsamp + 20 ^{*1, *2}			ns
TAUBxOy output cycle (x = 0, 1, y = 0 to 15)	t _{TBCYK}	Slow mode			10	MHz
TAUJxly input high/low level width ^{*3} (x = 0, 1, y = 0 to 3)	t _{WTJIH} / t _{WTJIL}		600			ns
TAUJxly pulse rejection ^{*4}	t _{WTJRJ}		100			ns
TAUJxOy output cycle (x = 0, 1, y = 0 to 3)	t _{TJCYK}	Slow mode			10	MHz
RTCA0OUT output cycle	t _{RTCYK}			1		Hz
TAPA0ESO input high/low level width ^{*3}	t _{WESIH} / t _{WESIL}		600			ns
TAPA0ESO pulse rejection ^{*4}	t _{WESIRJ}		100			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t _{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t _{WENTIH} / t _{WENTIL}		n × Tsamp + 20 ^{*1}			ns
ENCA0Ey input high/low level width (y = 0,1,C)	t _{WENyIH} / t _{WENyIL}		n × Tsamp + 20 ^{*1}			ns
PWGAyO output cycle (y = 0 to 95)	t _{PWGCYK}	Slow mode			10	MHz

- Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.
- Note 2. Input more than 1 count clock width of each timer counter channel.
- Note 3. TAUJxly and TAPA0ESO input width is needed to ensure that the internal timer input signal is activated.
- Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



1.19 RLIN2 / RLIN3 Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baudrate	1		115.2* ¹	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

Note 1. The LIN extended baudrate is not part of the LIN standard specification.

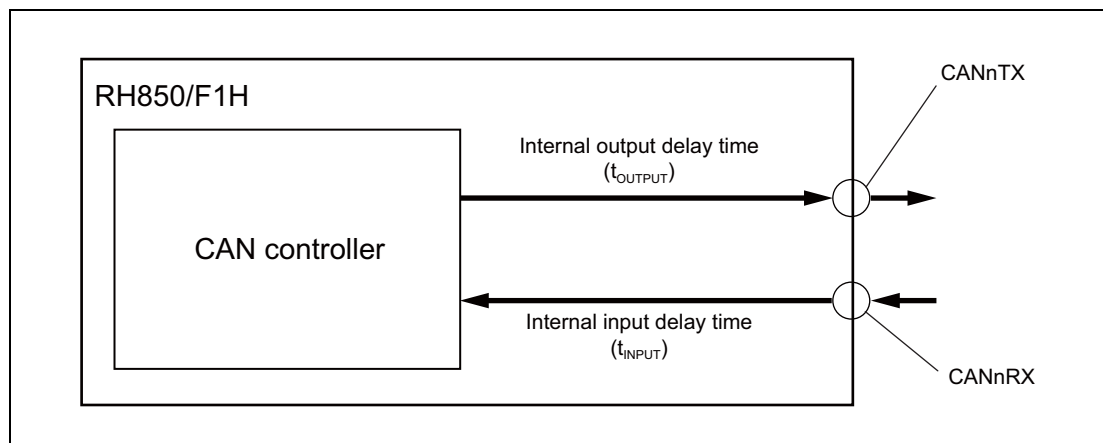
1.20 RS-CAN Timing

1.20.1 RS-CAN / RS-CANFD (Classical CAN Mode) Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1uF +/-30%, CISOVCL: 0.1uF +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time*1	t_{NODE}				100	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})

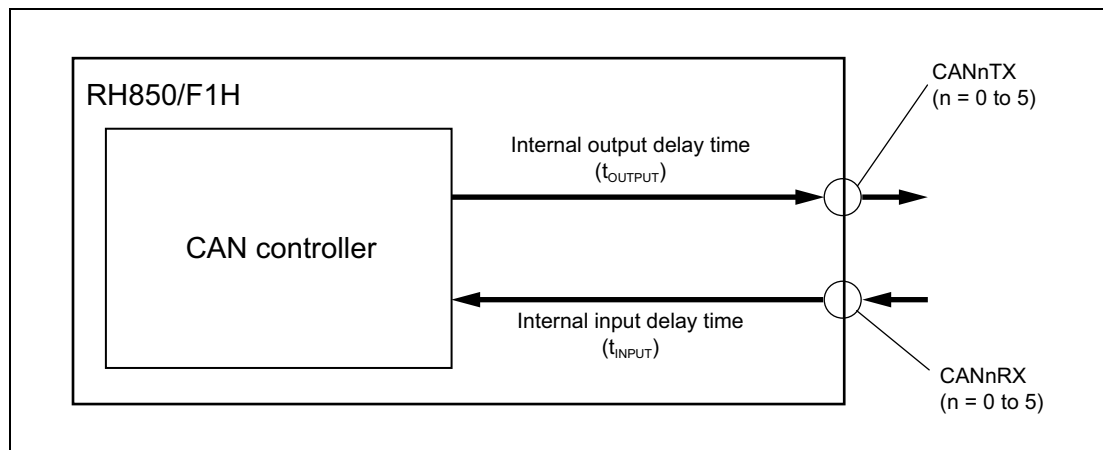


1.20.2 RS-CANFD (CAN-FD Mode) Timing (only PREMIUM product)

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1uF +/-30%, CISOVCL: 0.1uF +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					5	Mbps
Internal delay time*1	t_{NODE}				50	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



1.21 CSI Timing

1.21.1 CSIG Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Table 1.13 CSIG Timing (Master Mode)

<Output driver strength>

CSIGnSO, CSIGnSC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		$0.5 \times t_{KCYMGn} - 10$			ns
CSIGnSC low level width	t_{KWLMGn}		$0.5 \times t_{KCYMGn} - 10$			ns
CSIGnSI setup time (vs CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	$2 \times t_{KCYGn} + 25$			ns
CSIGnRYI High level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	$t_{KCYGn} + 5$			ns

¹**Table 1.14 CSIG Timing (Slave Mode)**

<Output driver strength>

CSIGnSO: Fast mode

CSIGnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		$0.5 \times t_{KCYSGn} - 10$			ns
CSIGnSC low level width	t_{KWLSGn}		$0.5 \times t_{KCYSGn} - 10$			ns
CSIGnSI setup time (vs CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs CSIGnSC)	t_{HSISGn}		$t_{KCYGn} + 5$			ns
CSIGnSO output delay (vs CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}	$t_{KCYSGn} \geq 8 \times t_{KCYGn}$			39	ns
		$t_{KCYSGn} < 8 \times t_{KCYGn}$			$39 + t_{KCYGn}$	ns
CSIGnSSI setup time (vs CSIGnSC)	t_{SSISGn}		$0.5 \times t_{KCYSGn} - 5$			ns
CSIGnSSI hold time (vs CSIGnSC)	$t_{HSSISGn}$		$t_{KCYGn} + 5$			ns

1.21.2 CSIH Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Table 1.15 CSIH Timing (Master Mode)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode (CL = 100 pF@n = 0 / 50 pF@n = 1 to 3)

CSIHnCSSm: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		$0.5 \times t_{KCYMHn} - 10$			ns
CSIHnSC low level width	t_{KWLMHn}		$0.5 \times t_{KCYMHn} - 10$			ns
CSIHnSI setup time (vs CSIHnSC)	t_{SSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs CSIHnSC)	t_{HSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	$t_{KCYHn} / 2$			ns
CSIHnSO output delay (vs CSIHnSC)	t_{DSOMHn}			7		ns
CSIHnRYI setup time (vs CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	$2 \times t_{KCYHn} + 25$			ns
CSIHnRYI High level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	$t_{KCYHn} + 5$			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		$CSIDLE \times t_{KCYMHn} - 15$			ns
CSIHnCSS0-7 setup time (vs CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	$CSSETUP \times t_{KCYMHn} - 23$			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	$(CSSETUP + 0.5) \times t_{KCYMHn} - 23$			ns
CSIHnCSS0-7 hold time (vs CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	$CSSHOLD \times t_{KCYMHn} - 5$			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	$(CSSHOLD + 0.5) \times t_{KCYMHn} - 5$			ns

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
 CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
 CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
 x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock period an inactive width time $t_{WSCSBHn}$ of " $0.5 \times t_{KCYMHn}$ " is added.

Table 1.16 CSIH Timing (Slave Mode)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode

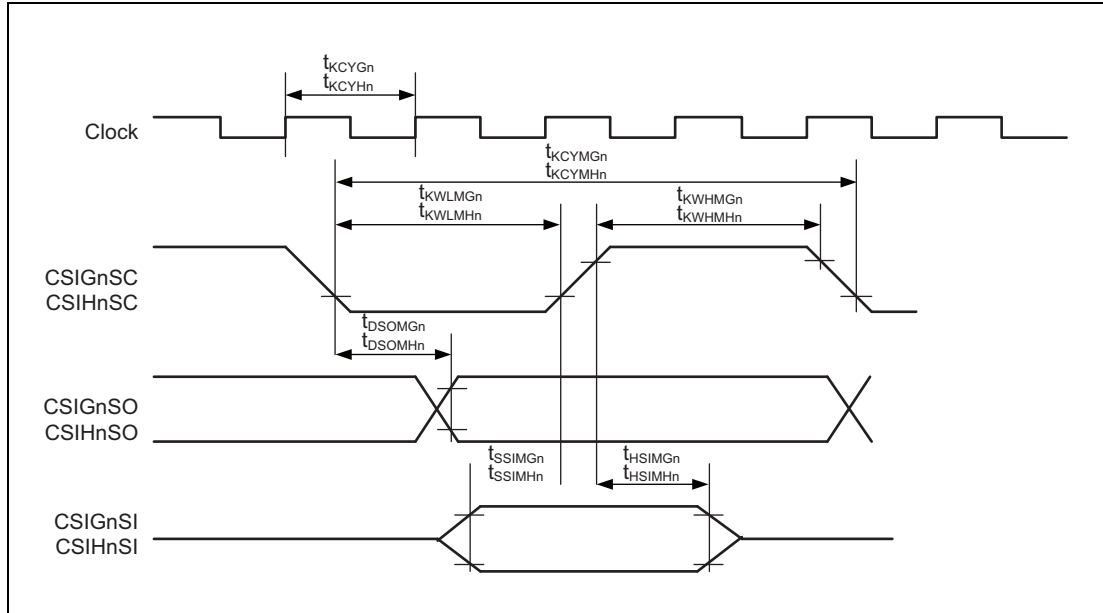
CSIHnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			39	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$39 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

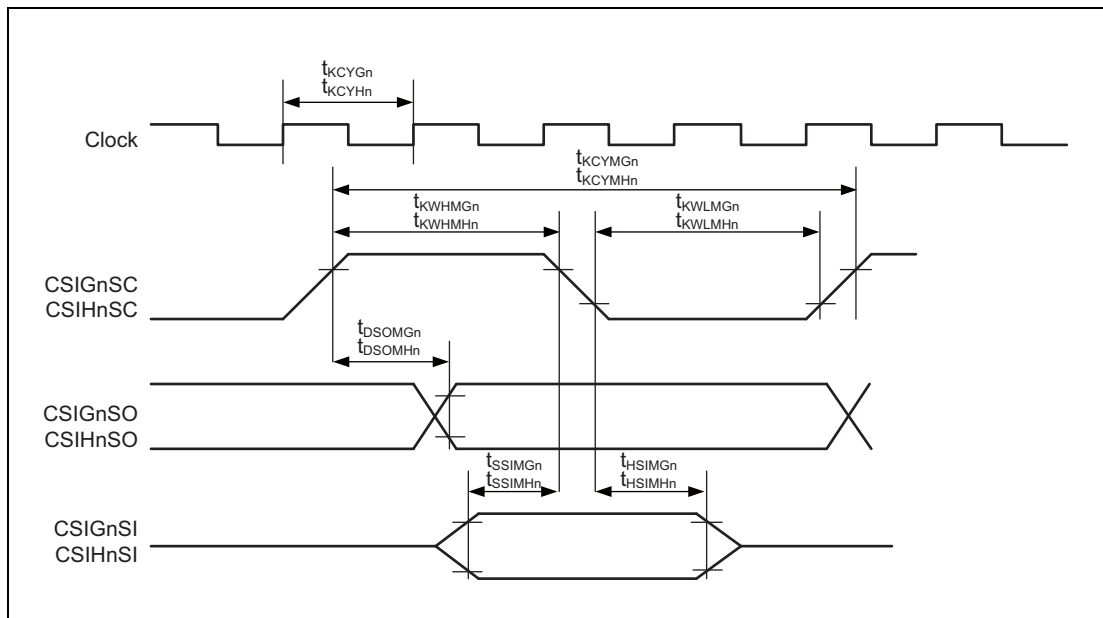
(1) SC/SI/SO

Master Mode:

- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

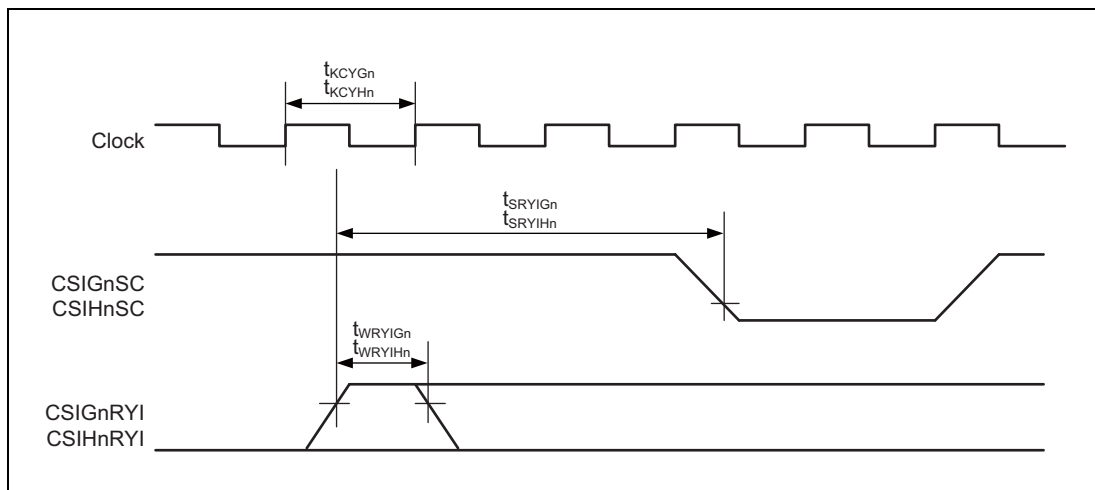


(2) RYI

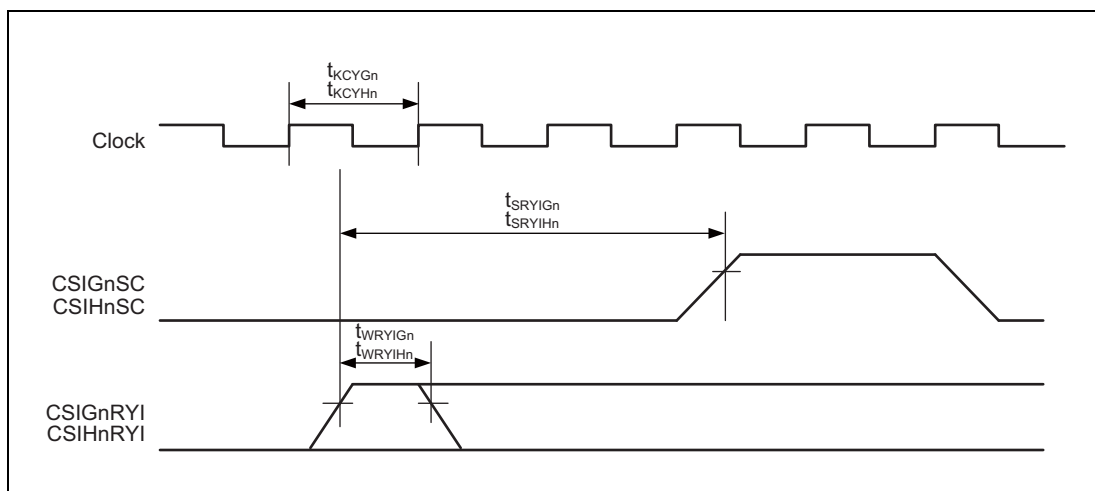
CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)

CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

- CSIG (CSIGnCTL1: CSIGnCKR = 0)
- CSIH (CSIHnCFGm: CSIHnCKPm = 0)



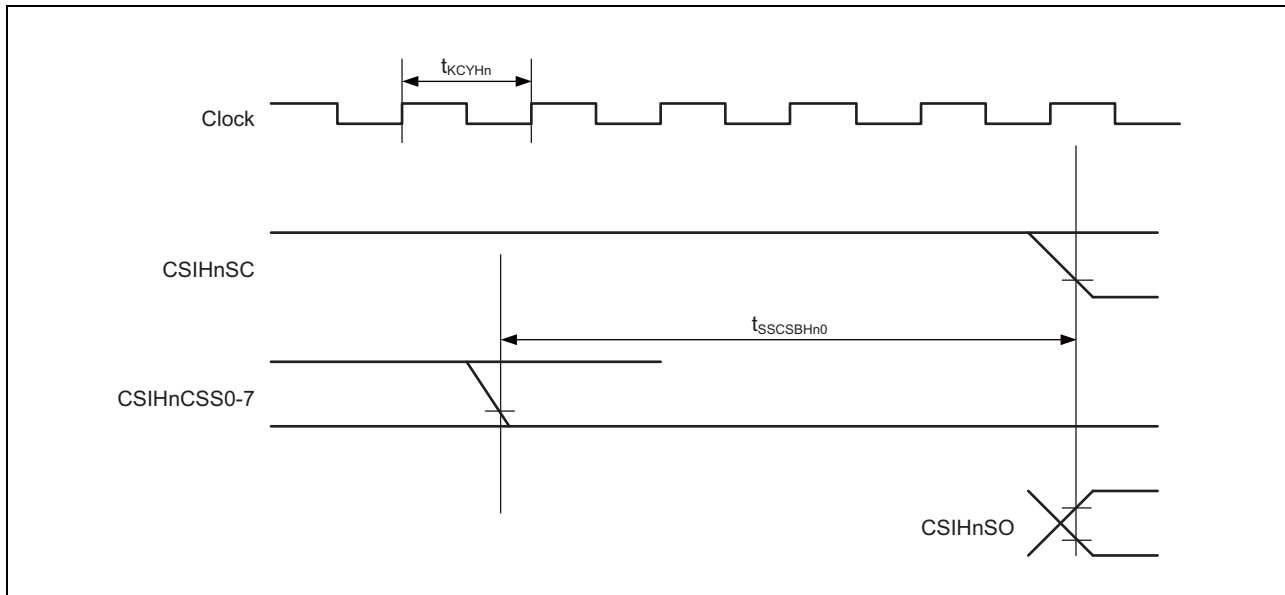
- CSIG (CSIGnCTL1: CSIGnCKR = 1)
- CSIH (CSIHnCFGm: CSIHnCKPm = 1)



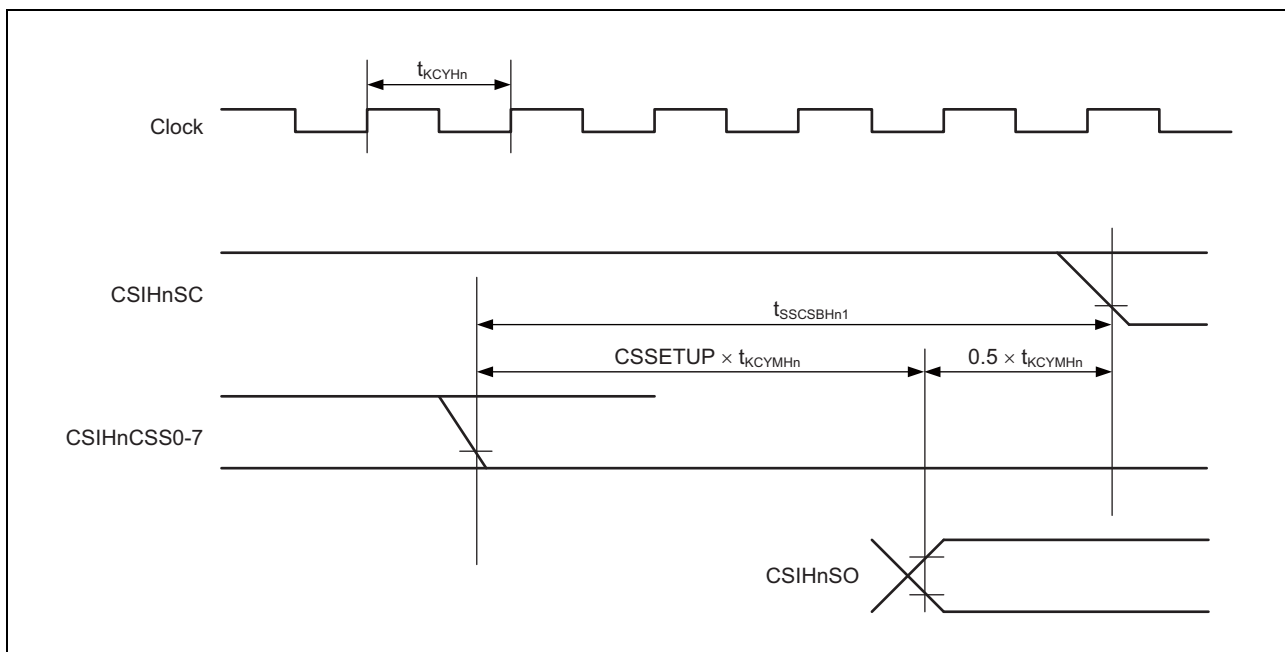
(3) CSSn

Only Master Mode (Setup Time):

- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0

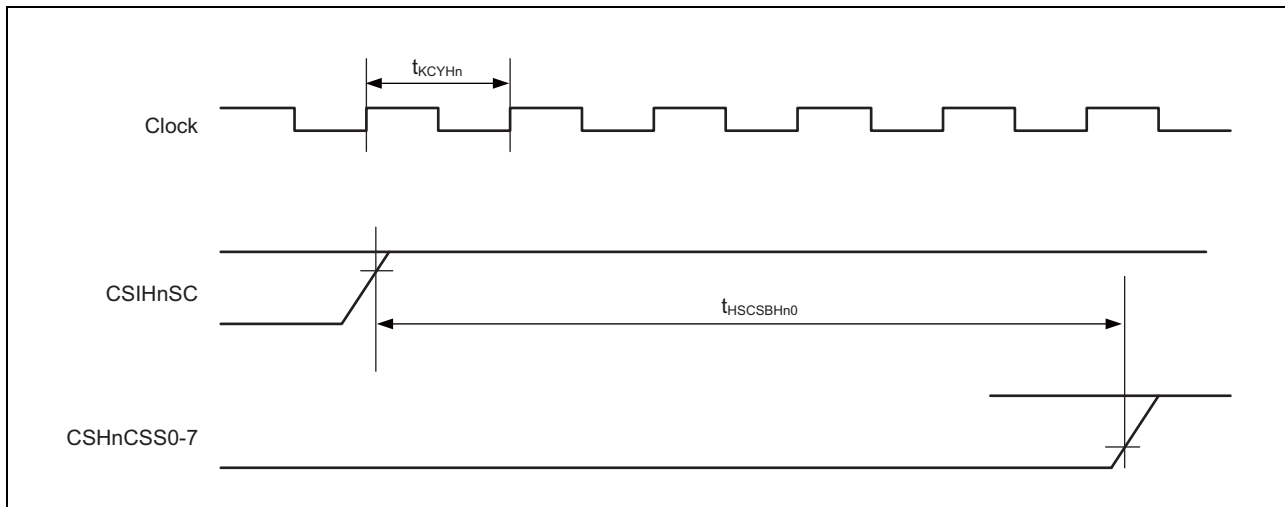


- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 1

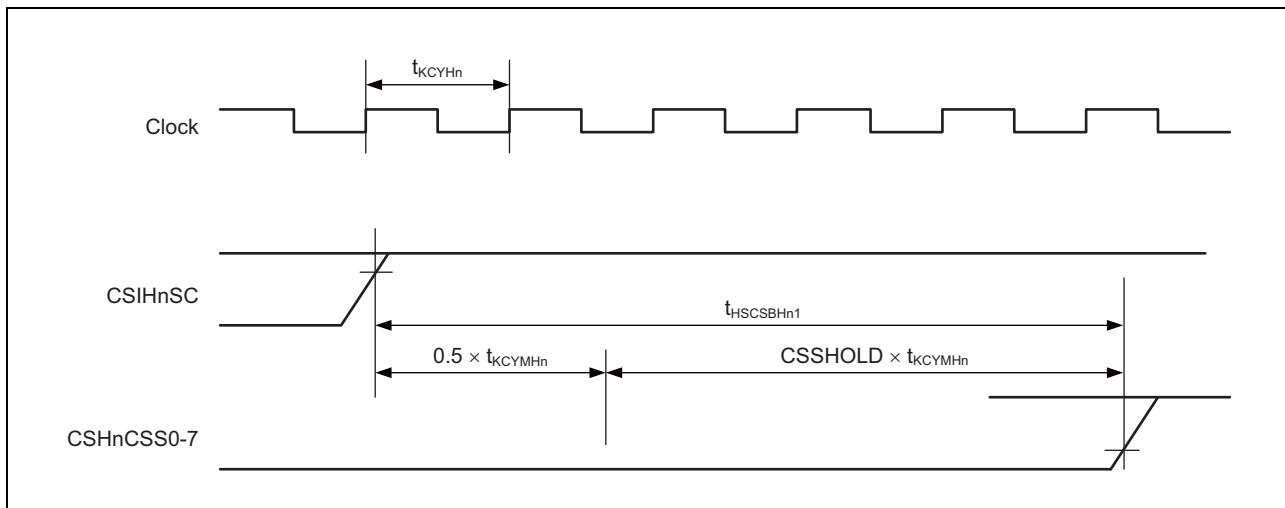


Only Master Mode (Hold Time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



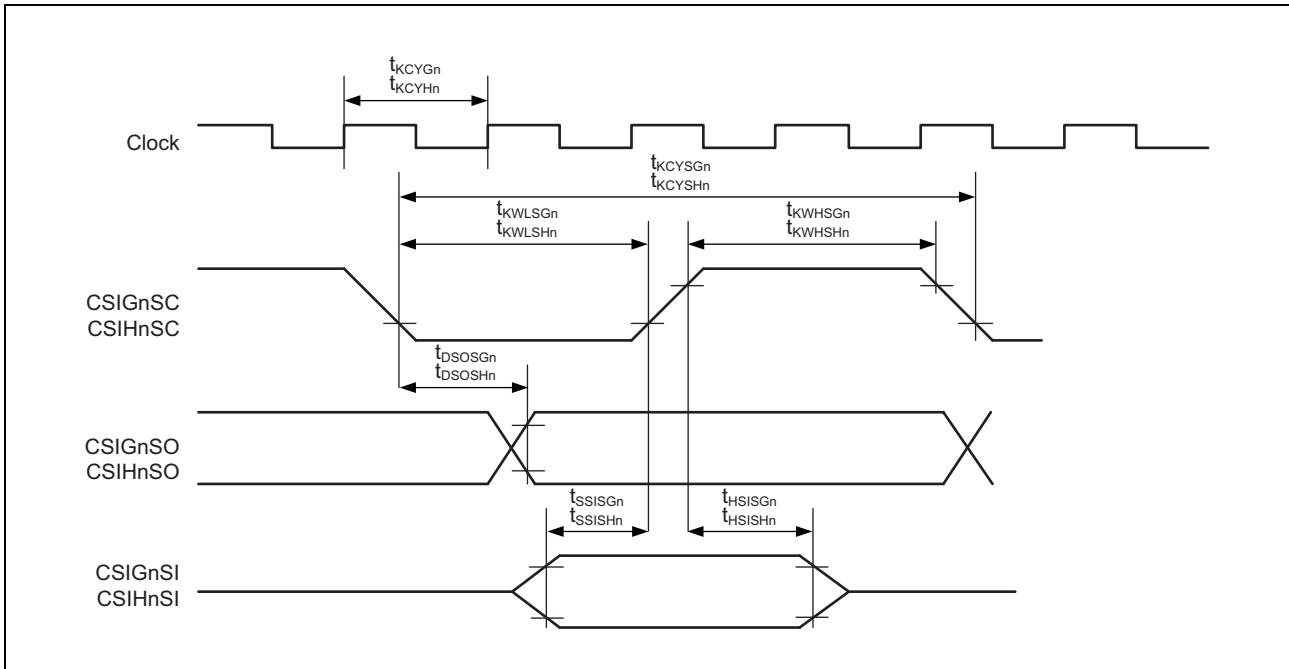
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



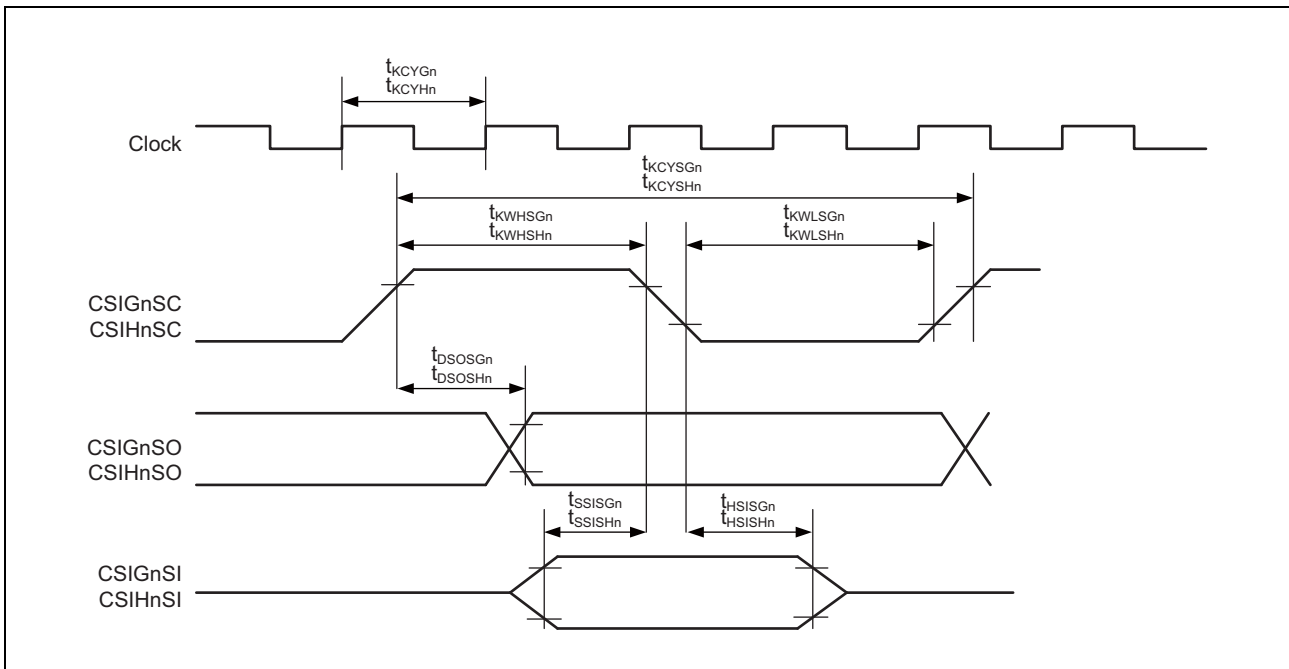
(4) SC/SI/SO

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0 /0 or 1/1)

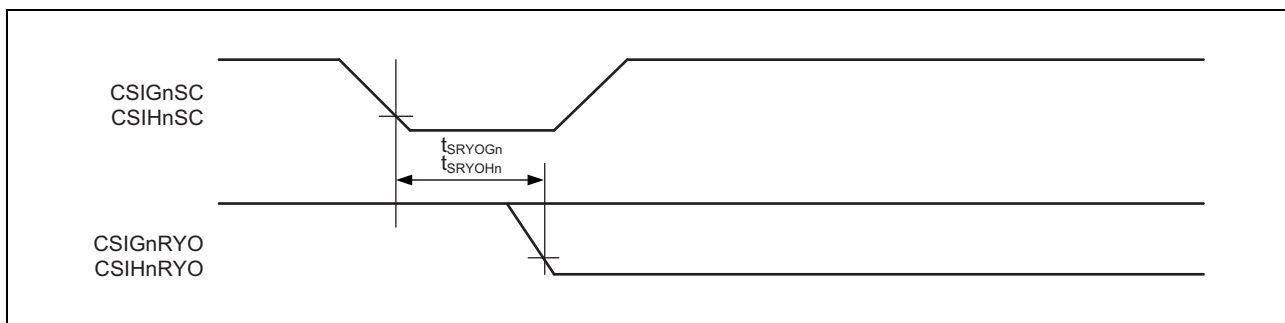


- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

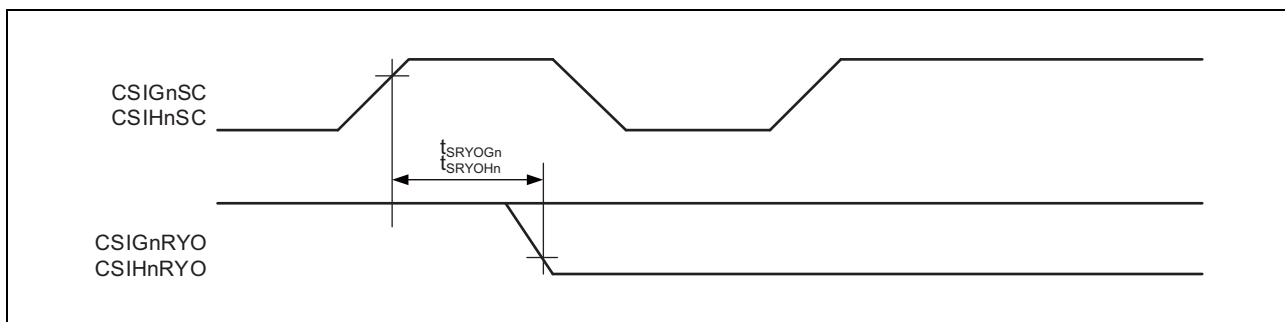


(5) RYO

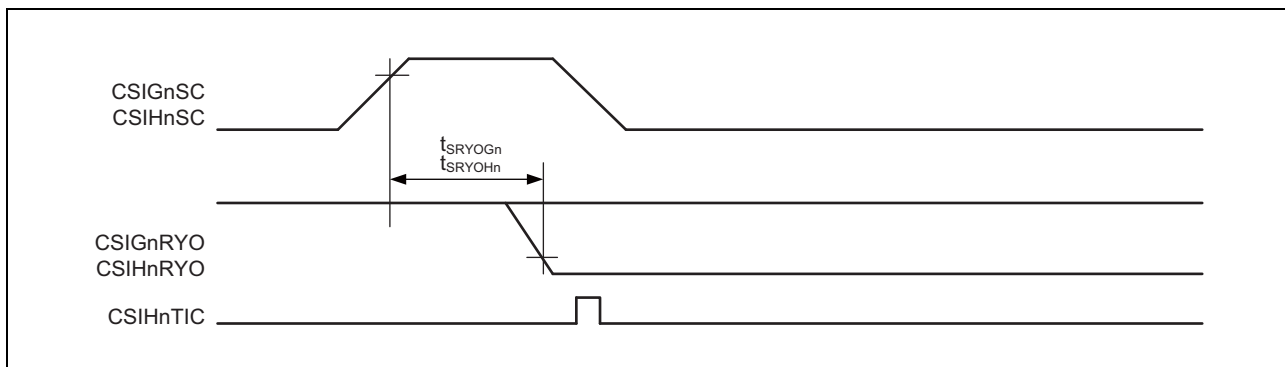
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0)



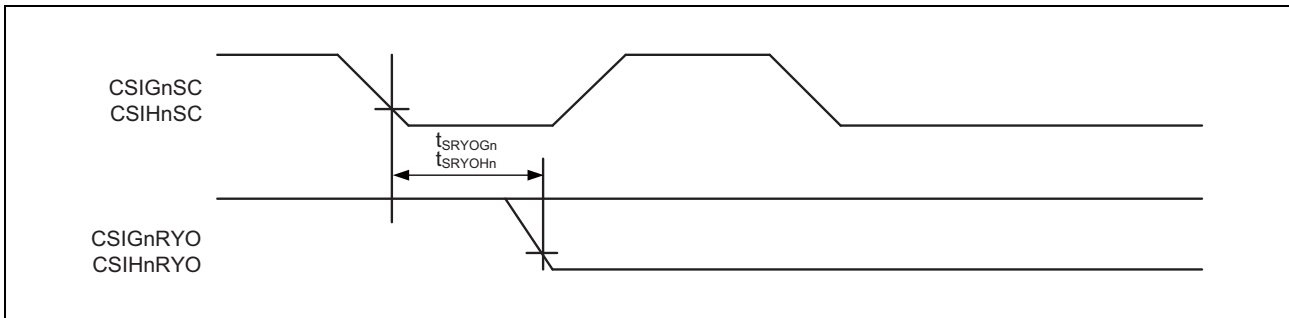
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0)



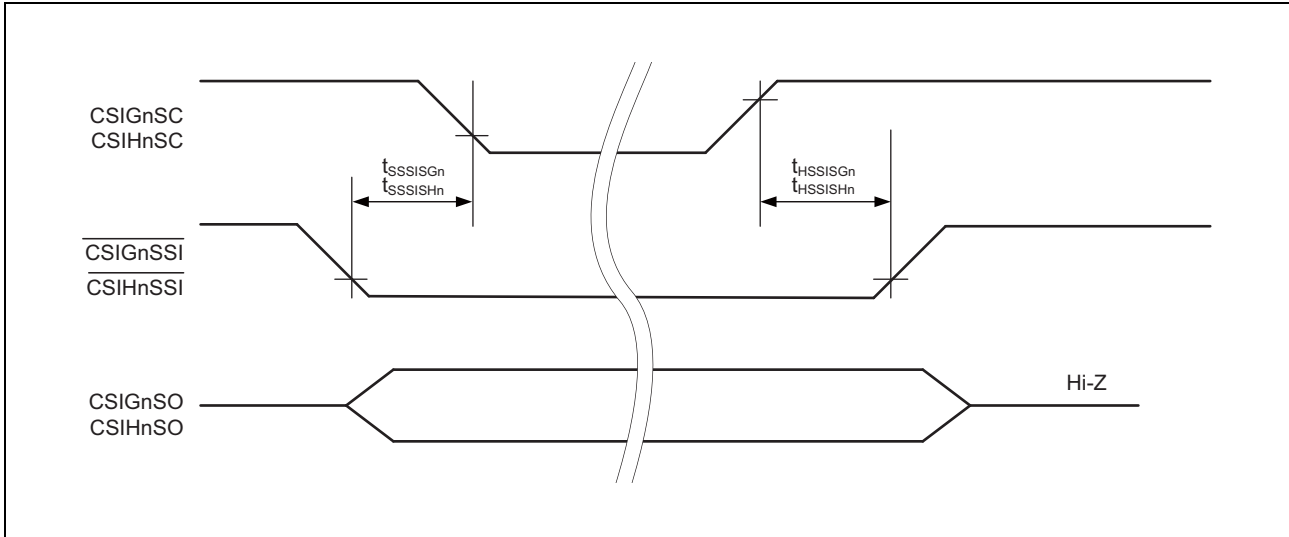
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/1)



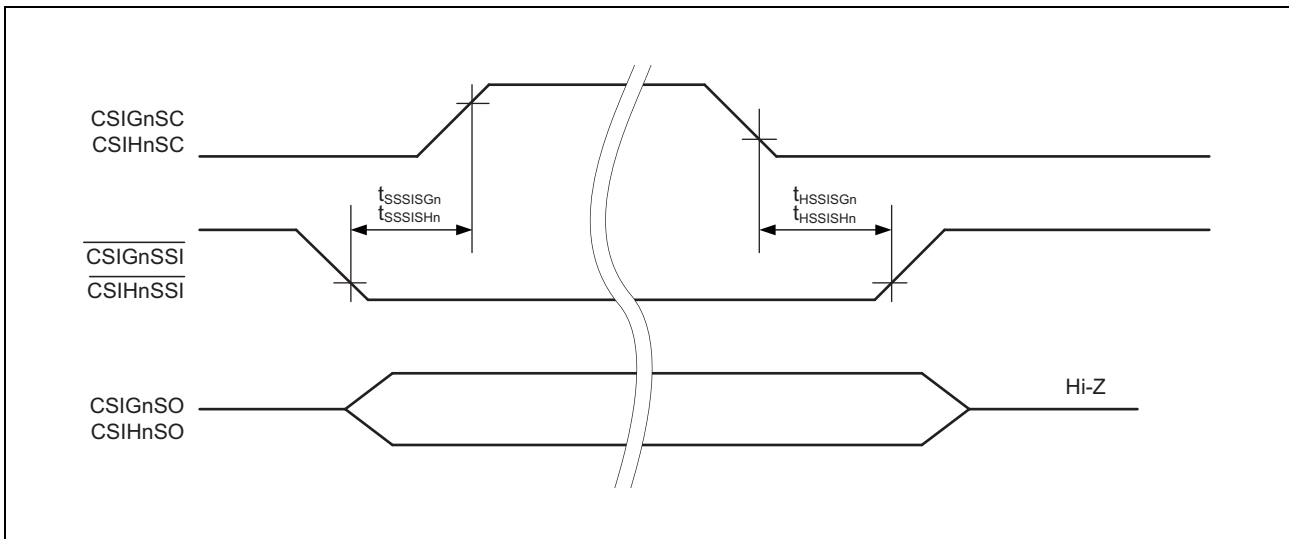
(6) SSI

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



1.22 RIIC Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C

Table 1.17 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			μ s
Hold time* ¹	t_{HD} : STA		4.0			μ s
RIIC0SCL clock low-level width	t_{LOW}		4.7			μ s
RIIC0SCL clock high-level time	t_{HIGH}		4.0			μ s
Setup time for start/restart condition	t_{SU} : STA		4.7			μ s
Data hold time	t_{HD} : DAT	CBUS compatible master	5.0			μ s
		IIC mode	0* ²			μ s
Data setup time	t_{SU} : DAT		250			ns
Stop condition setup time	t_{SU} : STO		4.0			μ s
Capacitance load of each bus line	C_b				400	pF

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{LOW}), only the maximum data hold time (t_{HD} : DAT) needs to be satisfied.

Table 1.18 RIIC Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			μ s
Hold time* ¹	t_{HD} : STA		0.6			μ s
RIIC0SCL clock low-level width	t_{LOW}		1.3			μ s
RIIC0SCL clock high-level time	t_{HIGH}		0.6			μ s
Setup time for start/restart condition	t_{SU} : STA		0.6			μ s
Data hold time	t_{HD} : DAT	IIC mode	0* ²			μ s
Data setup time	t_{SU} : DAT		100* ⁴			ns
Stop condition setup time	t_{SU} : STO		0.6			μ s
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	C_b				400	pF

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

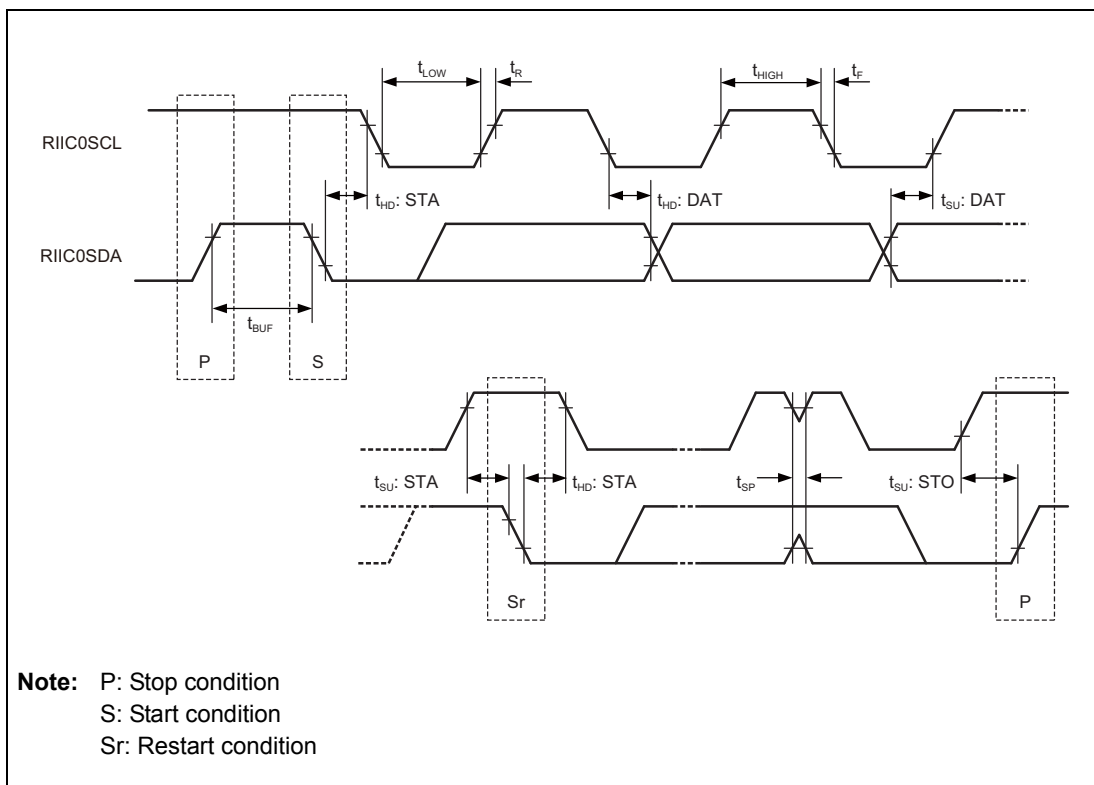
Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{LOW}), only the maximum data hold time (t_{HD} : DAT) needs to be satisfied.

Note 4. The fast mode IIC bus can be used in normal mode IIC bus system. In this case, set the fast mode IIC bus so that it meets the following conditions.

- If the system does not extend the RIIC0SCL signal's low state hold time: t_{SU} : DAT \geq 250 ns

- If the system extends the RIIC0SCL signal's low state hold time:

Transmit the following data bit to the RIIC0SDA line prior to releasing the RIIC0SCL line (1250 ns: Normal mode IIC bus specification).



1.23 FlexRay Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					10	Mbps

1.24 Ethernet Timing

1.24.1 MII Interface

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 15 pF

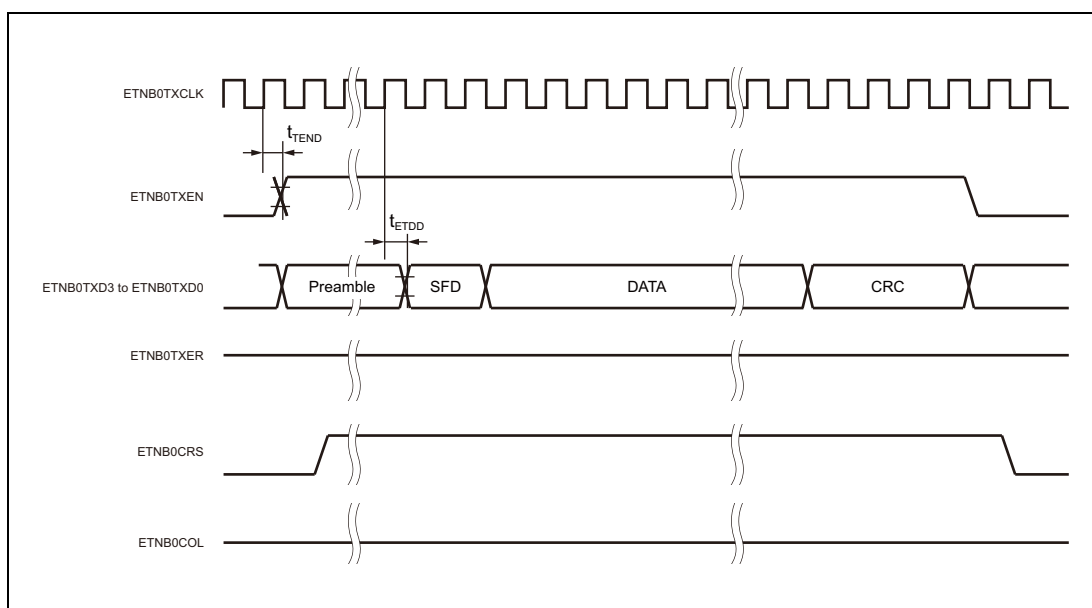
<Output driver strength>

ETNB0TXD3-0, ETNB0TXEN and ETNB0TXERR pin: Fast mode

ETNB0TXCLK pin: TTL type

Table 1.19 MII Interface (Transmission Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0TXCLK clock period	t_{Tcyc}		40			ns
ETNB0TXEN, ETNB0TXER delay vs ETNB0TXCLK \uparrow	t_{TEND}	CL = 15 pF			18	ns
ETNB0TXD[3:0] delay vs ETNB0TXCLK \uparrow	t_{ETDD}	CL = 15 pF			18	ns
ETNB0TXCLK high level width	t_{TKH}		$0.4 \times t_{Tcyc}$		$0.6 \times t_{Tcyc}$	ns
ETNB0TXCLK low level width	t_{TKL}		$0.4 \times t_{Tcyc}$		$0.6 \times t_{Tcyc}$	ns

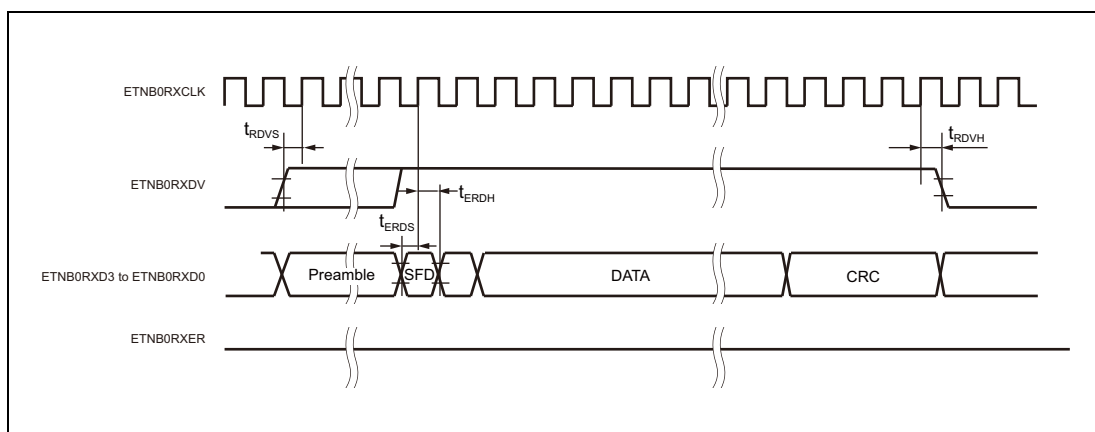


<Input buffer>

ETNB0RXCLK, ETNB0RXDV, ETNB0RXD[3:0] and ETNB0RXER pin: TTL type

Table 1.20 MII Interface (Reception Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0RXCLK clock period	t_{Rcyc}		40			ns
ETNB0RXDV hold time vs ETNB0RXCLK ↑	t_{RDVH}		10			ns
ETNB0RXDV setup time vs ETNB0RXCLK ↑	t_{RDVS}		10			ns
ETNB0RXD[3:0] hold time vs ETNB0RXCLK ↑	t_{ERDH}		10			ns
ETNB0RXD[3:0] setup time vs ETNB0RXCLK ↑	t_{ERDS}		10			ns
ETNB0RXER hold time vs ETNB0RXCLK ↑	t_{RERH}		10			ns
ETNB0RXER setup time vs ETNB0RXCLK ↑	t_{RERS}		10			ns
ETNB0RXCLK high level width	t_{RKH}		$0.4 \times t_{Rcyc}$		$0.6 \times t_{Rcyc}$	ns
ETNB0RXCLK low level width	t_{RKL}		$0.4 \times t_{Rcyc}$		$0.6 \times t_{Rcyc}$	ns



1.24.2 RMI Interface

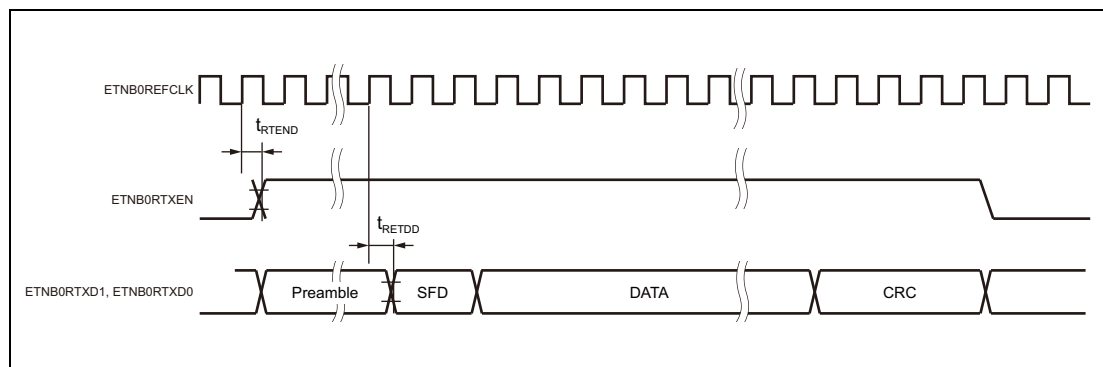
Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

<Input buffer>

ETNB0REFCLK pin: TTL type

Table 1.21 RMI Interface (Transmission Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0REFCLK clock period	f_{RTcyc}		50 – 50 ppm		50 + 50 ppm	MHz
ETNB0RTXEN delay vs ETNB0REFCLK \uparrow	t_{RTEND}				32	ns
ETNB0RTXD[1:0] delay vs ETNB0REFCLK \uparrow	t_{RETDD}				32	ns

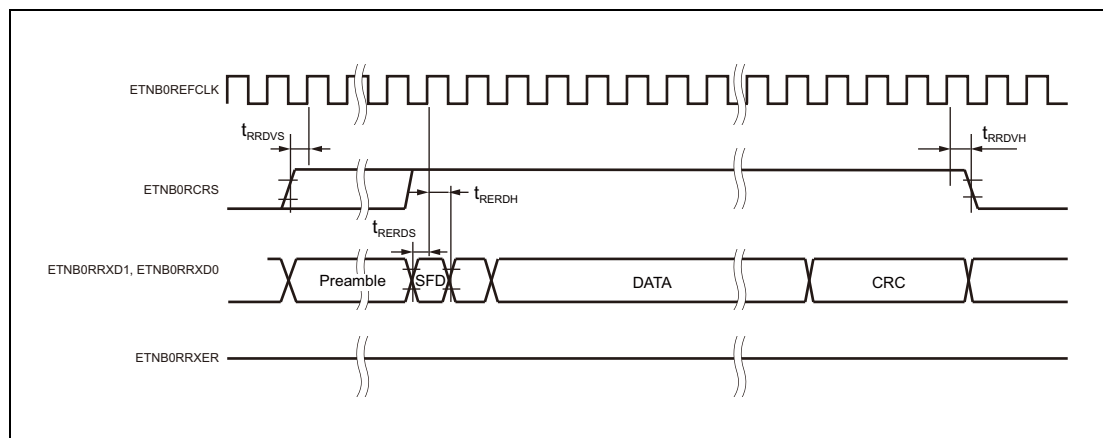


<Input buffer>

ETNB0REFCLK, ETNB0RCRS, ETNB0RRXD[1:0] and ETNB0RRXER pin: TTL type

Table 1.22 RMI Interface (Reception Interface)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNB0REFCLK clock period	f_{RTcyc}		50 – 50 ppm		50 + 50 ppm	MHz
ETNB0RCRS setup time vs ETNB0REFCLK \uparrow	t_{RRDVS}		6			ns
ETNB0RCRS hold time vs ETNB0REFCLK \uparrow	t_{RRDVH}		3			ns
ETNB0RRXD[1:0] setup time vs ETNB0REFCLK \uparrow	t_{RERDS}		6			ns
ETNB0RRXD[1:0] hold time vs ETNB0REFCLK \uparrow	t_{RERDH}		3			ns
ETNB0RRXER setup time vs ETNB0REFCLK \uparrow	t_{RRERS}		6			ns
ETNB0RRXER hold time vs ETNB0REFCLK \uparrow	t_{RRERH}		3			ns



1.24.3 Management Interface

Timing of management interface (ETNB0MDC and ETNB0MDIO) depends on software.

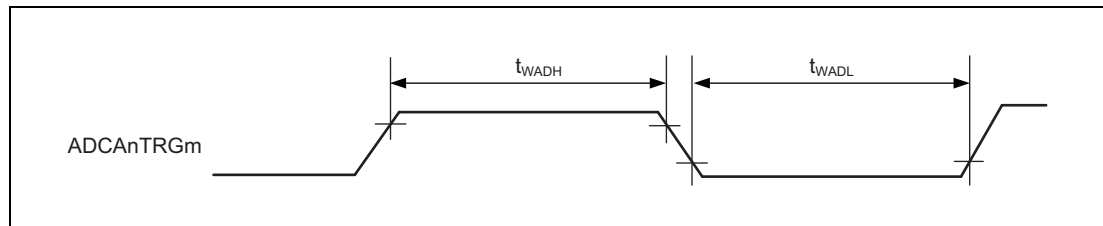
It is necessary to adjust wait time according to AC specification of PHY.

1.25 ADTRG Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high / low level width	t_{WADH} / t_{WADL}		$k \times T_{\text{samp}} + 20$ *1			ns

Note 1. k: Sampling number of the digital noise filter (DNFA_xxx) for each input.
Tsamp: Sampling time of the digital noise filter (DNFA_xxx) for each input.



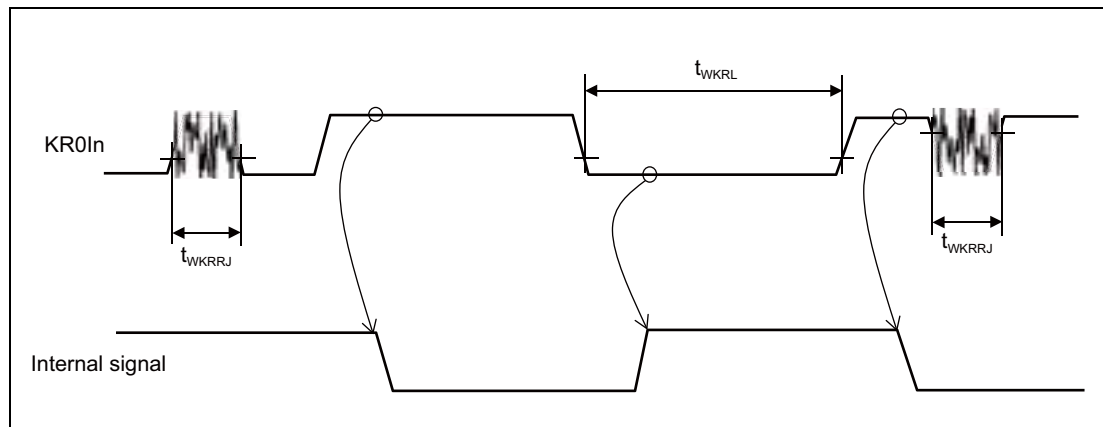
1.26 Key Return Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/-30%, CISOVCL: 0.1 μ F +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.

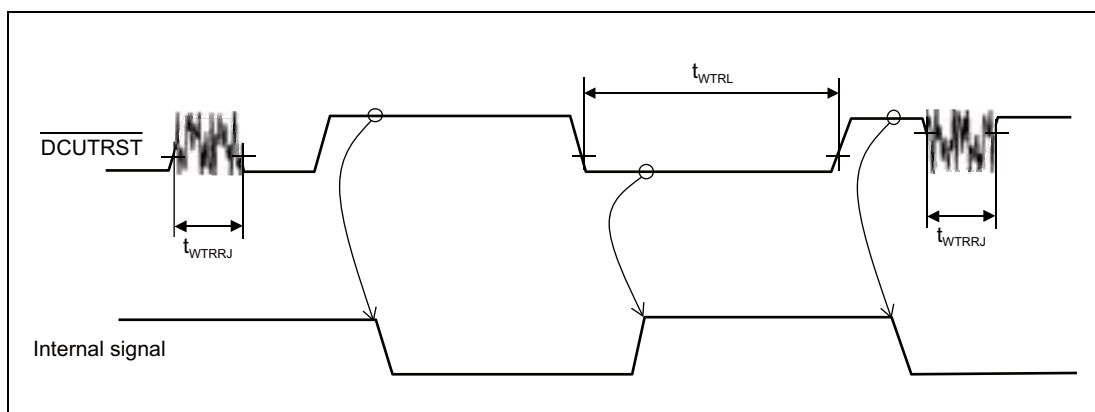


1.27 DCUTRST Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1uF +/-30%, CISOVCL: 0.1uF +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTRST input low level width*1	t_{WTRL}		600			ns
DCUTRST pulse rejection*2	t_{WTRRJ}		100			ns

- Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.
 Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



1.28 Debug Interface Characteristics

1.28.1 Nexus Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1uF +/-30%, CISOVCL: 0.1uF +/-30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

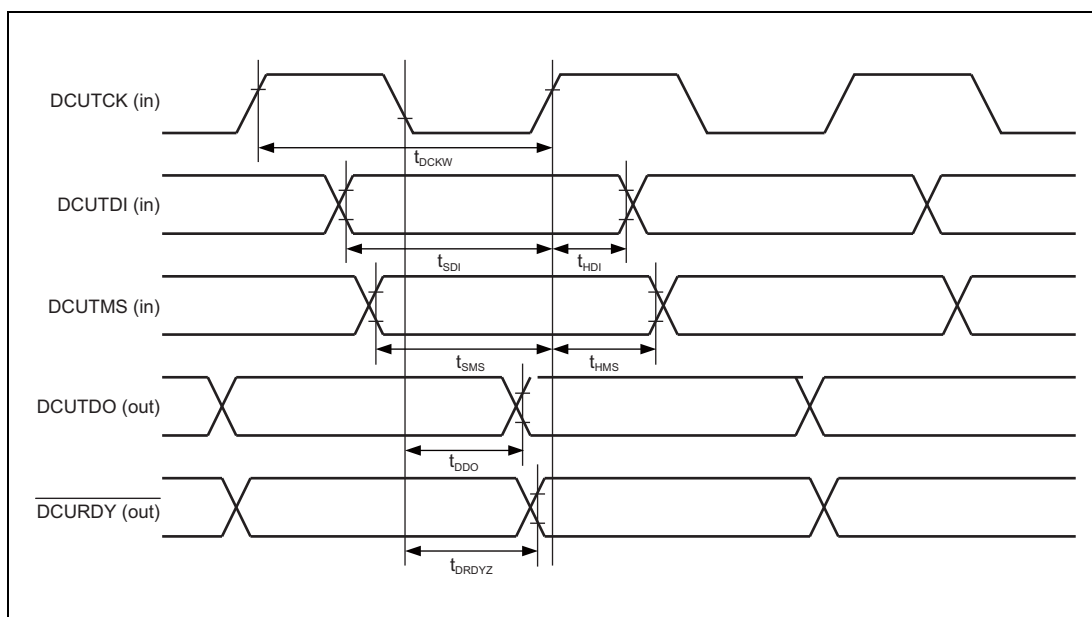
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTCK \uparrow)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK \uparrow)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK \uparrow)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK \uparrow)	t_{HMS}		3			ns
DCUTDO delay time (\downarrow DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (\downarrow DCUTCK)	t_{RDYZ}		0		20	ns



1.28.2 LPD (4 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V,
A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C,
CL = 30 pF

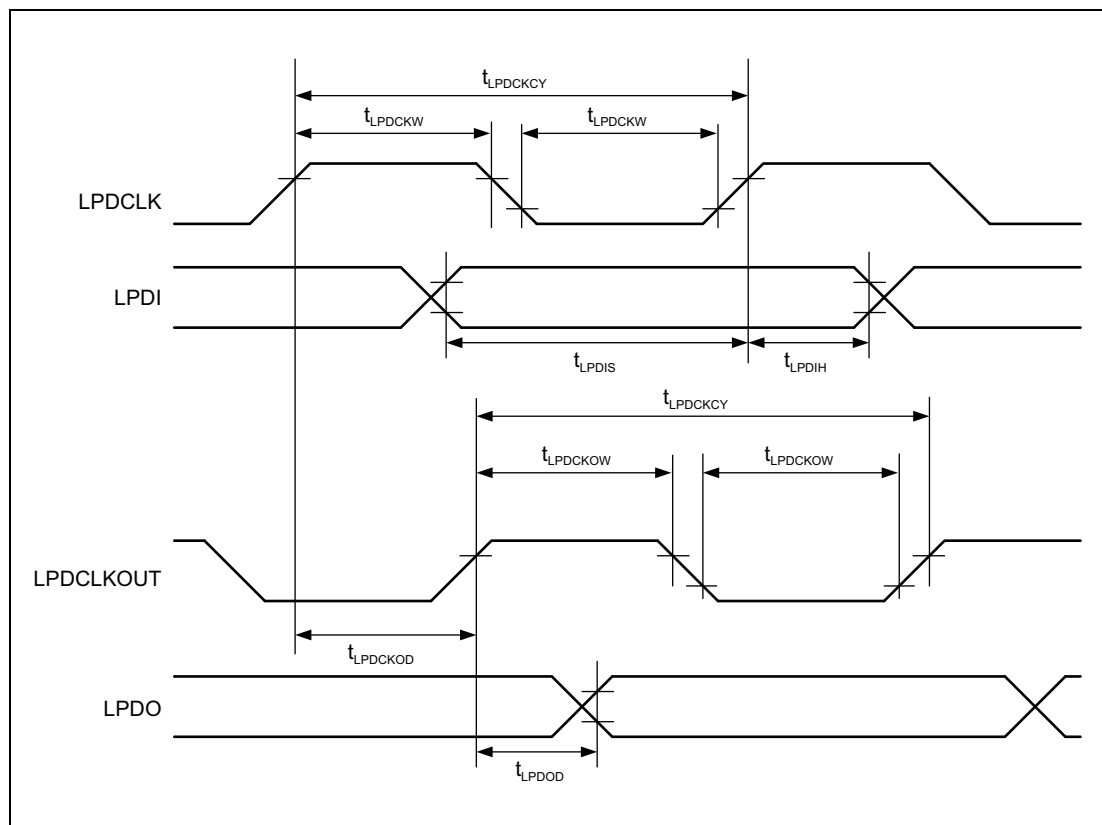
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCKCY}$		83.3 (max. 12 MHz)			ns
LPDCLK High-level width / LPDCLK Low-level width	t_{LPDCKW}		$0.5 \times t_{LPDCKCY} - 10$			ns
LPDCLKOUT High-level width / LPDCLKOUT low-level width	$t_{LPDCKOW}$		$t_{LPDCKW} - 10$			ns
LPDI setup time (LPDCLK \uparrow)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK \uparrow)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$			44		ns
LPDO delay time (LPDCLKOUT \uparrow)	t_{LPDOD}		0	15		ns



1.28.3 LPD (1 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V,
 A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,
 CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL =
 50 pF

<Input buffer>

LPDIO: TTL

<Output driver strength>

LPDIO: Fast mode

<External pull-up resistor>

LPDIO: 4.7 k Ω to 10 k Ω

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) baud rate					2.0	Mbps

1.29 Flash Programming Characteristics

1.29.1 Code Flash

The code flash memory is shipped in the erase state. If the code flash memory is read where it has not been written after ensure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Table 1.23 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}^{*3}		4 ^{*4}		30	MHz
Number of rewrites ^{*1}	CWRT	Data retention: 20 years ^{*2}	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is "n" (n = 1000), the device can be erased "n" times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful ensure of the code flash memory.

Note 3. $f_{PCLK} = 1/4 f_{CPUCLK}$: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.24 Programming Characteristics (1/2)

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit			
Programming time		$f_{PCLK} \geq 20$ MHz CWRT < 100 times	256 B		0.4* ¹	6* ¹	ms			
			8 KB		20	90	ms			
			32 KB		80	360	ms			
			256 KB		0.6	2.7	s			
			384 KB		0.9	4.1	s			
			512 KB		1.2	5.4	s			
			768 KB		1.7	8.1	s			
			1 MB		2.3	10.8	s			
			1.5 MB		3.4	16.2	s			
			2 MB		4.5	21.5	s			
			3 MB		6.8	32.3	s			
			4 MB		9	43	s			
			6 MB		13.5	64.5	s			
					$f_{PCLK} \geq 20$ MHz CWRT \geq 100 times	256 B		0.5* ¹	7.2* ¹	ms
						8 KB		24	108	ms
						32 KB		96	432	ms
						256 KB		0.7	3.3	s
384 KB		1.1				4.9	s			
512 KB		1.4				6.5	s			
768 KB		2.1				9.8	s			
1 MB		2.7				13	s			
1.5 MB		4.1				19.5	s			
2 MB		5.4				26	s			
3 MB		8.1				39	s			
4 MB		10.8	52	s						
6 MB		16.2	78	s						

Table 1.24 Programming Characteristics (2/2)

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Erase time		$f_{PCLK} \geq 20\text{MHz}$ CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
			1.5 MB		6.8	21	s
			2 MB		9	28	s
			3 MB		13.6	42	s
		4 MB		18.1	56	s	
		6 MB		27	84	s	
		$f_{PCLK} \geq 20\text{ MHz}$ CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s
			1.5 MB		8.1	25.2	s
2 MB			10.8	33.6	s		
3 MB			16.2	50.4	s		
4 MB		21.6	67.2	s			
6 MB		32.4	100.8	s			

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.29.2 Data Flash

The data flash memory is shipped in the erase state. If the data flash memory is read where it has not been written after ensure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Table 1.25 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}^{*3}		4 ^{*4}		30	MHz
Number of rewrites ^{*1}	CWRT	Data retention: 20 years ^{*2}	125 k			times
		Data retention: 3 years ^{*2}	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is "n" (n = 125000), the device can be erased "n" times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. $f_{PCLK} = 1/4 f_{CPUCLK}$: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.26 Programming Characteristics

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		$f_{PCLK} \geq 20$ MHz	4 B		0.16 ^{*1}	1.7 ^{*1}	ms
			64 KB		2.79	13.44	s
Erasure time		$f_{PCLK} \geq 20$ MHz	64 B		1.7 ^{*1}	10 ^{*1}	ms
			64 KB		1.74	10.24	s
Blank check time		$f_{PCLK} \geq 20$ MHz	4 B			30 ^{*1}	μ s
			64 B			100 ^{*1}	μ s
			64 KB			70.4	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.29.3 Serial Programming Interface

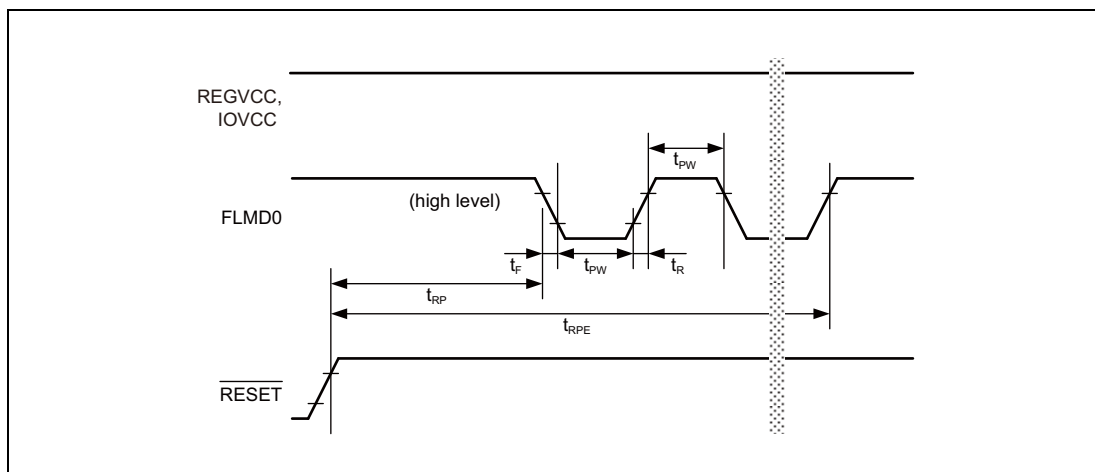
1.29.3.1 Serial Programmer Setup Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				101.5	ms
FLMD0 low/high level width	t_{PW}		1.6			μ s
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

NOTE

IOVCC: EVCC = BVCC = A0VREF = A1VREF



1.29.3.2 FLSCI3 Interface

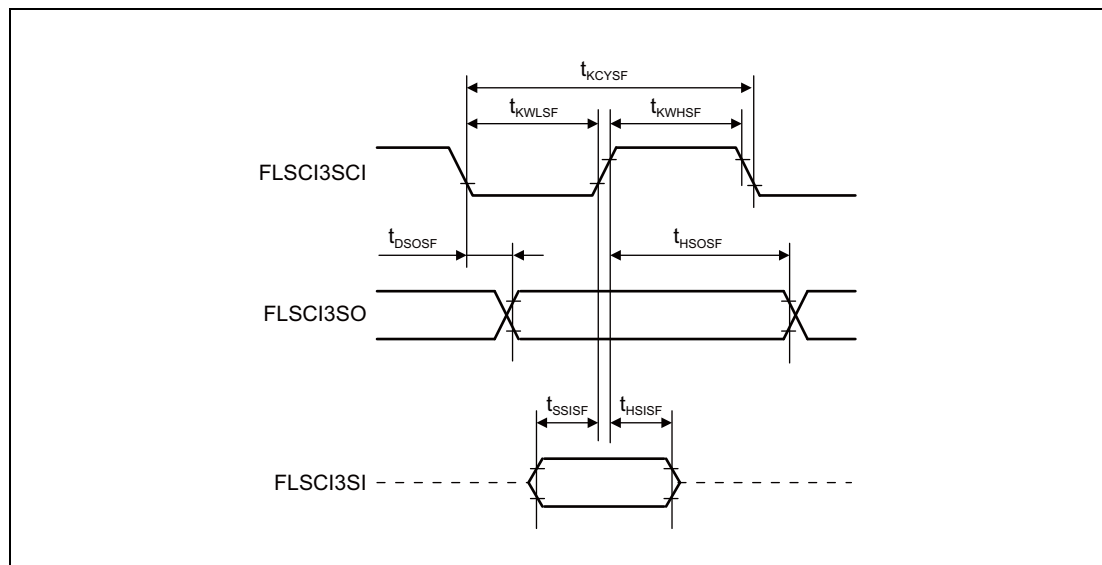
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLSCI3 transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode			1.5	Mbps
FLSCI3SCI cycle time	t_{KCYSF}	3-wired Clock Sync mode	200* ¹			ns
FLSCI3SCI high level width	t_{KWHSF}	3-wired Clock Sync mode	$t_{KCYSF} / 2 - 15$			ns
FLSCI3SCI low level width	t_{KWLSF}	3-wired Clock Sync mode	$t_{KCYSF} / 2 - 15$			ns
FLSCI3SI setup time (vs FLSCI3SCI)	t_{SSISF}	3-wired Clock Sync mode	55			ns
FLSCI3SI hold time (vs FLSCI3SCI)	t_{HSISF}	3-wired Clock Sync mode	55			ns
FLSCI3SO output delay (vs FLSCI3SCI)	t_{DSOSF}	3-wired Clock Sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired Clock Sync mode Not continuous transfer (data: except 1st bit)			$-t_{KWHSF} + 3 \times t_{Pcyc} + 36$	ns
FLSCI3SO hold time (vs FLSCI3SCI)	t_{HSOSF}	3-wired Clock Sync mode	$2 \times t_{Pcyc}$			ns

Note 1. Input the external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



1.30 A/D Converter Characteristics

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 μ F +/- 30%, CISOVCL: 0.1 μ F +/- 30%, Ta = -40 to (depend on the product) °C, CL = 30 pF

(1/3)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLKn		8*3		40	MHz
Resolution	RESn	12-bit mode	12	12	12	bit
		10-bit mode	10	10	10	bit
Conversion time	t _{CONn}	ADCA _n SMPCR.SMPT[7:0] = 12H (40 cycle) (8MHz*3 ≤ ADCLKn ≤ 32 MHz). External MPX is not used.	1.25		5	μs
		ADCA _n SMPCR.SMPT[7:0] = 18H (46 cycle) (8MHz*3 ≤ ADCLKn ≤ 40 MHz). External MPX is not used.	1.15		5.75	μs
		ADCA _n SMPCR.SMPT[7:0] = 12H (80 cycle) (8MHz*3 ≤ ADCLKn ≤ 32 MHz). External MPX is used.	2.5*4		10	μs
		ADCA _n SMPCR.SMPT[7:0] = 18H (92 cycle) (8MHz*3 ≤ ADCLKn ≤ 40MHz). External MPX is used.	2.3*4		11.5	μs
Sampling time	t _{SMP}	ADCA _n SMPCR.SMPT[7:0] = 12H (18 cycle) (8MHz*3 ≤ ADCLKn ≤ 32 MHz)	0.56		2.25	μs
		ADCA _n SMPCR.SMPT[7:0] = 18H (24 cycle) (8MHz*3 ≤ ADCLKn ≤ 40 MHz)	0.6		3	μs
Analog input voltage	VAIN0SN	ADCA _n Im T&H not used	AnVSS		AnVREF	V
		ADCA0I0-5 T&H used	0.2		A0VREF - 0.2	V
		ADCA0ImS A0VREF ≥ EVCC	A0VSS		EVCC	V
		A0VREF < EVCC	A0VSS		A0VREF	V
		ADCA1ImS A1VREF ≥ BVCC	A1VSS		BVCC	V
		A1VREF < BVCC	A1VSS		A1VREF	V
Operation current	IA0VREF IA1VREF	T&H is not used		1.1	3.0	mA
		T&H used (max. 6 pins)			*2	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS IA1VREFS			1	10	μA
T&H current	ITH			0.5	1.3	mA/ch
T&H sampling time	t _{THSMP}		450			ns
T&H hold time	t _{THHOLD}				10	μs
Set up time of self diagnosis voltage circuit	t _{BOOT}		500			ns
Set up time of self diagnosis voltage level	t _{OUT}		500			ns
Pull-down resistor for Discharge mode	ADCA _n Im pins		350	500	650	kΩ
	ADCA _n ImS pins		100	215	800	kΩ

(2/3)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit		
Accuracy of Self-diagnosis function	TESH0SN	12-bit mode	Self-diagnosis voltage level = AnVREF		4015 – [TOEn]	4095	—	
			Self-diagnosis voltage level = 2/3AnVREF		2651 – [TOEn]	2731	2811 + [TOEn]	—
			Self-diagnosis voltage level = 1/2AnVREF		1968 – [TOEn]	2048	2128 + [TOEn]	—
			Self-diagnosis voltage level = 1/3AnVREF		1285 – [TOEn]	1365	1445 + [TOEn]	—
			Self-diagnosis voltage level = AnVSS		0		80 + [TOEn]	—
		10-bit mode	Self-diagnosis voltage level = AnVREF		1003 – [TOEn]		1023	—
			Self-diagnosis voltage level = 2/3AnVREF		663 – [TOEn]	683	703 + [TOEn]	—
			Self-diagnosis voltage level = 1/2AnVREF		492 – [TOEn]	512	532 + [TOEn]	—
			Self-diagnosis voltage level = 1/3AnVREF		321 – [TOEn]	341	361 + [TOEn]	—
			Self-diagnosis voltage level = AnVSS		0		20 + [TOEn]	—
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V		ADCA0Im (w/o T&H)		±4.0	LSB
					ADCA0I0-5 (w/ T&H)		±6.0	LSB
			AnVREF = 3.6 V to 4.5 V		ADCA0Im (w/o T&H)		±6.0	LSB
					ADCA0I0-5 (w/ T&H)		±8.0	LSB
			AnVREF = 3.0 V to 3.6 V		ADCA0Im (w/o T&H)		±8.0	LSB
				ADCA0I0-5 (w/ T&H)		±10.0	LSB	
		10-bit mode	AnVREF = 4.5 V to 5.5 V		ADCA0Im		±1.0	LSB
					ADCA0ImS		±2.0	LSB
			AnVREF = 3.6 V to 4.5 V		ADCA0Im		±1.5	LSB
					ADCA0ImS		±2.5	LSB
AnVREF = 3.0 V to 3.6 V			ADCA0Im		±2.0	LSB		
		ADCA0ImS		±3.0	LSB			
Integral nonlinearity error*1	ILEn	12-bit mode	AnVREF = 4.5 V to 5.5 V		ADCA0Im (w/o T&H)		±2.0	LSB
					ADCA0I0-5 (w/ T&H)		±3.0	LSB
			AnVREF = 3.6 V to 4.5 V		ADCA0Im (w/o T&H)		±3.0	LSB
					ADCA0I0-5 (w/ T&H)		±4.0	LSB
			AnVREF = 3.0 V to 3.6 V		ADCA0Im (w/o T&H)		±4.0	LSB
				ADCA0I0-5 (w/ T&H)		±5.0	LSB	
		10-bit mode	AnVREF = 4.5 V to 5.5 V		ADCA0Im		±1.0	LSB
					ADCA0ImS		±2.0	LSB
			AnVREF = 3.0 V to 4.5 V		ADCA0Im		±1.5	LSB
					ADCA0ImS		±2.5	LSB
AnVREF = 3.0 V to 4.5 V			ADCA0Im		±1.0	LSB		
		ADCA0ImS		±2.0	LSB			
Differential nonlinearity error*1	DLEn	12-bit mode	AnVREF = 4.5 V to 5.5 V		ADCA0Im (w/o T&H)		±1.0	LSB
					ADCA0I0-5 (w/ T&H)		±2.0	LSB
			AnVREF = 3.6 V to 4.5 V		ADCA0Im (w/o T&H)		±3.0	LSB
					ADCA0I0-5 (w/ T&H)		±4.0	LSB
			AnVREF = 3.0 V to 3.6 V		ADCA0Im (w/o T&H)		±3.0	LSB
				ADCA0I0-5 (w/ T&H)		±4.0	LSB	
		10-bit mode	AnVREF = 4.5 V to 5.5 V		ADCA0Im		±1.0	LSB
					ADCA0ImS		±1.5	LSB
			AnVREF = 3.0 V to 4.5 V		ADCA0Im		±1.0	LSB
					ADCA0ImS		±2.0	LSB
AnVREF = 3.0 V to 4.5 V			ADCA0Im		±1.0	LSB		
		ADCA0ImS		±2.0	LSB			

(3/3)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Zero scale error* ¹ (offset error)	ZSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCA0Im (w/o T&H)		±3.5	LSB
				ADCA0I0-5 (w/ T&H)		±5.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCA0Im (w/o T&H)		±5.5	LSB
				ADCA0I0-5 (w/ T&H)		±7.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCA0Im (w/o T&H)		±7.5	LSB
				ADCA0I0-5 (w/ T&H)		±9.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCA0Im		±0.5	LSB
				ADCA0ImS		±1.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCA0Im		±1.0	LSB
				ADCA0ImS		±2.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCA0Im		±1.5	LSB
				ADCA0ImS		±2.5	LSB
Full scale error* ¹	FSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCA0Im (w/o T&H)		±3.5	LSB
				ADCA0I0-5 (w/ T&H)		±5.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCA0Im (w/o T&H)		±5.5	LSB
				ADCA0I0-5 (w/ T&H)		±7.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCA0Im (w/o T&H)		±7.5	LSB
				ADCA0I0-5 (w/ T&H)		±9.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCA0Im		±0.5	LSB
				ADCA0ImS		±1.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCA0Im		±1.0	LSB
				ADCA0ImS		±2.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCA0Im		±1.5	LSB
				ADCA0ImS		±2.5	LSB

Note 1. This does not include quantization error.

Note 2. $3 + 1.3 \times$ (the number of used T&H)

Note 3. Include the oscillation accuracy of HS IntOSC.

Note 4. When the external multiplexer is used, the detail time of A/D conversion is MPX setup time, sampling time and successive approximation time. MPX setup time is same as "sampling time + successive approximation time".

Note 5. Conversion accuracy when ADCA0ImS terminal is converted in 12-bit mode: Conversion accuracy can be applied if lower 2-bit is ignored from conversion result.

CAUTION

When an external digital pulse is applied to AP0, AP1, P8, P9, P18 and P19 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse.

The same behavior may apply when the digital buffer is used as output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

1.31 Injection Currents

For the injection current, there are two type specifications. These type are depend on Package, Flash size and Product name. These relationships are shown as the following table.

Product Name	Applicable Type
Except below products	Type 1
R7F701503xAFP R7F701508xABG R7F701511xABG R7F701512xABG R7F701513xABG	Type 2

Table 1.27 Definition of Pin Group (272 pin)

Symbol	Power Supply for Pin Group	Pin for Type 1 Products	Pin for Type 2 Products
PgR	REGVCC, AWOVSS	IP0_0	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20	JP0, P0, P1, P2, P3, P20
PgB	BVCC, BVSS	P10, P11, P12, P13, P21, P22	P10, P11, P12, P13, P21, P22
PgE'	EVCC, EVSS	P8, P9	Not Available* ¹
PgB'	BVCC, BVSS	P18, P19	Not Available* ¹
PgA0	A0VREF, A0VSS	AP0	AP0
PgA1	A1VREF, A1VSS	AP1	AP1

Note 1. Do not apply an overvoltage on P8, P9, P18 and P19 pins.

Table 1.28 Definition of Pin Group (233 pin)

Symbol	Power Supply for Pin Group	Pin for Type 1 Products	Pin for Type 2 Products
PgR	REGVCC, AWOVSS	IP0_0	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20	JP0, P0, P1, P2, P3, P20
PgB	BVCC, BVSS	P10, P11, P12, P13	P10, P11, P12, P13
PgE'	EVCC, EVSS	P8, P9	Not Available* ¹
PgB'	BVCC, BVSS	P18, P19	Not Available* ¹
PgA0	A0VREF, A0VSS	AP0	AP0
PgA1	A1VREF, A1VSS	AP1	AP1

Note 1. Do not apply an overvoltage on P8, P9, P18 and P19 pins.

Table 1.29 Definition of Pin Group (176 pin)

Symbol	Power Supply for Pin Group	Pin for Type 1 Products	Pin for Type 2 Products
PgR	REGVCC, AWOVSS	IP0_0	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P20	JP0, P0, P1, P2, P20
PgB	BVCC, BVSS	P10, P11, P12	P10, P11, P12
PgE'	EVCC, EVSS	P8, P9	Not Available* ¹
PgB'	BVCC, BVSS	P18	Not Available* ¹
PgA0	A0VREF, A0VSS	AP0	AP0
PgA1	A1VREF, A1VSS	AP1	AP1

Note 1. Do not apply an overvoltage on P8, P9 and P18 pins.

1.31.1 Absolute Maximum Ratings

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit		
Positive overload current VIN > VCC	I _{INJPM}	PGE	Per pin		10	mA		
			total		60	mA		
		PGB	Per pin		10	mA		
			total		60	mA		
		PGE'	Per pin		10	mA		
			Total		60	mA		
		PGB'	Per pin		10	mA		
			total		60	mA		
		PGA0	Per pin		10	mA		
			total		60	mA		
		PGA1	Per pin		10	mA		
			total		60	mA		
		PGR	Per pin		10	mA		
		Negative overload current VIN < VSS	I _{INJNM}	PGE	Per pin		-10	mA
					total		-60	mA
PGB	Per pin				-10	mA		
	total				-60	mA		
PGE'	Per pin				-10	mA		
	Total				-60	mA		
PGB'	Per pin				-10	mA		
	total				-60	mA		
PGA0	Per pin				-10	mA		
	total				-60	mA		
PGA1	Per pin				-10	mA		
	total				-60	mA		
PGR	Per pin				-10	mA		

CAUTIONS

1. The DC injection current (total) must satisfy the specifications of the injection current per pin.
2. In case of injected current for PGE and PGB, TESH0SN cannot be kept. Its deviating value will increase sharply with increasing absolute value of injection current.

1.31.2 DC Characteristics for Overload Current

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I _{INJP}	PgE	Per pin		2	mA
			Total		50	mA
		PgB	Per pin		2	mA
			Total		50	mA
		PgE'	Per pin		3	mA
			Total		20	mA
		PgB'	Per pin		3	mA
			total		20	mA
		PgA0	Per pin		3	mA
			Total		20	mA
		PgA1	Per pin		3	mA
			Total		20	mA
		PgR	Per pin		2	mA
		Negative overload current VIN < VSS	I _{INJN}	PgE	Per pin	
Total					-50	mA
PgB	Per pin				-2	mA
	Total				-50	mA
PgE'	Per pin				-3	mA
	Total				-20	mA
PgB'	Per pin				-3	mA
	total				-20	mA
PgA0	Per pin				-3	mA
	Total				-20	mA
PgA1	Per pin				-3	mA
	Total				-20	mA
PgR	Per pin				-2	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

1.31.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Leakage current coupling factor for positive overload current	K_{INJP}	PgE	Per pin			3.0×10^{-6}	—
		PgB	Per pin			3.0×10^{-6}	—
		PgE'	Per pin			3.0×10^{-6}	—
		PgB'	Per pin			3.0×10^{-6}	—
		PgA0	Per pin			4.8×10^{-6}	—
		PgA1	Per pin			4.8×10^{-6}	—
		PgR	Per pin			3.0×10^{-6}	—
Leakage current coupling factor for negative overload current	K_{INJN}	PgE	Per pin			7.5×10^{-6}	—
		PgB	Per pin			7.5×10^{-6}	—
		PgE'	Per pin			7.5×10^{-6}	—
		PgB'	Per pin			7.5×10^{-6}	—
		PgA0	Per pin			2.6×10^{-6}	—
		PgA1	Per pin			2.6×10^{-6}	—
		PgR	Per pin			7.5×10^{-6}	—

NOTES

1. This is reference value.
2. An overload current through a pin will cause a certain error current in the adjacent pins. This error current must be added to the respective leakage current (ILIH or ILIL) of the adjacent pins.
3. The amount of error leakage current depends on the overload current and is defined by the overload coupling factor K_{INJ} .
The total current through a pin is:
 $|I_{total}| = |ILIH \text{ or } ILIL| + (|I_{INJn}| \times K_{INJn})$

1.31.4 AD Characteristics for Pins Influenced by Injected Current on an Adjacent

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Degradation of overall error*1	I_{INJP}	Par = 3 mA	ADCAnIm		±1.3	LSB
			ADCAnImS		±1.3	LSB
		Total = 20 mA	ADCAnIm		±3.8	LSB
			ADCAnImS		±3.8	LSB
	I_{INJN}	Par = 3 mA	ADCAnIm		±1.4	LSB
			ADCAnImS		±1.4	LSB
		Total = 20 mA	ADCAnIm		±4.5	LSB
			ADCAnImS		±4.5	LSB

Note 1. This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Note 2. This is reference value.

CAUTION

When there is an increased leakage current on the analog input pins, based on currents injected into the pins adjacent to the converted channel, the effect on the ADC accuracy depends on the external analog source impedance.

[Example] Conditions: A0VREF = 5.0 V, external analog source impedance = 10 kΩ.

If there is a leakage current of 1 μA by injected current, the effect on the ADC accuracy is $1 (\mu\text{A}) \times 10 \text{ k} (\Omega) / 5 (\text{V}) = 0.2\% \text{FSR}$

1.32 Thermal Characteristics

1.32.1 Parameters

Package	Item	Symbol	Estimate	Unit	Note
272 pin FPBGA	Thermal Resistance	Θ_{ja}	19	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψ_{jb}	14		
233 pin FPBGA	Thermal Resistance	Θ_{ja}	20	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψ_{jb}	15		
176 pin LQFP	Thermal Resistance	Θ_{ja}	31	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψ_{jb}	24		

Note: The thermal resistance depend on the usage environment.

1.32.2 Assumed Board

Conforming to JESD51-7 (4 layers)

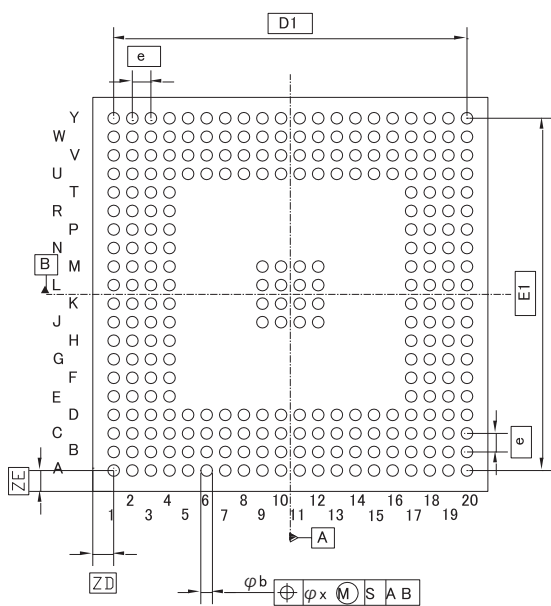
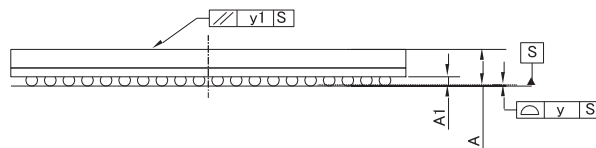
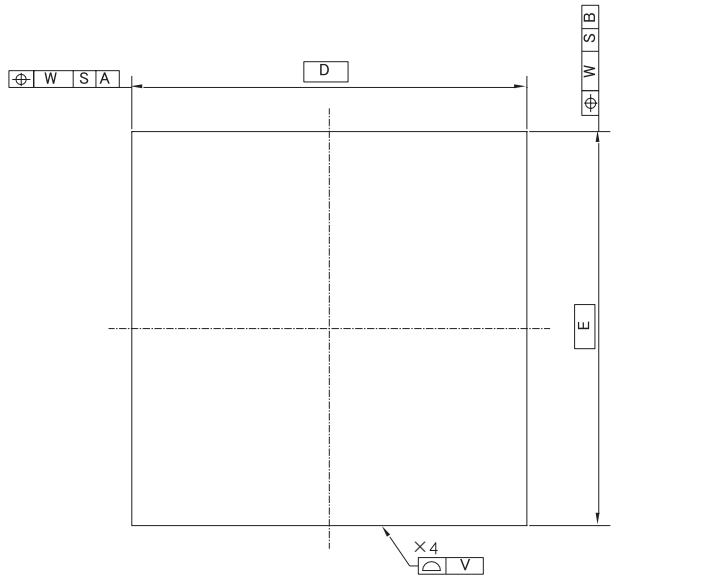
	Board size (mm)		Area (mm ²)
	X	Y	
Boad	76.2	114.3	8709.66
Remaining copper raes	Thickness of conductors		
50-95-95-50%	70-35-35-70 μ m		

Section 2 Package Dimensions

2.1 272 pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA272-17x17-0.80	PRBG0272GB-A	-	0.90

Unit:mm

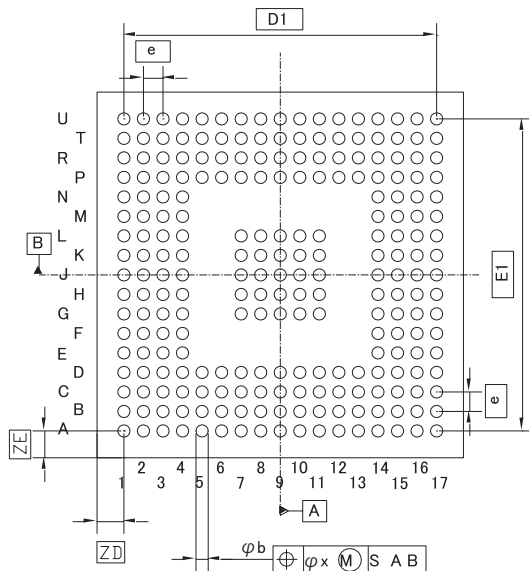
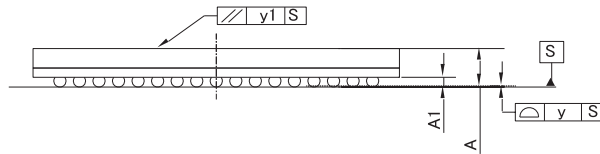
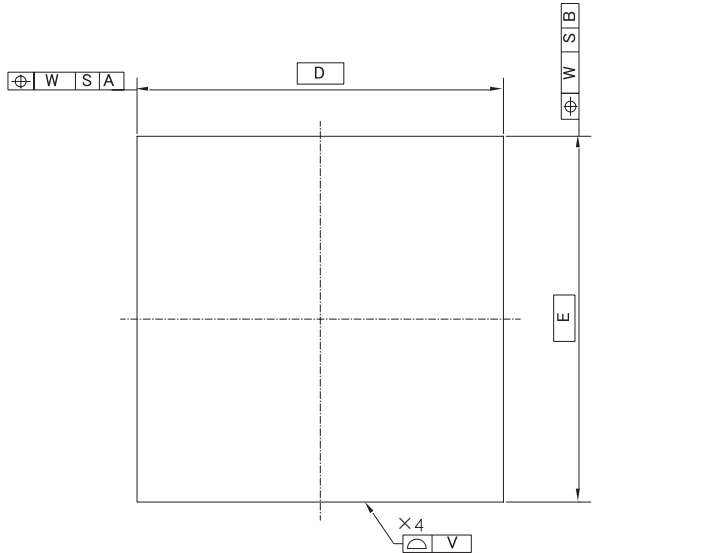


Reference Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	17.00	—
D1	—	15.20	—
E	—	17.00	—
E1	—	15.2	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	2.00
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	0.90	—
ZE	—	0.90	—

2.2 233 pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA233-15x15-0.80	PRBG0233GA-A	-	0.75

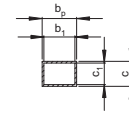
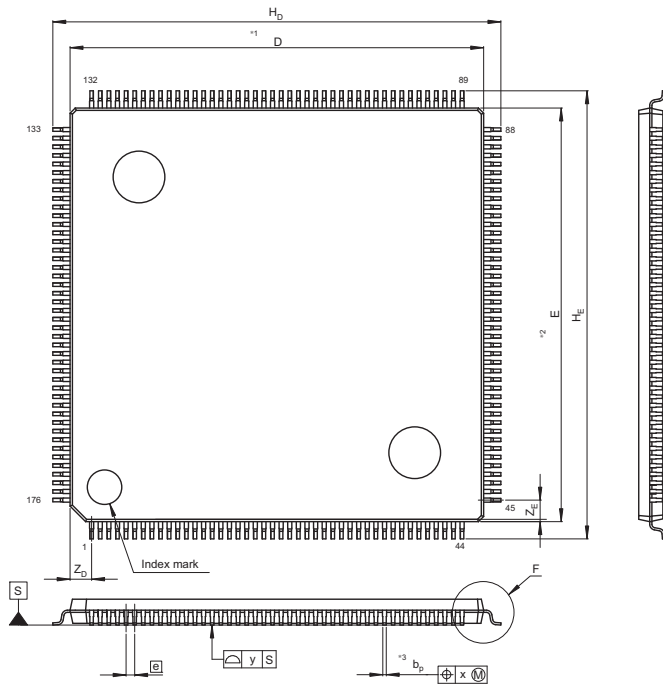
Unit:mm



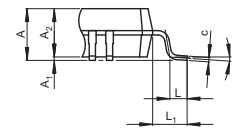
Reference Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	15.00	—
$D1$	—	12.80	—
E	—	15.00	—
$E1$	—	12.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	1.90
$A1$	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
$y1$	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

2.3 176 pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g



Terminal cross section



Detail F

NOTE)
 1. DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A ₂	—	1.4	—
H _D	25.8	26.0	26.2
H _E	25.8	26.0	26.2
A	—	—	1.7
A ₁	0.05	0.1	0.15
b _p	0.15	0.20	0.25
b ₁	—	0.18	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
⓪	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z _D	—	1.25	—
Z _E	—	1.25	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

REVISION HISTORY	RH850/F1H Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	May 29, 2014	—	First Edition issued
0.50	Jan 29, 2015	1 to 4	Product Introduction, added
		6	1.1.1.1 272-Pin, 1.1.1.2 233-Pin and 1.1.1.3 176-Pin: Section title and description added
		7	1.1.2.1 Common Conditions: Description of operating temperature, changed
		10	1.2.3 Port Current: Note, changed
		11 to 13	1.2.3.1 272-Pin: Section title and Table 1.1 Port Current (272-Pin), added
		14, 15	1.2.3.2 233-Pin: Section title and Table 1.2 Port Current (233-Pin), added
		16, 17	1.2.3.3 176-Pin: Section title and Table title, added
		17	1.2.4 Temperature Condition, changed
		18, 19	1.4 Operational Condition: Note 4., added
		19	1.5 Oscillator Characteristics, changed
		20	Figures MainOSC and SubOSC, changed
		21	1.7.1 PLL0 (for CPU) Characteristics, changed
		22	1.7.2 PLL1 (for Peripheral) Characteristics, changed
		23	1.8.1 Regulator Characteristics, changed
		24	1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics, changed
		25	Figure <POC>, changed
		26	Figure <CVM>, added
		27	Table 1.4 In case the $\overline{\text{RESET}}$ pin is used, changed
		28	Table 1.5 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin, changed
		29	Table 1.6 In case the RESET pin is not used and fixed to high level by pull-up*1, changed
		30	1.8.4 CPU Reset Release Timing, added
		31 to 38	1.9 Pin Characteristics, changed
		39, 40	1.9.1.1 272-Pin: Section title and Table 1.9 Output Current (272-Pin), added
		41, 42	1.9.1.2 233-Pin: Section title and Table 1.10 Output Current (233-Pin), added
		43, 44	1.9.1.3 176-Pin: Section title and Table title, added
		45	1.10 Power Supply Currents, changed
		48	1.11 MEMC0CLK Timing: Figure changed
		49	1.12.1 MEMC0CLK Asynchronous, changed
		52	1.12.2 MEMC0CLK Synchronous, changed
		61	1.19 RLIN2 / RLIN3 Timing, changed
		63	1.21.2 CSIH Timing: NOTE changed
		73	1.22 RIIC Timing, changed
		75	1.24.1 MII Interface, changed
76	Table 1.19 MII Interface (Reception Interface), changed		
77	1.24.2 RMII Interface: Description and Figures changed		
78	1.24.3 Management Interface, changed		
79	1.25 ADTRG Timing, changed		
84	1.29.1 Code Flash, changed		
85, 86	Table 1.23 Programming Characteristics, changed		

Rev.	Date	Description	
		Page	Summary
0.50	Jan 29, 2015	87	1.29.2 Data Flash, changed
		87	Table 1.25 Programming Characteristics, changed
		88	1.29.3.1 Serial Programmer Setup Timing, changed
		90, 91	1.30 A/D Converter Characteristics, changed
		93	1.31 Injection Currents, changed
		94	1.31.1 Absolute Maximum Ratings, changed
		95	1.31.2 DC Characteristics for Overload Current, changed
		96	1.31.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin, changed
		97	1.31.4 AD Characteristics, changed
		98 to 100	Section 2 Package Dimensions: Section title and figures added (272-Pin and 233-Pin)
1.00	Jun 30, 2015	1	typo (master/a slave → master/slave)
		2,6,11,12,51,99	description alignment (272-pin → 272 pin)
		3,6,13,14,51,100	description alignment (233-pin → 233 pin)
		4,6,15,16,51,101	description alignment (176-pin → 176 pin)
		5	Addition of products lineup for Gateway
		6	description alignment (removed "Related pins/port" for Pg R)
		7,18,20,21,22,23,24,27,31,36,47,48,51,54,55,56,57,58,59,61,62,63,73,75,77,79,80,81,82,83,84,87,88,89,90	description alignment (AWOVCL → CAWOVCL, ISOVCL → CISOVCL)
		7	Addition of products information (R7F7015xx3ABG, R7F7015xx4ABG)
		8	description alignment (added "it is recommended" for CAUTION)
		8	description alignment (min. → MIN., max. → MAX.)
		10	Addition of "P13" for GPIO list
		11,12,13,14,15,16	Table 1.1/2/3, description alignment ("Per side")
		16	Table, Addition of products information (R7F7015xx3ABG, R7F7015xx4ABG)
		16	description alignment (renamed "Product Introduction" → "Product Lineup")
		17	typo (FLC → FLXA, OSTM → OSTMn)
		18,45	description alignment (IntOsc → IntOSC)
		18	correction of "MainOsc oscillation operation point" level (MIN:2.4 → empty, TYP:empty → 0.5xREGVCC)
		18	Addition of "MainOsc oscillation amplitude"
		18	correction of "SubOsc current consumption" (TYP:2 → 1.5, MAX.:8 → 4)
		18	correction of "SubOsc DC operating point" (MIN:2.4 → empty, TYP:empty → 0.65)
		19	Improvement of figures (MainOSC and SubOSC)
		21	typo in Note 2.(PLL0C.PLL0P2-0 bits → PLL0C.PLL0P2-0 bits)
		21	typo in Note 4.(SELMPERCEN[2:0] → PLL0ADJ[2:0])
		22	correction of symbol of Output period jitter (t _{CPJ} → t _{CPJP})
		23	addition of "Condition for AWOVCL"(empty → AWOVCL pin)
		23	addition of "Condition for ISOVCL"(empty → ISOVCL pin)
		23	correction of "Equivalent series resistance ..." (for AWO area → for CAWOVCL)
23	correction of "Equivalent series resistance ..." (for ISO area → for CISOVCL)		
23	addition of "Note 2. This is reference value".		

Rev.	Date	Description	
		Page	Summary
1.00	Jun 30, 2015	24	description alignment for "Note 5": "=0.02 V/ms to 500 V/ms" → ":0.02 V/ms ≤ T _{VS} ≤ < 500 V/ms")
		24	addition of "Caution"
		26	correction of name for REGVCC level (VLVI → VVLVI)
		27,28	correction of Power Up/Down timing (FLMD0 hold time, FLMD0 setup time)
		27,28	case separation for timing whether in serial programming mode or except serial programming mode
		27	removed "Note 2" which explained handling of FLMD0 and FLMD1
		28	Improvement of figure (timing chart)
		29	removed "FLMD0,1 hold time" spec
		29	correction of MIN value for t _{DMPD} (0 → 1)
		29	Improvement of explanation for "Note 1" (added "include self-programming mode")
		32	correction: RESET/SHMT2 : with *4 → w/o *4 RESET/Pull-down : w/o *4 → with *4
		34	P8_7 to P8_12: Pull-down : tick and with *5 → with *1 P20_1,2: Slow → Slow/Fast P10_0 to P10_15, P11_0 to P11_4:
		34,35	Updated for "Port input Buffer Function" and "Port Output Drive Strength Modes" part
		35	addition in case of "Slow" condition
		36	addition of "Caution"
		37	correction, Condition of VIH for TTL changed (EVCC → IOVCC)
		37	description alignment of condition for Rise/Fall time ("P18_1-6" → "P18_1 to P18_6")
		45	correction: 1. RUN mode current (Symbol : IDDR → IDDR1) (Condition : "Run (80MHz)" → "Run (120MHz)") (MAX. : "170" → "144") 2. RUN mode current (During data/code flash programming) (Condition : "Run (80MHz)" → "Run (120MHz)") (MAX. : "187" → "161")
		46	description alignment (HS-IntOSC → HS IntOSC)
		49,50,52,53	description alignment: (out → output) (in → input)
		54,59,79,80	addition for Note 2 (page 54,79,80), Note 4 (page 59), "Noise such as the figure can be filtered"
		54	description alignment (High Speed Internal Oscillator → HS IntOSC)
		55,56	description alignment with another F1x products (timing is not changed)
		57	description alignment with another F1x products. separation for high level width and low level width. Addition Note 2 and Note 3.
		58	correction of Note 2. removed Note 3
		60	addition of t _{WENTIH} , t _{WENTIL}
		61	changed CSIGNRYO output delay spec
		63	correction of register name which is used as "Condition" CSIHnCTL1.CSIHnDAP → CSIHnCFGx.CSIHnDAP
		63	description alignment of bit number ("CSIHnCFG0-7.CSIHnID2-0" → "CSIHnCFGx.CSIHnID[2:0]") ("CSIHnCFG0-7.CSIHnSP3-0" → "CSIHnCFGx.CSIHnSPx[3:0]") ("CSIHnCFG0-7.CSIHnHD3-0" → "CSIHnCFGx.CSIHnHDx[3:0]")
		63	correction of register name which is used as "Condition" CSIHnCFG7-0.CSIHnCKP0-7 → CSIHnCFGx.CSIHnCKPx
64	changed CSIHnRYO output delay spec		

Rev.	Date	Description			
		Page	Summary		
1.00	Jun 30, 2015	73	removed "0" as MIN. of RIIC0SCL clock period (Normal Mode) removed "0" as MIN. of RIIC0SCL clock period (Fast Mode)		
		74	description alognment (subindex:STA, DAT, STO)		
		75	removed "CL = 15 pF (100Mbps interface only)"		
		76	changed spec : t_{RDVH} : 20 → 10 t_{EDRH} : 20 → 10 t_{RERH} : 20 → 10		
		84,87	addition "Note 4. Only for program/erase operation."		
		85	changed spec : ($f_{PCLK} \geq 20\text{MHz}$, $CWRT \geq 100$ times) 3MB (TYP.) : 8 → 8.1 4MB (TYP.) : 11 → 10.8 6MB (TYP.) : 16 → 16.2		
		86	changed spec : ($f_{PCLK} \geq 20\text{MHz}$, $CWRT < 100$ times) 384KB (MAX.) : 0 → 5.3 3MB (TYP.) : 14 → 13.6 4MB (TYP.) : 18 → 18.1		
		87	addition of Note 4 for f_{PCLK} (MIN.) value		
		88	improvement of time chart		
		90	description alignment : ($TCONn \rightarrow t_{CONn}$) ($TSHSMP \rightarrow t_{THSMP}$) ($TSHHOLD \rightarrow t_{THHOLD}$) ($TBOOT \rightarrow t_{BOOT}$) ($TOUT \rightarrow t_{OUT}$)		
		91	description alignment : (LSB → -)		
		92	addition "Note 5", CAUTIONS sentence 2		
		93	correction of Product Name list		
		93	correction : PgB : P19 added (Table 1.27) PgB : P19 added (Table 1.28)		
		93	addition "Note 1"		
		98	addition "1.32 Thermal Characteristics"		
		99	updated the package information ("PRBG0272GA-A" → "PRBG0272GB-A")		
		1.11	May 23, 2016	5	addition of discription to PREMIUM products
				18	addition spec: " V_{MOSCSP} " changed spec : $1^3 \rightarrow 0.4 \times \text{REGVCC} - 0.2^3$
				19	changed figure: MainOSC: Addition (V_{MOSCSP}) SubOSC: correction($MOSCST \rightarrow SOSCST$)
24	addition of Note 8 for Detection voltage				
27	removed FLMD0 setup time				
27	addition of Note 2 for figure				
62	addition "RS-CANFD (CAN-FD Mode) Timing (only PREMIUM product)"				
93	correction of CAUTION				
23	correction of 1.8.1 Regulator Characteristics addition of Note 3				
58	correction of note2 to 1.17 Mode Timing				

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