Product Introduction

Concept

The RH850/F1x microcontroller focus on low power and low cost for the body application.

The device is a high-end microcontroller with a 32-bit RH850G3K core for car body control. The features of this device are the low power consumption, the high processing power and the variable peripheral function.

In particular, Low power consumption is achieved by supporting wide stand-by control and the power supply insulation using the port polling, stand-by control of AD conversion and LIN communication which considered body control application.

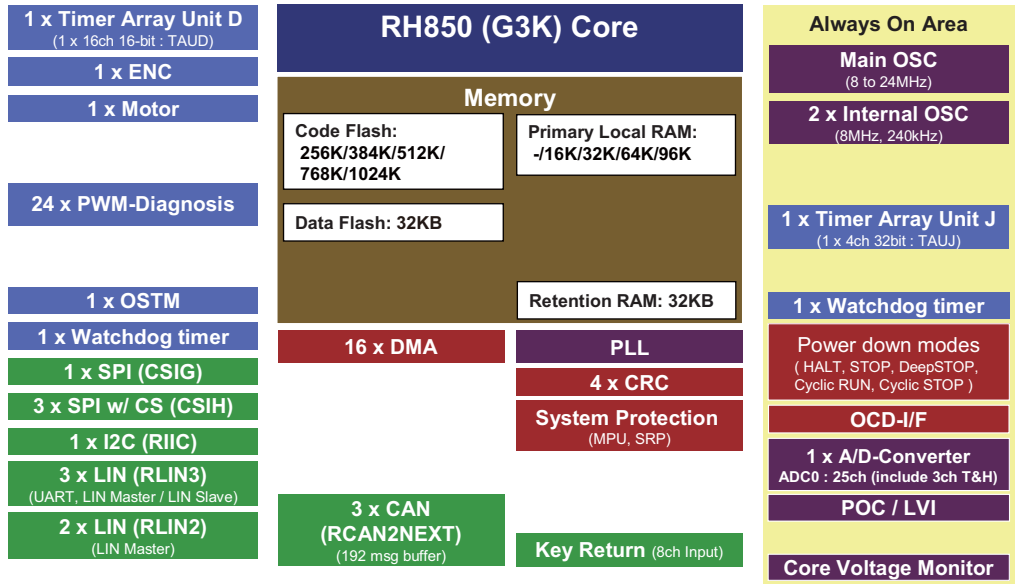
This device supports the security and safety function. And the local area network has been strengthened by upgrading each module of CAN, LIN master/slave.

Function Overview

- 32bit single core CPU (V850E3v5-S architecture class)
- The capacity of Code Flash: up to 1 MB
- The capacity of Data Flash: 32 KB
- The capacity of RAM: up to 128 KB
- DMA function
- System protection
- POC/LVI, CVM
- MainOSC which is available for a wide range frequency (8 MHz to 24 MHz)
- External interrupt: 12
- Low Power Sampler watching an outside event in standby mode
- Timer Array Unit D: 1 ch
- Timer Array Unit J: 1 ch
- PWM-Diagnosis function: 24 ch
- Encoder Timer: 1 ch
- Motor control: 1 ch
- OS Timer: 1 ch
- Watchdog Timer: 2 ch
- Asynchronous Serial Interface, LIN Master/Slave Controller: 3 ch
- LIN Master Controller: 2 ch
- CAN Controller: up to 3 ch
- Clocked Serial Interface G: 1 ch

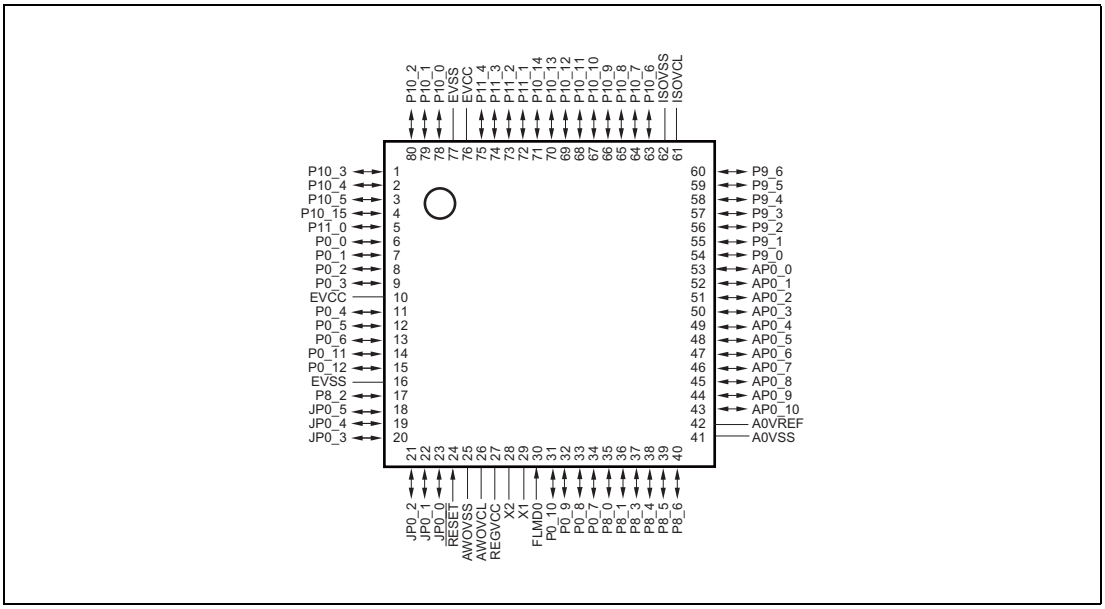
- Clocked Serial Interface H: 3 ch
- Data CRC: 4 ch
- A/D Converter: 1 ch
  - ADCA0In w/ T&H: 3 ch
  - ADCA0In w/o T&H: 8 ch
  - ADCA0InS: 14 ch
- Key Return: 8 ch

Block Diagram



Note 1. ADVANCED line support ICUSB

Pin Map


P10_2 80
P10_1 79
P10_0 78
EVSS 77
EVCC 76
P11_4 75
P11_3 74
P11_2 73
P11_1 72
P10_14 71
P10_13 70
P10_12 69
P10_11 68
P10_10 67
P10_9 66
P10_8 65
P10_7 64
P10_6 63
ISOVSS 62
ISOVCL 61
P10_3 1
P10_4 2
P10_5 3
P10_15 4
P11_0 5
P0_0 6
P0_1 7
P0_2 8
P0_3 9
EVCC 10
P0_4 11
P0_5 12
P0_6 13
P0_11 14
P0_12 15
EVSS 16
P8_2 17
JP0_5 18
JP0_4 19
JP0_3 20
60 P9_6
59 P9_5
58 P9_4
57 P9_3
56 P9_2
55 P9_1
54 P9_0
53 AP0_0
52 AP0_1
51 AP0_2
50 AP0_3
49 AP0_4
48 AP0_5
47 AP0_6
46 AP0_7
45 AP0_8
44 AP0_9
43 AP0_10
42 A0VREF
41 A0VSS
21 JP0_2
22 JP0_1
23 JP0_0
24 RESET
25 AWOVSS
26 AWOVCL
27 REGVCC
28 X2
29 X1
30 FLMD0
31 P0_10
32 P0_9
33 P0_8
34 P0_7
35 P8_0
36 P8_1
37 P8_3
38 P8_4
39 P8_5
40 P8_6

Product Lineup

Product	Max CPU Frequency	ICUSB	Code Flash	Data Flash	Local RAM (Primary)	Local RAM (Secondary)	Retention RAM (RRAM)	Operationing Temperature (Ta)	
								–40°C to +105°C[Caution]	–40°C to +125°C[Caution]
ECO	80 MHz	No	256 KB	32 KB	0 KB	0 KB	32 KB	R7F7010163AFP	R7F7010164AFP
			384 KB		16 KB			R7F7010173AFP	R7F7010174AFP
			512 KB		32 KB			R7F7010183AFP	R7F7010184AFP
			768 KB		64 KB			R7F7010193AFP	R7F7010194AFP
			1 MB		96 KB			R7F7010203AFP	R7F7010204AFP
ADVANCED	96 MHz	Yes	768 KB		64 KB			R7F7010423AFP	R7F7010424AFP
			1 MB		96 KB			R7F7010433AFP	R7F7010434AFP

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj (**Section 1.2.4, Temperature Condition**) and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Section 1 Electrical Specifications

1.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

1.1.1 Pin Groups

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10, P11 Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

1.1.2 General Measurement Conditions

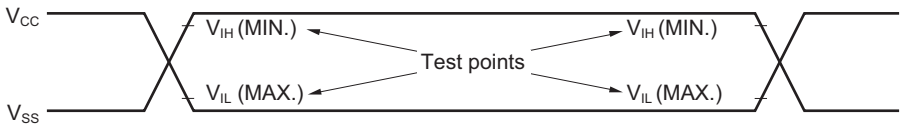
1.1.2.1 Common Conditions

- Power supply
  - REGVCC = EVCC = VPOC*1 to 5.5 V
  - A0VREF = 3.0 V to 5.5 V
  - AWOVSS = ISOVSS = EVSS = A0VSS = 0 V
- Capacitance of the internal regulator
  - CAWOVCL: 0.1 µF +/– 30%
  - CISOVCL: 0.1 µF +/– 30%
- Operating temperature
  - Ta:
    –40 to (depend on the product)°C
  - Tj:
    R7F7010xx3AFP : –40 to 130°C
    R7F7010xx4AFP : –40 to 150°C
- Load conditions
  - CL = 30 pF

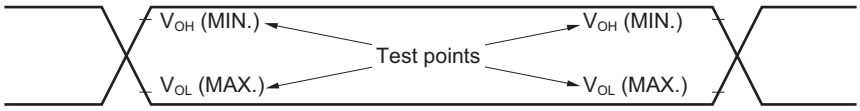
Note 1. “VPOC” means POC (power on clear) detection voltage. For more detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

1.1.2.2 AC Characteristic Measurement Condition

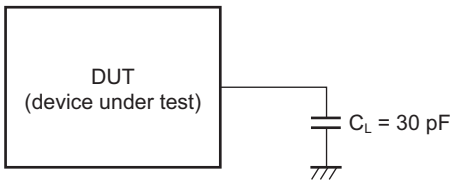
(1) AC test input measurement points



(2) AC test output measurement points



(3) Load conditions



CAUTION

If the load capacitance exceeds 30pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance till less than 30pF.

1.2 Absolute Maximum Ratings

CAUTIONS

1. **Do not directly connect outputs (or input/outputs) to each other, power supply and ground.**
2. **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
3. **When designing an external circuit ensure that the connections don't conflict with the port state of this device.**

1.2.1 Supply Voltages

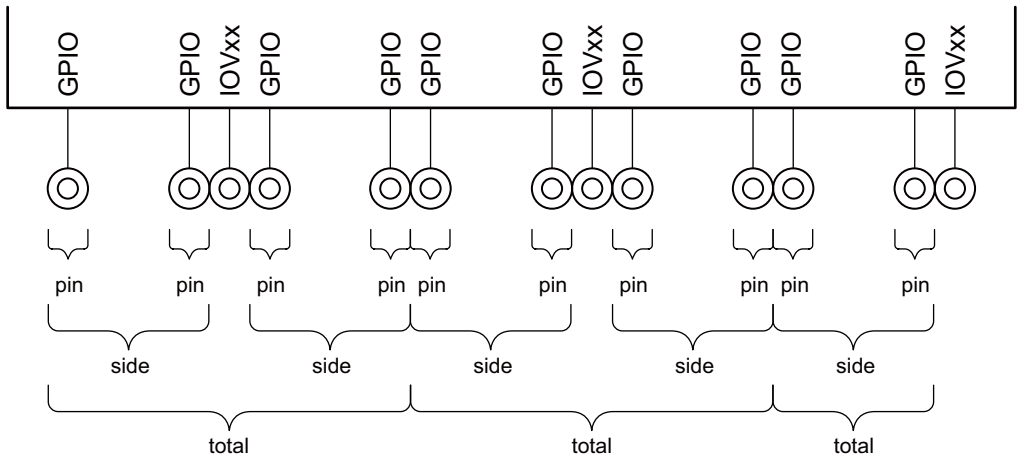
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V

1.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR	VI		-0.5		REGVCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.2.3 Port Current



Definition of the condition:

- **Per pin:** Output current of one GPIO
- **Per side:** Total output current of all GPIO pins on one side of one IOVxx
- **Total:** Total output current of both sides of one IOVxx

Note:

- **GPIO:** General-purpose I/O pin (JP0, P0, P8, P9, P10, P11, AP0)
- **IOVxx:** Power supply pin for I/O pins (EVCC/EVSS, A0VREF/A0VSS)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0)			–48	mA
			Per side (Total of JP0_0 to JP0_5, P0_4 to P0_12, P8_0 to P8_6)			–48	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Per side (Total of P0_0 to P0_6, P0_11, P0_12, P10_3 to P10_5, P10_15, P11_0)			48	mA
			Per side (Total of JP0_0 to JP0_5, P0_7 to P0_10, P8_0 to P8_6)			48	mA
			Total (EVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

1.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		170	°C
Junction temperature	Tj	R7F7010xx3AFP	–40		130	°C
		R7F7010xx4AFP	–40		150	°C

xx = 16, 17, 18, 19, 20, 42, 43

Regarding operation temperature of each product, refer to "**Product Lineup**".

1.3 Capacitance

Condition: REGVCC = EVCC = A0VREF = AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz 0 V for non measurement pins			10	pF
Input/output capacitance	CIO*2				10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

1.4 Operational Condition

ECO Line

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK}				80	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for CSCXFOUT			24	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for ENCA0				
		for TAPA				
		for PIC				
	f_{CKSCLK_IPERI2}	for PWM-diag			40	MHz
	f_{CKSCLK_ILIN}	for RLIN2			40	MHz
		for RLIN3				
	f_{CKSCLK_ICAN}	for RS-CAN (pclk)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RS-CAN (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIG			80	MHz
		for CSIH				
	f_{RL}	for WDTA1			240*2	kHz
	$f_{CPUCLK2}$	for OSTM			40	MHz
		for RIIC				
	f_{EMCLK}	for LPS			8	MHz
Power supply	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	A0VREF		3.0		5.5	V

Note 1. For clock specification of peripherals, refer to *Section 10, Clock Controller*, in *the RH850/F1L Group User's Manual: Hardware*.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on). For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

ADVANCED Line

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK}				96	MHz
Peripheral clock (clock domain) frequency*1	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for CSCXFOUT			24	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for ENCA0				
		for TAPA				
		for PIC				
	f_{CKSCLK_IPERI2}	for PWM-diag			48	MHz
	f_{CKSCLK_ILIN}	for RLIN2			48	MHz
		for RLIN3				
	f_{CKSCLK_ICAN}	for RS-CAN (pclk)			96	MHz
	$f_{CKSCLK\_ICANOSC}$	for RS-CAN (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIG			96	MHz
		for CSIH				
	f_{RL}	for WDTA1			240*2	kHz
	$f_{CPUCLK2}$	for OSTM			48	MHz
		for RIIC				
	f_{EMCLK}	for LPS			8	MHz
Power supply	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	A0VREF		3.0		5.5	V

Note 1. For clock specification of peripherals, refer to *Section 10, Clock Controller*, in *the RH850/F1L Group User's Manual: Hardware*.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on). For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.
In addition, the guaranteed operation in DC characteristic.
And AC characteristic is guaranteed when more than 3.0 V.
When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

1.5 Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC}	Crystal/Ceramic	8		24	MHz
MainOSC Current consumption	I_{MOSC}	After stabilization		1.9*2	2.3*2	mA
MainOSC oscillation start point	V_{MOSCSP}	Crystal/Ceramic	VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}			0.5 x REGVCC*2		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$	Crystal/Ceramic	0.4 x REGVCC–0.2*2			V
MainOSC oscillation stabilization time	t_{MSTB}			*1		ms

Note 1. Oscillator stabilization time is time until being set (“1”) in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written “1”, and depends on the setting value of MOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

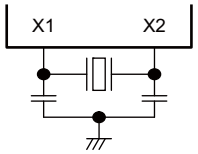
Note 2. This is reference value.

CAUTION

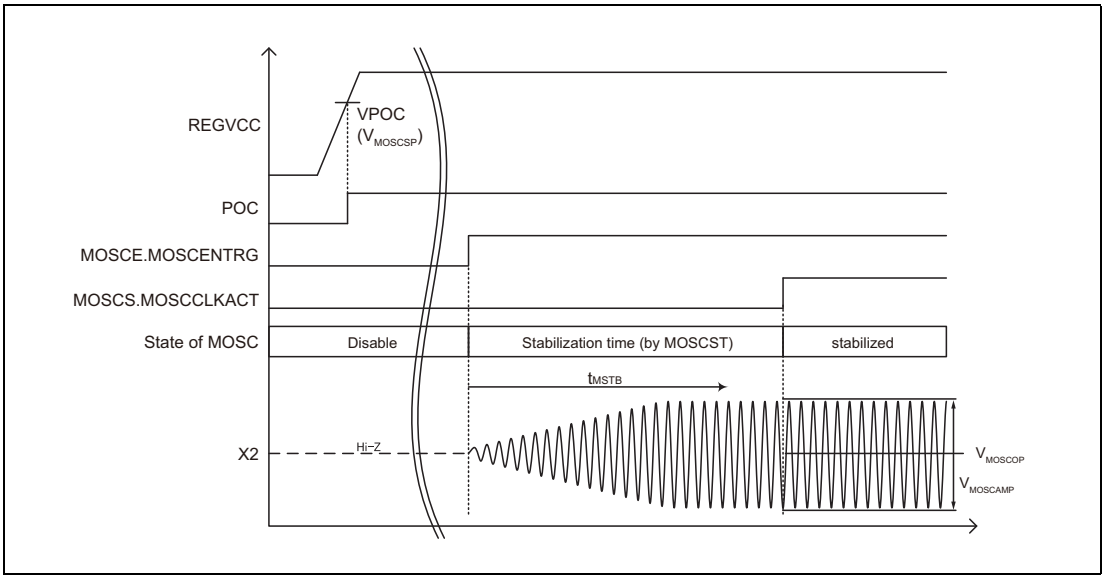
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

Recommended oscillator circuit is shown below.



MainOSC



1.6 Internal Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency	f_{RH}		7.36	8	8.64	MHz
		Ta = 25°C	7.6	8	8.4	MHz
HS IntOSC Current consumption	I_{RH}	After stabilization			25*1	µA
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	µs

Note 1. This is reference value.

1.7 PLL Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol		Condition	MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLLICLK}$			8		24	MHz
Output frequency (PLL for CPU)	f_{CPLL}		ECO line	25		80	MHz
			ADVANCED line,	25		96	MHz
Output frequency (PLL for Peripheral)	f_{PPLL}			25		80	MHz
Output period jitter*1 (PLL for CPU)	t_{CPJ}	PLLC.OUTBSEL = 0	par = 4*2	–150		150	ps
			par = 6*2 (f_{CPLL} = 80 MHz)	–150		150	ps
			par = 6*2 (f_{CPLL} < 80 MHz)	–200		200	ps
			par = 8*2	–250		250	ps
			par = 16*2	–300		300	ps
		PLLC.OUTBSEL = 1 ADVANCED line	f_{CPLL} = 96 MHz	–150		150	ps
			f_{CPLL} < 96 MHz	–200		200	ps
Output period jitter*1 (PLL for Peripheral)	t_{PPJ}		par = 4*2	–150		150	ps
			par = 6*2 (f_{PPLL} = 80 MHz)	–150		150	ps
			par = 6*2 (f_{PPLL} < 80 MHz)	–200		200	ps
			par = 8*2	–250		250	ps
			par = 16*2	–300		300	ps
Long term jitter*1 (Both PLL for CPU and PLL for Peripheral)	t_{LTJ}		term = 1 µs	–500		500	ps
			term = 10 µs	–1		1	ns
			term = 20 µs	–2		2	ns
Lock time*3	t_{LCKP}			104	112.3	122.1	µs

Note 1. This is reference value.
Note 2. “par” is set by PA[2:0] bit of PLLC register.
Note 3. Lock time is time until being set (“1”) in PLLS.PLLCLKACT bit after PLLE.PLLENTRG bit is written “1”.

1.8 Power Management Characteristics

1.8.1 Regulator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		5.5	V
Normal operation voltage	V_{OP}	AWOVCL pin, ISOVCL pin	1.10	1.25	1.35	V
Limited operation voltage	V_{LOP}	AWOVCL pin, ISOVCL pin	1.35		1.43*3	V
Regulator output voltage	V_{RO}	AWOVCL pin, ISOVCL pin	1.15	1.25	1.35	V
Output voltage	AWOVCL	AWOVCL pin	1.1	1.25	1.35	V
	ISOVCL	ISOVCL pin	1.1	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.10	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.10	0.13	µF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40*2	mΩ
	RVRISO	for CISOVCL			40*2	mΩ
Inrush current during power-on					100*2	mA

Note 1. “VPOC” means POC (power on clear) detection voltage (typ. 2.95V@at power-on, typ. 2.9V@after (except) power-on).
For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

Note 2. This is reference value.

Note 3. Reliability restrictions from 1.35 V to 1.43 V.

1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

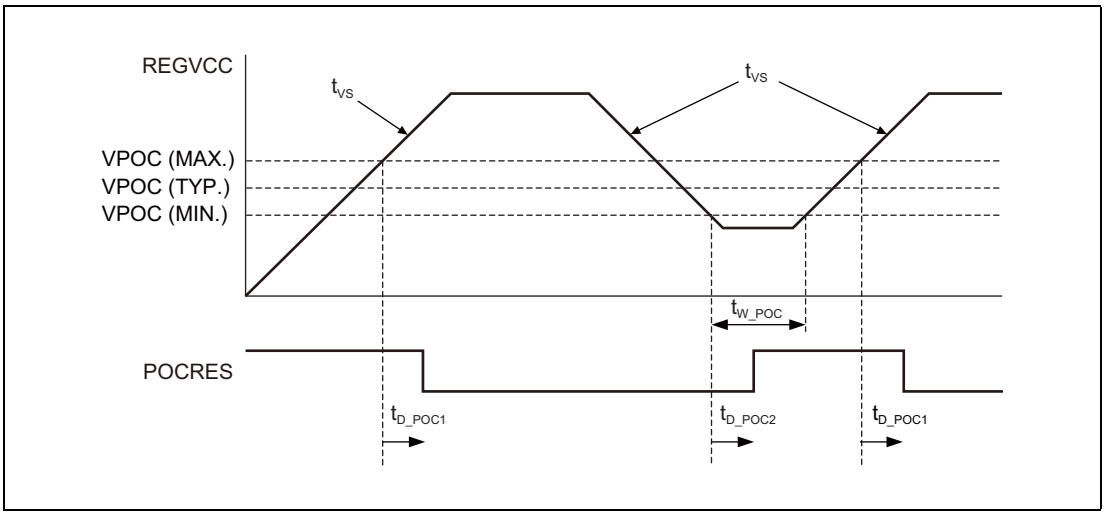
Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Detection voltage (REGVCC)	VPOC	POC	At power-on (Rise)		2.8	2.95	3.1	V
			After power-on (Fall)		2.8	2.9	3.0	V
	VLVI0	LVI	Rise		3.87	4.0	4.13	V
			Fall		3.9	4.0	4.1	V
	VLVI1		Rise		3.57	3.7	3.83	V
			Fall		3.6	3.7	3.8	V
	VLVI2		Rise		3.37	3.5	3.63	V
			Fall		3.4	3.5	3.6	V
	VVLVI	VLVI			1.8	1.9	2.0	V
Detection voltage (AWOVCL, ISOVCL)	VCVMH	CVM	High voltage**Caution**		1.40	1.50	1.60	V
	VCVML*8		Low voltage**Caution**		1.1	1.15	1.20	V
Response time	t_{D_POC1}*6	POC	At power-on (Rise)	*1			2	ms
				*2			6.3	ms
			After power-on (Rise)	*3			2	ms
				*4			5	ms
	t_{D_POC2}*7		After power-on (Fall)	*5			5	µs
	t_{D_LVI}	LVI					2	ms
	t_{D_VLVI}	VLVI		*3			2	ms
				*4			5	ms
	t_{D_CVM}	CVM			0.2		10	µs
Setup time	t_{S_LVI}	LVI	LVICNT0,1 bits are set to 1 (except 00_B), then LVI is ready to operate				80	µs
REGVCC minimum width	t_{W_POC}	POC			0.2			ms
	t_{W_LVI}	LVI			0.2			ms
	t_{W_VLVI}	VLVI			0.2			ms

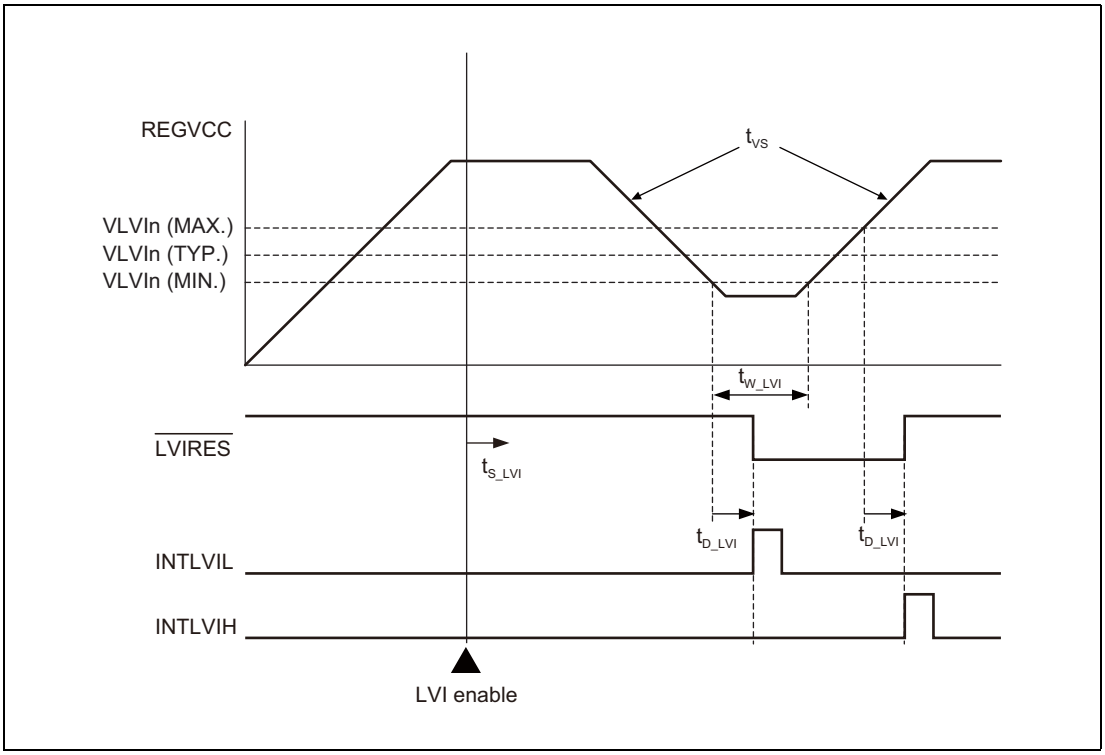
Note 1. Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms
Note 2. Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms
Note 3. Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms
Note 4. Voltage slope (t_{VS}) : 20 V/ms < t_{VS} ≤ 500 V/ms
Note 5. Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.
Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.
Note 8. The CVM monitors the internal voltage regulator output to ensure that AWOVCL/ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage AWOVCL or ISOVCL outside the specified level of VCVMH and VCVML is not ensured by CVM.

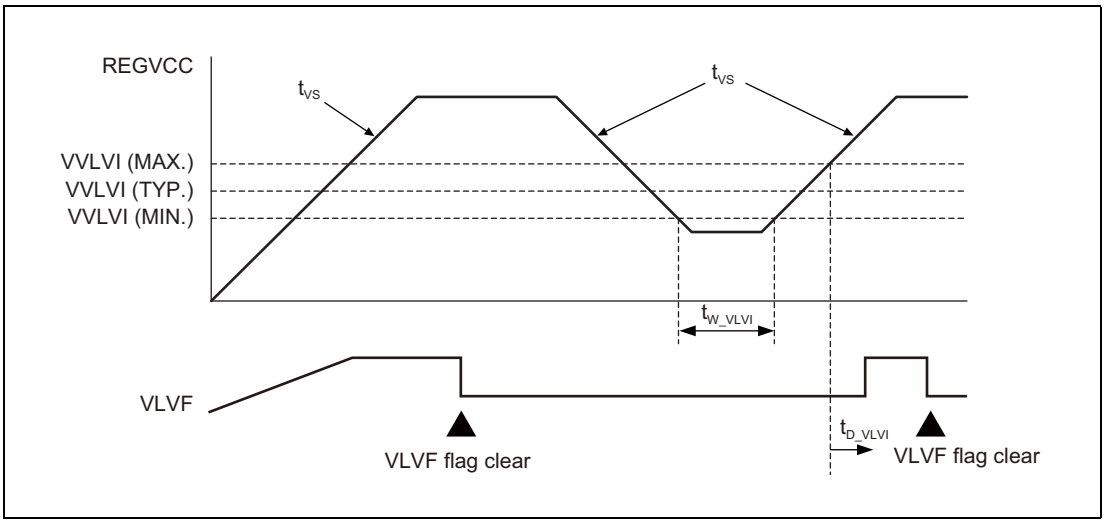
<POC>


REGVCC
VPOC (MAX.)
VPOC (TYP.)
VPOC (MIN.)
POCRES
tVS
tVS
tW_POC
tD_POC1
tD_POC2
tD_POC1

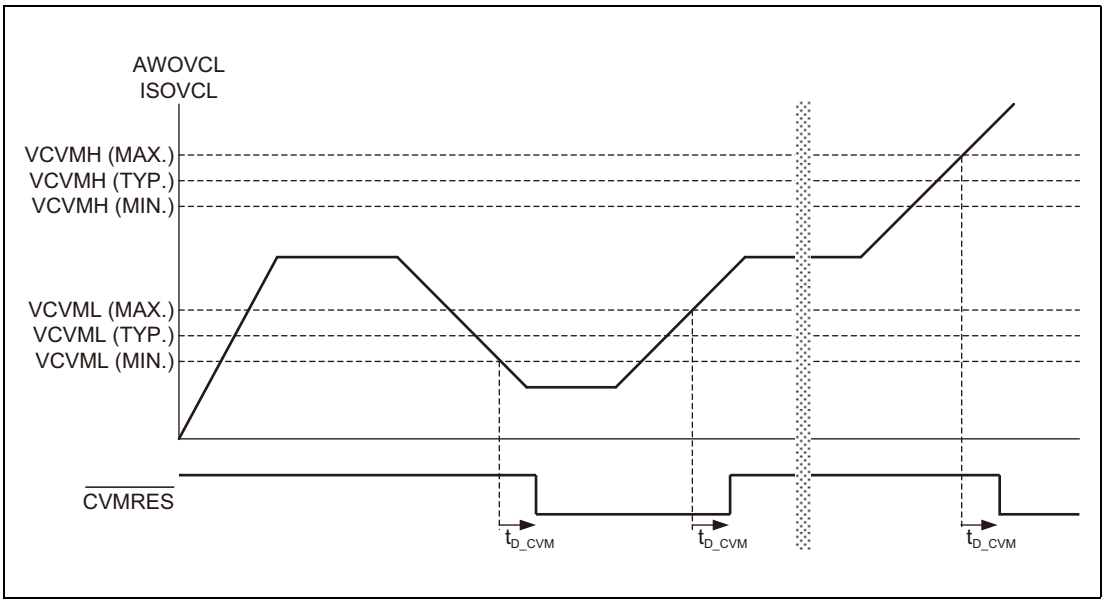
<LVI>


REGVCC
VLVIn (MAX.)
VLVIn (TYP.)
VLVIn (MIN.)
LVIRES
INTLVIL
INTLVIH
tVS
tW_LVI
tS_LVI
tD_LVI
tD_LVI
LVI enable

<VLVI>


REGVCC
t_{VS}
t_{VS}
VVLVI (MAX.)
VVLVI (TYP.)
VVLVI (MIN.)
t_{W_VLVI}
VLVF
VLVF flag clear
t_{D_VLVI}
VLVF flag clear

<CVM>

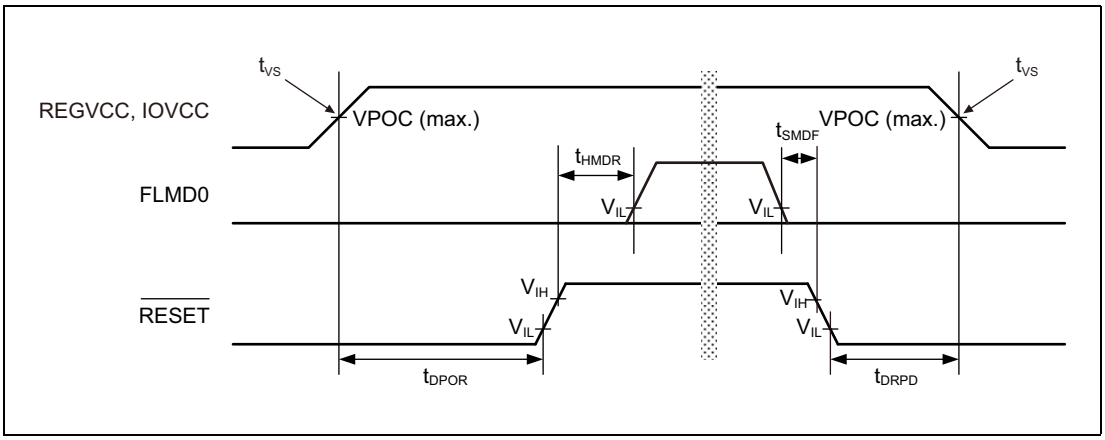

AWOVCL
ISOVCL
VCVMH (MAX.)
VCVMH (TYP.)
VCVMH (MIN.)
VCVML (MAX.)
VCVML (TYP.)
VCVML (MIN.)
CVMRES
t_{D_CVM}
t_{D_CVM}
t_{D_CVM}

1.8.3 Power Up/Down Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Table 1.1 In case the $\overline{\text{RESET}}$ pin is used (except Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↓)	t_{SMDF}		0*2			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC and A0VREF.

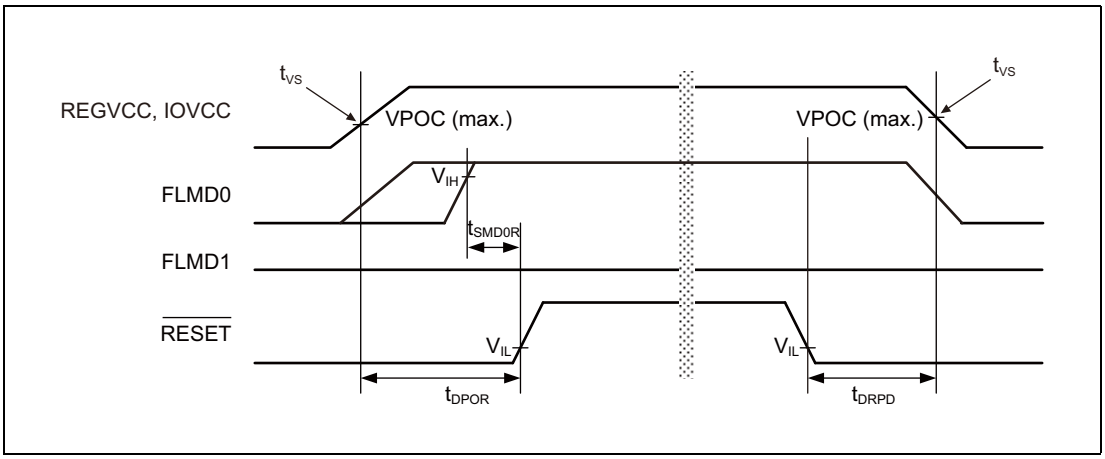
Note 2. When the $\overline{\text{RESET}}$ and FLMD0 pin input low level at same time (t_{SMDF} = 0µs) in the device entries on-chip debug mode and operates self-programming, following pins have a possibility to unstable level output for less than 23ns.

P10_0, P0_0, P10_5, P8_1

So, when the device was used in the device entries on-chip debug mode and operates self-programming, please input low level in FLMD0 before $\overline{\text{RESET}}$ pin input.

Table 1.2 In case the $\overline{\text{RESET}}$ pin is used (for Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC and A0VREF.

Table 1.3 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0, FLMD1, MODE0, MODE1 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMDR}		1			ms
$\overline{\text{RESET}}$↓ to REGCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ ↑)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ ↓)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC and A0VREF.

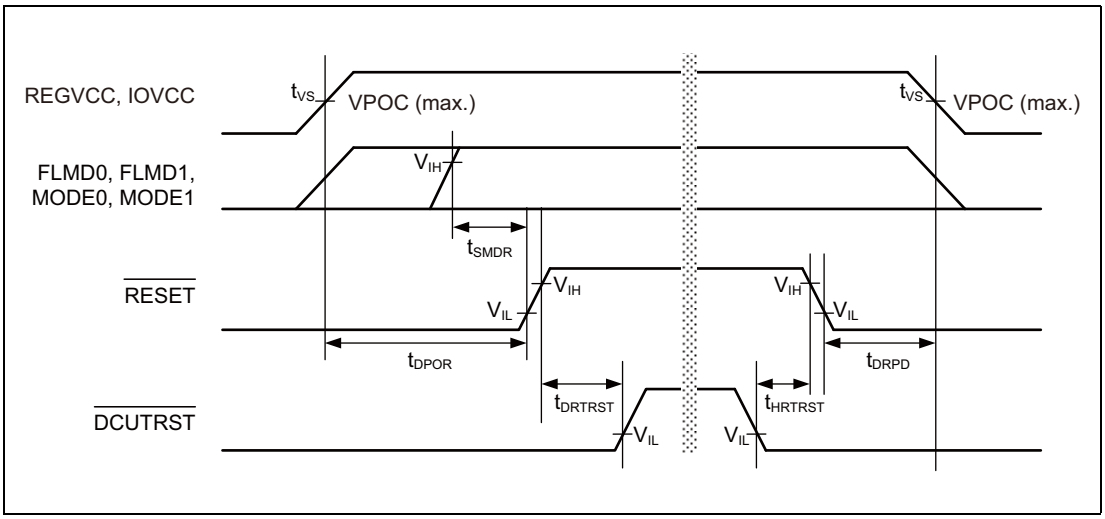
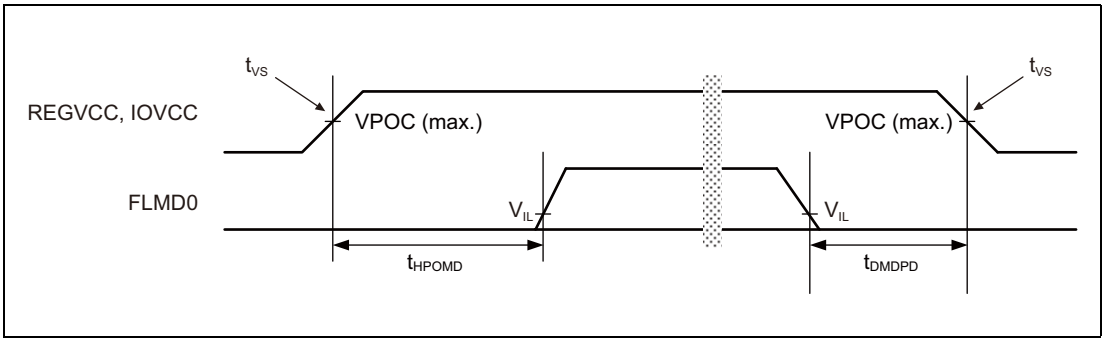


Table 1.4 In case the $\overline{\text{RESET}}$ pin is not used and fixed to high level by pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC ↑ to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 ↓ to REGVCC ↓ and IOVCC*2 ↓ delay time	t_{DMDPD}		1			µs

Note 1. This operating condition is available only in normal operation mode (include self-programming mode). When the device is used in except normal operation mode, please use the $\overline{\text{RESET}}$ pin.

Note 2. IOVCC means EVCC and A0VREF.



1.8.4 CPU Reset Release Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Table 1.5 In case the $\overline{\text{RESET}}$ pin is not used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms			2.58	ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms			8.30	ms

Note 1. This is reference value.

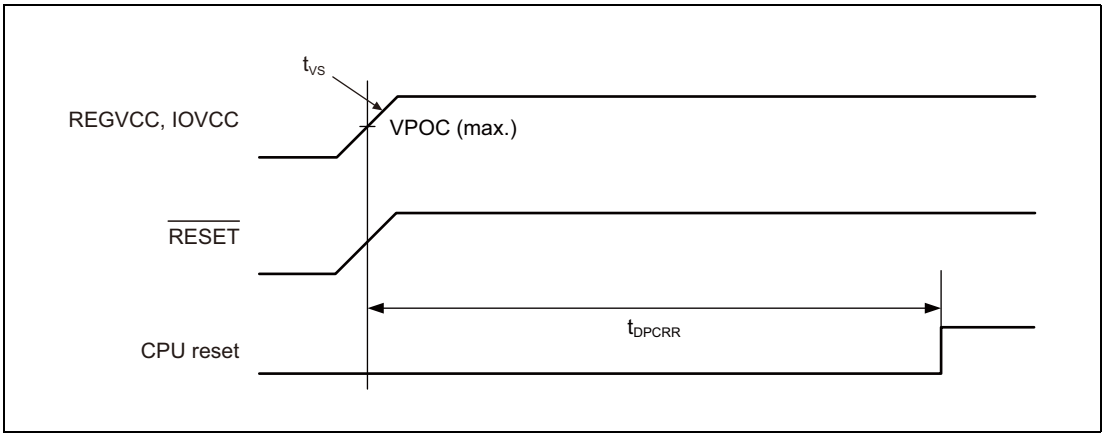
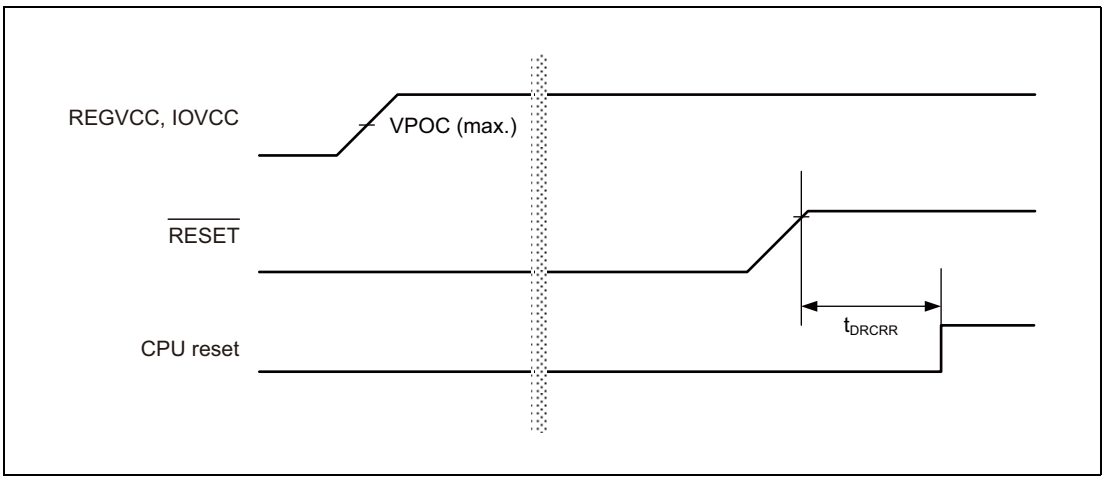


Table 1.6 In case the $\overline{\text{RESET}}$ pin is used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				8*2	µs

Note 1. This is reference value.

Note 2. At least t_{DPCRR} time is necessary reaching from VPOC (max) even if power up sequence is kept shown on **Section 1.8.3, Power Up/Down Timing**.



1.9 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

(1/2)

	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
$\overline{\text{RESET}}$	—	—	√	—	—	—	—	—	—[*4]
FLMD0	—	√	—	—	—	—	—	√	√
AP0_0	√	—	—	—	—	√	Slow	—	√[*1]
AP0_1	√	—	—	—	—	√	Slow	—	√[*1]
AP0_2	√	—	—	—	—	√	Slow	—	√[*1]
AP0_3	√	—	—	—	—	√	Slow	—	√[*1]
AP0_4	√	—	—	—	—	√	Slow	—	√[*1]
AP0_5	√	—	—	—	—	√	Slow	—	√[*1]
AP0_6	√	—	—	—	—	√	Slow	—	√[*1]
AP0_7	√	—	—	—	—	√	Slow	—	√[*1]
AP0_8	√	—	—	—	—	√	Slow	—	√[*1]
AP0_9	√	—	—	—	—	√	Slow	—	√[*1]
AP0_10	√	—	—	—	—	√	Slow	—	√[*1]
JP0_0	—	—	—	√	√	—	Slow	√	√
JP0_1	—	—	—	√	—	—	Slow/Fast	√	√
JP0_2	—	—	—	√	√	—	Slow	√	√
JP0_3	—	—	—	√	√	—	Slow	√	√
JP0_4	—	—	—	√	—	—	Slow	√	√
JP0_5	—	—	—	√	—	—	Slow/Fast	√	√
P0_0	—	√	—	√	—	—	Slow	√	√
P0_1	—	√	—	√	—	—	Slow	√	√
P0_2	—	√	—	√	—	—	Slow/Fast[*2]	√	√
P0_3	—	√	—	√	—	—	Slow/Fast[*2]	√	√
P0_4	—	√	—	√	—	—	Slow	√	√
P0_5	—	√	—	√	—	—	Slow/Fast[*3]	√	√
P0_6	—	√	—	√	—	—	Slow/Fast[*3]	√	√
P0_7	—	√	—	√	—	—	Slow/Fast	√	√
P0_8	—	—	—	√	—	—	Slow	√	√
P0_9	—	√	—	√	—	—	Slow	√	√
P0_10	—	—	—	√	—	—	Slow	√	√
P0_11	—	√	—	√	—	—	Slow	√	√
P0_12	—	√	—	√	—	—	Slow	√	√
P10_0	—	√	—	√	—	—	Slow/Fast	√	√
P10_1	—	—	—	√	—	—	Slow/Fast[*3]	√	√
P10_2	—	√	—	√	—	—	Slow/Fast[*3]	√	√
P10_3	—	√	—	√	—	—	Slow/Fast	√	√
P10_4	—	√	—	√	—	—	Slow/Fast	√	√
P10_5	—	—	—	√	—	—	Slow/Fast	√	√
P10_6	—	√	—	√	—	—	Slow/Fast	√	√
P10_7	—	—	—	√	—	—	Slow/Fast	√	√
P10_8	—	—	—	√	—	—	Slow	√	√
P10_9	—	√	—	√	—	—	Slow	√	√
P10_10	—	—	—	√	—	—	Slow	√	√

(2/2)

	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
Pin Name	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P10_11	—	√	—	√	—	—	Slow	√	√
P10_12	—	—	—	√	—	—	Slow	√	√
P10_13	—	√	—	√	—	—	Slow	√	√
P10_14	—	—	—	√	—	—	Slow	√	√
P10_15	—	√	—	√	—	—	Slow	√	√
P11_0	—	—	—	√	—	—	Slow	√	√
P11_1	—	√	—	√	—	—	Slow	√	√
P11_2	—	—	—	√	—	—	Slow/Fast*3	√	√
P11_3	—	√	—	√	—	—	Slow/Fast*3	√	√
P11_4	—	—	—	√	—	—	Slow	√	√
P8_0	—	—	—	√	—	√	Slow	√	√*5
P8_1	—	—	—	√	—	√	Slow	√	√*5
P8_2	—	—	—	√	—	√	Slow	√	√*5
P8_3	—	—	—	√	—	√	Slow	√	√*5
P8_4	—	—	—	√	—	√	Slow	√	√*5
P8_5	—	—	—	√	—	√	Slow	√	√*5
P8_6	—	—	—	√	—	√	Slow	√	√*5
P9_0	—	—	—	√	—	√	Slow	√	√*5
P9_1	—	—	—	√	—	√	Slow	√	√*5
P9_2	—	—	—	√	—	√	Slow	√	√*5
P9_3	—	—	—	√	—	√	Slow	√	√*5
P9_4	—	—	—	√	—	√	Slow	√	√*5
P9_5	—	—	—	√	—	√	Slow	√	√*5
P9_6	—	—	—	√	—	√	Slow	√	√*5

Note 1. Pull-down resistors for ADC diagnostic purpose. Control via ADC self-diagnostic register.

Note 2. Supports Cload: 100pF

Note 3. Supports Cload: 50pF

Note 4. At a power-on clear reset, an on-chip pull-down resistor at the $\overline{\text{RESET}}$ pin is enabled until the flash sequence is completed.

Note 5. Pull-down resistors for ADC diagnostic and internal pull-down purposes. For ADC diagnostic, control via ADC self-diagnostic register. For internal pull-down, control via PD register.

Caution: Regarding external pull-up resistor of $\overline{\text{RESET}}$ pin, please connect less than 6.6 kΩ.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 ×IOVCC		IOVCC + 0.3	V
		SHMT1 (except FLMD0 pin)		0.7 × IOVCC		IOVCC + 0.3	V
		SHMT1 (FLMD0 pin)*3		0.66 × EVCC		EVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
		TTL	EVCC = VPOC to 3.6 V	2.0		EVCC + 0.3	V
			EVCC = 3.6 V to 5.5 V	2.2		EVCC + 0.3	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.3 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
		TTL		–0.3		0.8	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P8, P9 pin, VI = EVCC*2				0.5	µA
		P10, P11 pin				0.5	µA
		AP0 pin, VI = A0VREF*2				0.5	µA
	ILIL	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P8, P9 pin, VI = 0 V*2				–0.5	µA
		P10, P11 pin, VI = 0 V*2				–0.5	µA
		AP0 pin, VI = 0 V*2				–0.5	µA
Internal pull-up resistance	RU	except FLMD0 pin		20 (275 µA)	40	100	kΩ
		FLMD0*3		10 (550 µA)	19	48	kΩ
Internal pull-down resistance	RD	except FLMD0 pin		20 (275 µA)	40	100	kΩ
		FLMD0		10 (550 µA)	19	50	kΩ
High level output voltage	VOH	Fast mode					
			IOH = –5 mA (6 pins)*4	IOVCC – 1.0			V
			IOH = –3 mA (10 pins)*4	IOVCC – 1.0			V
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
		Slow mode					
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
Low level output voltage	VOL	Fast mode					
			IOL = 5 mA (6 pins)*4			0.4	V
			IOL = 3 mA (10 pins)*4			0.4	V
			IOL = 1 mA (16 pins)*4			0.4	V
		Slow mode					
			IOL = 1 mA (16 pins)*4			0.4	V
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)*5	CL = 30 pF			7	ns
			CL = 50 pF			12	ns
			CL = 100 pF			24	ns
		Fast mode (P0_5, P0_6, P10_1, P10_2, P11_2, P11_3)*6	CL = 50 pF			6	ns
		Fast mode (P0_2, P0_3)*6	CL = 100 pF			6.15	ns
		Slow mode*5	CL = 30 pF			37	ns
			CL = 50 pF			62	ns
			CL = 100 pF			124	ns

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output frequency	f_O	Fast mode	CL = 30 pF			40	MHz
		Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz

Note 1. “IOVCC” means the pins are assigned to the power supply (EVCC and A0VREF).
Note 2. Not select the analog input function of ADCn.
Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 95 kΩ or more as external pull-down resistor.
Note 4. The number of pin indicates simultaneous ON.
Note 5. Measurement point: 0.1 × IOVCC to 0.9 × IOVCC
Note 6. Measurement point: 0.2 × IOVCC to 0.8 × IOVCC

1.9.1 Output Current

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side (Total of P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4)			–30	mA
			Per side (Total of P10_0 to P10_2)			–15	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0)			–30	mA
			Per side (Total of JP0_0 to JP0_5, P0_4 to P0_12, P8_0 to P8_6)			–30	mA
			Total (EVCC)			–60	mA
		PgA0	Total (A0VREF)			–11	mA
Low-level output current	IOL	PgE	Per side (Total of P9_0 to P9_6, P10_6 to P10_14, P11_1 to P11_4)			30	mA
			Per side (Total of P10_0 to P10_2)			15	mA
			Per side (Total of P0_0 to P0_6, P0_11, P0_12, P10_3 to P10_5, P10_15, P11_0)			30	mA
			Per side (Total of JP0_0 to JP0_5, P0_7 to P0_10, P8_0 to P8_6)			21	mA
			Total (EVSS)			60	mA
		PgA0	Total (A0VSS)			11	mA

Note 1. For detail of the definition of “side” and “total”, refer to **Section 1.2.3, Port Current**.

1.10 Power Supply Currents

Condition: REGVCC, EVCC and A0VREF total current. But the I/O buffer is stopped.

ECO Line

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Ta	Peripheral*2				
RUN mode current	IDDR	Run (80 MHz)	Run	–40 to 125°C	Run(#1)		25	60	mA
				25°C	Stop(#1)		19		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (80 MHz)	Run	–40 to 125°C	Run(#2)		36	60	mA
HALT mode current	IDDH	Run (80 MHz)	Run	–40 to 125°C	Run(#3)		20	56	mA

ADVANCED Line

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Ta	Peripheral*2				
RUN mode current	IDDR	Run (96 MHz)	Run	–40 to 125°C**Caution**	Run(#1)		28	72	mA
				25°C	Stop(#1)		21		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (96 MHz)	Run	–40 to 125°C**Caution**	Run(#2)		39	72	mA
HALT mode current	IDDH	Run (96 MHz)	Run	–40 to 125°C**Caution**	Run(#3)		22	68	mA

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Ta	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 85°C	Stop(#2)		0.35	3.5	mA
				105°C	Stop(#2)			8	mA
				125°C	Stop(#2)			12	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop(#3)		35	350	µA
				105°C	Stop(#3)			700	µA
				125°C	Stop(#3)			1000	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 85°C	Run(#4)		1.6	11	mA
				105°C	Run(#4)			17	mA
				125°C	Run(#4)			24	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 85°C	Run(#5)		0.40	6	mA
				105°C	Run(#5)			9	mA
				125°C	Run(#5)			13	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Ta = 25°C
- REGVCC = EVCC = A0VREF = 5.0 V
- AWOVSS = EVSS = A0VSS = 0 V

Note 2. Operating condition of each peripheral function is shown in the table of next page.

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj≤150°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Function		Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Stop	Stop
	FOUT	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read/Write	Read/Write	No access	Fetch	No access	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Stop	Stop	Stop
	ADCA0	Run*1	Run*1	Run*1	Stop	Stop	Stop	Stop	Stop
ISO	CPU	Run (PLL)	Run (PLL)	Halt (PLL)	Run (HS IntOSC)	Stop	Run (PLL)	Stop	Power off
	DMA	Run	Run	Run	Stop	Stop	Stop	Stop	
	PLL	Run	Run	Run	Stop	Stop	Run	Stop	
	Code flash	Fetch	Fetch	No access	No access	No access	Fetch	No access	
	Data flash	Read	Write\Erase	No access	No access	No access	Read	No access	
	PLRAM	Read/Write	Read/Write	No access	No access	No access	Read/Write	No access	
	SLRAM	Read/Write	Read/Write	No access	No access	No access	Read/Write	No access	
	OSTM0	Run	Run	Run	Stop	Stop	Stop	Stop	
	WDTA1	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAPA, PIC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	ENCA0	Run	Run	Run	Stop	Stop	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN3n	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN2n	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	RS-CANn	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CSIGn	Run	Run	Run	Stop	Stop	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Stop	Stop	
	RIIC0	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CLMA2	Run	Run	Run	Stop	Stop	Stop	Stop	

Note 1. T&H used.

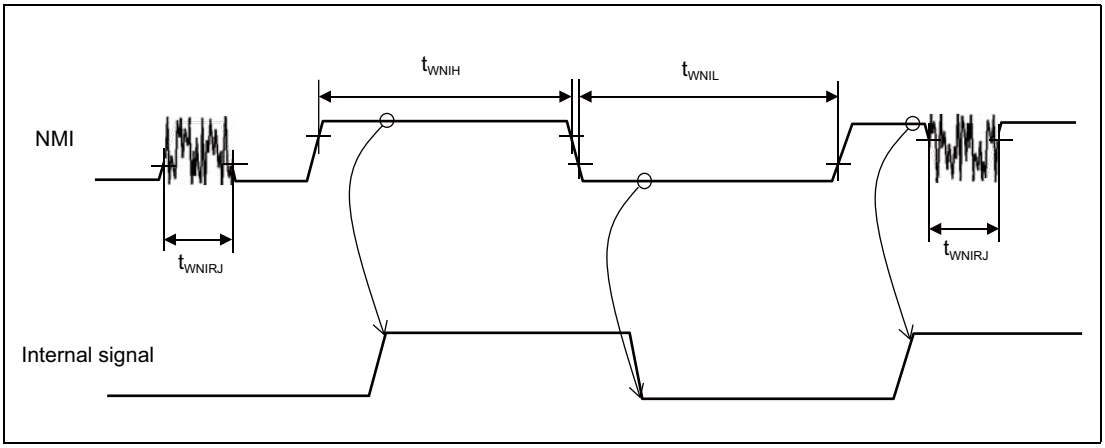
1.11 Interrupt Timing

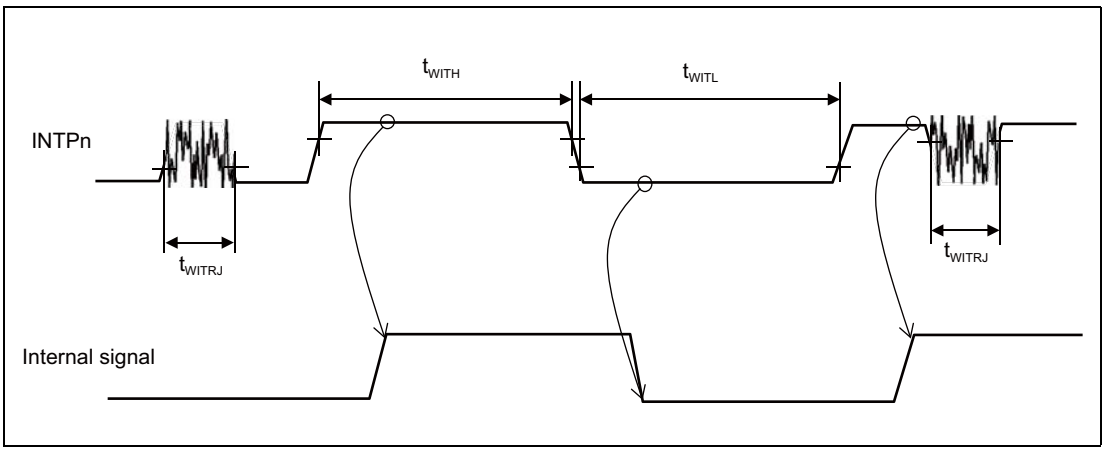
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high/low level width*1	t_{WNIH}/ t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			µs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high/low level width*1	t_{WITH}/ t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			µs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





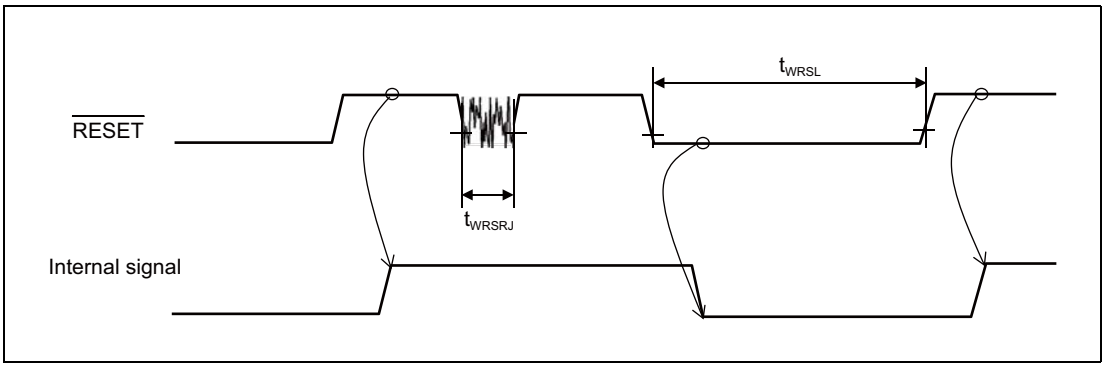
1.12 $\overline{\text{RESET}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	*3	0.6			µs
		*4	5.0			µs
		*5	600			µs
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		0.1			µs

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.

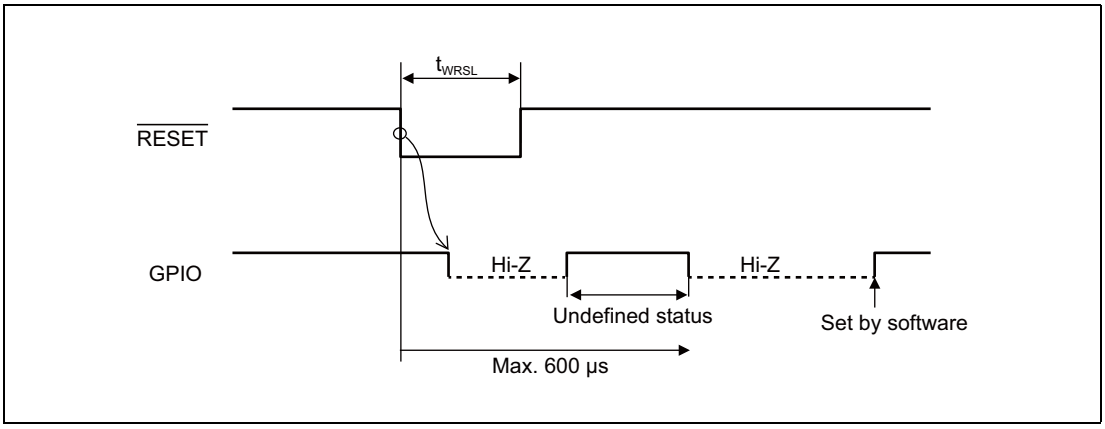


Note 3. After $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600 µs will become Hi-z. (figure (a))

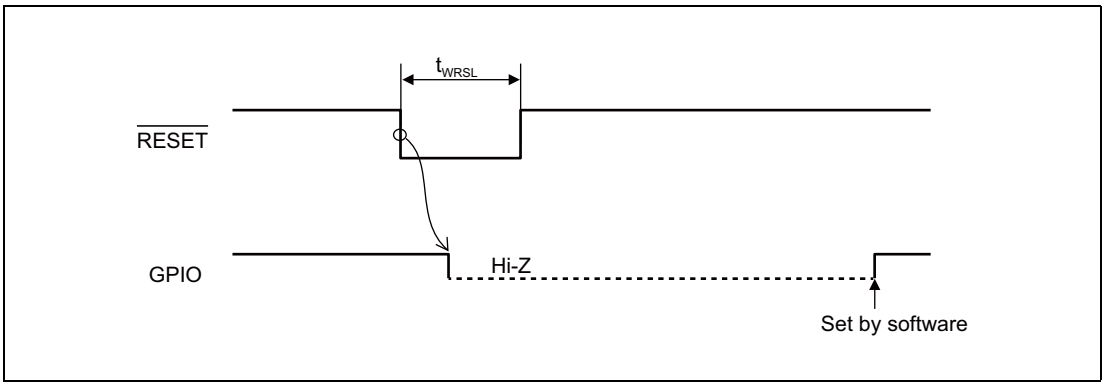
Note 4. If during RUN mode or HALT mode, after $\overline{\text{RESET}}$ is asserted GPIO pin will become Hi-z. For other modes, after $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600 µs will become Hi-z. (figure (a) and (b))

Note 5. GPIO output states will become Hi-z after $\overline{\text{RESET}}$ is asserted. (figure (b))

(a) In case of either
t_{WRSL} < 5 µs, any mode or
t_{WRSL} < 600 µs, any mode except for RUN and HALT mode.



(b) In case of either
5 µs ≤ t_{WRSL}, RUN and HALT mode or
600 µs ≤ t_{WRSL}, any mode.

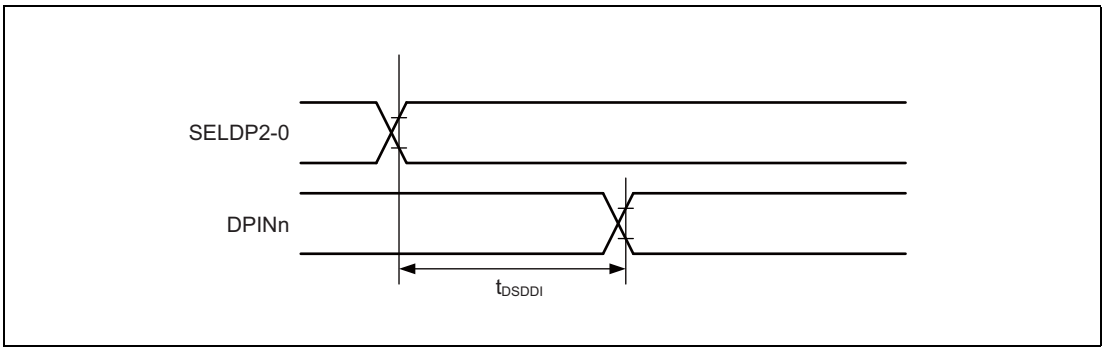


1.13 Low Power Sampler (DPIN input) Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note 1. n = 7 to 0



1.14 CSCXFOUT Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

<Output driver strength>

CSCXFOUT: Slow or fast mode (refer to the condition in the following table)

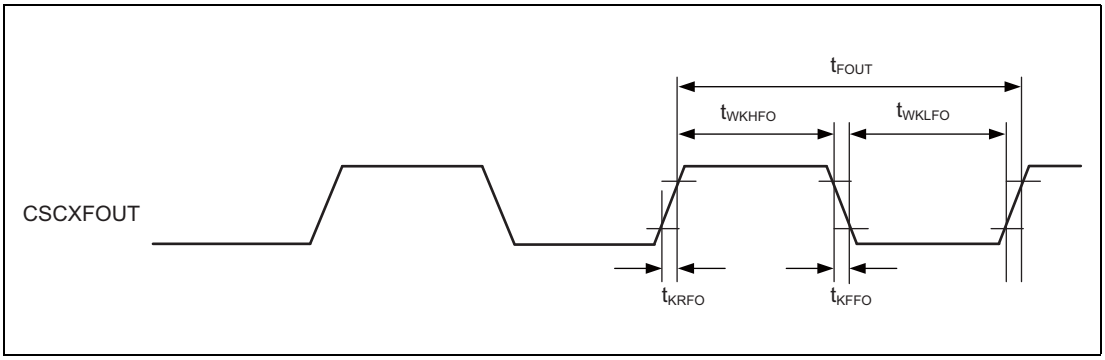
Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	Slow mode		100 (max. 10 MHz)			ns
		Fast mode (Except JP0_3 pin)*1		41.6 (max. 24 MHz)			ns
CSCXFOUT high level width	t_{WKHFO}	Slow mode	N: 1*2 or even value*3	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*3, *4	t_{FOUT} × (N+1) / 2N – 37			ns
		Fast mode (Except JP0_3 pin)*1	N: 1*2 or even value*3	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*3	t_{FOUT} × (N+1) / 2N – 10			ns
CSCXFOUT low level width	t_{WKLFO}	Slow mode	N: 1*2 or even value*3	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*3, *4	t_{FOUT} × (N–1) / 2N – 37			ns
		Fast mode (Except JP0_3 pin)*1	N: 1*2 or even value*3	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*3	t_{FOUT} × (N–1) / 2N – 10			ns
CSCXFOUT rise/ fall time	t_{KRFO}/ t_{KFFO}	Slow mode				37	ns
		Fast mode (Except JP0_3 pin)*1				10	ns

Note 1. JP0_3 does not support fast mode.

Note 2. When MainOSC, HS IntOSC or LS IntOSC is selected as source clock with the condition of N=1, the characteristics of output signal depends on the selected source clock. It is recommended to use output signal after evaluation on an actual environment.

Note 3. “N” is the value of “Clock divisor N” defined by FOUTDIV register.

Note 4. The selection of N = 3 is prohibited when slow mode is used.



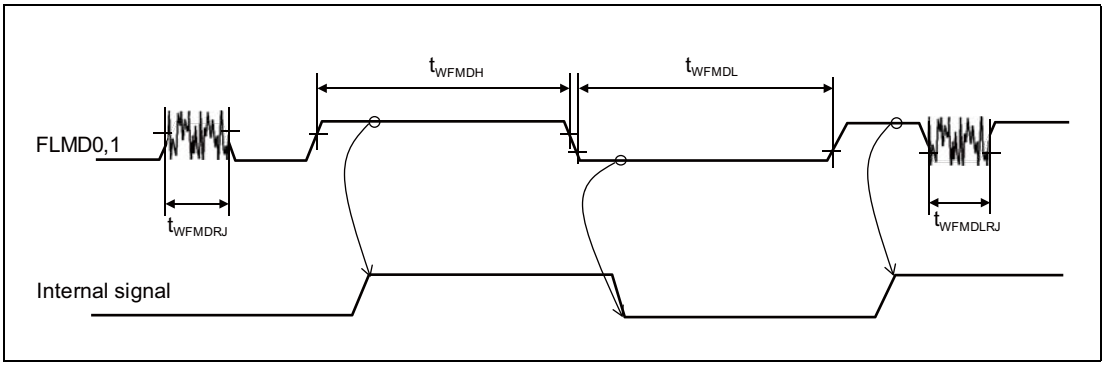
1.15 Mode Timing

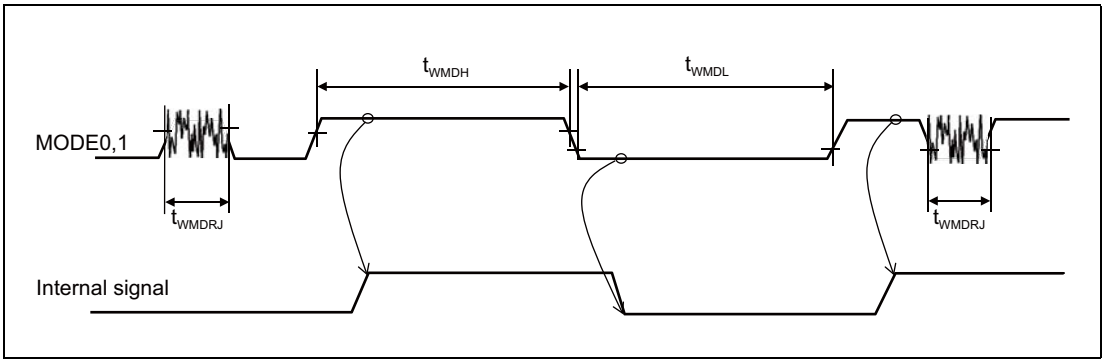
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0,1 input high/low level width*1	t_{WFMDH}/ t_{WFMDL}		600			ns
FLMD0, 1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0, 1 input high/low level width*1	t_{WMDH}/ t_{WMDL}		600			ns
MODE0, 1 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0,1 and MODE0,1 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





1.16 Timer Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

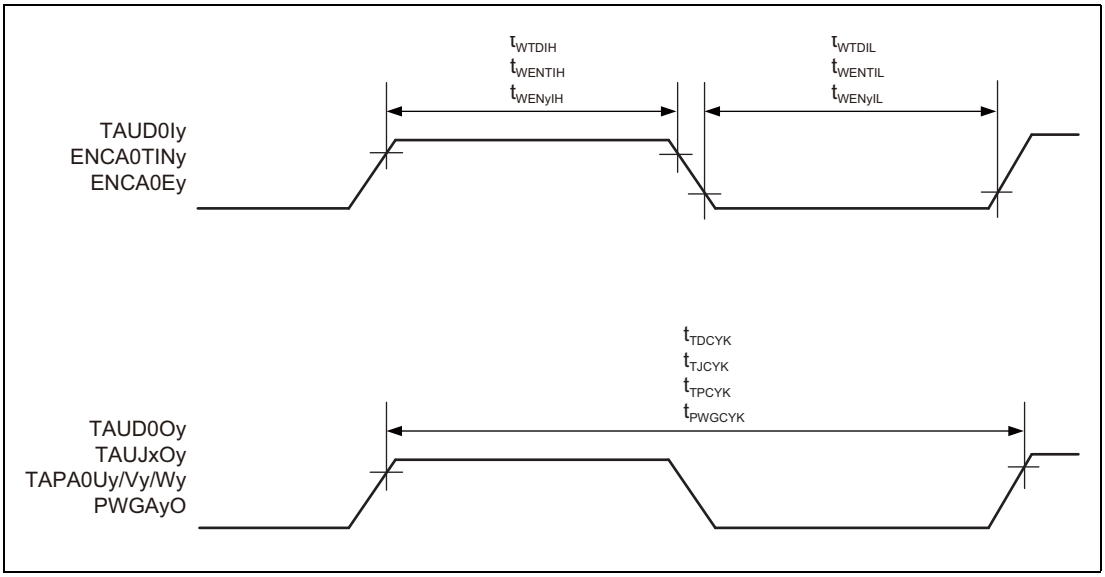
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20[*1, *2]			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width[*3] (x = 0, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxIy pulse rejection[*4]	t_{WTIJRJ}		100			ns
TAUJxOy output cycle (x = 0, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
TAPA0ESO input high/low level width[*3]	t_{WESIH}/ t_{WESIL}		600			ns
TAPA0ESO pulse rejection[*4]	t_{WESIRJ}		100			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t_{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t_{WENTIH}/ t_{WENTIL}		n × Tsamp + 20[*1]			ns
ENCA0Ey input high/low level width (y = 0,1,C)	t_{WENyIH}/ t_{WENyIL}		n × Tsamp + 20[*1]			ns
PWGAyO output cycle (y = 0 to 23)	t_{PWGCYK}	Slow mode			10	MHz

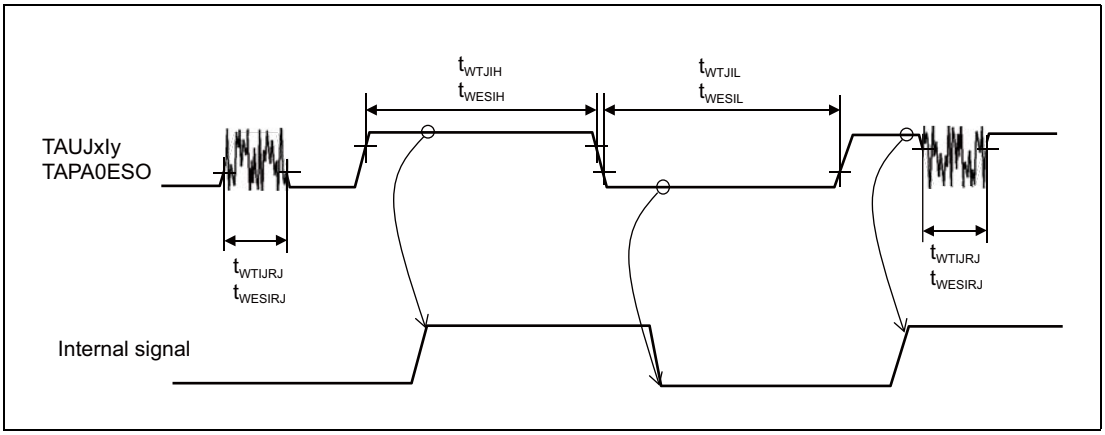
Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

Note 3. TAUJxIy and TAPA0ESO input width is needed to ensure that the internal timer input signal is activated.

Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.


tWTDIH
tWENTIH
tWENyIH
tWTDIL
tWENTIL
tWENyIL
TAUD0Iy
ENCA0TINy
ENCA0Ey
tTDCYK
tTJCYK
tTPCYK
tPWGCYK
TAUD0Oy
TAUJxOy
TAPA0Uy/Vy/Wy
PWGAyO


tWTJIH
tWESIH
tWTJIL
tWESIL
TAUJxIy
TAPA0ESO
tWTIJRJ
tWESIRJ
tWTIJRJ
tWESIRJ
Internal signal

1.17 RLIN2/RLIN3 Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baudrate	1		115.2*1	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

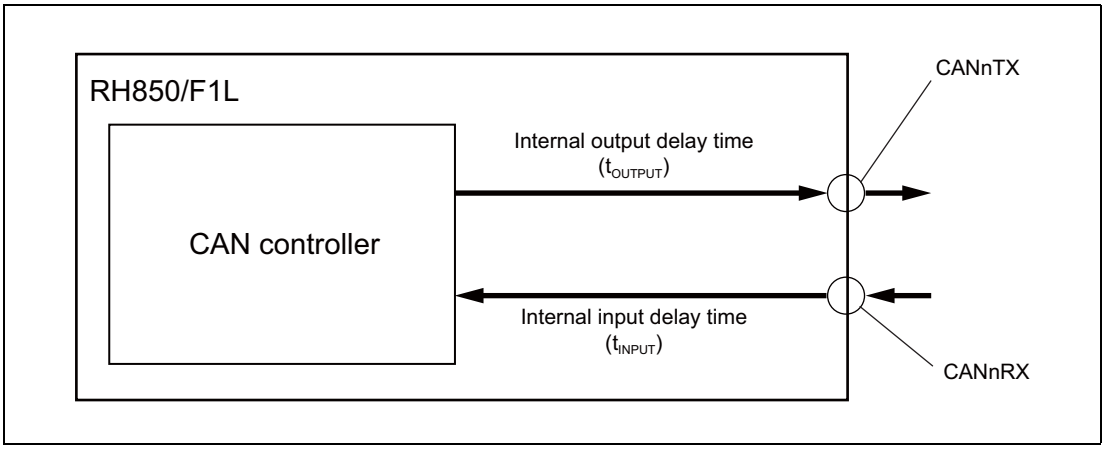
Note 1. The LIN extended baudrate is not part of the LIN standard specification.

1.18 RS-CAN Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time*1	t_{NODE}				100	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



1.19 CSI Timing

1.19.1 CSIG Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Table 1.7 CSIG Timing (Master Mode)

<Output driver strength>

CSIGnSO, CSIGnSC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}	ECO line	12.5 (max. 80 MHz)			ns
		ADVANCED line	10.42 (max. 96 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		$0.5 \times t_{KCYMGn} - 10$			ns
CSIGnSC low level width	t_{KWLMGn}		$0.5 \times t_{KCYMGn} - 10$			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	$2 \times t_{KCYGn} + 25$			ns
CSIGnRYI High level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	$t_{KCYGn} + 5$			ns

n = 0

Table 1.8 CSIG Timing (Slave Mode)

<Output driver strength>

CSIGnSO: Fast mode

CSIGnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}	ECO line	12.5 (max. 80 MHz)			ns
		ADVANCED line	10.42 (max. 96 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		$0.5 \times t_{KCYSGn} - 10$			ns
CSIGnSC low level width	t_{KWLSGn}		$0.5 \times t_{KCYSGn} - 10$			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSISGn}		$t_{KCYGn} + 5$			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}	$t_{KCYSGn} \geq 8 \times t_{KCYGn}$			38	ns
		$t_{KCYSGn} < 8 \times t_{KCYGn}$			$38 + t_{KCYGn}$	ns
$\overline{\text{CSIGnSSI}}$ setup time (vs.CSIGnSC)	$t_{SSSISGn}$		$0.5 \times t_{KCYSGn} - 5$			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs. CSIGnSC)	$t_{HSSISGn}$		$t_{KCYGn} + 5$			ns

n = 0

1.19.2 CSIH Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Table 1.9 CSIH Timing (Master Mode)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode (CL = 100pF@n=0 / 50pF@n=1-2)
CSIHnCSSm: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}	ECO line	12.5 (max. 80 MHz)			ns
		ADVANCED line	10.42 (max. 96 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn}/2			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI high level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 15			ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

n = 0 to 2

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]

CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]

CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]

x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock period an inactive width time $t_{WSCSBHn}$ of "0.5 × t_{KCYMHn}" is added.

Table 1.10 CSIH Timing (Slave Mode)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode
CSIHnRYO: Slow mode

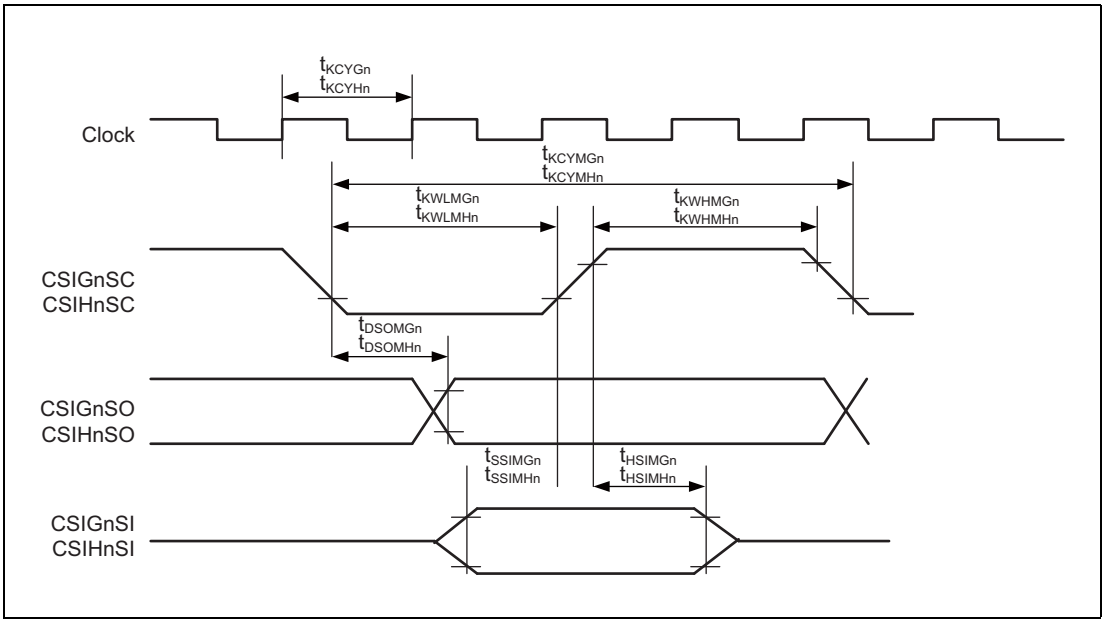
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}	ECO line	12.5 (max. 80 MHz)			ns
		ADVANCED line	10.42 (max. 96 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			38	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$38 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

n = 0 to 2

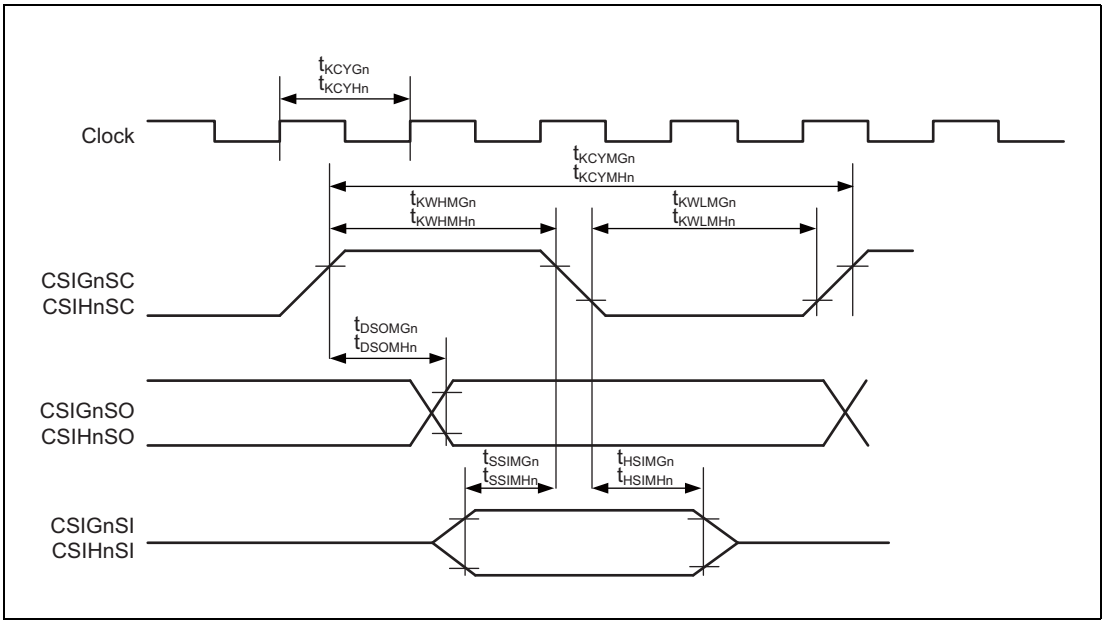
(1) SCKO/SI/SO

Master Mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

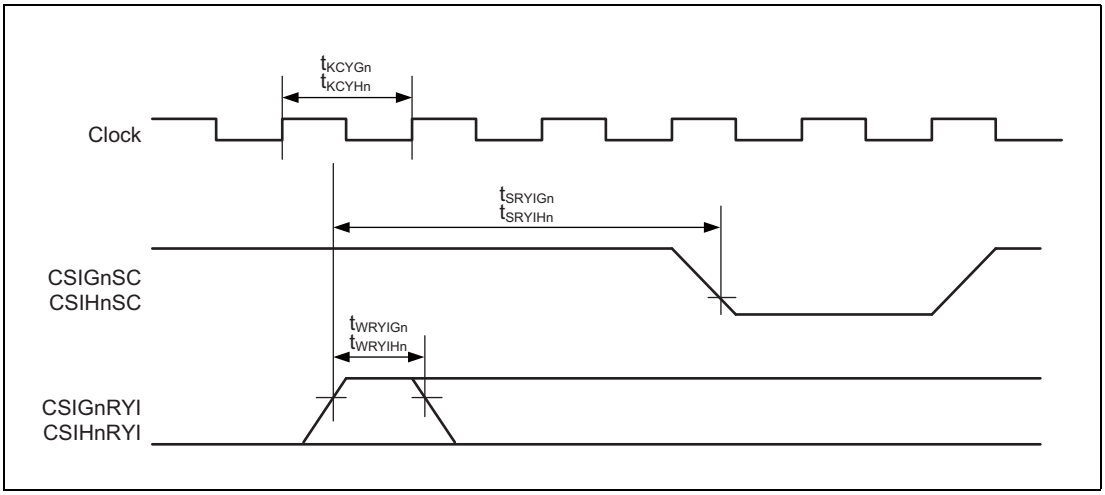


(2) RYI

- CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
- CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

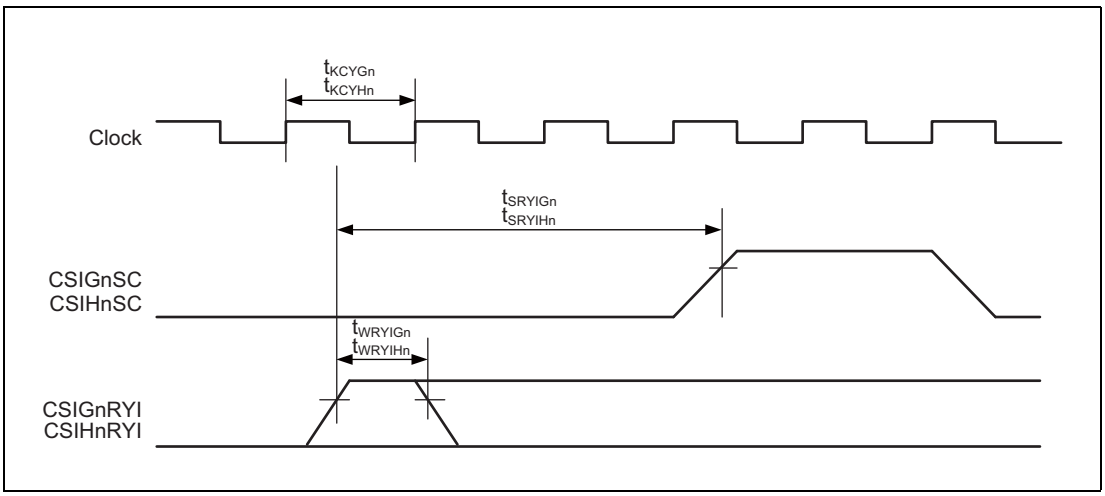
– CSIG (CSIGnCTL1: CSIGnCKR = 0)

– CSIH (CSIHnCFGm: CSIHnCKPm = 0)



– CSIG (CSIGnCTL1: CSIGnCKR = 1)

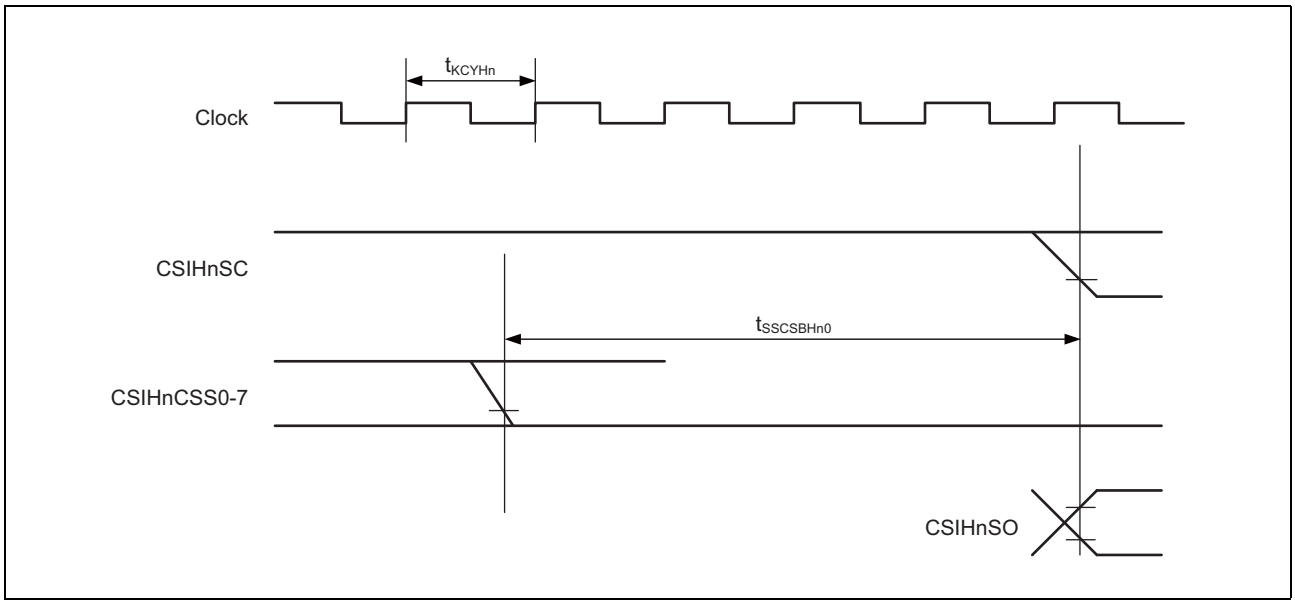
– CSIH (CSIHnCFGm: CSIHnCKPm = 1)



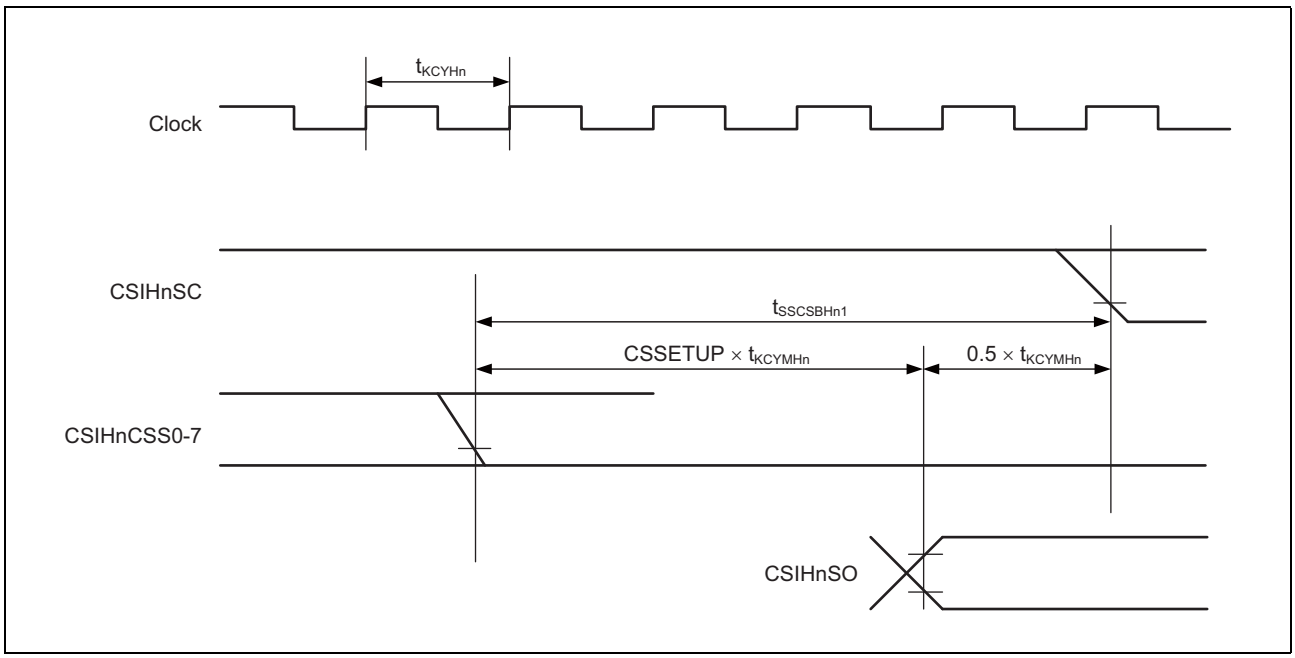
(3) CSSn

Only Master Mode (Setup Time):

- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0

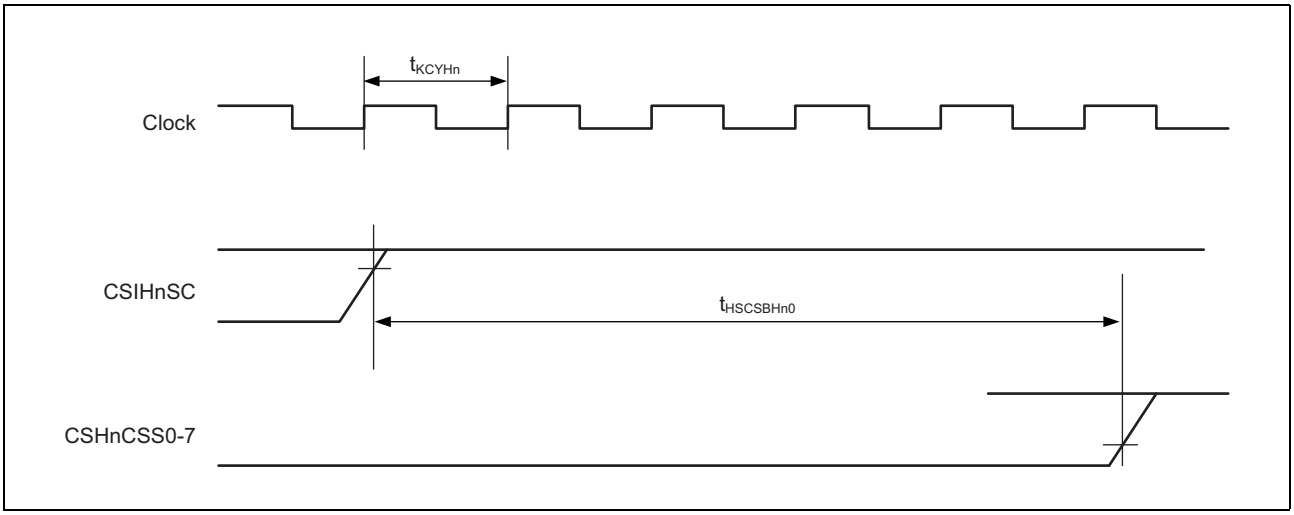


- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 1

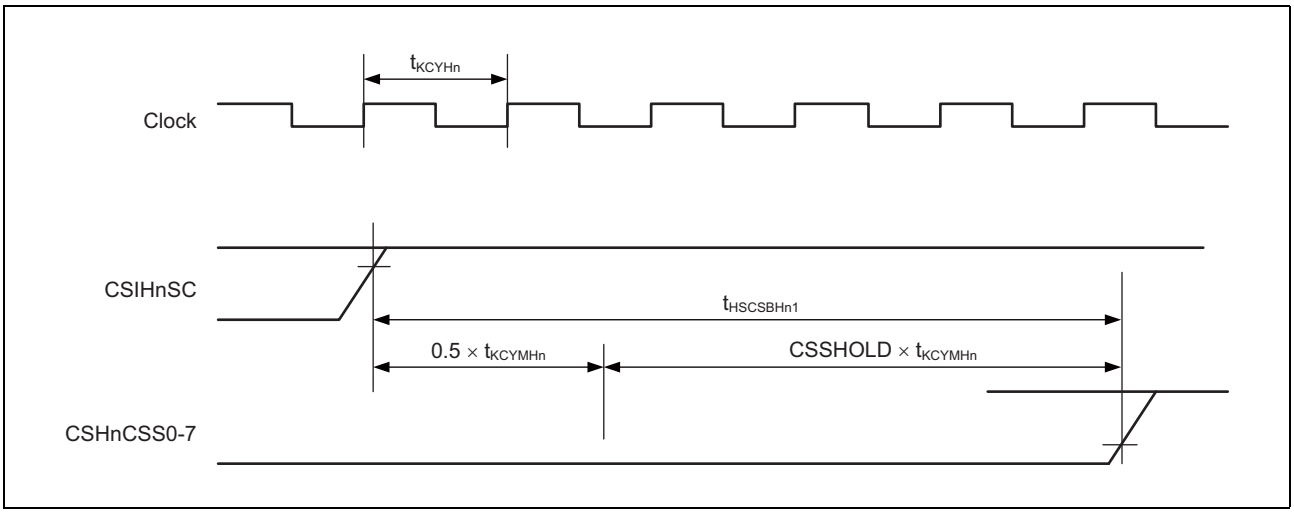


Only Master Mode (Hold Time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGm: CSIHnCKPm = 0,
  CSIHnCFGm: CSIHnDAPm = 0



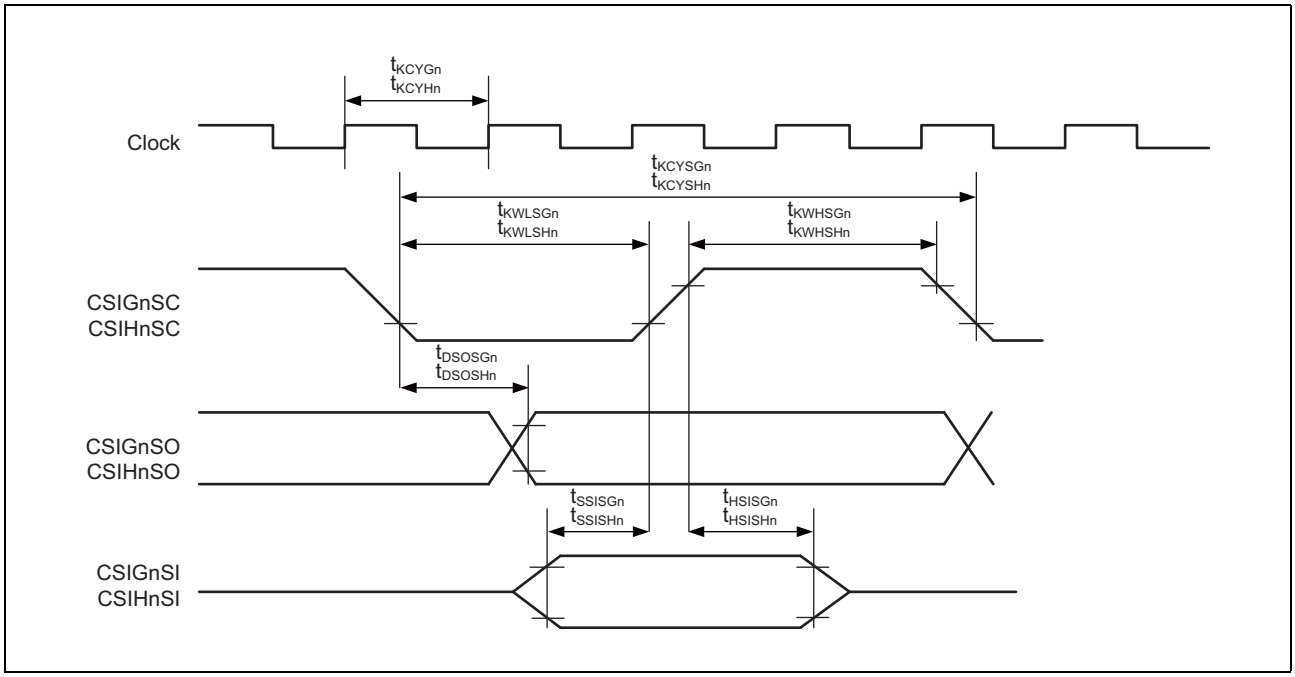
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



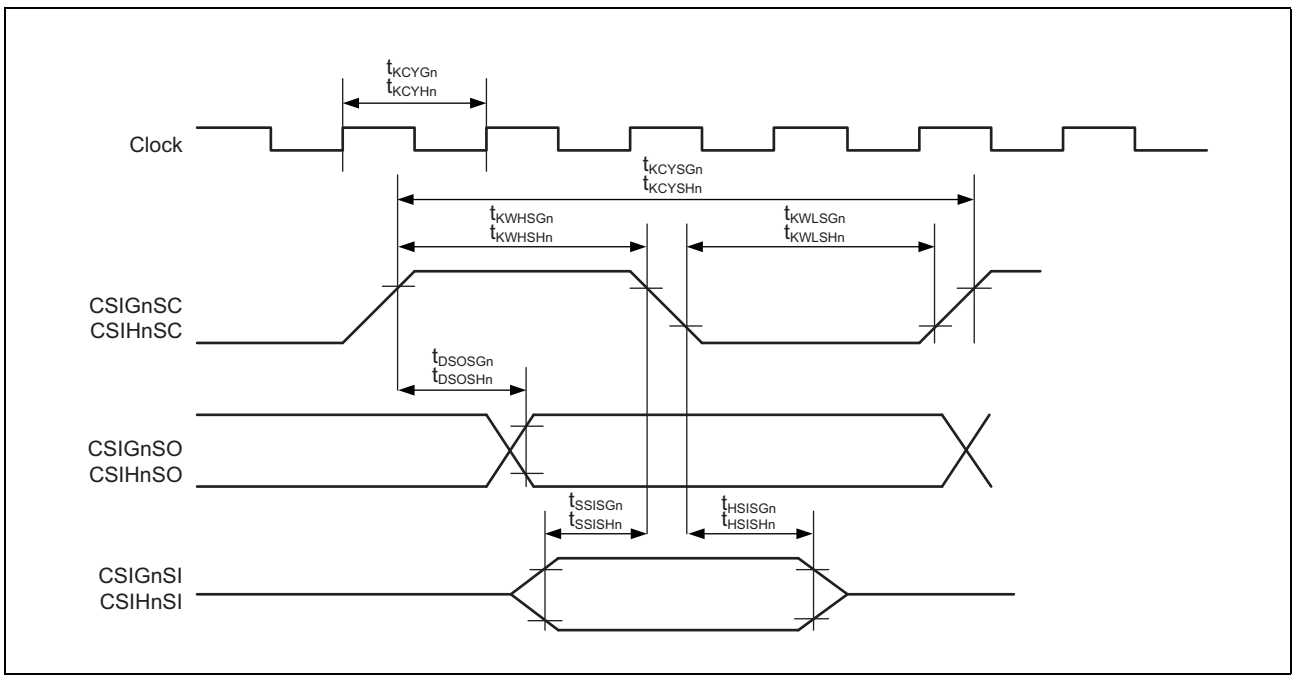
(4) SCKO/SI/SO

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)

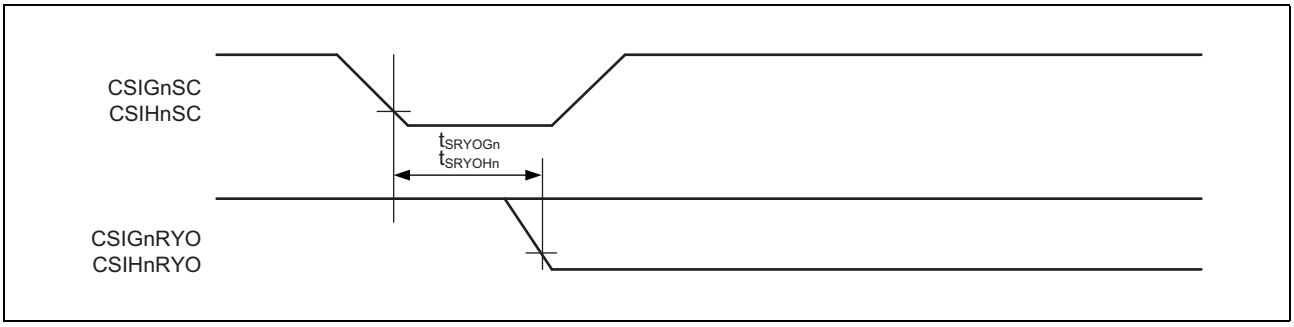


- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

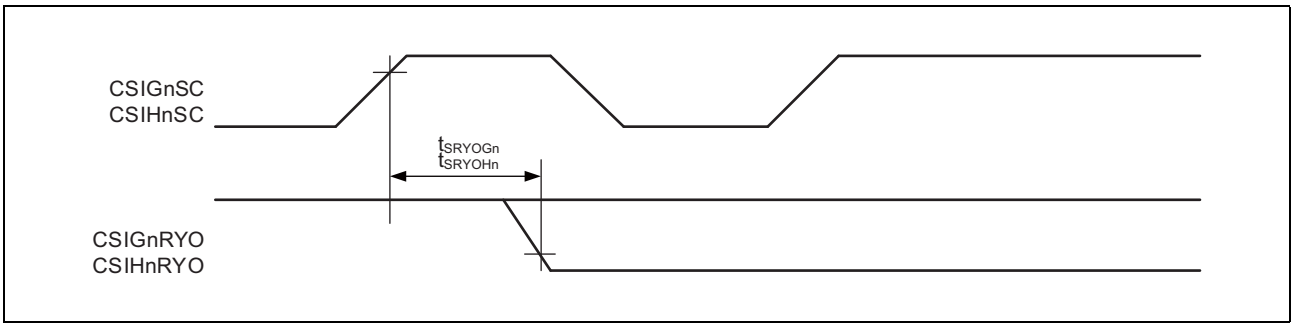


(5) RYO

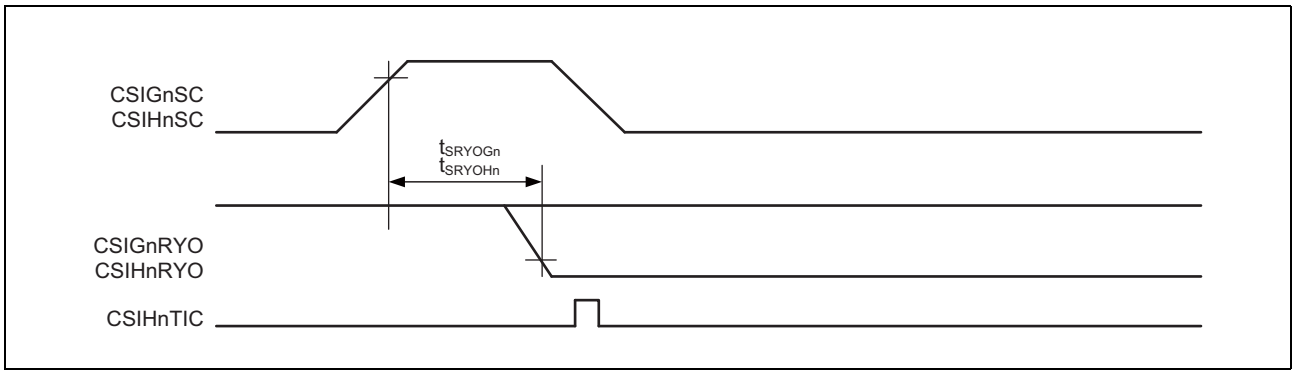
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0)



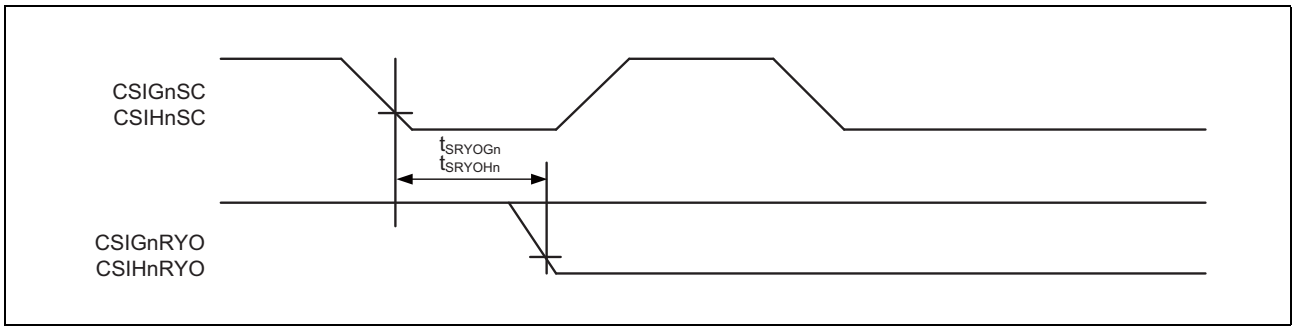
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0)



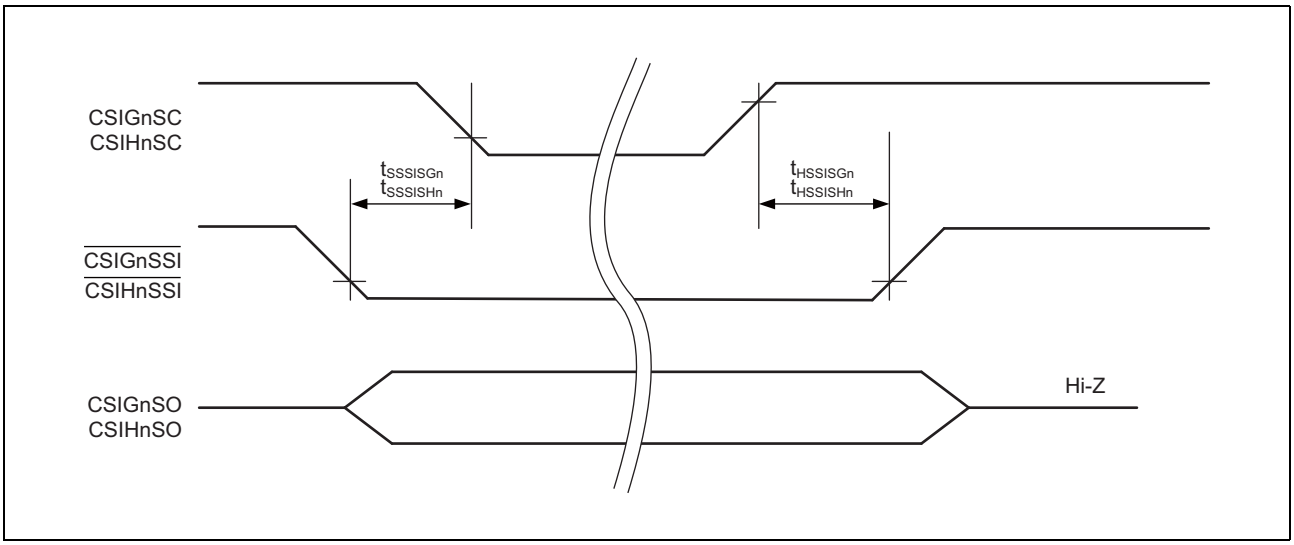
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/1)



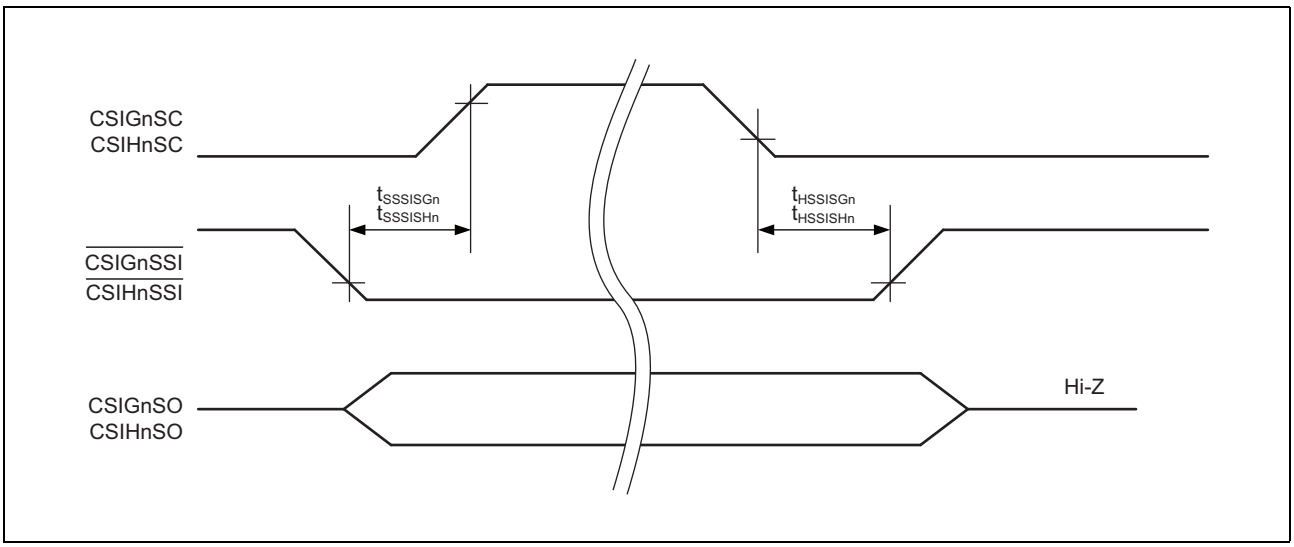
(6) SSI

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



1.20 RIIC Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C

Table 1.11 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RIIC0SCL clock low-level width	t_{LOW}		4.7			µs
RIIC0SCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Table 1.12 RIIC Timing (Fast Mode)

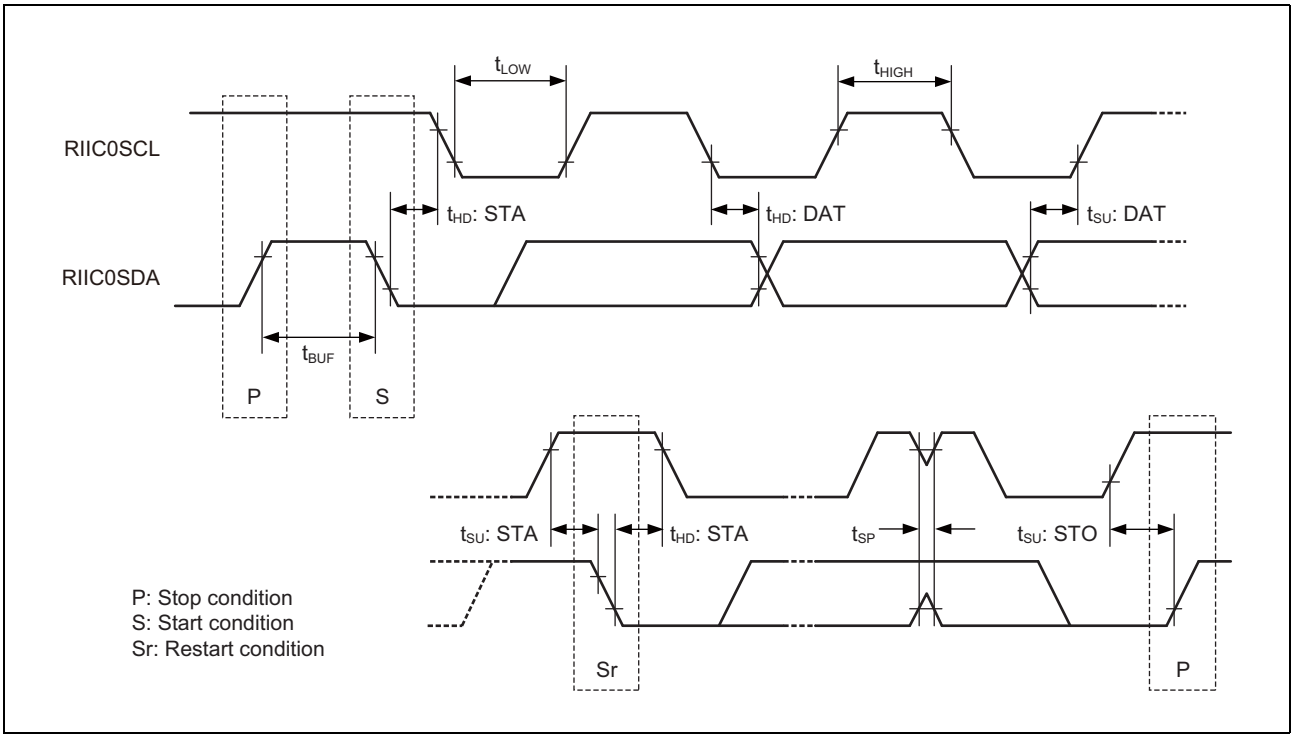
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RIIC0SCL clock low-level width	t_{LOW}		1.3			µs
RIIC0SCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		100*4			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 4. The fast mode IIC bus can be used in normal mode IIC bus system. In this case, set the fast mode IIC bus so that it meets the following conditions.
- If the system does not extend the RIIC0SCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIIC0SCL signal's low state hold time:
Transmit the following data bit to the RIIC0SDA line prior to releasing the RIIC0SCL line
(1250 ns: Normal mode IIC bus specification).

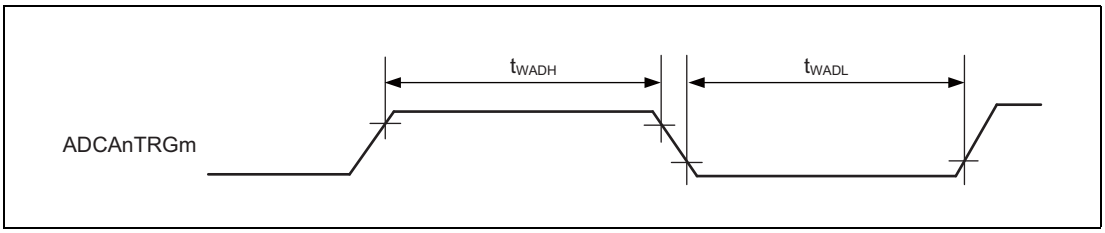

RIIC0SCL
RIIC0SDA
tLOW
tHIGH
tHD: STA
tHD: DAT
tSU: DAT
tBUF
P
S
tSU: STA
tHD: STA
tSP
tSU: STO
Sr
P
P: Stop condition
S: Start condition
Sr: Restart condition

1.21 ADTRG Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high/ low level width	t_{WADH}/ t_{WADL}		k × Tsamp + 20*1			ns

Note 1. k: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

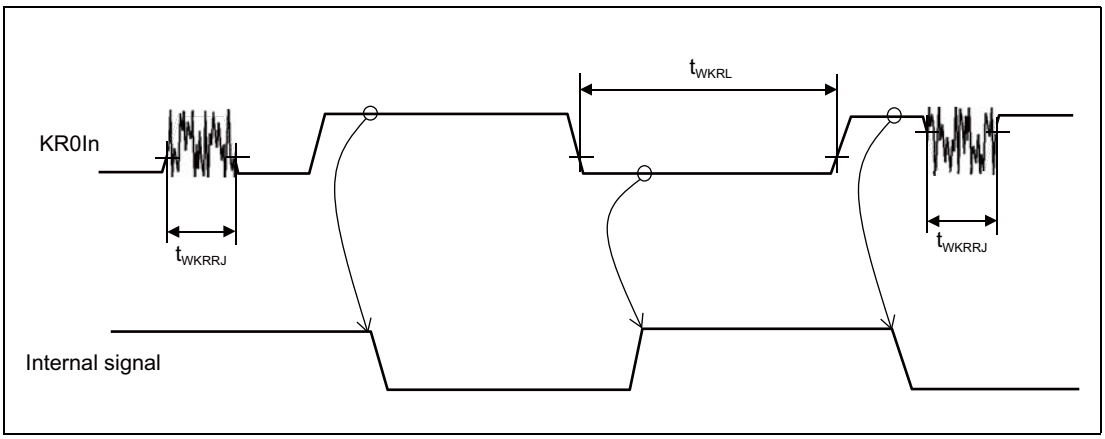


1.22 Key Return Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.
Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



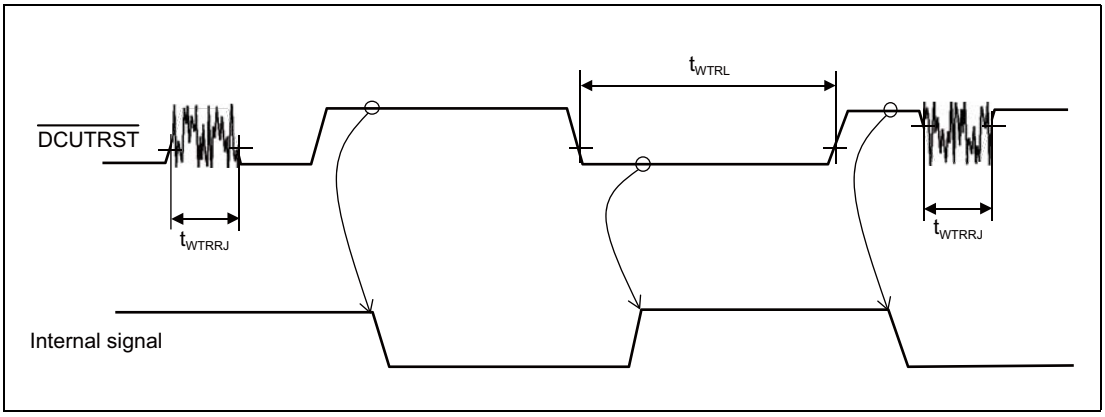
1.23 $\overline{\text{DCUTRST}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input low level width*1	t_{WTRL}		600			ns
$\overline{\text{DCUTRST}}$ pulse rejection*2	t_{WTRRJ}		100			ns

Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



1.24 Debug Interface Characteristics

1.24.1 Nexus Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

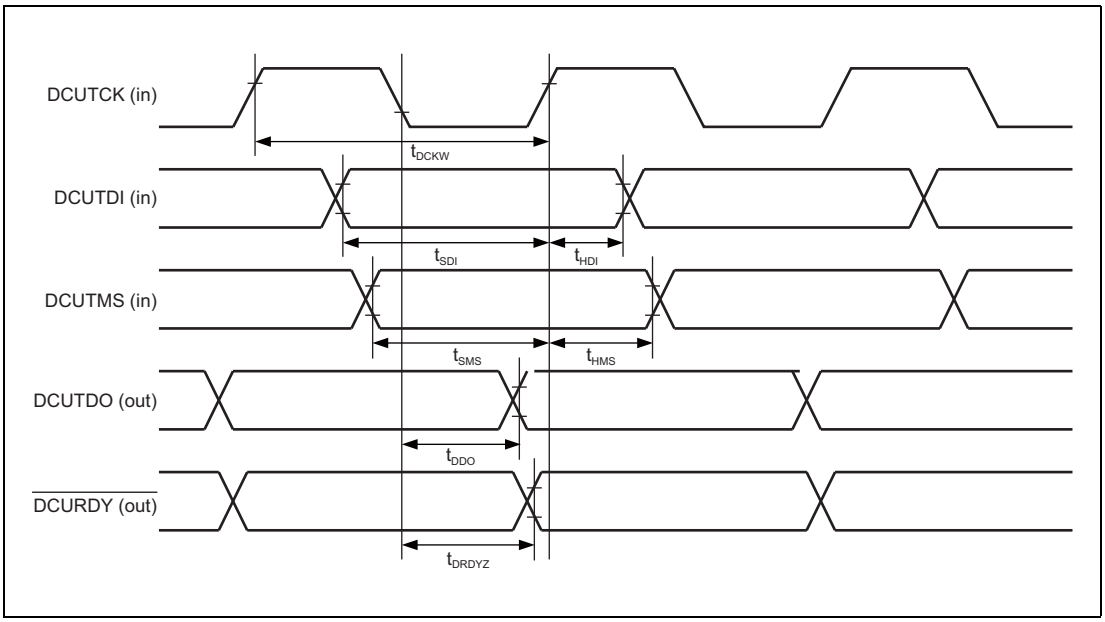
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTC K ↑)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK ↑)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK ↑)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK ↑)	t_{HMS}		3			ns
DCUTDO delay time (↓ DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (↓ DCUTCK)	t_{RDYZ}		0		20	ns



1.24.2 LPD (4 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 100 pF

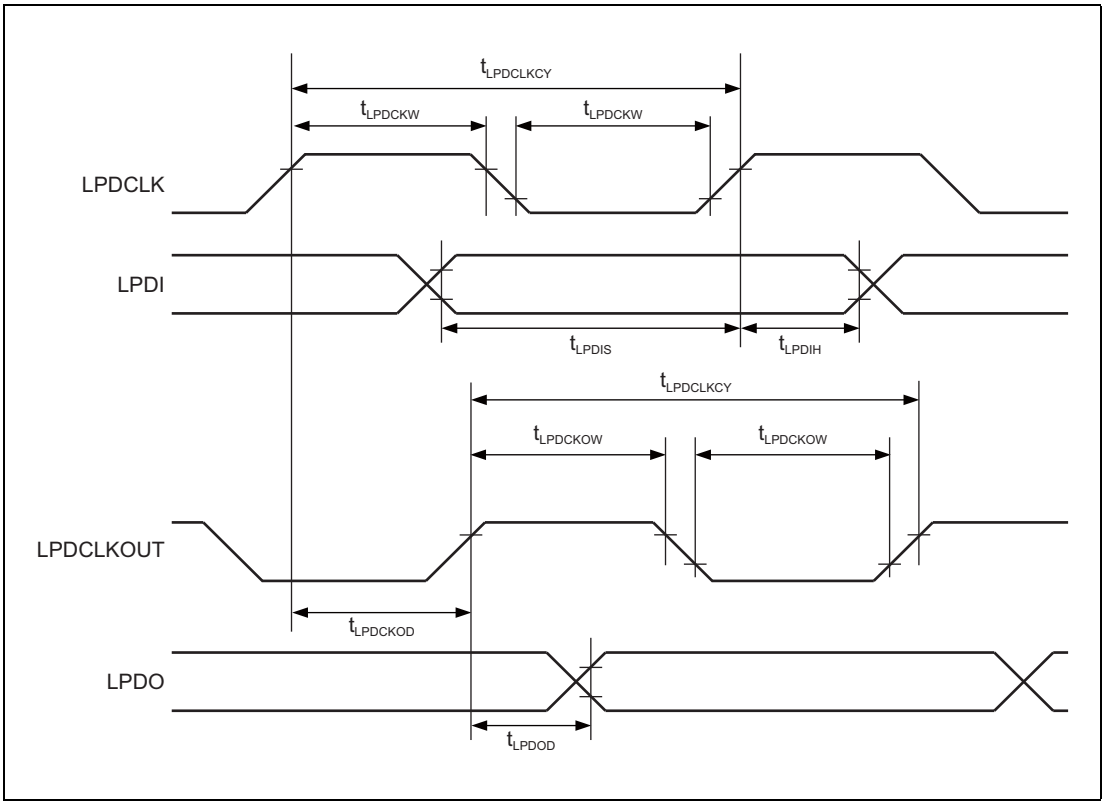
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max.12MHz)			ns
LPDCLK High-level width/ LPDCLK Low-level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT High-level width/ LPDCLKOUT low-level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns



1.24.3 LPD (1 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 50 pF

<Input buffer>

LPDIO: TTL

<Output driver strength>

LPDIO: Fast mode

<External pull-up resistor>

LPDIO: 4.7 kΩ to 10 kΩ

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) Baud rate					2.0	Mbps

1.25 Flash Programming Characteristics

1.25.1 Code Flash

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/– 30%, CISOVCL: 0.1µF +/– 30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Table 1.13 Basic characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3	ECO line	4*4		40	MHz
		ADVANCED line	4*4		48	MHz
Number of rewrites*1	CWRT	Data retention of 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. f_{PCLK} = 1/2 f_{CPUCLK}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.14 Programming characteristic (1/2)

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	256 B		0.4*1	6*1	ms
			8 KB		20	90	ms
			32 KB		80	360	ms
			256 KB		0.6	2.7	s
			384 KB		0.9	4.1	s
			512 KB		1.2	5.4	s
			768 KB		1.7	8.1	s
			1 MB		2.3	10.8	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		0.5*1	7.2*1	ms
			8 KB		24	108	ms
			32 KB		96	432	ms
			256 KB		0.7	3.3	s
			384 KB		1.1	4.9	s
			512 KB		1.4	6.5	s
			768 KB		2.1	9.8	s
			1 MB		2.7	13	s

Table 1.14 Programming characteristic (2/2)

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Erase time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.25.2 Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/– 30%, CISOVCL: 0.1µF +/– 30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Table 1.15 Basic characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3	ECO line	4*4		40	MHz
		ADVANCED line	4*4		48	MHz
Number of rewrites*1	CWRT	Data retention 20 years*2	125 k			times
		Data retention 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 168 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Note 3. f_{PCLK} = 1/2 f_{CPUCLK}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.16 Programming characteristics

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.16*1	1.7*1	ms
		f_{PCLK} ≥ 20 MHz	32 KB		1.4	6.8	s
Erasure time		f_{PCLK} ≥ 20 MHz	64 B		1.7*1	10*1	ms
		f_{PCLK} ≥ 20 MHz	32 KB		0.9	5.2	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100*1	µs
			32 KB			35.2	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.25.3 Serial Programming Interface

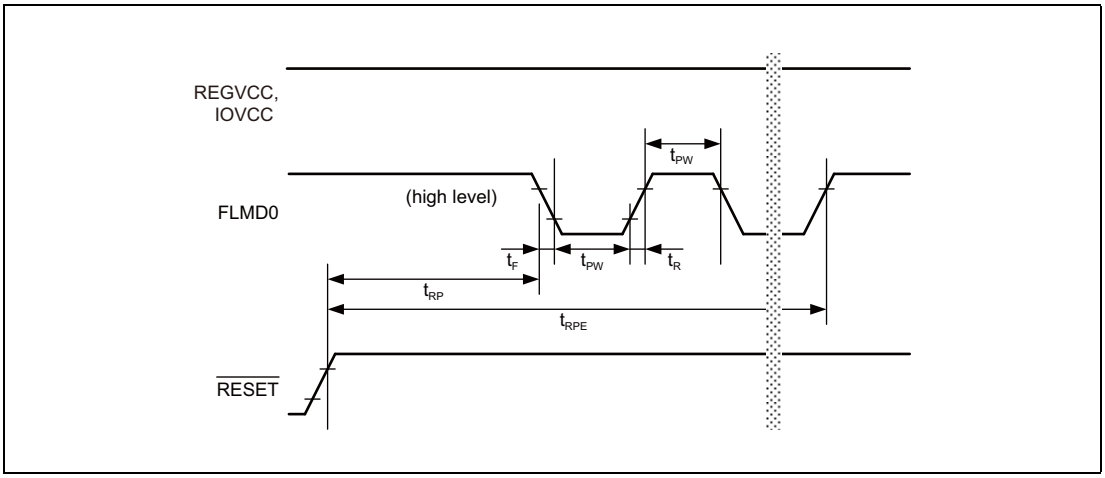
1.25.3.1 Serial Programmer Setup Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				11.5	ms
FLMD0 low/high level width	t_{PW}		0.8			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

NOTE

IOVCC: EVCC = A0VREF



1.25.3.2 FLSCI3 Interface

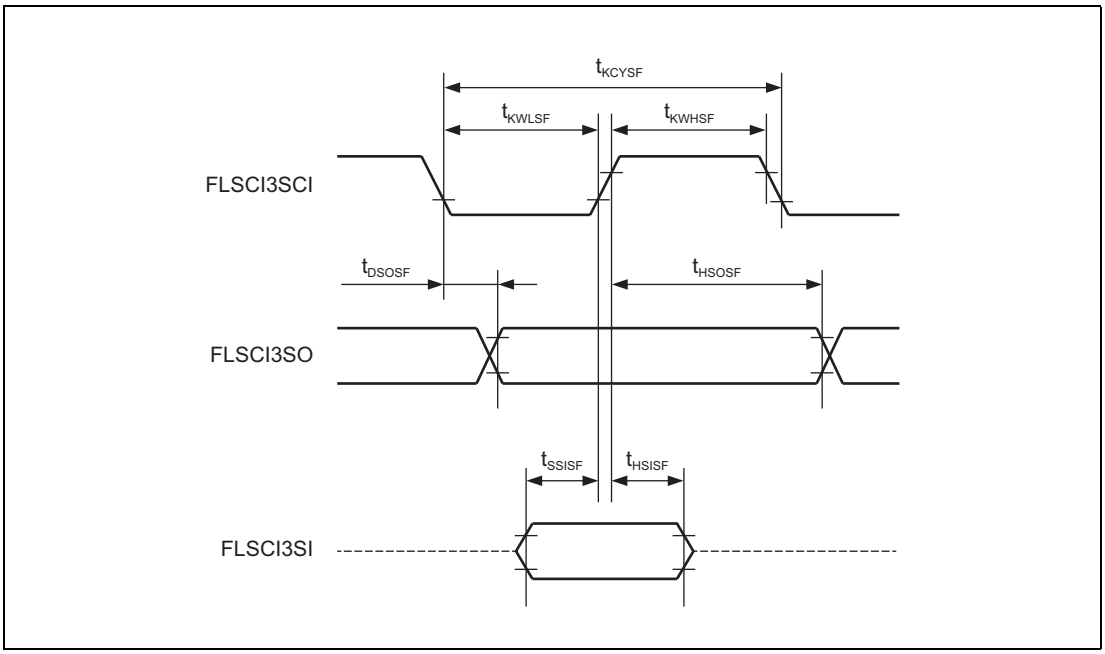
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/–30%, CISOVCL: 0.1µF +/–30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLSCI3 transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode			2	Mbps
FLSCI3SCI cycle time	t_{KCYSF}	3-wired clock sync mode	200*1			ns
FLSCI3SCI high level width	t_{KWHSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SCI low level width	t_{KWLSF}	3-wired clock sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SI setup time (vs. FLSCI3SCI)	t_{SSISF}	3-wired clock sync mode	55			ns
FLSCI3SI hold time (vs. FLSCI3SCI)	t_{HSISF}	3-wired clock sync mode	55			ns
FLSCI3SO output delay (vs. FLSCI3SCI)	t_{DSOSF}	3-wired clock sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired clock sync mode Not continuous transfer (data: except 1st bit)			$-t_{KWHSF}$ + 3 × t_{Pcyc} + 36	ns
FLSCI3SO hold time (vs. FLSCI3SCI)	t_{HSOSF}	3-wired clock sync mode	2 × t_{Pcyc}			ns

Note 1. Input the external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



1.26 A/D Converter Characteristics

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V,
CAWOVCL: 0.1µF +/– 30%, CISOVCL: 0.1µF +/– 30%, Ta = –40 to (depend on the product) °C,
CL = 30 pF

(1/3)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLKn	T&H is not used			8*3		40	MHz
		T&H used			16		40	MHz
Resolution	RESn	12-bit mode			12	12	12	bit
		10-bit mode			10	10	10	bit
Conversion time	t_{CONn}	ADCAnSMPCR.SMPT[7:0] = 12 H(40 cycle) (8M Hz*3 × ADCLKn × 32 MHz), External MPX is not used			1.25		5	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (46 cycle) (8 MHz*3 × ADCLKn × 40 MHz), External MPX is not used			1.15		5.75	µs
		ADCAnSMPCR.SMPT[7:0]=12 H (80 cycle) (8 MHz*3 × ADCLKn × 32 MHz), External MPX is used			2.5*4		10	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (92 cycle) (8 MHz*3 × ADCLKn × 40 MHz), External MPX is used			2.3*4		11.5	µs
Sampling time	t_{SMP}	ADCAnSMPCR.SMPT[7:0] = 12 H (18 cycle) (8 MHz*3 × ADCLKn × 32 MHz)			0.56		2.25	µs
		ADCAnSMPCR.SMPT[7:0] = 18 H (24cycle) (8 MHz*3 × ADCLKn × 40 MHz)			0.6		3	µs
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±4.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±6.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±6.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±8.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±8.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±10.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±2.0	LSB
				ADCAnImS			±3.0	LSB
Analog input voltage	VAIN0SN	ADCAnIm	T&H not used		AnVSS		AnVREF	V
		ADCA0I0,2,4	T&H used		0.2		A0VREF – 0.2	V
		ADCA0ImS	A0VREF ≥ EVCC		A0VSS		EVCC	V
			A0VREF < EVCC		A0VSS		A0VREF	V
Operation current	IA0VREF	T&H not used				1.1	3.0	mA
		T&H used (max. 3 pins)					*2	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS					1	10	µA
T&H current	ITH					0.5	1.3	mA/ch
T&H sampling time	t_{THSMP}				450			ns
T&H hold time	t_{THHOLD}						10	µs
Set up time of self diagnosis voltage circuit	t_{BOOT}				500			ns
Set up time of self diagnosis voltage level	t_{OUT}				500			ns

(2/3)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Pull-down resistor for discharge mode		ADCnIm pins			350	500	650	kΩ
		ADCnImS pins			100	215	800	kΩ
Accuracy of self-diagnosis function	TESH0SN	12bit mode	Self-diagnosis voltage level = AnVREF		4015-|TOEn|		4095	–
			Self-diagnosis voltage level = 2/3AnVREF		2651-|TOEn|	2731	2811+|TOEn|	–
			Self-diagnosis voltage level = 1/2AnVREF		1968-|TOEn|	2048	2128+|TOEn|	–
			Self-diagnosis voltage level = 1/3AnVREF		1285-|TOEn|	1365	1445+|TOEn|	–
			Self-diagnosis voltage level = AnVSS		0		80+|TOEn|	–
		10bit mode	Self-diagnosis voltage level = AnVREF		1003-|TOEn|		1023	–
			Self-diagnosis voltage level = 2/3AnVREF		663-|TOEn|	683	703+|TOEn|	–
			Self-diagnosis voltage level = 1/2AnVREF		492-|TOEn|	512	532+|TOEn|	–
			Self-diagnosis voltage level = 1/3AnVREF		321-|TOEn|	341	361+|TOEn|	–
			Self-diagnosis voltage level = AnVSS		0		20+|TOEn|	–
Integral nonlinearity error*1	ILEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±2.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±3.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±3.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±4.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±4.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±5.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Differential nonlinearity error*1	DLEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±1.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±2.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±3.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±4.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±3.0	LSB
				ADCA0I0,2,4 (w/ T&H)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0V to 4.5V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
Zero scale error (offset error)*1	ZSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±3.5	LSB
				ADCA0I0,2,4 (w/ T&H)			±5.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±5.5	LSB
				ADCA0I0,2,4 (w/ T&H)			±7.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±7.5	LSB
				ADCA0I0,2,4 (w/ T&H)			±9.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB

(3/3)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Full scale error*1	FSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±3.5	LSB
				ADCA0I0,2,4 (w/ T&H)			±5.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±5.5	LSB
				ADCA0I0,2,4 (w/ T&H)			±7.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±7.5	LSB
				ADCA0I0,2,4 (w/ T&H)			±9.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB

n = 0

Note 1. This does not include quantization error.

Note 2. 3.0 + 1.3 × (the number of used T&H)

Note 3. Include the oscillation accuracy of HS IntOSC.

Note 4. When the external multiplexer is used, the detail time of A/D conversion is MPX setup time, sampling time and successive approximation time. MPX setup time is same as “sampling time + successive approximation time”.

Note 5. Conversion accuracy when ADCA0ImS terminal is converted in 12-bit mode:
Conversion accuracy can be applied if lower 2-bit is ignored from conversion result.

CAUTION

When an external digital pulse is applied to AP0, P8 and P9 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse.

The same behavior may apply when the digital buffer is used as output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

1.27 Injection Currents

For the injection current, there are two type specifications. These type are depend on Package, Flash size and Product name. These relationships are shown as the following table.

Flash Size	Product Name	Applicable Type
1 MB/ 768 KB	Except below products	Type 1
	R7F701xxxxAFP#YJ1 R7F701xxxxAFP#YK1 R7F701xxxxAFP#YB1 R7F701xxxxAFP#AA1 R7F701xxxxAFP#KA1	Type 2
512 KB/ 384 KB/ 256 KB	Except below products	Type 1
	R7F701xxxxAFP#YJ1 R7F701xxxxAFP#YJ2 R7F701xxxxAFP#YK1 R7F701xxxxAFP#YK2 R7F701xxxxAFP#YB2 R7F701xxxxAFP#AA2 R7F701xxxxAFP#KA2	Type 2

Table 1.17 Definition of Pin Group

Symbol	Power Supply for Pin Group	Pin for Type 1 Products	Pin for Type 2 Products
PgE	EVCC, EVSS	JP0, P0, P10, P11	JP0, P0, P10, P11
PgE'	EVCC, EVSS	P8, P9	Not Available*1
PgA0	A0VREF, A0VSS	AP0	AP0

Note 1. Do not apply an overvoltage on P8 and P9 pins.

1.27.1 Absolute Maximum Ratings

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			total			–60	mA

CAUTIONS

1. The DC injection current (total) must satisfy the specifications of the injection current per pin.
2. In case of injected current for PgA0, TESH0SN cannot be kept. Its deviating value will increase sharply with increasing absolute value of injection current.

1.27.2 DC Characteristics for Overload Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

1.27.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Leakage current coupling factor for positive overload current	K_{INJP}	PgE	Per pin			3.0×10^{-6}	—
		PgE’	Per pin			3.0×10^{-6}	—
		PgA0	Per pin			4.8×10^{-6}	—
Leakage current coupling factor for negative overload current	K_{INJN}	PgE	Per pin			7.5×10^{-6}	—
		PgE’	Per pin			7.5×10^{-6}	—
		PgA0	Per pin			2.6×10^{-6}	—

NOTES

1. This is reference value.
2. An overload current through a pin will cause a certain error current in the adjacent pins. This error current must be added to the respective leakage current (ILIH or ILIL) of the adjacent pins.
3. The amount of error leakage current depends on the overload current and is defined by the overload coupling factor K_{INJ}.
   The total current through a pin is:
   $| I_{total} | = |$ ILIH or ILIL $| + (| I_{INJn} | \times K_{INJn})$

1.27.4 AD Characteristics for Pins Influenced by Injected Current on an Adjacent

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Degradation of overall error*1	I_{INJP}	3 mA per pin	ADCAnIm			±1.3	LSB
			ADCAnImS			±1.3	LSB
		Total 20 mA	ADCAnIm			±3.8	LSB
			ADCAnImS			±3.8	LSB
	I_{INJN}	–3 mA per pin	ADCAnIm			±1.4	LSB
			ADCAnImS			±1.4	LSB
		Total –20 mA	ADCAnIm			±4.5	LSB
			ADCAnImS			±4.5	LSB

n = 0

Note 1. This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Note 2. This is reference value.

CAUTION

When there is an increased leakage current on the analog input pins, based on currents injected into the pins adjacent to the converted channel, the effect on the ADC accuracy depends on the external analog source impedance.

[Example] Conditions: A0VREF = 5.0 V, external analog source impedance = 10 kΩ.

If there is a leakage current of 1 μA by injected current, the effect on the ADC accuracy is 1 (μA) × 10 k (Ω) / 5 (V) = 0.2%FSR

1.28 Thermal Characteristics

1.28.1 Parameters

Item	Symbol	Estimate	Unit	Note
Thermal Resistance	Θja	49	°C/W	Conforming to JESD51-7 (4 layers)
Thermal Characterization Parameter	ψjb	35	°C/W	Conforming to JESD51-7 (4 layers)

Note: The thermal resistance depend on the usage environment.

1.28.2 Assumed Board

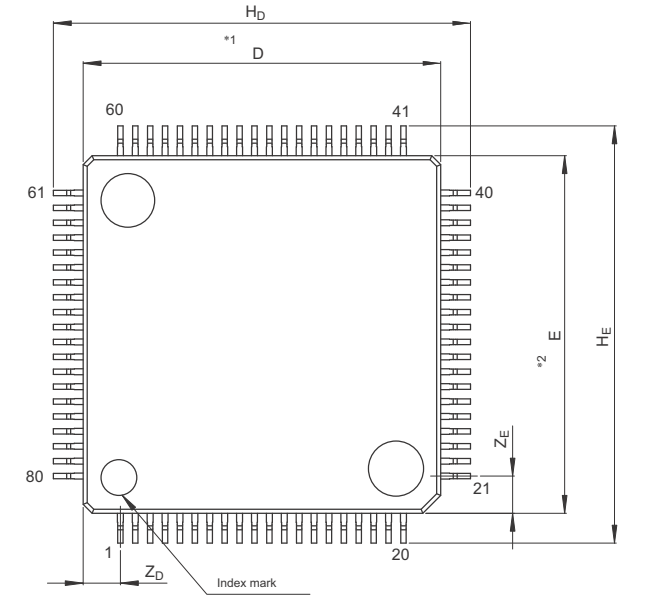
Conforming to JESD51-7 (4 layers)

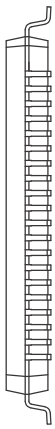
	Board size (mm)		
	X	Y	Area (mm^2)
Board	76.2	114.3	8709.66
Remaining copper rates	Thickness of conductors		
50-95-95-50%	70-35-35-70 µm		

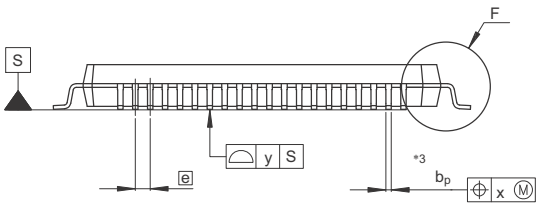
Section 2 Package Dimensions

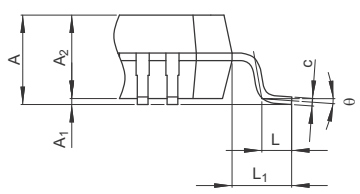
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KG-A	—	0.50

Unit: mm

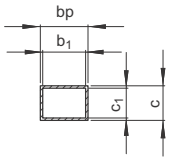








Detail F



Terminal cross section

NOTE)
1. DIMENSIONS "*1 AND "*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT
   INCLUDE TRIM OFFSET.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	0.10	0.15
bp	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	RH850/F1L (80 pin Version) Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Jul 10, 2013	—	First Edition issued
0.81	Dec 03, 2013	1	1.1.2.1 Common Conditions, Power supply, Capacitance of the internal regulator changed
		4	1.2.3 Port Current changed
		5	1.3 Capacitance, note 1 and note 2 changed
		5	1.4 Operational Condition, note 2 changed
		6	1.5 Oscillator Characteristics, CAUTION changed
		7	1.7 PLL Characteristics changed
		7	1.8 Regulator Characteristics changed; note 1 changed
		8, 9	1.9 Pin Characteristics changed, note 2 and note 6 changed
		10	1.10 Power Supply Currents changed
		12	1.11 Interrupt Timing changed
		13	1.12 Power Up/Down Timing, timing diagram changed
		19	1.20.2 CSIH Timing, CAUTION changed
		32	1.24 POC Characteristics changed
		33	1.25 LVI Characteristics changed
		33	1.26 VLVI Characteristics changed
		35	1.28 Core Voltage Monitor Characteristics changed
		35, 36	1.29 A/D Converter Characteristics changed
		37	1.30 Flash Characteristics, (1) Code Flash, Table 1.9 Basic Characteristics, note 2 changed
		37	1.30 Flash Characteristics, (1) Code Flash, Table 1.10 Programming Characteristics changed
		38	1.30 Flash Characteristics, (2) Data Flash, Table 1.11 Basic Characteristics, note 2 changed
		38	1.30 Flash Characteristics, (2) Data Flash, Table 1.12 Programming Characteristics, note 2 changed
		39, 40	1.31 Injection Currents, added
1.00	Oct 20, 2014	All	Arrangement of sections
		1 to 4	Product Introduction, added
		5	1.1 Overview, changed
		5	1.1.1 Pin Groups, changed
		5	1.1.2.1 Common Conditions, changed
		7	1.2 Absolute Maximum Ratings, CAUTIONS 1., changed
		7	1.2.2 Port Voltages, changed
		9	1.2.4 Temperature Condition, changed
		9	1.3 Capacitance, changed
		10, 11	1.4 Operational Condition, changed
		12	1.5 Oscillator Characteristics, changed; one figure added
		13	1.6 Internal Oscillator Characteristics, changed
		13	1.7 PLL Characteristics, changed
		14	1.8 Power Management Characteristics, subsection added
		14	1.8.1 Regulator Characteristics, changed
		15 to 17	1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics, added

Rev.	Date	Description	
		Page	Summary
1.00	Oct 20, 2014	18 to 20	1.8.3 Power Up/Down Timing, changed; Table 1.2 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin added; two figures added
		21	1.8.4 CPU Reset Release Timing, added
		22, 23	1.9 Pin Characteristics, changed
		25	1.9.1 Output Current, subsection added
		26, 27	1.10 Power Supply Currents, changed
		28	1.11 Interrupt Timing, changed; two figures added
		29	1.12 $\overline{\text{RESET}}$ Timing, changed; figure added
		29	1.13 Low power sampler (DPIN input) timing, subsection added
		30	1.14 CSCXFOUT Timing, changed
		31	1.15 Mode Timing, changed; two figures added
		32, 33	1.16 Timer Timing, changed; figure added
		34	1.17 RLIN2/RLIN3 Timing, changed
		34	1.18 RS-CAN Timing, changed
		35	1.19.1 CSIG Timing, changed
		36, 37	1.19.2 CSIH Timing, changed
		46	1.20 RIIC Timing, changed
		49	1.21 ADTRG Timing, changed
		49	1.22 Key Return Timing, changed; figure added
		50	1.23 $\overline{\text{DCUTRST}}$ Timing, added
		51	1.24 Debug Interface Characteristics, added
		51	1.24.1 NEXUS Interface Timing, added
		52	1.24.2 LPD (4 pin) Interface Timing, added
		53	1.24.3 LPD (1 pin) Interface Timing, added
		54, 55	1.25.1 Code Flash, subsection number changed, description changed
		56	1.25.2 Data Flash, subsection number changed, description changed
		57	1.25.3.1 Serial Programmer Setup Timing, changed
		58	1.25.3.2 FLSCI3 Interface, added
		59 to 61	1.26 A/D Converter Characteristics, changed
		62	1.26.1 Equivalent Circuit of the Analog Input Block, changed
		63	1.27 Injection Currents, changed
		63	1.27.1 Absolute Maximum Ratings, changed
		63	1.27.2 DC Characteristics for Overload Current, changed
		64	1.27.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin, changed
		65	1.27.4 AD Characteristics for Pins Influenced by Injected Current on an Adjacent, subsection added; description changed
		—	1.31.4 A/D Diagnosis Function Influenced by Injected Current, deleted
1.10	Dec 25, 2014	5	1.1.2.1 Common Conditions: Changed
		10, 11	1.4 Operational Condition: Note 3 changed
		12	1.5 Oscillator Characteristics: Changed, figures of “MainOSC” changed
		13	1.7 PLL Characteristics: Changed
		15 to 17	1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics: Changed, figures of “POC” changed, and figure of “CVM” added
		18	Table 1.1 In case the $\overline{\text{RESET}}$ pin is used: Changed

Rev.	Date	Description	
		Page	Summary
1.10	Dec 25, 2014	19	Table 1.2 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin: Changed
		20	Table 1.3 In case the $\overline{\text{RESET}}$ pin is not used and fixed to high level by pull-up*1: Changed
		21	Table 1.4 In case the $\overline{\text{RESET}}$ pin is not used: Changed
		22 to 25	1.9 Pin Characteristics: Changed
		32, 33	1.16 Timer Timing: Changed, figure changed
		46	1.20 RIIC Timing: Description of condition changed
		46	Table 1.10 RIIC Timing (Normal Mode): Changed
		47, 48	Table 1.11 RIIC Timing (Fast Mode): Changed, figure changed
		54	1.25.1 Code Flash: Description of condition changed
		54, 55	Table 1.13 Programming characteristic: Changed
		56	1.25.2 Data Flash: Description of condition changed
		56	Table 1.15 Programming characteristics: Changed
		58	1.25.3.2 FLSCI3 Interface: Figure changed
		59	1.26 A/D Converter Characteristics: Changed
		63	1.27 Injection Currents: Changed
		63	1.27.1 Absolute Maximum Ratings: Changed
		64	1.27.2 DC Characteristics for Overload Current: Changed
		64	1.27.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin: Changed
1.20	Jun 30, 2015	1	typo (master/a slave → master/slave)
		1,12,28,32	description alignment (MainOsc → MainOSC)
		5,12,13,15,18,22,25,29,30,31,32,33,34,36,37,38,48,51,52,53,54,55,56,58,59,60,61	description alignment (AWOVCL → CAWOVCL, ISOVCL → CISOVCL)
		8	correction , listed Port
		10,11,13,27,28,29,32,33,63	description alignment (IntOsc → IntOSC)
		12	correction of "MainOSC oscillation operation point" level (MIN:2.4->empty, TYP.:empty->0.5xREGVCC)
		12	Addition of "MainOSC oscillation amplitude"
		12	additon precise conditions (such as "Crystal", "Ceramic")
		12	Improvement of figures (MainOSC)
		14	addition of "Conditon for AWOVCL"(empty → AWOVCL pin)
		14	addition of "Conditon for ISOVCL"(empty → ISOVCL pin)
		14	correction of "Equivalent series resistance ..."(for AWO area → for CAWOVCL)
		14	correction of "Equivalent series resistance ..."(for ISO area → for CISOVCL)
		15	VCVML:1.00 → 1.1 (MIN>), 1.05 → 1.15 (TYP.), 1.10 → 1.20 (MAX.)
		15	correction: (Note 1-5) "=" → "-"
		15	description alignment for "Note 5": "=0.02 V/ms to 500 V/ms" → ":0.02 V/ms <= T_{VS} <= < 500 V/ms")
		17	correction of name for REGVCC level (VLVI → VVLVI)
		18,19	correction of Power Up/Down timing (FLMD0 hold time, FLMD0 setup time)
		18,19	case separation for timing whether in serial programming mode or except serial programming mode
		18	removed "FLMD0,1 hold time" spec

Rev.	Date	Description	
		Page	Summary
1.20	Jun 30, 2015	18	changed the condition of RESET edge from rise to fall for "FLMD0 setup time"
		18	changed the unit for "FLMD0 setup time" from "ms" to "us"
		18	removed "Note 2" which explained handling of FLMD0 and FLMD1
		19	correction of description for "Condtion" of t_{DPOR} ("=" → ":")
		20	correction of description for "Condtion" of t_{HPOMD} ("=" → ":")
		20	improvement of figure for mode insertion (VPOC(max.), t_{VS})
		21	Improvement of explanation for "Note 1" (added "include self-programming mode")
		21	addition "V_{IL}" in figure
		22	correction of description for "Condtion" of t_{DPOR} ("=" → ":")
		23	correction, RESET/SHMT2 : with *4 → w/o *4
		23,24	Pin Characteristics table have been updated
		24	correction, "resistor" → "resistors" for Note 1.
		24	addition of "Caution"
		27	description alignment, "Deep STOP" → "DeepSTOP"
		28	description alignment LS-IntOSC → LS IntOSC
		29	description alignment High Speed Internal Oscillator → HS IntOSC Low Speed Internal Oscillator → LS IntOSC
		32	description alignment with another F1x products. separation for high level width and low level width. Addition Note 1 to 4.
		35	addition of t_{WENTIH} , t_{WENTIL}
		29,30,33,34,51, 52	addition for Note 2 (page 29,30,33,51,52), Note 4 (page 34), "Noise such as the figure can be filtered"
		37	changed CSIGnRYO output delay spec
		38	correction of register name which is used as "Condition" CSIHnCTL1.CSIHnDAP → CSIHnCFGx.CSIHnDAP
		38	description alignment of bit number ("CSIHnCFG0-7.CSIHnID2-0" → "CSIHnCFGx.CSIHnID[2:0]") ("CSIHnCFG0-7.CSIHnSP3-0" → "CSIHnCFGx.CSIHnSPx[3:0]") ("CSIHnCFG0-7.CSIHnHD3-0" → "CSIHnCFGx.CSIHnHDx[3:0]")
		38	correction of register name which is used in "CAUTION" CSIHnCFG7-0.CSIHnCKP0-7 → CSIHnCFGx.CSIHnCKPx
		39	changed CSIHnRYO output delay spec
		42	CSSETUP → CSSETUP
		43	CSHOLD → CSHOLD
		48,49	removed "0" as MIN. of RIIC0SCL clock period (Normal Mode) removed "0" as MIN. of RIIC0SCL clock period (Fast Mode)
		55	description alignment 1-pin → 1 pin
		56,58	addition "Note 4. Only for program/erase operation."
		59	removed t_{DPOR}, t_{SMDR}, t_{HMDR}
		59	improvement of time chart
		61	description alignment, "CyclicSTOP" → "Cyclic STOP"
		62	description alignment : (LSB → -)
		63	addition "Note 5", CAUTIONS sentence 2
		64	removed "1.28.1 Equivalent Circuit of the Analog Input Block"
		64	correction of Product Name list and Type
		64	addition of "Note 1" for PgE' and PgB'
		67	addition "1.32 Thermal Characteristics"

Rev.	Date	Description	
		Page	Summary
1.30	Dec 09, 2015	12	addition spec: “V_{MOSCSP}” changed spec :1*3→0.4 x REGVCC - 0.2*3
		12	changed figure: MainOSC: Addition (V_{MOSCSP})
		15	addition of Note 8 for Detection voltage
		18	removed FLMD0 setup time
		18	addition of Note 2 for figure
		24	correction, P10_11 to P11_1,P11_4/Drive Strength : "Slow/Fast" → "Slow"
		63	correction of CAUTION
		68	description alignment of header "Parameter" → "Symbol"
1.31	Apr 20, 2016	14	addition of Note 3 of 1.8.1 Regulator Characteristics
		18	correction of Note 2 in 1.8.3 Power Up/Down Timing
		61	correction of ADCLKn spec in 1.26 A/D Converter Characteristics
		63	correction of caution of 1.26 A/D Converter Characteristics

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