Product Introduction

Concept

The RH850/F1x microcontroller focus on low power and low cost for the body application.

The device is a high-end microcontroller with a 32-bit RH850G3M core for car body control. The features of this device are the low power consumption, the high processing power and the variable peripheral function.

In particular, Low power consumption is achieved by supporting wide stand-by control and the power supply insulation using the port polling, stand-by control of A/D conversion and LIN communication which considered body control application.

This device supports the security and safety function. And the local area network has been strengthened by upgrading each module of CAN, LIN master/slave.

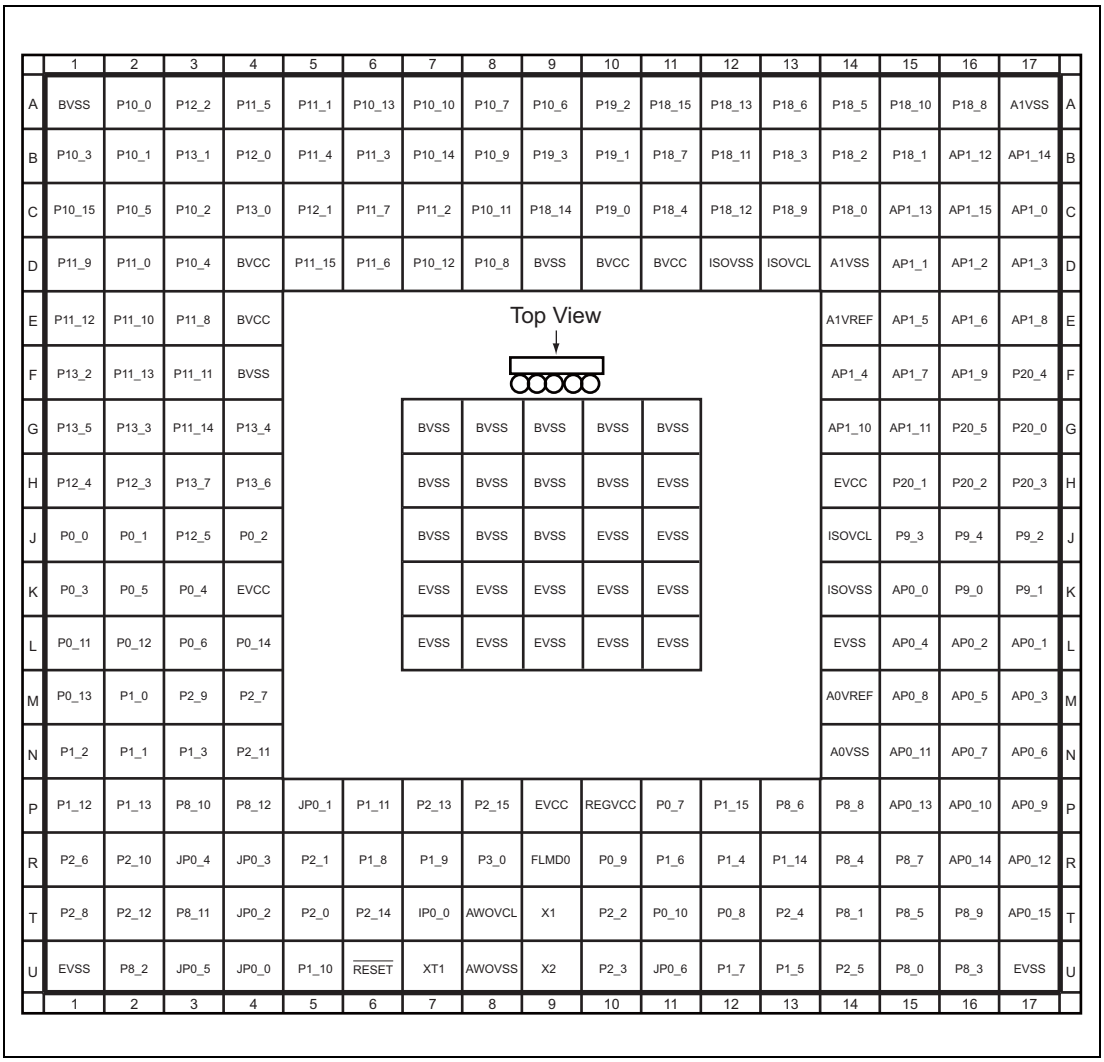
Function overview

Refer to the *RH850/F1M User's manual: Hardware*.

Block diagram

Refer to the *RH850/F1M User's manual: Hardware*.

Pin map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	BVSS	P10_0	P12_2	P11_5	P11_1	P10_13	P10_10	P10_7	P10_6	P19_2	P18_15	P18_13	P18_6	P18_5	P18_10	P18_8	A1VSS	A
B	P10_3	P10_1	P13_1	P12_0	P11_4	P11_3	P10_14	P10_9	P19_3	P19_1	P18_7	P18_11	P18_3	P18_2	P18_1	AP1_12	AP1_14	B
C	P10_15	P10_5	P10_2	P13_0	P12_1	P11_7	P11_2	P10_11	P18_14	P19_0	P18_4	P18_12	P18_9	P18_0	AP1_13	AP1_15	AP1_0	C
D	P11_9	P11_0	P10_4	BVCC	P11_15	P11_6	P10_12	P10_8	BVSS	BVCC	BVCC	ISOVSS	ISOVCL	A1VSS	AP1_1	AP1_2	AP1_3	D
E	P11_12	P11_10	P11_8	BVCC										A1VREF	AP1_5	AP1_6	AP1_8	E
F	P13_2	P11_13	P11_11	BVSS										AP1_4	AP1_7	AP1_9	P20_4	F
G	P13_5	P13_3	P11_14	P13_4				BVSS	BVSS	BVSS	BVSS	BVSS		AP1_10	AP1_11	P20_5	P20_0	G
H	P12_4	P12_3	P13_7	P13_6				BVSS	BVSS	BVSS	BVSS	EVSS		EVCC	P20_1	P20_2	P20_3	H
J	P0_0	P0_1	P12_5	P0_2				BVSS	BVSS	BVSS	EVSS	EVSS		ISOVCL	P9_3	P9_4	P9_2	J
K	P0_3	P0_5	P0_4	EVCC				EVSS	EVSS	EVSS	EVSS	EVSS		ISOVSS	AP0_0	P9_0	P9_1	K
L	P0_11	P0_12	P0_6	P0_14				EVSS	EVSS	EVSS	EVSS	EVSS		EVSS	AP0_4	AP0_2	AP0_1	L
M	P0_13	P1_0	P2_9	P2_7										A0VREF	AP0_8	AP0_5	AP0_3	M
N	P1_2	P1_1	P1_3	P2_11										A0VSS	AP0_11	AP0_7	AP0_6	N
P	P1_12	P1_13	P8_10	P8_12	JP0_1	P1_11	P2_13	P2_15	EVCC	REGVCC	P0_7	P1_15	P8_6	P8_8	AP0_13	AP0_10	AP0_9	P
R	P2_6	P2_10	JP0_4	JP0_3	P2_1	P1_8	P1_9	P3_0	FLMD0	P0_9	P1_6	P1_4	P1_14	P8_4	P8_7	AP0_14	AP0_12	R
T	P2_8	P2_12	P8_11	JP0_2	P2_0	P2_14	IP0_0	AWOVCL	X1	P2_2	P0_10	P0_8	P2_4	P8_1	P8_5	P8_9	AP0_15	T
U	EVSS	P8_2	JP0_5	JP0_0	P1_10	$\overline{\text{RESET}}$	XT1	AWOVSS	X2	P2_3	JP0_6	P1_7	P1_5	P2_5	P8_0	P8_3	EVSS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 1.1 Pin Connection Diagram (233 pin FPBGA)

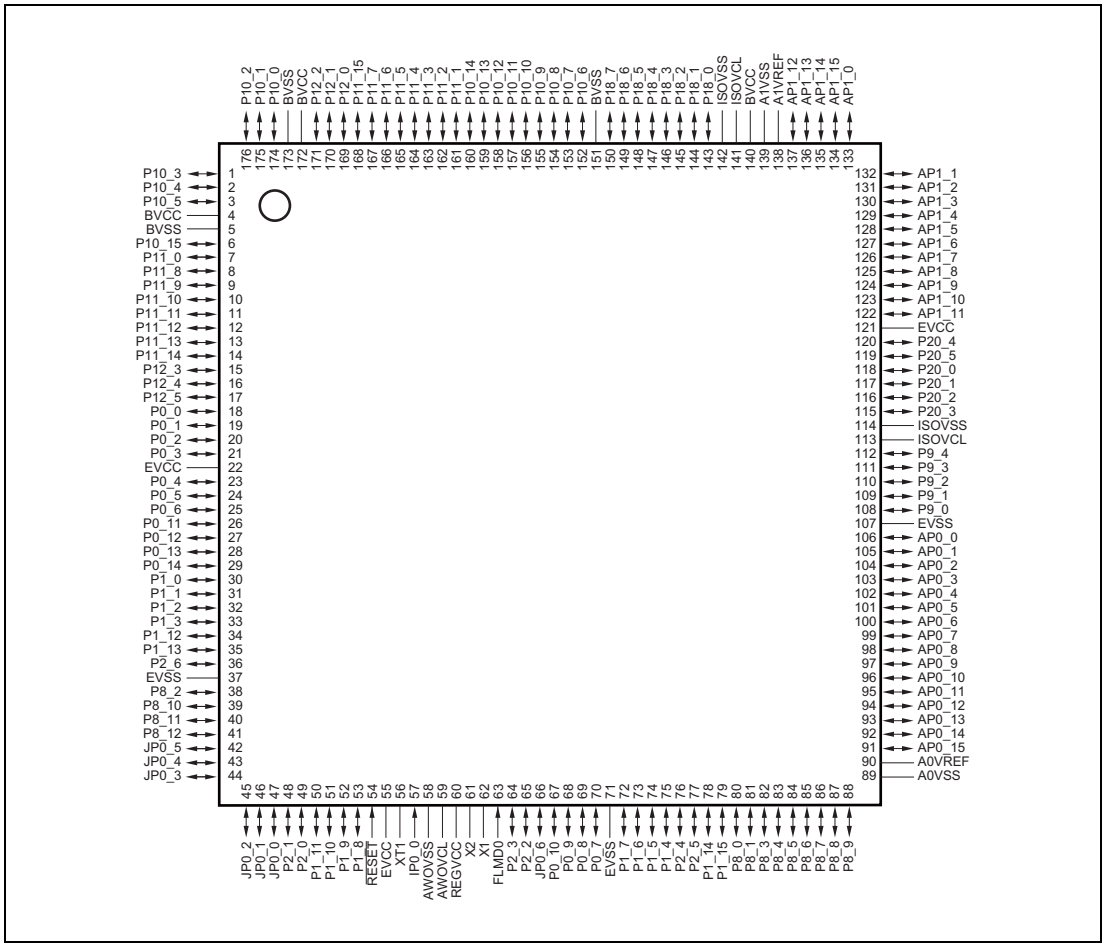


Figure 1.2 Pin Connection Diagram (176 pin LQFP)

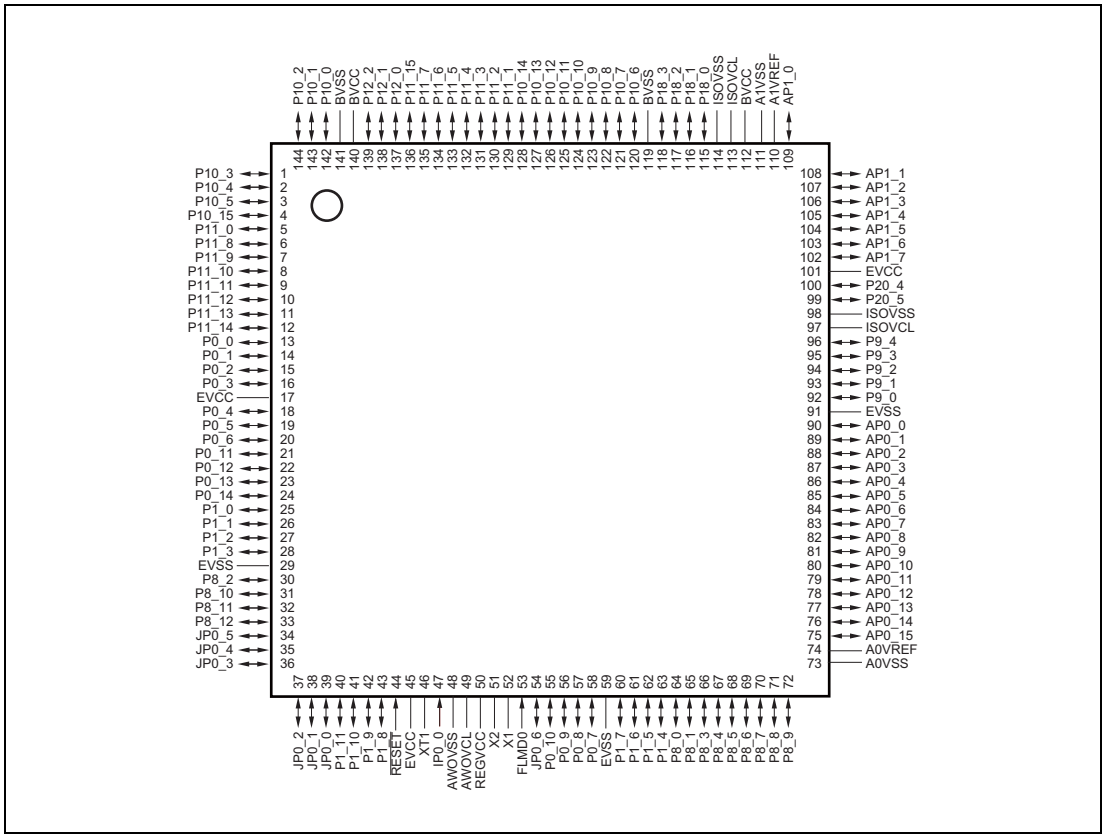


Figure 1.3 Pin Connection Diagram (144 pin LQFP)

Product Lineup

Pin Count	Memory					ICUS	CAN Interface	Product Name		Line Name
		CPU1 (Core #1)	Global Memory					Operating Temperature (Ta)		
	Code Flash	Local RAM	Data Flash	Global RAM	Retention RAM (RRAM)			–40°C to +105°C	–40°C to +125°C	
144 pin	3 MB	192 KB	64 KB	Not provided	64 KB	Not provided	RS-CAN	R7F7015443AFP	R7F7015444AFP	ECO
	4 MB	256 KB	64 KB	Not provided	64 KB	Not provided	RS-CAN	R7F7015453AFP	R7F7015454AFP	ECO
176 pin	3 MB	192 KB	64 KB	Not provided	64 KB	Not provided	RS-CAN	R7F7015483AFP	R7F7015484AFP	ECO
	4 MB	256 KB	64 KB	Not provided	64 KB	Not provided	RS-CAN	R7F7015493AFP	R7F7015494AFP	ECO
233 pin	3 MB	192 KB	64 KB	Not provided	64 KB	Not provided	RS-CAN	R7F7015523ABG	R7F7015524ABG	ECO
	4 MB	256 KB	64 KB	Not provided	64 KB	Not provided	RS-CAN	R7F7015533ABG	R7F7015534ABG	ECO
144 pin	3 MB	192 KB	64 KB	Not provided	64 KB	ICUSC	RS-CAN	R7F7015643AFP	R7F7015644AFP	ADVANCED
	4 MB	256 KB	64 KB	Not provided	64 KB	ICUSC	RS-CAN	R7F7015653AFP	R7F7015654AFP	ADVANCED
176 pin	3 MB	192 KB	64 KB	Not provided	64 KB	ICUSC	RS-CAN	R7F7015683AFP	R7F7015684AFP	ADVANCED
	4 MB	256 KB	64 KB	Not provided	64 KB	ICUSC	RS-CAN	R7F7015693AFP	R7F7015694AFP	ADVANCED
233 pin	3 MB	192 KB	64 KB	Not provided	64 KB	ICUSC	RS-CAN	R7F7015723ABG	R7F7015724ABG	ADVANCED
	4 MB	256 KB	64 KB	Not provided	64 KB	ICUSC	RS-CAN	R7F7015733ABG	R7F7015734ABG	ADVANCED

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj (**Section 1.2.4, Temperature Condition**) and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Section 1 Electrical Specifications

1.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

1.1.1 Pin Groups

1.1.1.1 233 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P3, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P13, P18, P19
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

1.1.1.2 176 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P2, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P18
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

1.1.1.3 144 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
PgR	REGVCC, AWOVSS	X1, X2, XT1, XT2/IP0_0
PgE	EVCC, EVSS	Related ports: JP0, P0, P1, P8, P9, P20 Related pins: $\overline{\text{RESET}}$, FLMD0
PgB	BVCC, BVSS	Related ports: P10, P11, P12, P18
PgA0	A0VREF, A0VSS	Related port: AP0
PgA1	A1VREF, A1VSS	Related port: AP1

1.1.2 General Measurement Conditions

1.1.2.1 Common Conditions

Power supply

- REGVCC = EVCC = VPOC*1 to 5.5 V
- BVCC = VPOC*1 to REGVCC
- A0VREF = 3.0 V to 5.5 V
- A1VREF = 3.0 V to 5.5 V
- AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Capacitance on internal regulator

- CAWOVCL: 0.1 µF ±30%
- CISOVCL: 0.1 µF ±30% per pin
- Operating temperature
  - Ta:
    –40 to (depend on the product)°C
  - Tj:
    R7F7015xx3AFP: –40 to 130°C
    R7F7015xx4AFP: –40 to 150°C
    R7F7015xx3ABG: –40 to 130°C
    R7F7015xx4ABG: –40 to 150°C

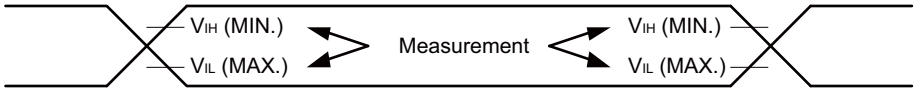
Load conditions

- CL = 30 pF

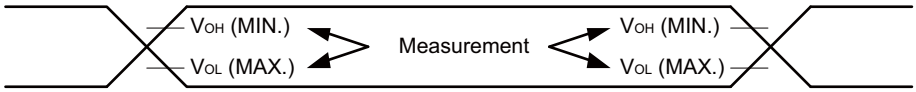
Note 1. “VPOC” means POC (power on clear) detection voltage. For more detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

1.1.2.2 AC Characteristic Measurement Condition

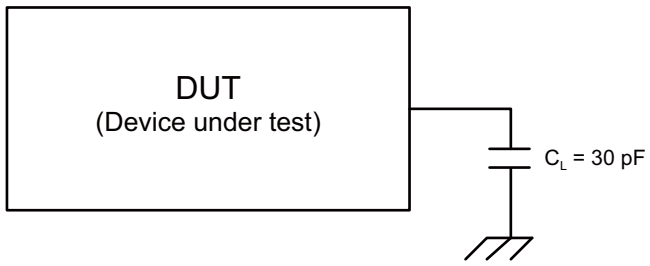
AC test input measurement points



AC test output measurement points



Load conditions



CAUTION

If the load capacitance exceeds 30 pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance till less than 30 pF.

1.2 Absolute Maximum Ratings

CAUTIONS

1. **Do not directly connect the output (or input/output) pins to each other, power supply and ground.**
2. **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
3. **When designing an external circuit ensure that the connections do not conflict with the port state of this device.**

1.2.1 Supply Voltages

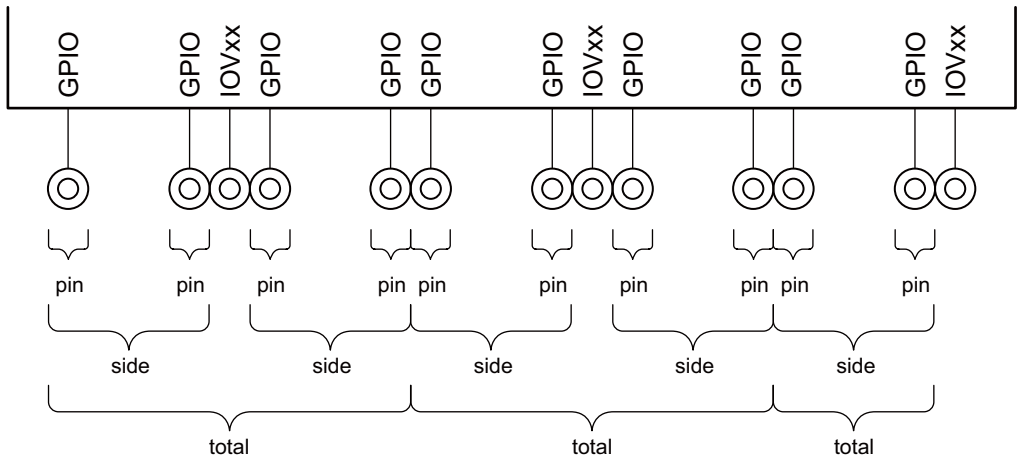
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	BVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
	BVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A1VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V
	A1VSS		–0.5		0.5	V

1.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR	VI		–0.5		REGVCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgB			–0.5		BVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V
	PgA1			–0.5		A1VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.2.3 Port Current



Definition of the condition

- **Per pin:** Output current of one GPIO
- **Per side:** Total output current of all GPIO pins on one side of one IOVxx
- **Total:** Total output current of both sides of one IOVxx

Note:

- **GPIO:** General-purpose I/O pin (JP0, P0, P1, P2, P3, P8, P9, P10, P11, P12, P13, P18, P19, P20, AP0, AP1)
- **IOVxx:** Power supply pin for I/O pins (EVCC/EVSS, BVCC/BVSS, A0VREF/A0VSS, A1VREF/A1VSS)

1.2.3.1 233 pin

Table 1.1 Port Current (233 pin) (1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P18_0 to P18_7)			–48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			–48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

Table 1.1 Port Current (233 pin) (2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2 to P2_3)			48	mA
			Per side (total of P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			48	mA
			Total (EVCC)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P18_8 to P18_15, P19_0 to P19_3)			48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7)			48	mA
			Total (BVCC)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VREF)			48	mA

1.2.3.2 176 pin

Table 1.2 Port Current (176 pin) (1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P10_6 to P10_9, P18_0 to P18_7)			–48	mA
			Per side (total of P10_10 to P10_14, P11_1 to P11_7, P11_5, P12_0 to P12_2)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

Table 1.2 Port Current (176 pin) (2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_0 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P2_2 to P2_3)			48	mA
			Per side (total of P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_7)			48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5)			48	mA
			Total (BVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VSS)			48	mA

1.2.3.3 144 pin

Table 1.3 Port Current (144 pin) (1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0 to P9_4, P20_4 to P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2, P1_8 to P1_11)			–48	mA
			Per side (total of JP0_6, P0_7 to P0_10, P1_4 to P1_7, P8_0 to P8_1, P8_3 to P8_9)			–48	mA
			Total (EVCC)			–60	mA
		PgB	Per pin			–10	mA
			Per side (total of P10_6 to P10_9, P18_0 to P18_3)			–48	mA
			Per side (total of P10_10 to P10_14, P11_1 to P11_7, P11_5, P12_0 to P12_2)			–48	mA
			Per side (total of P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_14)			–48	mA
			Total (BVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
		PgA1	Per pin			–10	mA
			Total (A1VREF)			–48	mA

Table 1.3 Port Current (144 pin) (2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0 to P9_4, P20_4 to P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3)			48	mA
			Per side (total of JP0_0 to JP0_5, P1_8 to P1_11, P8_2, P8_10 to P8_12)			48	mA
			Per side (total of JP0_6, P0_7 to P0_10)			48	mA
			Per side (total of P1_4 to P1_7, P8_0 to P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgB	Per pin			10	mA
			Per side (total of P18_0 to P18_3)			40	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_2)			48	mA
			Per side (total of P11_3 to P11_7, P11_15, P12_0 to P12_2)			48	mA
			Per side (total of P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_14)			48	mA
			Total (BVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA
		PgA1	Per pin			10	mA
			Total (A1VSS)			48	mA

1.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		170	°C
Junction temperature	Tj	R7F7015xx3AFP R7F7015yy3ABG	–40		130	°C
		R7F7015xx4AFP R7F7015yy4ABG	–40		150	°C

xx = 44, 45, 48, 49, 64, 65, 68, 69
yy = 52, 53, 72, 73

Regarding operation temperature of each product, refer to **Product Lineup**.

1.3 Capacitance

Condition: REGVCC = EVCC = BVCC = A0VREF = A1VREF = AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz 0 V for non measurement pins			10	pF
Input/Output capacitance	CIO*2				10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

1.4 Operational Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK}	PLL mode (Fixed frequency mode) SSCG mode (Dithered frequency mode)			120	MHz
Peripheral clock frequency	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
	f_{CKSCLK_ARTCA}	for RTCA0			4	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_AFOUT}	for CSCXFOUT			30	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
		for ENCA0				
		for TAPA				
		for PIC				
	f_{CKSCLK_IPERI2}	for TAUBn			60	MHz
		for PWM-diag				
	f_{CKSCLK_ILIN}	for RLIN2n			60	MHz
		for RLIN3n				
	f_{CKSCLK_AADCA}	for ADCA1			40	MHz
	f_{CKSCLK_ICAN}	for RS-CANn (pclk)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RS-CANn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIGn			80	MHz
		for CSIHn				
	f_{RL}	for WDTA1			240*2	kHz
	$f_{CPUCLK2}$	for FLXA (hclk)			60	MHz
		for OSTMn				
		for MEMC*4				
	$f_{PPLLCLK}$	for FLXA (clkc)			80	MHz
	$f_{CPUCLK4}$	for RIIC			30	MHz
	f_{EMCLK}	for LPS			8	MHz
Power supply range	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	BVCC		VPOC*3		REGVCC	V
	A0VREF		3.0		5.5	V
	A1VREF					

Note 1. For clock specification of peripherals, refer to *Section 11, Clock Controller*, in the *RH850/F1M Group User's Manual: Hardware*.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on). For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**. In addition, the guaranteed operation in DC characteristic. And AC characteristic is guaranteed when more than 3.0 V. When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

Note 4. Devided by 2 on MEMC internal.

1.5 Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC}	Crystal/Ceramic	8		24	MHz
MainOSC Current consumption	I_{MOSC}	After stabilization		1.9*3	2.3*3	mA
MainOSC oscillation start point	V_{MOSCSP}	Crystal/Ceramic	VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}			0.5 x REGVCC*3		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$	Crystal/Ceramic	0.4 x REGVCC–0.2*3			V
MainOSC oscillation stabilization time	t_{MSTB}			*1		ms
SubOSC frequency	f_{SOSC}	Crystal	30	32.768	38	kHz
SubOSC Current consumption	I_{SOSC}	After stabilization		1.5*3	4*3	µA
SubOSC DC operating point	$V_{SOSCDCOP}$			0.65*3		V
SubOSC oscillation stabilization time	t_{SSTB}			*2		s

Note 1. Oscillator stabilization time is time until being set ("1") in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written "1", and depends on the setting value of MOSCST register and EMCLK (8 MHz/240 kHz). Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

Note 2. Oscillator stabilization time is time until being set ("1") in SOSCS.SOSCCLKACT bit after SOSCE.SOSCENTRG bit is written "1", and depends on the setting value of SOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

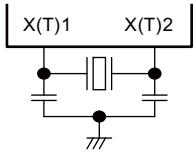
Note 3. This is reference value.

CAUTION

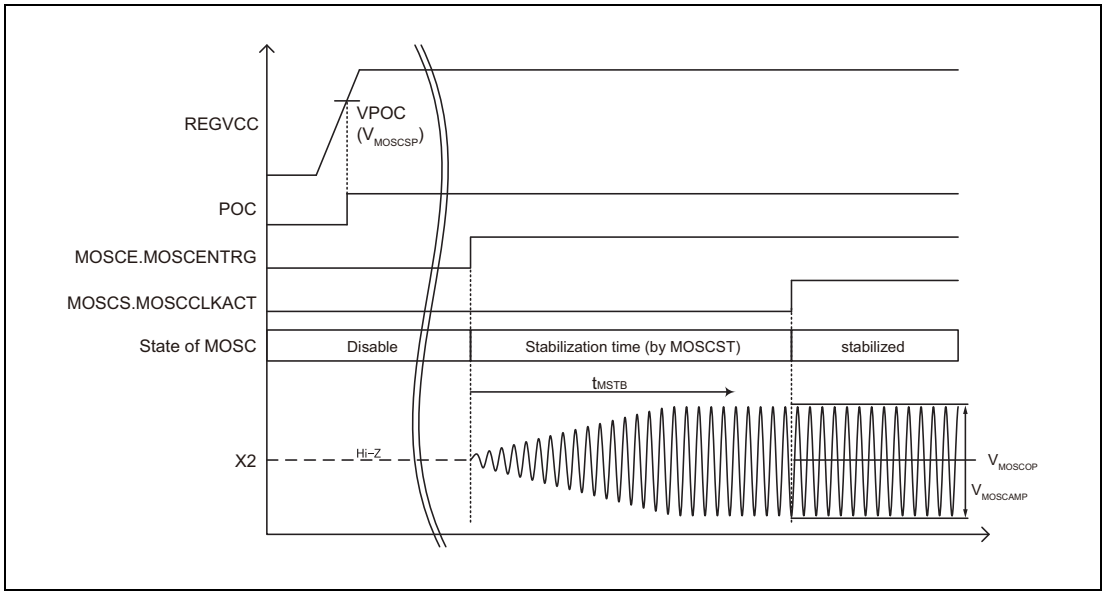
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

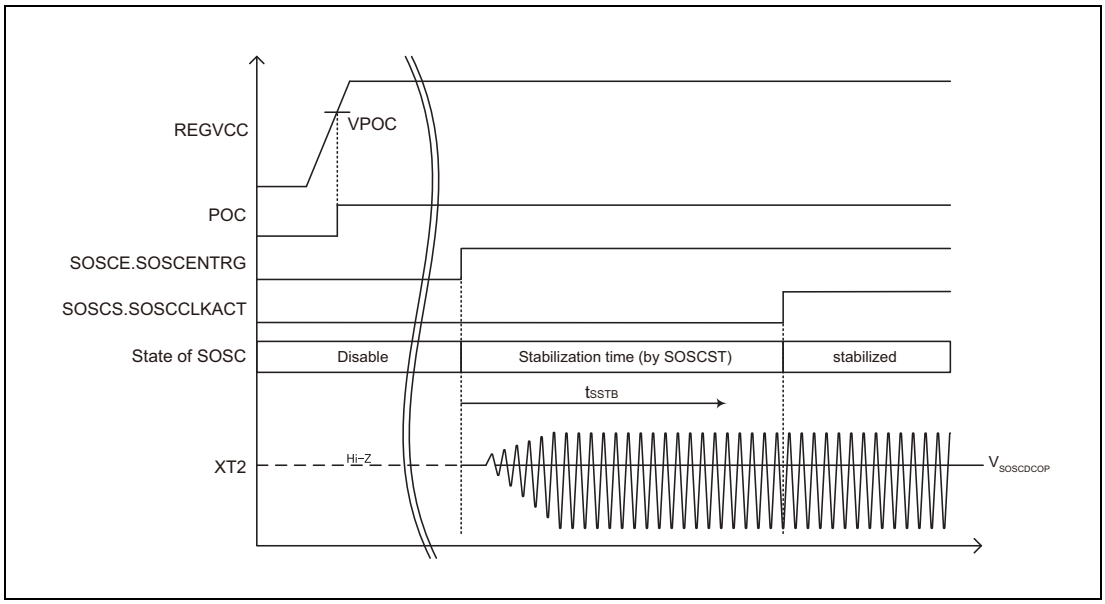
Recommended oscillator circuit is shown below.



MainOSC



SubOSC



1.6 Internal Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency	f_{RH}		7.36	8	8.64	MHz
		Ta = 25°C	7.6	8	8.4	MHz
HS IntOSC Current consumption	I_{RH}	After stabilization			25*1	µA
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	µs

Note 1. This is reference value.

1.7 PLL Characteristics

1.7.1 PLL0 (for CPU) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input frequency	$f_{SSCGICLK}$			8		24	MHz
Output frequency	f_{SSCGP}	PLL mode		25		120	MHz
	f_{SSCGS}	SSCG mode		25		120	MHz
Modulation frequency	f_{MOD}			20		100	kHz
Frequency dithering range*4	f_{DIT}			±0.82	±1.0	±1.18	%
				±1.64	±2.0	±2.36	%
				±2.46	±3.0	±3.54	%
				±3.28	±4.0	±4.72	%
				±4.1	±5.0	±5.9	%
Output period jitter*1	t_{CPJS}	pr = 4*2		–150		150	ps
		pr = 8*2		–200		200	ps
		pr = 16*2		–300		300	ps
Lock time*3	t_{LCKSP}	PLL mode	PLL0ST = 0000 $0AA0_H$	314.9	340	369.6	µs
	t_{LCKS}	SSCG mode	PLL0ST = 0000 $1B80_H$	814.9	880	956.6	µs

Note 1. This is reference value.

Note 2. The following parameters are set by PLL0C register.
- pr: PLL0C.PLL0P2 to 0 bits

Note 3. Lock time is time until being set (“1”) in PLL0S.PLL0CLKACT bit after PLL0E.PLL0ENTRG bit is written “1”.

Note 4. “Frequency dithering range” is set by PLL0ADJ[2:0] bits of PLL0C registers.

1.7.2 PLL1 (for Peripheral) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLLICLK}$			8		24	MHz
Output frequency	f_{PLL}			25		80	MHz
Output period jitter*1	t_{CPJP}	PLLC.OUTBSEL = 0	par = 4*2	–150		150	ps
			par = 6*2[($f_{PLLICLK}$/mr × nr) = 480 MHz]	–150		150	ps
			par = 6*2[($f_{PLLICLK}$/mr × nr) < 480 MHz]	–200		200	ps
			par = 8*2	–250		250	ps
			par = 16*2	–300		300	ps
		PLLC.OUTBSEL = 1	($f_{PLLICLK}$/mr × nr) = 480 MHz	–150		150	ps
			($f_{PLLICLK}$/mr × nr) < 480 MHz	–200		200	ps
Long term jitter*1	t_{LTJ}		term = 1 µs	–500		500	ps
			term = 10 µs	–1		1	ns
			term = 20 µs	–2		2	ns
Lock time*3	t_{LCKP}			104.0	112.3	122.1	µs

Note 1. This is reference value.

Note 2. The following parameters are set by PLL1C register.
- par: PLL1C.PA2-0 bits
- mr: PLL1C.M1-0 bits
- nr: PLL1C.N5-0 bits

Note 3. Lock time is time until being set (“1”) in PLL1S.PLL1CLKACT bit after PLL1E.PLL1ENTRG bit is written “1”.

1.8 Power Management Characteristics

1.8.1 Regulator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		5.5	V
Normal operation voltage	V_{OP}	AWOVCL pin, ISOVCL pin	1.10	1.25	1.35	V
Limited operation voltage	V_{LOP}	AWOVCL pin, ISOVCL pin	1.35		1.43*3	V
Regulator output voltage	V_{RO}	AWOVCL pin, ISOVCL pin	1.15	1.25	1.35	V
Output voltage	AWOVCL	AWOVCL pin	1.1	1.25	1.35	V
	ISOVCL	ISOVCL pin	1.1	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.1	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.1	0.13	µF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40*2	mΩ
	RVRISO	for CISOVCL			40*2	mΩ
Inrush current during power-on					200*2	mA

Note 1. “VPOC” means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on).
For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

Note 2. This is reference value.

Note 3. Reliability restrictions from 1.35 V to 1.43 V.

1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

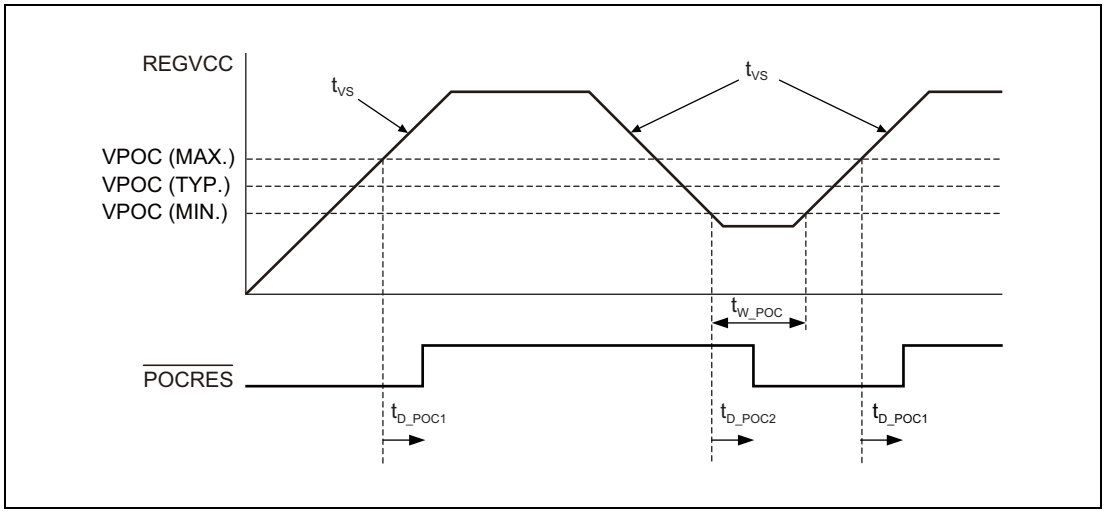
Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Detection voltage (REGVCC)	VPOC	POC	At power-on (Rise)		2.8	2.95	3.1	V
			After power-on (Fall)		2.8	2.9	3.0	V
	VLVI0	LVI	Rise		3.87	4.0	4.13	V
			Fall		3.9	4.0	4.1	V
	VLVI1		Rise		3.57	3.7	3.83	V
			Fall		3.6	3.7	3.8	V
	VLVI2		Rise		3.37	3.5	3.63	V
			Fall		3.4	3.5	3.6	V
	VVLVI	VLVI			1.8	1.9	2.0	V
Detection voltage (AWOVCL, ISOVCL)	VCVMH	CVM	High voltage		1.40	1.50	1.60	V
	VCVML*8		Low voltage		1.1	1.15	1.20	V
Response time	t_{D_POC1}*6	POC	At power-on (Rise)	*1			2	ms
				*2			6.3	ms
			After power-on (Rise)	*3			2	ms
				*4			5	ms
	t_{D_POC2}*7		After power-on (Fall)	*5			5	µs
	t_{D_LVI}	LVI					2	ms
	t_{D_VLVI}	VLVI		*3			2	ms
				*4			5	ms
	t_{D_CVM}	CVM			0.2		10	µs
Setup time	t_{S_LVI}	LVI	LVICNT0,1 bits are set to 1 (except 00_B), then LVI is ready to operate				80	µs
REGVCC minimum width	t_{W_POC}	POC			0.2			ms
	t_{W_LVI}	LVI			0.2			ms
	t_{W_VLVI}	VLVI			0.2			ms

Note 1. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms
Note 2. Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms
Note 3. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms
Note 4. Voltage slope (t_{VS}): 20 V/ms < t_{VS} ≤ 500 V/ms
Note 5. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.
Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.
Note 8. The CVM monitors the internal voltage regulator output to ensure that AWOVCL/ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage AWOVCL or ISOVCL outside the specified level of VCVMH and VCVML is not ensured by CVM.

<POC>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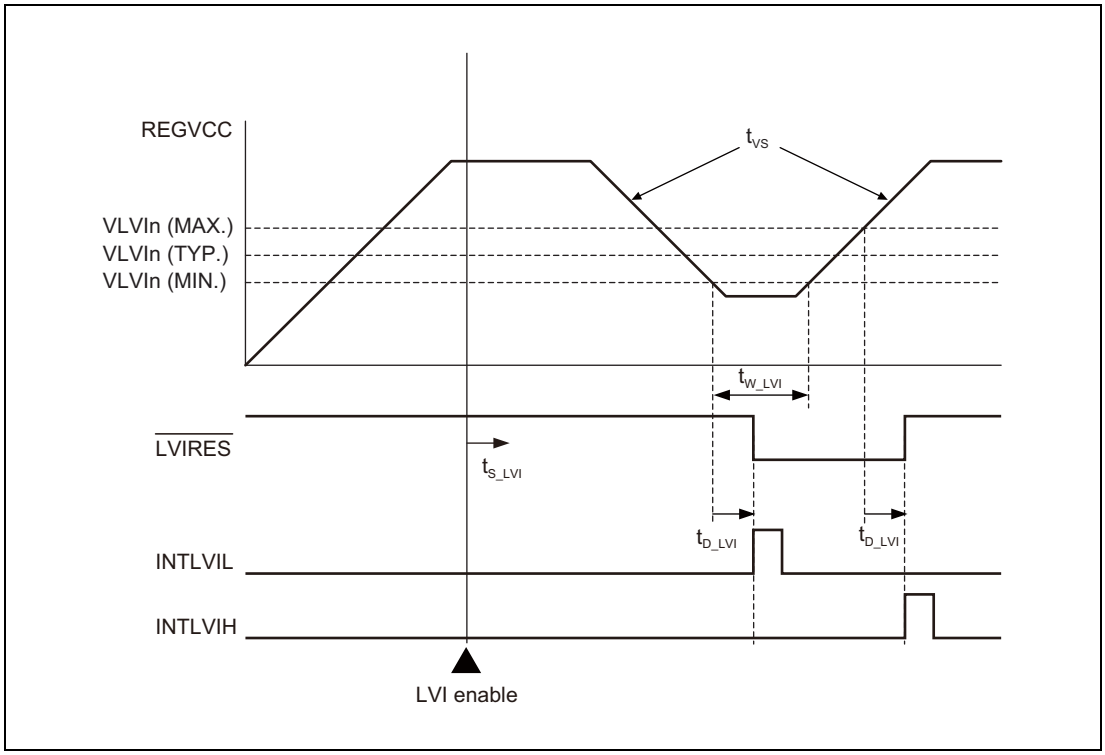
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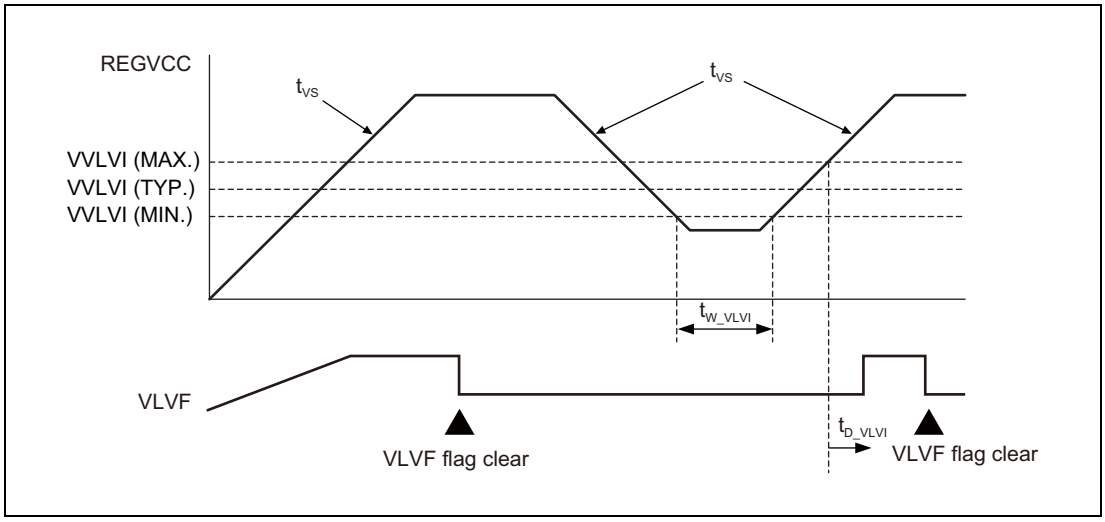
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VLVF flag clear

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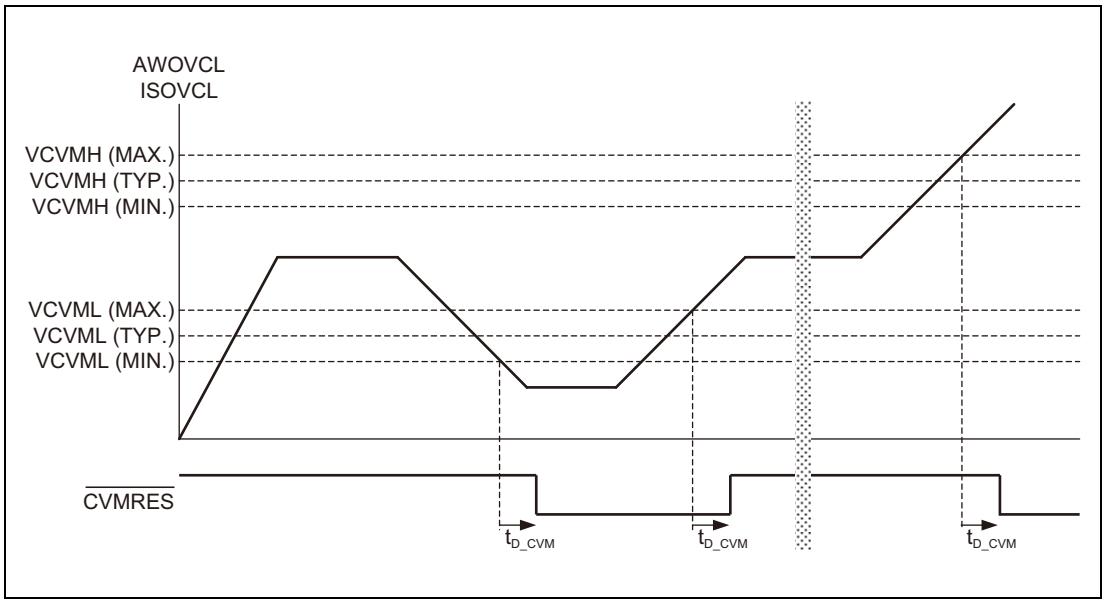
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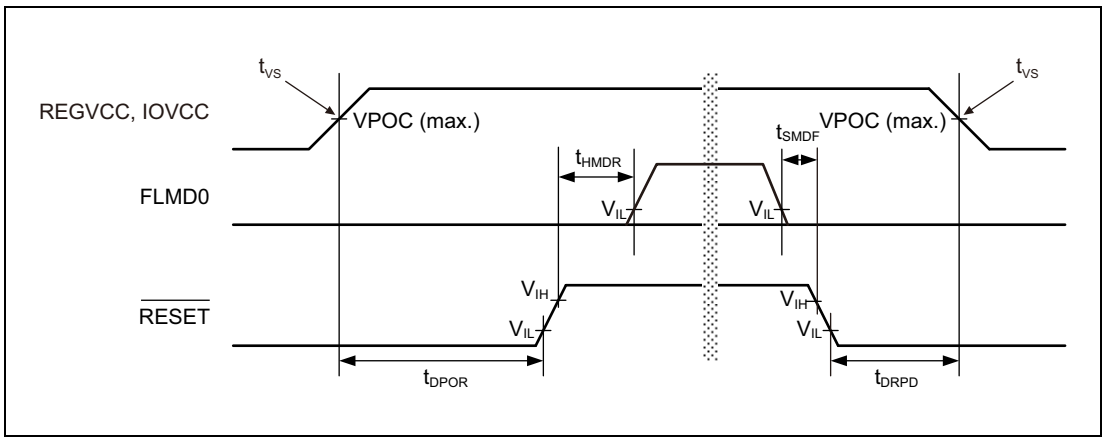
VCVMH (TYP.)
VCVMH (MIN.)
VCVML (MAX.)
VCVML (TYP.)
VCVML (MIN.)
CVMRES
tD_CVM
tD_CVM
tD_CVM

1.8.3 Power Up/Down Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Table 1.4 In case the $\overline{\text{RESET}}$ pin is used (except Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↓)	t_{SMDF}		0*2			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

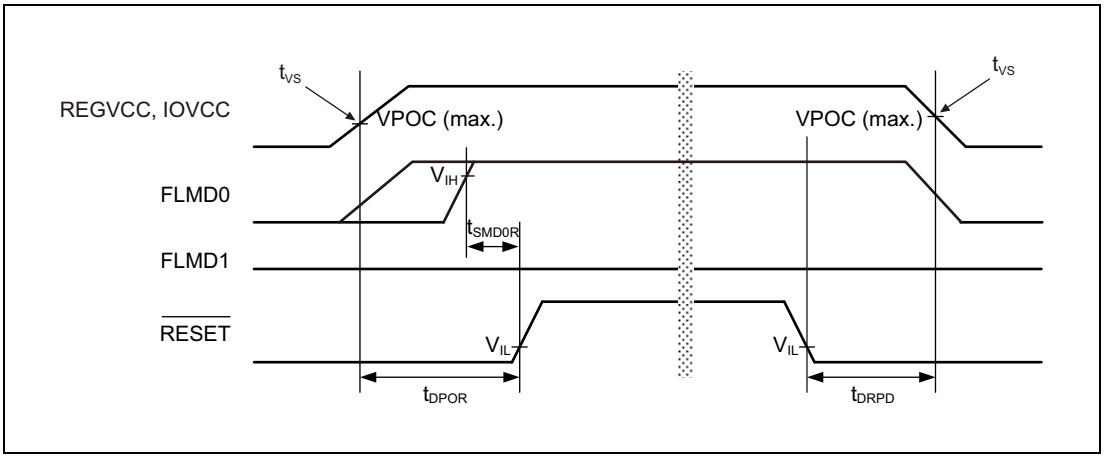
Note 2. When the $\overline{\text{RESET}}$ and FLMD0 pin input low level at same time (t_{SMDF} = 0µs) in the device entries on-chip debug mode and operates self-programming, following pins have a possibility to unstable level output for less than 23ns.

JP0_6, P10_0, P0_0, P10_5, P8_1

So, when the device was used in the device entries on-chip debug mode and operates self-programming, please input low level in FLMD0 before $\overline{\text{RESET}}$ pin input.

Table 1.5 In case the $\overline{\text{RESET}}$ pin is used (for Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

Table 1.6 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0, FLMD1, MODE0, MODE1setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMDR}		1			ms
$\overline{\text{RESET}}$ ↓ to REGCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ ↑)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ ↓)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC, BVCC, A0VREF and A1VREF.

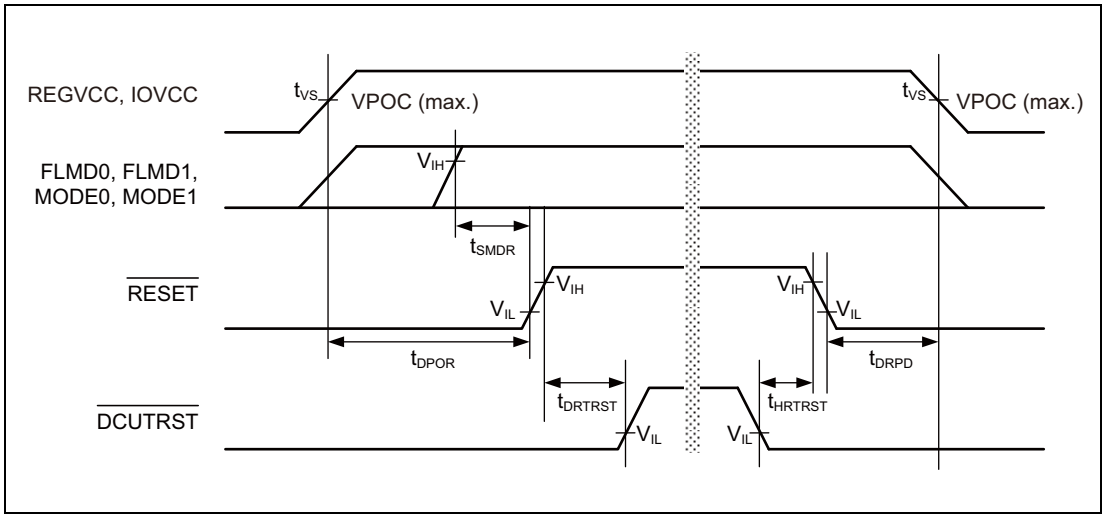
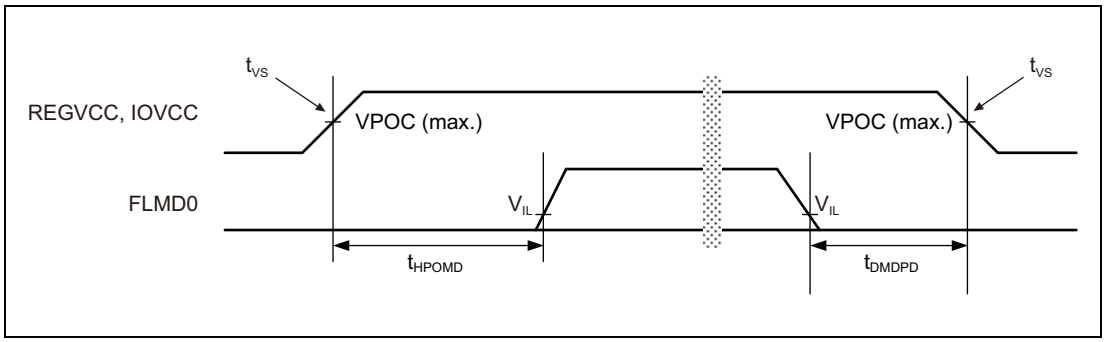


Table 1.7 In case the $\overline{\text{RESET}}$ pin is not used and fixed to high level by pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*2 ↑ to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 ↓ to REGVCC ↓ and IOVCC*2 ↓ delay time	t_{DMDPD}		1			µs

Note 1. This operating condition is available only in normal operation mode (include self-programming mode). When the device is used in except single chip mode, please use the $\overline{\text{RESET}}$ pin.

Note 2. IOVCC means EVCC, BVCC, A0VREF and A1VREF.



1.8.4 CPU Reset Release Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Table 1.8 In case the $\overline{\text{RESET}}$ pin is not used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}) : 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms			2.58	ms
		Voltage slope (t_{VS}) : 0.5 V/ms < t_{VS} ≤ 500 V/ms			8.38	ms

Note 1. This is reference value.

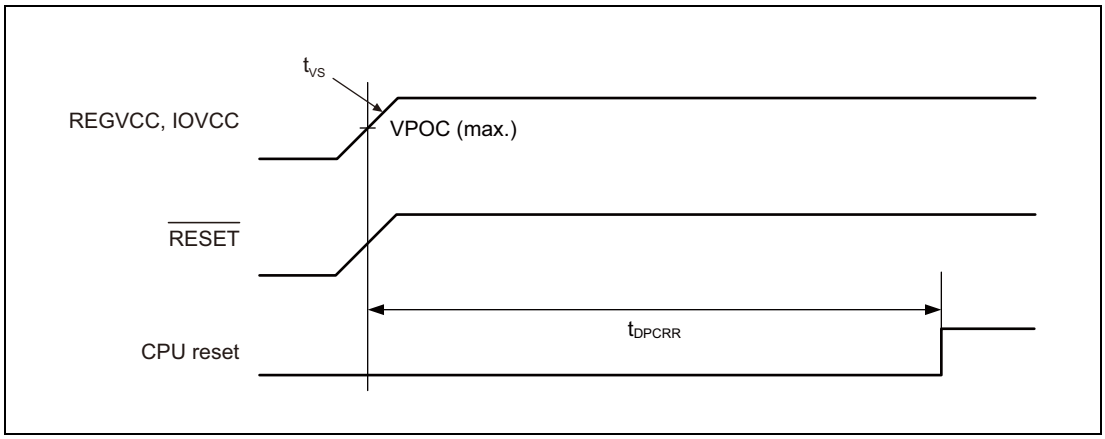
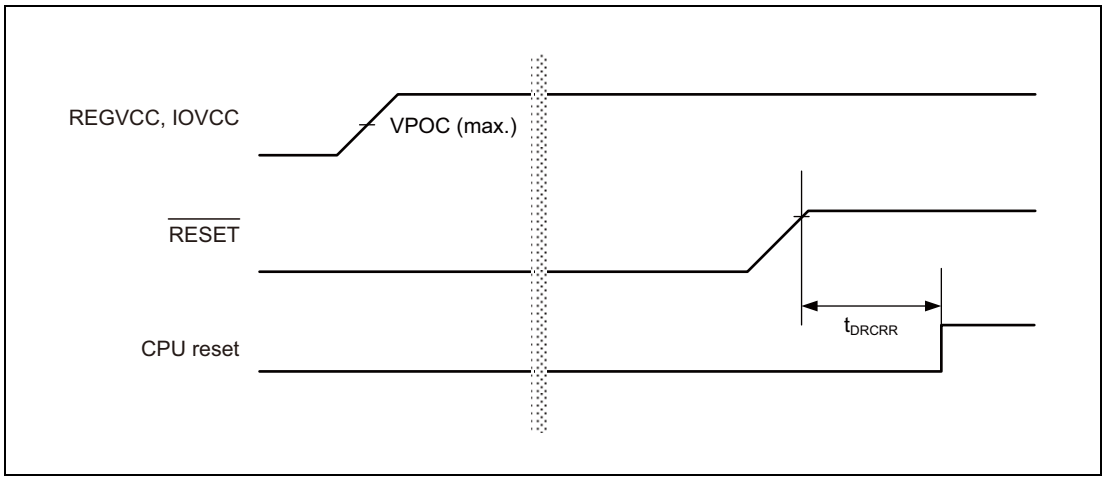


Table 1.9 In case the $\overline{\text{RESET}}$ pin is used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				14*2	ms

Note 1. This is reference value.

Note 2. At least t_{DPCRR} time is necessary reaching from VPOC (max) even if power up sequence is kept shown on **Section 1.8.3, Power Up/Down Timing**.



1.9 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

(1/5)

Pin Name	144 pin	176 pin	233 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
$\overline{\text{RESET}}$	√	√	√	—	—	√	—	—	—	—	—	—*4
FLMD0	√	√	√	—	√	—	—	—	—	—	√	√
IP0_0	√	√	√	—	—	—	—	—	—	—	—	—
JP0_0	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_1	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
JP0_2	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_3	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_4	√	√	√	—	—	—	√	√	—	Slow	√	√
JP0_5	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
JP0_6	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P0_0	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_1	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_2	√	√	√	—	√	—	√	—	—	Slow/Fast*2	√	√
P0_3	√	√	√	—	√	—	√	—	—	Slow/Fast*2	√	√
P0_4	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_5	√	√	√	—	√	—	√	—	—	Slow/Fast*3	√	√
P0_6	√	√	√	—	√*1	—	√	—	—	Slow/Fast*3	√	√
P0_7	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P0_8	√	√	√	—	—	—	√	—	—	Slow	√	√
P0_9	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_10	√	√	√	—	—	—	√	—	—	Slow	√	√
P0_11	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_12	√	√	√	—	√	—	√	—	—	Slow	√	√
P0_13	√	√	√	—	√	—	√	—	—	Slow/Fast	√	—
P0_14	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P1_0	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_1	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_2	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_3	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_4	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_5	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_6	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_7	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_8	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_9	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_10	√	√	√	—	√	—	√	—	—	Slow	√	—
P1_11	√	√	√	—	—	—	√	—	—	Slow	√	—
P1_12	—	√	√	—	√	—	√	—	—	Slow	√	—
P1_13	—	√	√	—	—	—	√	—	—	Slow	√	—
P1_14	—	√	√	—	√	—	√	—	—	Slow	√	—
P1_15	—	√	√	—	—	—	√	—	—	Slow	√	—

(2/5)

Pin Name	144 pin	176 pin	233 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P2_0	—	√	√	—	√	—	√	—	—	Slow	√	—
P2_1	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_2	—	√	√	—	√	—	√	—	—	Slow	√	—
P2_3	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_4	—	√	√	—	√	—	√	—	—	Slow	√	—
P2_5	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_6	—	√	√	—	—	—	√	—	—	Slow	√	—
P2_7	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_8	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_9	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_10	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_11	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_12	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_13	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_14	—	—	√	—	—	—	√	—	—	Slow	√	—
P2_15	—	—	√	—	—	—	√	—	—	Slow	√	—
P3_0	—	—	√	—	—	—	√	—	—	Slow	√	—
P8_0	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_1	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_2	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_3	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_4	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_5	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_6	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P8_7	√	√	√	—	—	—	√	—	ADC	Slow	√	√*1
P8_8	√	√	√	—	—	—	√	—	ADC	Slow	√	√*1
P8_9	√	√	√	—	—	—	√	—	ADC	Slow	√	√*1
P8_10	√	√	√	—	—	—	√	—	ADC	Slow	√	√*1
P8_11	√	√	√	—	—	—	√	—	ADC	Slow	√	√*1
P8_12	√	√	√	—	—	—	√	—	ADC	Slow	√	√*1
P20_0	—	√	√	—	√	—	√	—	—	Slow	√	—
P20_1	—	√	√	—	—	—	√	—	—	Slow	√	—
P20_2	—	√	√	—	√	—	√	—	—	Slow	√	—
P20_3	—	√	√	—	—	—	√	—	—	Slow	√	—
P20_4	√	√	√	—	√	—	√	—	—	Slow	√	—
P20_5	√	√	√	—	—	—	√	—	—	Slow	√	—
P9_0	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P9_1	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P9_2	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P9_3	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P9_4	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5

(3/5)

Pin Name	144 pin	176 pin	233 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P10_0	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_1	√	√	√	—	—	—	√	—	—	Slow/Fast*3	√	√
P10_2	√	√	√	—	√	—	√	—	—	Slow/Fast*3	√	√
P10_3	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_4	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_5	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P10_6	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_7	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P10_8	√	√	√	—	—	—	√	—	—	Slow/Fast	√	√
P10_9	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_10	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_11	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_12	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_13	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_14	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P10_15	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P11_0	—	√	√	—	—	—	√	—	—	Slow/Fast	√	√
	√	—	—							Slow		
P11_1	√	√	√	—	√	—	√	—	—	Slow/Fast	√	√
P11_2	√	√	√	—	—	—	√	—	—	Slow/Fast*3	√	√
P11_3	√	√	√	—	√	—	√	—	—	Slow/Fast*3	√	√
P11_4	—	√	√	—	—	—	√	—	—	Slow/Fast	√	√
	√	—	—							Slow		
P11_5	—	√	√	—	√	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P11_6	√	√	√	—	√	—	√	—	—	Slow/Fast*3	√	—
P11_7	√	√	√	—	—	—	√	—	—	Slow/Fast*3	√	—
P11_8	—	√	√	—	—	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P11_9	√	√	√	—	√	—	√	—	—	Slow/Fast	√	—
P11_10	√	√	√	—	—	—	√	—	—	Slow/Fast	√	—
P11_11	—	√	√	—	—	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P11_12	√	√	√	—	√	—	√	—	—	Slow	√	—
P11_13	—	√	√	—	√	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P11_14	—	√	√	—	—	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P11_15	—	√	√	—	√	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P12_0	—	√	√	—	—	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P12_1	—	√	√	—	√	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		
P12_2	—	√	√	—	—	—	√	—	—	Slow/Fast	√	—
	√	—	—							Slow		

(4/5)

Pin Name	144 pin	176 pin	233 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P12_3	—	√	√	—	√	—	√	—	—	Slow	√	—
P12_4	—	√	√	—	—	—	√	—	—	Slow	√	—
P12_5	—	√	√	—	—	—	√	—	—	Slow	√	—
P13_0	—	—	√	—	—	—	√	—	—	Slow/Fast	√	—
P13_1	—	—	√	—	—	—	√	—	—	Slow	√	—
P13_2	—	—	√	—	—	—	√	—	—	Slow	√	—
P13_3	—	—	√	—	—	—	√	—	—	Slow	√	—
P13_4	—	—	√	—	—	—	√	—	—	Slow	√	—
P13_5	—	—	√	—	—	—	√	—	—	Slow	√	—
P13_6	—	—	√	—	—	—	√	—	—	Slow	√	—
P13_7	—	—	√	—	—	—	√	—	—	Slow	√	—
P18_0	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_1	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_2	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_3	√	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_4	—	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_5	—	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_6	—	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_7	—	√	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_8	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_9	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_10	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_11	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_12	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_13	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_14	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P18_15	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P19_0	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P19_1	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P19_2	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
P19_3	—	—	√	—	—	—	√	—	ADC	Slow	√	√*5
AP0_0	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_1	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_2	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_3	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_4	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_5	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_6	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_7	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_8	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_9	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_10	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_11	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_12	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_13	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP0_14	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1

(5/5)

Pin Name	144 pin	176 pin	233 pin	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
				CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
AP0_15	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_0	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_1	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_2	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_3	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_4	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_5	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_6	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_7	√	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_8	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_9	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_10	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_11	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_12	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_13	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_14	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1
AP1_15	—	√	√	√	—	—	—	—	ADC	Slow	—	√*1

Note 1. Pull-down resistor for ADC diagnostic purpose. Control via ADC self-diagnostic register.

Note 2. Supports Cload: 100 pF, it can be set for CSIH0SO and CSIH0SC with fast mode

Note 3. Supports Cload: 50 pF, it can be set for CSIHnSO and CSIHnSC with fast mode. (n = 1 to 3)

Note 4. At a power-on clear reset, an on-chip pull-down resistor at the $\overline{\text{RESET}}$ pin is enabled until the flash sequence is completed.

Note 5. Pull-down resistors for ADC diagnostic and internal pull-down purposes. For ADC diagnostic, control via ADC self-diagnostic register. For internal pull-down, control via PD register.

Caution: Regarding external pull-up resistor of $\overline{\text{RESET}}$ pin, please connect less than 6.6 kΩ.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 ×IOVCC		IOVCC + 0.3	V
		SHMT1 (except FLMD0 pin)		0.7 × IOVCC		IOVCC + 0.3	V
		SHMT1 (FLMD0 pin)*3		0.66 × EVCC		EVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
		TTL	EVCC = VPOC to 3.6 V	2.0		EVCC + 0.3	V
			EVCC = 3.6 V to 5.5 V	2.2		EVCC + 0.3	V
		IP0_0 pin		0.7 × REGVCC		REGVCC	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.3 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
		TTL		–0.3		0.8	V
		IP0_0 pin		0		0.3 × REGVCC	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	IP0_0 pin, VI = REGVCC				0.5	µA
		$\overline{\text{RESET}}$, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 pin, VI = EVCC*2				0.5	µA
		P10, P11, P12, P13, P18, P19 pin, VI = BVCC				0.5	µA
		AP0 pin, VI = A0VREF*2				0.5	µA
		AP1 pin, VI = A1VREF*2				0.5	µA
	ILIL	IP0_0 pin, VI = 0 V				–0.5	µA
		$\overline{\text{RESET}}$, FLMD0, JP0, P0, P1, P2, P3, P8, P9, P20 pin, VI = 0 V*2				–0.5	µA
		P10, P11, P12, P13, P18, P19 pin, VI = 0 V*2				–0.5	µA
		AP0 pin, VI = 0 V*2				–0.5	µA
		AP1 pin, VI = 0 V*2				–0.5	µA
Internal pull-up resistance	RU	except FLMD0 pin		20	40	100	kΩ
		FLMD0*3		4	12	36	kΩ
Internal pull-down resistance	RD	except FLMD0 pin		20	40	100	kΩ
		FLMD0		4	12	36	kΩ
High level output voltage	VOH	Fast mode					
			IOH = –5 mA (6 pins)*4	IOVCC – 1.0			V
			IOH = –3 mA (10 pins)*4	IOVCC – 1.0			V
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
		Slow mode					
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
Low level output voltage	VOL	Fast mode					
			IOL = 5 mA (6 pins)*4			0.4	V
			IOL = 3 mA (10 pins)*4			0.4	V
		Slow mode					
			IOL = 1 mA (16 pins)*4			0.4	V

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)*5	CL = 30 pF			7	ns
			CL = 50 pF			12	ns
			CL = 100 pF			24	ns
		Fast mode (P0_5, P0_6, P10_1, P10_2, P11_2, P11_3, P11_6, P11_7)*6	CL = 50 pF			6	ns
		Fast mode (P0_2, P0_3)*6	CL = 100 pF			6.15	ns
		Slow mode*5	CL = 30 pF			37	ns
			CL = 50 pF			62	ns
			CL = 100 pF			124	ns
Output frequency	f_O	Fast mode	CL = 30 pF			40	MHz
		Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz

Note 1. “IOVCC” means the pins are assigned to the power supply (EVCC, BVCC, A0VREF and A1VREF).

Note 2. Not select the analog input function of ADCn.

Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 86 kΩ or more as external pull-down resistor.

Note 4. The number of pin indicates simultaneous ON.

Note 5. Measurement point: 0.1 × IOVCC to 0.9 × IOVCC

Note 6. Measurement point: 0.2 × IOVCC to 0.8 × IOVCC

1.9.1 Output Current

1.9.1.1 233 pin

Table 1.10 Output Current (233 pin) (1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
High level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			–11	mA
				P0_0 to P0_3			–12	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0			–14	mA
				JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9			–28	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P18_0 to P18_7			–30	mA
				P18_8 to P18_15, P19_0 to P19_3			–12	mA
				P10_6 to P10_14, P11_1 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			11	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6 to P2_12			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P2_13 to P2_15, P3_0, P8_2, P8_10 to P8_12			20	mA
				JP0_6, P0_7 to P0_10, P2_2 to P2_3			11	mA

Table 1.10 Output Current (233 pin) (2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgE	Per side	P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9			17	mA
			Total (EVSS)				60	mA
		PgB	Per side	P18_0 to P18_7			30	mA
				P18_8 to P18_15, P19_0 to P19_3			12	mA
				P10_6 to P10_14, P11_1 to P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2, P13_0 to P13_1			32	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5, P13_2 to P13_7			30	mA
			Total (BVSS)				60	mA
		PgA0	Total (A0VSS)				16	mA
		PgA1	Total (A1VSS)				16	mA

Note 1. For detail of the definition of “side” and “total”, refer to **Section 1.2.3, Port Current**.

1.9.1.2 176 pin

Table 1.11 Output Current (176 pin) (1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			–11	mA
				P0_0 to P0_3			–12	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11, P2_0 to P2_1			–9	mA
				JP0_6, P0_7 to P0_10, P1_4 to P1_7, P1_14 to P1_15, P2_2 to P2_5, P8_0 to P8_1, P8_3 to P8_9			–28	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P10_6 to P10_9, P18_0 to P18_7			–28	mA
				P10_10 to P10_14, P11_1 to P11_7, P11_5, P12_0 to P12_2			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–16	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_0 to P20_5			11	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P1_12 to P1_13, P2_6			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P2_0 to P2_1, P8_2, P8_10 to P8_12			16	mA
				JP0_6, P0_7 to P0_10, P2_2 to P2_3			11	mA
				P1_4 to P1_7, P1_14 to P1_15, P2_4 to P2_5, P8_0 to P8_1, P8_3 to P8_9			17	mA
			Total (EVSS)				60	mA

Table 1.11 Output Current (176 pin) (2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgB	Per side	P18_0 to P18_7			8	mA
				P10_6 to P10_14, P11_1 to P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0, P11_8 to P11_14, P12_3 to P12_5			30	mA
			Total (BVSS)				60	mA
		PgA0	Total (A0VSS)				16	mA
		PgA1	Total (A1VSS)				16	mA

Note 1. For detail of the definition of “side” and “total”, refer to **Section 1.2.3, Port Current**.

1.9.1.3 144 pin

Table 1.12 Output Current (144 pin) (1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side	P9_0 to P9_4, P20_4 to P20_5			–7	mA
				P0_0 to P0_3			–12	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P1_0 to P1_3, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2, P1_8 to P1_11			–7	mA
				JP0_6, P0_7 to P0_10, P1_4 to P1_7, P8_0 to P8_1, P8_3 to P8_9			–22	mA
			Total (EVCC)				–60	mA
		PgB	Per side	P10_6 to P10_9, P18_0 to P18_3			–24	mA
				P10_10 to P10_14, P11_1 to P11_7, P11_5, P12_0 to P12_2			–30	mA
				P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_14			–30	mA
			Total (BVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
		PgA1	Total (A1VREF)				–8	mA
Low-level output current	IOL	PgE	Per side	P9_0 to P9_4, P20_4 to P20_5			7	mA
				P0_0 to P0_6, P0_11 to P0_14, P1_0 to P1_3			30	mA
				JP0_0 to JP0_5, P1_8 to P1_11, P8_2, P8_10 to P8_12			14	mA
				JP0_6, P0_7 to P0_10			9	mA
				P1_4 to P1_7, P8_0 to P8_1, P8_3 to P8_9			13	mA
			Total (EVSS)				60	mA

Table 1.12 Output Current (144 pin) (2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Low-level output current	IOL	PgB	Per side	P18_0 to P18_3			4	mA
				P10_6 to P10_14, P11_1 to P11_2			30	mA
				P11_3 to P11_7, P11_15, P12_0 to P12_2			30	mA
				P10_0 to P10_5, P10_15, P11_0, P11_8 to P11_14			30	mA
			Total (BVSS)				60	mA
		PgA0	Total (A0VSS)				16	mA
		PgA1	Total (A1VSS)				8	mA

Note 1. For detail of the definition of “side” and “total”, refer to **Section 1.2.3, Port Current**.

1.10 Power Supply Currents

Condition: REGVCC, EVCC, BVCC, A0VREF and A1VREF total current. But, the I/O buffer is stopped.

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Ta	Peripheral				
RUN mode current	IDDR1	Run (120 MHz)	Run	–40 to 125°C	Run (#1)		64	125	mA
				25°C	Stop (#1)		51		mA
RUN mode current (During self programming)	IDDR3	Run (120 MHz)	Run	–40 to 125°C	Run (#2)		76	142	mA
HALT mode current	IDDH	Run	Run	–40 to 125°C	Run (#3)		42	110	mA
STOP mode current	IDDS	Stop	Stop	–40 to 85°C	Stop (#2)		0.75	12	mA
				105°C	Stop (#2)			20	mA
				125°C	Stop (#2)			34	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop (#3)		50	430	µA
				105°C	Stop (#3)			756	µA
				125°C	Stop (#3)			1274	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 85°C	Run (#4)		4	22	mA
				105°C	Run (#4)			35	mA
				125°C	Run (#4)			63	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 85°C	Run (#5)		2	19	mA
				105°C	Run (#5)			32	mA
				125°C	Run (#5)			61	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Ta = 25°C
- REGVCC = EVCC = BVCC = A0VREF = A1VREF = 5.0 V
- AWOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj ≤ 150°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

(1/2)

Power Domain	Function	Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Stop	Stop
	SubOSC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Stop	Stop
	FOUT	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read / Write	Read / Write	No access	Fetch	No access	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	RTCA0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Stop	Stop	Stop
	ADCA0	Run*1	Run*1	Run*1	Stop	Stop	Stop	Stop	Stop

(2/2)

Power Domain	Function	Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
ISO	CPU1 (PE1)	Run (PLL)	Run (PLL)	Halt (PLL)	Run (HS IntOSC)	Stop	Run (PLL)	Stop	Power off
	DMA	Run	Run	Run	Stop	Stop	Stop	Stop	
	PLL0	Run	Run	Run	Stop	Stop	Run	Stop	
	PLL1	Run	Run	Run	Stop	Stop	Run	Stop	
	Code Flash	Fetch	No access	No access	No access	No access	Fetch	No access	
	Data Flash	Read	Write / Erase	No access	No access	No access	Read	No access	
	LRAM (PE1)	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	GRAM	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	OSTMn	Run	Run	Run	Stop	Stop	Stop	Stop	
	WDTAn	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUBn	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUJ1	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAPA, PIC	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	ENCA0	Run	Run	Run	Stop	Stop	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN3n	Run (115.2kbps)	Run (115.2kbps)	Run (115.2kbps)	Stop	Stop	Stop	Stop	
	RLIN2n	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	RS-CANn	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CSIGn	Run	Run	Run	Stop	Stop	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Stop	Stop	
	RIIC0	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	Flexray	Run	Run	Run	Stop	Stop	Stop	Stop	
	EternetAVB	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	KR	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CLMA2	Run	Run	Run	Stop	Stop	Stop	Stop	
	ADCA1	Run	Run	Run	Stop	Stop	Stop	Stop	

Note 1. T&H used.

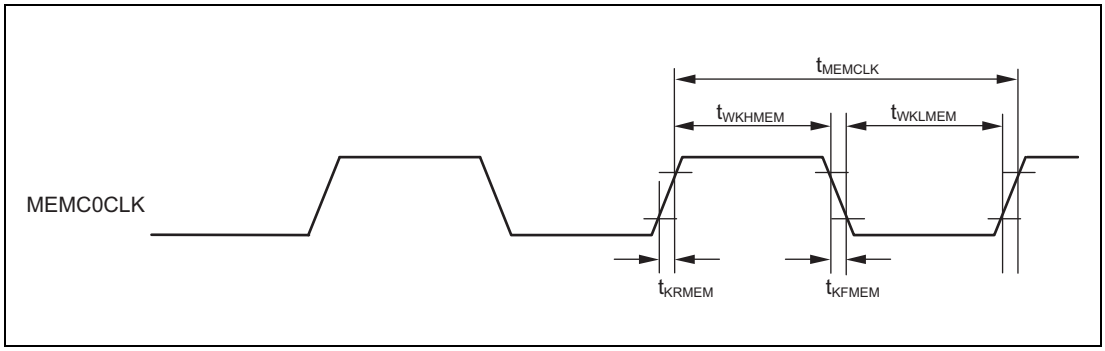
1.11 MEMC0CLK Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0CLK pin: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MEMC0CLK output cycle	t_{MEMCLK}		33.4 (max. 30 MHz)			ns
MEMC0CLK high / low level width	t_{WKHMEM} / t_{WKLMEM}		t_{MEMCLK} / 2 – 10			ns
MEMC0CLK rise / fall time	t_{KRMEM} / t_{KFMEM}				10	ns



1.12 External Bus Timing

1.12.1 MEMC0CLK Asynchronous

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0AD0-15, MEMC0A16-19, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, $\overline{\text{MEMC0ASTB}}$, $\overline{\text{MEMC0WR}}$, $\overline{\text{MEMC0RD}}$ pin: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max. 30 MHz)			ns
Address*6 setup time to $\overline{\text{MEMC0ASTB}}$ ↓	t_{SAST}	<1>	(1 + ASW) × T – 15			ns
Address (MEMC0AD15-0) hold time from $\overline{\text{MEMC0ASTB}}$ ↓	t_{HSTA}	<2>	(1 + AHW) × T – 15			ns
Address (MEMC0AD15-0) float delay time from $\overline{\text{MEMC0RD}}$ ↓	t_{FRDA}	<3>			9	ns
Address*7 hold time from $\overline{\text{MEMC0RD}}$ ↑	t_{HRDA}	<4>	–1.5			ns
Data (MEMC0AD15-0) input delay time from $\overline{\text{MEMC0RD}}$ ↓	t_{DRDID}	<5>	9		(1 + w) × T – 35	ns
Data (MEMC0AD15-0) input hold time from $\overline{\text{MEMC0RD}}$ ↑	t_{HRDID}	<6>	0			ns
Delay time from $\overline{\text{MEMC0ASTB}}$ ↓ to $\overline{\text{MEMC0RD}}$ ↓	t_{DSTRD}	<7>	(1 + AHW) × T – 15			ns
Delay time from $\overline{\text{MEMC0ASTB}}$ ↓ to $\overline{\text{MEMC0WR}}$ ↓	t_{DSTWR}	<8>	(1 + AHW) × T – 15			ns
$\overline{\text{MEMC0RD}}$, $\overline{\text{MEMC0WR}}$ low level width	t_{WRDST}	<9>	(1 + w) × T – 10			ns
Data (MEMC0AD15-0) output delay time from $\overline{\text{MEMC0WR}}$ ↓	t_{DWROD}	<10>			11	ns
Address*7 hold time from $\overline{\text{MEMC0WR}}$ ↑	t_{HWRA}	<11>	(1 + DHW) × T – 15			ns
Data (MEMC0AD15-0) output setup time to $\overline{\text{MEMC0WR}}$ ↑	t_{SODWR}	<12>	(1 + w) × T – 15			ns
Data (MEMC0AD15-0) output hold time from $\overline{\text{MEMC0WR}}$ ↑	t_{HWROD}	<13>	(1 + DHW) × T – 15			ns
$\overline{\text{MEMC0WAIT}}$ setting delay from $\overline{\text{MEMC0ASTB}}$ ↓	t_{SSTWT1}	<14>			(2 + AHW) × T – (4 × t_{CPUCLK} + 35)	ns
	t_{SSTWT2}	<15> w ≥ 1			(2 + w + AHW) × T – (4 × t_{CPUCLK} + 35)	ns
$\overline{\text{MEMC0WAIT}}$ hold time from $\overline{\text{MEMC0ASTB}}$ ↓	t_{HSTWT1}	<16> w ≥ 1	(1 + w + AHW) × T – (4 × t_{CPUCLK} + 20)			ns
	t_{HSTWT2}	<17> w ≥ 1	(2 + w + AHW) × T – (4 × t_{CPUCLK} + 20)			ns

Note 1. ASW means the number of address setup wait for multiplex bus.

Note 2. AHW means the number of address hold wait for multiplex bus.

Note 3. “w” means the number of data wait.

Note 4. t_{CPUCLK}: CPU clock period.

Note 5. DHW means the number of data hold wait for multiplex bus.

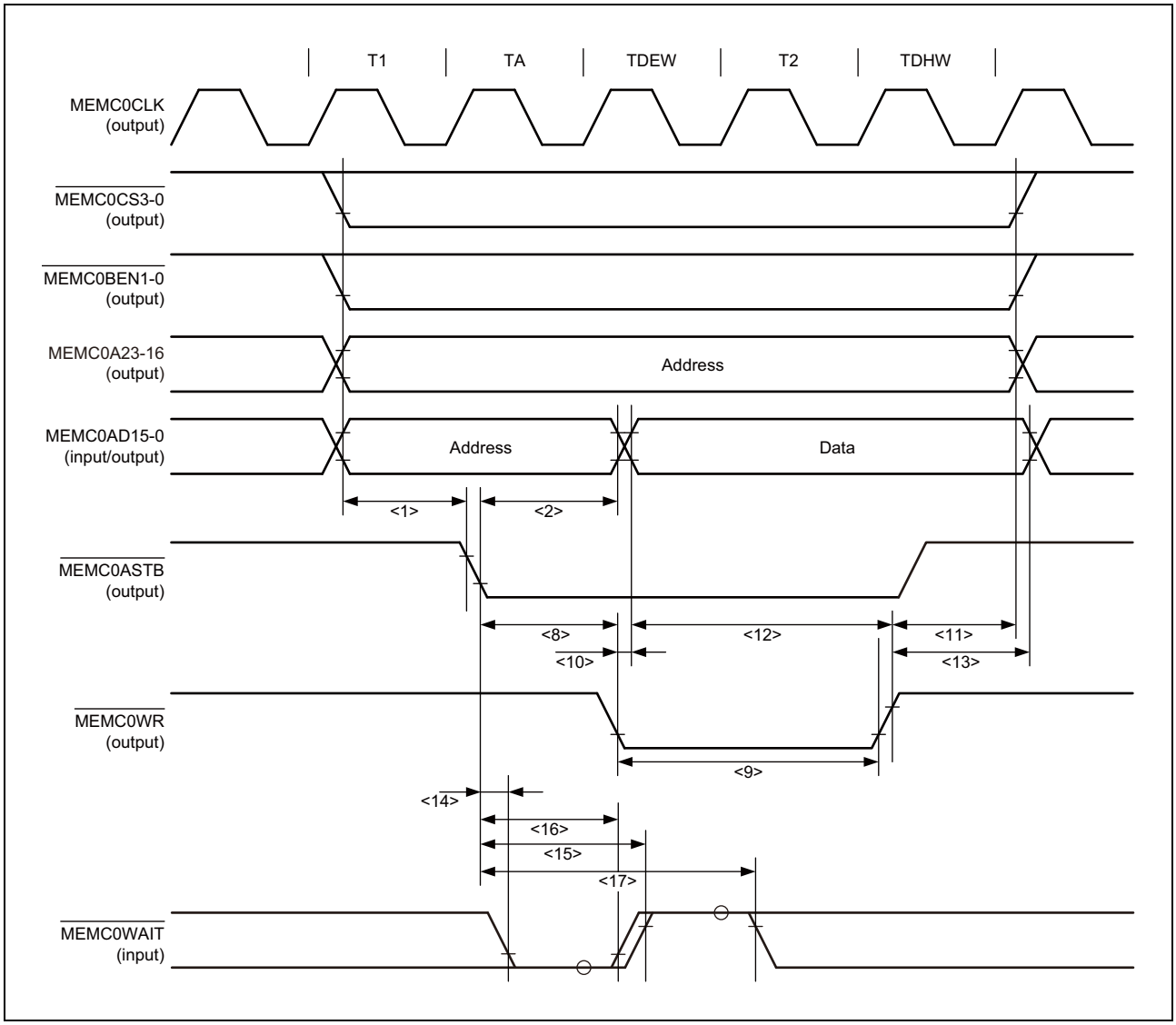
Note 6. Address means MEMC0AD15-0, MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$ and $\overline{\text{MEMC0BEN1-0}}$. 233 pin and 176 pin products support 20 bit address.

Note 7. Address means MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$ and $\overline{\text{MEMC0BEN1-0}}$. 233 pin and 176 pin products support 20 bit address.

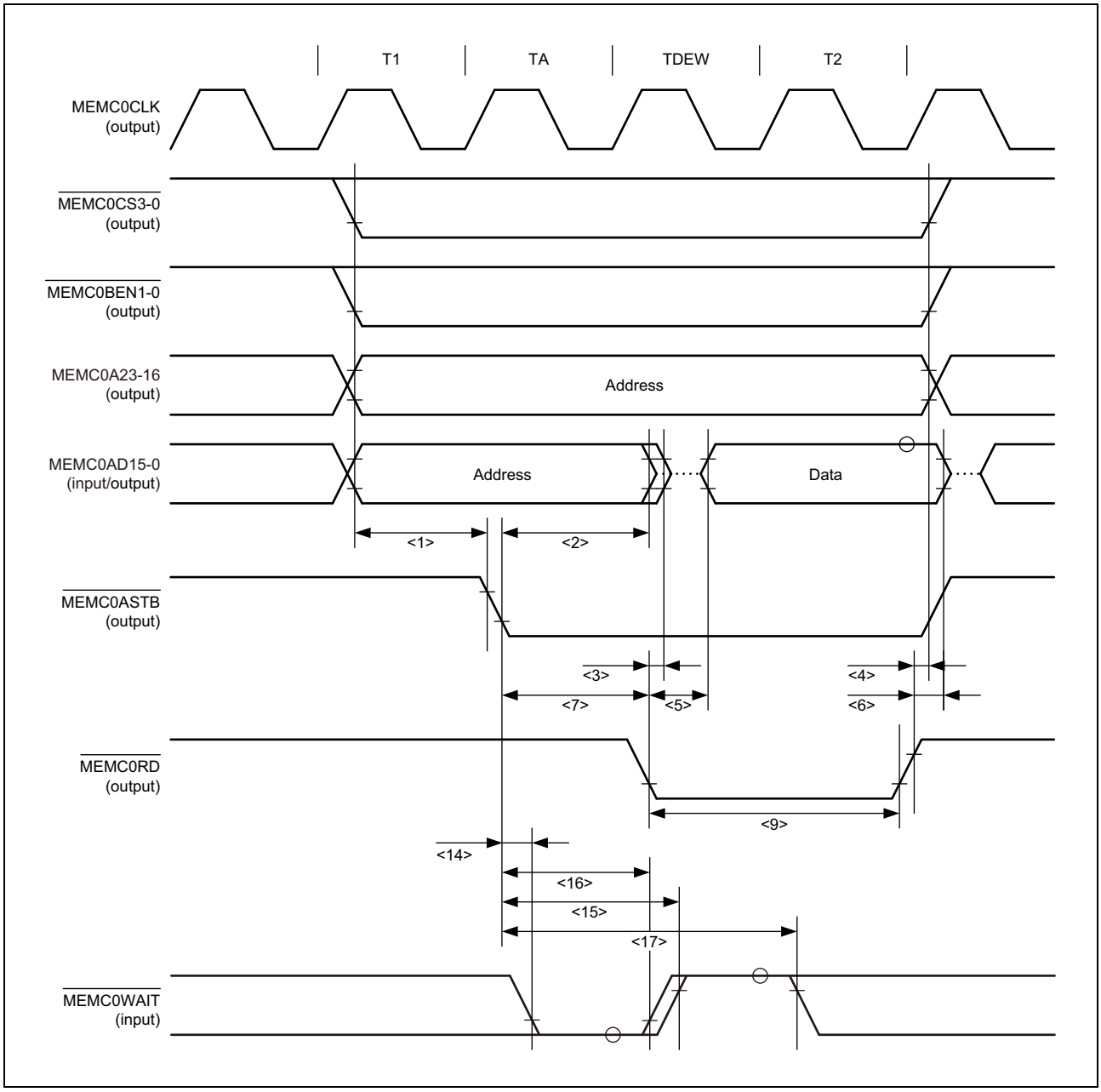
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1data wait. (w = 1)

(1) Multiplex Write Cycle (Asynchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Asynchronous; 1 Data Wait)



1.12.2 MEMC0CLK Synchronous

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

MEMC0CLK, MEMC0AD0-15, MEMC0A16-19, $\overline{\text{MEMC0CS3-0}}$, $\overline{\text{MEMC0BEN1-0}}$, $\overline{\text{MEMC0ASTB}}$, $\overline{\text{MEMC0WR}}$, $\overline{\text{MEMC0RD}}$ pin: Fast mode

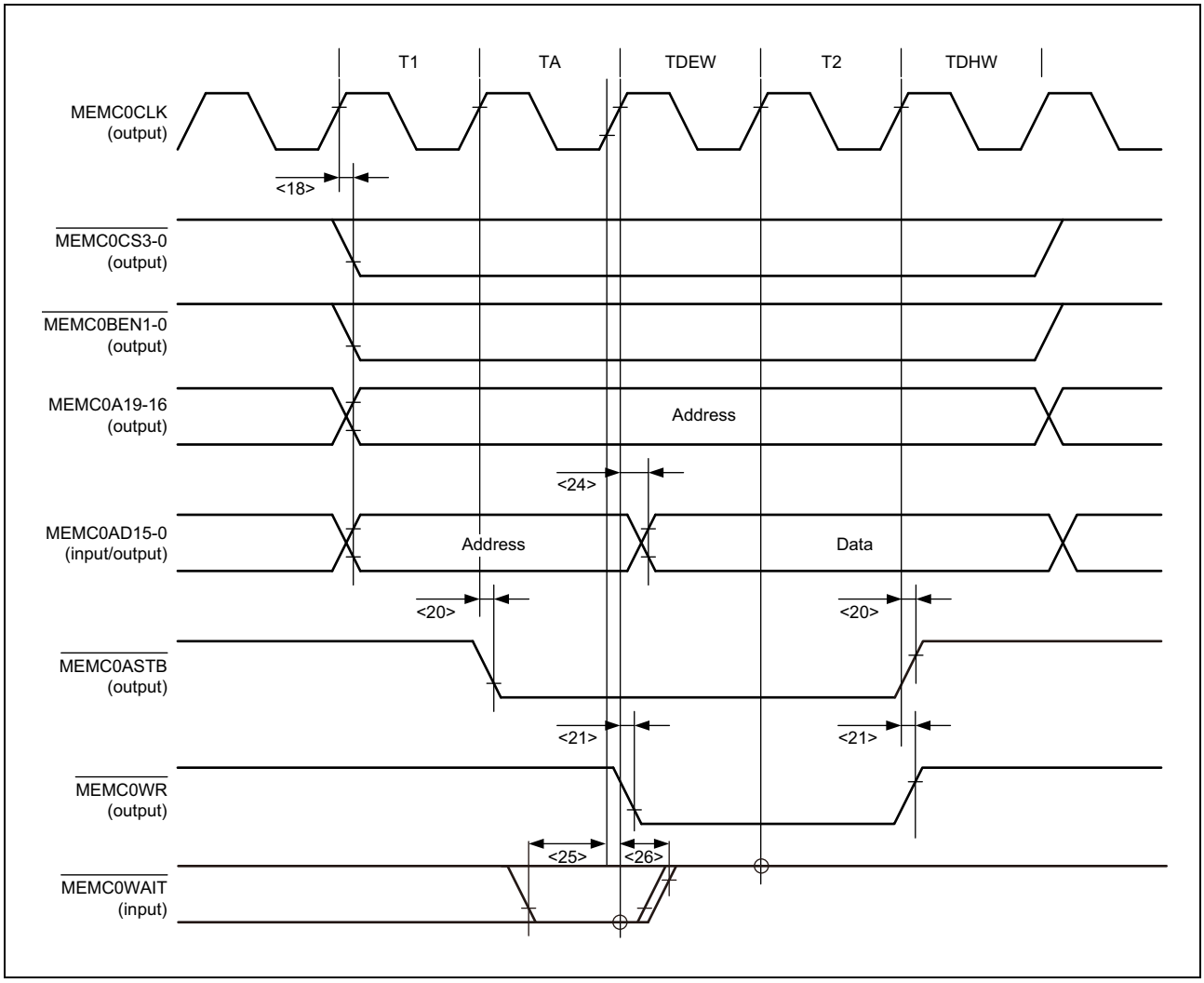
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T		33.4 (max. 30 MHz)			ns
Delay time from MEMC0CLK ↑ to address*1	t_{DKA}	<18>	–0.5		15	ns
Delay time from MEMC0CLK ↑ to address (MEMC0AD15-0) float	t_{FKA}	<19>	0		12	ns
Delay time from MEMC0CLK ↑ to $\overline{\text{MEMC0ASTB}}$	t_{DKST}	<20>	0		11	ns
Delay time from MEMC0CLK ↑ to $\overline{\text{MEMC0RD}}$ and $\overline{\text{MEMC0WR}}$	t_{DKRDWR}	<21>	–2.5		6	ns
Data (MEMC0AD15-0) input setup time (from MEMC0CLK ↑)	t_{SIDK}	<22>	10			ns
Data (MEMC0AD15-0) input hold time (from MEMC0CLK ↑)	t_{HKID}	<23>	2.5			ns
Data (MEMC0AD15-0) output delay time (from MEMC0CLK ↑)	t_{DKOD}	<24>			15	ns
$\overline{\text{MEMC0WAIT}}$ setup time (to MEMC0CLK ↑)	t_{SWTK}	<25>	22 + 4 × t_{CPUCLK}			ns
$\overline{\text{MEMC0WAIT}}$ hold time (from MEMC0CLK ↑)	t_{HKWT}	<26>	–5 – 4 × t_{CPUCLK}			ns

Note 1. Address means MEMC0AD15-0, MEMC0A23-16, $\overline{\text{MEMC0CS3-0}}$ and $\overline{\text{MEMC0BEN1-0}}$. All F1M products support 20 bit address.

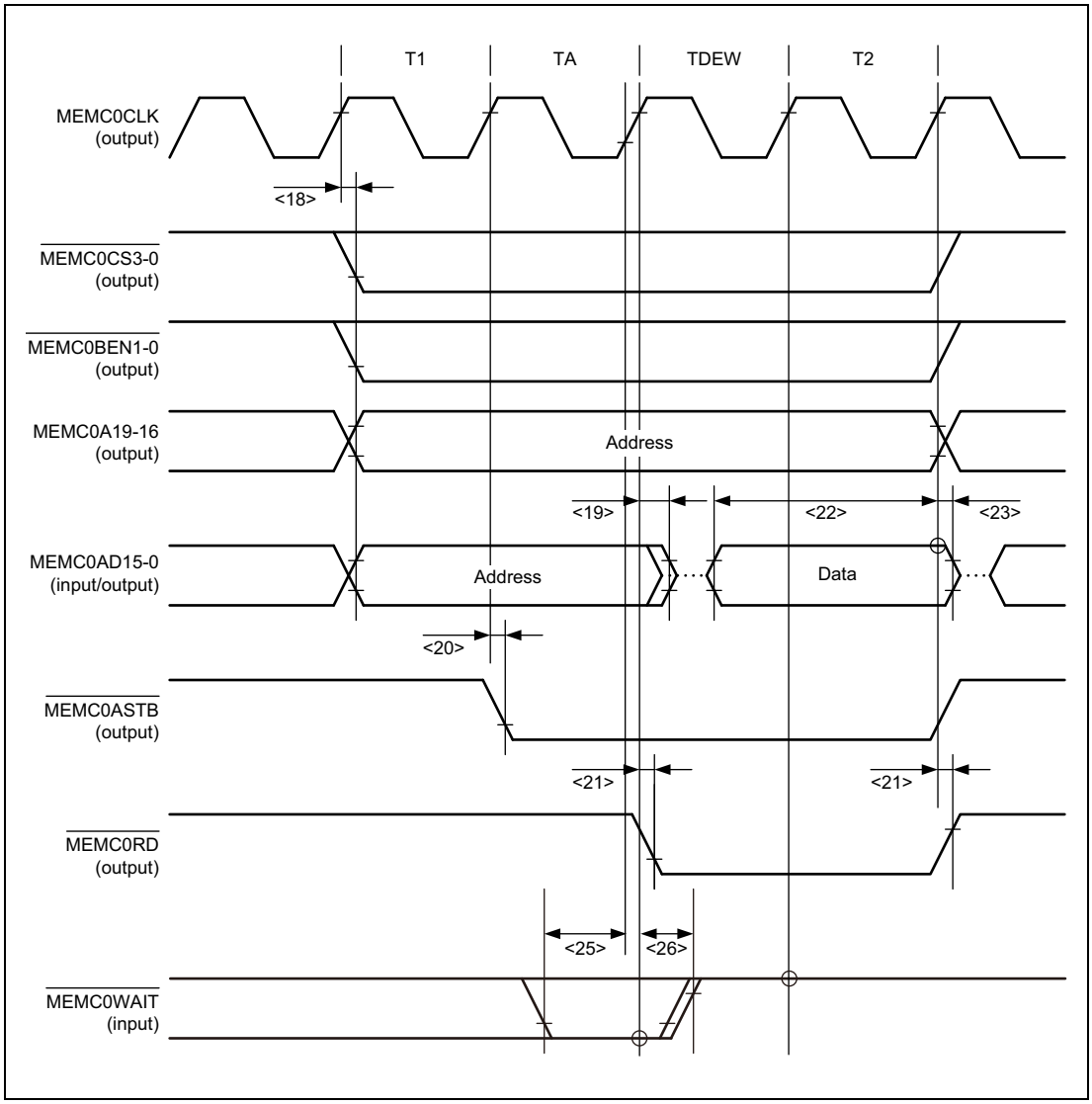
NOTE

When the bus period (T) is shorter than 44 ns, t_{DRDID} spec requires at least 1data wait. (w = 1)

(1) Multiplex Write Cycle (Synchronous; 1 Data Wait)



(2) Multiplex Read Cycle (Synchronous; 1 Data Wait)



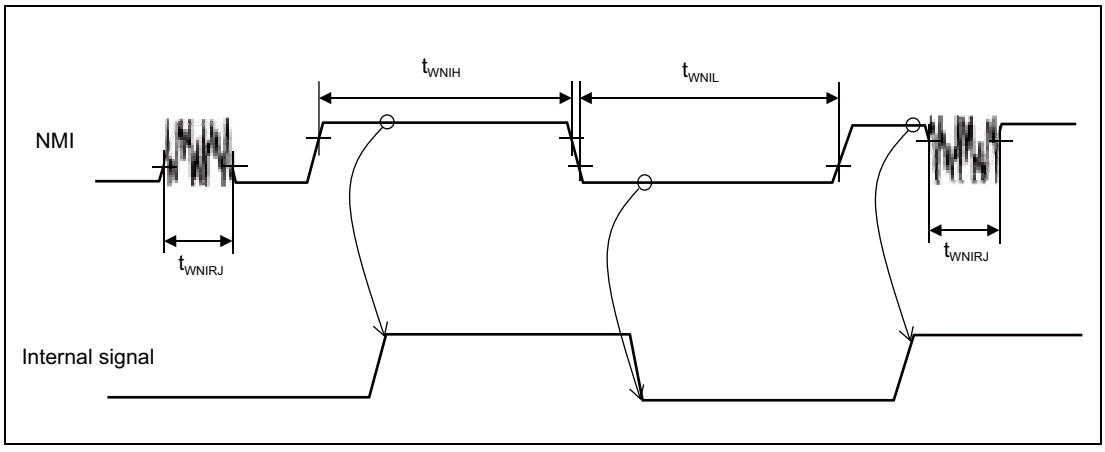
1.13 Interrupt Timing

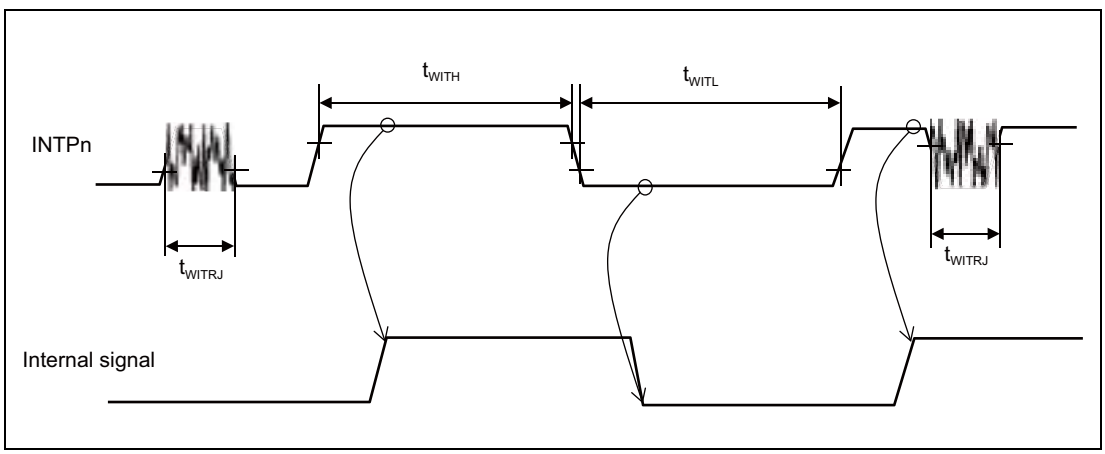
Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high / low level width*1	t_{WNIH} / t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			µs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high / low level width*1	t_{WITH} / t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			µs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





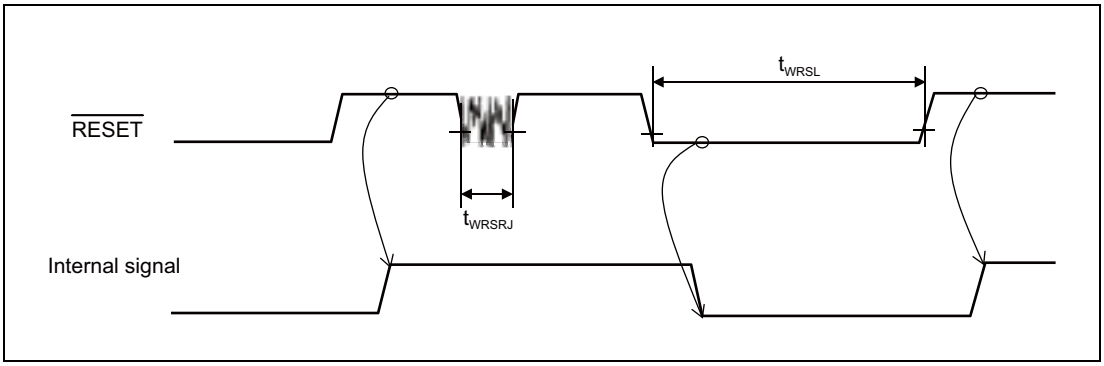
1.14 $\overline{\text{RESET}}$ Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	*3	0.6			µs
		*4	5.0			µs
		*5	600			µs
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		0.1			µs

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



Note 3. After $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600µs will become Hi-z. (figure (a))

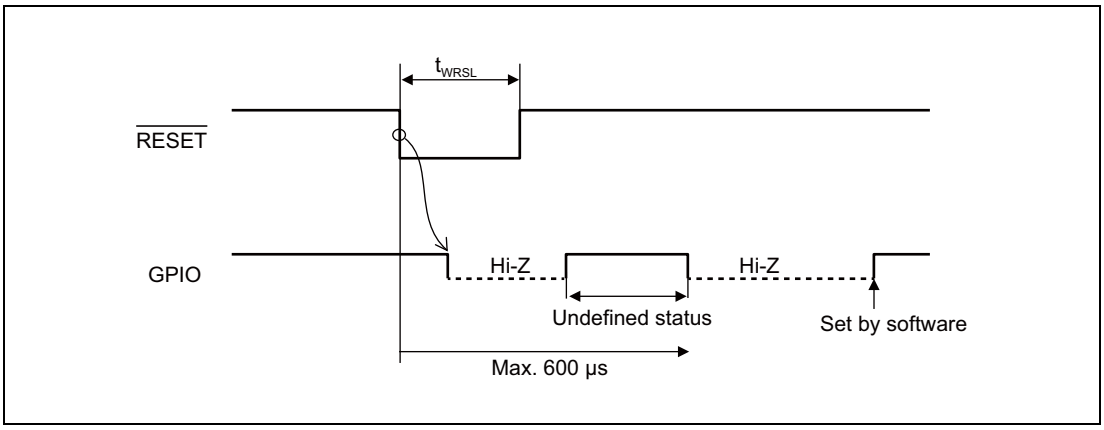
Note 4. If during RUN mode or HALT mode, after $\overline{\text{RESET}}$ is asserted GPIO pin will become Hi-z. For other modes, after $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600µs will become Hi-z. (figure (a) and (b))

Note 5. GPIO output states will become Hi-z after $\overline{\text{RESET}}$ is asserted. (figure (b))

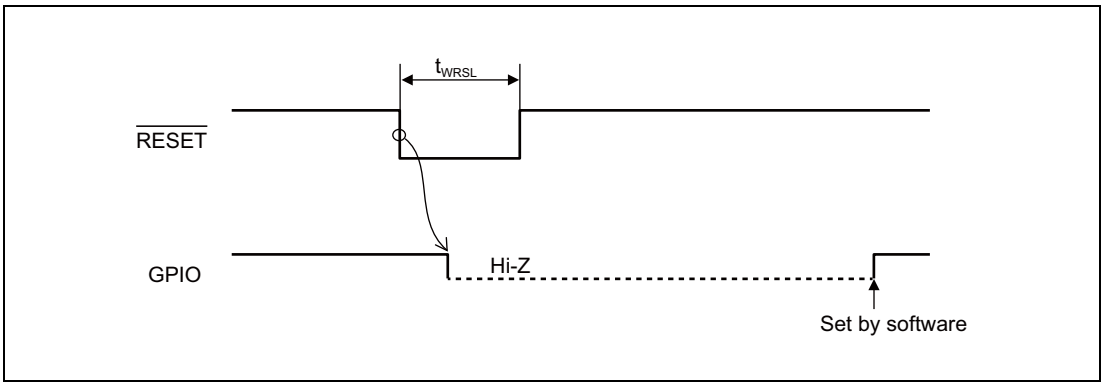
(a) In case of either

t_{WRSL} < 5 µs, any mode or

t_{WRSL} < 600 µs, any mode except for RUN and HALT mode.



(b) In case of either
5 µs ≤ t_{WRSL}, RUN and HALT mode or
600 µs ≤ t_{WRSL}, any mode.

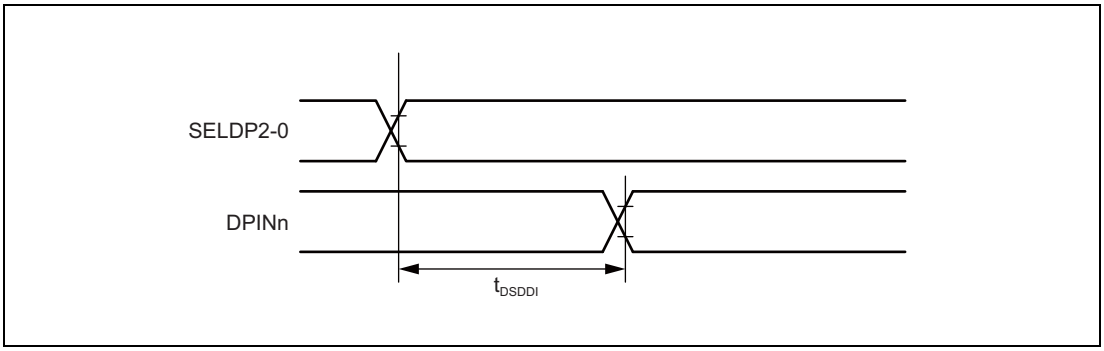


1.15 Low Power Sampler (DPIN Input) Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note 1. n = 7 to 0



1.16 CSCXFOUT Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

<Output driver strength>

CSCXFOUT: Slow or fast mode (refer to the condition in the following table)

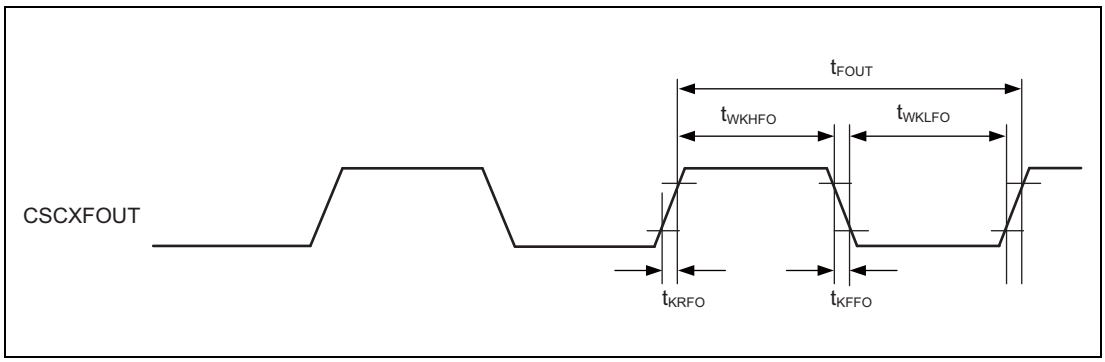
Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	Slow mode		100 (max.10 MHz)			ns
		Fast mode (Except JP0_3 pin)*1		33.4 (30 MHz)			ns
CSCXFOUT high level width	t_{WKHFO}	Slow mode	N: 1*2 or even value*3	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*3, *4	t_{FOUT} × (N+1) / 2N – 37			ns
		Fast mode (Except JP0_3 pin)*1	N: 1*2 or even value*3	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*3	t_{FOUT} × (N+1) / 2N – 10			ns
CSCXFOUT low level width	t_{WKLFO}	Slow mode	N: 1*2 or even value*3	t_{FOUT} / 2 – 37			ns
			N: Odd value (N ≥ 5)*3, *4	t_{FOUT} × (N–1) / 2N – 37			ns
		Fast mode (Except JP0_3 pin)*1	N: 1*2 or even value*3	t_{FOUT} / 2 – 10			ns
			N: Odd value (N ≥ 3)*3	t_{FOUT} × (N–1) / 2N – 10			ns
CSCXFOUT rise / fall time	t_{KRFO} / t_{KFFO}	Slow mode				37	ns
		Fast mode (Except JP0_3 pin)*1				10	ns

Note 1. JP0_3 does not support fast mode.

Note 2. When MainOSC, HS IntOSC, LS IntOSC or SubOSC is selected as source clock with the condition of N = 1, the characteristics of output signal depends on the selected source clock. It is recommended to use output signal after evaluation on an actual environment.

Note 3. “N” is the value of “Clock divisor N” defined by FOUTDIV register.

Note 4. The selection of N = 3 is prohibited when slow mode is used.



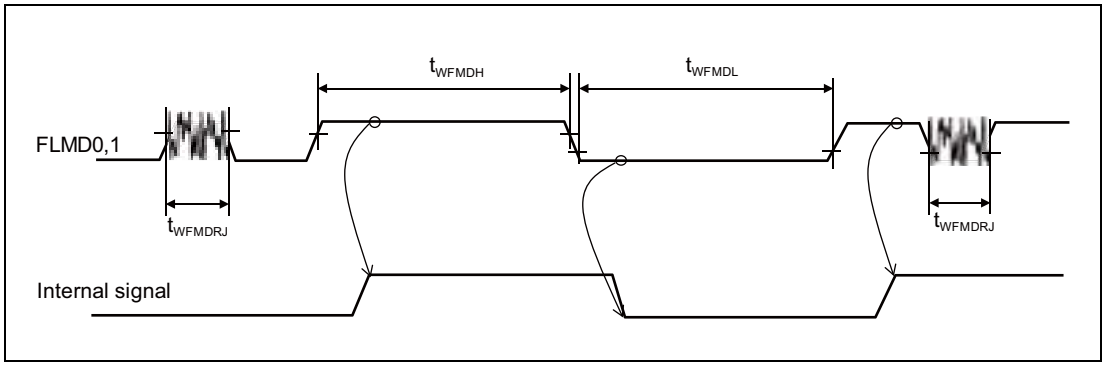
1.17 Mode Timing

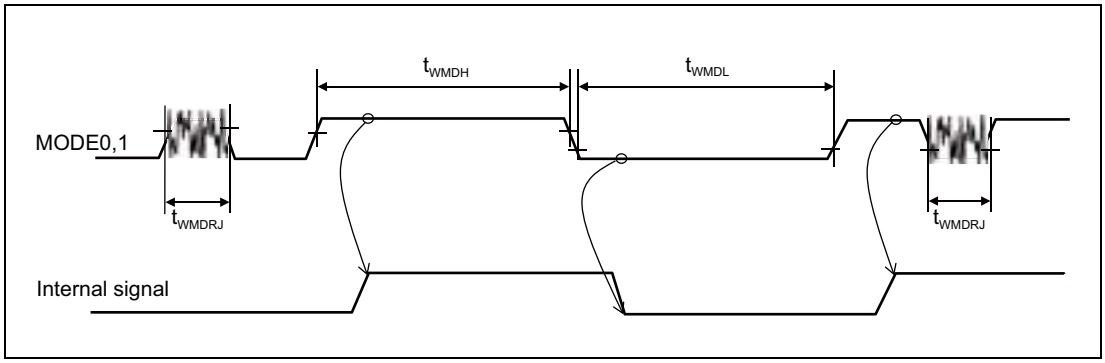
Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0,1 input high/low level width*1	t_{WFMDH} / t_{WFMDL}		600			ns
FLMD0,1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0,1 input high / low level width*1	t_{WMDH} / t_{WMDL}		600			ns
MODE0,1 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0,1 and MODE0,1 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum will be ignored. This is reference value. Noise such as the figure can be filtered.





1.18 Timer Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

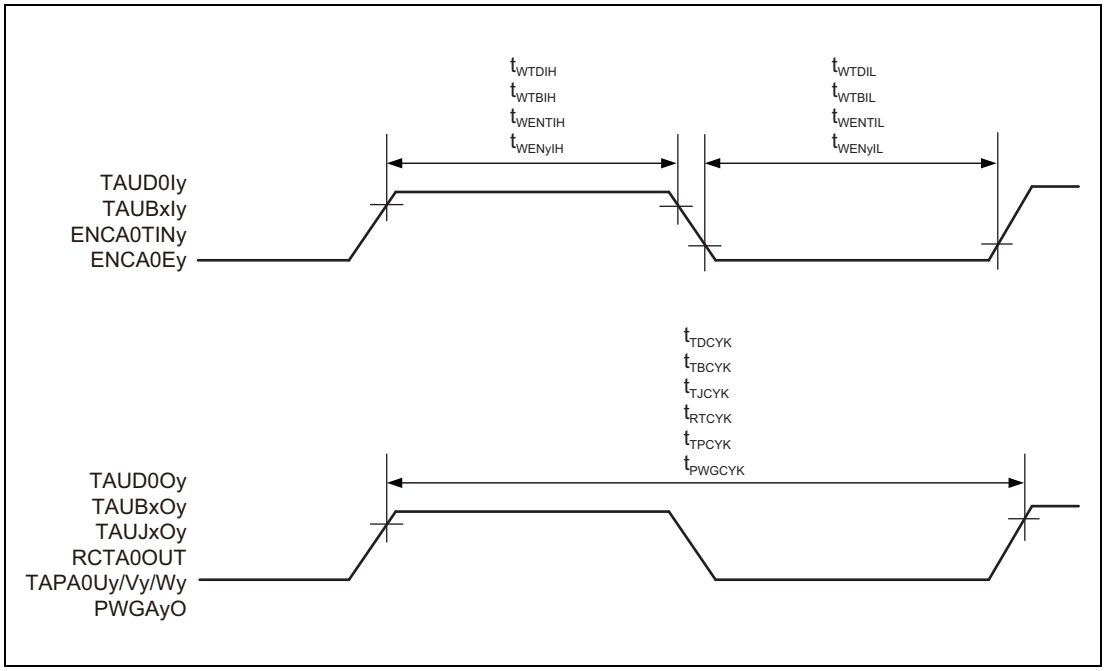
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20[*1, *2]			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUBxIy input high/low level width (x = 0, 1, y = 0 to 15)	t_{WTBIH}/ t_{WTBIL}		n × Tsamp + 20[*1, *2]			ns
TAUBxOy output cycle (x = 0, 1, y = 0 to 15)	t_{TBCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width[*3] (x = 0, 1, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxIy pulse rejection[*4]	t_{WTIJRJ}		100			ns
TAUJxOy output cycle (x = 0, 1, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
RTCA0OUT output cycle	t_{RTCYK}			1		Hz
TAPA0ESO input high/low level width[*3]	t_{WESIH}/ t_{WESIL}		600			ns
TAPA0ESO pulse rejection[*4]	t_{WESIRJ}		100			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t_{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t_{WENTIH}/ t_{WENTIL}		n × Tsamp + 20[*1]			ns
ENCA0Ey input high/low level width (y = 0, 1, C)	t_{WENyIH}/ t_{WENyIL}		n × Tsamp + 20[*1]			ns
PWGAyO output cycle (y = 0 to 95)	t_{PWGCYK}	Slow mode			10	MHz

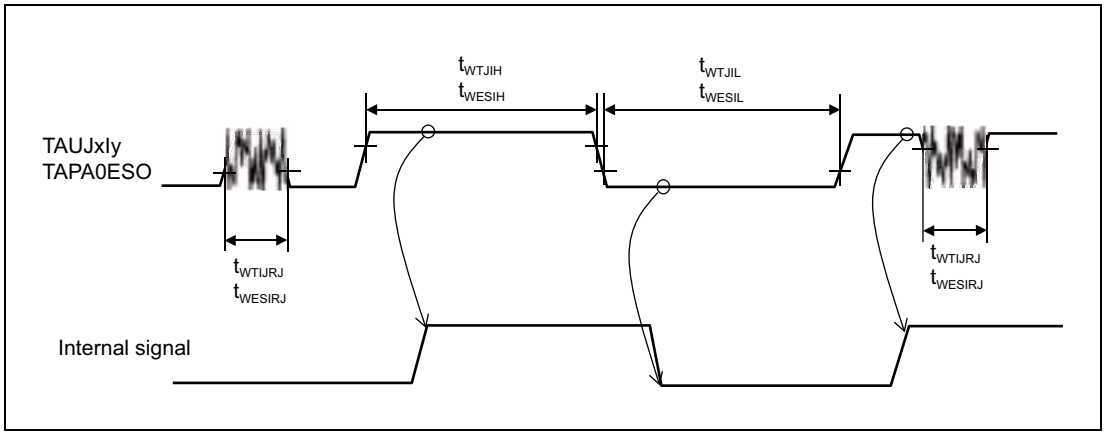
Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

Note 3. TAUJxIy and TAPA0ESO input width is needed to ensure that the internal timer input signal is activated.

Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.


tWTDIH
tWTBIH
tWENTIH
tWENyIH
tWTDIL
tWTBIL
tWENTIL
tWENyIL
TAUD0Iy
TAUBxIy
ENCA0TINy
ENCA0Ey
tTDCYK
tTBCYK
tTJCYK
tRTCYK
tTPCYK
tPWGCYK
TAUD0Oy
TAUBxOy
TAUJxOy
RCTA0OUT
TAPA0Uy/Vy/Wy
PWGAyO


tWTJIH
tWESIH
tWTJIL
tWESIL
TAUJxIy
TAPA0ESO
tWTIJRJ
tWESIRJ
tWTIJRJ
tWESIRJ
Internal signal

1.19 RLIN2 / RLIN3 Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baudrate	1		115.2*1	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

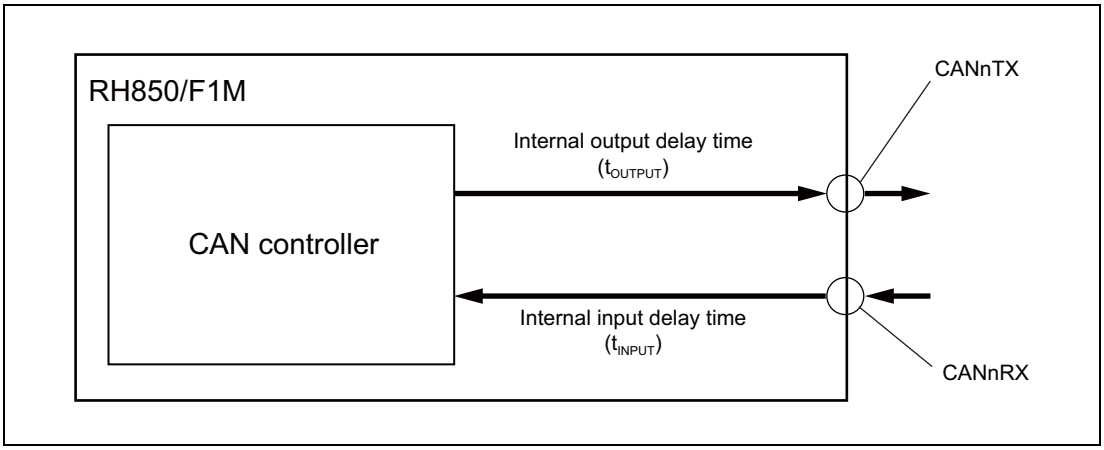
Note 1. The LIN extended baudrate is not part of the LIN standard specification.

1.20 RS-CAN Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time*1	t_{NODE}				100	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



1.21 CSI Timing

1.21.1 CSIG Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Table 1.13 CSIG Timing (Master Mode)

<Output driver strength>

CSIGnSO, CSIGnSC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSC low level width	t_{KWLMGn}		0.5 × t_{KCYMGn} – 10			ns
CSIGnSI setup time (vs CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	2 × t_{KCYGn} + 25			ns
CSIGnRYI High level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	t_{KCYGn} + 5			ns

Table 1.14 CSIG Timing (Slave Mode)

<Output driver strength>

CSIGnSO: Fast mode

CSIGnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSC low level width	t_{KWLSGn}		0.5 × t_{KCYSGn} – 10			ns
CSIGnSI setup time (vs CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs CSIGnSC)	t_{HSISGn}		t_{KCYGn} + 5			ns
CSIGnSO output delay (vs CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}	$t_{KCYSGn} \geq 8 \times t_{KCYGn}$			38	ns
		$t_{KCYSGn} < 8 \times t_{KCYGn}$			38 + t_{KCYGn}	ns
$\overline{\text{CSIGnSSI}}$ setup time (vsCSIGnSC)	$t_{SSSISGn}$		0.5 × t_{KCYSGn} – 5			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs CSIGnSC)	$t_{HSSISGn}$		t_{KCYGn} + 5			ns

1.21.2 CSIH Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Table 1.15 CSIH Timing (Master Mode)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode (CL = 100 pF@n = 0 / 50 pF@n = 1 to 3)
CSIHnCSSm: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs CSIHnSC)	t_{SSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs CSIHnSC)	t_{HSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn} / 2			ns
CSIHnSO output delay (vs CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI High level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 15			ns
CSIHnCSS0-7 setup time (vs CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock period an inactive width time $t_{WSCSBHn}$ of "0.5 × t_{KCYMHn}" is added.

Table 1.16 CSIH Timing (Slave Mode)

<Output driver strength>

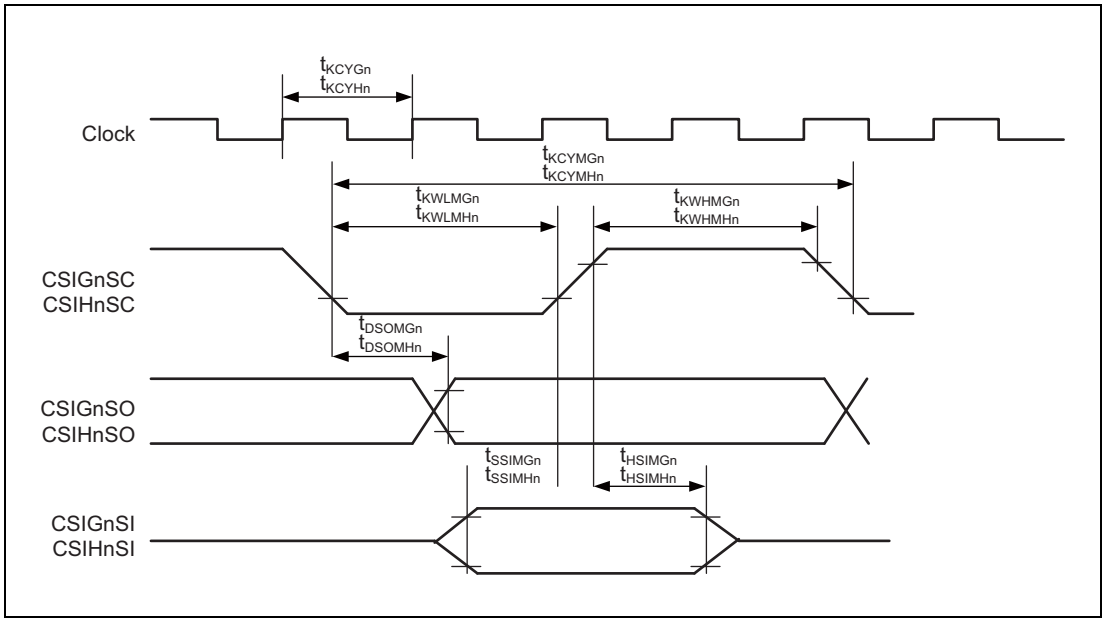
CSIHnSO, CSIHnSC (output): Fast mode
CSIHnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			38	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$38 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

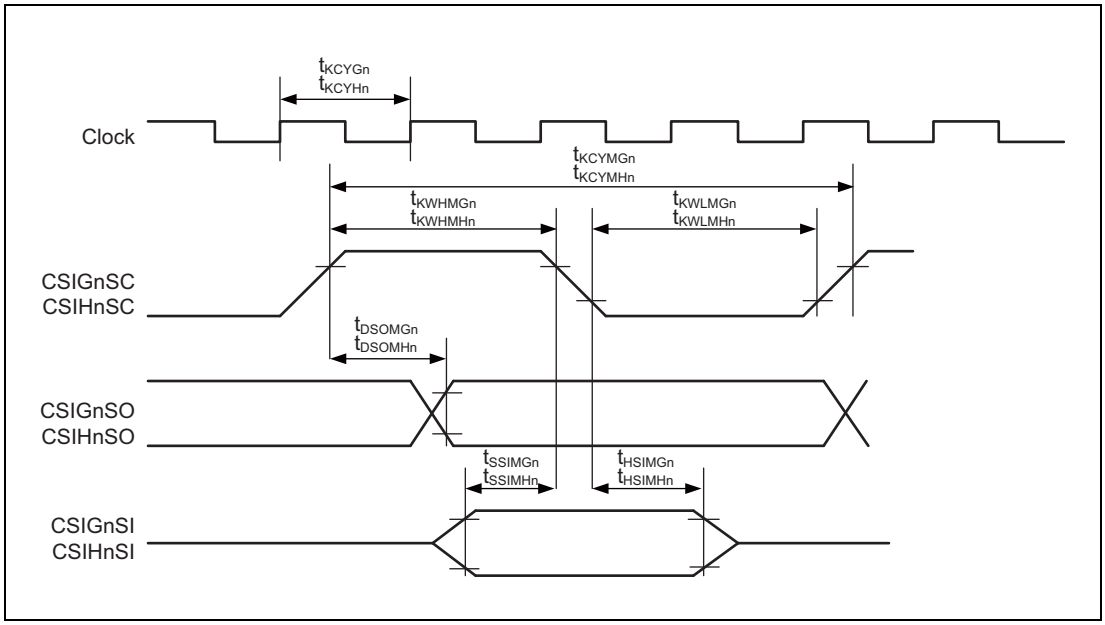
(1) SC/SI/SO

Master Mode:

- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



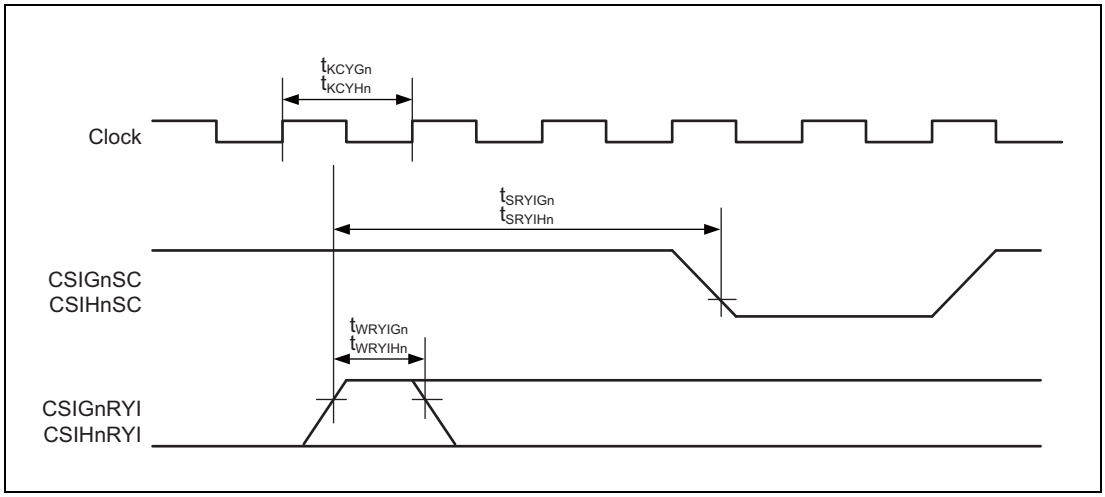
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



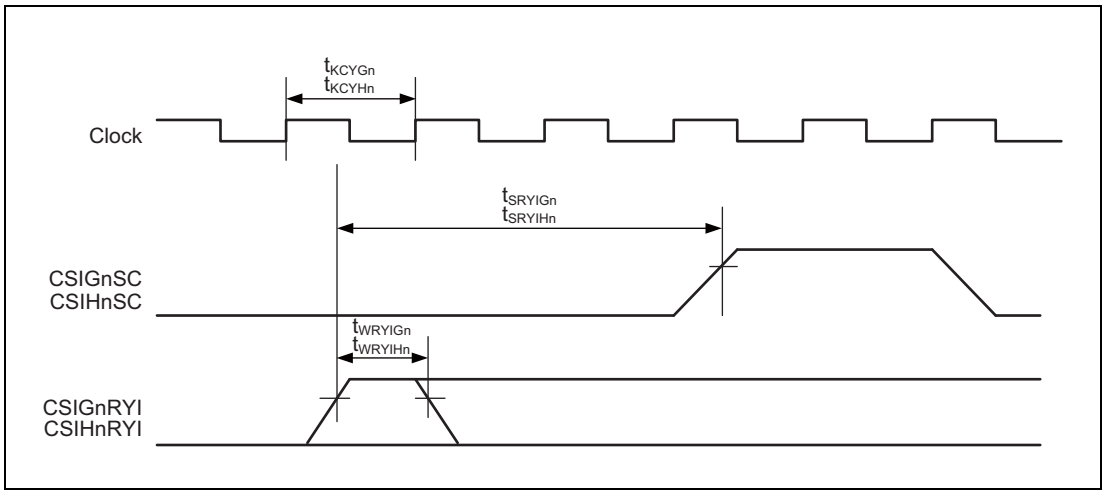
(2) RYI

CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

- CSIG (CSIGnCTL1: CSIGnCKR = 0)
- CSIH (CSIHnCFGm: CSIHnCKPm = 0)



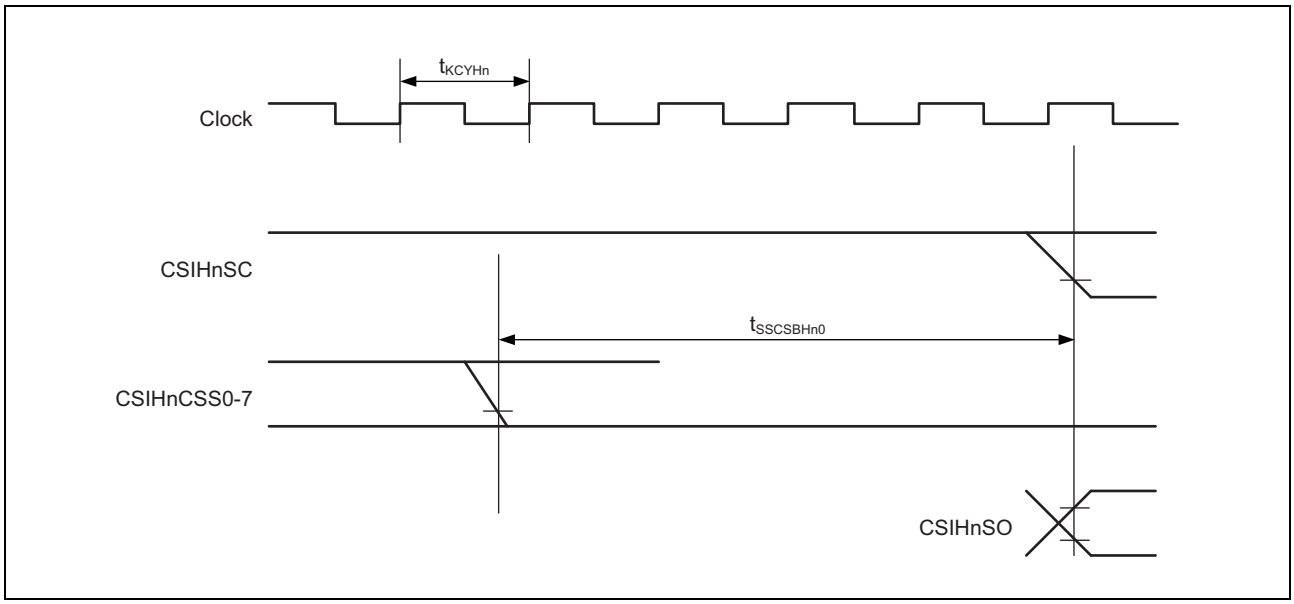
- CSIG (CSIGnCTL1: CSIGnCKR = 1)
- CSIH (CSIHnCFGm: CSIHnCKPm = 1)



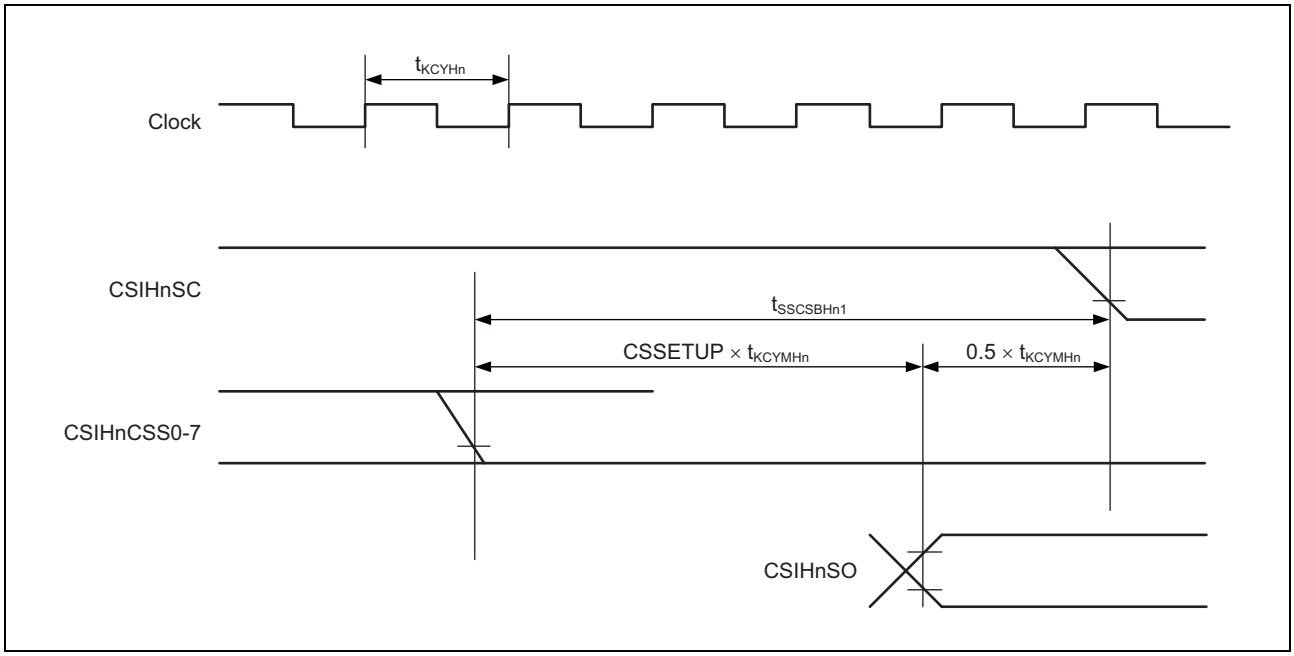
(3) CSSn

Only Master Mode (Setup Time):

- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0

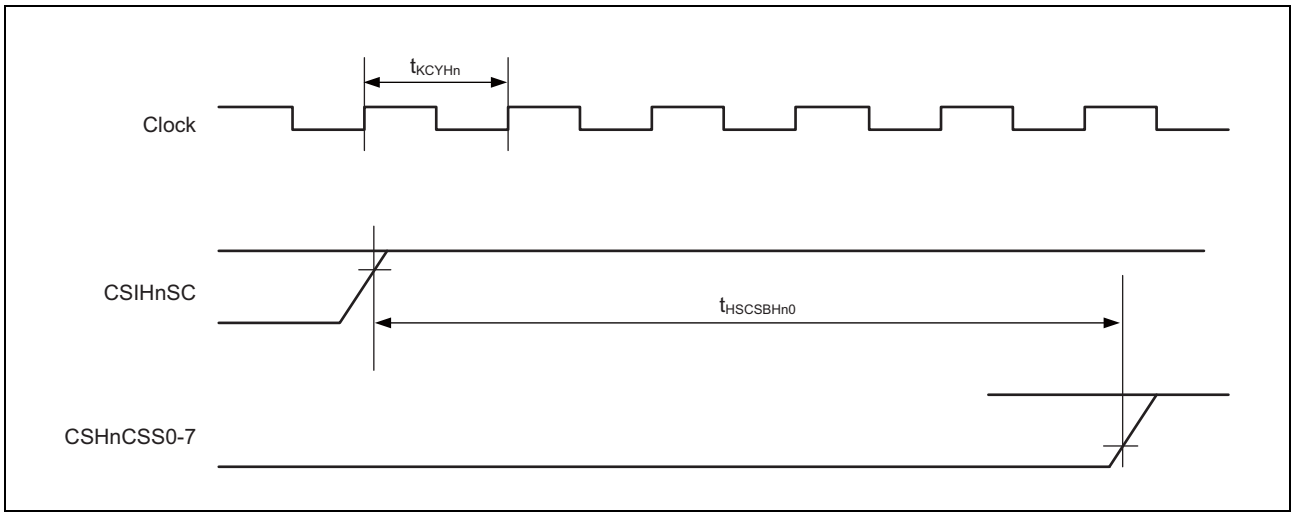


- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 1

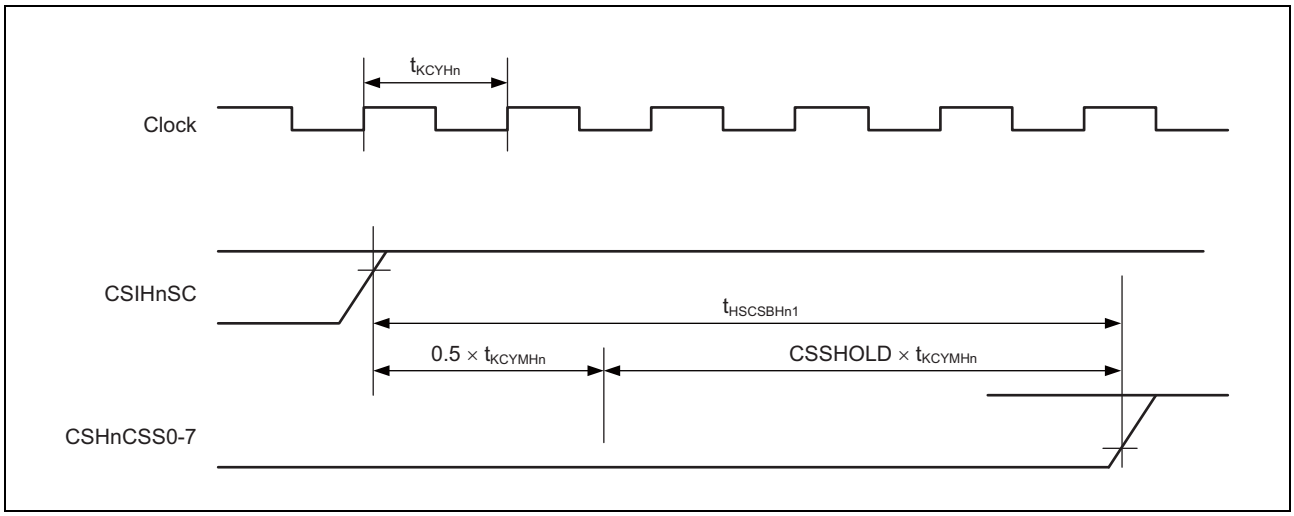


Only Master Mode (Hold Time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



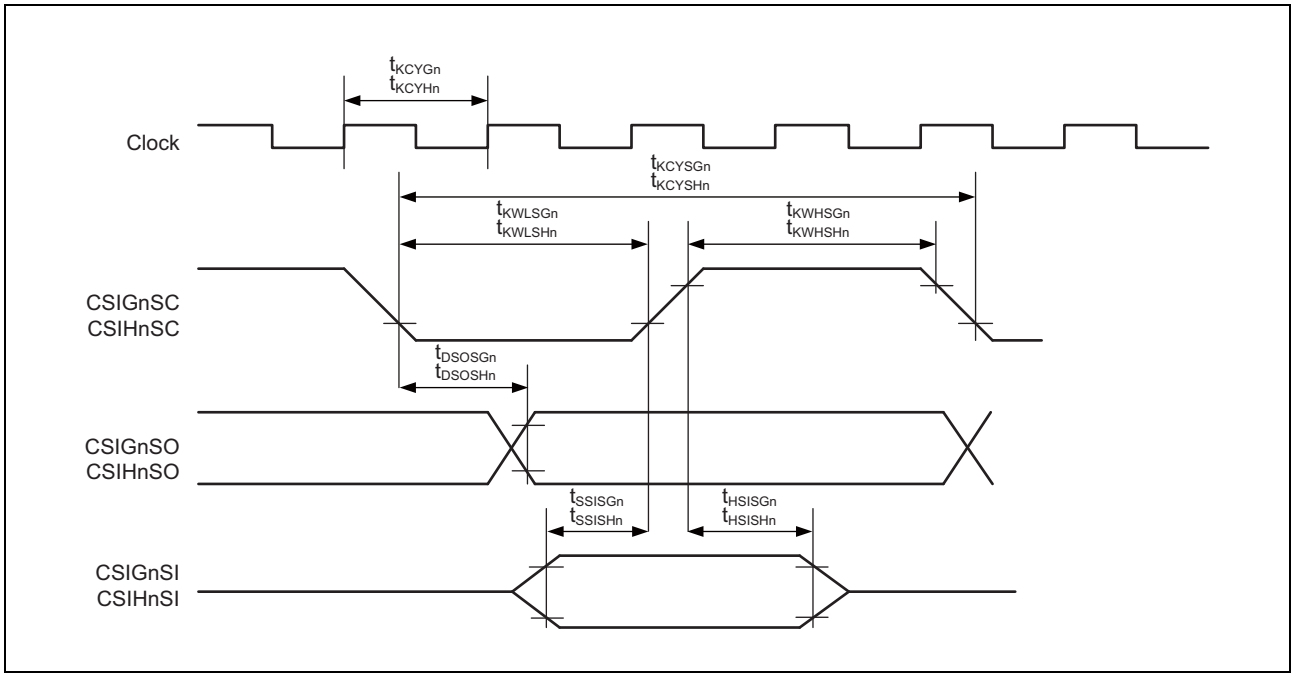
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



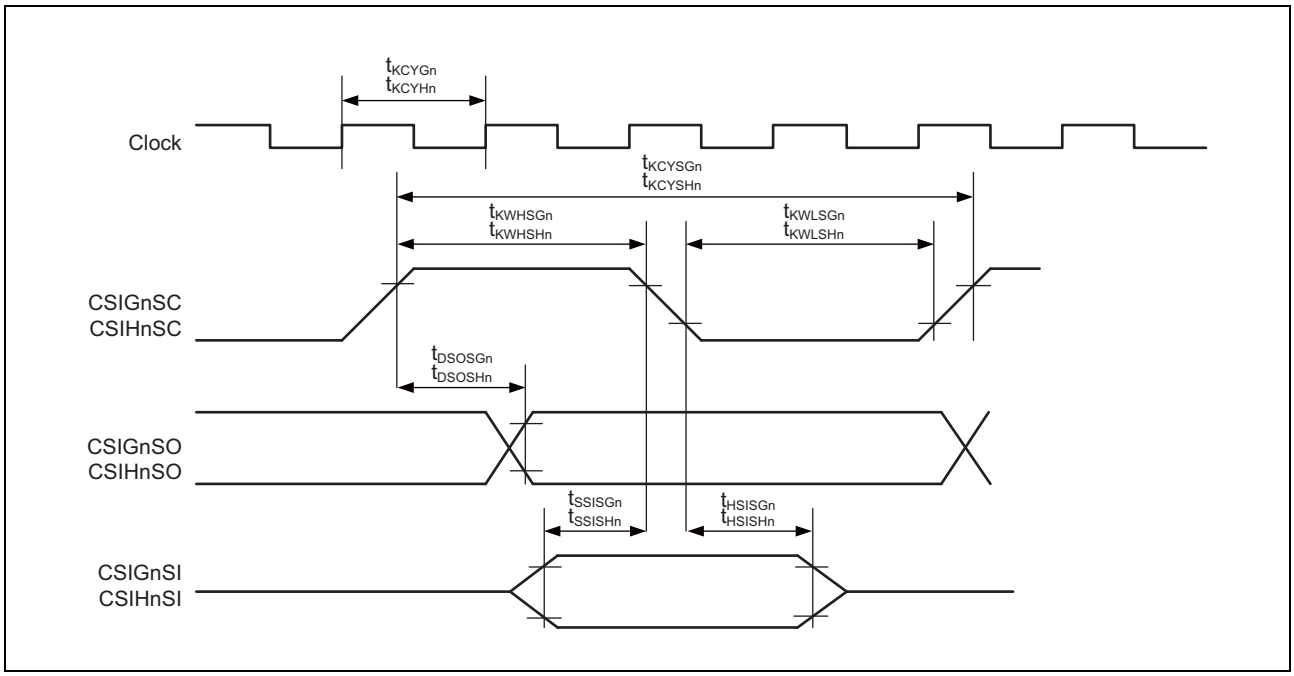
(4) SC/SI/SO

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0 /0 or 1/1)

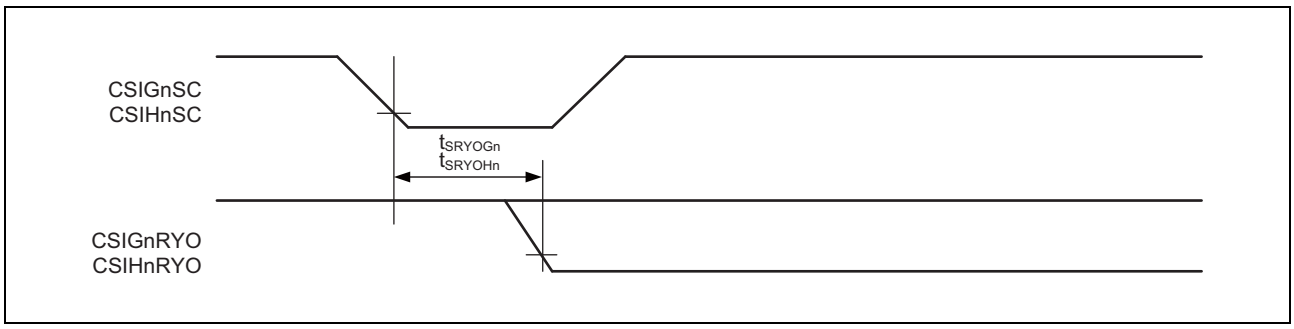


- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

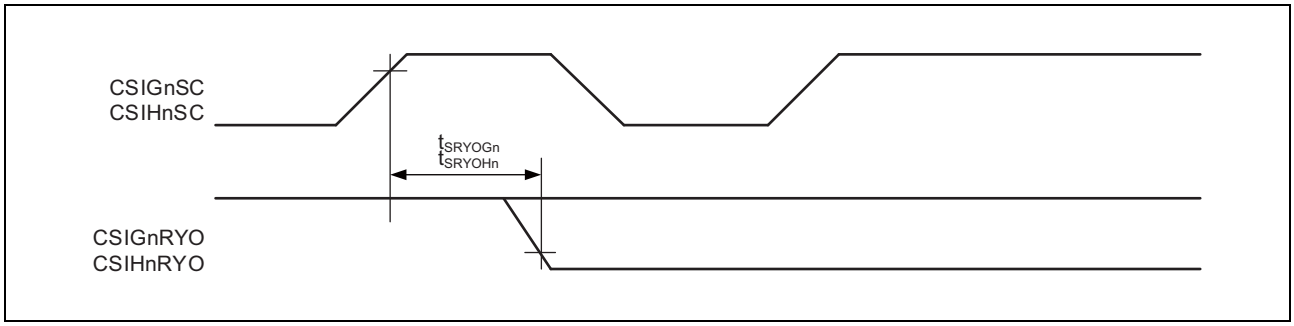


(5) RYO

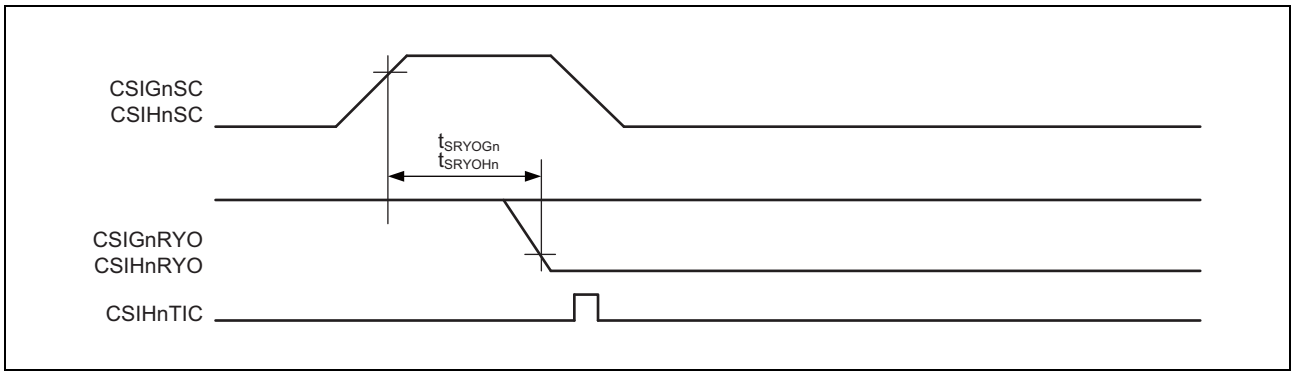
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0)



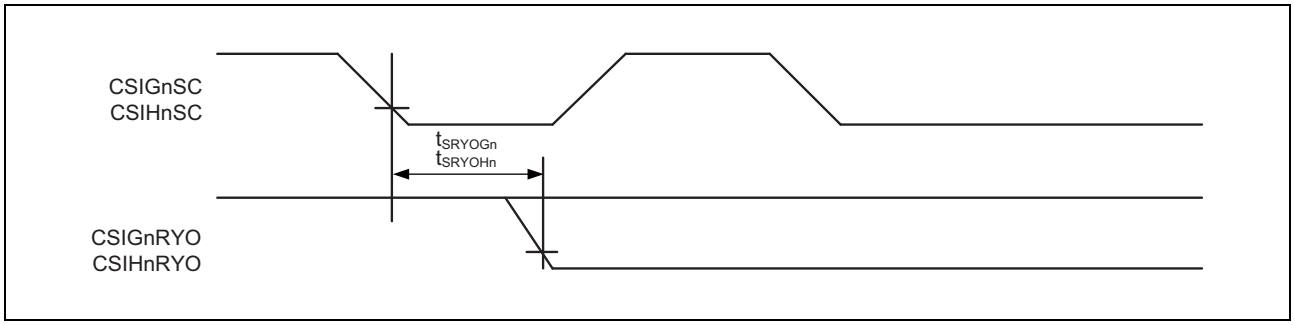
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0)



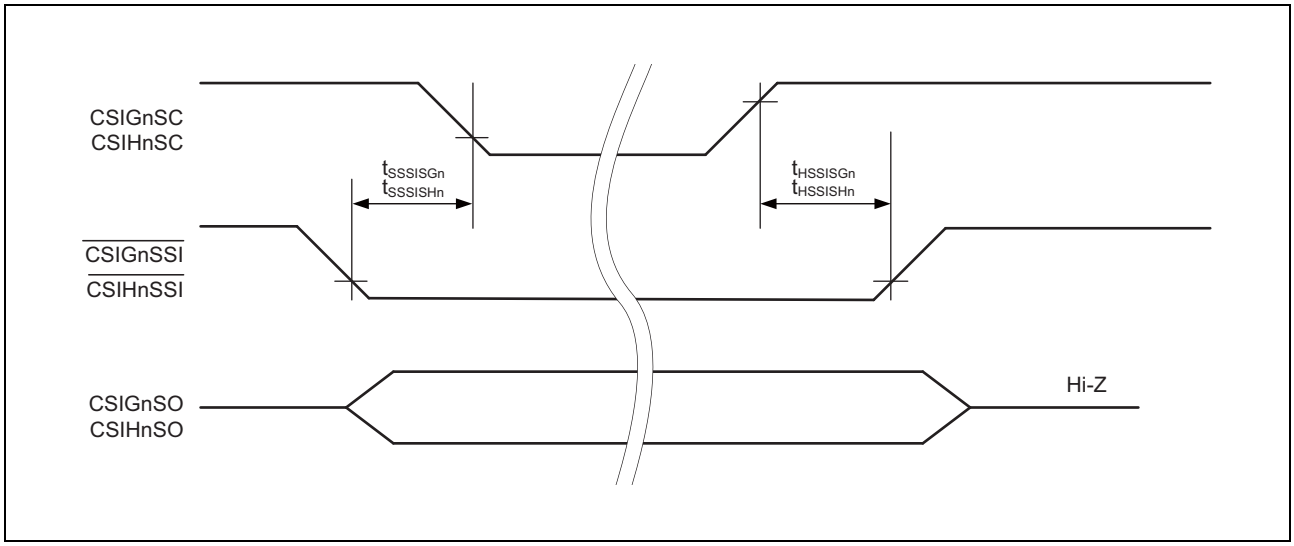
- CSIG (CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/1)



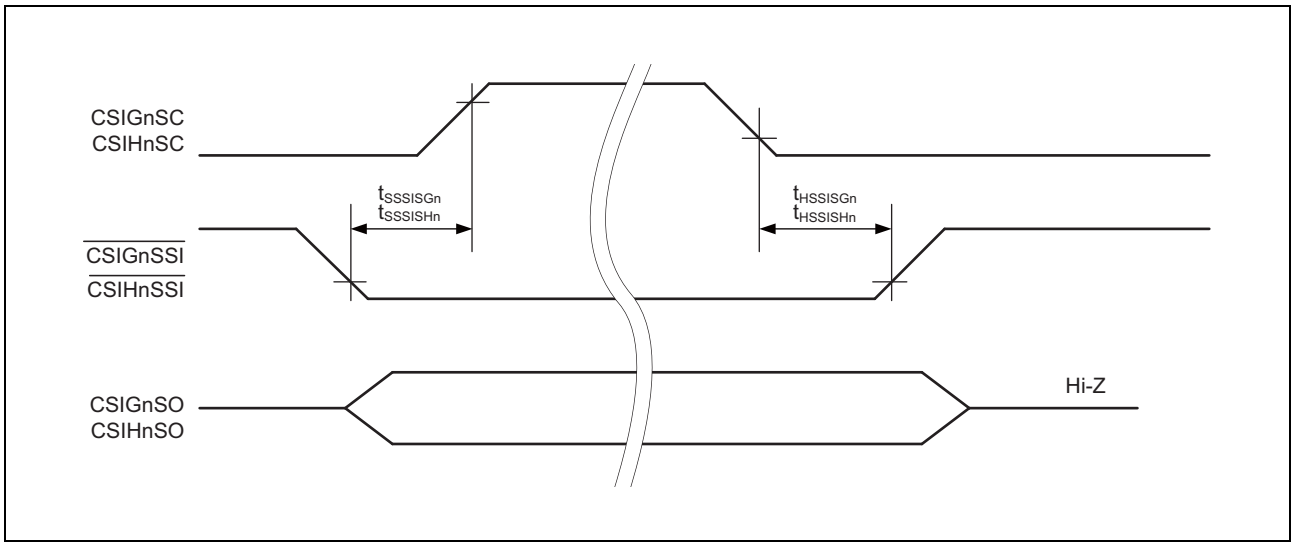
(6) SSI

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR / CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



1.22 RIIC Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C

Table 1.17 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RIIC0SCL clock low-level width	t_{LOW}		4.7			µs
RIIC0SCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Table 1.18 RIIC Timing (Fast Mode)

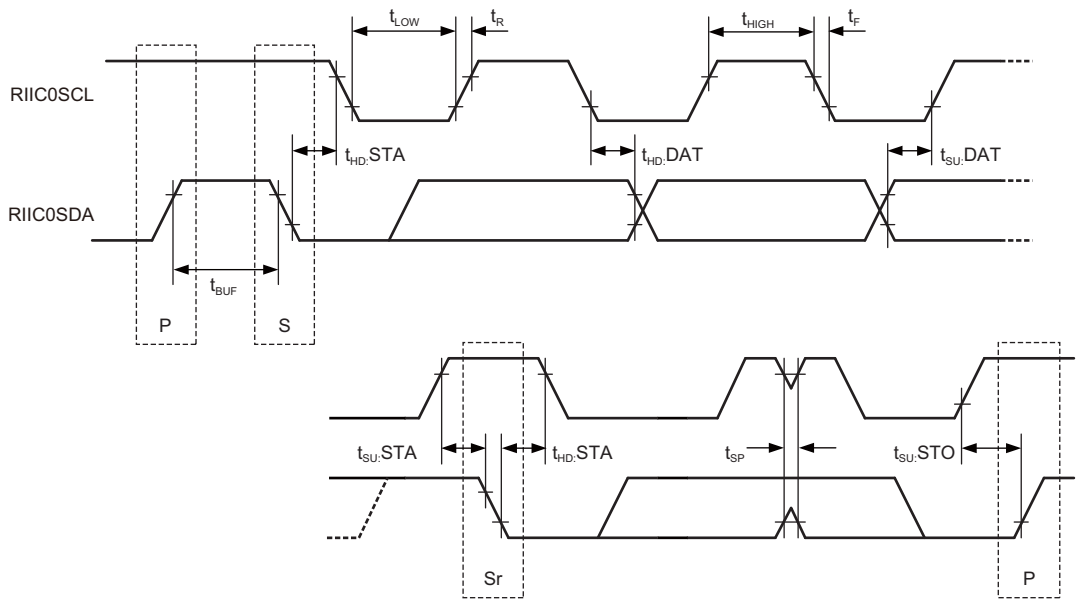
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RIIC0SCL clock low-level width	t_{LOW}		1.3			µs
RIIC0SCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		100*4			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 4. The fast mode IIC bus can be used in normal mode IIC bus system. In this case, set the fast mode IIC bus so that it meets the following conditions.
- If the system does not extend the RIIC0SCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIIC0SCL signal's low state hold time:
Transmit the following data bit to the RIIC0SDA line prior to releasing the RIIC0SCL line (1250 ns: Normal mode IIC bus specification).



Note: P: Stop condition
S: Start condition
Sr: Restart condition

1.23 FlexRay Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

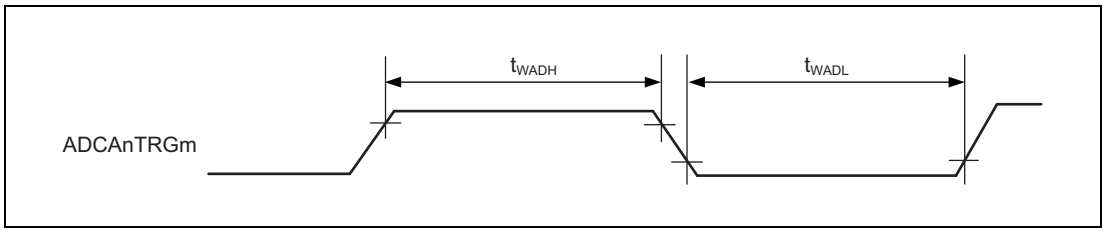
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					10	Mbps

1.24 ADTRG Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high / low level width	t_{WADH} / t_{WADL}		k × Tsamp + 20 *1			ns

Note 1. k: Sampling number of the digital noise filter (DNFA_xxx) for each input.
Tsamp: Sampling time of the digital noise filter (DNFA_xxx) for each input.



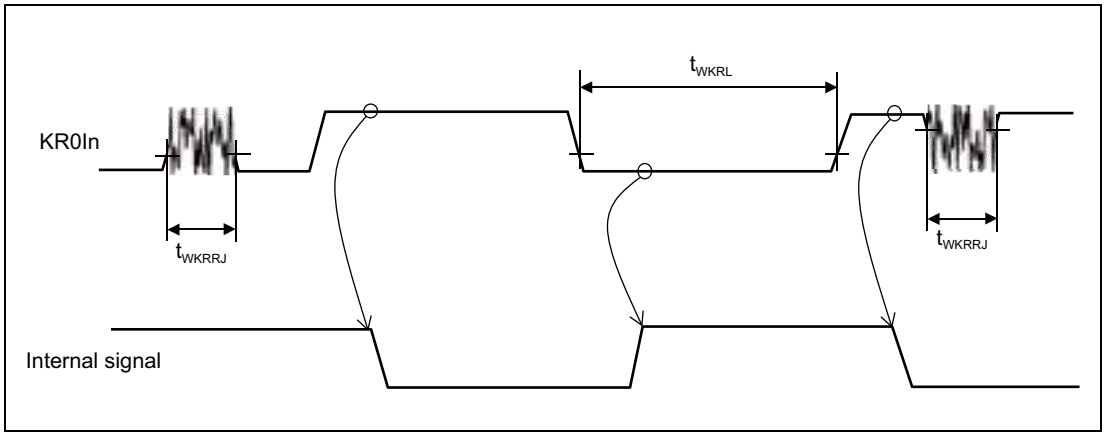
1.25 Key Return Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



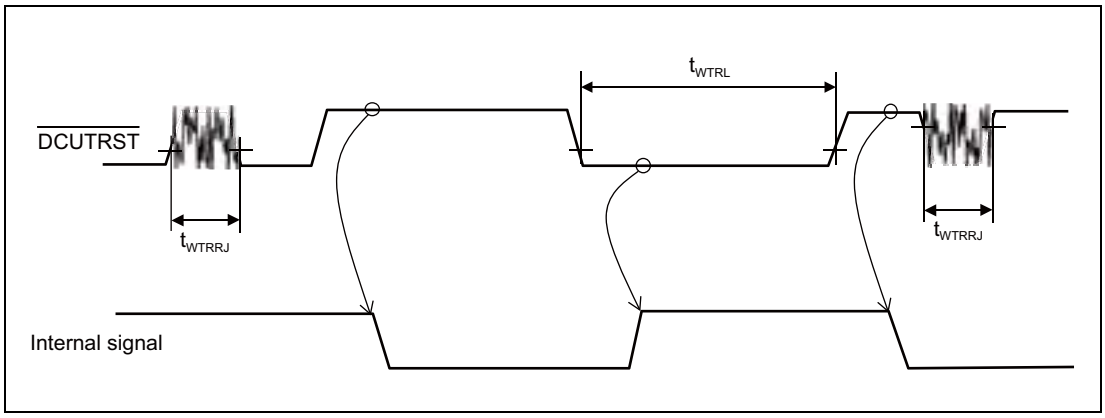
1.26 $\overline{\text{DCUTRST}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input low level width*1	t_{WTRL}		600			ns
$\overline{\text{DCUTRST}}$ pulse rejection*2	t_{WTRRJ}		100			ns

Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



1.27 Debug Interface Characteristics

1.27.1 Nexus Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

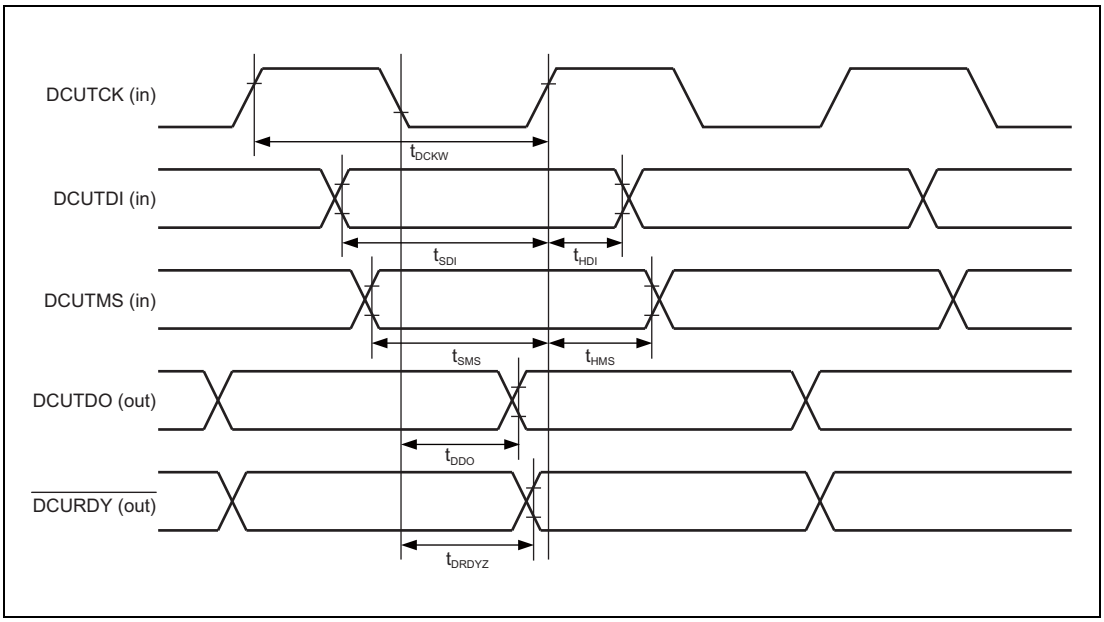
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTCK ↑)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK ↑)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK ↑)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK ↑)	t_{HMS}		3			ns
DCUTDO delay time (↓ DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (↓ DCUTCK)	t_{RDYZ}		0		20	ns



1.27.2 LPD (4 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, BVCC = 3.0 to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

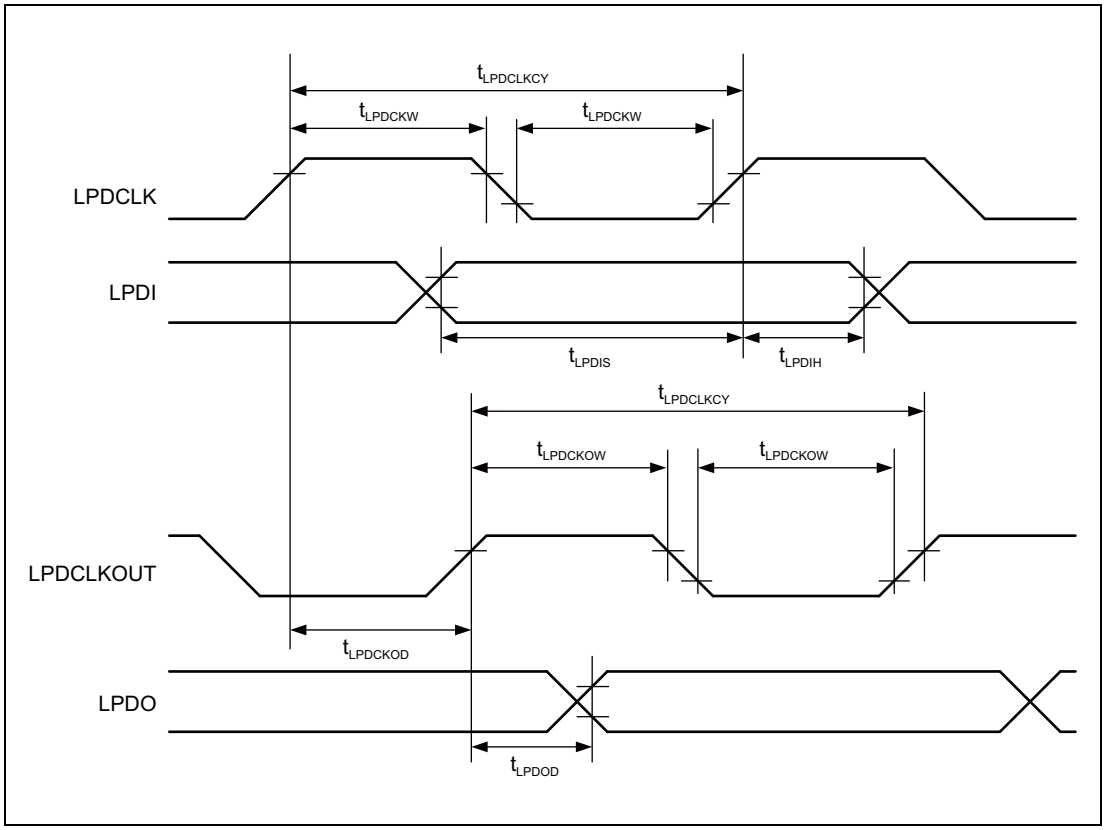
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max. 12 MHz)			ns
LPDCLK High-level width / LPDCLK Low-level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT High-level width / LPDCLKOUT low-level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns



1.27.3 LPD (1 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 50 pF

<Input buffer>

LPDIO: TTL

<Output driver strength>

LPDIO: Fast mode

<External pull-up resistor>

LPDIO: 4.7 kΩ to 10 kΩ

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) baud rate					2.0	Mbps

1.28 Flash Programming Characteristics

1.28.1 Code Flash

The code flash memory is shipped in the erase state. If the code flash memory is read where it has not been written after ensure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Table 1.19 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		4*4		30	MHz
Number of rewrites*1	CWRT	Data retention: 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful ensure of the code flash memory.

Note 3. f_{PCLK} = 1/4 f_{CPUCLK}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.20 Programming Characteristics (1/2)

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	256 B		0.4*1	6*1	ms
			8 KB		20	90	ms
			32 KB		80	360	ms
			256 KB		0.6	2.7	s
			384 KB		0.9	4.1	s
			512 KB		1.2	5.4	s
			768 KB		1.7	8.1	s
			1 MB		2.3	10.8	s
			1.5 MB		3.4	16.2	s
			2 MB		4.5	21.5	s
			3 MB		6.8	32.3	s
			4 MB		9	43	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		0.5*1	7.2*1	ms
			8 KB		24	108	ms
			32 KB		96	432	ms
			256 KB		0.7	3.3	s
			384 KB		1.1	4.9	s
			512 KB		1.4	6.5	s
			768 KB		2.1	9.8	s
			1 MB		2.7	13	s
			1.5 MB		4.1	19.5	s
			2 MB		5.4	26	s
			3 MB		8.1	39	s
			4 MB		10.8	52	s

Table 1.20 Programming Characteristics (2/2)

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Erase time		f_{PCLK} ≥ 20MHz CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
			1.5 MB		6.8	21	s
			2 MB		9	28	s
			3 MB		13.6	42	s
			4 MB		18.1	56	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s
			1.5 MB		8.1	25.2	s
			2 MB		10.8	33.6	s
			3 MB		16.2	50.4	s
			4 MB		21.6	67.2	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.28.2 Data Flash

The data flash memory is shipped in the erase state. If the data flash memory is read where it has not been written after ensure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Table 1.21 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		4*4		30	MHz
Number of rewrites*1	CWRT	Data retention: 20 years*2	125 k			times
		Data retention: 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. f_{PCLK} = 1/4 f_{CPUCLK}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.22 Programming Characteristics

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.16*1	1.7*1	ms
			64 KB		2.79	13.44	s
Erase time		f_{PCLK} ≥ 20 MHz	64 B		1.7*1	10*1	ms
			64 KB		1.74	10.24	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100*1	µs
			64 KB			70.4	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.28.3 Serial Programming Interface

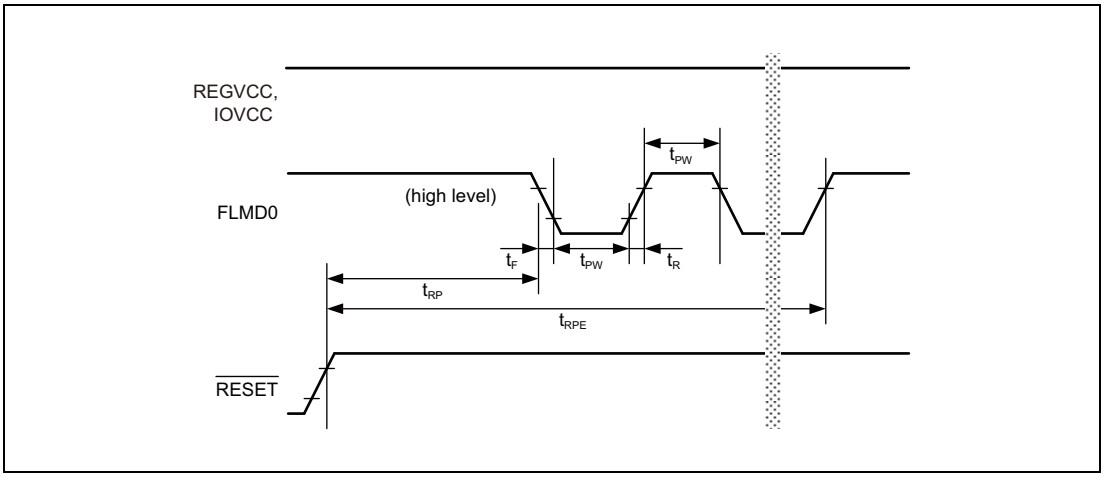
1.28.3.1 Serial Programmer Setup Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				101.5	ms
FLMD0 low/high level width	t_{PW}		1.6			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

NOTE

IOVCC: EVCC = BVCC = A0VREF = A1VREF



1.28.3.2 FLSCI3 Interface

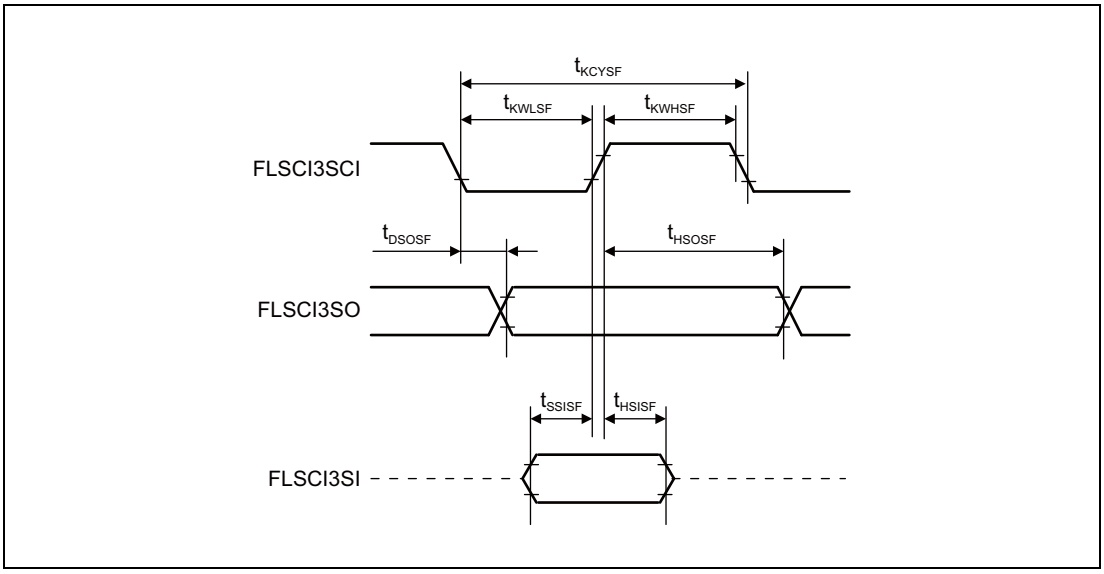
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLSCI3 transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode			1.5	Mbps
FLSCI3SCI cycle time	t_{KCYSF}	3-wired Clock Sync mode	200*1			ns
FLSCI3SCI high level width	t_{KWHSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SCI low level width	t_{KWLSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SI setup time (vs FLSCI3SCI)	t_{SSISF}	3-wired Clock Sync mode	55			ns
FLSCI3SI hold time (vs FLSCI3SCI)	t_{HSISF}	3-wired Clock Sync mode	55			ns
FLSCI3SO output delay (vs FLSCI3SCI)	t_{DSOSF}	3-wired Clock Sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired Clock Sync mode Not continuous transfer (data: except 1st bit)			$-t_{KWHSF} + 3 \times t_{Pcyc} + 36$	ns
FLSCI3SO hold time (vs FLSCI3SCI)	t_{HSOSF}	3-wired Clock Sync mode	$2 \times t_{Pcyc}$			ns

Note 1. Input the external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



1.29 A/D Converter Characteristics

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Ta = –40 to (depend on the product) °C, CL = 30 pF

(1/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLKn			8*3		40	MHz
Resolution	RESn	12-bit mode		12	12	12	bit
		10-bit mode		10	10	10	bit
Conversion time	t_{CONn}	ADCAnSMPCR.SMPT[7:0] = 12H (40 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz). External MPX is not used.		1.25		5	µs
		ADCAnSMPCR.SMPT[7:0] = 18H (46 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz). External MPX is not used.		1.15		5.75	µs
		ADCAnSMPCR.SMPT[7:0] = 12H (80 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz). External MPX is used.		2.5*4		10	µs
		ADCAnSMPCR.SMPT[7:0] = 18H (92 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz). External MPX is used.		2.3*4		11.5	µs
Sampling time	t_{SMP}	ADCAnSMPCR.SMPT[7:0] = 12H (18 cycle) (8 MHz*3 ≤ ADCLKn ≤ 32 MHz)		0.56		2.25	µs
		ADCAnSMPCR.SMPT[7:0] = 18H (24 cycle) (8 MHz*3 ≤ ADCLKn ≤ 40 MHz)		0.6		3	µs
Analog input voltage	VAIN0SN	ADCAnIm	T&H not used	AnVSS		AnVREF	V
		ADCA0I0-5	T&H used	0.2		A0VREF – 0.2	V
		ADCA0ImS	A0VREF ≥ EVCC	A0VSS		EVCC	V
			A0VREF < EVCC	A0VSS		A0VREF	V
		ADCA1ImS	A1VREF ≥ BVCC	A1VSS		BVCC	V
			A1VREF < BVCC	A1VSS		A1VREF	V
Operation current	IA0VREF IA1VREF	T&H is not used			1.1	3.0	mA
		T&H used (max. 6 pins)				*2	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS IA1VREFS				1	10	µA
T&H current	ITH				0.5	1.3	mA/ch
T&H sampling time	t_{THSMP}			450			ns
T&H hold time	t_{THHOLD}					10	µs
Set up time of self diagnosis voltage circuit	t_{BOOT}			500			ns
Set up time of self diagnosis voltage level	t_{OUT}			500			ns
Pull-down resistor for Discharge mode		ADCnIm pins		350	500	650	kΩ
		ADCnImS pins		100	215	800	kΩ

(2/3)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Accuracy of Self-diagnosis function	TESH0SN	12-bit mode	Self-diagnosis voltage level = AnVREF		4015 – [TOEn]		4095	—
			Self-diagnosis voltage level = 2/3AnVREF		2651 – [TOEn]	2731	2811 + [TOEn]	—
			Self-diagnosis voltage level = 1/2AnVREF		1968 – [TOEn]	2048	2128 + [TOEn]	—
			Self-diagnosis voltage level = 1/3AnVREF		1285 – [TOEn]	1365	1445 + [TOEn]	—
			Self-diagnosis voltage level = AnVSS		0		80 + [TOEn]	—
		10-bit mode	Self-diagnosis voltage level = AnVREF		1003 – [TOEn]		1023	—
			Self-diagnosis voltage level = 2/3AnVREF		663 – [TOEn]	683	703 + [TOEn]	—
			Self-diagnosis voltage level = 1/2AnVREF		492 – [TOEn]	512	532 + [TOEn]	—
			Self-diagnosis voltage level = 1/3AnVREF		321 – [TOEn]	341	361 + [TOEn]	—
			Self-diagnosis voltage level = AnVSS		0		20 + [TOEn]	—
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±4.0	LSB
				ADCA0I0-5 (w/ T&H)			±6.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±6.0	LSB
				ADCA0I0-5 (w/ T&H)			±8.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±8.0	LSB
				ADCA0I0-5 (w/ T&H)			±10.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±2.0	LSB
				ADCAnImS			±3.0	LSB
Integral nonlinearity error*1	ILEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±2.0	LSB
				ADCA0I0-5 (w/ T&H)			±3.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±3.0	LSB
				ADCA0I0-5 (w/ T&H)			±4.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±4.0	LSB
				ADCA0I0-5 (w/ T&H)			±5.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Differential nonlinearity error*1	DLEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±1.0	LSB
				ADCA0I0-5 (w/ T&H)			±2.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±3.0	LSB
				ADCA0I0-5 (w/ T&H)			±4.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±3.0	LSB
				ADCA0I0-5 (w/ T&H)			±4.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.0 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB

(3/3)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Zero scale error*1 (offset error)	ZSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±3.5	LSB
				ADCA0I0-5 (w/ T&H)			±5.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±5.5	LSB
				ADCA0I0-5 (w/ T&H)			±7.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±7.5	LSB
				ADCA0I0-5 (w/ T&H)			±9.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
Full scale error*1	FSEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm (w/o T&H)			±3.5	LSB
				ADCA0I0-5 (w/ T&H)			±5.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm (w/o T&H)			±5.5	LSB
				ADCA0I0-5 (w/ T&H)			±7.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm (w/o T&H)			±7.5	LSB
				ADCA0I0-5 (w/ T&H)			±9.5	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±0.5	LSB
				ADCAnImS			±1.5	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB

Note 1. This does not include quantization error.

Note 2. 3 + 1.3 × (the number of used T&H)

Note 3. Include the oscillation accuracy of HS IntOSC.

Note 4. When the external multiplexer is used, the detail time of A/D conversion is MPX setup time, sampling time and successive approximation time. MPX setup time is same as “sampling time + successive approximation time”.

Note 5. Conversion accuracy when ADCA0ImS terminal is converted in 12-bit mode: Conversion accuracy can be applied if lower 2-bit is ignored from conversion result.

CAUTION

When an external digital pulse is applied to AP0, AP1, P8, P9, P18 and P19 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse.

The same behavior may apply when the digital buffer is used as output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

1.30 Injection Currents

Table 1.23 Definition of Pin Group (233 pin)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P3, P20
PgB	BVCC, BVSS	P10, P11, P12, P13
PgE'	EVCC, EVSS	P8, P9
PgB'	BVCC, BVSS	P18, P19
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 1.24 Definition of Pin Group (176 pin)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P2, P20
PgB	BVCC, BVSS	P10, P11, P12
PgE'	EVCC, EVSS	P8, P9
PgB'	BVCC, BVSS	P18
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

Table 1.25 Definition of Pin Group (144 pin)

Symbol	Power Supply for Pin Group	Pin
PgR	REGVCC, AWOVSS	IP0_0
PgE	EVCC, EVSS	JP0, P0, P1, P20
PgB	BVCC, BVSS	P10, P11, P12
PgE'	EVCC, EVSS	P8, P9
PgB'	BVCC, BVSS	P18
PgA0	A0VREF, A0VSS	AP0
PgA1	A1VREF, A1VSS	AP1

1.30.1 Absolute Maximum Ratings

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			total			60	mA
		PgB	Per pin			10	mA
			total			60	mA
		PgE’	Per pin			10	mA
			Total			60	mA
		PgB’	Per pin			10	mA
			total			60	mA
		PgA0	Per pin			10	mA
			total			60	mA
		PgA1	Per pin			10	mA
			total			60	mA
		PgR	Per pin			10	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			total			–60	mA
		PgB	Per pin			–10	mA
			total			–60	mA
		PgE’	Per pin			–10	mA
			Total			–60	mA
		PgB’	Per pin			–10	mA
			total			–60	mA
		PgA0	Per pin			–10	mA
			total			–60	mA
		PgA1	Per pin			–10	mA
			total			–60	mA
		PgR	Per pin			–10	mA

CAUTIONS

1. The DC injection current (total) must satisfy the specifications of the injection current per pin.
2. In case of injected current for PgA0 and PgA1, TESH0SN cannot be kept. Its deviating value will increase sharply with increasing absolute value of injection current.

1.30.2 DC Characteristics for Overload Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgB	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgB’	Per pin			3	mA
			total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
		PgA1	Per pin			3	mA
			Total			20	mA
		PgR	Per pin			2	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgB	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgB’	Per pin			–3	mA
			total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA
		PgA1	Per pin			–3	mA
			Total			–20	mA
		PgR	Per pin			–2	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

1.30.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Leakage current coupling factor for positive overload current	K_{INJP}	PgE	Per pin			3.0×10^{-6}	—
		PgB	Per pin			3.0×10^{-6}	—
		PgE’	Per pin			3.0×10^{-6}	—
		PgB’	Per pin			3.0×10^{-6}	—
		PgA0	Per pin			4.8×10^{-6}	—
		PgA1	Per pin			4.8×10^{-6}	—
		PgR	Per pin			3.0×10^{-6}	—
Leakage current coupling factor for negative overload current	K_{INJN}	PgE	Per pin			7.5×10^{-6}	—
		PgB	Per pin			7.5×10^{-6}	—
		PgE’	Per pin			7.5×10^{-6}	—
		PgB’	Per pin			7.5×10^{-6}	—
		PgA0	Per pin			2.6×10^{-6}	—
		PgA1	Per pin			2.6×10^{-6}	—
		PgR	Per pin			7.5×10^{-6}	—

NOTES

1. This is reference value.
2. An overload current through a pin will cause a certain error current in the adjacent pins. This error current must be added to the respective leakage current (ILIH or ILIL) of the adjacent pins.
3. The amount of error leakage current depends on the overload current and is defined by the overload coupling factor K_{INJ}.
   The total current through a pin is:
   $| I_{total} | = |$ ILIH or ILIL $| + (| I_{INJn} | \times K_{INJn})$

1.30.4 AD Characteristics for Pins Influenced by Injected Current on an Adjacent Pin

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Degradation of overall error[*1]	I_{INJP}	Par = 3 mA	ADCAnIm			±1.3	LSB
			ADCAnImS			±1.3	LSB
		Total = 20 mA	ADCAnIm			±3.8	LSB
			ADCAnImS			±3.8	LSB
	I_{INJN}	Par = 3 mA	ADCAnIm			±1.4	LSB
			ADCAnImS			±1.4	LSB
		Total = 20 mA	ADCAnIm			±4.5	LSB
			ADCAnImS			±4.5	LSB

Note 1. This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Note 2. This is reference value.

CAUTION

When there is an increased leakage current on the analog input pins, based on currents injected into the pins adjacent to the converted channel, the effect on the ADC accuracy depends on the external analog source impedance.

[Example] Conditions: A0VREF = 5.0 V, external analog source impedance = 10 kΩ.

If there is a leakage current of 1 µA by injected current, the effect on the ADC accuracy is 1 (µA) × 10 k (Ω) / 5 (V) = 0.2%FSR

1.31 Thermal Characteristics

1.31.1 Parameters

Package	Item	Symbol	Estimate	Unit	Note
233 pin FPBGA	Thermal Resistance	Θja	20	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	15		
176 pin LQFP	Thermal Resistance	Θja	31	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	24		
144 pin LQFP	Thermal Resistance	Θja	32	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	24		

Note: The thermal resistance depend on the usage environment.

1.31.2 Assumed Board

Conforming to JESD51-7 (4 layers)

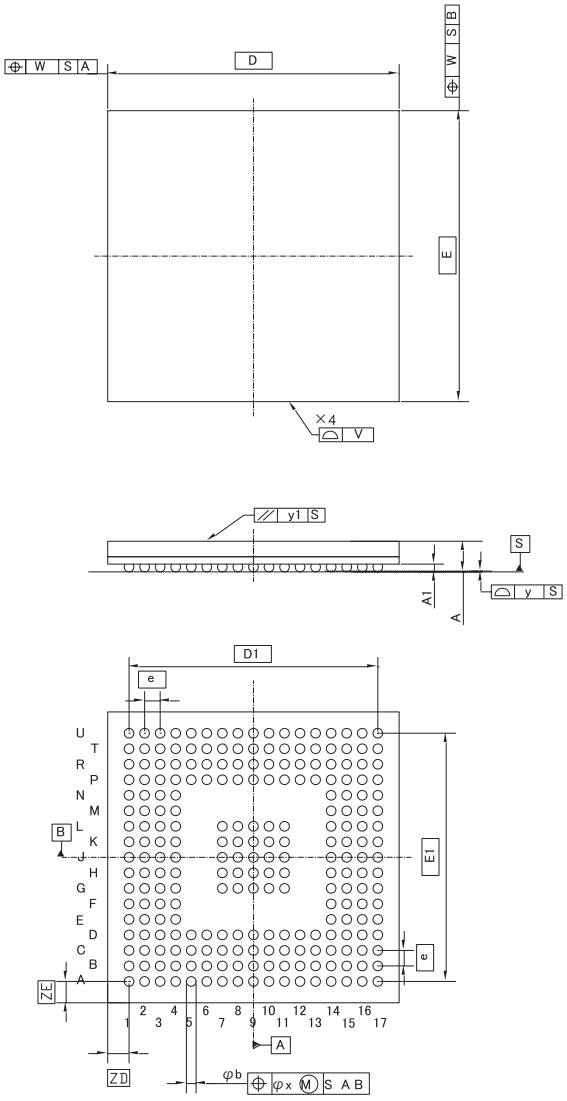
	Board size (mm)		
	X	Y	Area (mm^2)
Board	76.2	114.3	8709.66
Remaining copper rates	Thickness of conductors		
50-95-95-50%	70-35-35-70 µm		

Section 2 Package Dimensions

2.1 233 pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA233-15x15-0.80	PRBG0233GA-A	-	0.75

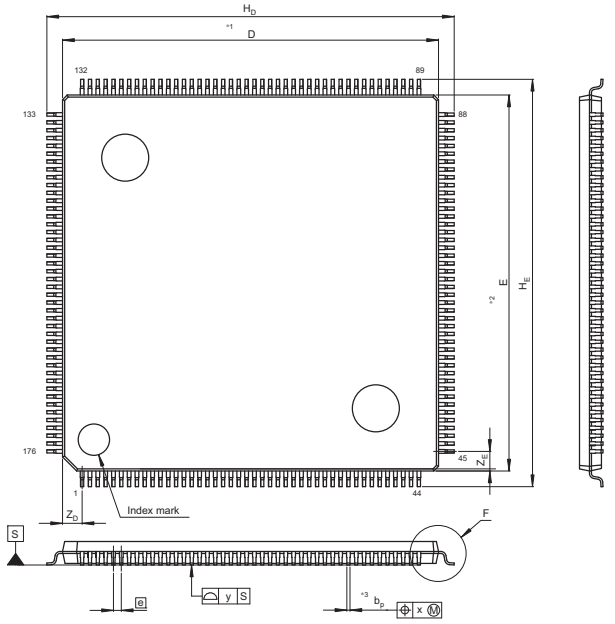
Unit:mm

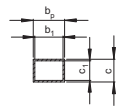


Referance Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	15.00	—
D1	—	12.80	—
E	—	15.00	—
E1	—	12.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	1.90
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

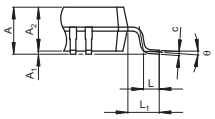
2.2 176 pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





Terminal cross section



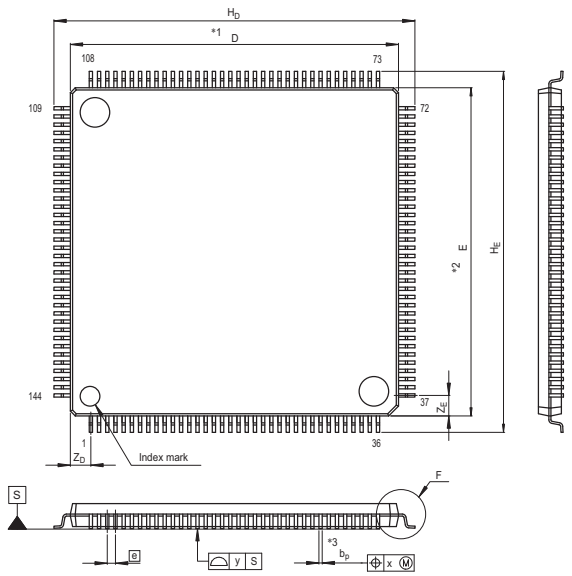
Detail F

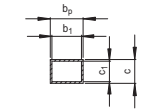
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

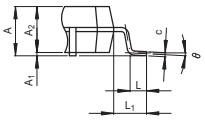
2.3 144 pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	RH850/F1M Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Nov 04, 2014	—	First Edition issued
0.50	Feb 27, 2015	1 to 5	Product Introduction, added
		6	1.1 Overview, changed
		6	1.1.1.1 233-Pin, 1.1.1.2 172-Pin and 1.1.1.3 144-Pin: Section title and description added
		7	1.1.2.1 Common Conditions: Description of operating temperature, changed
		10	1.2.3 Port Current: Note, changed
		11, 12	1.2.3.1 233-Pin: Section title and Table 1.1 Port Current (233-Pin), added
		13, 14	1.2.3.2 172-Pin: Section title and Table title, added
		15, 16	1.2.3.3 144-Pin: Section title and Table 1.3 Port Current (144-Pin), added
		16	1.2.4 Temperature Condition, changed
		17, 18	1.4 Operational Condition: Note 4., added
		18	1.5 Oscillator Characteristics, changed
		19	Figures MainOSC and SubOSC, added
		19	1.6 Internal Oscillator Characteristics, changed
		20	1.7.1 PLL0 (for CPU) Characteristics, changed
		21	1.7.2 PLL1 (for Peripheral) Characteristics, changed
		22	1.8.1 Regulator Characteristics, changed
		23	1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics, changed
		24	Figure <POC>, changed
		25	Figure <VLVI>, changed
		25	Figure <CVM>, added
		26	Table 1.4 In case the $\overline{\text{RESET}}$ pin is used, changed
		27	Table 1.5 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin, changed
		28	Table 1.6 In case the $\overline{\text{RESET}}$ pin is not used and fixed to high level by pull-up[*1], changed
		30	1.8.4 CPU Reset Release Timing, changed
		30 to 36	1.9 Pin Characteristics, changed
		37, 38	1.9.1.1 233-Pin: Section title and Table 1.9 Output Current (233-Pin), added
		39, 40	1.9.1.2 177-Pin: Section title and Table title, added
		41, 42	1.9.1.3 144-Pin: Section title and Table 1.11 Output Current (144-Pin), added
		43, 44	1.10 Power Supply Currents, changed
		45	1.11 MEMC0CLK Timing, changed
		46	1.12.1 MEMC0CLK Asynchronous, changed
		49	1.12.2 MEMC0CLK Synchronous, changed
		55	1.17 Mode Timing: Note 2, changed
		55	1.17 Mode Timing: Note 3, added
		57	1.18 Timer Timing: Figure, changed
		70	1.22 RIIC Timing, changed
		73	1.24 ADTRG Timing: Note 1, changed
		79, 80	Table 1.19 Programming Characteristics, changed
		81	1.28.2 Data Flash, changed
		81	Table 1.21 Programming Characteristics, changed
		82	1.28.3.1 Serial Programmer Setup Timing, changed
		84 to 86	1.29 A/D Converter Characteristics, changed
		87	1.30 Injection Currents, changed
		88	1.30.1 Absolute Maximum Ratings, changed
		89	1.30.2 DC Characteristics for Overload Current, changed
		90	1.30.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin, changed

Rev.	Date	Description	
		Page	Summary
0.50	Feb 27, 2015	91	1.30.4 AD Characteristics for Pins Influenced by Injected Current on an Adjacent Pin, changed
		92 to 94	Section 2 Package Dimensions: Section title and figures added (233-Pin and 144-Pin)
1.00	Jun 30, 2015	1	typo (AD → A/D, master/a slave → master/slave)
		2,11,12,38,39,89,95	description alignment (233-pin → 233 pin)
		3,13,14,40,41,89,96	description alignment (176-pin → 176 pin)
		4,15,16,42,43,89,97	description alignment (144-pin → 144 pin)
		6	removed "Preliminary"
		6	description alignment (removed "Related pins/port" for Pg R)
		7,18,20,21,22,23,26,30,36,46,47,50,53,54,55,56,57,58,60,61,62,72,74,75,76,77,78,79,80,83,84,85,86	description alignment (AWOVCL → CAWOVCL, ISOVCL → CISOVCL)
		8	description alignment (added "it is recommended" for CAUTION)
		8	description alignment (min. → MIN., max. → MAX.)
		10	Addition of "P13" for GPIO list
		11,12,13,14,15,16	Table 1.1/2/3, description alignment ("Per side")
		16	description alignment (renamed "Product Introduction" → "Product Lineup")
		17	typo (FLC → FLXA, OSTM → OSTMn)
		18,20,44,45,53,56,88	description alignment (IntOsc → IntOSC)
		18	correction of "MainOsc oscillation operation point" level (MIN:2.4->empty, TYP.:empty->0.5xREGVCC)
		18	Addition of "MainOsc oscillation amplitude"
		18	correction of "SubOsc current consumption" (TYP:2->1.5, MAX.:8->4)
		18	correction of "SubOsc DC operating point" (MIN:2.4->empty, TYP.:empty->0.65)
		19	Improvement of figures (MainOSC and SubOSC)
		20	typo in Note 2.(PLLC0C.PLL0P2-0 bits → PLL0C.PLL0P2-0 bits)
		22	correction of "Conditon for AWOVCL"for AWO area → AWOVCL pin)
		22	correction of "Conditon for ISOVCL"(for ISO area → ISOVCL pin)
		22	correction of "Equivalent series resistance ..."(for AWO area → for CAWOVCL)
		22	correction of "Equivalent series resistance ..."(for ISO area → for CISOVCL)
		23	VCVML:1.00 → 1.1 (MIN.), 1.05 → 1.15 (TYP.), 1.10 → 1.20 (MAX.)
		23	description alignment for "Note 5": '"=0.02 V/ms to 500 V/ms" → ":0.02 V/ms <= T_{VS} <= < 500 V/ms")
		23	addition of "Caution"
		26,27	correction of Power Up/Down timing (FLMD0 hold time, FLMD0 setup time)
		26,27	case separation for timing whether in serial programming mode or except serial programming mode
		26	removed "Note 2" which explained handling of FLMD0 and FLMD1
		27	Improvement of figure (timing chart)
		28	removed "FLMD0,1 hold time" spec
		28	correction of MIN value for t_{DMDPD} (0 → 1)
		28	Improvement of explanation for "Note 1" (added "include self-programming mode")

Rev.	Date	Description	
		Page	Summary
1.00	Jun 30, 2015	32	correction: RESET/SHMT2 : with *4 → w/o *4 RESET/Pull-down : w/o *4 → with *4
		31,32,33,34,35	Pin Characteristics table have been updated
		35	addition of "Caution"
		48,49,51,52	description alignment: (out → output) (in → input)
		53,54,57,58,75, 76	addition for Note 2 (page 53,54,57,75,76), Note 4 (page 58), "Noise such as the figure can be filtered"
		53	description alignment (Low Speed Internal Oscillator → LS IntOSC)
		53	description alignment (High Speed Internal Oscillator → HS IntOSC)
		54,55	description alignment with another F1x products (timing is not changed)
		56	description alignment with another F1x products. separation for high level width and low level width. Addition Note 2 and Note 3.
		57	correction of Note 2. removed Note 3
		59	addition of t_{WENTIH} , t_{WENTIL}
		62	description alignment of bit number ("CSIHnCFG0-7.CSIHnID2-0" → "CSIHnCFGx.CSIHnID[2:0]") ("CSIHnCFG0-7.CSIHnSP3-0" → "CSIHnCFGx.CSIHnSPx[3:0]") ("CSIHnCFG0-7.CSIHnHD3-0" → "CSIHnCFGx.CSIHnHDx[3:0]")
		62	correction of register name which is used as "Condition" CSIHnCFG7-0.CSIHnCKP0-7 → CSIHnCFGx.CSIHnCKPx
		73	description alognment (subindex:STA, DAT, STO)
		80,83	addition "Note 4. Only for program/erase operation."
		84	removed t_{DPOR}, t_{SMDR}, t_{HMDR}, t_{SU}
		84	improvement of time chart
		86	description alignment : (T_{THSMP} → t_{THSMP}) (T_{THHOLD} → t_{THHOLD}) (T_{BOOT} → t_{BOOT}) (T_{OUT} → t_{OUT})
		87	description alignment : (LSB → -)
		88	addition "Note 5", CAUTIONS sentence 2
		89	addition of "P19" for PgB'
		93	addition of "ADCAnImS" for "Total = 20mA"
		94	addition "1.31 Thermal Characteristics"
1.11	May 23, 2016	18	addition spec: "V_{MOSCSP}" changed spec :1*3→0.4 x REGVCC - 0.2*3
		19	changed figure: MainOSC: Addition (V_{MOSCSP})
		23	addition of Note 8 for Detection voltage
		26	removed FLMD0 setup time
		26	addition of Note 2 for figure
		88	correction of CAUTION
		22	correction of 1.8.1 Regulator Characteristics addition of Note 3
		23	correction of 1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

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