RH850/U2B

Renesas microcontroller

Section 1 Overview

The RH850/U2B-EVA, U2B-FCC, U2B10 and U2B6 are products of the single-chip microcontroller RH850 series from Renesas Electronics.

This section gives an overview of the RH850/U2B-EVA, U2B-FCC, U2B10 and U2B6.

1.1 Outline

This RH850/U2B is a 32-bit single-chip microcontroller with multiple CPUs, Code Flash, Data Flash, RAM modules, DMA controllers, A/D converters, timer units and many communication interfaces that are used in the automotive applications. This microcontroller conforms to the Automotive Safety Integrity Level (ASIL) that is highly demanded in the recent automotive field (ASIL D level).

RH850/U2B main features are as follows:

(1) **RH850 multi-core CPU**

This microcontroller contains multi RH850G4MH2 cores support RISC-type instruction sets and have significantly improved the instruction execution speed with basic instructions (one clock cycle per instruction) and the optimized 10-stage pipeline configurations. Furthermore, this product also supports multiplication instructions using a 32-bit hardware multiplier, saturated product-sum operation instructions, and bit manipulation instructions as instructions best suited for various fields.In addition, this product also support CPU virtualization function. Two-byte basic instructions and high-level language instructions improve object code efficiency for the C compiler and reduce the program size. Furthermore, this product is suited for advanced real-time control applications by offering a high-speed response time including the processing time of the onchip interrupt controller.

(2) **On-Chip Code Flash and Data Flash**

This microcontroller has high-speed Code Flash from which CPU can fetch the instructions and the constant data. Code Flash with a capacity of up to 24MB can be reprogrammed when the chip is implemented in the application system. This chip also has Data Flash capable of EEPROM emulation with a capacity of up to 512 KB and up to 160 KB exclusively for ICUMHB.

(3) **Rich peripheral functionality**

This microcontroller supports common communication interfaces such as SPI as well as automotive-oriented communication interfaces such as Ethernet, RHSIF, FlexRay, CAN-FD, LIN, SENT and PSI5. As internal peripheral modules, this microcontroller incorporates A/D Converter, System Timer, Generic Timer Module, and a dedicated Peripheral Interconnection module which connects the functionalities of these peripherals.

(4) **Functional Safety support**

This microcontroller includes several dedicated functionalities such as Dual-Core Lockstep configuration for CPU, the memory protection with ECC/EDC on data and the address feedback mechanism, the bus protection with ECC/EDC on data and address, the peripheral module protection, and clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(5) **Security support**

This microcontroller supports various security features. The Intelligent Cryptographic Unit - Master (ICUMHB) has a dedicated secure CPU (RH850 G3K) and some secure peripherals such as AES engines, a public key cryptography coprocessor, an engine that supports a HASH function based on SHA and Random Number Generator (RNG). This microcontroller also realizes the HW-level domain separation between non-secure and secure domains. The internal resources such as Code and Data Flash can be assigned to either a non-secure or secure domain, and the secure domain is protected against non-secure accesses by the HW mechanism. This microcontroller also has the protection scheme for debug and test functionality.

1.2 Application Fields

Automotive field (including body control, chassis & safety, engine control system and transmission control system)

1.3 Ordering Information

Table 1.1 Product Name List

Product Name	Package	On-Chip ROM	Operating Temperature (Tj)	External Oscillator	Maximum Operating Frequency	ADCK restriction*1 RAM restriction*2	Note
R7F70254*FABG-C (RH850/U2B10)	Plastic FBGA-468 0.8-mm ball pitch 25 mm × 25 mm	10 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70254*FABA-C (RH850/U2B10)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	10 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70254*FABB-C (RH850/U2B10)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	10 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70254*AFABG-C (RH850/U2B10)	Plastic FBGA-468 0.8-mm ball pitch 25 mm × 25 mm	10 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70254*AFABA-C (RH850/U2B10)	Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm	10 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70254*AFABB-C (RH850/U2B10)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	10 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70255*FABB-C (RH850/U2B6)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	6 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	Yes	*3
R7F70255*AFABB-C (RH850/U2B6)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	6 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—
R7F70255*BFABB-C (RH850/U2B6)	Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm	6 MB	max. 160°C	16/20/24/25/40 MHz	400 MHz	No	—

Note 1. Refer to RH850/U2B Group User's Manual:Hardware **Section 50.12, ADCK restriction**.

Note 2. Refer to RH850/U2B Group User's Manual:Hardware **Section 64.5, RAM restriction**.

Note 3. As sales of these products is limited, please contact your sales representative first when considering these products for purchasing and project development.

FBGA is hereafter referred to as BGA unless the complete abbreviation is required.

The RH850/U2B-FCC has 8 variants. Select the proper product according to the table below.

Table 1.2 RH850/U2B-FCC, EVA List

Frequency	Package			
	FCBGA-600	FCBGA-468	FCBGA-373	FCBGA-292
400 MHz	R7F702Z2*ADBG (For EVA)	R7F702Z2*EDBG (For U2B24) R7F702Z2*EDBG (For U2B10)	R7F702Z2*EDBA (For U2B24) R7F702Z2*EDBA (For U2B10)	R7F702Z2*EDBB (For U2B10) R7F702Z2*EDBB (For U2B6)

1.4 Differences in the Specifications of RH850/U2B

The table below lists the differences in the specifications of RH850/U2B.

Table 1.3 Device Overview Table (1/3)

Feature		RH850 U2B24	RH850 U2B10	RH850 U2B6
Core	Main Core/Lockstep in performance config	6/4	4/2	3/2
	Main Core/Lockstep in safety config	5/5	3/3	3/2
	FPU performence config/safety config	6/5 (each main core)	4/3 (each main core)	3 (each main core)
	FXU (FP-SIMD)	2	FCC/EVA:2 MP:1	1
	MPU Region	32	32	32
	Frequency	400MHz	400MHz	400MHz
System	Virtualization	Yes	Yes	Yes
	QoS	Yes	Yes	-
Flash	Code Flash	24Mbyte	10Mbyte	6Mbyte
	Data Flash (EEPROM emulation)	512Kbyte	256Kbyte	128Kbyte
	Data Flash (HSM)	160Kbyte	64Kbyte	64Kbyte
SRAM	Total (CRAM + LRAM)	4096Kbyte	1280Kbyte	576Kbyte
	Local Data (LRAM)	64Kbyte/core	64Kbyte/core	64Kbyte/core
	Cluster (CRAM)	3712Kbyte	1024Kbyte	384Kbyte
	Standby RAM (included in CRAM)	128Kbyte	128Kbyte	32Kbyte
	Instruction Cache	16Kbyte/core	16Kbyte/core	16Kbyte/core
		(PBS 4way)	(PBS 4way)	(PBS 4way)
	Data Cache (Flash only)	4lines (256bit/line)	4lines (256bit/line)	4lines (256bit/line)
	Emulation RAM	(7MByte*1)	(6MByte*1)	(5MByte*1)
	Instrumentation RAM	- (96KByte*1)	- (96KByte*1)	- (96KByte*1)
	Trace RAM	- (64KByte*1)	- (64KByte*1)	- (64KByte*1)
DMA	Channels (sDMAC/DTS)	32/128	32/128	16/128
SAR ADC	Modules	5	4	3
	Total inputs	96	96	64
	Virtual channels per module	64	64	64
Delta Sigma ADC	Modules	10	10	4
	Total inputs	38	38	18
Cyclic ADC	Modules	1	1	-
	Total inputs	8	8	-
DSMIF*3	Unit	2	2	-
	Channel	4	4	-
RDC	RDC3AL	-	-	2
	RDC3AS	2	2	-

Table 1.3 Device Overview Table (2/3)

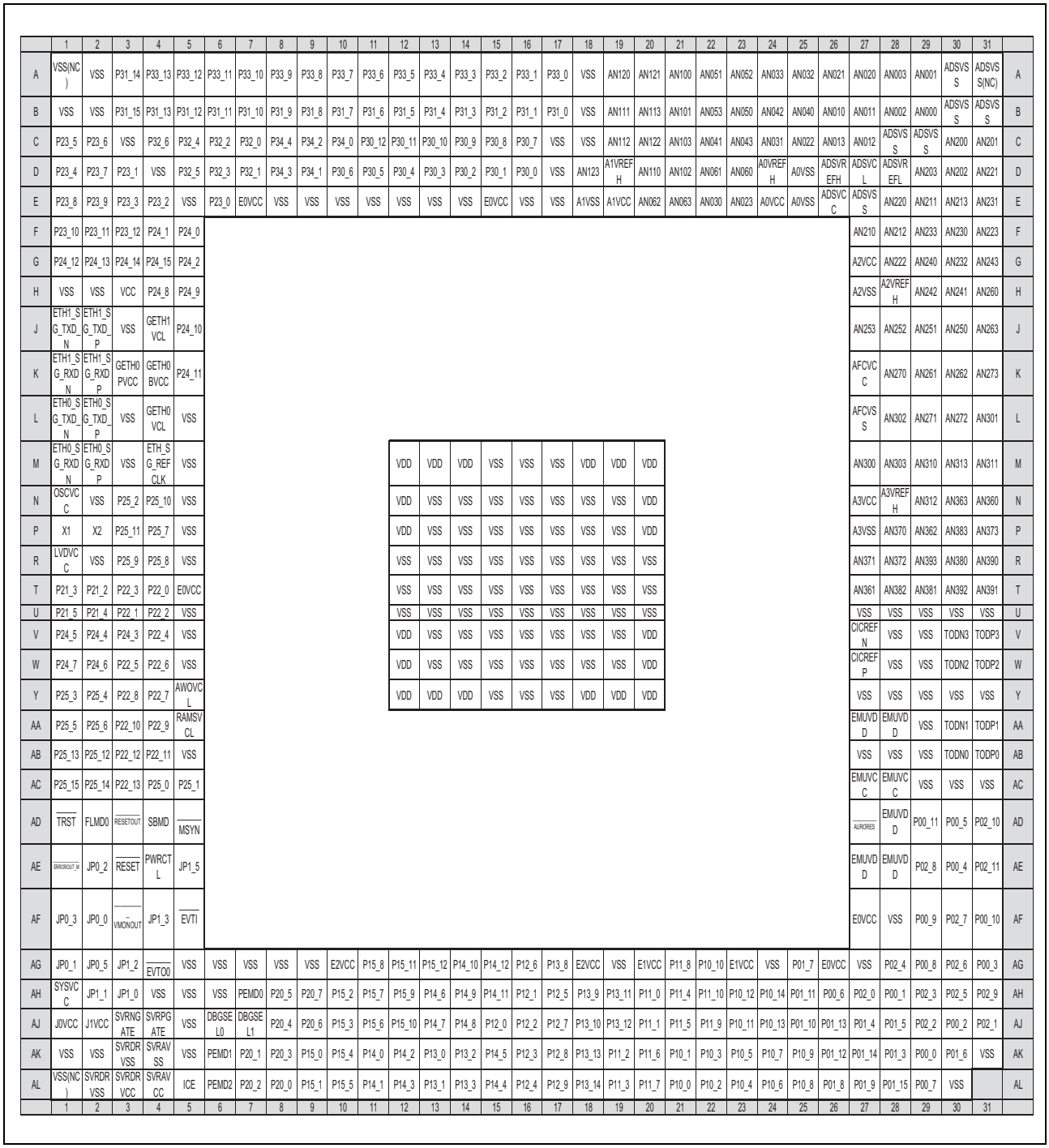
Feature		RH850 U2B24	RH850 U2B10	RH850 U2B6
Fast comparator	Modules	1	1	1
	Comparator	10	4	4
	DAC	10	4	4
Timer (GTM)	GTM	1	1	1
Timer (ATU-VI)	Timer A	8	8	6
	Timer B	1	1	1
	Timer C	External: 44 Internal: 16	External: 36 Internal: 8	External: 16 Internal: 4
	Timer D	24 w/MSF* 24 w/o MSF* *MSF: Multi Shot Pulse Function	20 w/MSF* 12 w/o MSF* *MSF: Multi Shot Pulse Function	8 w/MSF* 8 w/o MSF* *MSF: Multi Shot Pulse Function
	Timer E	40	36	20
	Timer F	20	16	7
	Timer G	14	14	10
Timer	HRPWM	16	16	16
	TAPA	6	6	6
	TAUD	4	4	4
	TAUJ	2 (AWO)	-	-
	TPBA	2	2	2
	TSG3	3	3	3
	ENCA	2	2	2
	RTCA	1 (AWO	-	-
	Window Watchdog Timer (WDTB)	6 + 1 (AWO)	4	3
	Secure Watchdog Timer (SWDT)	1	1	1
	OS Timer (OSTM)	6	4	3
	Time Protection Timer (TPTM)	6	4	3
	Long-Term System Counter (LTSC)	1	1	1
Accelerator	Data Flow Processor (DFP)	DR1000C	DR1000C	-
	Digital Filter Engine (DFE) (units/channels)	2/20	2/20	2/16
	Enhanced Motor Control Unit (EMU)	-	-	2
Security	ICUMHB	Yes	Yes	Yes
	Secure RAM	64 KB	64 KB	64 KB
	Secure Data Flash	160 KB	64 KB	64 KB
	Code Flash Protection	Yes	Yes	Yes
	ACEU	2	-	-

Table 1.3 Device Overview Table (3/3)

Feature		RH850 U2B24	RH850 U2B10	RH850 U2B6
Interfaces	FlexRay Nodes [Channels]	1 [2ch]	1 [2ch]	1 [2ch]
	RS-CANFD	10	8	8
	MSPI/MSPI (LVDS)/RLIN3/RLIN3 (25Mpbs)	8/2/23/1	8/2/6/1	6/1/6/1
	RIIC	2	2	-
	RSENT/PSI5/PSI5S	30/4/2	30/4/2	10/-/-
	RHSIF/RHSB	2/4	1/3	-/2
	Ethernet (100Mb (TSN)/1Gb (TSN))	-/2	1/-	1/-
Safety	CRC	6	4	4
	Voltage monitor	Yes	Yes	Yes
	Clock monitor	Yes	Yes	Yes
	Temperature Sensor	Yes	Yes	Yes
	ECM	1	1	1
Power Management	LPS	Yes	-	-
	STBC	Yes	Yes	Yes
	STOP mode	Yes	Yes	Yes
	DeepSTOP mode	Yes	-	-
	Cyclic RUN mode/Cyclic STOP mode	Yes	-	-
	Power off standby	Yes	Yes	Yes
External Memory Interfaces	MMCA	1	1	-
	SFMA	1	1	1
Debug	Nexus-JTAG	Yes	Yes	Yes
	Trace I/F (Aurora)	(No*1)	(No*1)	(No*1)
	Low Pin Debug I/F (4-pin)	Yes	Yes	Yes
	RHSIF Debug I/F	(No*1)	(No*1)	(No*1)
	Boundary Scan	Yes	Yes	Yes
Package	FCBGA600*2	No	No	No
	FCBGA468	Yes	No	No
	FCBGA373	Yes	No	No
	BGA468	No	Yes	No
	BGA373	No	Yes	No
	BGA292	No	Yes	Yes

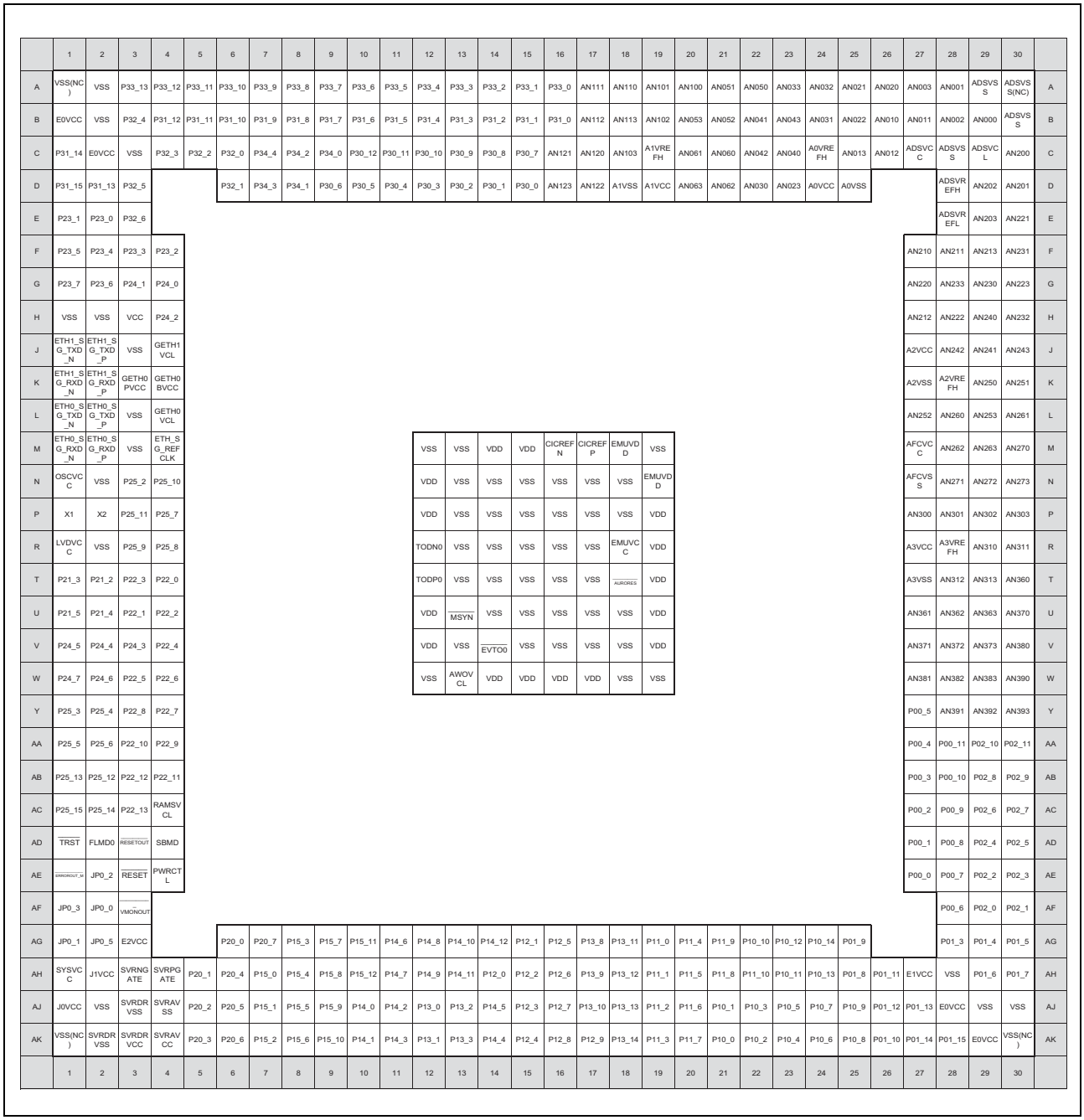
Note 1. Only FCC and EVA device is supported
Note 2. Only EVA device is supported
Note 3. FCC and EVA device is not supported

1.5 Pin Connection Diagram (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
A	VSS(NC)	VSS	P31_14	P33_13	P33_12	P33_11	P33_10	P33_9	P33_8	P33_7	P33_6	P33_5	P33_4	P33_3	P33_2	P33_1	P33_0	VSS	AN120	AN121	AN100	AN051	AN052	AN033	AN032	AN021	AN020	AN003	AN001	ADSVSS	ADSVSS(NC)	A
B	VSS	VSS	P31_15	P31_13	P31_12	P31_11	P31_10	P31_9	P31_8	P31_7	P31_6	P31_5	P31_4	P31_3	P31_2	P31_1	P31_0	VSS	AN111	AN113	AN101	AN053	AN050	AN042	AN040	AN010	AN011	AN002	AN000	ADSVSS	ADSVSS	B
C	P23_5	P23_6	VSS	P32_6	P32_4	P32_2	P32_0	P34_4	P34_2	P34_0	P30_12	P30_11	P30_10	P30_9	P30_8	P30_7	VSS	VSS	AN112	AN122	AN103	AN041	AN043	AN031	AN022	AN013	AN012	ADSVSS	ADSVSS	AN200	AN201	C
D	P23_4	P23_7	P23_1	VSS	P32_5	P32_3	P32_1	P34_3	P34_1	P30_6	P30_5	P30_4	P30_3	P30_2	P30_1	P30_0	VSS	AN123	A1VREFH	AN110	AN102	AN061	AN060	A0VREFH	A0VSS	ADSVREFH	ADSVCL	ADSVREFL	AN203	AN202	AN221	D
E	P23_8	P23_9	P23_3	P23_2	VSS	P23_0	E0VCC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	E0VCC	VSS	VSS	A1VSS	A1VCC	AN062	AN063	AN030	AN023	A0VCC	A0VSS	ADSVCC	ADSVSS	AN220	AN211	AN213	AN231	E
F	P23_10	P23_11	P23_12	P24_1	P24_0																						AN210	AN212	AN233	AN230	AN223	F
G	P24_12	P24_13	P24_14	P24_15	P24_2																						A2VCC	AN222	AN240	AN232	AN243	G
H	VSS	VSS	VCC	P24_8	P24_9																						A2VSS	A2VREFH	AN242	AN241	AN260	H
J	ETH1_SG_TXD_N	ETH1_SG_TXD_P	VSS	GETH1VCL	P24_10																						AN253	AN252	AN251	AN250	AN263	J
K	ETH1_SG_RXD_N	ETH1_SG_RXD_P	GETH0PVCC	GETH0BVCC	P24_11																						AFCVCC	AN270	AN261	AN262	AN273	K
L	ETH0_SG_TXD_N	ETH0_SG_TXD_P	VSS	GETH0VCL	VSS																						AFCVSS	AN302	AN271	AN272	AN301	L
M	ETH0_SG_RXD_N	ETH0_SG_RXD_P	VSS	ETH_SG_REFCLK	VSS																						AN300	AN303	AN310	AN313	AN311	M
N	OSCVCC	VSS	P25_2	P25_10	VSS																						A3VCC	A3VREFH	AN312	AN363	AN360	N
P	X1	X2	P25_11	P25_7	VSS																						A3VSS	AN370	AN362	AN383	AN373	P
R	LVDVCC	VSS	P25_9	P25_8	VSS																						AN371	AN372	AN393	AN380	AN390	R
T	P21_3	P21_2	P22_3	P22_0	E0VCC																						AN361	AN382	AN381	AN392	AN391	T
U	P21_5	P21_4	P22_1	P22_2	VSS																						VSS	VSS	VSS	VSS	VSS	U
V	P24_5	P24_4	P24_3	P22_4	VSS																						CICREFN	VSS	VSS	TODN3	TODP3	V
W	P24_7	P24_6	P22_5	P22_6	VSS																						CICREFP	VSS	VSS	TODN2	TODP2	W
Y	P25_3	P25_4	P22_8	P22_7	AWOVCL																						VSS	VSS	VSS	VSS	VSS	Y
AA	P25_5	P25_6	P22_10	P22_9	RAMSVCL																						EMUVDD	EMUVDD	VSS	TODN1	TODP1	AA
AB	P25_13	P25_12	P22_12	P22_11	VSS																						VSS	VSS	VSS	TODN0	TODP0	AB
AC	P25_15	P25_14	P22_13	P25_0	P25_1																						EMUVCC	EMUVCC	VSS	VSS	VSS	AC
AD	TRST	FLMD0	RESETOUT	SBMD	MSYN																						AURORES	EMUVDD	P00_11	P00_5	P02_10	AD
AE	ERROROUT_M	JP0_2	RESET	PWRCTL	JP1_5																						EMUVDD	EMUVDD	P02_8	P00_4	P02_11	AE
AF	JP0_3	JP0_0	VMONOUT	JP1_3	EVTI																						E0VCC	VSS	P00_9	P02_7	P00_10	AF
AG	JP0_1	JP0_5	JP1_2	EVTO0	VSS	VSS	VSS	VSS	VSS	E2VCC	P15_8	P15_11	P15_12	P14_10	P14_12	P12_6	P13_8	E2VCC	VSS	E1VCC	P11_8	P10_10	E1VCC	VSS	P01_7	E0VCC	VSS	P02_4	P00_8	P02_6	P00_3	AG
AH	SYSVCC	JP1_1	JP1_0	VSS	VSS	VSS	PEMD0	P20_5	P20_7	P15_2	P15_7	P15_9	P14_6	P14_9	P14_11	P12_1	P12_5	P13_9	P13_11	P11_0	P11_4	P11_10	P10_12	P10_14	P01_11	P00_6	P02_0	P00_1	P02_3	P02_5	P02_9	AH
AJ	J0VCC	J1VCC	SVRNGATE	SVRPGATE	VSS	DBGSEL0	DBGSEL1	P20_4	P20_6	P15_3	P15_6	P15_10	P14_7	P14_8	P12_0	P12_2	P12_7	P13_10	P13_12	P11_1	P11_5	P11_9	P10_11	P10_13	P01_10	P01_13	P01_4	P01_5	P02_2	P00_2	P02_1	AJ
AK	VSS	VSS	SVRDRVSS	SVRAVSS	VSS	PEMD1	P20_1	P20_3	P15_0	P15_4	P14_0	P14_2	P13_0	P13_2	P14_5	P12_3	P12_8	P13_13	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	P01_12	P01_14	P01_3	P00_0	P01_6	VSS	AK
AL	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	ICE	PEMD2	P20_2	P20_0	P15_1	P15_5	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_9	P13_14	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_8	P01_9	P01_15	P00_7	VSS		AL
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 1.1 Pin Connection Diagram U2B-EVA (FCBGA600)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
A	VSS(NC)	VSS	P33_13	P33_12	P33_11	P33_10	P33_9	P33_8	P33_7	P33_6	P33_5	P33_4	P33_3	P33_2	P33_1	P33_0	AN111	AN110	AN101	AN100	AN051	AN050	AN033	AN032	AN021	AN020	AN003	AN001	ADSVSS	ADSVS S(NC)	A
B	E0VCC	VSS	P32_4	P31_12	P31_11	P31_10	P31_9	P31_8	P31_7	P31_6	P31_5	P31_4	P31_3	P31_2	P31_1	P31_0	AN112	AN113	AN102	AN053	AN052	AN041	AN043	AN031	AN022	AN010	AN011	AN002	AN000	ADSVSS	B
C	P31_14	E0VCC	VSS	P32_3	P32_2	P32_0	P34_4	P34_2	P34_0	P30_12	P30_11	P30_10	P30_9	P30_8	P30_7	AN121	AN120	AN103	A1VREFH	AN061	AN060	AN042	AN040	A0VREFH	AN013	AN012	ADSVCC	ADSVSS	ADSVCL	AN200	C
D	P31_15	P31_13	P32_5			P32_1	P34_3	P34_1	P30_6	P30_5	P30_4	P30_3	P30_2	P30_1	P30_0	AN123	AN122	A1VSS	A1VCC	AN063	AN062	AN030	AN023	A0VCC	A0VSS			ADSVREFH	AN202	AN201	D
E	P23_1	P23_0	P32_6																									ADSVREFL	AN203	AN221	E
F	P23_5	P23_4	P23_3	P23_2																							AN210	AN211	AN213	AN231	F
G	P23_7	P23_6	P24_1	P24_0																							AN220	AN233	AN230	AN223	G
H	VSS	VSS	VCC	P24_2																							AN212	AN222	AN240	AN232	H
J	ETH1_SG_TXD_N	ETH1_SG_TXD_P	VSS	GETH1VCL																							A2VCC	AN242	AN241	AN243	J
K	ETH1_SG_RXD_N	ETH1_SG_RXD_P	GETH0PVCC	GETH0BVCC																							A2VSS	A2VREFH	AN250	AN251	K
L	ETH0_SG_TXD_N	ETH0_SG_TXD_P	VSS	GETH0VCL																							AN252	AN260	AN253	AN261	L
M	ETH0_SG_RXD_N	ETH0_SG_RXD_P	VSS	ETH_SG_REFCLK																							AFCVCC	AN262	AN263	AN270	M
N	OSCVCC	VSS	P25_2	P25_10																							AFCVSS	AN271	AN272	AN273	N
P	X1	X2	P25_11	P25_7																							AN300	AN301	AN302	AN303	P
R	LVDVCC	VSS	P25_9	P25_8																							A3VCC	A3VREFH	AN310	AN311	R
T	P21_3	P21_2	P22_3	P22_0																							A3VSS	AN312	AN313	AN360	T
U	P21_5	P21_4	P22_1	P22_2																							AN361	AN362	AN363	AN370	U
V	P24_5	P24_4	P24_3	P22_4																							AN371	AN372	AN373	AN380	V
W	P24_7	P24_6	P22_5	P22_6																							AN381	AN382	AN383	AN390	W
Y	P25_3	P25_4	P22_8	P22_7																							P00_5	AN391	AN392	AN393	Y
AA	P25_5	P25_6	P22_10	P22_9																							P00_4	P00_11	P02_10	P02_11	AA
AB	P25_13	P25_12	P22_12	P22_11																							P00_3	P00_10	P02_8	P02_9	AB
AC	P25_15	P25_14	P22_13	RAMSVCL																							P00_2	P00_9	P02_6	P02_7	AC
AD	TRST	FLMD0	RESETOUT	SBMD																							P00_1	P00_8	P02_4	P02_5	AD
AE	ERRORGOUT_M	JP0_2	RESET	PWRCTL																							P00_0	P00_7	P02_2	P02_3	AE
AF	JP0_3	JP0_0	VMONOUT																									P00_6	P02_0	P02_1	AF
AG	JP0_1	JP0_5	E2VCC			P20_0	P20_7	P15_3	P15_7	P15_11	P14_6	P14_8	P14_10	P14_12	P12_1	P12_5	P13_8	P13_11	P11_0	P11_4	P11_9	P10_10	P10_12	P10_14	P01_9			P01_3	P01_4	P01_5	AG
AH	SYSVCC	J1VCC	SVRNGATE	SVRPGATE	P20_1	P20_4	P15_0	P15_4	P15_8	P15_12	P14_7	P14_9	P14_11	P12_0	P12_2	P12_6	P13_9	P13_12	P11_1	P11_5	P11_8	P11_10	P10_11	P10_13	P01_8	P01_11	E1VCC	VSS	P01_6	P01_7	AH
AJ	J0VCC	VSS	SVRDRVSS	SVRAVSS	P20_2	P20_5	P15_1	P15_5	P15_9	P14_0	P14_2	P13_0	P13_2	P14_5	P12_3	P12_7	P13_10	P13_13	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	P01_12	P01_13	E0VCC	VSS	VSS	AJ
AK	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	P20_3	P20_6	P15_2	P15_6	P15_10	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P12_9	P13_14	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_10	P01_14	P01_15	E0VCC	VSS(NC)	AK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	

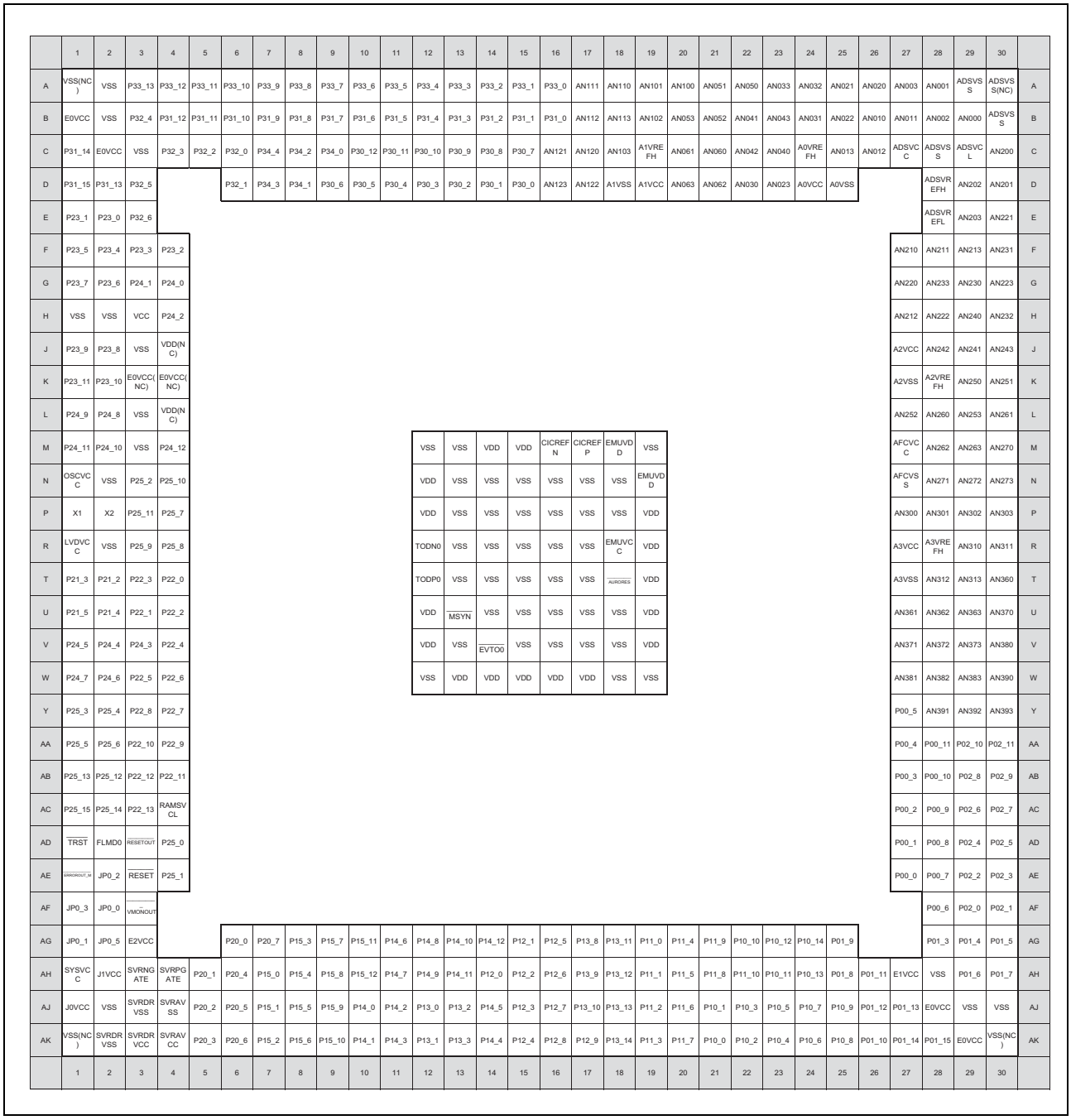
VSS	VSS	VDD	VDD	CICREFN	CICREFP	EMUVDD	VSS
VDD	VSS	VSS	VSS	VSS	VSS	VSS	EMUVDD
VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD
TODN0	VSS	VSS	VSS	VSS	VSS	EMUVCC	VDD
TODP0	VSS	VSS	VSS	VSS	VSS	AURORES	VDD
VDD	MSYN	VSS	VSS	VSS	VSS	VSS	VDD
VDD	VSS	EVTO0	VSS	VSS	VSS	VSS	VDD
VSS	AWOVCL	VDD	VDD	VDD	VDD	VSS	VSS

Figure 1.2 Pin Connection Diagram U2B24-FCC (FCBGA468)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS(NC)	VSS	P33_13	P33_12	P33_11	P33_9	P33_7	P33_5	P33_3	P33_1	P33_0	AN111	AN110	AN100	AN051	AN050	AN042	AN040	AN021	AN020	AN010	AN011	AN002	AN000	ADSVSS(NC)	A
B	E0VCC	VSS	P32_4	P32_2	P32_1	P33_10	P33_8	P33_6	P33_4	P33_2	AN121	AN120	AN102	AN101	AN053	AN052	AN033	AN032	AN031	AN013	AN003	AN001	ADSVCL	AN203	AN200	B
C	P23_0	E0VCC	VSS	P32_3	P32_0	P34_2	P34_0	P30_4	P30_2	P30_0	AN112	AN113	AN103	A1VREFH	AN061	AN060	AN041	AN043	AN022	A0VREFH	AN012	ADSVCC	ADSVSS	AN202	AN201	C
D	P23_6	P23_1	P32_5			P34_4	P34_3	P34_1	P30_3	P30_1	AN123	AN122	A1VSS	A1VCC	AN063	AN062	AN030	AN023	A0VCC	A0VSS			ADSVREFH	AN221	AN213	D
E	P23_7	P23_5	P32_6																				ADSVREFL	AN231	AN230	E
F	VSS	VSS	P23_3	P23_2																		AN210	AN220	AN223	AN233	F
G	ETH1_SG_TXD_N	ETH1_SG_TXD_P	VCC	P23_4																		A2VCC	A2VREFH	AN232	AN222	G
H	ETH1_SG_RXD_N	ETH1_SG_RXD_P	VSS	GETH1VCL																		A2VSS	AN211	AN240	AN250	H
J	ETH0_SG_TXD_N	ETH0_SG_TXD_P	GETH0PVCC	GETH0BVCC																		AN212	AN243	AN241	AN251	J
K	ETH0_SG_RXD_N	ETH0_SG_RXD_P	VSS	GETH0VCL																		AN242	AN252	AN260	AN253	K
L	OSCVCC	VSS	VSS	ETH_SG_REFCLK																		AFCVCC	AN262	AN270	AN261	L
M	X1	X2	P25_2	P22_0																		AFCVSS	AN263	AN271	AN272	M
N	LVDVCC	VSS	P22_3	P22_1																		AN311	AN310	AN300	AN273	N
P	P21_3	P21_2	P22_2	P22_4																		A3VCC	A3VREFH	AN302	AN301	P
R	P21_5	P21_4	P22_5	P22_6																		A3VSS	AN313	AN312	AN303	R
T	P25_3	P25_4	P22_7	P22_8																		P00_5	P00_11	P02_10	P02_11	T
U	P25_5	P25_6	P22_9	P22_10																		P00_4	P00_10	P02_8	P02_9	U
V	P22_11	P22_12	P22_13	RAMSVCL																		P00_3	P00_9	P02_6	P02_7	V
W	$\overline{TRST}$	FLMD0	$\overline{RESETOUT}$	SBMD																		P00_2	P00_8	P02_4	P02_5	W
Y	$\overline{ERROROUT\_M}$	JP0_2	$\overline{RESET}$	PWRCTL																		P00_1	P00_7	P02_2	P02_3	Y
AA	JP0_3	JP0_0	$\overline{VMONOUT}$																				P00_0	P02_0	P02_1	AA
AB	JP0_1	JP0_5	E2VCC			P20_0	P20_7	P14_6	P14_10	P14_11	P12_0	P12_2	P12_6	P13_8	P13_12	P11_5	P11_8	P11_10	P10_10	P10_13			P00_6	P01_4	P01_5	AB
AC	SYSVCC	J1VCC	SVRNGATE	SVRPGATE	P20_1	P20_4	P14_8	P14_7	P14_9	P14_12	P12_1	P12_3	P12_7	P13_9	P13_13	P11_0	P11_4	P11_9	P10_11	P10_12	P10_14	E1VCC	VSS	P01_6	P01_7	AC
AD	J0VCC	VSS	SVRDRVSS	SVRAVSS	P20_2	P20_5	P14_0	P14_2	P13_0	P13_2	P14_5	P12_4	P12_8	P13_10	P13_14	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	E0VCC	VSS	P01_3	AD
AE	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	P20_3	P20_6	P14_1	P14_3	P13_1	P13_3	P14_4	P12_5	P12_9	P13_11	P11_3	P11_1	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_8	E0VCC	VSS(NC)	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

VSS	VSS	VDD	CICREFN	CICREFP	EMUVDD	VSS
VDD	VSS	VSS	VSS	VSS	VSS	EMUVDD
TODN0	VSS	VSS	VSS	VSS	VSS	VDD
TODP0	VSS	VSS	VSS	VSS	EMUVCC	VDD
VDD	$\overline{MSYN}$	VSS	VSS	VSS	$\overline{AURORES}$	VDD
VDD	VSS	$\overline{EVTO0}$	VSS	VSS	VSS	VDD
VSS	AWOVCL	VDD	VDD	VDD	VSS	VSS

Figure 1.3 Pin Connection Diagram U2B24-FCC (FCBGA373)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
A	VSS(NC)	VSS	P33_13	P33_12	P33_11	P33_10	P33_9	P33_8	P33_7	P33_6	P33_5	P33_4	P33_3	P33_2	P33_1	P33_0	AN111	AN110	AN101	AN100	AN051	AN050	AN033	AN032	AN021	AN020	AN003	AN001	ADSVSS	ADSVSS(NC)	A
B	E0VCC	VSS	P32_4	P31_12	P31_11	P31_10	P31_9	P31_8	P31_7	P31_6	P31_5	P31_4	P31_3	P31_2	P31_1	P31_0	AN112	AN113	AN102	AN053	AN052	AN041	AN043	AN031	AN022	AN010	AN011	AN002	AN000	ADSVSS	B
C	P31_14	E0VCC	VSS	P32_3	P32_2	P32_0	P34_4	P34_2	P34_0	P30_12	P30_11	P30_10	P30_9	P30_8	P30_7	AN121	AN120	AN103	A1VREFH	AN061	AN060	AN042	AN040	A0VREFH	AN013	AN012	ADSVCC	ADSVSS	ADSVCL	AN200	C
D	P31_15	P31_13	P32_5			P32_1	P34_3	P34_1	P30_6	P30_5	P30_4	P30_3	P30_2	P30_1	P30_0	AN123	AN122	A1VSS	A1VCC	AN063	AN062	AN030	AN023	A0VCC	A0VSS			ADSVREFH	AN202	AN201	D
E	P23_1	P23_0	P32_6																									ADSVREFL	AN203	AN221	E
F	P23_5	P23_4	P23_3	P23_2																							AN210	AN211	AN213	AN231	F
G	P23_7	P23_6	P24_1	P24_0																							AN220	AN233	AN230	AN223	G
H	VSS	VSS	VCC	P24_2																							AN212	AN222	AN240	AN232	H
J	P23_9	P23_8	VSS	VDD(NC)																							A2VCC	AN242	AN241	AN243	J
K	P23_11	P23_10	E0VCC(NC)	E0VCC(NC)																							A2VSS	A2VREFH	AN250	AN251	K
L	P24_9	P24_8	VSS	VDD(NC)																							AN252	AN260	AN253	AN261	L
M	P24_11	P24_10	VSS	P24_12									VSS	VSS	VDD	VDD	CICREFN	CICREFP	EMUVDD	VSS							AFCVCC	AN262	AN263	AN270	M
N	OSCVCC	VSS	P25_2	P25_10									VDD	VSS	VSS	VSS	VSS	VSS	VSS	EMUVDD							AFCVSS	AN271	AN272	AN273	N
P	X1	X2	P25_11	P25_7									VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD							AN300	AN301	AN302	AN303	P
R	LVDVCC	VSS	P25_9	P25_8									TODN0	VSS	VSS	VSS	VSS	VSS	EMUVCC	VDD							A3VCC	A3VREFH	AN310	AN311	R
T	P21_3	P21_2	P22_3	P22_0									TODP0	VSS	VSS	VSS	VSS	VSS	AURORES	VDD							A3VSS	AN312	AN313	AN360	T
U	P21_5	P21_4	P22_1	P22_2									VDD	MSYN	VSS	VSS	VSS	VSS	VSS	VDD							AN361	AN362	AN363	AN370	U
V	P24_5	P24_4	P24_3	P22_4									VDD	VSS	EVTO0	VSS	VSS	VSS	VSS	VDD							AN371	AN372	AN373	AN380	V
W	P24_7	P24_6	P22_5	P22_6									VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS							AN381	AN382	AN383	AN390	W
Y	P25_3	P25_4	P22_8	P22_7																							P00_5	AN391	AN392	AN393	Y
AA	P25_5	P25_6	P22_10	P22_9																							P00_4	P00_11	P02_10	P02_11	AA
AB	P25_13	P25_12	P22_12	P22_11																							P00_3	P00_10	P02_8	P02_9	AB
AC	P25_15	P25_14	P22_13	RAMSVCL																							P00_2	P00_9	P02_6	P02_7	AC
AD	TRST	FLMD0	RESETOUT	P25_0																							P00_1	P00_8	P02_4	P02_5	AD
AE	ERROROUT_M	JP0_2	RESET	P25_1																							P00_0	P00_7	P02_2	P02_3	AE
AF	JP0_3	JP0_0	VMONOUT																									P00_6	P02_0	P02_1	AF
AG	JP0_1	JP0_5	E2VCC			P20_0	P20_7	P15_3	P15_7	P15_11	P14_6	P14_8	P14_10	P14_12	P12_1	P12_5	P13_8	P13_11	P11_0	P11_4	P11_9	P10_10	P10_12	P10_14	P01_9			P01_3	P01_4	P01_5	AG
AH	SYSVCC	J1VCC	SVRNGATE	SVRPGATE	P20_1	P20_4	P15_0	P15_4	P15_8	P15_12	P14_7	P14_9	P14_11	P12_0	P12_2	P12_6	P13_9	P13_12	P11_1	P11_5	P11_8	P11_10	P10_11	P10_13	P01_8	P01_11	E1VCC	VSS	P01_6	P01_7	AH
AJ	J0VCC	VSS	SVRDRVSS	SVRAVSS	P20_2	P20_5	P15_1	P15_5	P15_9	P14_0	P14_2	P13_0	P13_2	P14_5	P12_3	P12_7	P13_10	P13_13	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	P01_12	P01_13	E0VCC	VSS	VSS	AJ
AK	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	P20_3	P20_6	P15_2	P15_6	P15_10	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P12_9	P13_14	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_10	P01_14	P01_15	E0VCC	VSS(NC)	AK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	

Figure 1.4 Pin Connection Diagram U2B10-FCC (FCBGA468)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS(NC)	VSS	P33_13	P33_12	P33_11	P33_9	P33_7	P33_5	P33_3	P33_1	P33_0	AN111	AN110	AN100	AN051	AN050	AN042	AN040	AN021	AN020	AN010	AN011	AN002	AN000	ADSVSS(NC)	A
B	E0VCC	VSS	P32_4	P32_2	P32_1	P33_10	P33_8	P33_6	P33_4	P33_2	AN121	AN120	AN102	AN101	AN053	AN052	AN033	AN032	AN031	AN013	AN003	AN001	ADSVCL	AN203	AN200	B
C	P23_0	E0VCC	VSS	P32_3	P32_0	P34_2	P34_0	P30_4	P30_2	P30_0	AN112	AN113	AN103	A1VREFH	AN061	AN060	AN041	AN043	AN022	A0VREFH	AN012	ADSVCC	ADSVSS	AN202	AN201	C
D	P23_6	P23_1	P32_5			P34_4	P34_3	P34_1	P30_3	P30_1	AN123	AN122	A1VSS	A1VCC	AN063	AN062	AN030	AN023	A0VCC	A0VSS			ADSVREFH	AN221	AN213	D
E	P23_7	P23_5	P32_6																				ADSVREFL	AN231	AN230	E
F	VSS	VSS	P23_3	P23_2																		AN210	AN220	AN223	AN233	F
G	P23_9	P23_8	VCC	P23_4																		A2VCC	A2VREFH	AN232	AN222	G
H	P23_11	P23_10	VSS	VDD(NC)																		A2VSS	AN211	AN240	AN250	H
J	P24_9	P24_8	E0VCC(NC)	E0VCC(NC)																		AN212	AN243	AN241	AN251	J
K	P24_11	P24_10	VSS	VDD(NC)									VSS	VSS	VDD	CICREFN	CICREFP	EMUVDD	VSS			AN242	AN252	AN260	AN253	K
L	OSCVCC	VSS	VSS	P24_12									VDD	VSS	VSS	VSS	VSS	VSS	EMUVDD			AFCVCC	AN262	AN270	AN261	L
M	X1	X2	P25_2	P22_0									TODN0	VSS	VSS	VSS	VSS	VSS	VDD			AFCVSS	AN263	AN271	AN272	M
N	LVDVCC	VSS	P22_3	P22_1									TODP0	VSS	VSS	VSS	VSS	EMUVCC	VDD			AN311	AN310	AN300	AN273	N
P	P21_3	P21_2	P22_2	P22_4									VDD	$\overline{\text{MSYN}}$	VSS	VSS	VSS	$\overline{\text{AURORES}}$	VDD			A3VCC	A3VREFH	AN302	AN301	P
R	P21_5	P21_4	P22_5	P22_6									VDD	VSS	$\overline{\text{EVTO0}}$	VSS	VSS	VSS	VDD			A3VSS	AN313	AN312	AN303	R
T	P25_3	P25_4	P22_7	P22_8									VSS	VDD	VDD	VDD	VDD	VSS	VSS			P00_5	P00_11	P02_10	P02_11	T
U	P25_5	P25_6	P22_9	P22_10																		P00_4	P00_10	P02_8	P02_9	U
V	P22_11	P22_12	P22_13	RAMSVCL																		P00_3	P00_9	P02_6	P02_7	V
W	$\overline{\text{TRST}}$	FLMD0	$\overline{\text{RESETOUT}}$	P25_0																		P00_2	P00_8	P02_4	P02_5	W
Y	$\overline{\text{ERRROUT_M}}$	JP0_2	$\overline{\text{RESET}}$	P25_1																		P00_1	P00_7	P02_2	P02_3	Y
AA	JP0_3	JP0_0	$\overline{\text{VMONOUT}}$																				P00_0	P02_0	P02_1	AA
AB	JP0_1	JP0_5	E2VCC			P20_0	P20_7	P14_6	P14_10	P14_11	P12_0	P12_2	P12_6	P13_8	P13_12	P11_5	P11_8	P11_10	P10_10	P10_13			P00_6	P01_4	P01_5	AB
AC	SYSVCC	J1VCC	SVRNGATE	SVRPGATE	P20_1	P20_4	P14_8	P14_7	P14_9	P14_12	P12_1	P12_3	P12_7	P13_9	P13_13	P11_0	P11_4	P11_9	P10_11	P10_12	P10_14	E1VCC	VSS	P01_6	P01_7	AC
AD	J0VCC	VSS	SVRDRVSS	SVRAVSS	P20_2	P20_5	P14_0	P14_2	P13_0	P13_2	P14_5	P12_4	P12_8	P13_10	P13_14	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	E0VCC	VSS	P01_3	AD
AE	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	P20_3	P20_6	P14_1	P14_3	P13_1	P13_3	P14_4	P12_5	P12_9	P13_11	P11_3	P11_1	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_8	E0VCC	VSS(NC)	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Figure 1.5 Pin Connection Diagram U2B10-FCC (FCBGA373)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS(NC)	P32_2	P33_7	P33_5	P33_2	P33_1	P33_0	AN120	AN110	AN103	AN101	AN042	AN040	AN033	AN032	AN010	AN011	AN003	AN001	ADSVSS(NC)	A
B	P32_4	VSS	P32_3	P33_8	P33_6	P33_4	P33_3	AN112	AN121	AN111	AN102	AN100	AN030	AN023	AN021	AN020	AN002	AN000	ADSVSS	AN221	B
C	P23_1	P32_5																	ADSVCC	AN231	C
D	P23_5	P32_6		VSS(NC)	P32_1	P34_4	P34_2	P34_0	AN122	AN113	A1VREFH	AN043	A0VREFH	AN031	AN022	AN013	AN012		AN200	AN213	D
E	P23_6	P23_3		P23_0	VSS	P32_0	P34_3	P34_1	AN123	A1VSS	A1VCC	AN041	A0VCC	A0VSS	ADSVCL	ADSVREFL	AN202		AN201	AN230	E
F	P23_7	P23_4		P23_2	E0VCC											ADSVREFH	AN203		AN222	AN223	F
G	OSCVCC	P25_2		P22_1	P22_0				VDD	VDD	CICREFN	CICREFP	VSS	EMUVDD		AN210	AN211		AN233	AN232	G
H	X1	X2		P22_3	P22_2			VDD		VSS	VSS	VSS	VSS		EMUVDD	AN220	AN212		AN240	AN242	H
J	LVDVCC	VSS		P22_5	P22_4			VDD	VSS		VSS	VSS		VSS	VSS	A2VCC	A2VREFH		AN241	AN243	J
K	P21_3	P21_2		P22_7	P22_6			TODN0	VSS	VSS	VSS	VSS	VSS	VSS	EMUVCC	A2VSS	AN252		AFCVCC	AFCVSS	K
L	P21_5	P21_4		P22_9	P22_8			TODP0	VSS	VSS	VSS	VSS	VSS	VSS	AURORES	AN260	AN261		AN250	AN251	L
M	P25_3	P25_4		P22_11	P22_10			VDD	MSYN		VSS	VSS		VSS	VDD	AN262	AN263		AN270	AN253	M
N	P25_5	P25_6		P22_12	RAMSVCL			VDD		EVTO0	VSS	VSS	VSS		VDD	AN271	AN273		P02_9	P02_10	N
P	TRST	FLMD0		P22_13	RESETOUT				VDD	VDD	VSS	VSS	VDD	VDD		AN272	P00_5		P02_7	P02_8	P
R	ERROROUT_M	JP0_2		RESET	P20_0											E0VCC	P00_4		P02_5	P02_6	R
T	JP0_3	JP0_0		VMONOUT	P20_1	P20_3	E2VCC	P12_0	P12_2	P12_5	P11_0	P11_8	P11_9	E1VCC	P00_2	VSS	P00_3		P02_3	P02_4	T
U	JP0_1	JP0_5		SYSVCC	P20_4	P20_6	P20_7	P12_1	P12_6	P12_3	P11_1	P11_5	P11_4	P11_10	P00_1	P00_0	VSS(NC)		P02_1	P02_2	U
V	VCC	SVRDRVCC																	P00_6	P02_0	V
W	J0VCC	SVRDRVSS	SVRAVSS	SVRNGATE	P20_2	P14_0	P14_2	P13_0	P13_2	P14_5	P12_7	P12_9	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	VSS	P00_7	W
Y	VSS(NC)	SVRDRVSS	SVRAVCC	SVRPGATE	P20_5	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	VSS(NC)	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.6 Pin Connection Diagram U2B10-FCC (FCBGA292)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS(NC)	P32_2	P33_7	P33_5	P33_2	P33_1	P33_0	AN120	AN110	AN103	AN101	AN042	AN040	AN033	AN032	AN010	AN011	AN003	AN001	ADSVSS(NC)	A
B	P32_4	VSS	P32_3	P33_8	P33_6	P33_4	P33_3	AN112	AN121	AN111	AN102	AN100	AN030	AN023	AN021	AN020	AN002	AN000	ADSVSS	AN221	B
C	P23_1	P32_5																	ADSVCC	AN231	C
D	P23_5	P32_6		VSS(NC)	P32_1	P34_4	P34_2	P34_0	AN122	AN113	A1VREFH	AN043	A0VREFH	AN031	AN022	AN013	AN012		AN200	AN213	D
E	P23_6	P23_3		P23_0	VSS	P32_0	P34_3	P34_1	AN123	A1VSS	A1VCC	AN041	A0VCC	A0VSS	ADSVCL	ADSVREFL	AN202		AN201	AN230	E
F	P23_7	P23_4		P23_2	E0VCC											ADSVREFH	AN203		AN222	AN223	F
G	OSCVCC	P25_2		P22_1	P22_0				VDD	VDD	CICREFN	CICREFP	VSS	EMUVDD		AN210	AN211		AN233	AN232	G
H	X1	X2		P22_3	P22_2				VDD		VSS	VSS	VSS	VSS		EMUVDD	AN220	AN212	AN240	AN242	H
J	LVDVCC	VSS		P22_5	P22_4				VDD	VSS		VSS	VSS		VSS	VSS	A2VCC	A2VREFH	AN241	AN243	J
K	P21_3	P21_2		P22_7	P22_6				TODN0	VSS	VSS	VSS	VSS	VSS	VSS	EMUVCC	A2VSS	AN252	AFCVCC	AFCVSS	K
L	P21_5	P21_4		P22_9	P22_8				TODP0	VSS	VSS	VSS	VSS	VSS	VSS	AURORES	AN260	AN261	AN250	AN251	L
M	P25_3	P25_4		P22_11	P22_10				VDD	MSYN		VSS	VSS		VSS	VDD	AN262	AN263	AN270	AN253	M
N	P25_5	P25_6		P22_12	RAMSVCL				VDD		EVTO0	VSS	VSS	VSS		VDD	AN271	AN273	P02_9	P02_10	N
P	TRST	FLMD0		P22_13	RESETOUT					VDD	VDD	VSS	VSS	VDD	VDD		AN272	P00_5	P02_7	P02_8	P
R	ERROROUT_M	JP0_2		RESET	P20_0											E0VCC	P00_4		P02_5	P02_6	R
T	JP0_3	JP0_0		VMONOUT	P20_1	P20_3	E2VCC	P12_0	P12_2	P12_5	P11_0	P11_8	P11_9	E1VCC	P00_2	VSS	P00_3		P02_3	P02_4	T
U	JP0_1	JP0_5		SYSVCC	P20_4	P20_6	P20_7	P12_1	P12_6	P12_3	P11_1	P11_5	P11_4	P11_10	P00_1	P00_0	VSS(NC)		P02_1	P02_2	U
V	VCC	SVRDRVCC																	P00_6	P02_0	V
W	J0VCC	SVRDRVSS	SVRAVSS	SVRNGATE	P20_2	P14_0	P14_2	P13_0	P13_2	P14_5	P12_7	P12_9	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	VSS	P00_7	W
Y	VSS(NC)	SVRDRVSS	SVRAVCC	SVRPGATE	P20_5	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	VSS(NC)	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.7 Pin Connection Diagram U2B6-FCC (FCBGA292)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
A	VSS(NC)	VSS	P33_13	P33_12	P33_11	P33_10	P33_9	P33_8	P33_7	P33_6	P33_5	P33_4	P33_3	P33_2	P33_1	P33_0	AN111	AN110	AN101	AN100	AN051	AN050	AN033	AN032	AN021	AN020	AN003	AN001	ADSVSS	ADSVSS(NC)	A
B	E0VCC	VSS	P32_4	P31_12	P31_11	P31_10	P31_9	P31_8	P31_7	P31_6	P31_5	P31_4	P31_3	P31_2	P31_1	P31_0	AN112	AN113	AN102	AN053	AN052	AN041	AN043	AN031	AN022	AN010	AN011	AN002	AN000	ADSVSS	B
C	P31_14	E0VCC	VSS	P32_3	P32_2	P32_0	P34_4	P34_2	P34_0	P30_12	P30_11	P30_10	P30_9	P30_8	P30_7	AN121	AN120	AN103	A1VREFH	AN061	AN060	AN042	AN040	A0VREFH	AN013	AN012	ADSVCC	ADSVSS	ADSVCL	AN200	C
D	P31_15	P31_13	P32_5			P32_1	P34_3	P34_1	P30_6	P30_5	P30_4	P30_3	P30_2	P30_1	P30_0	AN123	AN122	A1VSS	A1VCC	AN063	AN062	AN030	AN023	A0VCC	A0VSS			ADSVREFH	AN202	AN201	D
E	P23_1	P23_0	P32_6																									ADSVREFL	AN203	AN221	E
F	P23_5	P23_4	P23_3	P23_2																							AN210	AN211	AN213	AN231	F
G	P23_7	P23_6	P24_1	P24_0																							AN220	AN233	AN230	AN223	G
H	VSS	VSS	VCC	P24_2																							AN212	AN222	AN240	AN232	H
J	P23_9	P23_8	VSS	VDD(NC)																							A2VCC	AN242	AN241	AN243	J
K	P23_11	P23_10	E0VCC(NC)	E0VCC(NC)																							A2VSS	A2VREFH	AN250	AN251	K
L	P24_9	P24_8	VSS	VDD(NC)																							AN252	AN260	AN253	AN261	L
M	P24_11	P24_10	VSS	P24_12									VSS	VSS	VDD	VDD	VDD(NC)	VDD(NC)	VDD(NC)	VSS							AFCVCC	AN262	AN263	AN270	M
N	OSCVCC	VSS	P25_2	P25_10									VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD(NC)							AFCVSS	AN271	AN272	AN273	N
P	X1	X2	P25_11	P25_7									VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD							AN300	AN301	AN302	AN303	P
R	LVDVCC	VSS	P25_9	P25_8									VDD(NC)	VSS	VSS	VSS	VSS	VSS	VSS(NC)	VDD							A3VCC	A3VREFH	AN310	AN311	R
T	P21_3	P21_2	P22_3	P22_0									VDD(NC)	VSS	VSS	VSS	VSS	VSS	VSS(NC)	VDD							A3VSS	AN312	AN313	AN360	T
U	P21_5	P21_4	P22_1	P22_2									VDD	VSS(NC)	VSS	VSS	VSS	VSS	VSS	VDD							AN361	AN362	AN363	AN370	U
V	P24_5	P24_4	P24_3	P22_4									VDD	VSS	VSS(NC)	VSS	VSS	VSS	VSS	VDD							AN371	AN372	AN373	AN380	V
W	P24_7	P24_6	P22_5	P22_6									VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS							AN381	AN382	AN383	AN390	W
Y	P25_3	P25_4	P22_8	P22_7																							P00_5	AN391	AN392	AN393	Y
AA	P25_5	P25_6	P22_10	P22_9																							P00_4	P00_11	P02_10	P02_11	AA
AB	P25_13	P25_12	P22_12	P22_11																							P00_3	P00_10	P02_8	P02_9	AB
AC	P25_15	P25_14	P22_13	RAMSVCL																							P00_2	P00_9	P02_6	P02_7	AC
AD	$\overline{TRST}$	FLMD0	RESETOUT	P25_0																							P00_1	P00_8	P02_4	P02_5	AD
AE	ERROROUT_M	JP0_2	$\overline{RESET}$	P25_1																							P00_0	P00_7	P02_2	P02_3	AE
AF	JP0_3	JP0_0	VMONOUT																									P00_6	P02_0	P02_1	AF
AG	JP0_1	JP0_5	E2VCC			P20_0	P20_7	P15_3	P15_7	P15_11	P14_6	P14_8	P14_10	P14_12	P12_1	P12_5	P13_8	P13_11	P11_0	P11_4	P11_9	P10_10	P10_12	P10_14	P01_9			P01_3	P01_4	P01_5	AG
AH	SYSVCC	VCC	SVRNGATE	SVRPGATE	P20_1	P20_4	P15_0	P15_4	P15_8	P15_12	P14_7	P14_9	P14_11	P12_0	P12_2	P12_6	P13_9	P13_12	P11_1	P11_5	P11_8	P11_10	P10_11	P10_13	P01_8	P01_11	E1VCC	VSS	P01_6	P01_7	AH
AJ	VCC	VSS	SVRDRVSS	SVRAVSS	P20_2	P20_5	P15_1	P15_5	P15_9	P14_0	P14_2	P13_0	P13_2	P14_5	P12_3	P12_7	P13_10	P13_13	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	P01_12	P01_13	E0VCC	VSS	VSS	AJ
AK	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	P20_3	P20_6	P15_2	P15_6	P15_10	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P12_9	P13_14	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_10	P01_14	P01_15	E0VCC	VSS(NC)	AK
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	

Figure 1.8 Pin Connection Diagram U2B10 (BGA468)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS(NC)	VSS	P33_13	P33_12	P33_11	P33_9	P33_7	P33_5	P33_3	P33_1	P33_0	AN111	AN110	AN100	AN051	AN050	AN042	AN040	AN021	AN020	AN010	AN011	AN002	AN000	ADSVSS(NC)	A
B	E0VCC	VSS	P32_4	P32_2	P32_1	P33_10	P33_8	P33_6	P33_4	P33_2	AN121	AN120	AN102	AN101	AN053	AN052	AN033	AN032	AN031	AN013	AN003	AN001	ADSVCL	AN203	AN200	B
C	P23_0	E0VCC	VSS	P32_3	P32_0	P34_2	P34_0	P30_4	P30_2	P30_0	AN112	AN113	AN103	A1VREFH	AN061	AN060	AN041	AN043	AN022	A0VREFH	AN012	ADSVCC	ADSVSS	AN202	AN201	C
D	P23_6	P23_1	P32_5			P34_4	P34_3	P34_1	P30_3	P30_1	AN123	AN122	A1VSS	A1VCC	AN063	AN062	AN030	AN023	A0VCC	A0VSS			ADSVREFH	AN221	AN213	D
E	P23_7	P23_5	P32_6																				ADSVREFL	AN231	AN230	E
F	VSS	VSS	P23_3	P23_2																		AN210	AN220	AN223	AN233	F
G	P23_9	P23_8	VCC	P23_4																		A2VCC	A2VREFH	AN232	AN222	G
H	P23_11	P23_10	VSS	VDD(NC)																		A2VSS	AN211	AN240	AN250	H
J	P24_9	P24_8	E0VCC(NC)	E0VCC(NC)																		AN212	AN243	AN241	AN251	J
K	P24_11	P24_10	VSS	VDD(NC)						VSS	VSS	VDD	VDD(NC)	VDD(NC)	VDD(NC)	VSS						AN242	AN252	AN260	AN253	K
L	OSCVCC	VSS	VSS	P24_12						VDD	VSS	VSS	VSS	VSS	VSS	VDD(NC)						AFCVCC	AN262	AN270	AN261	L
M	X1	X2	P25_2	P22_0						VDD(NC)	VSS	VSS	VSS	VSS	VSS	VDD						AFCVSS	AN263	AN271	AN272	M
N	LVDVCC	VSS	P22_3	P22_1						VDD(NC)	VSS	VSS	VSS	VSS	VSS(NC)	VDD						AN311	AN310	AN300	AN273	N
P	P21_3	P21_2	P22_2	P22_4						VDD	VSS(NC)	VSS	VSS	VSS	VSS(NC)	VDD						A3VCC	A3VREFH	AN302	AN301	P
R	P21_5	P21_4	P22_5	P22_6						VDD	VSS	VSS(NC)	VSS	VSS	VSS	VDD						A3VSS	AN313	AN312	AN303	R
T	P25_3	P25_4	P22_7	P22_8						VSS	VDD	VDD	VDD	VDD	VSS	VSS						P00_5	P00_11	P02_10	P02_11	T
U	P25_5	P25_6	P22_9	P22_10																		P00_4	P00_10	P02_8	P02_9	U
V	P22_11	P22_12	P22_13	RAMSVCL																		P00_3	P00_9	P02_6	P02_7	V
W	$\overline{\text{TRST}}$	FLMD0	$\overline{\text{RESETOUT}}$	P25_0																		P00_2	P00_8	P02_4	P02_5	W
Y	$\overline{\text{ERROROUT_M}}$	JP0_2	$\overline{\text{RESET}}$	P25_1																		P00_1	P00_7	P02_2	P02_3	Y
AA	JP0_3	JP0_0	$\overline{\text{VMONOUT}}$																				P00_0	P02_0	P02_1	AA
AB	JP0_1	JP0_5	E2VCC			P20_0	P20_7	P14_6	P14_10	P14_11	P12_0	P12_2	P12_6	P13_8	P13_12	P11_5	P11_8	P11_10	P10_10	P10_13			P00_6	P01_4	P01_5	AB
AC	SYSVCC	VCC	SVRNGATE	SVRPGATE	P20_1	P20_4	P14_8	P14_7	P14_9	P14_12	P12_1	P12_3	P12_7	P13_9	P13_13	P11_0	P11_4	P11_9	P11_11	P10_12	P10_14	E1VCC	VSS	P01_6	P01_7	AC
AD	VCC	VSS	SVRDRVSS	SVRAVSS	P20_2	P20_5	P14_0	P14_2	P13_0	P13_2	P14_5	P12_4	P12_8	P13_10	P13_14	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	P10_9	E0VCC	VSS	P01_3	AD
AE	VSS(NC)	SVRDRVSS	SVRDRVCC	SVRAVCC	P20_3	P20_6	P14_1	P14_3	P13_1	P13_3	P14_4	P12_5	P12_9	P13_11	P11_3	P11_1	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	P01_8	E0VCC	VSS(NC)	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Figure 1.9 Pin Connection Diagram U2B10 (BGA373)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS(NC)	P32_2	P33_7	P33_5	P33_2	P33_1	P33_0	AN120	AN110	AN103	AN101	AN042	AN040	AN033	AN032	AN010	AN011	AN003	AN001	ADSVSS(NC)	A
B	P32_4	VSS	P32_3	P33_8	P33_6	P33_4	P33_3	AN112	AN121	AN111	AN102	AN100	AN030	AN023	AN021	AN020	AN002	AN000	ADSVSS	AN221	B
C	P23_1	P32_5																	ADSVCC	AN231	C
D	P23_5	P32_6		VSS(NC)	P32_1	P34_4	P34_2	P34_0	AN122	AN113	A1VREFH	AN043	A0VREFH	AN031	AN022	AN013	AN012		AN200	AN213	D
E	P23_6	P23_3		P23_0	VSS	P32_0	P34_3	P34_1	AN123	A1VSS	A1VCC	AN041	A0VCC	A0VSS	ADSVCL	ADSVREFL	AN202		AN201	AN230	E
F	P23_7	P23_4		P23_2	E0VCC											ADSVREFH	AN203		AN222	AN223	F
G	OSCVCC	P25_2		P22_1	P22_0			VDD	VDD	VSS(NC)	VSS(NC)	VSS	VDD(NC)			AN210	AN211		AN233	AN232	G
H	X1	X2		P22_3	P22_2		VDD		VSS	VSS	VSS	VSS		VDD(NC)		AN220	AN212		AN240	AN242	H
J	LVDVCC	VSS		P22_5	P22_4		VDD	VSS		VSS	VSS		VSS	VSS		A2VCC	A2VREFH		AN241	AN243	J
K	P21_3	P21_2		P22_7	P22_6		VSS(NC)	VSS	VSS	VSS	VSS	VSS	VSS	VSS(NC)		A2VSS	AN252		AFCVCC	AFCVSS	K
L	P21_5	P21_4		P22_9	P22_8		VSS(NC)	VSS	VSS	VSS	VSS	VSS	VSS	VSS(NC)		AN260	AN261		AN250	AN251	L
M	P25_3	P25_4		P22_11	P22_10		VDD	VSS(NC)		VSS	VSS		VSS	VDD		AN262	AN263		AN270	AN253	M
N	P25_5	P25_6		P22_12	RAMSVCL		VDD		VSS(NC)	VSS	VSS	VSS		VDD		AN271	AN273		P02_9	P02_10	N
P	$\overline{\text{TRST}}$	FLMD0		P22_13	$\overline{\text{RESETOUT}}$			VDD	VDD	VSS	VSS	VDD	VDD			AN272	P00_5		P02_7	P02_8	P
R	$\overline{\text{ERROROUT_M}}$	JP0_2		$\overline{\text{RESET}}$	P20_0											E0VCC	P00_4		P02_5	P02_6	R
T	JP0_3	JP0_0		$\overline{\text{VMONOUT}}$	P20_1	P20_3	E2VCC	P12_0	P12_2	P12_5	P11_0	P11_8	P11_9	E1VCC	P00_2	VSS	P00_3		P02_3	P02_4	T
U	JP0_1	JP0_5		SYSVCC	P20_4	P20_6	P20_7	P12_1	P12_6	P12_3	P11_1	P11_5	P11_4	P11_10	P00_1	P00_0	VSS(NC)		P02_1	P02_2	U
V	VCC	SVRDRVCC																	P00_6	P02_0	V
W	VCC	SVRDRVSS	SVRAVSS	SVRNGATE	P20_2	P14_0	P14_2	P13_0	P13_2	P14_5	P12_7	P12_9	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	VSS	P00_7	W
Y	VSS(NC)	SVRDRVSS	SVRAVCC	SVRPGATE	P20_5	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	VSS(NC)	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.10 Pin Connection Diagram U2B10 (BGA292)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS(NC)	P32_2	P33_7	P33_5	P33_2	P33_1	P33_0	AN120	AN110	AN103	AN101	AN042	AN040	AN033	AN032	AN010	AN011	AN003	AN001	ADSVSS(NC)	A
B	P32_4	VSS	P32_3	P33_8	P33_6	P33_4	P33_3	AN112	AN121	AN111	AN102	AN100	AN030	AN023	AN021	AN020	AN002	AN000	ADSVSS	AN221	B
C	P23_1	P32_5																	ADSVCC	AN231	C
D	P23_5	P32_6	VSS(NC)	P32_1	P34_4	P34_2	P34_0	AN122	AN113	A1VREFH	AN043	A0VREFH	AN031	AN022	AN013	AN012			AN200	AN213	D
E	P23_6	P23_3	P23_0	VSS	P32_0	P34_3	P34_1	AN123	A1VSS	A1VCC	AN041	A0VCC	A0VSS	ADSVCL	ADSVREFL	AN202			AN201	AN230	E
F	P23_7	P23_4	P23_2	E0VCC											ADSVREFH	AN203			AN222	AN223	F
G	OSCVCC	P25_2	P22_1	P22_0				VDD	VDD	VSS(NC)	VSS(NC)	VSS	VDD(NC)		AN210	AN211			AN233	AN232	G
H	X1	X2	P22_3	P22_2				VDD		VSS	VSS	VSS	VSS		VDD(NC)	AN220	AN212		AN240	AN242	H
J	LVDVCC	VSS	P22_5	P22_4				VDD	VSS		VSS	VSS		VSS	VSS	A2VCC	A2VREFH		AN241	AN243	J
K	P21_3	P21_2	P22_7	P22_6				VSS(NC)	VSS	VSS	VSS	VSS	VSS	VSS	VSS(NC)	A2VSS	AN252		AFCVCC	AFCVSS	K
L	P21_5	P21_4	P22_9	P22_8				VSS(NC)	VSS	VSS	VSS	VSS	VSS	VSS	VSS(NC)	AN260	AN261		AN250	AN251	L
M	P25_3	P25_4	P22_11	P22_10				VDD	VSS(NC)		VSS	VSS		VSS	VDD	AN262	AN263		AN270	AN253	M
N	P25_5	P25_6	P22_12	RAMSVCL				VDD		VSS(NC)	VSS	VSS	VSS		VDD	AN271	AN273		P02_9	P02_10	N
P	$\overline{\text{TRST}}$	FLMD0	P22_13	$\overline{\text{RESETOUT}}$					VDD	VDD	VSS	VSS	VDD	VDD		AN272	P00_5		P02_7	P02_8	P
R	$\overline{\text{ERROROUT_M}}$	JP0_2	$\overline{\text{RESET}}$	P20_0												E0VCC	P00_4		P02_5	P02_6	R
T	JP0_3	JP0_0	$\overline{\text{VMONOUT}}$	P20_1	P20_3	E2VCC	P12_0	P12_2	P12_5	P11_0	P11_8	P11_9	E1VCC	P00_2	VSS	P00_3			P02_3	P02_4	T
U	JP0_1	JP0_5	SYSVCC	P20_4	P20_6	P20_7	P12_1	P12_6	P12_3	P11_1	P11_5	P11_4	P11_10	P00_1	P00_0	VSS(NC)			P02_1	P02_2	U
V	VCC	SVRDRVCC																	P00_6	P02_0	V
W	VCC	SVRDRVSS	SVRAVSS	SVRNGATE	P20_2	P14_0	P14_2	P13_0	P13_2	P14_5	P12_7	P12_9	P11_2	P11_6	P10_1	P10_3	P10_5	P10_7	VSS	P00_7	W
Y	VSS(NC)	SVRDRVSS	SVRAVCC	SVRPGATE	P20_5	P14_1	P14_3	P13_1	P13_3	P14_4	P12_4	P12_8	P11_3	P11_7	P10_0	P10_2	P10_4	P10_6	P10_8	VSS(NC)	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.11 Pin Connection Diagram U2B6 (BGA292)

1.6 Functional Block Configuration

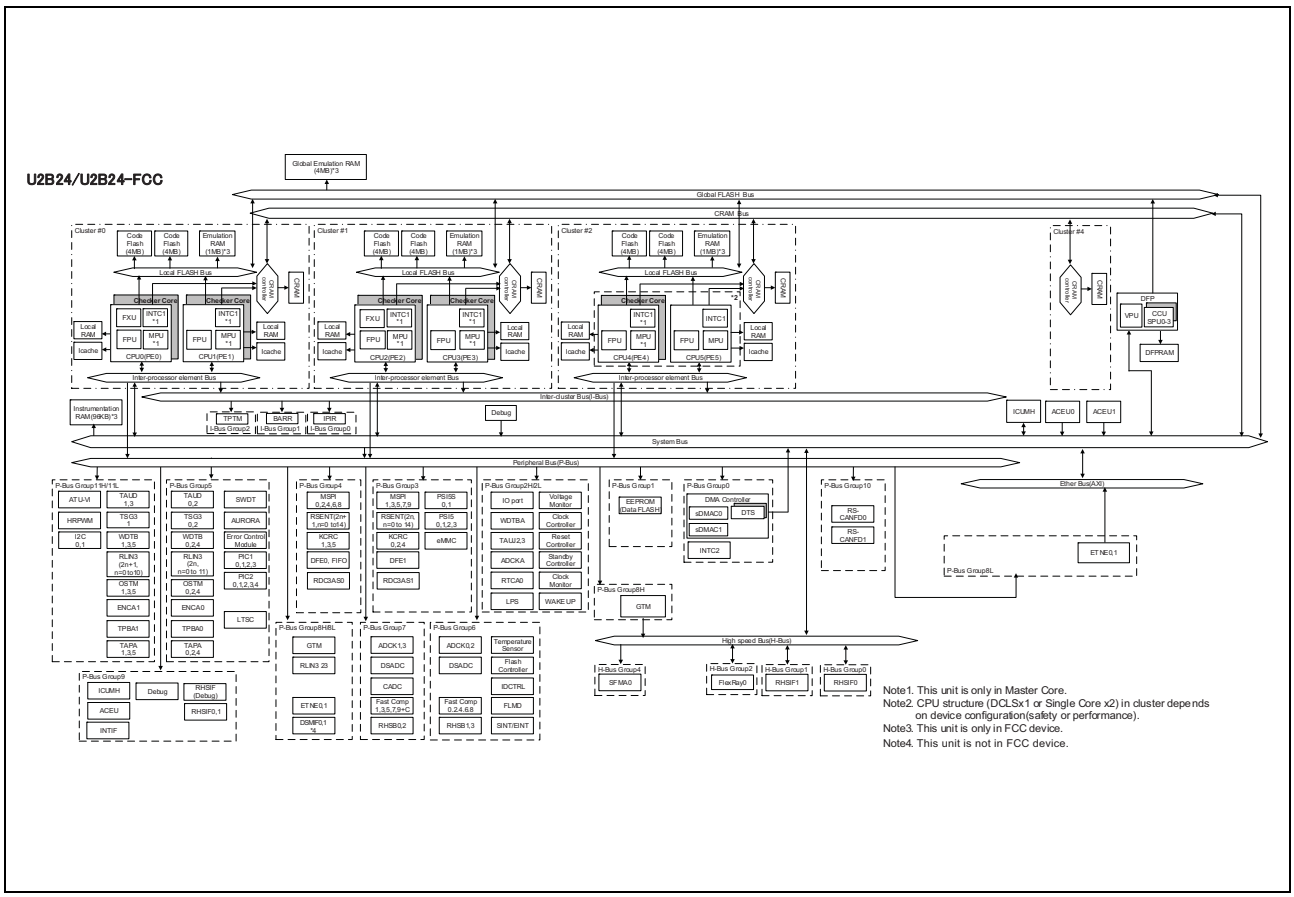


Figure 1.12 Internal Block Diagram (U2B24-FCC)

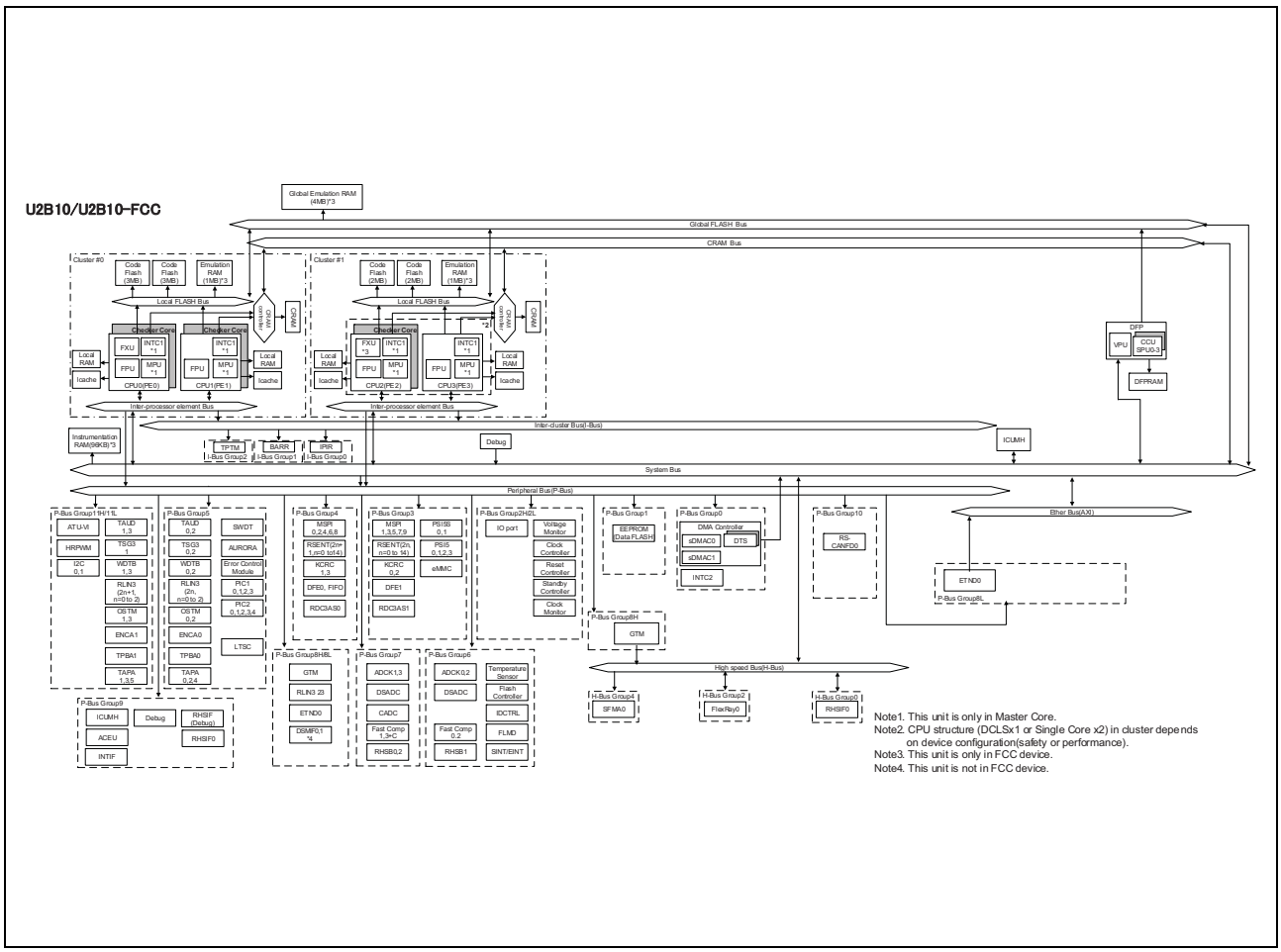


Figure 1.13 Internal Block Diagram (U2B10 and U2B10-FCC)

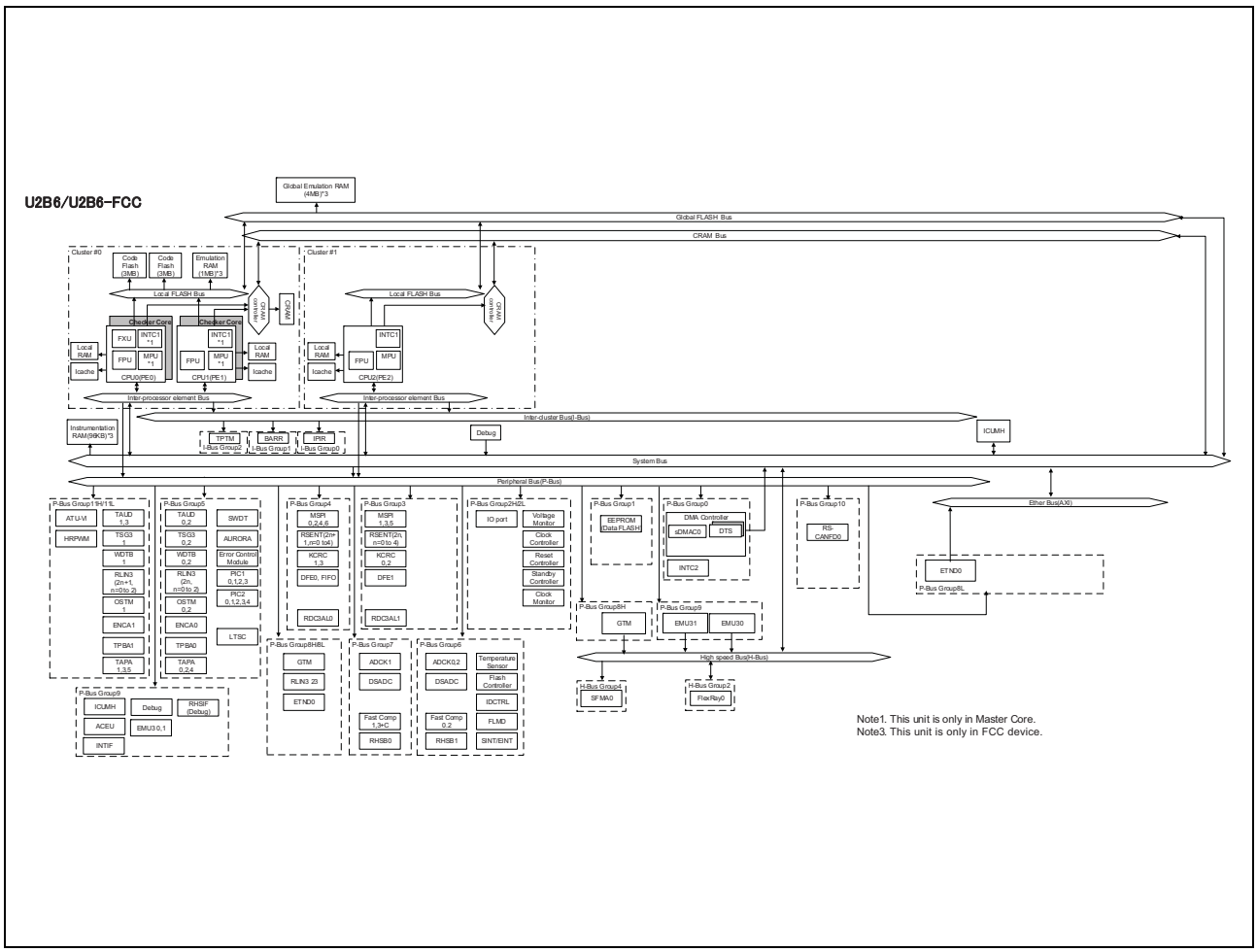


Figure 1.14 Internal Block Diagram (U2B6 and U2B-FCC for U2B6)

Section 2 Pin Functions

2.1 Pin List

2.1.1 Pin List and Function assignment

For detail information, refer to Appendix “E02_01_List_of_Pin_Assignment.xlsx”.

2.1.2 Pin Function name

For detail information, refer to Appendix “E02_03_List_of_Pin_Function.xlsx".

Section 3 Electrical Characteristics

The specifications in this section are for devices operating under the conditions shown in **Section 3.2.1, Operational Conditions**. Where a special condition is required for a given specification, the condition will be indicated. Furthermore, the specifications in this section are not guaranteed unless the conditions listed below are met.

3.1 Absolute Maximum Ratings

Conditions:

- VSS = SVRDRVSS = SVRAVSS = AnVSS = ADSVSS = AFCVSS
- Reference ground potential: VSS = 0 V.

Table 3.1 Absolute Maximum Ratings (1/3)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Voltage	$V_{AMRSYSVCC}$	SYSVCC	–0.5		6.5 *8	V
	V_{AMRVCC}	VCC	–0.5		6.5 *8	V
	V_{AMRVDD}	VDD	–0.5		1.42 *9	V
	$V_{AMRE0VCC}$	E0VCC	–0.5		6.5 *8	V
	$V_{AMRE1VCC}$	E1VCC	–0.5		6.5 *8	V
	$V_{AMRE2VCC}$	E2VCC	–0.5		6.5 *8	V
	$V_{AMRLVDVCC}$	LVDVCC	–0.5		6.5 *8	V
	$V_{AMRA0VCC}$	A0VCC	–0.5		6.5 *8	V
	$V_{AMRA1VCC}$	A1VCC	–0.5		6.5 *8	V
	$V_{AMRA2VCC}$	A2VCC	–0.5		6.5 *8	V
	$V_{AMRA3VCC}$	A3VCC	–0.5		6.5 *8	V
	$V_{AMRSVRDRVCC}$	SVRDRVCC	–0.5		6.5*8	V
	$V_{AMRSVRAVCC}$	SVRAVCC	–0.5		6.5 *8	V
	$V_{AMREMUVCC}$	EMUVCC*8	–0.5		4.6 *10	V
	$V_{AMREMUVDD}$	EMUVDD*8	–0.5		1.42 *9	V
	$V_{AMRGETH0BVCC}$	GETH0BVCC	–0.5		4.6 *10	V
	$V_{AMRGETH0PVCC}$	GETH0PVCC	–0.5		6.5 *8	V
	$V_{AMRADSVCC}$	ADSVCC	–0.5		6.5 *8	V
	$V_{AMRAFCVCC}$	AFCVCC	–0.5		6.5 *8	V
	$V_{AMROSCVCC}$	OSCVCC	–0.5		6.5 *8	V
	$V_{AMRJ0VCC}$	J0VCC	–0.5		6.5 *8	V
	$V_{AMRJ1VCC}$	J1VCC	–0.5		6.5 *8	V

Table 3.1 Absolute Maximum Ratings (2/3)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage	V_{AMRI}	E0VCC pin[*1]	–0.5		E0VCC + 0.5[*12]	V
		E1VCC pin[*2]	–0.5		E1VCC + 0.5[*12]	V
		E2VCC pin[*3]	–0.5		E2VCC + 0.5[*12]	V
		JP1, JP0_0, JP0_1, JP0_2, JP0_3, JP0_5, EVTI, MSYN	–0.5		VCC + 0.5[*12]	V
		X1	–0.5		OSCVCC + 0.5[*12]	V
		CICREFN, CICREFP	–0.5		EMUVCC + 0.5[*12]	V
		RHSIF, RHSB[*4]	–0.5		LVDVCC + 0.5[*12]	V
		SGMII I/F[*5]	–0.5		GETH0BVCC + 0.5[*12]	V
		ETH_SG_REFCLK	–0.5		GETH0PVCC + 0.5[*12]	V
		5 V tolerant pin[*13]	–0.5		6.0	V
Analog reference voltage	$V_{AMRAVREF}$	A0VREFH	–0.5		A0VCC + 0.5	V
		A1VREFH	–0.5		A1VCC + 0.5	V
		A2VREFH	–0.5		A2VCC + 0.5	V
		A3VREFH	–0.5		A3VCC + 0.5	V
		ADSVREFH	–0.5		ADSVCC + 0.5	V
Analog input voltage	V_{AMRIAN}	A0VCC pins	–0.5		A0VCC + 0.5	V
		A1VCC pins	–0.5		A1VCC + 0.5	V
		A2VCC pins	–0.5		A2VCC + 0.5	V
		A3VCC pins	–0.5		A3VCC + 0.5	V
		ADSVCC pins	–0.5		ADSVCC + 0.5	V
		AFCVCC pins	–0.5		AFCVCC + 0.5	V
VSS differential voltage	$V_{VSSDIFF}$		–0.1		0.1	V
Injection current per digital input	I_{INJ_DIN}	[*11]	-25		25	mA
Injection current per analog input	I_{INJ_AIN}	[*11]	-25		25	mA
Total Injection current of the device	$\lvert I_{INJ\_TOT} \rvert$	[*11]			120	mA
Output low current[*6]	I_{OL1p}	per pin			10	mA
	I_{OLall}	Sum of all output low currents of all EnVCC/ AnVCC pins			200	mA

Table 3.1 Absolute Maximum Ratings (3/3)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output high current[*6]	I_{OH1p}	per pin			–10	mA
	I_{OHall}	Sum of all output high currents of all EnVCC/ AnVCC pins			–200	mA
Junction temperature	T_j	U2B-FCC(U2B24 mode)	–40		150	°C
		other than above products	–40		160	°C
Storage temperature[*7]	T_{stg}	U2B-FCC(U2B24 mode)	–55		150	°C
		other than above products	–55		160	°C

Note 1. P00, P01, P02, P21, P22, P23, P24, P25, P30, P31, P32, P33, P34, RESETOUT

Note 2. P10, P11

Note 3. P12, P13, P14, P15, P20

Note 4. RHSIF0: HSIF0_TXDP, HSIF0_TXDN, HSIF0_RXDP, HSIF0_RXDN
RHSIF1: HSIF1_TXDP, HSIF1_TXDN, HSIF1_RXDP, HSIF1_RXDN
RHSB0: RHSB0FCLP, RHSB0FCLN, RHSB0NMFCLP, RHSB0NMFCLN, RHSB0MCSIP, RHSB0MCSIN, RHSB0MCSOP, RHSB0MCSON, RHSB0SOP, RHSB0SON, RHSB0NMSOP, RHSB0NMSON
RHSB3: RHSB3FCLP, RHSB3FCLN, RHSB3NMFCLP, RHSB3NMFCLN, RHSB3MCSIP, RHSB3MCSIN, RHSB3MCSOP, RHSB3MCSON, RHSB3SOP, RHSB3SON, RHSB3NMSOP, RHSB3NMSON

Note 5. ETH0_SG_TXD_N, ETH0_SG_TXD_P, ETH0_SG_RXD_N, ETH0_SG_RXD_P, ETH1_SG_TXD_N, ETH1_SG_TXD_P, ETH1_SG_RXD_N, ETH1_SG_RXD_P

Note 6. Given specification includes injected currents.

Note 7. After mounting

Note 8. Voltage overshoot 5.8 V to 6.5 V is permissible, cumulative time is less than 2 h. Voltage overshoot 5.5 V to 5.8 V is permissible, cumulative time is less than 100 h.

Note 9. Voltage overshoot 1.205 V to 1.42 V is permissible, cumulative time is less than 2 h. Voltage overshoot 1.155 V to 1.205 V is permissible, cumulative time is less than 100 h.

Note 10. Voltage overshoot 3.9 V to 4.6 V is permissible, cumulative time is less than 2 h. Voltage overshoot 3.6 V to 3.9 V is permissible, cumulative time is less than 100 h.

Note 11. Input voltage must be kept within -0.8 V =< Vin =< 6.5 V. Power supply voltage must be kept within rated values. Injection current must be kept within rated values on all states include ramp-up/down, and poweron/off. Injection current effects power dissipation in the package for thermal characteristics.

Note 12. See **Table 3.2, Supply Voltage Characteristics *1**.

Note 13. See E02_01_List_of_Pin_Assignment for understaiding which is 5V tolerant pin.

CAUTION

- **Even momentarily exceeding the absolute maximum rating for just one parameter creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
- **Input voltage, analog reference voltage and analog input voltage must not exceed 6.5 V**
- **Even in case when input voltage does not meet the specified characteristics, it is accepted if the injected current characteristics specified in Section 3.2.7, Injection Current Characteristics are met.**

3.2 DC Characteristics

3.2.1 Operational Conditions

Conditions:

- Temperature range: Tj (min) to Tj (max).
- VSS = SVRAVSS = SVRDRVSS = AnVSS = ADSVSS = AFCVSS
- Reference ground potential: VSS = 0 V.

Table 3.2 Supply Voltage Characteristics (1/2)*1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System control supply voltage	V_{SYSVCC}	*2	3.0		3.6	V
			4.5		5.5	V
Regulator supply voltage	V_{VCC}		3.0		3.6	V
			4.5		5.5	V
Core supply voltage	V_{VDD}		1.025	1.09	1.155	V
IO supply voltage	V_{E0VCC} V_{E1VCC} V_{E2VCC}		3.0		3.6	V
			4.5		5.5	V
RHSIF/RHSB supply voltage	V_{LVDVCC}		3.0		3.6	V
			4.5		5.5	V
ADC supply voltage	V_{A0VCC} V_{A1VCC} V_{A2VCC} V_{A3VCC} V_{ADSVCC}		3.0*7		3.6	V
			4.5		5.5	V
ADC reference voltage supply	$V_{A0VREFH}$ $V_{A1VREFH}$ $V_{A2VREFH}$ $V_{A3VREFH}$ $V_{ADSVREFH}$		3.0*7		3.6	V
			4.5		5.5	V
SVR supply voltage	$V_{SVRDRVCC}$	*3	3.0		3.6	V
			4.5		5.5	V
	$V_{SVRAVCC}$		3.0		3.6	V
			4.5		5.5	V
Aurora I/F supply voltage (Analog) Aurora control IO supply voltage	V_{EMUVCC}		3.0		3.6	V
Aurora I/F supply voltage (Digital) Aurora control core supply voltage ERAM core supply voltage	V_{EMUVDD}	Aurora used	1.04	1.09	1.14	V
		Aurora unused	1.025	1.09	1.155	V
SGMII supply voltage*5	$V_{GETH0PVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused	3.0		3.6	V
			4.5		5.5	V
	$V_{GETH0BVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused		*4		V
Fast Comparator, RD Converter supply voltage	V_{AFCVCC}		3.0*7		3.6	V
			4.5		5.5	V
Power supply for OSC*6	V_{OSCVCC}		3.0		3.6	V
			4.5		5.5	V

Table 3.2 Supply Voltage Characteristics (2/2)*1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HSIF (debug) supply voltage*8	V_{J0VCC}	-	3.0		3.6	V
			4.5		5.5	V
HSIF clock (debug) supply voltage*8	V_{J1VCC}	-	3.0		3.6	V
			4.5		5.5	V

Note 1. Use this device with the following conditions.
SVRDRVCC ≥ SYSVCC = SVRAVCC
VCC = OSCVCC = J0VCC = J1VCC
SYSVCC=VCC, when SBMD=1. SYSVCC = VCC condition is not needed, when SBMD=0.
E0VCC = LVDVCC
A0VCC ≥ A0VREFH
A1VCC ≥ A1VREFH
A2VCC ≥ A2VREFH
A3VCC ≥ A3VREFH
ADSVCC ≥ ADSVREFH
A0VCC = A1VCC = A2VCC = A3VCC = ADSVCC = AFCVCC
GETH0PVCC = GETH0BVCC, when SGMII use.

Note 2. SYSVCC is monitored by POC, see **Section 3.2.11, Voltage Detector (POC) Characteristics**.

Note 3. Maximum allowable noise for SVRDRVCC is 500mV peak to peak.

Note 4. Input 3.0V to 3.6V voltage or connect to VSS with 1 kΩ or more pull-down resistance.

Note 5. Maximum allowable noise for SGMII supply voltage power is 50mV peak to peak.

Note 6. Maximum allowable noise for OSCVCC is 100mV peak to peak.
When MainOSC is used as the clock source of SGMII, allowable noise for OSCVCC will be 50mV peak to peak.

Note 7. SAR-ADC and FCMP can work at 3.3V voltage. When SAR-ADC or FCMP work at 3.3V voltage, please set DS-ADC, Cyclic-ADC and RD Converter to module standby mode.

Note 8. Maximum allowable noise for J0VCC and J1VCC are 100mV peak to peak.

CAUTION

During operations, supply the specified voltages to all power lines. When stopping operation, turn off all power supplies.

3.2.2 Input Voltage Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.3 Input Voltage Characteristics (Input Voltage IOVCC=3.0~3.6V)

Parameter	Symbol	Condition*1		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	SHMT1		0.65 × IOVCC		IOVCC + 0.3	V
	V_{IH2}	SHMT2	Other than the following	0.75 × IOVCC		IOVCC + 0.3	V
			5V tolerant pins	0.75 × IOVCC		5.5 + 0.3	V
	V_{IH3}	SHMT4		0.80 × IOVCC		IOVCC + 0.3	V
	V_{IH4}	SHMTMSC		0.60 × IOVCC		IOVCC + 0.3	V
	V_{IH5}	TTL	Other than the following	2.2		IOVCC + 0.3	V
			5V tolerant pins	2.2		5.5 + 0.3	V
Low level input voltage	V_{IL1}	SHMT1		–0.3		0.35 × IOVCC	V
	V_{IL2}	SHMT2		–0.3		0.25 × IOVCC	V
	V_{IL3}	SHMT4		–0.3		0.50 × IOVCC	V
	V_{IL4}	SHMTMSC		–0.3		0.36 × IOVCC	V
	V_{IL5}	TTL		–0.3		0.8	V
Input hysteresis for Schmitt *3	V_{HS1}	SHMT1		0.3			V
	V_{HS2}	SHMT2		0.2 × IOVCC			V
	V_{HS3}	SHMT4		0.1			V
	V_{HS4}	SHMTMSC		0.082 × IOVCC			V
Clock input voltage (X1) (MOSC_EXCLKINPUTZ = 0)*4	V_{IH}			OSCVCC × 0.7		OSCVCC + 0.3	V
	V_{IL}			−0.3		OSCVCC × 0.2	V
Clock input voltage (X1) (MOSC_EXCLKINPUTZ = 1)*4	V_{IH}			2.0		OSCVCC + 0.3	V
	V_{IL}			−0.3		0.5	V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. For X1 pin, see **Section 3.3.4.1, Main Oscillator Characteristics**.

Note 3. The configured drive strength of the output terminals in a power group might affect the hysteresis characteristics of the input terminals in the same power group. See Appendix file "E02_01_List_of_Pin_Assignment.xlsx" for the assignment of power group.

Note 4. See RH850/U2B Group User's Manual:Hardware **Section 63.12.16, OPBT10 — Option Byte 10 for the setting of MOSC_EXCLKINPUTZ**.

Table 3.4 Input Voltage Characteristics (Input Voltage IOVCC=4.5~5.5V)

Parameter	Symbol	Condition*1		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	SHMT1		0.65 × IOVCC		IOVCC + 0.3	V
	V_{IH2}	SHMT2	Other than the following	0.75 × IOVCC		IOVCC + 0.3	V
			5V tolerant pins	0.75 × IOVCC		5.5 + 0.3	V
	V_{IH3}	SHMT4		0.80 × IOVCC		IOVCC + 0.3	V
	V_{IH4}	SHMTMSC		0.60 × IOVCC		IOVCC + 0.3	V
	V_{IH5}	TTL	Other than the following	2.2		IOVCC + 0.3	V
			5V tolerant pins	2.2		5.5 + 0.3	V
Low level input voltage	V_{IL1}	SHMT1		–0.3		0.35 × IOVCC	V
	V_{IL2}	SHMT2		–0.3		0.25 × IOVCC	V
	V_{IL3}	SHMT4		–0.3		0.50 × IOVCC	V
	V_{IL4}	SHMTMSC		–0.3		0.36 × IOVCC	V
	V_{IL5}	TTL		–0.3		0.8	V
Input hysteresis for Schmitt *3	V_{HS1}	SHMT1		0.4			V
	V_{HS2}	SHMT2		0.2 × IOVCC			V
	V_{HS3}	SHMT4		0.1			V
	V_{HS4}	SHMTMSC		0.082 × IOVCC			V
Clock input voltage (X1) (MOSC_EXCLKINPUTZ = 0) *4	V_{IH}			OSCVCC × 0.7		OSCVCC + 0.3	V
	V_{IL}			−0.3		OSCVCC × 0.2	V
Clock input voltage (X1) (MOSC_EXCLKINPUTZ = 1) *4	V_{IH}			2.0		OSCVCC + 0.3	V
	V_{IL}			−0.3		0.5	V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. For X1 pin, see **Section 3.3.4.1, Main Oscillator Characteristics**.

Note 3. The configured drive strength of the output terminals in a power group might affect the hysteresis characteristics of the input terminals in the same power group. See Appendix file "E02_01_List_of_Pin_Assignment.xlsx" for the assignment of power group.

Note 4. See RH850/U2B Group User's Manual:Hardware **Section 63.12.16, OPBT10 — Option Byte 10 for the setting of MOSC_EXCLKINPUTZ**.

3.2.3 Input Leakage Current Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions.**
- See RH850/U2B Group User's Manual:Hardware **Section 2, Pin Functions** and the appendix "E02_01_List_of_Pin_Assignment.xlsx" for understanding pins which each package has.

Table 3.5 Input Leakage Current (1/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LIH1}	Vin = 0 to EnVCC Vin = 0 to SYSVCC Vin = 0 to VCC Vin = 0 to OSCVCC Vin = 0 to EMUVCC (U2B-FCC only) • Except terminals specified on the condition of I_{LIH2} through I_{LIH8}.	Tj ≤ 105 °C			0.5	µA
			105 °C < Tj ≤ 150 °C			1.0	µA
			150 °C < Tj			2.0	µA
	I_{LIH2}	Vin = 0 to EnVCC Vin = 0 to LVDVCC P10_0 to P10_5, P13_0 to P13_3, P14_4 to P14_5, P21_2 to P21_5, P24_4 to P24_7, P25_3 to P25_6, P25_12 to P25_15	Tj ≤ 105 °C			0.5	µA
			105 °C < Tj ≤ 150 °C			1.0	µA
			150 °C < Tj			2.0	µA
	I_{LIH3}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*4 Excluding RDC3AL pins (RDC3ALn_S1, RDC3ALn_S2, RDC3ALn_S3, RDC3ALn_S4, RDC3ALn_RSO and RDC3ALn_COM)	Tj ≤ 150 °C			0.18	µA
			150 °C < Tj			0.27	µA
	I_{LIH4}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*1 Excluding RDC3AL pins (RDC3ALn_S1, RDC3ALn_S2, RDC3ALn_S3, RDC3ALn_S4, RDC3ALn_RSO and RDC3ALn_COM)	Tj ≤ 150 °C			0.26	µA
			150 °C < Tj			0.39	µA
	I_{LIH5}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*2 Including RDC3AL pins (RDC3ALn_S1, RDC3ALn_S2, RDC3ALn_S3, RDC3ALn_S4)	Tj ≤ 150 °C			0.5	µA
			150 °C < Tj			0.75	µA
	I_{LIH6}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*3 Including RDC3AL pins (RDC3ALn_RSO or RDC3ALn_COM)	Tj ≤ 150 °C			1.0	µA
			150 °C < Tj			1.5	µA
	I_{LIH7}	Vin = 0 to J0VCC Vin = 0 to VCC • JP0_0, JP0_1, JP0_3, JP0_5 (U2B-FCC only)	Tj ≤ 105 °C			0.5	µA
			105 °C < Tj ≤ 150 °C			2.0	µA
			150 °C < Tj			4.0	µA

Table 3.5 Input Leakage Current (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
	I_{LIH8}	Vin = 0 to J1VCC Vin = 0 to VCC • JP0_2 (U2B-FCC only)	Tj ≤ 105 °C			1.0	µA
			105 °C < Tj ≤ 150 °C			2.0	µA
			150 °C < Tj			4.0	µA
Input leakage current	I_{LIL1}	Vin = 0 to EnVCC Vin = 0 to SYSVCC Vin = 0 to VCC Vin = 0 to OSCVCC Vin = 0 to EMUVCC (U2B-FCC only) • Except terminals specified on the condition of I_{LIL2} through I_{LIL8}.	Tj ≤ 105 °C			-0.5	µA
			105 °C < Tj ≤ 150 °C			-1.0	µA
			150 °C < Tj			-2.0	µA
	I_{LIL2}	Vin = 0 to EnVCC Vin = 0 to LVDVCC P10_0 to P10_5, P13_0 to P13_3, P14_4 to P14_5, P21_2 to P21_5, P24_4 to P24_7, P25_3 to P25_6, P25_12 to P25_15	Tj ≤ 105 °C			-0.5	µA
			105 °C < Tj ≤ 150 °C			-1.0	µA
			150 °C < Tj			-2.0	µA
	I_{LIL3}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*4 Excluding RDC3AL pins (RDC3ALn_S1, RDC3ALn_S2, RDC3ALn_S3, RDC3ALn_S4, RDC3ALn_RSO and RDC3ALn_COM)	Tj ≤ 150 °C			-0.18	µA
			150 °C < Tj			-0.27	µA
	I_{LIL4}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*1 Excluding RDC3AL pins (RDC3ALn_S1, RDC3ALn_S2, RDC3ALn_S3, RDC3ALn_S4, RDC3ALn_RSO and RDC3ALn_COM)	Tj ≤ 150 °C			-0.26	µA
			150 °C < Tj			-0.39	µA
	I_{LIL5}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*2 Including RDC3AL pins (RDC3ALn_S1, RDC3ALn_S2, RDC3ALn_S3 or RDC3ALn_S4)	Tj ≤ 150 °C			-0.5	µA
			150 °C < Tj			-0.75	µA
	I_{LIL6}	Vin = 0 to AnVCC Vin = 0 to ADSVCC Vin = 0 to AFCVCC • ANnpq*3 Including RDC3AL pins (RDC3ALn_RSO or RDC3ALn_COM)	Tj ≤ 150 °C			-1.0	µA
			150 °C < Tj			-1.5	µA
	I_{LIL7}	Vin = 0 to J0VCC Vin = 0 to VCC • JP0_0, JP0_1, JP0_3, JP0_5 (U2B-FCC only)	Tj ≤ 105 °C			-0.5	µA
			105 °C < Tj ≤ 150 °C			-2.0	µA
			150 °C < Tj			-4.0	µA
	I_{LIL8}	Vin = 0 to J1VCC Vin = 0 to VCC • JP0_2 (U2B-FCC only)	Tj ≤ 105 °C			-1.0	µA
			105 °C < Tj ≤ 150 °C			-2.0	µA
			150 °C < Tj			-4.0	µA

Note 1. Target pin is the following.

[U2B24FCC, U2B10FCC]
AN020 to AN023, AN030 to AN033, AN040 to AN043, AN050 to AN053, AN060 to AN063,
AN112, AN113, AN120,
AN240 to AN243, AN250 to AN253, AN260 to AN263, AN270 to AN273,
AN302, AN303, AN310 to AN313
[U2B10]
AN020 to AN023, AN030 to AN033, AN040 to AN043, AN050 to AN053, AN060 to AN063,
AN240, AN241, AN250 to AN253
[U2B6FCC]
AN020 to AN023, AN030 to AN033, AN040 to AN043,
AN112, AN113, AN120,
AN252, AN253, AN261, AN270
[U2B6]
AN252, AN253

Note 2. Target pin is the following.
[U2B6FCC, U2B6]
AN240 to AN243, AN260, AN262, AN271, AN272

Note 3. Target pin is the following.
[U2B6FCC, U2B6]
AN250, AN251, AN263, AN273

Note 4. Target pin is following.
[Other than U2B6]
AN000 to AN003, AN010 to AN013, AN100 to AN103, AN110 to AN111, AN121 to AN123, AN200 to AN203,
AN210 to AN213, AN220 to AN223, AN230 to AN233, AN300 to AN301, AN360 to AN363, AN370 to
AN373, AN380 to AN383, AN390 to AN393
[U2B6]
AN000 to AN003, AN010 to AN013, AN100 to AN103, AN110 to AN111, AN121 to AN123, AN200 to AN203,
AN210 to AN213, AN220 to AN223, AN230 to AN233

3.2.4 Pull-up/Pull-down MOS Current Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.6 Pull-up/Pull-down Characteristics (IOVCC = 3.0 ~ 3.6V)

Parameter	Symbol	Condition		MIN.	TYP.*1	MAX.	Unit
Input pull-up current source	I_{PU1}	Other than below	IOVCC*1 = 3.0 to 3.6V Vin = 0V PULVSEL5_n=0	30		150	µA
		SHMTMSC support pin	IOVCC*1 = 3.0 to 3.6V Vin = 0V PISn_m=1, PISAn_m=1	15		90	µA
Input pull-down current source	I_{PD1}	Other than below	IOVCC*1 = 3.0 to 3.6V Vin = IOVCC*1 PULVSEL5_n=0	30		150	µA
		SHMTMSC support pin	IOVCC*1 = 3.0 to 3.6V Vin = IOVCC*1 PISn_m=1, PISAn_m=1	15		120	µA
		$\overline{\text{RESET}}$ $\overline{\text{AURORES}}$	IOVCC*1 = 3.0 to 3.6V Vin = IOVCC*1			110	µA
		*2	IOVCC*1 = 3.0 to 3.6V Vin = IOVCC*1	30		150	µA

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. FLMD0, SBMD, TRST, ICE.

Table 3.7 Pull-up/Pull-down Characteristics (IOVCC = 4.5 ~ 5.5V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input pull-up current source	I_{PU1}	Other than below	IOVCC*1 = 4.5 to 5.5V Vin = 0V	30		350	µA
		SHMTMSC support pin	IOVCC*1 = 4.5 to 5.5V Vin = 0V PISn_m=1, PISAn_m=1	40		190	µA
Input pull-down current source	I_{PD1}	Other than below	IOVCC*1 = 4.5 to 5.5V Vin = IOVCC*1	30		350	µA
		SHMTMSC support pin	IOVCC*1 = 4.5 to 5.5V Vin = IOVCC*1 PISn_m=1, PISAn_m=1	50		240	µA
		$\overline{\text{RESET}}$	SYSVCC = 4.5 to 5.5V Vin = SYSVCC			110	µA
		*2	IOVCC*1 = 4.5 to 5.5V Vin = IOVCC*1	30		350	µA

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. FLMD0, SBMD, TRST, ICE.

3.2.5 Output Voltage Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.8 Output Voltage Characteristics

Parameter	Symbol	Condition*1		MIN.*1	TYP.	MAX.	Unit
Output resistance	R_{O11}	Drive strength = 1 (Very High)	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	6		40	Ω
	R_{O12}	Drive strength = 2 (High)	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	11		72	Ω
	R_{O13}	Drive strength = 3 (Medium)	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	18		100	Ω
	R_{O14}	Drive strength = 4 (Low)	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	32		200	Ω
	R_{O15}	Drive strength = 5 (Very low)	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	61		400	Ω
High level output voltage	V_{OH1}	Drive strength = 1 (Very High)	I_{OH} = –4 mA / pin (4 output pins)*2	IOVCC–0.8			V
			I_{OH}= –2 mA / pin (4 output pins)*2	IOVCC–0.5			V
	V_{OH2}	Drive strength = 2 (High)	I_{OH} = –4 mA / pin (8 output pins)*2	IOVCC–0.8			V
			I_{OH}= –2 mA / pin (8 output pins)*2	IOVCC–0.5			V
	V_{OH3}	Drive strength = 3 (Medium)	I_{OH} = –4 mA / pin (8 output pins)*2	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (8 output pins)*2	IOVCC–0.5			V
	V_{OH4}	Drive strength = 4 (Low)	I_{OH} = –2 mA / pin (16 output pins)*2	IOVCC–0.7			V
			I_{OH} = –1 mA / pin (16 output pins)*2	IOVCC–0.5			V
	V_{OH5}	Drive strength = 5 (Very low)	I_{OH} = –1 mA / pin (16 output pins)*2	IOVCC–0.7			V
			I_{OH} = –500 µA / pin (16 output pins)*2	IOVCC–0.5			V
	V_{OH6}	RHSB	I_{OH} = −2mA / pin (14 output pins)*2	IOVCC–0.4			V
Low level output voltage	V_{OL1}	Drive strength = 1 (Very High)	I_{OL} = 4 mA / pin (4 output pins)*2			0.8	V
			I_{OL} = 2 mA / pin (4 output pins)*2			0.5	V
	V_{OL2}	Drive strength = 2 (High)	I_{OL} = 4 mA / pin (8 output pins)*2			0.8	V
			I_{OL} = 2 mA / pin (8 output pins)*2			0.5	V
	V_{OL3}	Drive strength = 3 (Medium)	I_{OL} = 4 mA / pin (8 output pins)*2			0.7	V
			I_{OL} = 2 mA / pin (8 output pins)*2			0.5	V
	V_{OL4}	Drive strength = 4 (Low)	I_{OL} = 2 mA / pin (16 output pins)*2			0.7	V
			I_{OL} = 1 mA / pin (16 output pins)*2			0.5	V
	V_{OL5}	Drive strength = 5 (Very low)	I_{OL} = 1 mA / pin (16 output pins)*2			0.7	V
			I_{OL} = 500 µA / pin (16 output pins)*2			0.5	V
	V_{OL6}	RHSB	I_{OL} = 2mA / pin (14 output pins)*2			0.4	V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. The number of pin indicates simultaneous ON in one power. The influence of the noise emission should be considered when switching the output level.

3.2.6 Output Current

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.9 Allowable Output Current Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level allowable output current	$\|I_{OH}\|$	per pin			8	mA
	$\Sigma\|I_{OH}\|$	Each EnVCC			60	mA
Low level allowable output current	$\|I_{OL}\|$	per pin			8	mA
	$\Sigma\|I_{OL}\|$	Each EnVCC			60	mA

3.2.7 Injection Current Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.10 Injection Current Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DC injection current (per pin)	I_{INJ_DIN}	Digital pin *1, *3	–2		3	mA
	I_{INJ_AIN}	Analog pin*2	–3		3	mA
DC injection current (each power supply)	I_{INJ_E0VCC}	E0VCC			50	mA
	I_{INJ_E1VCC}	E1VCC			50	mA
	I_{INJ_E2VCC}	E2VCC			50	mA
	I_{INJ_A0VCC}	A0VCC			20	mA
	I_{INJ_A1VCC}	A1VCC			20	mA
	I_{INJ_A2VCC}	A2VCC			20	mA
	I_{INJ_A3VCC}	A3VCC			20	mA
	I_{INJ_ADSVCC}	ADSVCC			20	mA
	I_{INJ_AFCVCC}	AFCVCC			20	mA
DC injection current (total)					80	mA

Note 1. Injection current to the logic pin multiplexed with the LVDS function is prohibited when the LVDS function is used. When the LVDS function is not used, Injection current to the logic pin multiplexed with the LVDS function causes at maximum an additional 1 µA leakage current at the complimentary P/N pin. For example, injection current to RHSB0FCLP causes at maximum an additional 1 µA leakage current at RHSB0FCLN.

Note 2. If injection current is applied to following RDC3AL and pins multiplexed with these, it will affect the specification characteristics of Resolver to Digital Converter (RDC3AL), Analog to Digital Converter (ADCK), Delta-Sigma Analog to Digital Converter (DSADC), and Fast Comparator (FCMP).
[U2B24-FCC, U2B10-FCC]
AN252, AN253, AN261, AN270
[U2B6-FCC, U2B6]
AN240 to AN243, AN250 to AN253,
AN260 to AN263, AN270 to AN273

Note 3. [FCC only] Injection current to the JP0_3 or JP0_0 pin multiplexed with the LVDS function causes at maximum an additional 3 µA leakage current at the complimentary P/N pin.

NOTE

- Input voltage must be kept within –0.8V ≤ Vin ≤ 6.0V
- Power supply voltage must be kept within operating conditions.
- Injection current effects power dissipation in the package for thermal characteristics.

3.2.8 LVDS Characteristics

3.2.8.1 LVDS Driver Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.11 LVDS Driver Characteristics (based on IEEE 1596.3-1996 Reduced)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output low-level voltage	V_{LVDSOL}		1000			mV
Output high-level voltage	V_{LVDSOH}				1400	mV
Output differential voltage	V_{LVDSOD}		150		250	mV
Offset voltage	V_{LVDSOS}		1.125		1.275	V
Output impedance	R_{LVDSOI}		40		300	Ω

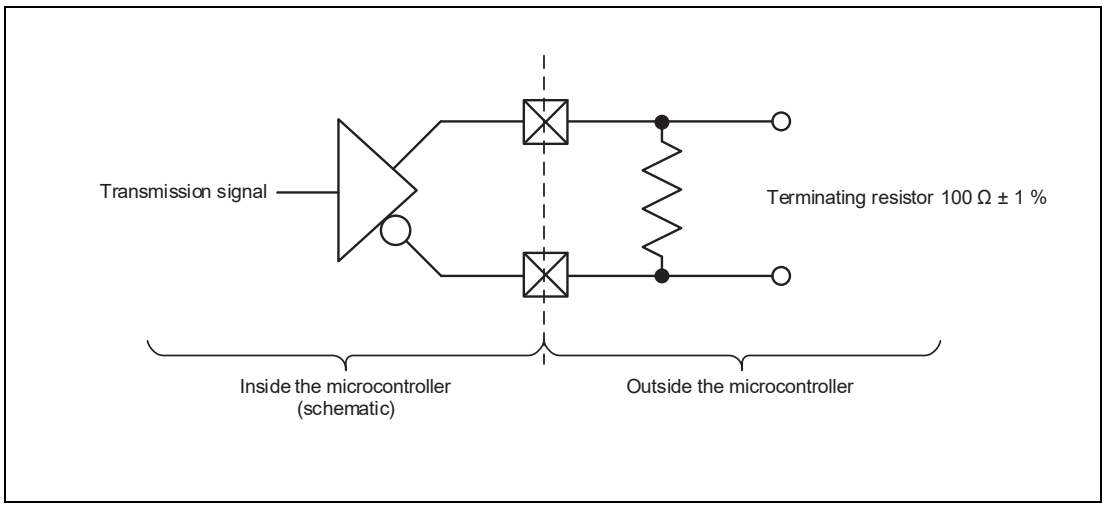


Figure 3.1 LVDS Driver Measurement Conditions

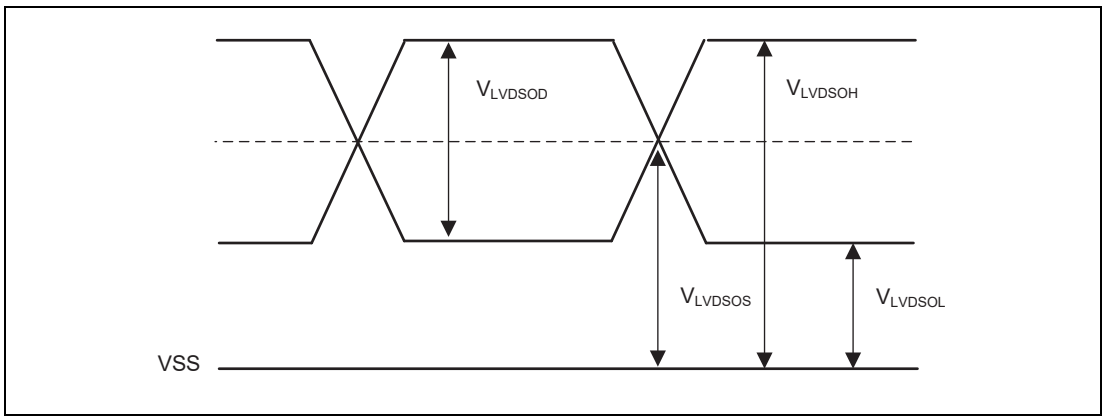


Figure 3.2 Meaning of LVDS Driver Symbols

Table 3.12 DC Characteristics (LVDS Driver (ANSI/TIA/EIA-644 standard) Characteristics)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output differential voltage	V_{OD}		250	—	450	mV
Offset voltage	V_{OS}		1125	—	1375	mV

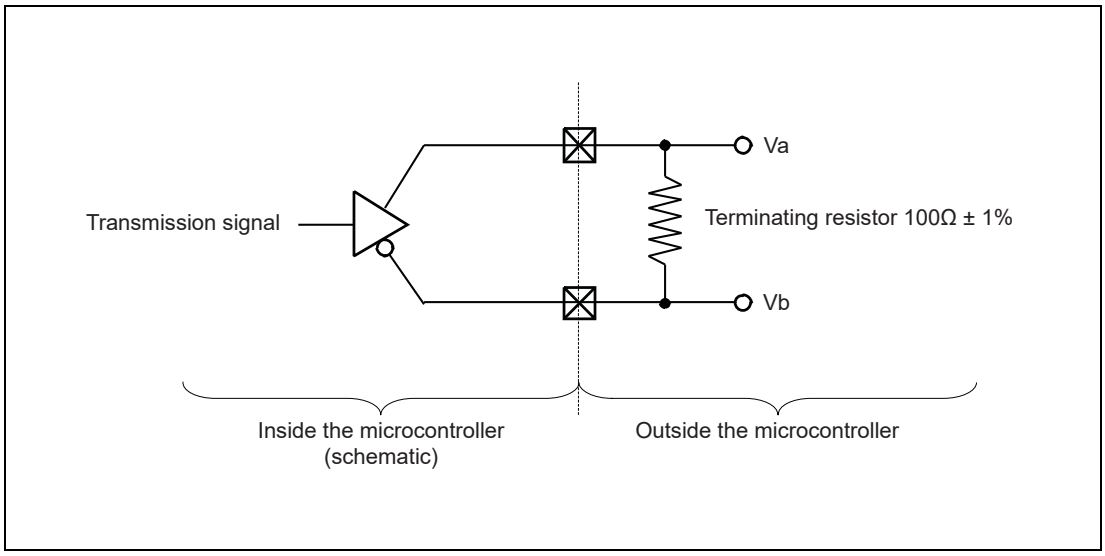


Figure 3.3 LVDS Driver Va / Vb Measurement Conditions

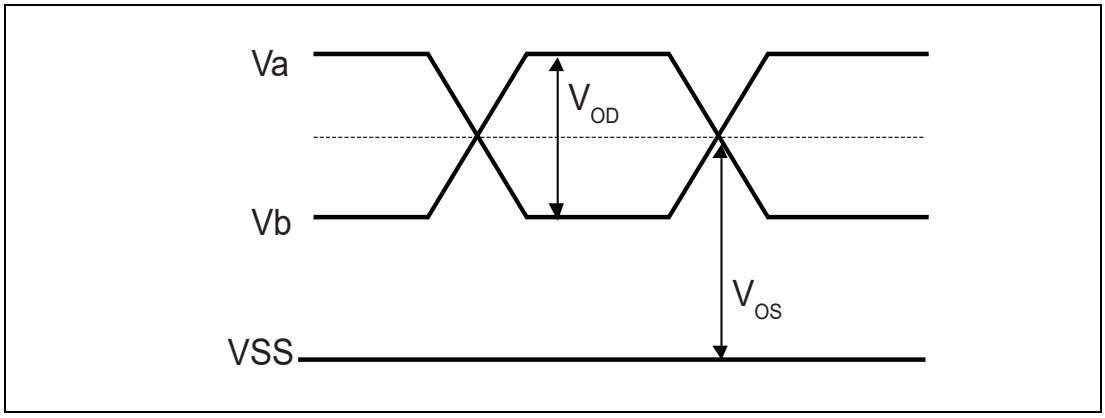


Figure 3.4 Definition of LVDS Driver Symbols

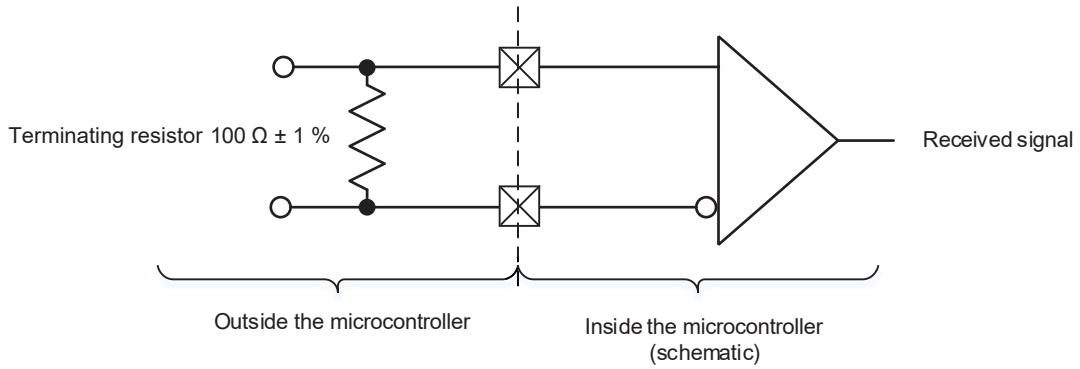
3.2.8.2 LVDS Receiver Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.13 LVDS Receiver Characteristics (based on ANSI/TIA/EIA-644)

Parameter	Symbol	Condition	MIN.	TYP.	MAX	Unit
Differential Input threshold voltage	$V_{LVDSIDTH}$		–100		100	mV
Input voltage range	V_{LVDI}		0		2.4	V
		RHSIF or RHSB+with Manchester 50Mbps or more used	0.5		2.0	V
Input impedance	R_{IN}	RHSIF Debug interface	75	100	140	Ω



Note: Be sure to connect a terminating resistor of the LVDS receiver nearest the microcontroller, because it isn't built in the microcontroller.

Figure 3.5 LVDS Receiver Measurement Conditions

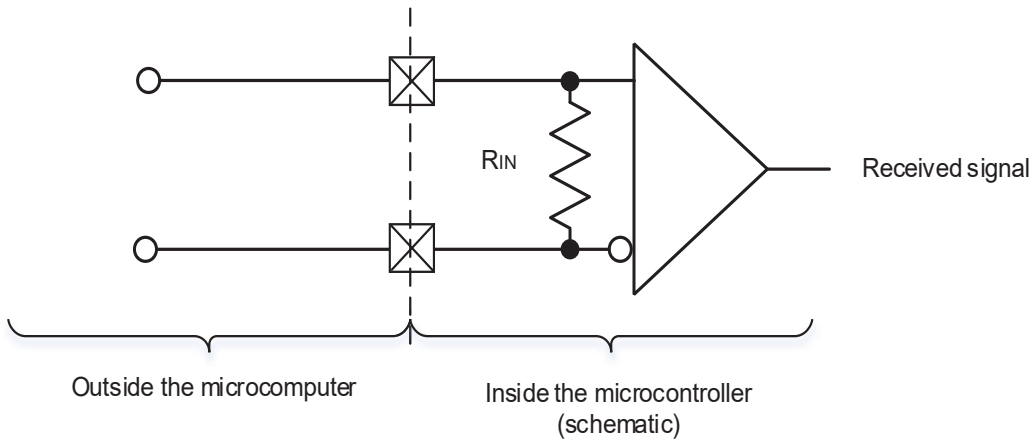


Figure 3.6 LVDS Receiver Measurement Conditions (RHSIF Debug Interface)

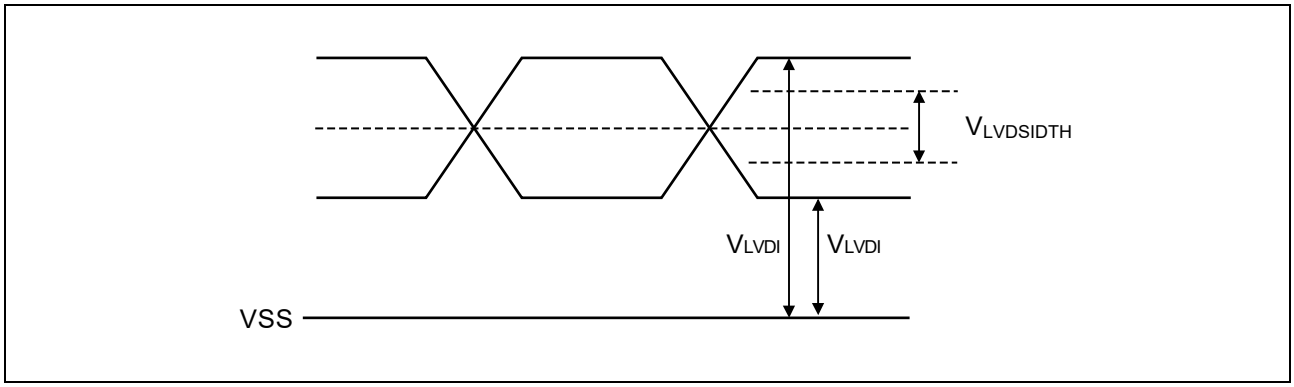


Figure 3.7 Meaning of LVDS Receiver Symbols

3.2.9 IO Capacitances

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.14 IO Capacitances *1, *2,*3,*4

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V for non measurement pins				10	pF
Input/output capacitance	C_{IO}		Other than the following			10	pF
			RDC3AL pins (RDC3ALn_RSO or RDC3ALn_COM)			15	pF
Output capacitance	C_O					10	pF

Note 1. This capacity is the capacity value per BGA_Ball 1 terminal.

Note 2. X1 and X2 are excluded. About X1 and X2 configuration, see RH850/U2B Group User's Manual:Hardware **Section 15, Clock Controller**.

Note 3. For analog input pins (ANnpq), refer to **Section 3.4, A/D Converter Characteristics**.

Note 4. SVRPGATE and SVRNGATE are excluded.

3.2.10 Supply Current Characteristics

3.2.10.1 General Definition

Power consumption except for the current of I/O buffer (I_{EnVCC}) is specified below.

The parameter I_{EnVCC} depends on customer's application and thus need to be defined by customer in order to determine the total power dissipation of a device.

3.2.10.2 Power Supply Currents

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.15 Current consumption for RH850/U2B24 (SYSVCC=VCC=3.0V～3.6V) *2, *3

Parameter	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.1*4	MAX.2*5	Unit
RUN mode current U2B-FCC (U2B24 mode)	$I_{SYSVCC\_R\_FCC}$	SYSVCC (SBMD=0)	400 MHz		0.7	5	-	mA
			320 MHz		0.7	5	-	mA
			240 MHz		0.7	5	-	mA
		SYSVCC (SBMD=1)	400 MHz		5	30	-	mA
			320 MHz		5	30	-	mA
			240 MHz		5	30	-	mA
	$I_{VCC\_R\_FCC}$	VCC/OSCVCC	400 MHz		25	120	-	mA
			320 MHz		25	120	-	mA
			240 MHz		25	120	-	mA
	$I_{ISOVDD\_R\_FCC}$	ISOVDD	400 MHz*8		1930	4600	-	mA
			320 MHz*9		1860	4080	-	mA
			240 MHz*10		1490	3560	-	mA
Programming / Erasure of the flash memory U2B-FCC (U2B24 mode)	$I_{CC\_FPE\_FCC}$	VCC/OSCVCC			120	260	-	mA
Current during reset U2B-FCC (U2B24 mode)	$I_{SYSVCC\_RST\_FCC}$	SYSVCC(SBMD=0)		1	2.1	8	-	mA
		SYSVCC(SBMD=1)		1	2.2	34	-	mA
	$I_{VCC\_RST\_FCC}$	VCC/OSCVCC		10	20	100	-	mA
	$I_{ISOVDD\_RST\_FCC}$	ISOVDD		300	850	3200	-	mA
STOP mode current*6 U2B-FCC (U2B24 mode)	$I_{SYSVCC\_S\_FCC}$	SYSVCC(SBMD=0)			1.6	5	-	mA
		SYSVCC(SBMD=1)			1.8	30	-	mA
	$I_{VCC\_S\_FCC}$	VCC			0.1	1	-	mA
	$I_{ISOVDD\_S\_FCC}$	ISOVDD			25	2150	-	mA
	$I_{OSCVCC\_S\_FCC}$	OSCVCC			3.8	8	-	mA
DeepSTOP mode current*6 (SBMD = 1) U2B-FCC (U2B24 mode)	$I_{SYSVCC\_DS\_FCC}$	SYSVCC			1.7	34	-	mA
	$I_{VCC\_DS\_FCC}$	VCC			200	400	-	µA
	$I_{ISOVDD\_DS\_FCC}$	ISOVDD			25	2100*7	-	mA
	$I_{OSCVCC\_DS\_FCC}$	OSCVCC			100	400	-	µA
Cyclic RUN mode current*6 (SBMD = 1) U2B-FCC (U2B24 mode)	$I_{SYSVCC\_CR\_FCC}$	SYSVCC	10 MHz		3	30	-	mA
	$I_{VCC\_CR\_FCC}$	VCC	10 MHz		0.2	1.2	-	mA
	$I_{ISOVDD\_CR\_FCC}$	ISOVDD	10 MHz		440	2350	-	mA
	$I_{OSCVCC\_CR\_FCC}$	OSCVCC	10 MHz		3.8	8	-	mA
Cyclic STOP mode current*6 (SBMD = 1) U2B-FCC (U2B24 mode)	$I_{SYSVCC\_CS\_FCC}$	SYSVCC			2	30	-	mA
	$I_{VCC\_CS\_FCC}$	VCC			0.1	1	-	mA
	$I_{ISOVDD\_CS\_FCC}$	ISOVDD			25	2150	-	mA
	$I_{OSCVCC\_CS\_FCC}$	OSCVCC			3.8	8	-	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C

- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 3.3 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.
Note 3. The above value does not include the current of I/O buffer.
Note 4. Tj = 150°C
Note 5. Tj = 160°C
Note 6. MainOSC is stopped.
Note 7. Indicated leak current wil be applied if the power continues supplying to ISOVDD during DeepSTOP mode.
Note 8. DFP frequency is 400 MHz.
Note 9. DFP frequency is 320 MHz.
Note 10. DFP frequency is 240 MHz.

Table 3.16 Current consumption for RH850/U2B24 (SYSVCC=VCC=4.5V～5.5V) *2, *3

Parameter	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.1*4	MAX.2*5	Unit
RUN mode current U2B-FCC (U2B24 mode)	$I_{SYSVCC\_R\_FCC}$	SYSVCC (SBMD=0)	400 MHz		0.7	5	-	mA
			320 MHz		0.7	5	-	mA
			240 MHz		0.7	5	-	mA
		SYSVCC (SBMD=1)	400 MHz		5	30	-	mA
			320 MHz		5	30	-	mA
			240 MHz		5	30	-	mA
	$I_{VCC\_R\_FCC}$	VCC/OSCVCC	400 MHz		25	120	-	mA
			320 MHz		25	120	-	mA
			240 MHz		25	120	-	mA
	$I_{ISOVDD\_R\_FCC}$	ISOVDD	400 MHz*8		1930	4600	-	mA
			320 MHz*9		1860	4080	-	mA
			240 MHz*10		1490	3560	-	mA
Programming / Erasure of the flash memory U2B-FCC (U2B24 mode)	$I_{CC\_FPE\_FCC}$	VCC/OSCVCC			120	260	-	mA
Current during reset U2B-FCC (U2B24 mode)	$I_{SYSVCC\_RST\_FCC}$	SYSVCC(SBMD=0)		1	2.1	8	-	mA
		SYSVCC(SBMD=1)		1	2.2	34	-	mA
	$I_{VCC\_RST\_FCC}$	VCC/OSCVCC		10	20	100	-	mA
	$I_{ISOVDD\_RST\_FCC}$	ISOVDD		300	850	3200	-	mA
STOP mode current*6 U2B-FCC (U2B24 mode)	$I_{SYSVCC\_S\_FCC}$	SYSVCC(SBMD=0)			1.6	5	-	mA
		SYSVCC(SBMD=1)			1.8	30	-	mA
	$I_{VCC\_S\_FCC}$	VCC			0.1	1	-	mA
	$I_{ISOVDD\_S\_FCC}$	ISOVDD			25	2150	-	mA
	$I_{OSCVCC\_S\_FCC}$	OSCVCC			3.8	8	-	mA
DeepSTOP mode current*6 (SBMD = 1) U2B-FCC (U2B24 mode)	$I_{SYSVCC\_DS\_FCC}$	SYSVCC			1.7	34	-	mA
	$I_{VCC\_DS\_FCC}$	VCC			200	400	-	µA
	$I_{ISOVDD\_DS\_FCC}$	ISOVDD			25	2100*7	-	mA
	$I_{OSCVCC\_DS\_FCC}$	OSCVCC			100	400	-	µA
Cyclic RUN mode current*6 (SBMD = 1) U2B-FCC (U2B24 mode)	$I_{SYSVCC\_CR\_FCC}$	SYSVCC	10 MHz		3	30	-	mA
	$I_{VCC\_CR\_FCC}$	VCC	10 MHz		0.2	1.2	-	mA
	$I_{ISOVDD\_CR\_FCC}$	ISOVDD	10 MHz		440	2350	-	mA
	$I_{OSCVCC\_CR\_FCC}$	OSCVCC	10 MHz		3.8	8	-	mA
Cyclic STOP mode current*6 (SBMD = 1) U2B-FCC (U2B24 mode)	$I_{SYSVCC\_CS\_FCC}$	SYSVCC			2	30	-	mA
	$I_{VCC\_CS\_FCC}$	VCC			0.1	1	-	mA
	$I_{ISOVDD\_CS\_FCC}$	ISOVDD			25	2150	-	mA
	$I_{OSCVCC\_CS\_FCC}$	OSCVCC			3.8	8	-	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.

Note 4. Tj = 150°C

Note 5. Tj = 160°C

Note 6. MainOSC is stopped.
Note 7. Indicated leak current wil be applied if the power continues supplying to ISOVDD during DeepSTOP mode.
Note 8. DFP frequency is 400 MHz.
Note 9. DFP frequency is 320 MHz.
Note 10. DFP frequency is 240 MHz.

Table 3.17 Current consumption for RH850/U2B10 (SYSVCC=VCC=3.0V～3.6V) *2, *3

Parameter	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.1*4	MAX.2*5	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	I_{VCC_R}	VCC/OSCVCC	400 MHz		20	80	90	mA
			320 MHz		20	80	90	mA
			240 MHz		20	80	90	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz*7		1500	2800	3000	mA
			320 MHz*8		1200	2430	2630	mA
			240 MHz*9		900	2060	2260	mA
Programming / Erasure of the flash memory	I_{CC_FPE}	VCC/OSCVCC			72	160	170	mA
Current during reset	I_{SYSVCC_RST}	SYSVCC		1	2	8	10	mA
	I_{VCC_RST}	VCC/OSCVCC		7	14	60	70	mA
	I_{ISOVDD_RST}	ISOVDD		300	645	2050	2250	mA
STOP mode current*6	I_{SYSVCC_S}	SYSVCC			1.6	5	5	mA
	I_{VCC_S}	VCC			0.1	1	1	mA
	I_{ISOVDD_S}	ISOVDD			10	1100	1300	mA
	I_{OSCVCC_S}	OSCVCC			3	8	8	mA
RUN mode current U2B-FCC (U2B10 mode)	$I_{SYSVCC\_R\_FCC}$	SYSVCC (SBMD=0)	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	$I_{VCC\_R\_FCC}$	VCC/OSCVCC	400 MHz		25	120	140	mA
			320 MHz		25	120	140	mA
			240 MHz		25	120	140	mA
	$I_{ISOVDD\_R\_FCC}$	ISOVDD	400 MHz*7		1730	4000	4600	mA
			320 MHz*8		1410	3570	4170	mA
			240 MHz*9		1120	3140	3740	mA
Programming / Erasure of the flash memory U2B-FCC (U2B10 mode)	$I_{CC\_FPE\_FCC}$	VCC/OSCVCC			95	200	220	mA
Current during reset U2B-FCC (U2B10 mode)	$I_{SYSVCC\_RST\_FCC}$	SYSVCC(SBMD=0)		1	2.1	8	10	mA
	$I_{VCC\_RST\_FCC}$	VCC/OSCVCC		10	20	100	120	mA
	$I_{ISOVDD\_RST\_FCC}$	ISOVDD		300	780	2950	3550	mA
STOP mode current*6 U2B-FCC (U2B10 mode)	$I_{SYSVCC\_S\_FCC}$	SYSVCC(SBMD=0)			1.6	5	5	mA
	$I_{VCC\_S\_FCC}$	VCC			0.1	1	1	mA
	$I_{ISOVDD\_S\_FCC}$	ISOVDD			20	2000	2600	mA
	$I_{OSCVCC\_S\_FCC}$	OSCVCC			3.8	8	8	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 3.3 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.
Note 4. Tj = 150°C
Note 5. Tj = 160°C
Note 6. MainOSC is stopped.
Note 7. DFP frequency is 400 MHz.
Note 8. DFP frequency is 320 MHz.
Note 9. DFP frequency is 240 MHz.

Table 3.18 Current consumption for RH850/U2B10 (SYSVCC=VCC=4.5V～5.5V) *2, *3

Parameter	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.1*4	MAX.2*5	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	I_{VCC_R}	VCC/OSCVCC	400 MHz		20	80	90	mA
			320 MHz		20	80	90	mA
			240 MHz		20	80	90	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz*7		1500	2800	3000	mA
			320 MHz*8		1200	2430	2630	mA
			240 MHz*9		900	2060	2260	mA
Programming / Erasure of the flash memory	I_{CC_FPE}	VCC/OSCVCC			72	160	170	mA
Current during reset	I_{SYSVCC_RST}	SYSVCC		1	2	8	10	mA
	I_{VCC_RST}	VCC/OSCVCC		7	14	60	70	mA
	I_{ISOVDD_RST}	ISOVDD		300	645	2050	2250	mA
STOP mode current*6	I_{SYSVCC_S}	SYSVCC			1.6	5	5	mA
	I_{VCC_S}	VCC			0.1	1	1	mA
	I_{ISOVDD_S}	ISOVDD			10	1100	1300	mA
	I_{OSCVCC_S}	OSCVCC			3	8	8	mA
RUN mode current U2B-FCC (U2B10 mode)	$I_{SYSVCC\_R\_FCC}$	SYSVCC (SBMD=0)	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	$I_{VCC\_R\_FCC}$	VCC/OSCVCC	400 MHz		25	120	140	mA
			320 MHz		25	120	140	mA
			240 MHz		25	120	140	mA
	$I_{ISOVDD\_R\_FCC}$	ISOVDD	400 MHz*7		1730	4000	4600	mA
			320 MHz*8		1410	3570	4170	mA
			240 MHz*9		1120	3140	3740	mA
Programming / Erasure of the flash memory U2B-FCC (U2B10 mode)	$I_{CC\_FPE\_FCC}$	VCC/OSCVCC			95	200	220	mA
Current during reset U2B-FCC (U2B10 mode)	$I_{SYSVCC\_RST\_FCC}$	SYSVCC(SBMD=0)		1	2.1	8	10	mA
	$I_{VCC\_RST\_FCC}$	VCC/OSCVCC		10	20	100	120	mA
	$I_{ISOVDD\_RST\_FCC}$	ISOVDD		300	780	2950	3550	mA
STOP mode current*6 U2B-FCC (U2B10 mode)	$I_{SYSVCC\_S\_FCC}$	SYSVCC(SBMD=0)			1.6	5	5	mA
	$I_{VCC\_S\_FCC}$	VCC			0.1	1	1	mA
	$I_{ISOVDD\_S\_FCC}$	ISOVDD			20	2000	2600	mA
	$I_{OSCVCC\_S\_FCC}$	OSCVCC			3.8	8	8	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.
Note 4. Tj = 150°C
Note 5. Tj = 160°C
Note 6. MainOSC is stopped.
Note 7. DFP frequency is 400 MHz.
Note 8. DFP frequency is 320 MHz.
Note 9. DFP frequency is 240 MHz.

Table 3.19 Current consumption for RH850/U2B6 (SYSVCC=VCC=3.0V～3.6V) *2, *3

Parameter	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.1*4	MAX.2*5	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	I_{VCC_R}	VCC/OSCVCC	400 MHz		15	75	80	mA
			320 MHz		15	75	80	mA
			240 MHz		15	75	80	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz		730	1200	1300	mA
			320 MHz		580	1050	1150	mA
			240 MHz		420	900	1000	mA
Programming / Erasure of the flash memory	I_{CC_FPE}	VCC/OSCVCC			100	155	160	mA
Current during reset	I_{SYSVCC_RST}	SYSVCC		1	2	6	8	mA
	I_{VCC_RST}	VCC/OSCVCC		5	10	55	60	mA
	I_{ISOVDD_RST}	ISOVDD		300	900	1000	1100	mA
STOP mode current*6	I_{SYSVCC_S}	SYSVCC			1.6	5	5	mA
	I_{VCC_S}	VCC			0.1	1	1	mA
	I_{ISOVDD_S}	ISOVDD			10	400	500	mA
	I_{OSCVCC_S}	OSCVCC			1	8	8	mA
RUN mode current U2B-FCC (U2B6 mode)	$I_{SYSVCC\_R\_FCC}$	SYSVCC (SBMD=0)	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	$I_{VCC\_R\_FCC}$	VCC/OSCVCC	400 MHz		25	120	140	mA
			320 MHz		25	120	140	mA
			240 MHz		25	120	140	mA
	$I_{ISOVDD\_R\_FCC}$	ISOVDD	400 MHz		920	2600	3000	mA
			320 MHz		720	2360	2760	mA
			240 MHz		530	2120	2520	mA
Programming / Erasure of the flash memory U2B-FCC (U2B6 mode)	$I_{CC\_FPE\_FCC}$	VCC/OSCVCC			95	200	220	mA
Current during reset U2B-FCC (U2B6 mode)	$I_{SYSVCC\_RST\_FCC}$	SYSVCC(SBMD=0)		1	2	6	8	mA
	$I_{VCC\_RST\_FCC}$	VCC/OSCVCC		10	20	100	120	mA
	$I_{ISOVDD\_RST\_FCC}$	ISOVDD		300	760	2400	2800	mA
STOP mode current*6 U2B-FCC (U2B6 mode)	$I_{SYSVCC\_S\_FCC}$	SYSVCC(SBMD=0)			1.6	5	5	mA
	$I_{VCC\_S\_FCC}$	VCC			0.1	1	1	mA
	$I_{ISOVDD\_S\_FCC}$	ISOVDD			20	1550	1950	mA
	$I_{OSCVCC\_S\_FCC}$	OSCVCC			3.8	8	8	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 3.3 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.
Note 4. Tj = 150°C
Note 5. Tj = 160°C
Note 6. MainOSC is stopped.

Table 3.20 Current consumption for RH850/U2B6 (SYSVCC=VCC=4.5V～5.5V) *2, *3

Parameter	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.1*4	MAX.2*5	Unit
RUN mode current	I_{SYSVCC_R}	SYSVCC	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	I_{VCC_R}	VCC/OSCVCC	400 MHz		15	75	80	mA
			320 MHz		15	75	80	mA
			240 MHz		15	75	80	mA
	I_{ISOVDD_R}	ISOVDD	400 MHz		730	1200	1300	mA
			320 MHz		580	1050	1150	mA
			240 MHz		420	900	1000	mA
Programming / Erasure of the flash memory	I_{CC_FPE}	VCC/OSCVCC			100	155	160	mA
Current during reset	I_{SYSVCC_RST}	SYSVCC		1	2	6	8	mA
	I_{VCC_RST}	VCC/OSCVCC		5	10	55	60	mA
	I_{ISOVDD_RST}	ISOVDD		300	900	1000	1100	mA
STOP mode current*6	I_{SYSVCC_S}	SYSVCC			1.6	5	5	mA
	I_{VCC_S}	VCC			0.1	1	1	mA
	I_{ISOVDD_S}	ISOVDD			10	400	500	mA
	I_{OSCVCC_S}	OSCVCC			1	8	8	mA
RUN mode current U2B-FCC (U2B6 mode)	$I_{SYSVCC\_R\_FCC}$	SYSVCC (SBMD=0)	400 MHz		0.7	5	5	mA
			320 MHz		0.7	5	5	mA
			240 MHz		0.7	5	5	mA
	$I_{VCC\_R\_FCC}$	VCC/OSCVCC	400 MHz		25	120	140	mA
			320 MHz		25	120	140	mA
			240 MHz		25	120	140	mA
	$I_{ISOVDD\_R\_FCC}$	ISOVDD	400 MHz		920	2600	3000	mA
			320 MHz		720	2360	2760	mA
			240 MHz		530	2120	2520	mA
Programming / Erasure of the flash memory U2B-FCC (U2B6 mode)	$I_{CC\_FPE\_FCC}$	VCC/OSCVCC			95	200	220	mA
Current during reset U2B-FCC (U2B6 mode)	$I_{SYSVCC\_RST\_FCC}$	SYSVCC(SBMD=0)		1	2	6	8	mA
	$I_{VCC\_RST\_FCC}$	VCC/OSCVCC		10	20	100	120	mA
	$I_{ISOVDD\_RST\_FCC}$	ISOVDD		300	760	2400	2800	mA
STOP mode current*6 U2B-FCC (U2B6 mode)	$I_{SYSVCC\_S\_FCC}$	SYSVCC(SBMD=0)			1.6	5	5	mA
	$I_{VCC\_S\_FCC}$	VCC			0.1	1	1	mA
	$I_{ISOVDD\_S\_FCC}$	ISOVDD			20	1550	1950	mA
	$I_{OSCVCC\_S\_FCC}$	OSCVCC			3.8	8	8	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- SYSVCC = VCC = EnVCC = LVDVCC = AnVCC = AnVREFH = SVRDRVCC = SVRAVCC = 5.0 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of SVR converter.

Note 3. The above value does not include the current of I/O buffer.
Note 4. Tj = 150°C
Note 5. Tj = 160°C
Note 6. MainOSC is stopped.

Table 3.21 Current consumption during Power-off standby (SYSVCC=VCC=3.0V~3.6V)

Parameter	Symbol	Power supply	MIN.	TYP.	MAX.	Unit	Tj
Power-off standby U2B10	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	7.5	mA	25°C < Tj ≤ 105°C
			-	-	8	mA	105°C < Tj ≤ 150°C
			-	-	10	mA	150°C < Tj ≤ 160°C
Power-off standby U2B6	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	5.5	mA	25°C < Tj ≤ 105°C
			-	-	6	mA	105°C < Tj ≤ 150°C
			-	-	8	mA	150°C < Tj ≤ 160°C
Power-off standby (SBMD = 0) U2B-FCC (U2B24 mode)	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	7.5	mA	25°C < Tj ≤ 105°C
			-	-	8	mA	105°C < Tj ≤ 150°C
Power-off standby (SBMD = 0) U2B-FCC (U2B10 mode)	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	7.5	mA	25°C < Tj ≤ 105°C
			-	-	8	mA	105°C < Tj ≤ 150°C
			-	-	10	mA	150°C < Tj ≤ 160°C
Power-off standby (SBMD = 0) U2B-FCC (U2B6 mode)	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	5.5	mA	25°C < Tj ≤ 105°C
			-	-	6	mA	105°C < Tj ≤ 150°C
			-	-	8	mA	150°C < Tj ≤ 160°C

Table 3.22 Current consumption during Power-off standby (SYSVCC=VCC=4.5V~5.5V)

Parameter	Symbol	Power supply	MIN.	TYP.	MAX.	Unit	Tj
Power-off standby U2B10	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	7.5	mA	25°C < Tj ≤ 105°C
			-	-	8	mA	105°C < Tj ≤ 150°C
			-	-	10	mA	150°C < Tj ≤ 160°C
Power-off standby U2B6	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	5.5	mA	25°C < Tj ≤ 105°C
			-	-	6	mA	105°C < Tj ≤ 150°C
			-	-	8	mA	150°C < Tj ≤ 160°C
Power-off standby (SBMD = 0) U2B-FCC (U2B24 mode)	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	7.5	mA	25°C < Tj ≤ 105°C
			-	-	8	mA	105°C < Tj ≤ 150°C
Power-off standby (SBMD = 0) U2B-FCC (U2B10 mode)	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	7.5	mA	25°C < Tj ≤ 105°C
			-	-	8	mA	105°C < Tj ≤ 150°C
			-	-	10	mA	150°C < Tj ≤ 160°C
Power-off standby (SBMD = 0) U2B-FCC (U2B6 mode)	I_{SB}	SYSVCC	-	-	0.7	mA	-40°C < Tj ≤ 25°C
			-	-	5.5	mA	25°C < Tj ≤ 105°C
			-	-	6	mA	105°C < Tj ≤ 150°C
			-	-	8	mA	150°C < Tj ≤ 160°C

Table 3.23 Current consumption for RH850/U2B (FCC chip only)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
EMUVCC	I_{EMUVCC_FCC}	Current of EMUVCC	-	11	50	55	mA
EMUVDD	I_{EMUVDD_FCC}	Current of EMUVDD	-	180	600	700	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

3.2.10.3 Power Supply Currents for specific features

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.24 Current consumption for specific features (SYSVCC=VCC=3.0V～3.6V) *1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*2	MAX.2*3	Unit
SVR converter	I_{SVR_SYSVCC}	Current of SYSVCC	-	1	5.5	7	mA
	$I_{SVR\_SVRAVCC}$	Current of SVRAVCC	-	5	18	23	mA
LVDS for RHSIF	I_{LVDS}	Current of LVDVCC	-	9	20	25	mA / ch
LVDS for RHSB (0ch, 3ch)	I_{LVDS}	Current of LVDVCC	-	10	25	30	mA / ch
LVDS for RHSB (1ch, 2ch)	I_{LVDS}	Current of EnVCC	-	8	17	20	mA / ch
LVDS for MSPI	I_{LVDS}	Current of EnVCC	-	10	20	25	mA / ch
RHSIF for Debug	I_{DEBUG}	Current of JnVCC	-	9	30	35	mA
Gigabit Ethernet	I_{GBETH}	Current of GETH0BVCC, and GETH0PVCC	-	45	90	90	mA / ch

Note 1. This table shows additional current when the specific function indicated above is used.
Note 2. Tj = 150°C
Note 3. Tj = 160°C

Table 3.25 Current consumption for specific features (SYSVCC=VCC=4.5V～5.5V) *1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*2	MAX.2*3	Unit
SVR converter	I_{SVR_SYSVCC}	Current of SYSVCC	-	1	5.5	7	mA
	$I_{SVR\_SVRAVCC}$	Current of SVRAVCC	-	5	18	23	mA
LVDS for RHSIF	I_{LVDS}	Current of LVDVCC	-	9	20	25	mA / ch
LVDS for RHSB (0ch, 3ch)	I_{LVDS}	Current of LVDVCC	-	10	25	30	mA / ch
LVDS for RHSB (1ch, 2ch)	I_{LVDS}	Current of EnVCC	-	8	17	20	mA / ch
LVDS for MSPI	I_{LVDS}	Current of EnVCC	-	10	20	25	mA / ch
RHSIF for Debug	I_{DEBUG}	Current of JnVCC	-	9	30	35	mA
Gigabit Ethernet	I_{GBETH}	Current of GETH0BVCC, and GETH0PVCC	-	45	90	90	mA / ch

Note 1. This table shows additional current when the specific function indicated above is used.
Note 2. Tj = 150°C
Note 3. Tj = 160°C

Table 3.26 3V Analog power/reference current (U2B24)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
ADCK0 U2B-FCC (U2B24 mode)	I_{ADC0_FCC}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF\_FCC}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1 U2B-FCC (U2B24 mode)	I_{ADC1_FCC}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF\_FCC}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2 U2B-FCC (U2B24 mode)	I_{ADC2_FCC}	Current of A2VCC	-	1.4	2.8	2.8	mA
	$I_{ADC2REF\_FCC}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
ADCK3, ADCKA U2B-FCC (U2B24 mode)	I_{ADC3_FCC}	Current of A3VCC (ADCK3 used)	-	1.4	2.8	2.8	mA
		Current of A3VCC (ADCKA used)	-	1.4	2.8	2.8	mA
	$I_{ADC3REF\_FCC}$	Current of A3VREFH (ADCK3 used)	-	0.1	0.2	0.2	mA
		Current of A3VREFH (ADCKA used)	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC U2B-FCC (U2B24 mode)	I_{ADS_FCC}	Current of ADSVCC	-	-	-	-	mA
	I_{ADSREF_FCC}	Current of ADSVREFH	-	-	-	-	mA
Fast Comparator U2B-FCC (U2B24 mode)	I_{AFCVCC_FCC}	Current of AFCVCC	-	4	12	13	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

Table 3.27 5V Analog power/reference current (U2B24)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
ADCK0 U2B-FCC (U2B24 mode)	I_{ADC0_FCC}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF\_FCC}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1 U2B-FCC (U2B24 mode)	I_{ADC1_FCC}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF\_FCC}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2 U2B-FCC (U2B24 mode)	I_{ADC2_FCC}	Current of A2VCC	-	1.4	2.8	2.8	mA
	$I_{ADC2REF\_FCC}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
ADCK3, ADCKA U2B-FCC (U2B24 mode)	I_{ADC3_FCC}	Current of A3VCC (ADCK3 used)	-	1.4	2.8	2.8	mA
		Current of A3VCC (ADCKA used)	-	1.4	2.8	2.8	mA
	$I_{ADC3REF\_FCC}$	Current of A3VREFH (ADCK3 used)	-	0.1	0.2	0.2	mA
		Current of A3VREFH (ADCKA used)	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC U2B-FCC (U2B24 mode)	I_{ADS_FCC}	Current of ADSVCC	-	21	35	37	mA
	I_{ADSREF_FCC}	Current of ADSVREFH	-	0.7	1.5	1.6	mA
Fast Comparator U2B-FCC (U2B24 mode)	I_{AFCVCC_FCC}	Current of AFCVCC	-	4	12	13	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

Table 3.28 3V Analog power/reference current (U2B10)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
ADCK0	I_{ADC0}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1	I_{ADC1}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2	I_{ADC2}	Current of A2VCC	-	1.4	2.8	2.8	mA
	$I_{ADC2REF}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
ADCK3	I_{ADC3}	Current of A3VCC	-	1.4	2.8	2.8	mA
	$I_{ADC3REF}$	Current of A3VREFH	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC	I_{ADS}	Current of ADSVCC	-	-	-	-	mA
	I_{ADSREF}	Current of ADSVREFH	-	-	-	-	mA
Fast Comparator	I_{AFCVCC}	Current of AFCVCC	-	1.5	6	6.5	mA
ADCK0 U2B-FCC (U2B10 mode)	I_{ADC0_FCC}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF\_FCC}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1 U2B-FCC (U2B10 mode)	I_{ADC1_FCC}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF\_FCC}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2 U2B-FCC (U2B10 mode)	I_{ADC2_FCC}	Current of A2VCC	-	1.4	2.8	2.8	mA
	$I_{ADC2REF\_FCC}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
ADCK3 U2B-FCC (U2B10 mode)	I_{ADC3_FCC}	Current of A3VCC	-	1.4	2.8	2.8	mA
	$I_{ADC3REF\_FCC}$	Current of A3VREFH	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC U2B-FCC (U2B10 mode)	I_{ADS_FCC}	Current of ADSVCC	-	-	-	-	mA
	I_{ADSREF_FCC}	Current of ADSVREFH	-	-	-	-	mA
Fast Comparator U2B-FCC (U2B10 mode)	I_{AFCVCC_FCC}	Current of AFCVCC	-	1.5	6	6.5	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

Table 3.29 5V Analog power/reference current (U2B10)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
ADCK0	I_{ADC0}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1	I_{ADC1}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2	I_{ADC2}	Current of A2VCC	-	1.4	2.8	2.8	mA
	$I_{ADC2REF}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
ADCK3	I_{ADC3}	Current of A3VCC	-	1.4	2.8	2.8	mA
	$I_{ADC3REF}$	Current of A3VREFH	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC	I_{ADS}	Current of ADSVCC	-	21	32	34	mA
	I_{ADSREF}	Current of ADSVREFH	-	0.7	1.2	1.3	mA
Fast Comparator	I_{AFCVCC}	Current of AFCVCC	-	1.5	6	6.5	mA
ADCK0 U2B-FCC (U2B10 mode)	I_{ADC0_FCC}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF\_FCC}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1 U2B-FCC (U2B10 mode)	I_{ADC1_FCC}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF\_FCC}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2 U2B-FCC (U2B10 mode)	I_{ADC2_FCC}	Current of A2VCC	-	1.4	2.8	2.8	mA
	$I_{ADC2REF\_FCC}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
ADCK3 U2B-FCC (U2B10 mode)	I_{ADC3_FCC}	Current of A3VCC	-	1.4	2.8	2.8	mA
	$I_{ADC3REF\_FCC}$	Current of A3VREFH	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC U2B-FCC (U2B10 mode)	I_{ADS_FCC}	Current of ADSVCC	-	21	35	37	mA
	I_{ADSREF_FCC}	Current of ADSVREFH	-	0.7	1.5	1.6	mA
Fast Comparator U2B-FCC (U2B10 mode)	I_{AFCVCC_FCC}	Current of AFCVCC	-	1.5	6	6.5	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

Table 3.30 3V Analog power/reference current (U2B6)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
ADCK0	I_{ADC0}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1	I_{ADC1}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2	I_{ADC2}	Current of A2VCC 4ch T&H function is used	-	4	7.6	7.6	mA
	$I_{ADC2REF}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
DS-ADC	I_{ADS}	Current of ADSVCC	-	-	-	-	mA
	I_{ADSREF}	Current of ADSVREFH	-	-	-	-	mA
Fast Comparator,RD Comverter	I_{AFCVCC}	Current of AFCVCC (RDC3AL is used)	-	5	15	16	mA
		Current of AFCVCC (FCMP is used)	-	1.5	6	6.5	
ADCK0 U2B-FCC (U2B6 mode)	I_{ADC0_FCC}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF\_FCC}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1 U2B-FCC (U2B6 mode)	I_{ADC1_FCC}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF\_FCC}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2 U2B-FCC (U2B6 mode)	I_{ADC2_FCC}	Current of A2VCC 4ch T&H function is used	-	4	7.6	7.6	mA
	$I_{ADC2REF\_FCC}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
DS-ADC/Cyclic-ADC U2B-FCC (U2B6 mode)	I_{ADS_FCC}	Current of ADSVCC	-	-	-	-	mA
	I_{ADSREF_FCC}	Current of ADSVREFH	-	-	-	-	mA
Fast Comparator,RD Comverter U2B-FCC (U2B6 mode)	I_{AFCVCC_FCC}	Current of AFCVCC (RDC3AL is used)	-	5	15	16	mA
		Current of AFCVCC (FCMP is used)	-	1.5	6	6.5	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

Table 3.31 5V Analog power/reference current (U2B6)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.1*1	MAX.2*2	Unit
ADCK0	I_{ADC0}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1	I_{ADC1}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2	I_{ADC2}	Current of A2VCC 4ch T&H function is used	-	4	7.6	7.6	mA
	$I_{ADC2REF}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
DS-ADC	I_{ADS}	Current of ADSVCC	-	6.5	11	12	mA
	I_{ADSREF}	Current of ADSVREFH	-	0.25	0.45	0.5	mA
Fast Comparator,RD Comverter	I_{AFCVCC}	Current of AFCVCC (RDC3AL is used)	-	5	15	16	mA
		Current of AFCVCC (FCMP is used)	-	1.5	6	6.5	
ADCK0 U2B-FCC (U2B6 mode)	I_{ADC0_FCC}	Current of A0VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC0REF\_FCC}$	Current of A0VREFH	-	0.1	0.2	0.2	mA
ADCK1 U2B-FCC (U2B6 mode)	I_{ADC1_FCC}	Current of A1VCC 6ch T&H function is used	-	5.5	10.2	10.2	mA
	$I_{ADC1REF\_FCC}$	Current of A1VREFH	-	0.1	0.2	0.2	mA
ADCK2 U2B-FCC (U2B6 mode)	I_{ADC2_FCC}	Current of A2VCC 4ch T&H function is used	-	4	7.6	7.6	mA
	$I_{ADC2REF\_FCC}$	Current of A2VREFH	-	0.1	0.2	0.2	mA
DS-ADC U2B-FCC (U2B6 mode)	I_{ADS_FCC}	Current of ADSVCC	-	7	12.5	13.5	mA
	I_{ADSREF_FCC}	Current of ADSVREFH	-	0.3	0.6	0.65	mA
Fast Comparator,RD Comverter U2B-FCC (U2B6 mode)	I_{AFCVCC_FCC}	Current of AFCVCC (RDC3AL is used)	-	5	15	16	mA
		Current of AFCVCC (FCMP is used)	-	1.5	6	6.5	mA

Note 1. Tj = 150°C

Note 2. Tj = 160°C

3.2.11 Voltage Detector (POC) Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.32 Voltage Detector (POC) Characteristics*1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage (SYSVCC)	V_{POC}		2.5	2.63	2.75	V
Response time	t_{DPOC1}	Rise			1.2	ms
	t_{DPOC2}	Fall			10	µs
SYSVCC minimum pulse width	t_{WPOC}		0.5			ms
SYSVCC voltage ramp	t_{SYSVS}		0.002		550	ms/V

Note 1. POC monitors SYSVCC supply voltage.

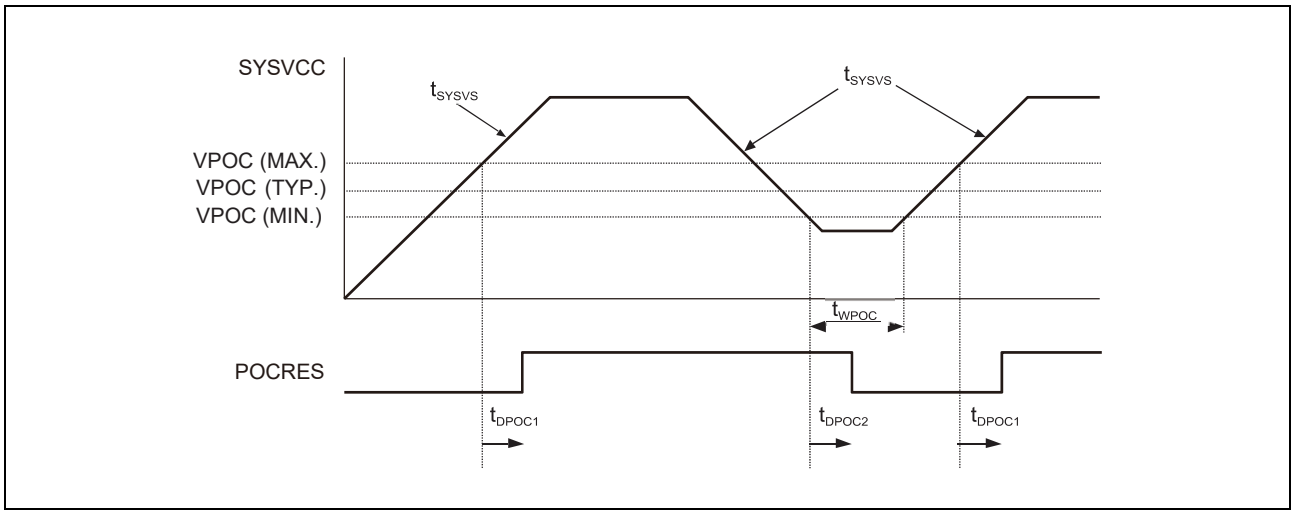


Figure 3.8 POC Characteristic

3.2.12 Primary Detection of Voltage Monitor (VMON) Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.33 VMON Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VDD primary high detection level	V_{VDDMAH}	AWOVDD/ ISOVDD2	1.155	1.17	1.205	V
	V_{VDDMIH}	ISOVDD	1.155	1.17	1.205	V
VDD primary low detection level	V_{VDDMAL}	AWOVDD/ ISOVDD2	0.975	1.01	1.025	V
	V_{VDDMIL}	Assisted by the Delay Monitor (DMON)	0.985	1.01	1.025	
VCC primary high detection level	V_{VCCMH}		5.5	5.64	5.8	V
VCC primary low detection level	V_{VCCML}		2.8	2.9	3	V
E0VCC primary high detection level	V_{EVCCMH}		5.5	5.64	5.8	V
E0VCC primary low detection level	V_{EVCCML}		2.8	2.9	3	V
$\overline{\text{VMONOUT}}$ delay time	t_{DVMON}				10+Filter time*1	µs
VMON minimum pulse width	t_{WVMON}		0.2			ms
Voltage ramp	t_{VS}		0.002		550	ms/V

Note 1. See RH850/U2B Group User's Manual:Hardware **Section 13.3.6, Registers** for detail specification of filter time.

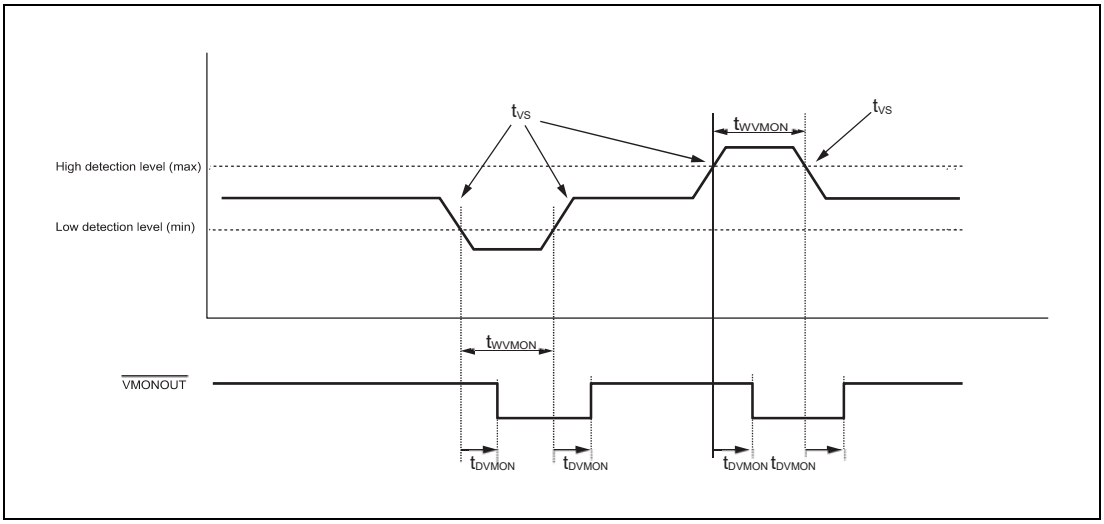


Figure 3.9 VMON Characteristics

3.2.13 SGMII Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.34 SGMII REFCK Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.0		GETH0BVCC + 0.3	V
Low level input voltage	V_{IL}		–0.3		0.8	V

Table 3.35 SGMII Tx Buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V_{OH}				1525	mV
Output voltage low	V_{OL}		875			mV
Output Differential Voltage	$\|V_{OD}\|$		150		400	mV
Output Offset Voltage	V_{OS}		1075		1325	mV
Change in V_{OD} between “0” and “1”	$\Delta\|V_{OD}\|$				25	mV
Change in V_{OS} between “0” and “1”	ΔV_{OS}				25	mV
Output current on Short to GND	I_{sa}, I_{sb}				40	mA
Output current when a, b are shorted	I_{sab}				12	mA

Note 1. For a detailed description of the symbols, please refer to the IEEE1596.3-1996 standard.
Note 2. All parameters measured at Rload = 100 Ω ±1 % load

Table 3.36 SGMII Rx Buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage range a or b	V_I		675		1725	mV
Input differential threshold	V_{idth}		–50		50	mV
Receiver differential input impedance	R_{in}		80		120	Ω

Note 1. For a detailed description of the symbols please refer to the IEEE1596.3-1996 standard.

3.2.14 Aurora Interface Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.37 Aurora Interface Clock Characteristics (CICREFP, CICREFN)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential input voltage	$V_{DIFFCIC}$ *1		200		1600	mV
External AC coupling capacitor	C_{ACC}		75	100	200	nF
Differential input resistance	$Z_{DIFFCIC}$		70	100	130	Ω

Note 1. Peak to peak differential input voltage.

Table 3.38 Aurora Interface Characteristics (TODP0-3/TODN0-3)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential output voltage	$V_{DIFFTOD}$ *1		800		1600	mV
Differential output resistance	$Z_{DIFFTOD}$		70		130	Ω

Note 1. Peak to peak differential input voltage.

3.2.15 Regulator Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.39 Regulator Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	V_{AWOVCL}	AWOVCL pin	1.025	1.09	1.155	V
	$V_{GETH0VCL}$	GETH0VCL pin	1.025	1.09	1.155	V
	$V_{GETH1VCL}$	GETH1VCL pin	1.025	1.09	1.155	V
	V_{RAMVCL}	RAMSVCL pin	1.025	1.09	1.155	V
Capacitance	C_{AWOVCL}	AWOVCL pin	0.140	0.2	0.286	µF
	$C_{GETH0VCL}$	GETH0VCL pin	0.154	0.22	0.286	µF
	$C_{GETH1VCL}$	GETH1VCL pin	0.154	0.22	0.286	µF
	C_{RAMVCL}	RAMSVCL pin	0.140	0.2	0.286	µF
Equivalent series resistance for load capacitance	R_{VRAWO}	for C_{AWOVCL}			40*1	mΩ
	$R_{VRGETH0}$	for $C_{GETH0VCL}$			40*1	mΩ
	$R_{VRGETH1}$	for $C_{GETH1VCL}$			40*1	mΩ
	R_{RAMVCL}	RAMSVCL pin			40*1	mΩ
Inrush current during power-on U2B-EVA U2B-FCC (U2B24 mode)	$I_{RUSYSVCC}$	SYSVCC*2			400*1*3	mA
	$I_{RUOSCVCC}$	OSCVCC*2			400*1*3	mA
	$I_{RUJ0VCC}$	J0VCC*2			400*1*3	mA
	$I_{RUGETH0PVCC}$	GETH0PVCC	-	-	300*1	mA
Inrush current during power-on U2B-FCC (U2B10 mode) U2B-FCC (U2B6 mode)	$I_{RUSYSVCC}$	SYSVCC*4			400*1*3	mA
Inrush current during power-on U2B10	$I_{RUSYSVCC}$	SYSVCC*4			400*1*3	mA
Inrush current during power-on U2B6	$I_{RUSYSVCC}$	SYSVCC*4			400*1*3	mA

Note 1. This is reference value.
Note 2. When returning from Power Off Standby or DeepSTOP.
Note 3. The time of current flow is less than 2.5 µs.
Note 4. When returning from Power Off Standby.

Table 3.40 Switching Voltage Regulator Characteristics (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	VDD		1.025	1.09	1.155	V
Switching frequency	f_{SVRSW}	SVRFSWMODE[1:0] = 00_B	432	465	497	kHz
		SVRFSWMODE[1:0] = 01_B	865	930	995	kHz
		SVRFSWMODE[1:0] = 10_B	1318	1417	1516	kHz
		SVRFSWMODE[1:0] = 11_B	1956	2103	2250	kHz
Modulation frequency*11	f_{SVRmod}	SVRFSWMODE[1:0] = 00	0.86(=432/500)		7.96(=497/62.5)	kHz
		SVRFSWMODE[1:0] = 01	1.73(=865/500)		15.92(=995/62.5)	kHz
		SVRFSWMODE[1:0] = 10	2.64(=1318/500)		24.25(=1516/62.5)	kHz
		SVRFSWMODE[1:0] = 11	3.91(=1956/500)		35.95(=2250/62.5)	kHz
Frequency dithering range *6	f_{SVRdit}	SVRAJSSCGD[1:0] = 00_B SVRFSWMODE[1:0] = 00_B/01_B/10_B			5	%
		SVRAJSSCGD[1:0] = 01_B SVRFSWMODE[1:0] = 00_B/01_B/10_B			9	%
		SVRAJSSCGD[1:0] = 00_B SVRFSWMODE[1:0] = 11_B			6	%
SVR load transient response		Less than ΔI (max)	–38*1		38*1	mV
SVR efficiency		SVRFSWMODE[1:0] = 00_B		80*1		%
		SVRFSWMODE[1:0] = 01_B		70*1		%
		SVRFSWMODE[1:0] = 10_B		70*1		%
		SVRFSWMODE[1:0] = 11_B		70*1		%
Capacitance*2	$C_{SVRDRVCC}$	SVRDRVCC pin		*2		μF
	$C_{SVRAVCC}$	SVRAVCC pin		*2		μF
	C_{VDD0}	VDD pin. Close to LX		*2		μF
Equivalent series resistance for load capacitance*2	$R_{VRSVRDRVCC}$	for $C_{SVRDRVCC}$ (@0.1MHz to 5MHz)			10	mΩ
	$R_{VRSVRAVCC}$	for $C_{SVRAVCC}$ (@0.1MHz to 5MHz)			10	mΩ
	R_{VRVDD}	for C_{VDD0} (@0.1MHz to 5MHz)			10	mΩ
Inductance*2	LX	Close to external MOSFETs		*2		μH
DC resistance for inductance*2	R_{LX}	for LX			40*10	mΩ

Table 3.40 Switching Voltage Regulator Characteristics (2/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating current valiation	ΔI	I_{ISOVDD_R}, U2B10	-	-	600*7	mA/ 100us
		I_{ISOVDD_R}, U2B6	-	-	350*8	
		I_{ISOVDD_R}, U2B24FCC	-	-	600*9	
		I_{ISOVDD_R}, U2B10FCC	-	-	600*9	
		I_{ISOVDD_R}, U2B6FCC	-	-	600*9	
Ramp-up time with soft start	t_{RUT}				3.8	ms

Note 1. This is reference value.

Note 2. See the application note separately issued.

Note 3. The total capacitance for the device has to be distributed around thermal ball.

Note 4. Operating current variation filtered by simple moving average of 20 µs window can be ignored.

Note 5. Operating current variation with smaller than 1 mA/µs slope is not necessary to be counted as “ΔI”.

Note 6. Dithered frequency mode is only supported in down spread mode.

Note 7. 47 uF x 4 and 4.7 uH @f_{SVRSW} = 465 kHz
47 uF x 2, 22 uF x 1, and 2.2 uH @f_{SVRSW} = 930 kHz, SVRDRVCC, SYSVCC, SVRAVCC = 3.0-3.6 V
47 uF x 3 and 2.2 uH @f_{SVRSW} = 930 kHz, SVRDRVCC, SYSVCC, SVRAVCC = 4.5-5.5V
22 uF x 4 and 1.5 uH @f_{SVRSW} = 1420 kHz
22 uF x 3 and 1.0 uH @f_{SVRSW} = 2100 kHz

Note 8. 47 uF x 2, 22 uF x 1, and 4.7 uH @f_{SVRSW} = 465 kHz
22 uF x 4 and 2.2 uH @f_{SVRSW} = 930 kHz
22 uF x 3 and 1.5 uH @f_{SVRSW} = 1420 kHz
22 uF x 3 and 1.0 uH @f_{SVRSW} = 2100 kHz

Note 9. 47 uF x 4 and 4.7 uH @f_{SVRSW} = 465 kHz
47 uF x 2, 22 uF x 1, and 2.2 uH @f_{SVRSW} = 930 kHz
22 uF x 4 and 1.5 uH @f_{SVRSW} = 1420 kHz
22 uF x 3 and 1.0 uH @f_{SVRSW} = 2100 kHz

Note 10. Contact our sale office for the method of setting parameters.

Note 11. Dose not include frequency dithering range.

3.3 AC Characteristics

3.3.1 AC Characteristic Measurement Condition

3.3.1.1 General Conditions

Below conditions are valid for all subsequent timing specifications if not noted otherwise:

- See **Section 3.2.1, Operational Conditions**.
- Drive strength = 3 (Medium)
- CL = 30 pF
- All bits of PINVn/JPINV0 are set as 0.
- All bits of PODCn/JPODC0 are set as 0 except for specification on RIIC timing.

NOTE

Even though AC characteristics correspond to the nominal frequency, a main oscillator tolerance of up to 1000 ppm is considered with regard to timing characteristics for communication modules.

The AC characteristics are specified on the assumption that each pin is used at the same EnVCC voltage.

3.3.1.2 Input Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

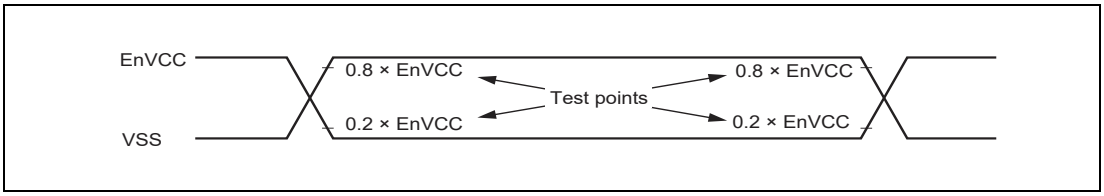


Figure 3.10 AC Input Measurement Points

3.3.1.3 Output Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

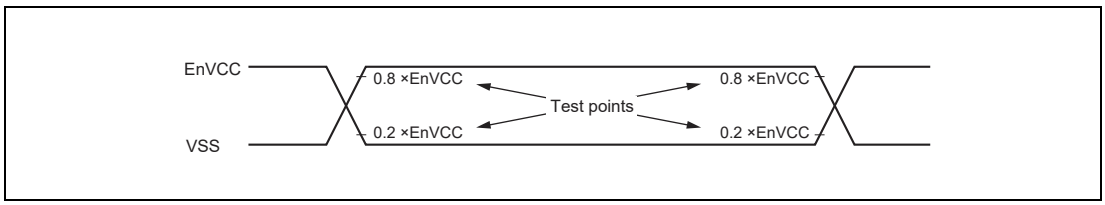


Figure 3.11 AC Output Measurement Points

3.3.1.4 Load conditions

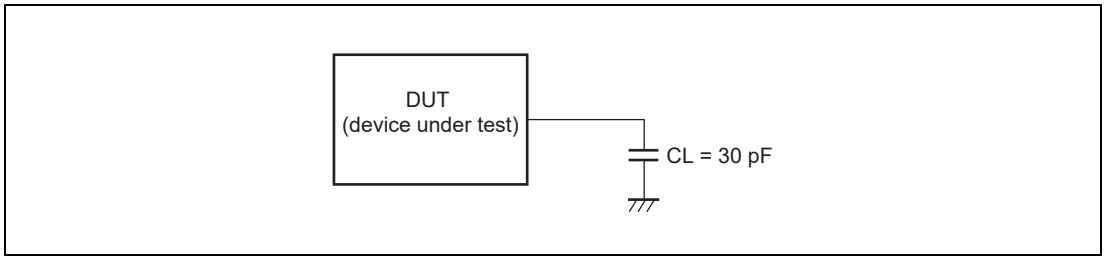


Figure 3.12 AC Load Conditions

3.3.2 Power On/Off Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.41 Power On/Off Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power wait time at power-on[*7] [U2B-EVA/U2B-FCC Only]	t_{WAIT}	Power-up SVR is not used	0.7			ms
Reset hold time at power-on	t_{RESH1}	Power-up[*1] SVR is used	1.3 + t_{RUT}			ms
		Power-up[*1] SVR is not used	1.3			ms
Power hold time at reset assertion[*5]	t_{PWH}	Power-down[*2]	2			µs
Operation mode low level hold time at power-on	t_{MDL}	SVR is used	0.1 + t_{RUT}			ms
		SVR is not used	0.1			ms
Operating mode setup time at power-on	t_{MDS1}		1			ms
Operating mode setup time at reset assert	t_{MDS2}		1			ms
Operating mode hold time at reset negate	t_{MDH1}		1			ms
Operating mode hold time at power-off	t_{MDH2}		0			µs
$\overline{TRST}$ setup time at reset	t_{TRMDS}		2			µs
$\overline{TRST}$ hold time at reset negate[*4]	t_{TRMDH}		30			ms
$\overline{TRST}$ hold time at power-on	t_{TRSTH1}	SVR is used	1.29 + t_{RUT}			ms
		SVR is not used	1.29			ms
$\overline{TRST}$ hold time at power-off	t_{TRSTH3}	Time since SYSVCC and VDD were power-off.			10	µs
Oscillator stabilization time	t_{OSC}				5.5	ms
PLL lock in time	t_{PLLL}	[*3]			1	ms

Note 1. t_{RESH1} is the reset time required for the supply of internal clock signals to become stable after all power supplies are turned on. There are no restrictions on the rising order of each power supply.
However, if rising of ISOVDD before rising of SYSVCC, leakage current from ISOVDD to SYSVCC may occur while ramp-up.

Note 2. t_{PWH2} is the time from assertion of the reset signal until any of the power voltages have dropped below the lower-limit voltages.
There are no restrictions on the falling order of each power supply.
However, if falling of SYSVCC before falling of ISOVDD, leakage current from ISOVDD to SYSVCC may occur while ramp- down.

Note 3. t_{PLLL} is the time required for PLL to lock in after MOSC oscillation has become stable.

Note 4. Access by the Nexus, LPD and BSCAN during t_{TRMDH} duration is prohibited (both of High and low condition of $\overline{TRST}$).

Note 5. The device can withstand up to 1000 uncontrolled power down cycles without impact on lifetime.
Uncontrolled means not according to power down timing requirements.

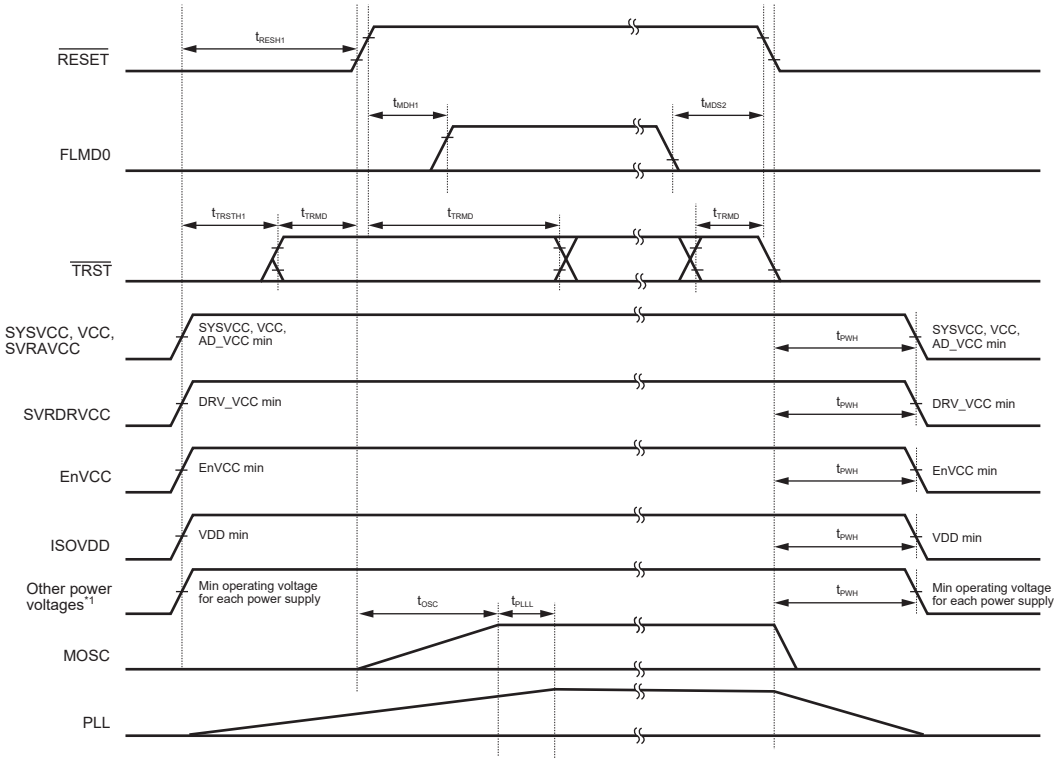
Note 6. Objection of power supplies for tRESH1, tTRSTH1 and tMDL is changed by power configuration.
When SVR is used: All power supplies except for ISOVDD
When SVR is not used: All power supplies

Note 7. Power wait time at power-on (t_{WAIT}) is required from the following power supply voltages exceed 2.75V to ISOVDD power supply voltage reaches 0.99V.
U2B-EVA/U2B24-FCC, U2B10-FCC/U2B6-FCC: SYSVCC, VCC, SVRAVCC
U2B-EVA/U2B24-FCC: SYSVCC, SVRAVCC
There are no restrictions on the rising order of the following power supply.
- EnVCC
- Other power voltages
Supply voltage to SVRDRVCC on condition specified in the **Section 3.2.1, Operational Conditions**.

U2B-EVA/U2B24-FCC, U2B10-FCC/U2B6-FCC: SVRDRVCC ≥ SYSVCC = SVRAVCC = VCC
U2B-EVA/U2B24-FCC: SVRDRVCC ≥ SYSVCC = SVRAVCC
The ramp up of SYSVCC, VCC, SVRAVCC, SVRDRVCC must be within the range of SYSVCC voltage ramp (t_{SYSVS}) specified in the **Section 3.2.11, Voltage Detector (POC) Characteristics**.

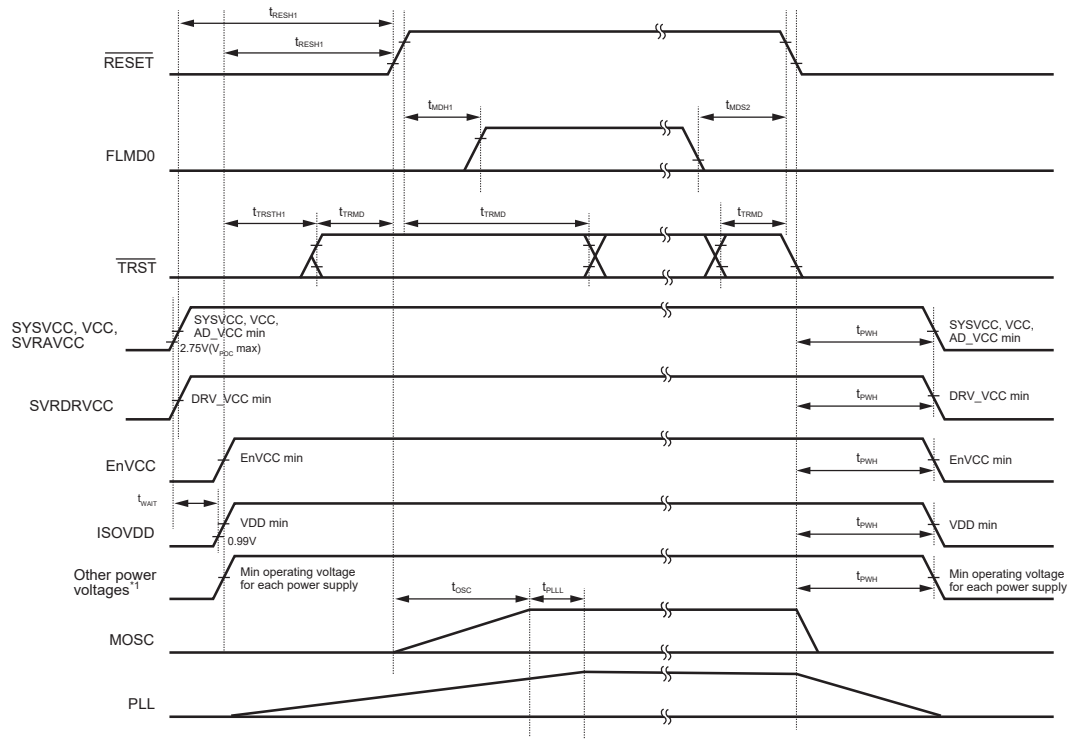
CAUTION

The states of I/O pins are not reset during the noise cancellation interval of the reset signal following its assertion while power is being turned off. During that time, do not allow any input of mid-range potential to the pin or contention of output data.



Note 1. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1 kΩ or more pull-down resistance.

Figure 3.13 Power On/Off Timings (Normal operating mode and User boot mode 0) [For U2B10/U2B6]

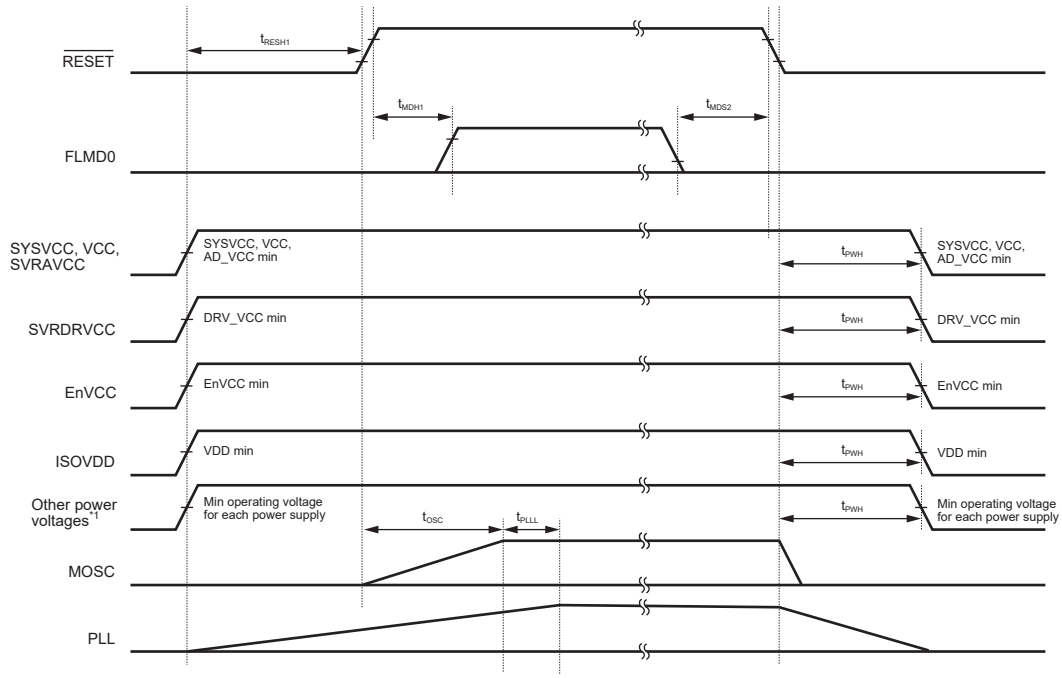


Note 1. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1 kΩ or more pull-down resistance.

Figure 3.14 Power On/Off Timings (Normal operating mode and User boot mode 0) [For U2B-EVA/U2B-FCC]

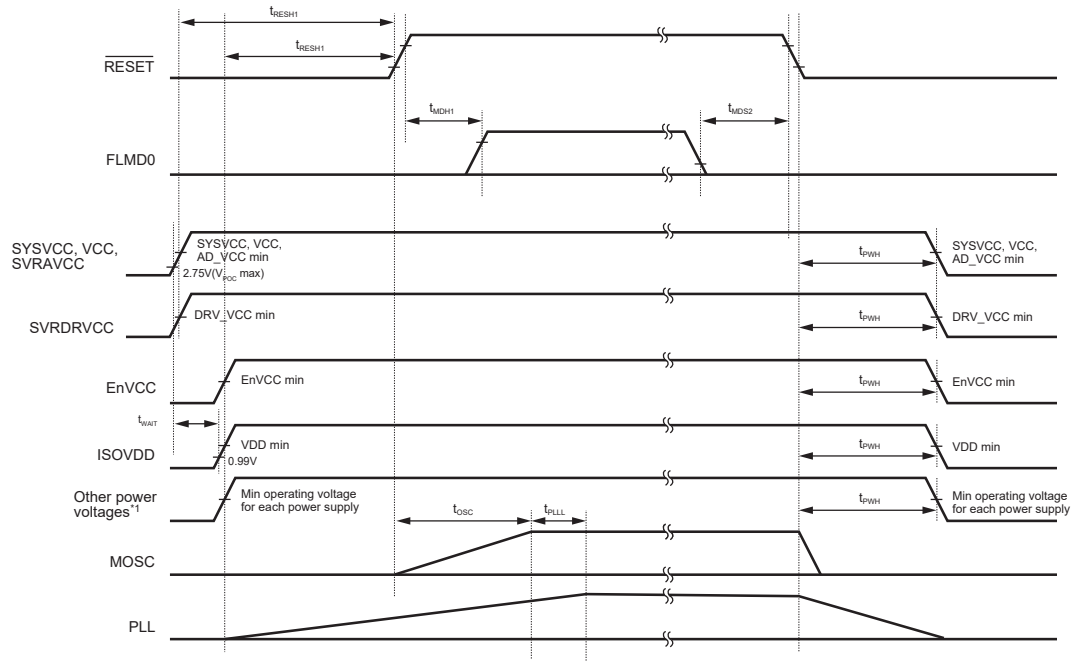
NOTE

For the $\overline{\text{AURORES}}$ timing, see **Section 3.3.28, Debug Reset Timing**.



Note 1. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1 kΩ or more pull-down resistance.

Figure 3.15 Power On/Off Timings (Serial programming mode 0) [For U2B10/U2B6]

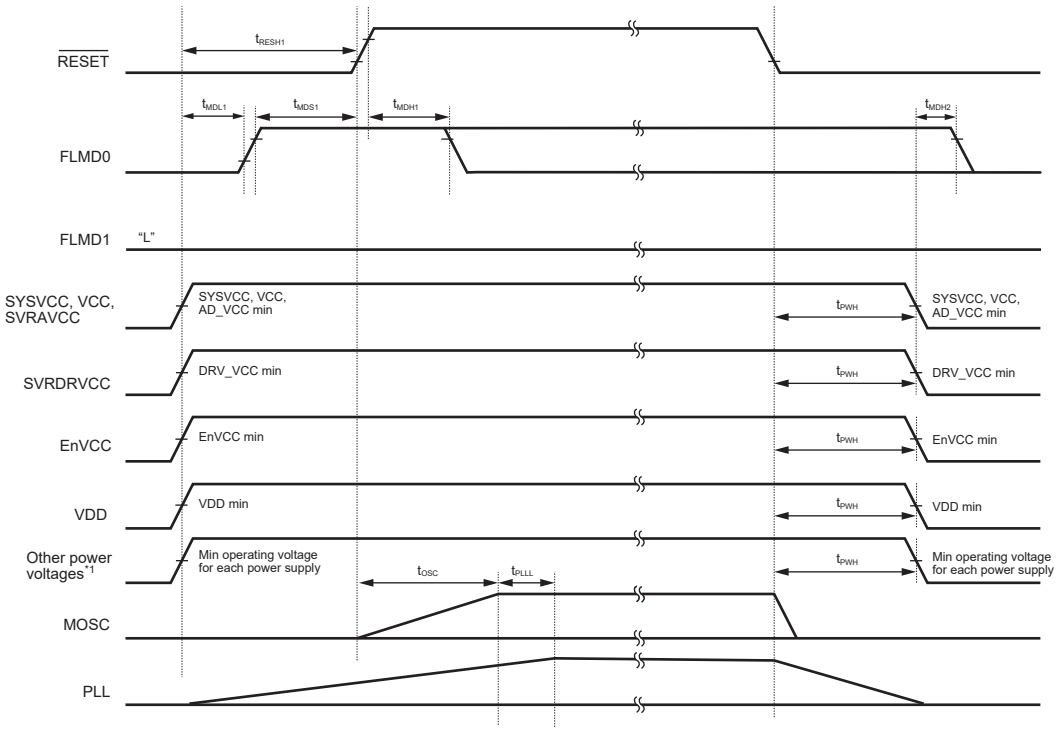


Note 1. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1 kΩ or more pull-down resistance.

Figure 3.16 Power On/Off Timings (Serial programming mode 0) [For U2B-EVA/U2B-FCC]

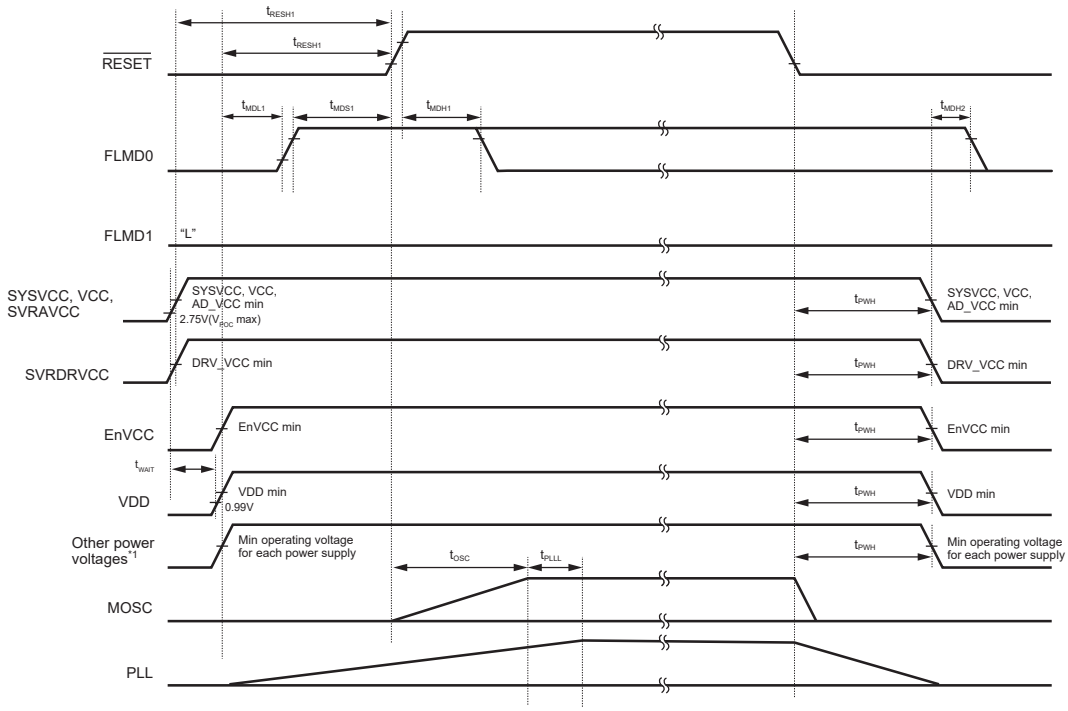
NOTE

For the $\overline{\text{AURORES}}$ timing, see **Section 3.3.28, Debug Reset Timing**.



Note 1. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1 kΩ or more pull-down resistance.

Figure 3.17 Power On/Off Timings (Serial programming mode 1) [For U2B10/U2B6]



Note 1. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1 kΩ or more pull-down resistance.

Figure 3.18 Power On/Off Timings (Serial programming mode 1) [For U2B-EVA/U2B-FCC]

NOTE

For the $\overline{\text{AURORES}}$ timing, see **Section 3.3.28, Debug Reset Timing**.

3.3.2.1 Power Up Sequencing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**

Table 3.42 Power Up Sequencing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Runtime from release of $\overline{\text{RESET}}$ to start of instruction fetch					2.4 + t_{BIST}	ms

Note 1. t_{BIST} means BIST run time. Refer to RH850/U2B Group User's Manual:Hardware **Table 55.626, BIST scenario selection at the next System Reset 2** on **Section 55.6.2.39, BSEQ0SEL — BIST Scenario Select Register** for details. Note that the given BIST run time is the typical value and the tolerance of the corresponding clock needs to be taken into account for the maximum value.

3.3.3 Standby Transition/Return Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**

Table 3.43 DeepSTOP Transition/Return Timing In case of VDD External Supply (SBMD=1)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Wake-up trigger to PWRCTL delay time	$t_{DPWRCTL}$				300	µs
VDD hold time	t_{HDD}		0			µs
VDD power-on start time	t_{PDD}		0			µs

Table 3.44 Power-Off StandbyTiming (SBMD=0)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset hold time at return from power-off standby mode time	t_{RESH2}	-	t_{RESH1}	-	ms
$\overline{TRST}$ hold time at return from power-off standby mode	t_{TRSTH2}	-	t_{TRSTH1}	-	ms
voltage at transition to power-off standby mode*1	Vstdby1	-	2.6	-	V
SYSVCC voltage in power-off standby mode	SYSVCCLow	-	2.75	5.5	V
Power hold voltage for EVCC power supply	VoltageMin	-	2.7	-	V

Note 1. This is the voltage for transition to power-off standby mode. This value must be equal to or less than the min. Vstdby1 value.
Both VCC and EVCC must be less than Vstdby1.

CAUTION

For resetting while flash memory is being programmed or erased, follow the specifications in the RH850/U2B Flash Memory User's Manual: Hardware Interface.

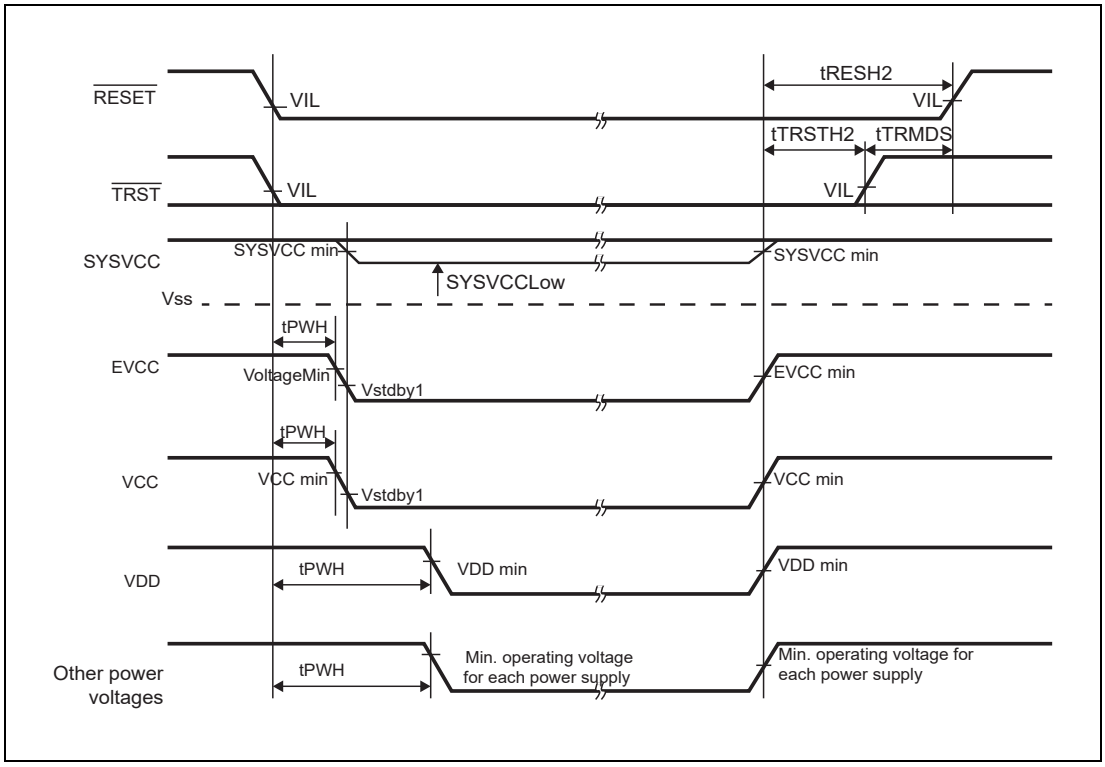


Figure 3.19 Power-Off Standby Timing

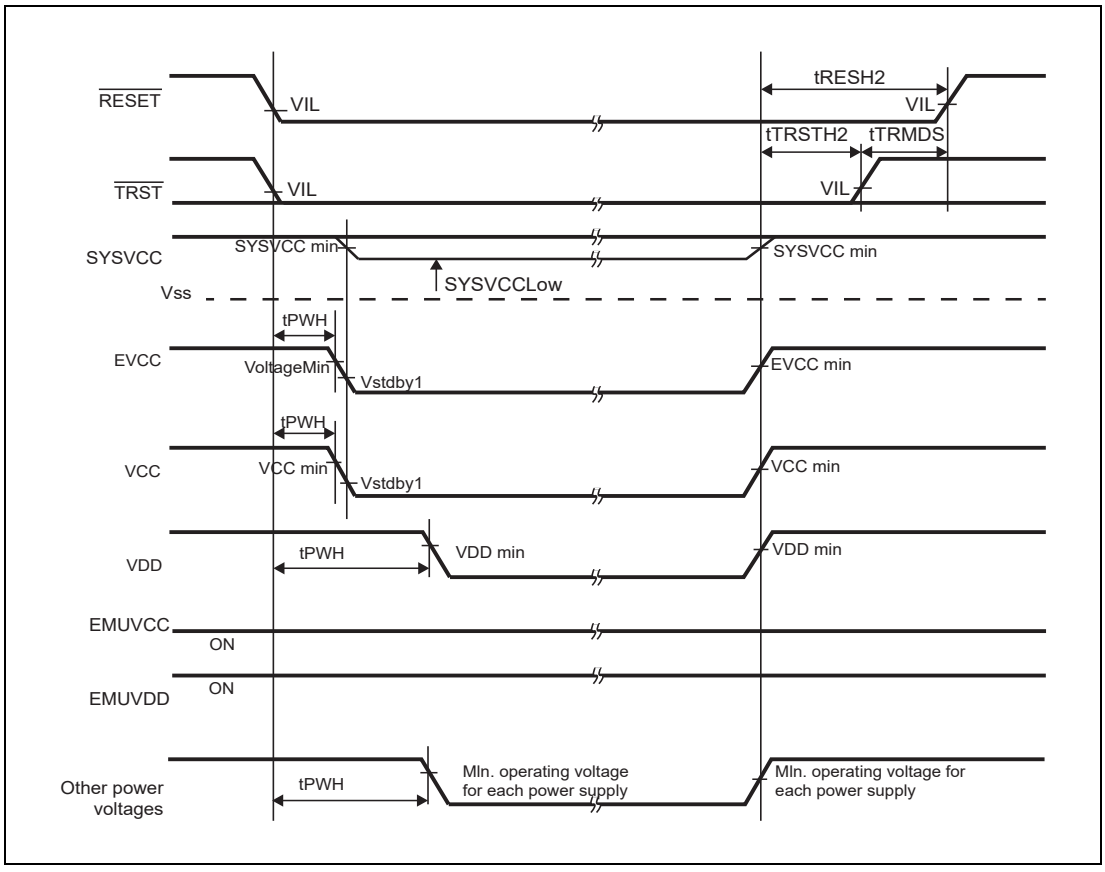


Figure 3.20 Power-Off Standby Timing (when EMUVDD is supplied)

3.3.4 Clock Timing

3.3.4.1 Main Oscillator Characteristics

Conditions:

- Supply voltage range: Refer to **Section 3.2.1, Operational Conditions**.

Table 3.45 Main Oscillator Characteristics (1/3)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC}*1,*2	Crystal/Ceramic		16 - 1%		40 + 1%	MHz
		Crystal (for SGMII) *5		20 –100ppm		20 + 100ppm	MHz
				25 – 100ppm		25 + 100ppm	MHz
				40 – 100ppm		40 + 100 ppm	MHz
MainOSC oscillation operating point	V_{MOSCOP}	Crystal/Ceramic			1.217		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$	Crystal/Ceramic		0.9			V
MainOSC oscillation stabilization time	t_{MSTB}	Crystal/Ceramic				5	ms
MainOSC oscillation amplifier reaction time	$t_{MOSCAMP}$	Crystal/Ceramic				200	µs
Internal Capacitor size selectable by MOSC_CAP_SEL setting (OPBT10 setting)	C_{capsel}	MOSC_CAP_SEL [3:0]	= 0000_B	*4	0 (4.0), 0 (5.6)*3	*4	pF
			= 0001_B	*4	1 (4.9), 1 (6.5)*3	*4	pF
			= 0010_B	*4	2 (6.0), 2 (7.6)*3	*4	pF
			= 0011_B	*4	3 (6.9), 3 (8.5)*3	*4	pF
			= 0100_B	*4	4 (7.7), 4 (9.3)*3	*4	pF
			= 0101_B	*4	5 (8.7), 5 (10.2)*3	*4	pF
			= 0110_B	*4	6 (9.8), 6 (11.3)*3	*4	pF
			= 0111_B	*4	7 (10.6), 7 (12.1)*3	*4	pF
			= 1000_B	*4	8 (11.5), 8 (13.1)*3	*4	pF
			= 1001_B	*4	9 (12.6), 9 (14.1)*3	*4	pF
			= 1010_B	*4	10 (13.5), 10 (15.0)*3	*4	pF
Internal damping resistor size selectable by MOSC_RD_SEL_A and MOSC_RD_SEL_B setting (OPBT10 setting) *2	R_{rdsel}	MOSC_RD_SEL_A [2:0] MOSC_RD_SEL_B [2:0]	= 000_B	230	340	578	Ω
			= 001_B	378	540	1026	Ω
			= 010_B	574	820	1435	Ω
			= 011_B	756	1080	1782	Ω
			= 100_B	959	1370	2124	Ω
			= 101_B	1764	2520	3402	Ω
			= 110_B	1764	2520	3402	Ω
			= 111_B	1764	2520	3402	Ω

Table 3.45 Main Oscillator Characteristics (2/3)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Trans conductance size (gm) and Output conductance size (gds) selectable by MOSC_SHTSTBY_A, MOSC_AMPSEL_A, MOSC_SHTSTBY_B and MOSC_AMPSEL_B setting (OPBT10 setting) *2	gm, gds	{MOSC_SHTSTBY_A, MOSC_AMPSEL_A} or {MOSC_SHTSTBY_B, MOSC_AMPSEL_B} OSCVCC = 3.0 V to 3.6 V	= 0000_B	1.05, 0.079	2.28, 0.153	3.69, 0.452	ms
			= 0001_B	1.66, 0.108	3.58, 0.204	5.78, 0.521	ms
			= 0010_B	2.25, 0.134	4.85, 0.251	7.80, 0.585	ms
			= 0011_B	2.82, 0.158	6.08, 0.294	9.76, 0.645	ms
			= 0100_B	3.73, 0.196	8.07, 0.362	12.91, 0.739	ms
			= 0101_B	4.76, 0.238	10.32, 0.437	16.49, 0.846	ms
			= 0110_B	5.56, 0.271	12.10, 0.496	19.35, 0.929	ms
			= 0111_B	6.33, 0.302	13.81, 0.553	22.08, 1.007	ms
			= 1000_B	3.94, 0.194	8.45, 0.371	13.52, 0.592	ms
			= 1001_B	4.46, 0.215	9.58, 0.409	15.32, 0.651	ms
			= 1010_B	4.97, 0.236	10.69, 0.446	17.07, 0.708	ms
			= 1011_B	5.46, 0.255	11.76, 0.481	18.78, 0.764	ms
			= 1100_B	6.24, 0.286	13.49, 0.538	21.54, 0.852	ms
			= 1101_B	7.12, 0.321	15.46, 0.603	24.71, 0.953	ms
			= 1110_B	7.82, 0.351	17.04, 0.653	27.24, 1.031	ms
			= 1111_B	8.49, 0.377	18.56, 0.701	29.68, 1.105	ms
Trans conductance size (gm) and Output conductance size (gds) selectable by MOSC_SHTSTBY_A, MOSC_AMPSEL_A, MOSC_SHTSTBY_B and MOSC_AMPSEL_B setting (OPBT10 setting) *2	gm, gds	{MOSC_SHTSTBY_A, MOSC_AMPSEL_A} or {MOSC_SHTSTBY_B, MOSC_AMPSEL_B} OSCVCC = 4.5 V to 5.5 V	= 0000_B	1.15, 0.089	2.47, 0.163	4.06, 0.535	ms
			= 0001_B	1.80, 0.119	3.85, 0.211	6.27, 0.592	ms
			= 0010_B	2.44, 0.145	5.19, 0.254	8.41, 0.645	ms
			= 0011_B	3.05, 0.170	6.48, 0.295	10.47, 0.647	ms
			= 0100_B	4.04, 0.209	8.57, 0.358	13.80, 0.781	ms
			= 0101_B	5.17, 0.251	10.96, 0.428	17.58, 0.876	ms
			= 0110_B	6.06, 0.284	12.87, 0.482	20.61, 0.952	ms
			= 0111_B	6.91, 0.314	14.70, 0.535	23.53, 1.023	ms
			= 1000_B	4.28, 0.204	8.98, 0.365	14.44, 0.580	ms
			= 1001_B	4.85, 0.226	10.18, 0.401	16.34, 0.633	ms
			= 1010_B	5.41, 0.246	11.36, 0.435	18.20, 0.684	ms
			= 1011_B	5.95, 0.266	12.50, 0.467	20.01, 0.734	ms
			= 1100_B	6.83, 0.297	14.35, 0.522	22.96, 0.815	ms
			= 1101_B	7.82, 0.333	16.49, 0.581	26.35, 0.903	ms
			= 1110_B	8.61, 0.363	18.20, 0.627	29.38, 0.973	ms
			= 1111_B	9.37, 0.389	19.86, 0.672	31.72, 1.040	ms
X1 clock Input frequency	f_{EX} *1			15.8		40.0	MHz
X1 clock Input cycle time	t_{EXCYC}			25.0		63.1	ns
X1 Input leakage current	I_{LIH}	VI = OSCVCC				0.5	µA
	I_{LIL}	VI = 0 V				–0.5	µA
X1 clock Input low level pulse width	t_{EXL}	f_{EX} = 16 MHz		26			ns
		f_{EX} = 20 MHz		20			ns
		f_{EX} = 24 MHz		16			ns
		f_{EX} = 25 MHz		16			ns
		f_{EX} = 40 MHz		10			ns

Table 3.45 Main Oscillator Characteristics (3/3)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
X1 clock Input high level pulse width	t_{EXH}	f_{EX} = 16 MHz	26			ns
		f_{EX} = 20 MHz	20			ns
		f_{EX} = 24 MHz	16			ns
		f_{EX} = 25 MHz	16			ns
		f_{EX} = 40 MHz	10			ns
X1 clock rise time	t_{EXR}	f_{EX} = 16 MHz			4	ns
		f_{EX} = 20 MHz			4	ns
		f_{EX} = 24 MHz			3	ns
		f_{EX} = 25 MHz			3	ns
		f_{EX} = 40 MHz			2.5	ns
X1 clock fall time	t_{EXF}	f_{EX} = 16 MHz			4	ns
		f_{EX} = 20 MHz			4	ns
		f_{EX} = 24 MHz			3	ns
		f_{EX} = 25 MHz			3	ns
		f_{EX} = 40 MHz			2.5	ns
X1 clock Input total jitter (Dj + 14 * rms Random jitter)		The clock source of SGMII used @ 20MHz			73 *6	ps
X1 Input capacitance	C_{X1}	Main OSC. EXCLK mode, MOSC_CAP_SEL = **0010**			10	pF

Note 1. To reach internal usable clocks only following 5 frequencies are supported: 16MHz, 20MHz, 24MHz, 25MHz and 40MHz. Tolerance of external quartz crystal is assumed as +/–1%.

Note 2. The StartUp is supported without external components under following conditions:
See RH850/U2B Group User's Manual:Hardware **Section 63.12.16, OPBT10 — Option Byte 10** for default values of drivability, damping resistance and internal capacitance.
Specification covers a maximum external stray capacitance of up to 6pF to each pin X1 and X2.
After StartUp drivability and capacitance will be configured by OPBT10.
A possible exceeding of the recommended maximum drive level for a crystal for all start-up phases have to be agreed with the crystal manufacturers separately.

Note 3. Ccapsel_x1 (Ccapsel_x1 including parasitic capacitance to ground at the X1 side), Ccapsel_x2".

Note 4. The capacitor tolerance is ±15%.

Note 5. The clock source of SGMII used. Ethernet grade crystal is mandatory. Example: CX3225GA(KYOCERA)

Note 6. 12 kHz to 20 MHz rms jitter = 3 ps.

CAUTION

Oscillation stabilization times differ according to matching with the resonator. Secure an oscillation stabilization time determined through evaluation of matching.

3.3.4.2 Internal Oscillator Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.46 Internal Oscillator Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		216	240	264	kHz
HS IntOSC frequency	f_{RH}		191	200	209	MHz
HV IntOSC frequency	f_{RHV}		8	16	24	MHz

3.3.4.3 PLL Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.47 PLL Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL output long term jitter*1	t_{PLLLTJ}	Term = 1 µs	–500		500	ps
		Term = 20 µs	–1		1	ns
PLL lock time*2	t_{PLLLCT}		201		222	µs

Note 1. This characteristic is not tested in production.
Note 2. Lock time is time until being set "1" in PLLS.PLLCLKSTAB bit after PLLE.PLLENTRG bit is written "1".

Table 3.48 SSCG PLL Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Modulation frequency	f_{mod}		20		60	kHz
Frequency dithering range*1	f_{dit}	SELMPERCENT=000	0.9	0.95	0.995	%
		SELMPERCENT=001	1.64	2.0	2.36	%
		SELMPERCENT=010	2.46	3.0	3.54	%
		SELMPERCENT=011	3.28	4.0	4.72	%
		SELMPERCENT=100	4.10	5.0	5.90	%
PLL lock time					200	us

Note 1. Dithered frequency mode is only supported in down spread mode.

Table 3.49 RHSIF PLL Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL lock time	$t_{RHPLLLCT}$				50	µs

3.3.4.4 External Clock Output Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.50 Clock Output Timing*1*2

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock output period time	t_{CLKOUT}		41.6			ns
Clock output high level width	t_{WCOH}		t_{CLKOUT} / 2 – 10			ns
Clock output low level width	t_{WCOL}		t_{CLKOUT} / 2 – 10			ns

Note 1. There is a function to output the internal clock via EXTCLKnO pin.

Note 2. For base clock, refer to related RH850/U2B Group User's Manual:Hardware **Section 15, Clock Controller**.

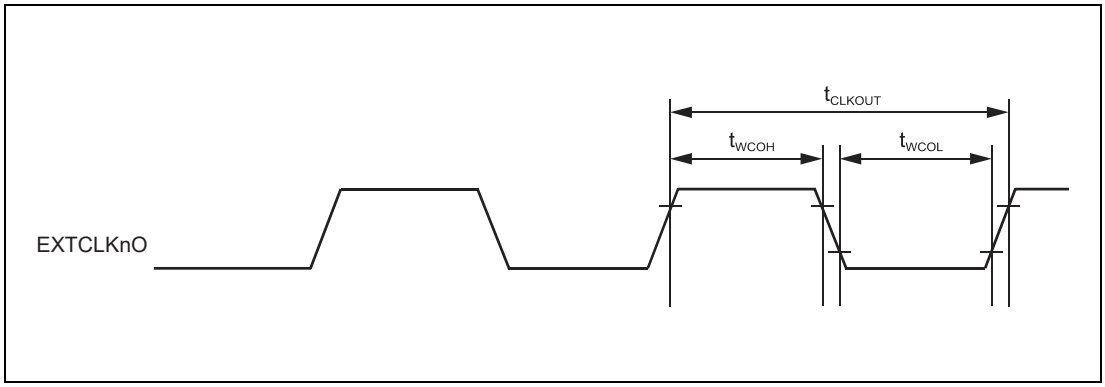


Figure 3.21 Clock Output Timing

3.3.5 ERAM / INSTMRAM and Aurora Retention Mode Timing

Table 3.51 ERAM / INSTMRAM and Aurora Retention Mode Timing

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SYSVCC Voltage slope (ERAM / INSTMRAM and Aurora retention mode)	tvs	-	5	-	µs/V

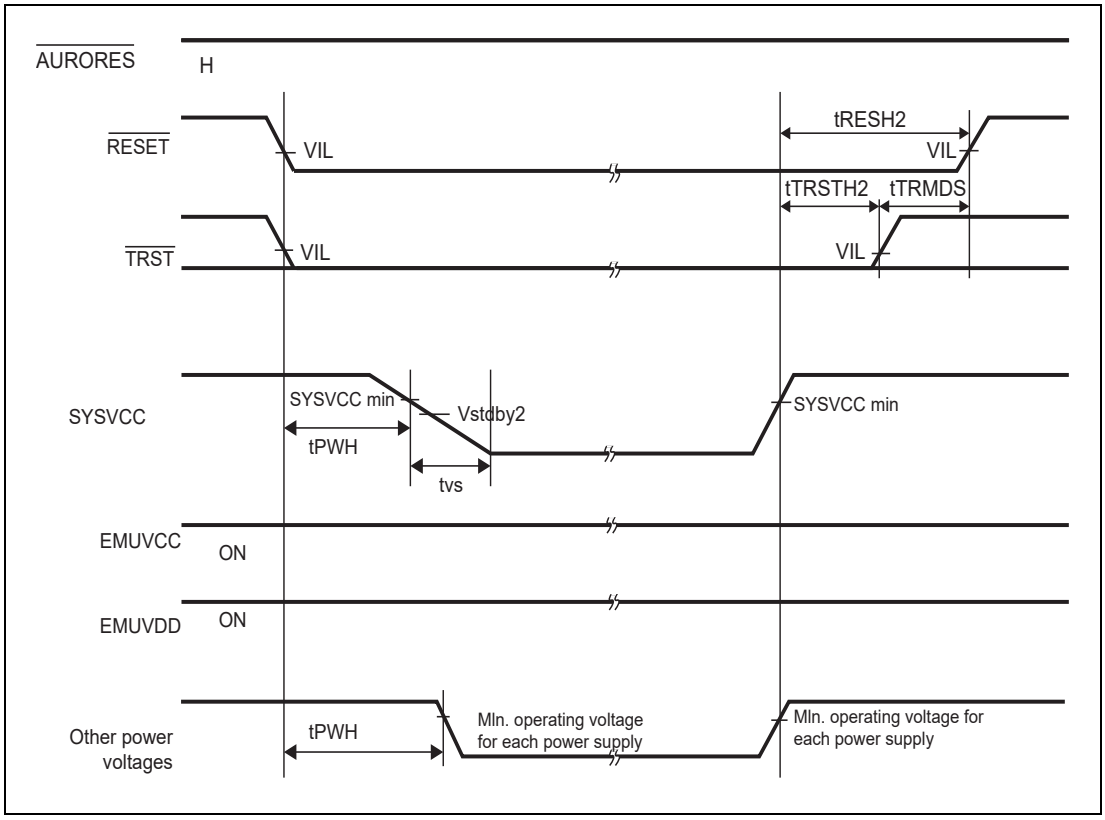


Figure 3.22 ERAM / INSTMRAM and Aurora Retention Mode Timing

3.3.6 Output Slew Rate

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.52 Output Slew Rate (IOVCC = 3.3 ± 0.3V*2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output rise and fall time	t_{KRP11}/t_{KFP11}	Drive strength = 1 20% to 80%*1	CL = 100 pF		3.1	6.7	ns
	t_{KRP12}/t_{KFP12}	Drive strength = 2 20% to 80%*1	CL = 30 pF		1.9	4.0	ns
			CL = 50 pF		3.0	6.7	ns
			CL = 100 pF		5.7	13.4	ns
	t_{KRP13}/t_{KFP13}	Drive strength = 3 20% to 80%*1	CL = 30 pF		2.7	6.7	ns
			CL = 50 pF		4.4	11.1	ns
			CL = 100 pF		8.5	21.0	ns
	t_{KRP14}/t_{KFP14}	Drive strength = 4 20% to 80%*1	CL = 30 pF		6.0	13.5	ns
			CL = 50 pF		10.0	22.5	ns
			CL = 100 pF		20.0	45.0	ns
	t_{KRP15}/t_{KFP15}	Drive strength = 5 20% to 80%*1	CL = 30 pF		12.0	27.0	ns
			CL = 50 pF		20.0	45.0	ns
			CL = 100 pF		40.0	90.0	ns

Note 1. Please see **Section 3.2.5, Output Voltage Characteristics Table 3.8, Output Voltage Characteristics**.

Note 2. "IOVCC" means power supply voltage for I/O ports. See the appendix “E02_01_List_of_Pin_Assignment.xlsx” for the power supply of each pin.

Table 3.53 Output Slew Rate (IOVCC = 5.0 ± 0.5V*2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output rise and fall time	t_{KRP11}/t_{KFP11}	Drive strength = 1 20% to 80%*1	CL = 100 pF		2.4	6.2	ns
	t_{KRP12}/t_{KFP12}	Drive strength = 2 20% to 80%*1	CL = 30 pF		1.5	3.6	ns
			CL = 50 pF		2.4	6.0	ns
			CL = 100 pF		4.7	12.2	ns
	t_{KRP13}/t_{KFP13}	Drive strength = 3 20% to 80%*1	CL = 30 pF		2.0	5.3	ns
			CL = 50 pF		3.3	8.5	ns
			CL = 100 pF		6.4	16.6	ns
	t_{KRP14}/t_{KFP14}	Drive strength = 4 20% to 80%*1	CL = 30 pF		4.6	10.3	ns
			CL = 50 pF		7.5	16.9	ns
			CL = 100 pF		14.8	33.3	ns
	t_{KRP15}/t_{KFP15}	Drive strength = 5 20% to 80%*1	CL = 30 pF		9.0	20.3	ns
			CL = 50 pF		15.0	33.8	ns
			CL = 100 pF		30.0	67.5	ns

Note 1. Please see **Section 3.2.5, Output Voltage Characteristics Table 3.8, Output Voltage Characteristics**.

Note 2. "IOVCC" means power supply voltage for I/O ports. See the appendix "E02_01_List_of_Pin_Assignment.xlsx" for the power supply of each pin.

3.3.7 Control Signal Timing

3.3.7.1 RESET Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.54 RESET Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}*1		2000			µs
$\overline{\text{RESET}}$ pulse rejection width*2	t_{WRRJ}*2		200		1200	ns

Note 1. t_{WRSL} is the minimum required time to complete the reset state generated by an external reset signal. When an external reset signal is input that is shorter than this time, the reset state will continue even after the external reset release. This microcontroller is completely reset after completion of the reset state. An external reset request is accepted with a reset input width of more than the maximum time of t_{WRRJ}. When the reset pulse width is less than the minimum value of the reset noise rejection width, the reset request is not accepted. When the reset signal is input during DeepSTOP mode, the reset state will continue during the wait time set by PWRGD_CNT even when the external reset signal is released.

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

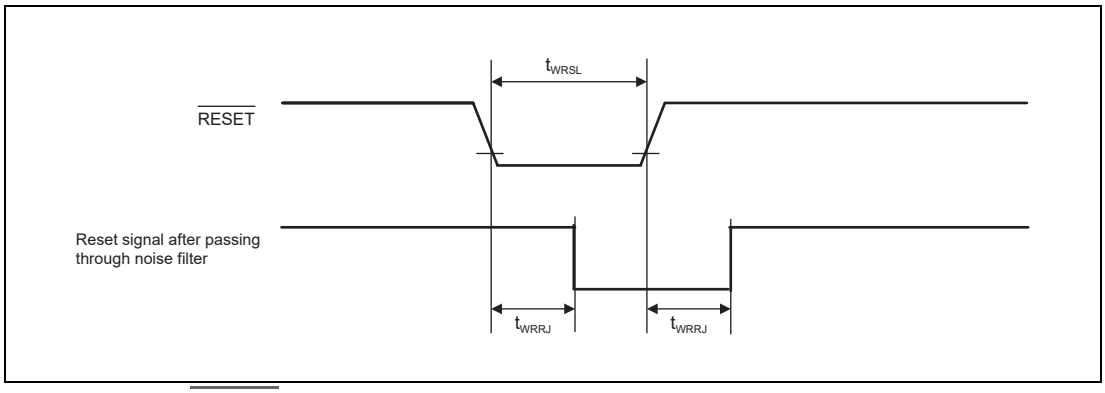


Figure 3.23 $\overline{\text{RESET}}$ Timing

3.3.7.2 Interrupt, Wake-up and Error Input Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.55 Interrupt Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	*3	600			ns
		*4	20			µs
NMI input low level width	t_{WNIL}	*3	600			ns
		*4	20			µs
NMI pulse rejection width*2	t_{WNIRJ}		100		600	ns
IRQn input high level width	t_{WITH}	*3	600			ns
		*4	20			µs
IRQn input low level width	t_{WITL}	*3	600			ns
		*4	20			µs
IRQn pulse rejection width*2	t_{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t_{WRLINH}		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up input low level width	t_{WRLINL}		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	$t_{WRLINRJ}$		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
CANnRX wake-up input high level width	t_{WCANH}		(S + 1) x 1/fs*1			ns
CANnRX wake-up input low level width	t_{WCANL}		(S + 1) x 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t_{WCANRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
FLXnRXDA wake-up input high level width	t_{WFLXH}		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up input low level width	t_{WFLXL}		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t_{WFLXRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
ERRORINn wake-up input high level width	t_{WERRH}		(S + 1) x 1/fs*1			ns
ERRORINn wake-up input low level width	t_{WERRL}		(S + 1) x 1/fs*1			ns
ERRORINn wake-up pulse rejection width*2	t_{WERRRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOSC/20)

Note 4. Level Detection (CLK_LPS is operated by CLK_LSIOSC)

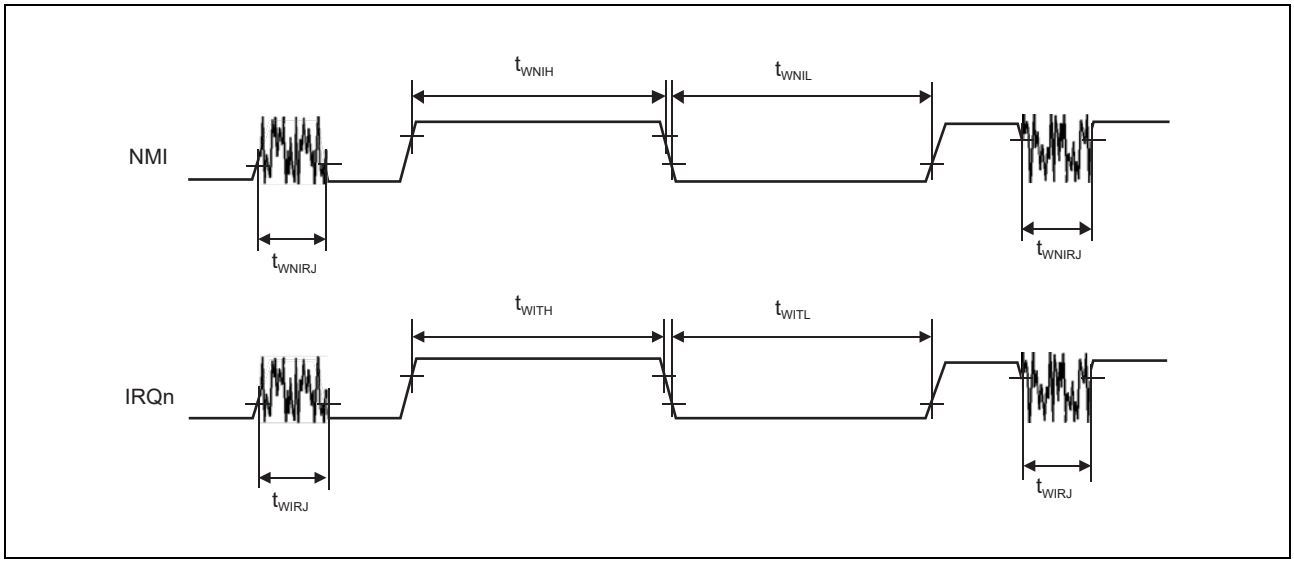


Figure 3.24 Interrupt, wake-up and error input timing

3.3.7.3 Mode Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.56 Mode Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0, FLMD1, SBMD, input high level width	t_{WMDH}		600			ns
FLMD0, FLMD1, SBMD, input low level width	t_{WMDL}		600			ns
FLMD0, FLMD1, SBMD, pulse rejection width*1	t_{WMDRJ}		100		600	ns

Note 1. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

NOTE

Switching of FLMD0 after rising edge of $\overline{\text{RESET}}$ is prohibited except for serial programming mode.

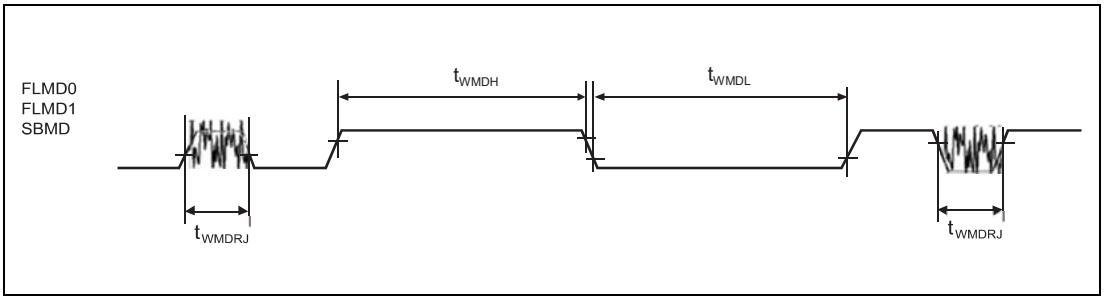


Figure 3.25 Mode Timing

3.3.7.4 ADTRG Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.57 ADCKnTRGm Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCKnTRGm input high level width	t_{WADH}		(S + 1) x 1/fs*1			ns
ADCKnTRGm input low level width	t_{WADL}		(S + 1) x 1/fs*1			ns
ADCKnTRGm pulse rejection width*2	t_{WADRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB, CLKA_ADC
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

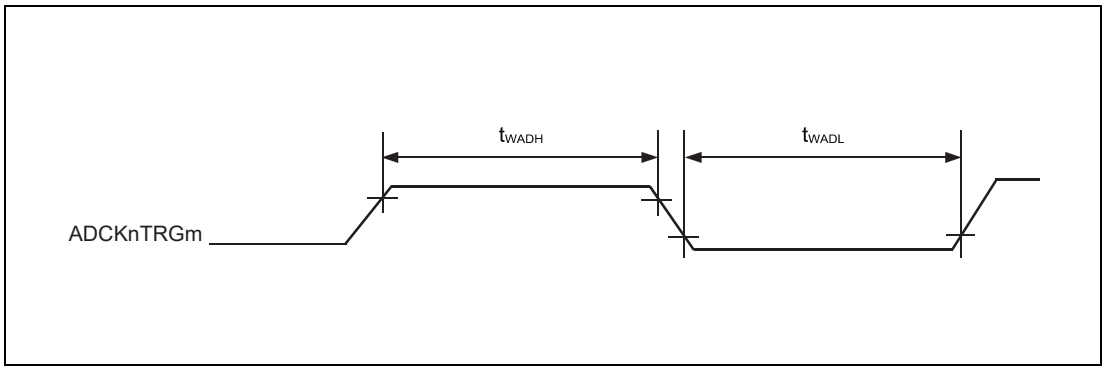


Figure 3.26 ADCKnTRGm Timing

3.3.7.5 Communication Signal Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.58 Control Signal

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	$t_{WSENTIH}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
SENTnRX input low level width	$t_{WSENTIL}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
SENTnRX pulse rejection width*2	$t_{WSENTIRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
PSI5nRX input high level width*	$t_{WPSI5IH}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
PSI5nRX input low level width	$t_{WPSI5IL}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
PSI5nRX pulse rejection width*2	$t_{WPSI5IRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
RHSBnEMRG pulse rejection width	$t_{WRHSBIH}$		(S + 1) x 1/fs*1			ns
RHSBnEMRG input low level width	$t_{WRHSBIL}$		(S + 1) x 1/fs*1			ns
RHSBnEMRG pulse rejection width*2	$t_{WRHSBIRJ}$		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB (for SENTnRX and PSI5nRX)
frequency of CLK_LSB (for RHSBnEMRG)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

3.3.8 Low Power Sampler (DPIN input) Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 3 (Medium) (SELDP2-0)

Table 3.59 Low Power Sampler Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time	t_{DSDDI}				150	ns

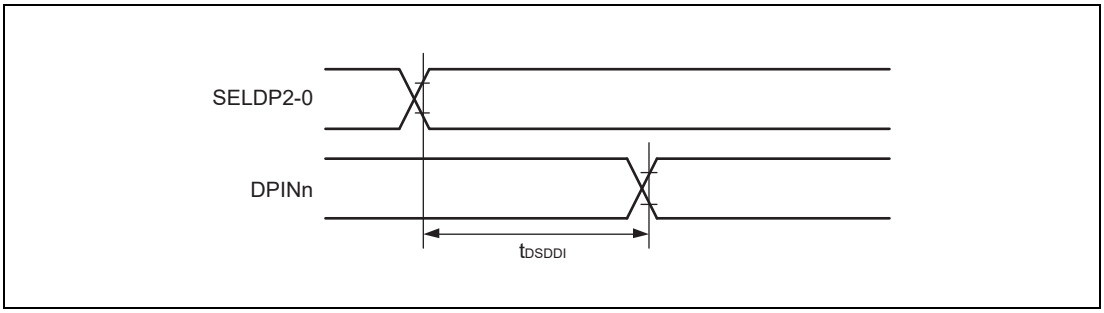


Figure 3.27 Low Power Sampler Timing

3.3.9 SFMA Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.60 SFMA Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SFMA0CLK clock cycle	$t_{SFMAcyc}$		25			ns
SFMA0CLK high pulse width	t_{SFMAWH}		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK low pulse width	t_{SFMAWL}		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
Data input setup time	$t_{SFMADIS}$		9.0			ns
Data input hold time	t_{SFMDIH}		0.0			ns
SFMA0SSL setup time	t_{SFMASS}		1 × $t_{SFMA0cyc}$ – 12.5		8 × $t_{SFMA0cyc}$	ns
SFMA0SSL hold time	t_{SFMASH}		1.5 × $t_{SFMA0cyc}$		8.5 × $t_{SFMA0cyc}$ + 12.5	ns
Continuous transfer delay time	$t_{SFMACTD}$		1 × $t_{SFMA0cyc}$		8 × $t_{SFMA0cyc}$	ns
Data output delay time	$t_{SFMADOD}$				6.6	ns
Data output hold time	$t_{SFMADOH}$		–4.6			ns
Data output buffer on time	$t_{SFMADBON}$				6.6	ns
Data output buffer off time	$t_{SFMADBOFF}$		–7.0		3.0	ns

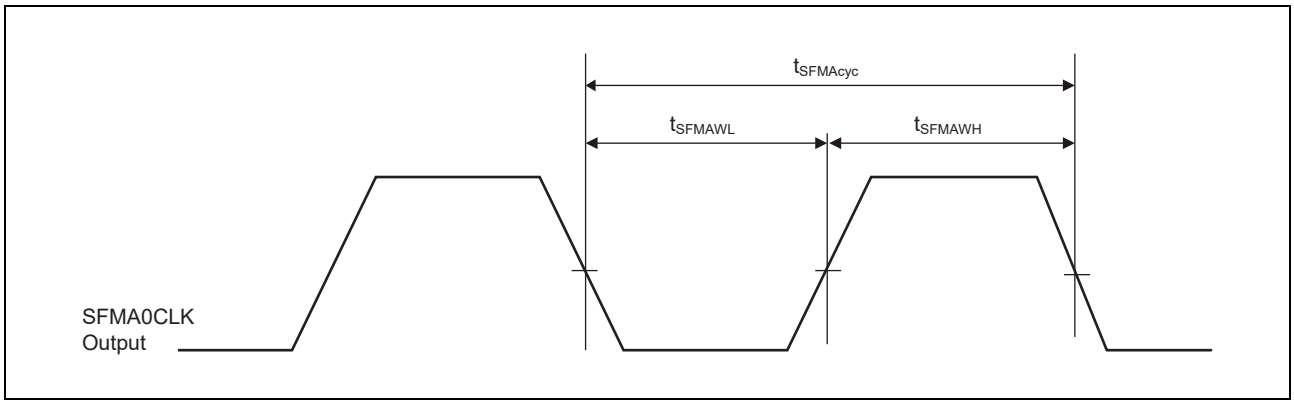


Figure 3.28 SFMA Clock Output Timing

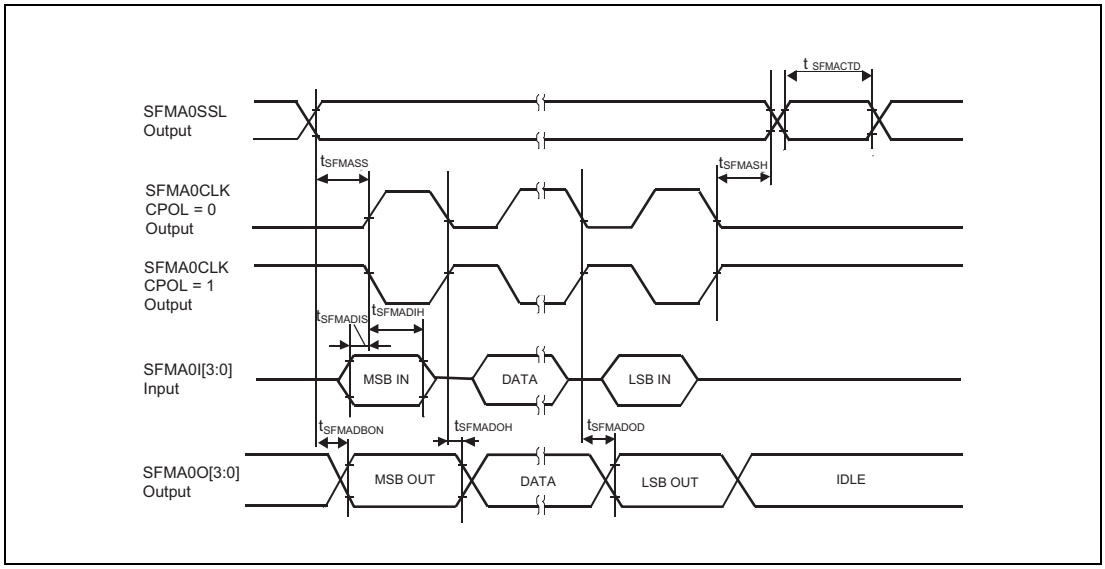


Figure 3.29 SFMA Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)

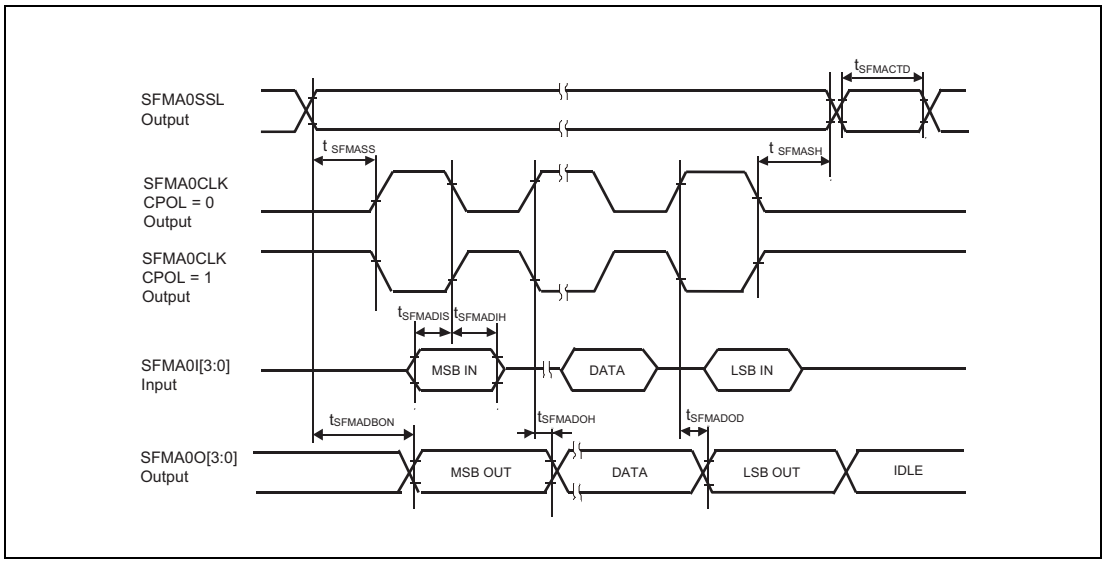


Figure 3.30 SFMA Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)

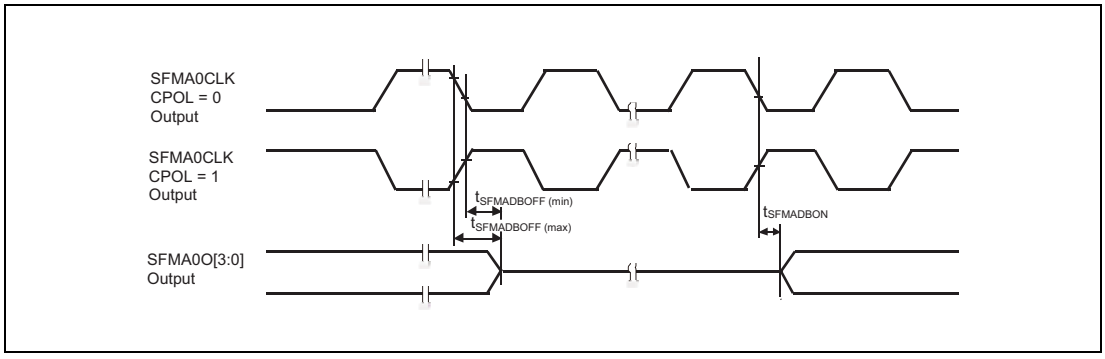


Figure 3.31 SFMA Timing Switching the Buffers on and off (CPHAT = 0, CPHAR = 0)

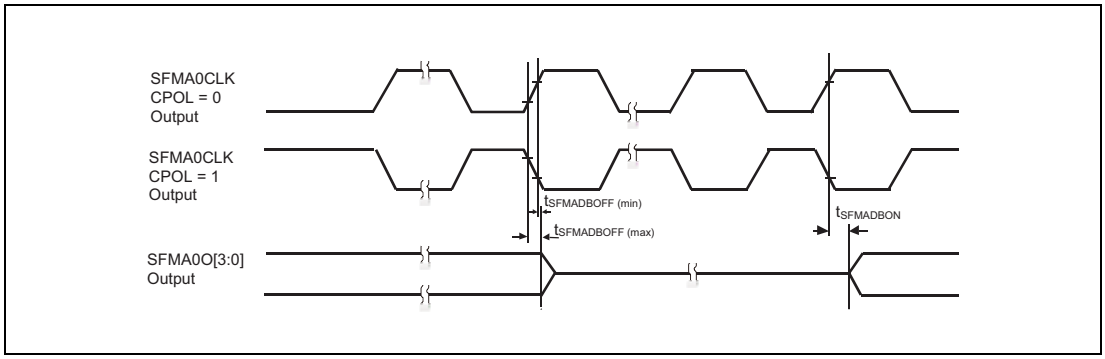


Figure 3.32 SFMA Timing for Switching the Buffers on and off (CPHAT = 1, CPHAR = 1)

3.3.10 MMCA Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.61 MMCA Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MMCA0CLK clock cycle	$t_{MMCA0CYC}$		25			ns
MMCA0CLK high time	$t_{MMCA0WH}$		6.5			ns
MMCA0CLK low time	$t_{MMCA0WL}$		6.5			ns
MMCA0CMD output data delay time	$t_{MMCA0CMDD}$		– 6.5		6.5	ns
Data output delay time	$t_{MMCA0DADD}$		– 6.5		6.5	ns
MMCA0CMD input data setup time	$t_{MMCA0CMS}$		7.5			ns
MMCA0CMD input data hold time	$t_{MMCA0CMH}$		2.5			ns
Data input setup time	$t_{MMCA0DAS}$		7.5			ns
Data input hold time	$t_{MMCA0DAH}$		2.5			ns

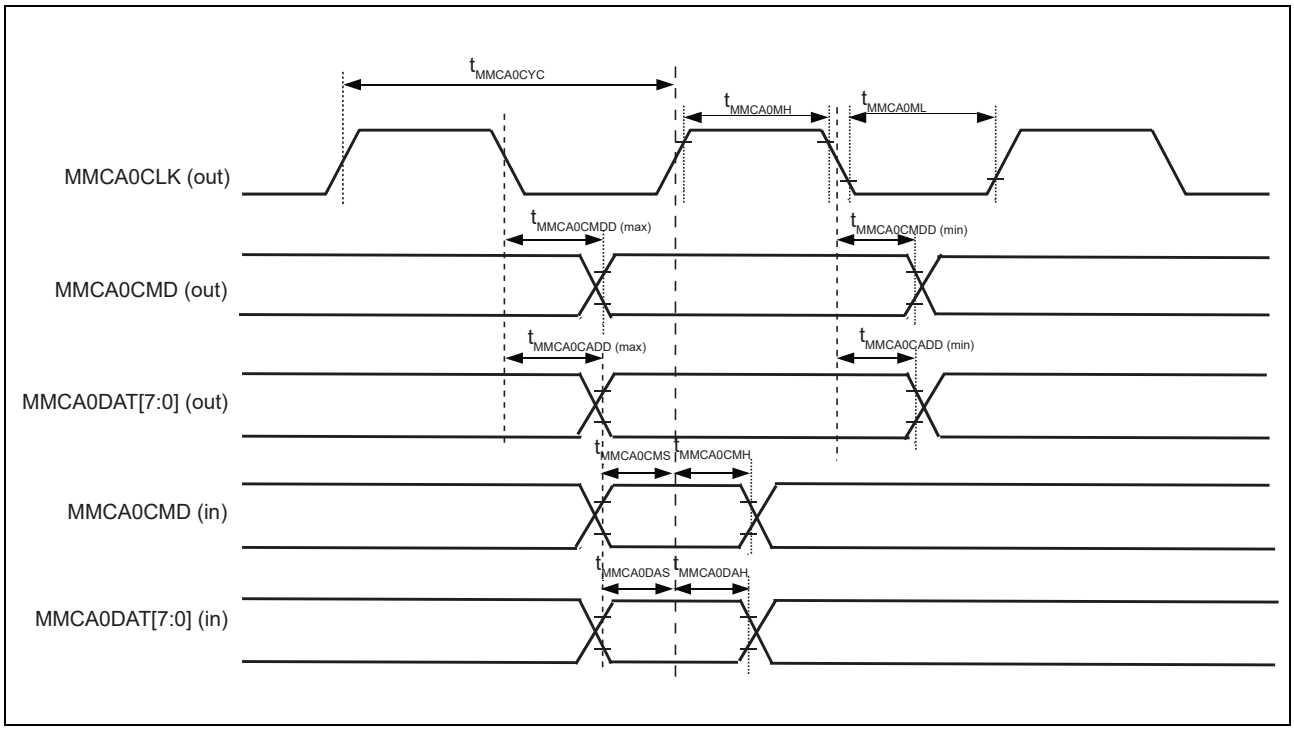


Figure 3.33 MMCA Timing

3.3.11 MSPI Timing

3.3.11.1 MSPI Communication Speed Overview

Table 3.62 MSPI Communication Speed Overview (1/3)

MSPIn pin name		Port	Max. Frequency
MSPI0	SC	P11_5	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SO	P11_9	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SI	P11_4	20 MHz
	SC	P14_1	10 MHz
	SO	P14_2	10 MHz
	SI	P13_1	10 MHz
MSPI1	SC	P11_2	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SO	P11_7	20 MHz(The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SI	P11_6	20 MHz
	SC	P10_4	10 MHz
	SO	P10_2	10 MHz
	SI	P10_3	10 MHz
MSPI2	SC	P14_0	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SO	P14_3	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SI	P14_2	20 MHz
	SC	P15_4	10 MHz
	SO	P15_3	10 MHz
	SI	P15_7	10 MHz
MSPI3	SC	P02_9	20 MHz
	SO	P02_5	20 MHz
	SI	P02_6	20 MHz
	SC	P10_0	10 MHz
	SO	P10_3	10 MHz
	SI	P10_1	10 MHz
	SC	P01_7	10 MHz
	SO	P01_6	10 MHz
	SI	P01_5	10 MHz

Table 3.62 MSPI Communication Speed Overview (2/3)

MSPIn pin name		Port	Max. Frequency
MSPI4	SC	P22_1	20 MHz
	SO	P22_3	20 MHz
	SI	P22_2	20 MHz
	SC	P33_6	10 MHz
	SO	P33_2	10 MHz
	SI	P33_3	10 MHz
	SC	P33_9	10 MHz
	SO	P33_11	10 MHz
	SI	P33_10	10 MHz
MSPI5	SC	P23_7	20 MHz
	SO	P23_5	20 MHz
	SI	P23_6	20 MHz
	SC	P22_6	10 MHz
	SO	P22_2	10 MHz
	SI	P22_3	10 MHz
	SC	P14_12	10 MHz
	SO	P14_11	10 MHz
	SI	P14_10	10 MHz
MSPI6	SC	P10_7	20 MHz
	SO	P10_6	20 MHz
	SI	P10_8	20 MHz
	SC	P12_0	10 MHz
	SO	P12_2	10 MHz
	SI	P12_1	10 MHz
	SCKN/SCKP	P10_0, P10_1	40 MHz
	SON/SOP	P10_2, P10_3	40 MHz
	SIN/SIP	P10_4, P10_5	40 MHz
MSPI7	SC	P34_2	20 MHz
	SO	P34_4	20 MHz
	SI	P34_3	20 MHz
	SC	P32_6	10 MHz
	SO	P32_5	10 MHz
	SI	P23_3	10 MHz
	SC	P30_1	10 MHz
	SO	P30_0	10 MHz
	SI	P30_2	10 MHz

Table 3.62 MSPI Communication Speed Overview (3/3)

MSPIn pin name		Port	Max. Frequency
MSPI8	SC	P20_4	20 MHz
	SO	P20_0	20 MHz
	SI	P20_1	20 MHz
	SC	P22_9	10 MHz
	SO	P22_8	10 MHz
	SI	P22_7	10 MHz
	SC	P11_0	10 MHz
	SO	P11_5	10 MHz
	SI	P11_8	10 MHz
MSPI9	SC	P12_9	20 MHz
	SO	P12_4	20 MHz
	SI	P12_8	20 MHz
	SC	P15_6	10 MHz
	SO	P15_5	10 MHz
	SI	P15_2	10 MHz
	SCKN/SCKP	P13_0, P13_1	40 MHz
	SON/SOP	P13_3, P13_2	40 MHz
	SIN/SIP	P14_4, P14_5	40 MHz

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

3.3.11.2 MSPI Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.63 MSPI Timing (Master mode: Communication Speed 10MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle[*1*5]	T_{SCKCYC}		100			ns
MSPInSCK Low/High width[*1]	T_{SCKWID}	CL = 30 pF Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 9			ns
		CL = 50 pF Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 12			ns
		CL = 100 pF Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 23			ns
		CL = 30 pF Drive strength = 4 (Low)	0.5 × T_{SCKCYC} – 15.5			ns
		CL = 50 pF Drive strength = 2 (High)	0.5 × T_{SCKCYC} – 10			ns
		CL = 100 pF Drive strength = 1[*4] (Very High)	0.5 × T_{SCKCYC} – 10			ns
Chip select signal setup time[*2*6]	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] x $T_{MSPInCLK}$ - 15			ns
Chip select signal hold time[*3]	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] x $T_{MSPInCLK}$ - 5			ns
Receive data setup time (MSPInSAMP =0)	T_{MSISU1}		20			ns
Receive data setup time (MSPInSAMP =1)	T_{MSISU2}		20			ns
Receive data hold time (MSPInSAMP =0)	T_{MSIHO}		0			ns
Receive data hold time (MSPInSAMP =1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}		—		7	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC} / 2) – 5			ns

Note 1. This parameter is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].

Note 2. This parameter is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.

Note 3. This parameter is programmable, the value can be set by MSPInHOLDm.

Note 4. The selection of "Drive strength = 1" is available on P11_2, P11_5 and P14_0 only.

Note 5. Use by “PCLK/2 ≧ MSPInSCK”.

Note 6. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.64 MSPI Timing (Master mode: Communication Speed 20MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*4	T_{SCKCYC}		50			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 15pF@50Ω Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 6			ns
Chip select signal setup time*2*5	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] x $T_{MSPInCLK}$ – 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] x $T_{MSPInCLK}$ – 5			ns
Receive data setup time (MSPInSAMP = 1)	T_{MSISU2}		20			ns
Receive data hold time (MSPInSAMP = 1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}		—		7	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC}/2) – 5			ns

Note 1. This parameter is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].
Note 2. This parameter is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.
Note 3. This parameter is programmable, the value can be set by MSPInHOLDm.
Note 4. Use by “PCLK/2 ≧ MSPInSCK”.
Note 5. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.65 MSPI Timing (Master mode: Communication Speed 40MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*4	T_{SCKCYC}		25			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 15pF@LVDS	0.5 × T_{SCKCYC} – 2.5			ns
Chip select signal setup time*2*5	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] x $T_{MSPInCLK}$ – 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] x $T_{MSPInCLK}$ – 5			ns
Receive data setup time (MSPInSAMP = 1)	T_{MSISU2}		7			ns
Receive data hold time (MSPInSAMP = 1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}		—		5	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC}/2) – 5			ns

Note 1. This parameter is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].
Note 2. This parameter is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.
Note 3. This parameter is programmable, the value can be set by MSPInHOLDm.
Note 4. Use by “PCLK/2 ≧ MSPInSCK”.
Note 5. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.66 MSPI Timing (Slave mode: Communication Speed 10MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		100			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 23$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}		—		54	ns
Transmit data delay time 2 (MSPInCSIE = 1)	T_{SSODL2}		—		40	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC}/2) - 5$			ns
Transmit data release time (MSPInCSIE = 1)	T_{SSOREL}		—		40	ns

Table 3.67 MSPI Timing (Slave mode: Communication Speed 20MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		50			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 6$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}		—		24	ns
Transmit data delay time 2 (MSPInCSIE = 1)	T_{SSODL2}		—		40	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC}/2) - 5$			ns
Transmit data release time (MSPInCSIE = 1)	T_{SSOREL}		—		40	ns

Table 3.68 MSPI Timing (Slave mode: Communication Speed 40MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		25			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 2.5$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}		—		12	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC}/2) - 5$			ns

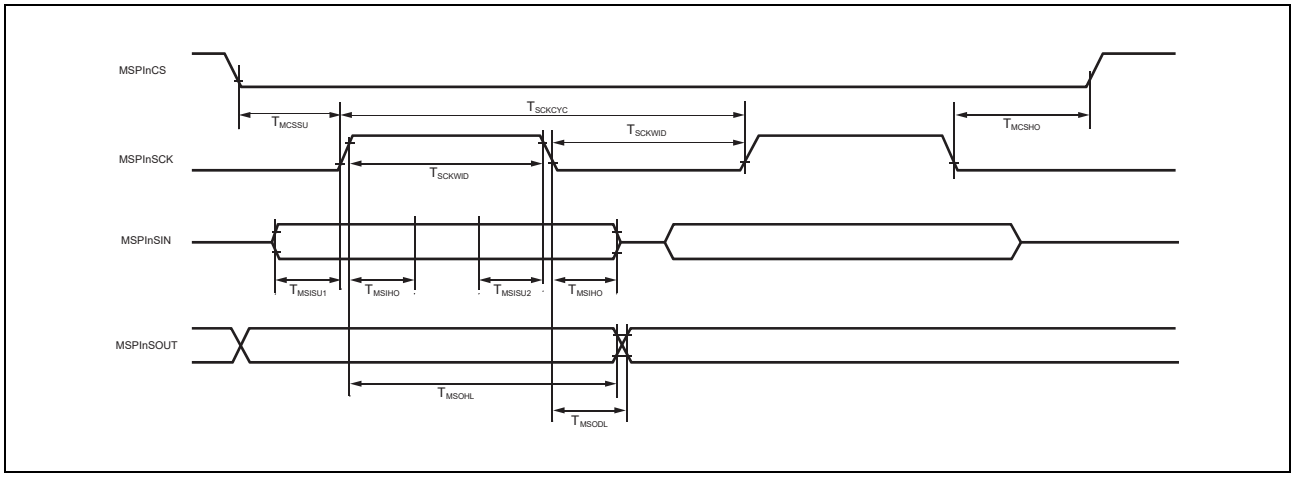


Figure 3.34 MSPIn Timing (Master Mode, MSPInCPHAm = 0)

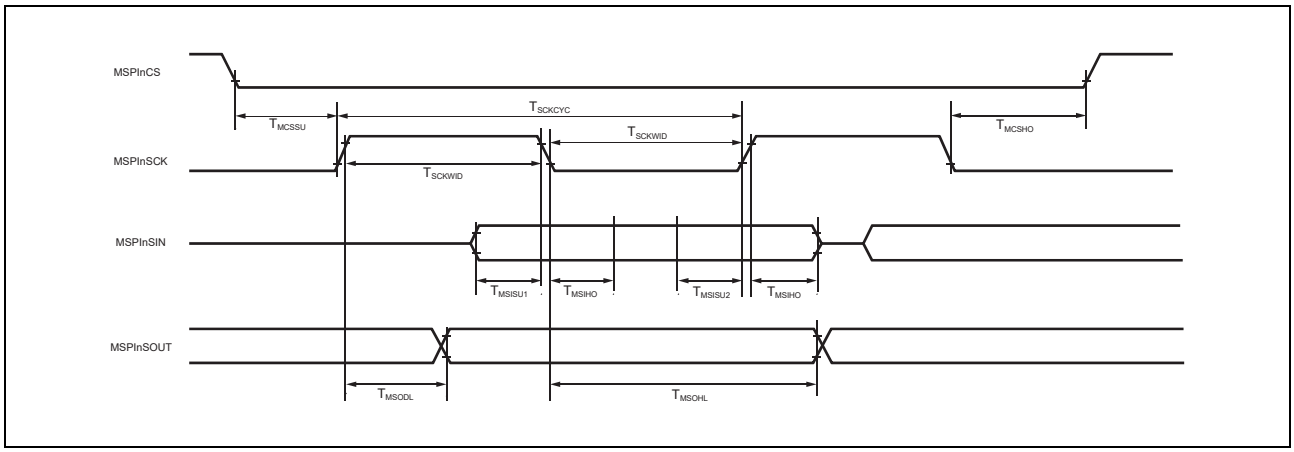


Figure 3.35 MSPIn Timing (Master Mode, MSPInCPHAm = 1)

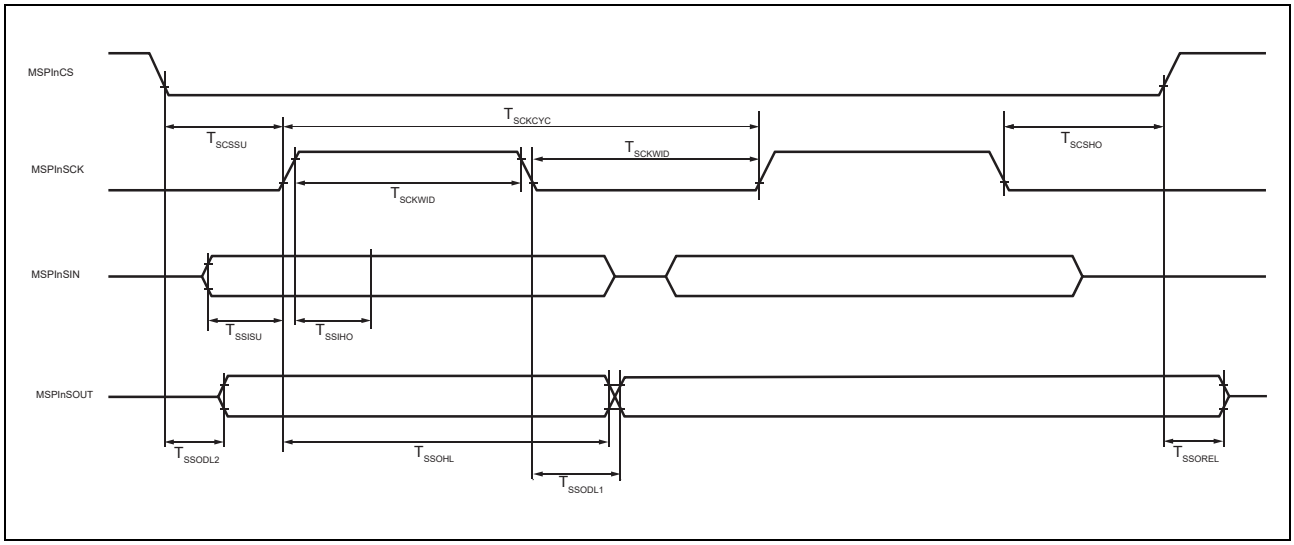


Figure 3.36 MSPIn Timing (Slave Mode, MSPInCPHA0 = 0)

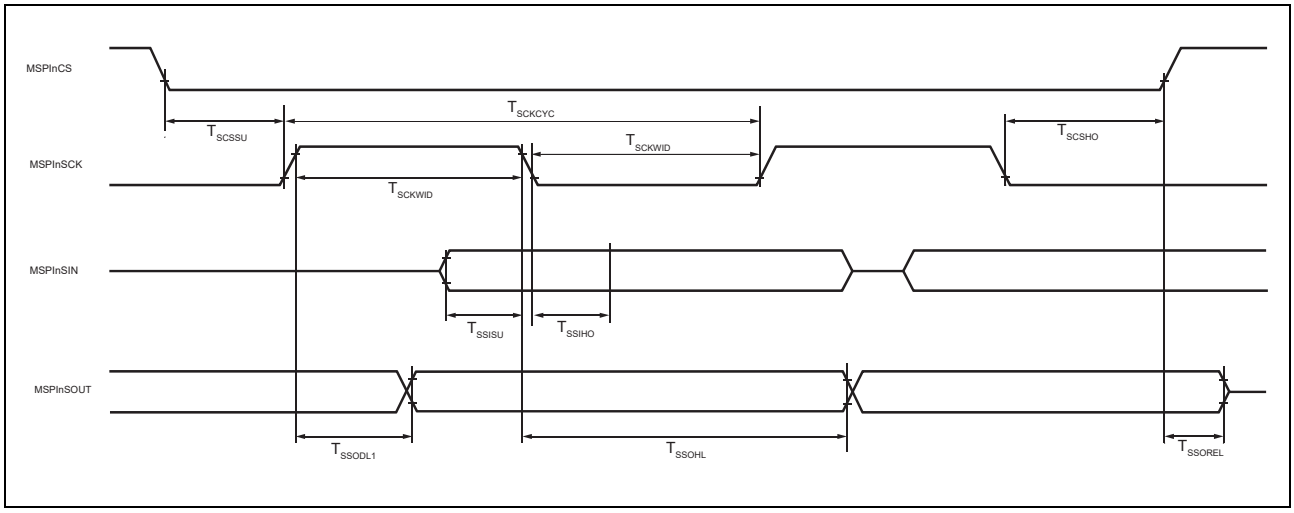


Figure 3.37 MSPIn Timing (Slave Mode, MSPInCPHA0 = 1)

3.3.12 RLIN3 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.69 RLIN3 Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate	r_{RLin}	LIN mode			20	kbps
	r_{RLine}	LIN extended baud rate*1			115.2	kbps
	r_{RLurt}	UART mode (LIN communication clock is 100MHz)			25	Mbps
		UART mode (LIN communication clock is 80MHz)			20	Mbps

Note 1. The LIN extended baud rate is not part of the LIN standard specification.

3.3.13 RIIC Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.70 RIIC Timing (Normal Mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time[*1]	t_{HD}: STA		4.0			µs
RIICnSCL clock low level width	t_{LOW}		4.7			µs
RIICnSCL clock high level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		I^2C mode	0[*2]		[*3]	µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Note 3. If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Table 3.71 RIIC Timing (Fast Mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIICnSCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time[*1]	t_{HD}: STA		0.6			µs
RIICnSCL clock low level width	t_{LOW}		1.3			µs
RIICnSCL clock high level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	I^2C mode	0[*2]		[*5]	µs
Data setup time	t_{SU}: DAT		100[*3]			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		[*4]	ns

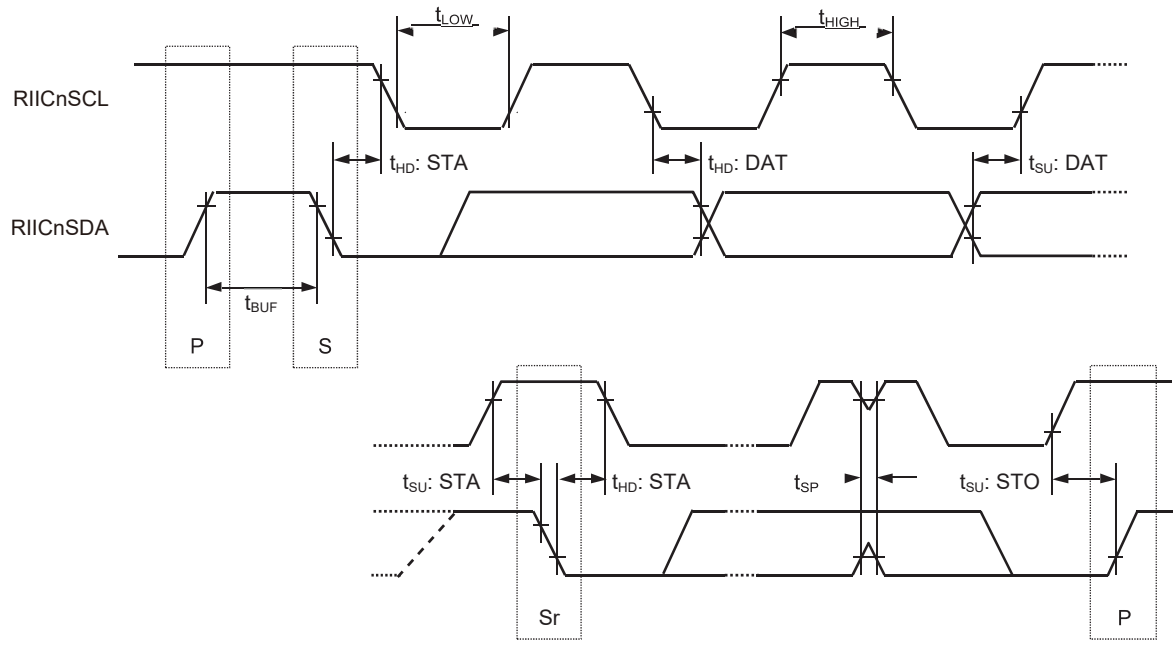
Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIICnSDA signal (at VIH min. of RIICnSCL signal). In order to occupy the undefined area at the falling edge of RIICnSCL.

Note 3. The fast mode I^2C bus can be used in normal mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.
- If the system does not extend the RIICnSCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIICnSCL signal's low state hold time:
Transmit the following data bit to the RIICnSDA line prior to releasing the RIICnSCL line (1250 ns: Normal mode I^2C bus specification).

Note 4. The filtered width is specified by the frequency of IICΦ and the value of RIICnMR3.NF[1:0].

Note 5. If the system does not extend the RIICnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.



Note
P: Stop condition S: Start condition Sr: Restart condition

Figure 3.38 RIIC Timing

3.3.14 RS-CANFD Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.72 RS-CANFD Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	r_{CN1}	Classical CAN mode			1	Mbps
	r_{CN2}	CAN FD mode (nominal bit rate)			1	Mbps
	r_{CN3}	CAN FD mode (data bit rate)			8	Mbps
Internal delay time	t_{DCIN}	$t_{INPUT} + t_{OUTPUT}$			50	ns

Note 1. For the configuration of the transfer speed, see RH850/U2B Group User's Manual:Hardware **Section 24.5.1.3, Baud Rate**.

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

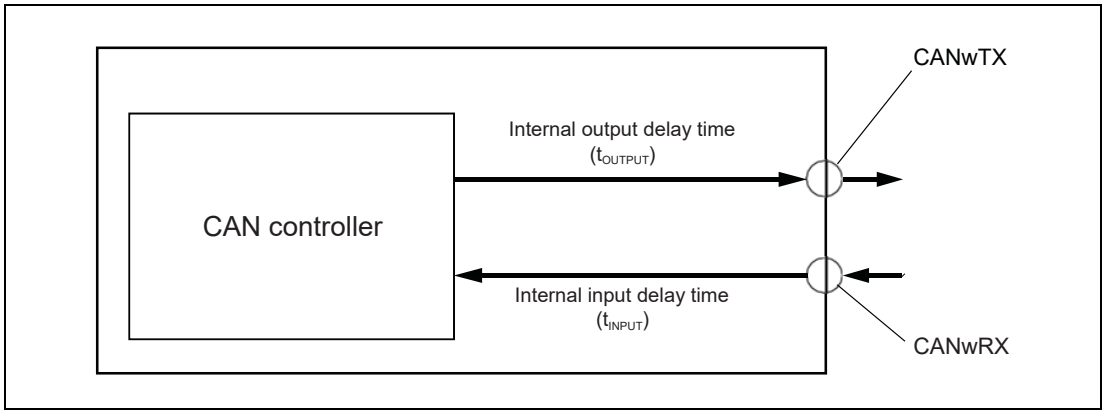


Figure 3.39 RS-CANFD Timing

3.3.15 Reserved

3.3.16 FlexRay Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.73 FlexRay Timing*1 (E0VCC = E1VCC = E2VCC = 3.3 ± 0.3 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	rFLXA				10	Mbps
FLXAnTXDA/B, FLXAnTXENA/B transmit data rise time	t_{CTXr}				4.5	ns
FLXAnTXDA/B, FLXAnTXENA/B transmit data fall time	t_{CTXf}				4.5	ns

Table 3.74 FlexRay Timing*1 (E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	rFLXA				10	Mbps
FLXAnTXDA/B, FLXAnTXENA/B transmit data rise time	t_{CTXr}				4.5	ns
		CL=15pF			2.5	ns
FLXAnTXDA/B, FLXAnTXENA/B transmit data fall time	t_{CTXf}				4.5	ns
		CL=15pF			2.5	ns

Note 1. Base of this specification is “FlexRay Electrical Physical Layer Specification V3.0.1, Oct-2010”

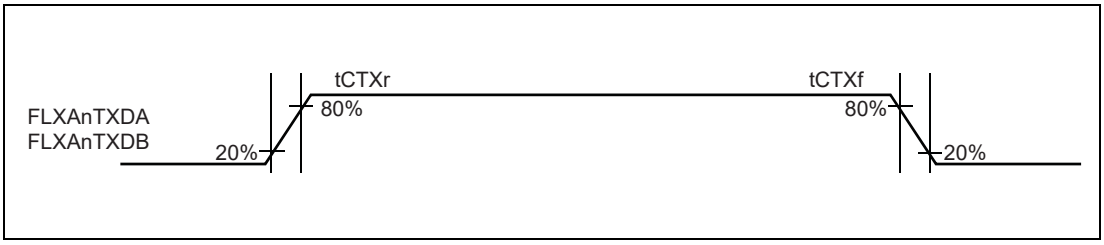


Figure 3.40 FlexRay Timing

3.3.17 RSENT Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4 (Low)
- Buffer type = SHMT1

Table 3.75 RSENT Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3.3.18 Renesas High-speed Serial I/F Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIFn_REFCLK: CL = 15 pF
- Buffer type = SHMT1

Table 3.76 External Reference Clock Input/Output Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
External Reference Clock Input frequency	f_{REFCKI}		10		20	MHz
External Reference Clock Input duty cycle	DCREFCKI		35		65	%
External Reference Clock output frequency	f_{REFCKO}		10		20	MHz
External Reference Clock output duty cycle	DCREFCKO		35		65	%

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIFn_REFCLK: CL = 15 pF
- HSIFn_TXDP, HSIFn_TXDN: CL = 5.0 pF

Table 3.77 RHSIF Transmit Data Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmit data cycle	f_{TX}	Slow mode			5	M Baud
		Fast mode			320	M Baud
Transmit data delay time (HSIFn_REFCLK input)	$t_{REFITXDD}$	Slow mode	0		60	ns
		Fast mode*1				ns
Transmit data delay time (HSIFn_REFCLK output)	$t_{REFOTXDD}$	Slow mode RHSIFnREFCLK	-20		20	ns
		Fast mode*1				ns

Note 1. Asynchronous

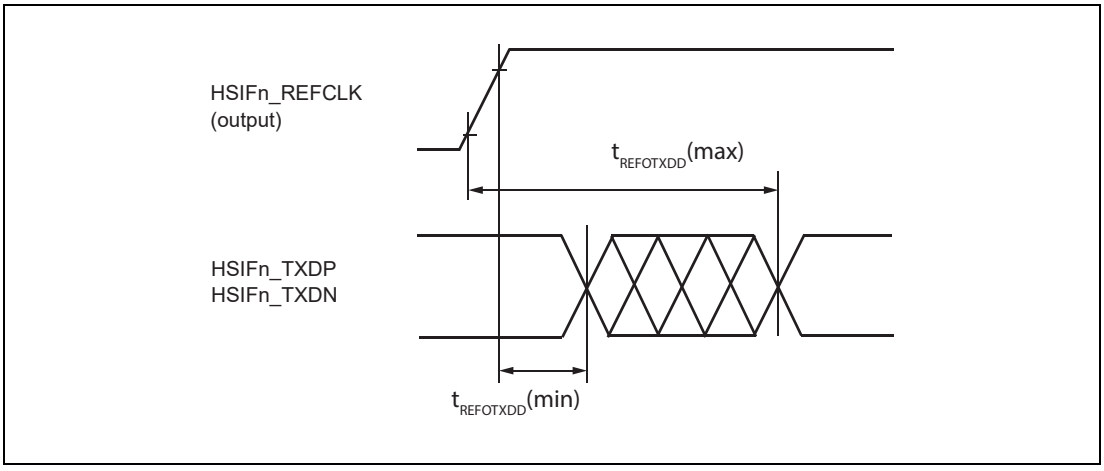


Figure 3.41 RHSIF Transmit Data Timing (HSIFn_REFCLK: output)

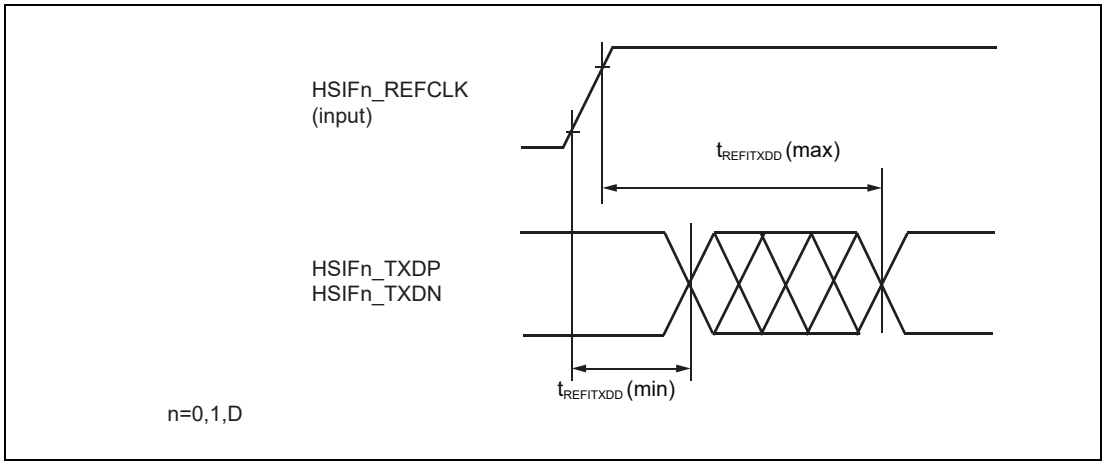


Figure 3.42 RHSIF Transmit Data Timing (HSIF0_REFCLK: input)

Table 3.78 RHSIF Receipt Data Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Receipt data cycle	f_{RX}	Slow mode			5	M Baud
		Fast mode			320	M Baud

3.3.18.1 Renesas High-speed Serial I/F Timing (For debug)

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIFD_REFCLK: Buffer type = TTL

Table 3.79 External Reference Clock Input/Output Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
External Reference Clock Input frequency	f_{REFCKI}		20		20	MHz
External Reference Clock Input duty cycle	DCREFCKI		35		65	%

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIFD_TXDP, HSIFD_TXDN: CL = 5.0 pF

Table 3.80 RHSIF Transmit Data Timing (Debug)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmit data cycle	f_{TX}	Fast mode			320*1	M Baud

Note 1. 320Mbps is not supported by BGA292 package device.

Table 3.81 RHSIF Receipt Data Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Receipt data cycle	f_{RX}	Fast mode			320*1	M Baud

Note 1. 320Mbps is not supported by BGA292 package device.

3.3.19 RHSB Timing

3.3.19.1 MSC mode

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMTMSC

Table 3.82 RHSB Timing LVDS Mode, Up to 80 Mbps

Parameter	Symbol	Condition	MIN.	MAX.	Unit
RHSBnFCL clock cycle	t_{FCLcyc}	CL = 5 pF, CL = 25 pF, CL = 30 pF	12.5	-	ns
RHSBnFCL high-level period	t_{FCLWH}	CL = 5 pF, CL = 25 pF, CL = 30 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns
RHSBnFCL low-level period	t_{FCLWL}	CL = 5 pF, CL = 25 pF, CL = 30 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns
RHSBnSO output delay time *1	t_{SOD}	CL = 5 pF	(DDDC - DFDC) × t_{CLKC} - 3.6	(DDDC - DFDC) × t_{CLKC} + 3.6	ns
		CL = 25 pF	(DDDC - DFDC) × t_{CLKC} - 4.4	(DDDC - DFDC) × t_{CLKC} + 4.4	ns
		CL = 30 pF	(DDDC - DFDC) × t_{CLKC} - 5.8	(DDDC - DFDC) × t_{CLKC} + 5.8	ns
RHSBnCSDx output rising delay time *2	t_{CSDRD}	CL = 5 pF	(DCRDCx - DFDC) × t_{CLKC} - 3.6	(DCRDCx - DFDC) × t_{CLKC} + 3.6	ns
		CL = 25 pF	(DCRDCx - DFDC) × t_{CLKC} - 4.4	(DCRDCx - DFDC) × t_{CLKC} + 4.4	ns
		CL = 30 pF	(DCRDCx - DFDC) × t_{CLKC} - 5.8	(DCRDCx - DFDC) × t_{CLKC} + 5.8	ns
RHSBnCSDx output falling delay time *3	t_{CSDFD}	CL = 5 pF	(DCFDCx - DFDC) × t_{CLKC} - 3.6	(DCFDCx - DFDC) × t_{CLKC} + 3.6	ns
		CL = 25 pF	(DCFDCx - DFDC) × t_{CLKC} - 4.4	(DCFDCx - DFDC) × t_{CLKC} + 4.4	ns
		CL = 30 pF	(DCFDCx - DFDC) × t_{CLKC} - 5.8	(DCFDCx - DFDC) × t_{CLKC} + 5.8	ns
RHSBnSI rise time	t_{SIr}	10 to 90%	-	0.5 × t_{FCLcyc}	ns
RHSBnSI fall time	t_{SIf}	10 to 90%	-	0.5 × t_{FCLcyc}	ns
RHSBnSI 1-bit length	t_{SIW}		8 × t_{FCLcyc}	-	ns

Note 1. This parameter is programable, the value can be set by t_{CLKC}, DFDC and DDDC.
Note 2. This parameter is programable, the value can be set by t_{CLKC}, DFDC and DCRDCx (x = 0, 1).
Note 3. This parameter is programable, the value can be set by t_{CLKC}, DFDC and DCFDCx (x = 0, 1).
Note 4. t_{CLKC} means 1 / (frequency of CLK_RHSB_Cj) (j = 0 to 3).
DFDC means the value which was set to RHSBjDDC2.DFDC[4:0] (j = 0 to 3).
DDDC means the value which was set to RHSBjDDC2.DDDC[4:0] (j = 0 to 3).
DCRDCx means the value which was set to RHSBjDDC0.DCRDCx[4:0] (j = 0 to 3, x = 0, 1).
DCFDCx means the value which was set to RHSBjDDC0.DCFDCx[4:0] (j = 0 to 3, x = 0, 1).

Table 3.83 RHSB Timing Single-ended Mode, Up to 20 Mbps

Parameter	Symbol	Condition	MIN.	MAX.	Unit
RHSBnFCL clock cycle	t_{FCLcyc}	CL = 20 pF	50	-	ns
RHSBnFCL high-level period	t_{FCLWH}	CL = 20 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns
RHSBnFCL low-level period	t_{FCLWL}	CL = 20 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns
RHSBnFCL rise time	t_{FCLr}	10 to 90%	-	0.15 × t_{FCLcyc}	ns
RHSBnFCL fall time	t_{FCLf}	10 to 90%	-	0.15 × t_{FCLcyc}	ns
RHSBnSO output delay time *1	t_{SOD}	CL = 20 pF	(DDDC - DFDC) × t_{CLKC} - 0.25 × t_{FCLcyc}	(DDDC - DFDC) × t_{CLKC} + 0.25 × t_{FCLcyc}	ns
RHSBnCSDx output rising delay time *2	t_{CSDRD}	CL = 20 pF	(DCRDCx - DFDC) × t_{CLKC} - 0.25 × t_{FCLcyc}	(DCRDCx - DFDC) × t_{CLKC} + 0.25 × t_{FCLcyc}	ns
RHSBnCSDx output falling delay time *3	t_{CSDFD}	CL = 20 pF	(DCFDCx - DFDC) × t_{CLKC} - 0.25 × t_{FCLcyc}	(DCFDCx - DFDC) × t_{CLKC} + 0.25 × t_{FCLcyc}	ns
RHSBnSI rise time	t_{SIr}	10 to 90%	-	0.5 × t_{FCLcyc}	ns
RHSBnSI fall time	t_{SIf}	10 to 90%	-	0.5 × t_{FCLcyc}	ns
RHSBnSI 1-bit length	t_{SIW}		8 × t_{FCLcyc}	-	ns

Note 1. This parameter is programable, the value can be set by t_{CLKC}, DFDC and DDDC.

Note 2. This parameter is programable, the value can be set by t_{CLKC}, DFDC and DCRDCx (x = 0, 1).

Note 3. This parameter is programable, the value can be set by t_{CLKC}, DFDC and DCFDCx (x = 0, 1).

Note 4. t_{CLKC} means 1 / (frequency of CLK_RHSB_Cj) (j = 0 to 3).
DFDC means the value which was set to RHSBjDDC2.DFDC[4:0] (j = 0 to 3).
DDDC means the value which was set to RHSBjDDC2.DDDC[4:0] (j = 0 to 3).
DCRDCx means the value which was set to RHSBjDDC0.DCRDCx[4:0] (j = 0 to 3, x = 0, 1).
DCFDCx means the value which was set to RHSBjDDC0.DCFDCx[4:0] (j = 0 to 3, x = 0, 1).

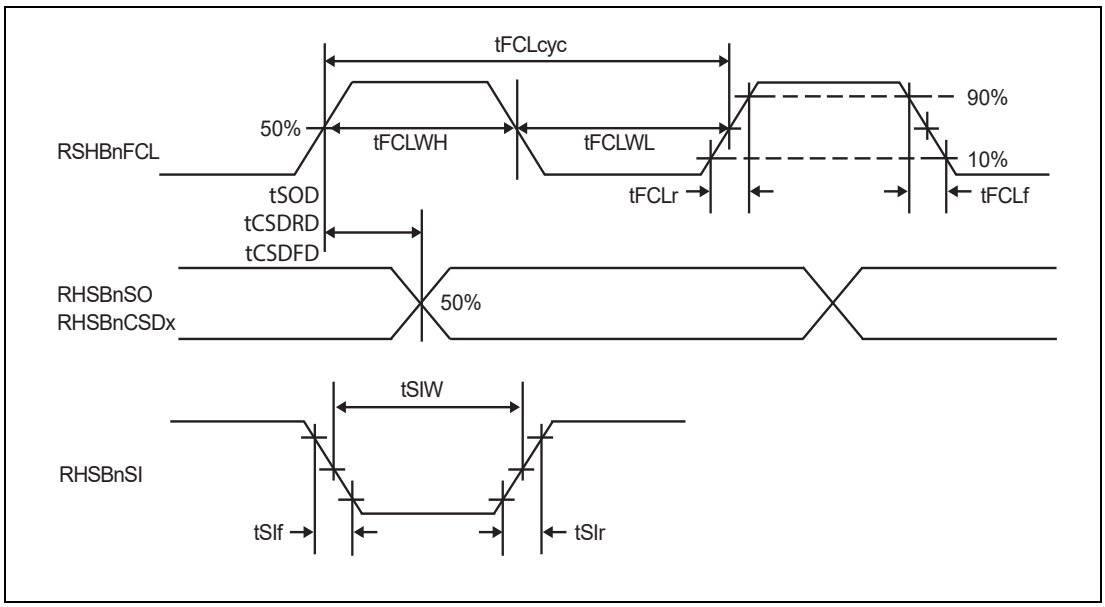


Figure 3.43 RHSB Timing MSC mode

3.3.19.2 MSC-Plus mode

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMTMSC

Table 3.84 RHSB Timing (Manchester mode)

Parameter	Symbol	Condition	Min.	Max.	Unit
Bit rate	—	RHSB0, RHSB3	—	80	Mbps
	—	RHSB1, RHSB2	—	40	Mbps

Table 3.85 RHSB0, RHSB3 Timing LVDS Mode, Up to 80 Mbps (Non-Manchester mode)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
RHSBnNMFCL clock cycle	$t_{NMFCLcyc}$	CL = 5 pF, CL = 25 pF, CL = 30 pF	12.5	-	ns
RHSBnNMFCL high-level period	$t_{NMFCLWH}$	CL = 5 pF, CL = 25 pF, CL = 30 pF	0.45 × $t_{NMFCLcyc}$	0.55 × $t_{NMFCLcyc}$	ns
RHSBnNMFCL low-level period	$t_{NMFCLWL}$	CL = 5 pF, CL = 25 pF, CL = 30 pF	0.45× $t_{NMFCLcyc}$	0.55 × $t_{NMFCLcyc}$	ns
RHSBnNMSO / RHSBnNMEN output delay time	t_{NMSOD}	CL = 5 pF	-3.6	3.6	ns
		CL = 25 pF	-4.4	4.4	ns
		CL = 30 pF	-5.8	5.8	ns

Table 3.86 RHSB1, RHSB2 Timing LVDS Mode, Up to 40 Mbps (Non-Manchester mode)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
RHSBnNMFCL clock cycle	$t_{NMFCLcyc}$	CL = 5 pF, CL = 25 pF, CL = 30 pF	25	-	ns
RHSBnNMFCL high-level period	$t_{NMFCLWH}$	CL = 5 pF, CL = 25 pF, CL = 30 pF	0.45 × $t_{NMFCLcyc}$	0.55 × $t_{NMFCLcyc}$	ns
RHSBnNMFCL low-level period	$t_{NMFCLWL}$	CL = 5 pF, CL = 25 pF, CL = 30 pF	0.45× $t_{NMFCLcyc}$	0.55 × $t_{NMFCLcyc}$	ns
RHSBnNMSO / RHSBnNMEN output delay time	t_{NMSOD}	CL = 5 pF	-7.2	7.2	ns
		CL = 25 pF	-8.8	8.8	ns
		CL = 30 pF	-11.6	11.6	ns

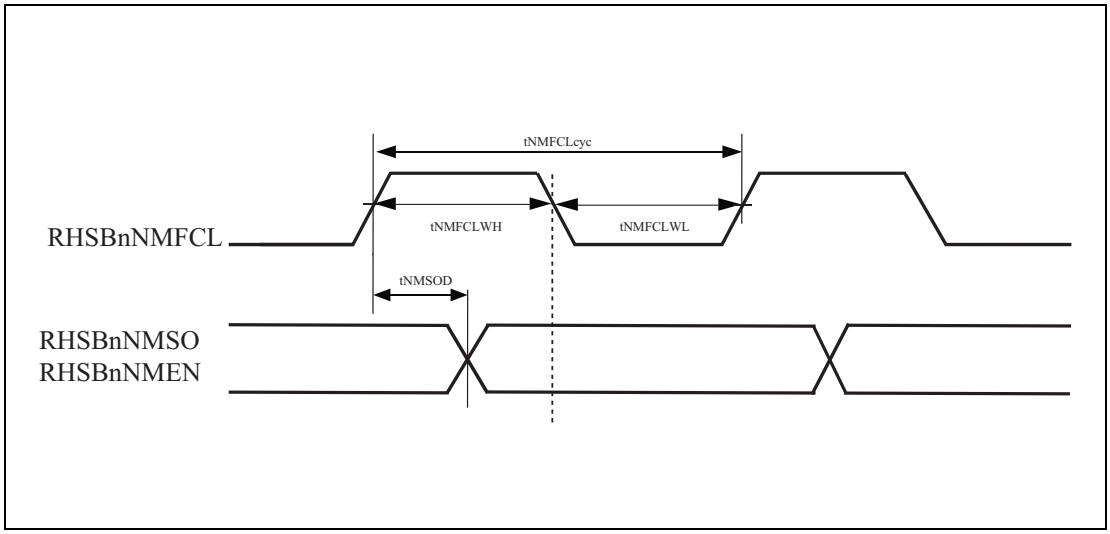


Figure 3.44 RHSB Timing for Non-Manchester (MSC plus mode)

3.3.20 Ethernet Timing

3.3.20.1 MII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Buffer type = TTL

Table 3.87 Ethernet Timing – 10 Mbit/s MII Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	t_{MTC}		400 – 100 ppm	400	400 + 100 ppm	ns
ETHn_MII_TX_CLK high width	t_{MTCH}	*1	140	200	260	ns
ETHn_MII_TX_CLK low width	t_{MTCL}	*1	140	200	260	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		0		25	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		0		25	ns
ETHn_MII_RX_CLKwidth	t_{MRC}		400 – 100 ppm	400	400 + 100 ppm	ns
ETHn_MII_RX_CLK high width	t_{MRCH}	*1	140	200	260	ns
ETHn_MII_RX_CLK low width	t_{MRCL}	*1	140	200	260	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		10			ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		10			ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Cload = 15 pF
- Drive strength = 2
- Buffer type = TTL

Table 3.88 Ethernet Timing – 100 Mbit/s MII Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	t_{MTC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETHn_MII_TX_CLK high width	t_{MTCH}	*1	14	20	26	ns
ETHn_MII_TX_CLK low width	t_{MTCL}	*1	14	20	26	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		0		25	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		0		25	ns
ETHn_MII_RX_CLKwidth	t_{MRC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETHn_MII_RX_CLK high width	t_{MRCH}	*1	14	20	26	ns
ETHn_MII_RX_CLK low width	t_{MRCL}	*1	14	20	26	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		10			ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		10			ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65%inclusive (IEEE802.3).

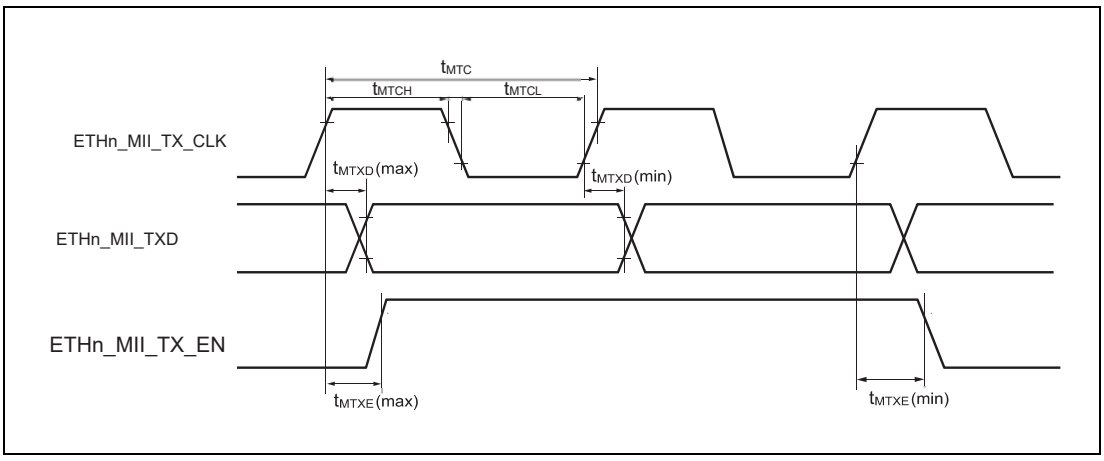


Figure 3.45 Ethernet Timing – MII Transmitter

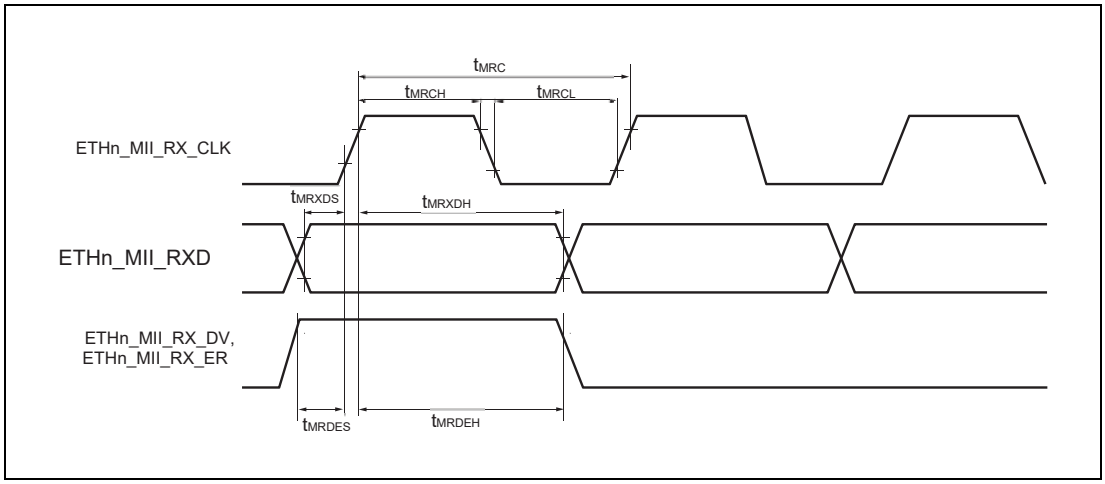


Figure 3.46 Ether net Timing – MII Receiver

3.3.20.2 Reverse-PHY MII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Drive strength = 2 (High)
- Buffer type = TTL

Table 3.89 10 Mbit/s MII (Reverse MII MAC mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	tMTC		400 - 1%		400 + 1%	ns
ETHn_MII_TX_CLK high level width	tMTCH	*1	140		260	ns
ETHn_MII_TX_CLK low level width	tMTCL	*1	140		260	ns
ETHn_MII_TXD [3:0] delay time	tMTXD		0		20	ns
ETHn_MII_TX_EN delay time	tMTXE		0		20	ns
ETHn_MII_RX_CLK width	tMRC		400 - 1%		400 + 1%	ns
ETHn_MII_RX_CLK high level width	tMRCH	*1	140		260	ns
ETHn_MII_RX_CLK low level width	tMRCL	*1	140		260	ns
ETHn_MII_RXD [3:0] setup time	tMRXDS		10			ns
ETHn_MII_RXD [3:0] hold time	tMRXDH		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	tMRDES		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	tMRDEH		10			ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Table 3.90 10 Mbit/s MII (Reverse MII PHY mode) (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) width	tMTC		400 - 1%		400 + 1%	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) high level width	tMTCH	*1, *2	140		260	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) low level width	tMTCL	*1, *2	140		260	ns
ETHn_MII_TXD [3:0] delay time	tMTXD		10		28	ns
ETHn_MII_TX_EN delay time	tMTXE		10		28	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK)width	tMRC		400 - 1%		400 + 1%	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) high level width	tMRCH	*1, *2	140		260	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) low level width	tMRCL	*1, *2	140		260	ns
ETHn_MII_RXD [3:0] setup time	tMRXDS		18			ns

Table 3.90 10 Mbit/s MII (Reverse MII PHY mode) (2/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_RXD [3:0] hold time	tMRXDH		0			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	tMRDES		18			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	tMRDEH		0			ns

Note 1. The duty cycle of ETHn_MII_TX_CLK and ETHn_MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Note 2. When MII PHY mode, ETHn_MII_TX_CLK and ETHn_MII_RX_CLK all are ETHn_RevMII_CLK pin

Table 3.91 100 Mbit/s MII (Reverse MII MAC mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	tMTC		40 - 1%		40 + 1%	ns
ETHn_MII_TX_CLK high level width	tMTCH	*1	14		26	ns
ETHn_MII_TX_CLK low level width	tMTCL	*1	14		26	ns
ETHn_MII_TXD [3:0] delay time	tMTXD		0		20	ns
ETHn_MII_TX_EN delay time	tMTXE		0		20	ns
ETHn_MII_RX_CLK width	tMRC		40 - 1%		40 + 1%	ns
ETHn_MII_RX_CLK high level width	tMRCH	*1	14		26	ns
ETHn_MII_RX_CLK low level width	tMRCL	*1	14		26	ns
ETHn_MII_RXD [3:0] setup time	tMRXDS		10		-	ns
ETHn_MII_RXD [3:0] hold time	tMRXDH		10		-	ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	tMRDES		10		-	ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	tMRDEH		10		-	ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Table 3.92 100 Mbit/s MII (Reverse MII PHY mode) (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) width	tMTC		40 - 1%		40 + 1%	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) high level width	tMTCH	*1, *2	14		26	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) low level width	tMTCL	*1, *2	14		26	ns
ETHn_MII_TXD [3:0] delay time	tMTXD		10		28	ns
ETHn_MII_TX_EN delay time	tMTXE		10		28	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK)width	tMRC		40 - 1%		40 + 1%	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) high level width	tMRCH	*1, *2	14		26	ns

Table 3.92 100 Mbit/s MII (Reverse MII PHY mode) (2/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) low level width	tMRCL	*1, *2	14		26	ns
ETHn_MII_RXD [3:0] setup time	tMRXDS		18		-	ns
ETHn_MII_RXD [3:0] hold time	tMRXDH		0		-	
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	tMRDES		18		-	
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	tMRDEH		0		-	

Note 1. The duty cycle of ETHn_MII_TX_CLK and ETHn_MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Note 2. When MII PHY mode, ETHn_MII_TX_CLK and ETHn_MII_RX_CLK all are ETHn_RevMII_CLK pin.

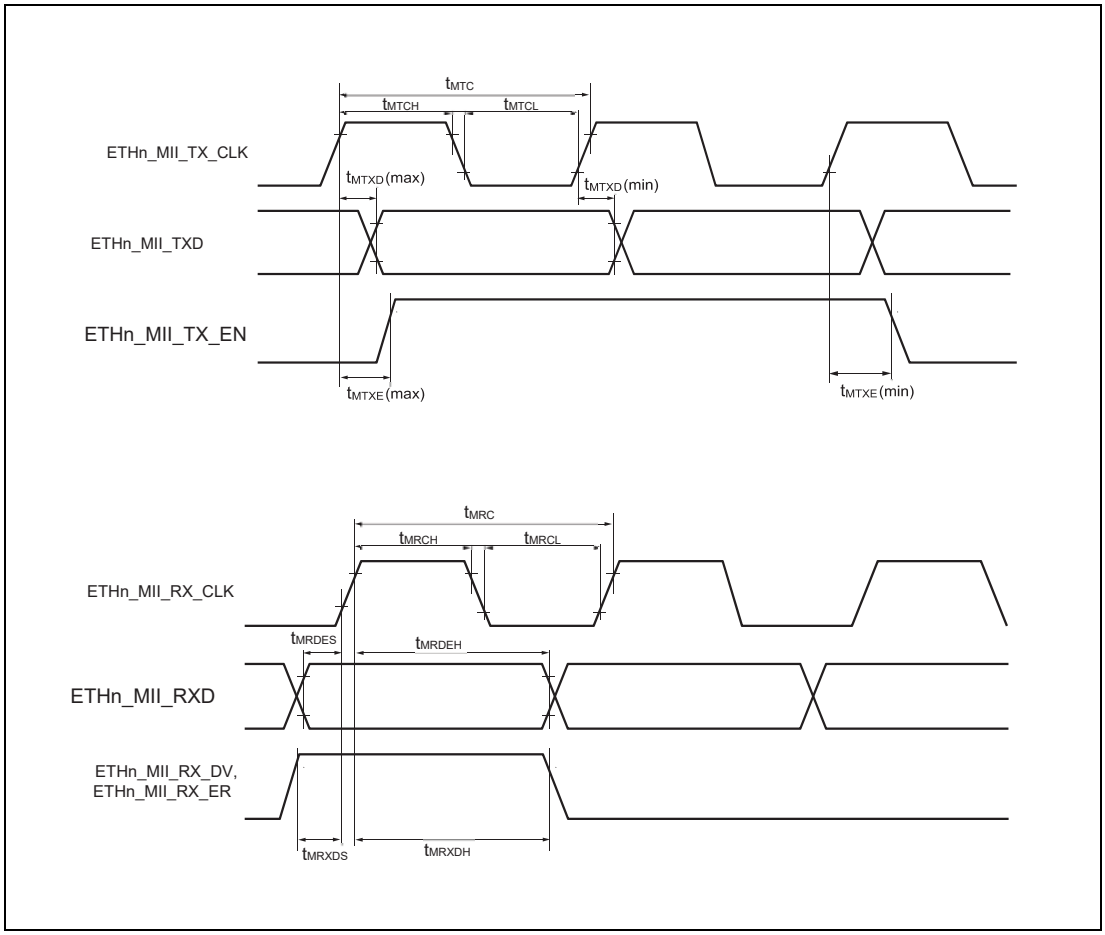


Figure 3.47 Ethernet Timing – Reverse-PHY MII

3.3.20.3 RMII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Drive strength = 2 (High)
- Buffer type = TTL

Table 3.93 Ethernet Timing – RMII Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNCnREF50CK width	t_{RMC}		20 – 50 ppm	20	20 + 50 ppm	ns
ETNCnREF50CK high width	t_{RMCH}	*1, *2	7		13	ns
ETNCnREF50CK low width	t_{RMCL}	*1, *2	7		13	ns
ETHn_RMII_RXD [1:0], ETHn_RMII_RX_DV and ETHn_RMII_RX_ER setup time	t_{RMS}		4			ns
ETHn_RMII_RXD [1:0], ETHn_RMII_RX_DV and ETHn_RMII_RX_ER hold time	t_{RMH}		2			ns
ETHn_RMII_TXD [1:0], ETHn_RMII_TX_EN output delay time	t_{RMD}		2		16	ns

Note 1. The duty cycle of ETNC0REF50CK shall be between 35 to 65% inclusive (RMIITM specification).
Note 2. ETNCnREF50CK is same with ETHn_MII_TX_CLK pin in RMII mode

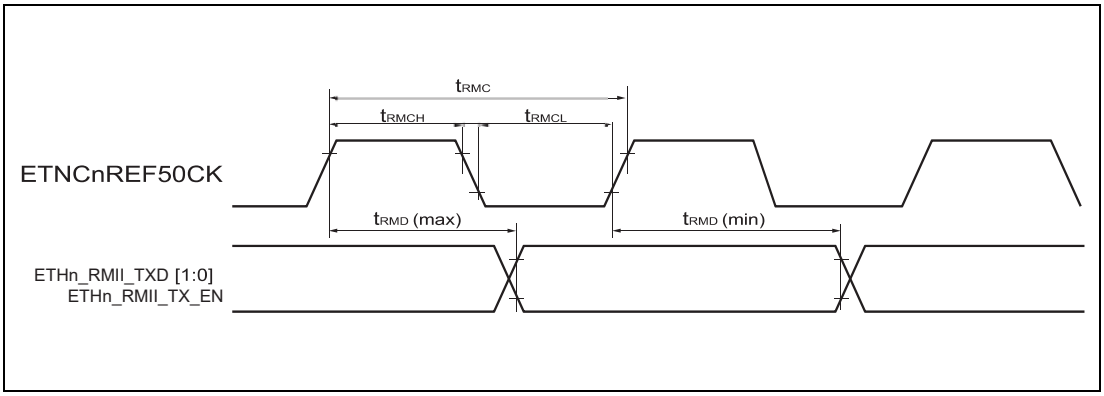


Figure 3.48 Ethernet Timing – RMII Transmitter

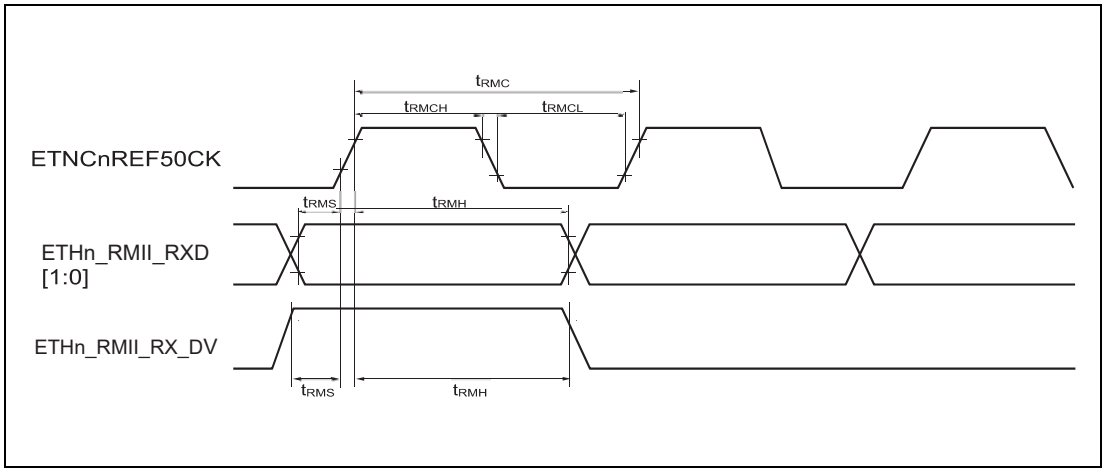


Figure 3.49 Ethernet Timing – RMII Receiver

3.3.20.4 SGMII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**[*2].

Table 3.94 Ethernet Timing – SGMII REFCK Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock input frequency	t_{CIF}		40 – 100 ppm		40 + 100 ppm	ns
Clock input duty cycle	t_{CIDC}		45		55	%
Clock input rising/falling time (20%-80%)	t_{CIRFT}				3	ns
Clock Input Total jitter (Dj+ 14* rms Random jitter)	t_{CITJ}				73[*1]	ps peak to peak

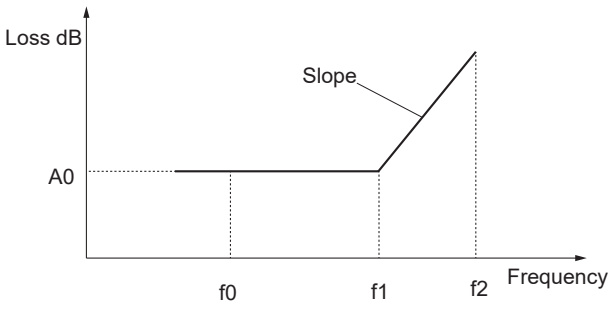
Note 1. 12 kHz to 20 MHz rms jittrer = 3ps.

Note 2. No CL defenition in this chapter.

Table 3.95 Ethernet Timing – SGMII Tx buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Signaling speed	t_{SS}		1.25 – 100 ppm		1.25 + 100 ppm	GBd
Total output jitter (Dj+14*rms random jitter)	t_{TOJ}				300	ps peak to peak
VOD rise/fall time (20% - 80%)	t_{VRFT}		60		250	ps
Differential output return loss (min)	DORL				[*1]	dB

Note 1. See the **Figure 3.50, Differential output return loss** for the detail of differential output return loss.



Parameter value		Unit
A0	-8	dB
f0	50	MHz
f1	0.625	GHz
f2	1.25	GHz
Slope	10	dB/dec

Figure 3.50 Differential output return loss

Table 3.96 Ethernet Timing – SGMII Rx buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Signaling speed	t_{SS}		1.25 – 100 ppm		1.25 + 100 ppm	GBd
Total input jitter tolerance (Dj+14*rms random jitter)	t_{TIJT}				400	ps peak to peak

Table 3.97 Ethernet Timing – Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SGMII power stabilization time	t_{SPST}				1.2	ms

3.3.20.5 Management Interface

Timing of management interface (ETHn_MDC and ETHn_MDIO) depends on software. It is necessary to adjust wait time according to AC specification of PHY.

3.3.21 PSI5 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4 (Low)
- Buffer type = SHMT1

Table 3.98 PSI5 Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bit time		125 kbps (Low speed)	7.6	8.0	8.4	µs
		189 kbps (High speed)	5.0	5.3	5.6	µs
		250 kbps (PAS compatibility)	3.8	4.0	4.2	µs
Gap time		125 kbps (Low speed)	8.4			µs
		189 kbps (High speed)	5.6			µs
		250 kbps (PAS compatibility)	2.0			µs

3.3.22 Reserved

3.3.23 PSI5-S Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.99 PSI5-S Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PSI5-S transfer rate	r_{PSI5S1}	PSI5-S mode			5.33	Mbps
	r_{PSI5S2}	UART mode			5.33	Mbps
Output clock cycle	$t_{PSIScyc}$	PSI5-S mode	37.5			ns
Output clock pulse width	$t_{PSISCKW}$	PSI5-S mode	0.3 × $t_{PSIScyc}$		0.5 × $t_{PSIScyc}$	ns

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file *"Limited_conditions_for_AC_specification.xlsx"*.

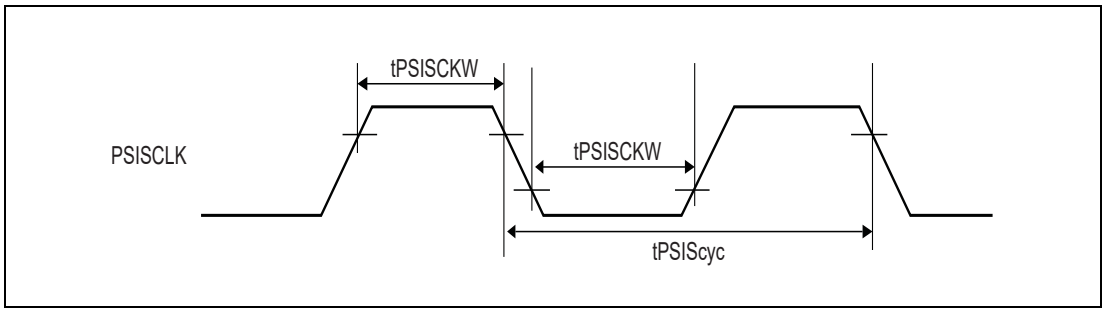


Figure 3.51 PSI5-S Clock Output Timing

3.3.24 Timer Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.100 Timer Input Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t_{WTDIH}		(S + 1) x 1/fs*1			ns
TAUDnIm input low level width	t_{WTDIL}		(S + 1) x 1/fs*1			ns
TAUDnIm pulse rejection width*2	t_{WTDRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
TAUJnIm input high level width	t_{WTJIH}	Analog noise filter	600*3			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAUJnIm input low level width	t_{WTJIL}	Analog noise filter	600*3			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAUJnIm pulse rejection width*2	t_{WTJRJ}	Analog noise filter	100		600*3	ns
		Digital noise filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
TAPAnESO input high level width*4	t_{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAPAnESO input low level width*4	t_{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs*1			ns
TAPAnESO pulse rejection width*2, *4	t_{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
ENCAnTINm input high level width	t_{WENIH}		(S + 1) x 1/fs*1			ns
ENCAnTINm input low level width	t_{WENIL}		(S + 1) x 1/fs*1			ns
ENCAnTINm pulse rejection width*2	t_{WENRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI high level width	t_{WTGIH}		(S + 1) x 1/fs*1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI low level width	t_{WTGIL}		(S + 1) x 1/fs*1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI pulse rejection width*2	t_{WTGRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLKC_HSB (others)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not.
This characteristic is not tested in production.

Note 3. When CLK_LSOSC is selected by CKS_ATAUJC register, at least one clock period of CLK_LSOSC (4.6 µs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 µs width may be rejected.

Note 4. By-pass of filter is possible. For detail, see RH850/U2B Group User's Manual:Hardware **Section 2.7.2.11, ANF/DNF Type F1**.

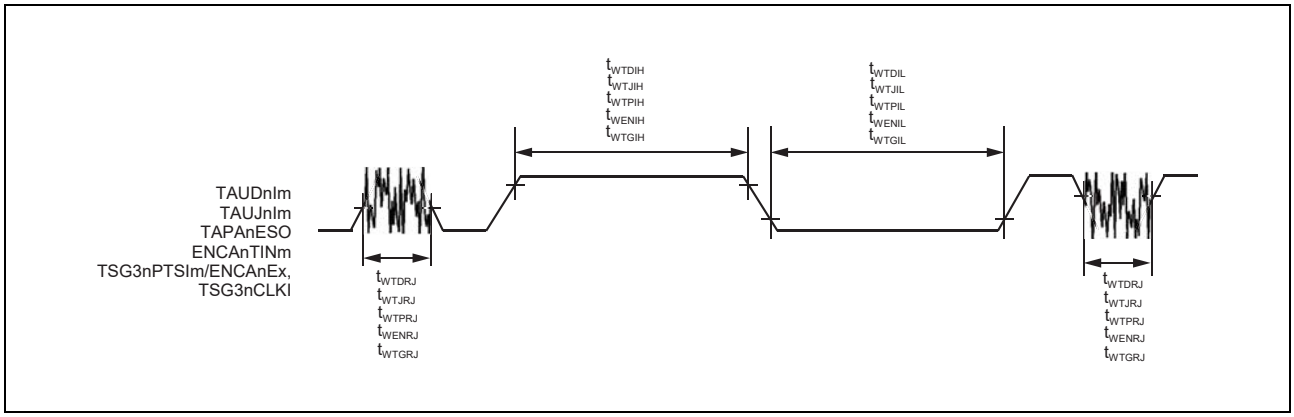


Figure 3.52 Timer Input Timing

3.3.25 GTM Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.101 GTM Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
GTM input high level width	t_{WGTIH}		4 × Tsamp*1			ns
GTM input low level width	t_{WGTIL}		4 × Tsamp*1			ns
GTM output cycle time	t_{CYGTO}		25			ns
GTMECLKn output cycle	$t_{CYGTECLK}$		25			ns
GTMECLKn output high level width	t_{WGTOH}	Z/N*2*3: Integer value	$t_{CYGTECLK}$ / 2 - 4			ns
		Z/N*2*3: Indivisible value	$t_{CYGTECLK}$ / 2 x (2Z/N - 1) / (2Z/N) - 4			ns
GTMECLKn output low level width	t_{WGTOL}	Z/N*2*3: Integer value	$t_{CYGTECLK}$ / 2 - 4			ns
		Z/N*2*3: Indivisible value	$t_{CYGTECLK}$ / 2 x (2Z/N - 1) / (2Z/N) - 4			ns

Note 1. Tsamp = $1/f_{CLK\_GTM}$

Note 2. “Z” is the value of “Numerator for external clock divider” by CMU_ECLK_[z]_NUM register.

Note 3. “N” is the value of “Denominator for external clock divider” by CMU_ECLK_[z]_DEN register.

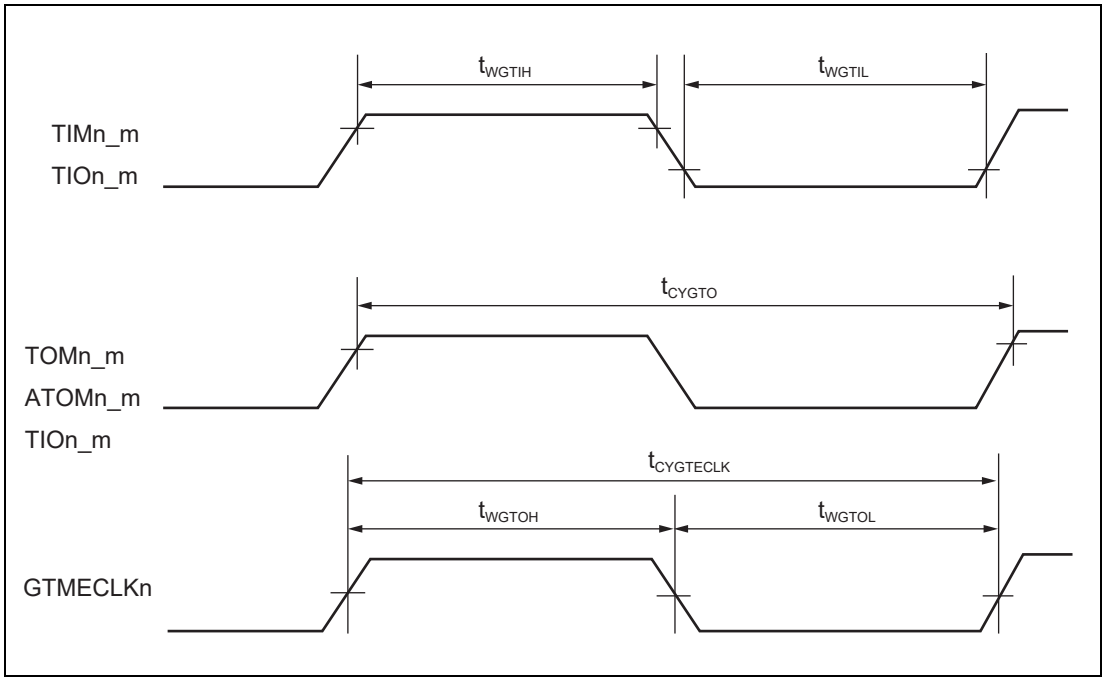


Figure 3.53 GTM Timing

3.3.26 HRPWM Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.102 HRPWM Timing

Parameter	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	-	80	-	200	MHz
Resolution	HRPWM_CLK=80MHz	-	390	-	ps
	HRPWM_CLK=160MHz	-	195	-	ps
	HRPWM_CLK=200MHz	-	156	-	ps
Pulse width of input PWM	Input of pico sec delay	2	-	-	Cycle (HRPWM_CLK)
DLL Lockup time（OFF->ON)		-	-	30	us

3.3.27 Emergency shut-Off (ESO) Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.103 ESO Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ATOMn_m(N)(_H) Hi-z delay time	t_{DESO}				50	ns

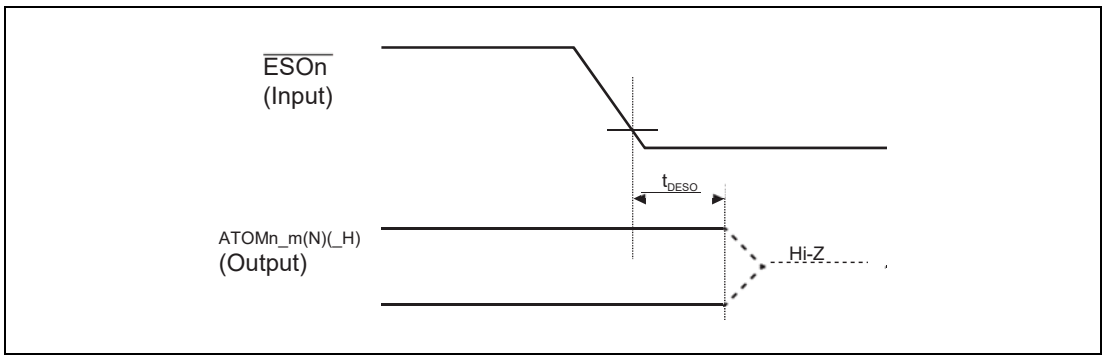


Figure 3.54 ESO Timing

3.3.28 Debug Reset Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.104 Debug Reset Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{TRST}}$ input low level width	t_{WTRL}		600			ns
$\overline{\text{TRST}}$ pulse rejection[*1]	t_{WTRRJ}		100		600	ns
Aurora reset hold time at emulation power-on	$t_{AURORESH}$		2.4	-	-	µs
Aurora reset noise cancel width	$t_{ARESNCW}$		0.2	-	1.2	µs
$\overline{\text{AURORES}}$ input low level width	t_{WARSL}		600			ns
$\overline{\text{AURORES}}$ pulse rejection width[*1]	t_{WARRJ}		100		600	ns

Note 1. Input pulses shorter than the given min. value will be filtered out (resulting in no interrupt detected). Input pulses between min. and max. value result in an undefined interrupt request signal condition (i.e. pulses might be filtered out or not).

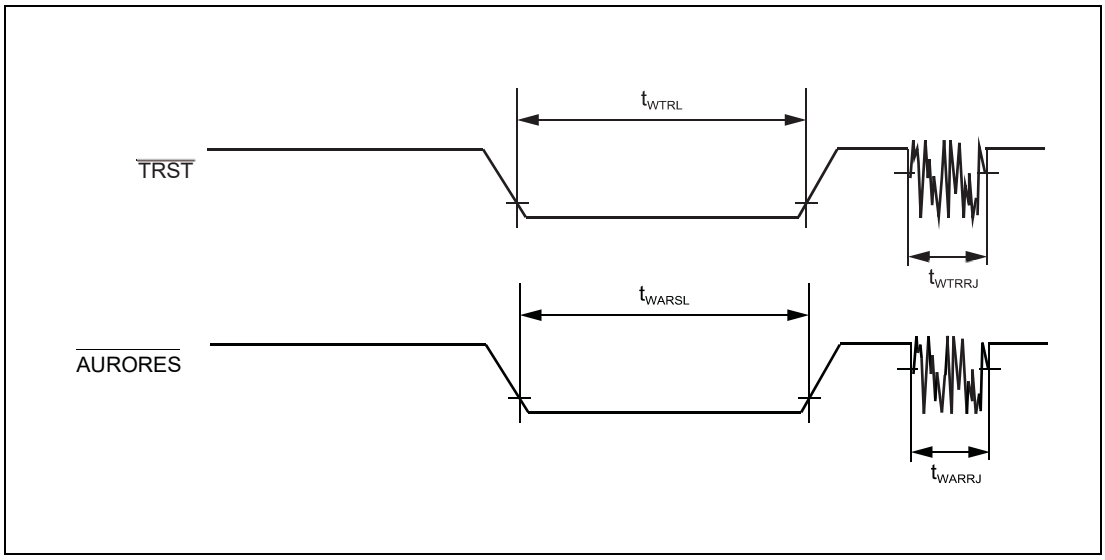


Figure 3.55 Debug Reset Timing

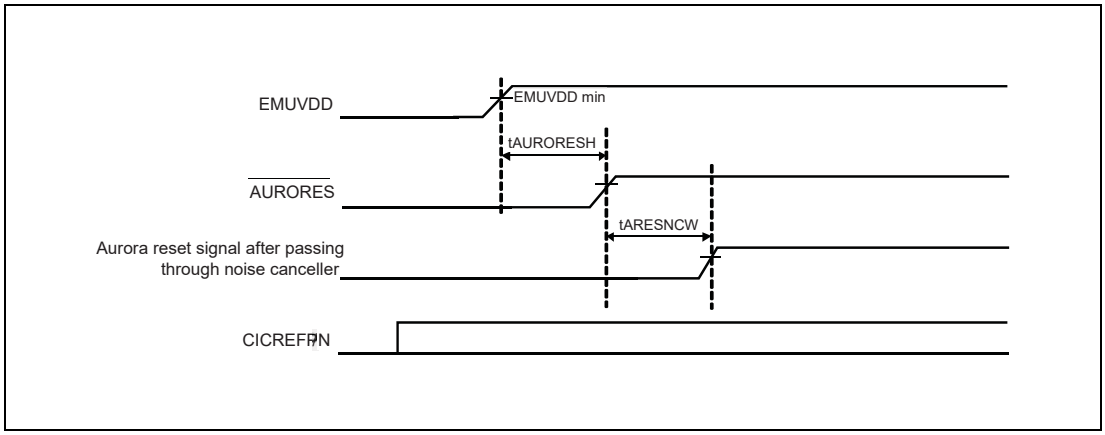


Figure 3.56 Aurora Reset Timing

3.3.29 Debug Interface Mode Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.105 Debug Interface Mode Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TCK (JP0_2) input timing before $\overline{\text{TRST}}$	$t_{DBGIFSWCK}$		$10 \times t_{LPDCKCYC}$ $10 \times t_{TCKW}$			ns
TDI (JP0_0) setup time	$t_{DBGIFSWS}$		$10 \times t_{LPDCKCYC}$ $10 \times t_{TCKW}$			ns
TDI (JP0_0) hold time	$t_{DBGIFSWH}$		2			µs

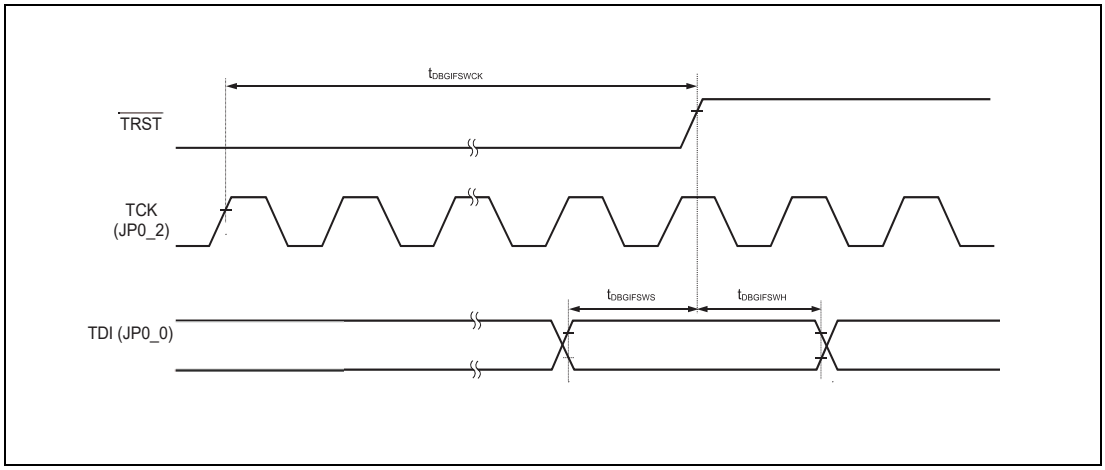


Figure 3.57 Debug Interface Mode Timing

3.3.30 JTAG/Nexus Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive Strength = 2 (fast)
- Buffer type = TTL

Table 3.106 Nexus Interface Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK Cycle width	t_{TCKW}		25			ns
TCK high level width	t_{TCKWH}		10			ns
TCK low level width	t_{TCKWL}		10			ns
TMS/TDI setup time	t_{TISU}		6			ns
TMS/TDI hold time	t_{TIH}		6			ns
TDO output delay time	t_{TDOD}				14	ns
$\overline{RDY}$ delay time	t_{RDYD}				14	ns
TCK/$\overline{TRST}$/TMS/TDI input rising time	t_{TIR}				4	ns
TCK/$\overline{TRST}$/TMS/TDI input falling time	t_{TIF}				4	ns

Note: EVA product can be switched to JTAG/Nexus Interface or LPD (4pin) Interface by DBGSEL1/0.
JP1_0 (TDI/LPDI)
JP1_1 (TDO/LPDO)
JP1_2 (TCK/LPDCLKI)
JP1_3 ($\overline{TMS}$)
JP1_5 ($\overline{RDY}$/LPDCLKO)

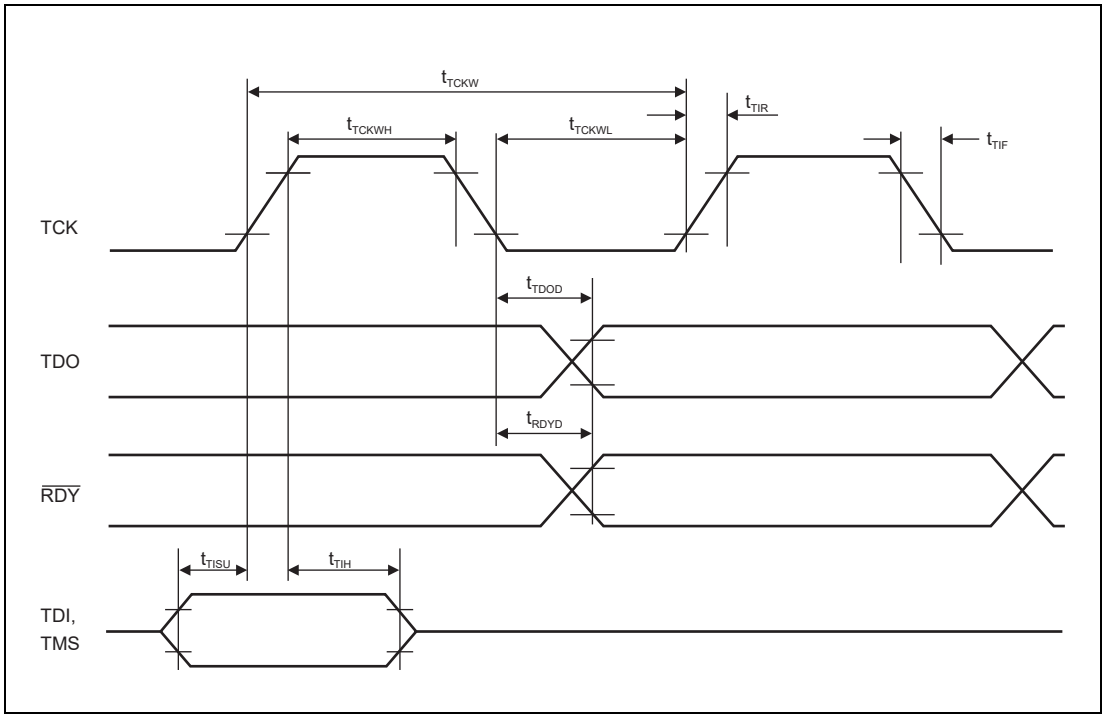


Figure 3.58 Nexus Interface Timing

3.3.31 JTAG/DFP Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive Strength = 2 (fast)
- Buffer type=TTL

Table 3.107 DFP Interface Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK Cycle width	t_{TCKW}		50			ns
TCK high level width	t_{TCKWH}		21			ns
TCK low level width	t_{TCKWL}		21			ns
TMS/TDI setup time	t_{TISU}		6			ns
TMS/TDI hold time	t_{TIH}		6			ns
TDO output delay time	t_{TDOD}				20	ns
TCK/$\overline{\text{TRST}}$/TMS/TDI input rising time	t_{TIR}				4	ns
TCK/$\overline{\text{TRST}}$/TMS/TDI input falling time	t_{TIF}				4	ns

Note: EVA product can be switched to JTAG/ DFP Interface or LPD (4pin) Interface by DBGSEL1/0.
JP1_0 (TDI/LPDI)
JP1_1 (TDO/LPDO)
JP1_2 (TCK/LPDCLKI)
JP1_3 (TMS)

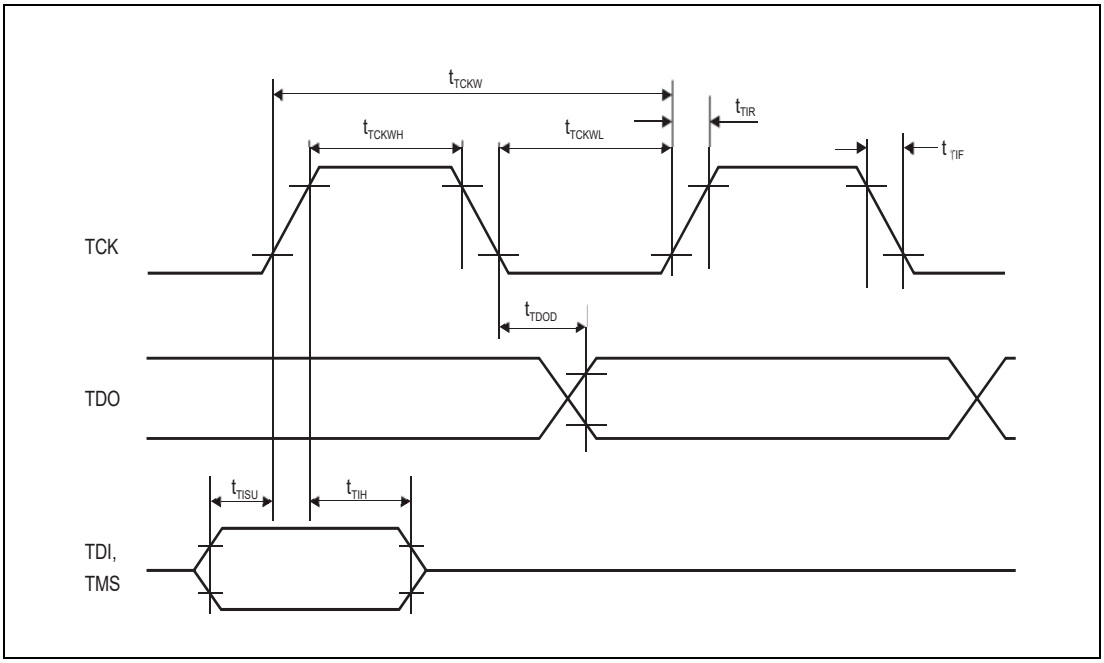


Figure 3.59 DFP Interface Timing

3.3.32 LPD (4pin) Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = TTL

Table 3.108 LPD (4pin) Interface Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLKI cycle time	$t_{LPDCKCYC}$		25			ns
LPDCLKI high/low level width	t_{LPDCKW}		4.5			ns
LPDCLKI input rising/falling time	$t_{LPDCKRF}$				8	ns
LPDI setup time	t_{LPDSU}		3			ns
LPDI hold time	t_{LPDH}		3			ns
LPDCLKO cycle time	$t_{LPDCKOCYC}$		25			ns
LPDCLKO high/low level width	$t_{LPDCKOW}$		t_{LPDCKW} - 2			ns
LPDCLKI to LPDCLKO delay time	$t_{LPDCKOD}$				44	ns
LPDO output delay	t_{LPDOD}		0		18	ns

Note: EVA product can be switched to JTAG/Nexus Interface or LPD (4pin) Interface by DBGSEL1/0.
JP1_0 (TDI/LPDI)
JP1_1 (TDO/LPDO)
JP1_2 (TCK/LPDCLKI)
JP1_3 (TMS)
JP1_5 (RDY/LPDCLKO)

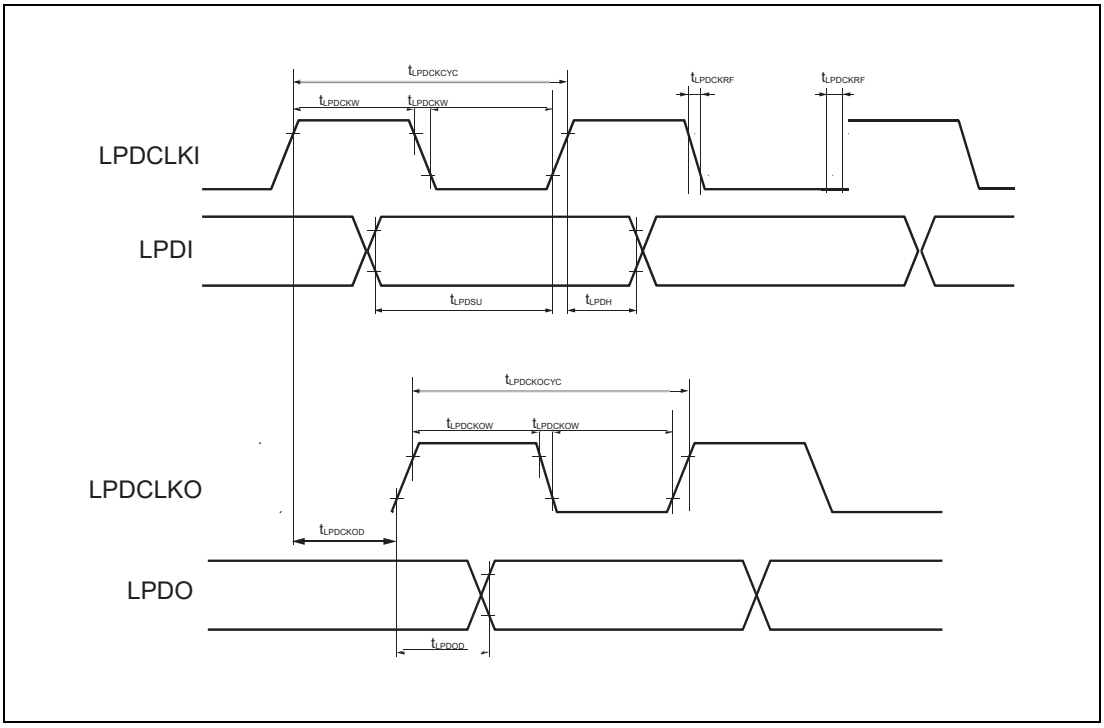


Figure 3.60 LPD (4pin) Interface Timing

3.3.33 BSCAN Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive Strength = 2 (fast)
- Buffer type = TTL

Table 3.109 BSCAN Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK (JP0_2) cycle width	t_{DCKW}		100			ns
TDI (JP0_0) setup time	t_{SDI}		12			ns
TDI (JP0_0) hold time	t_{HDI}		3			ns
TMS (JP0_3) setup time	t_{SMS}		12			ns
TMS (JP0_3) hold time	t_{HMS}		3			ns
TDO (JP0_1) delay time	t_{DDO}		0		30	ns

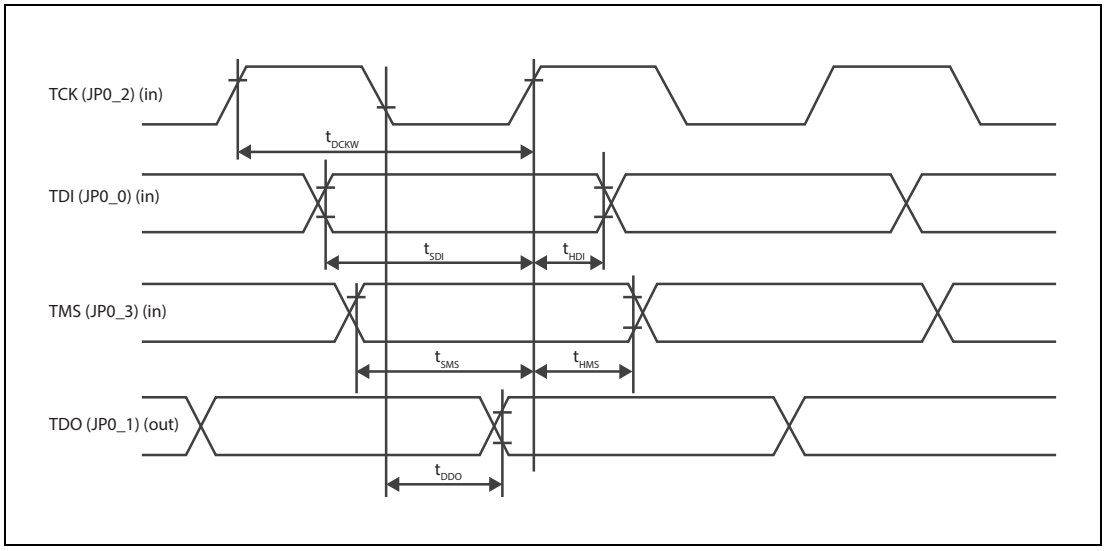


Figure 3.61 BSCAN Timing

3.3.34 Aurora Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

3.3.34.1 Aurora Interface — 1.25 Gbps baud rate

Table 3.110 Aurora Interface Operating Condition – 1.25Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	60			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			25	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	800		800	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.34.2 Aurora Interface — 2.5 Gbps baud rate

Table 3.111 Aurora Interface Operating Condition – 2.5Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	40			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			20	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	400		400	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.34.3 Aurora Interface — 3.125 Gbps baud rate

Table 3.112 Aurora Interface Operating Condition – 3.125Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise / Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	320		320	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.34.4 Aurora Interface — 5 Gbps baud rate

Table 3.113 Aurora Interface Operating Condition – 5Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.25	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	200		200	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.34.5 Aurora Interface — 6.25 Gbps baud rate

Table 3.114 Aurora Interface Operating Condition – 6.25Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise / Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.25	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	160		160	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.34.6 Aurora Interface — Transmitter clock Timing

Table 3.115 Aurora Interface Transmitter clock timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference clock frequency	f_{AICLK}	1.25 Gbps baud rate		62.5		MHz
		2.5 Gbps baud rate		125		MHz
		3.125 Gbps baud rate		156.25		MHz
		5 Gbps baud rate		125		MHz
		6.25 Gbps baud rate		156.25		MHz
Reference clock rise time	t_{AICTR}			200	400	ps
Reference clock fall time	t_{AICTF}			200	400	ps
Reference clock duty cycle			45		55	%
Reference clock total jitter	t_{AICTJ}	*1			40*2	ps
Stability	$t_{AICSTAB}$				50	ppm

Note 1. Peak to peak.
Note 2. Phase noise of CICREF[P/N] should be below the line of **Figure 3.62, Phase noise of CICREF[P/N]**.

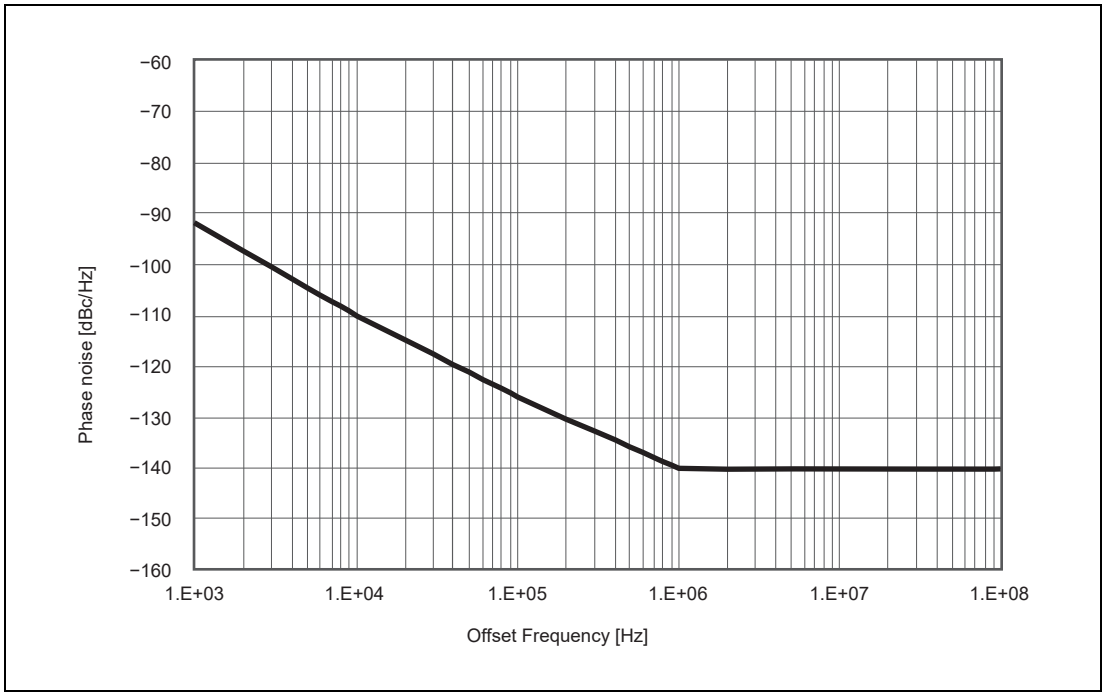


Figure 3.62 Phase noise of CICREF[P/N]

3.3.35 Debug Event Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.116 Debug Event Interface Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{EVTI}}$ input high level width	t_{WEVIH}	*1	2 ×t_{MCKW}*3			ns
		*2	2 ×t_{TCKW}			ns
$\overline{\text{EVTI}}$ input low level width	t_{WEVIL}	*1	2 ×t_{MCKW}*3			ns
		*2	2 ×t_{TCKW}			ns
$\overline{\text{EVTOn}}$ (n=0,1) output high level width	t_{WEVTOH}		t_{MCKW}*3			ns
$\overline{\text{EVTOn}}$ (n=0,1) output low level width	t_{WEVTOL}		t_{MCKW}*3			ns
$\overline{\text{MSYN}}$ input high level width	t_{WMSNH}		2 ×t_{MCKW}*3			ns
$\overline{\text{MSYN}}$ input low level width	t_{WMSNL}		2 ×t_{MCKW}*3			ns

Note 1. When used as event trigger.

Note 2. When used as break input.

Note 3. tMCKW(= MCKO) is the cycle of the clock obtained by dividing the CPU clock (CLK_CPU) and the value must be divided by 16 (default). For details, please refer to the *RH850/U2BFCC Emulation Manual: TCU(TRO_CTRL.MCD[2:0])*.

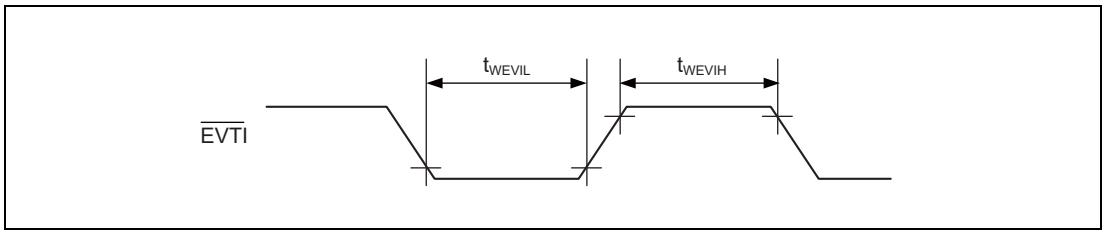


Figure 3.63 $\overline{\text{EVTI}}$ Timing

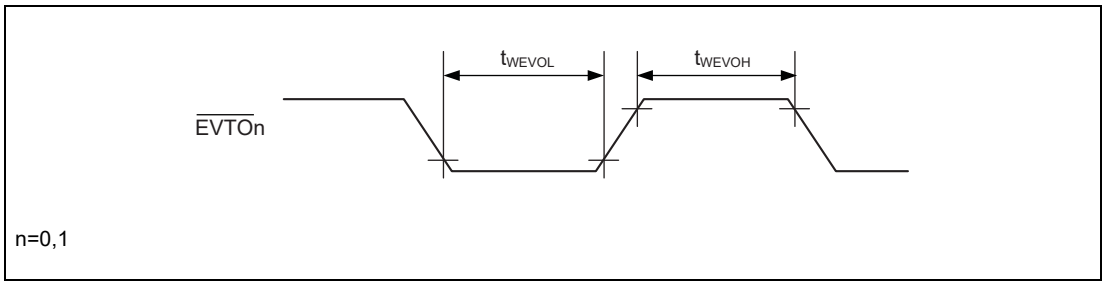


Figure 3.64 $\overline{\text{EVTO}}$ Timing

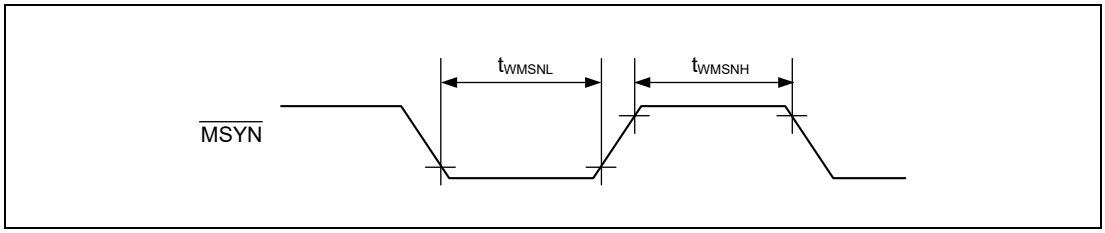


Figure 3.65 $\overline{MSYN}$ Timing

3.3.36 Debug Wake-up Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.117 Debug wake-up timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
INTDCUTDI setup time	t_{IDCUS}		1			ms
INTDCUTDI hold time	t_{IDCUH}		3			ms

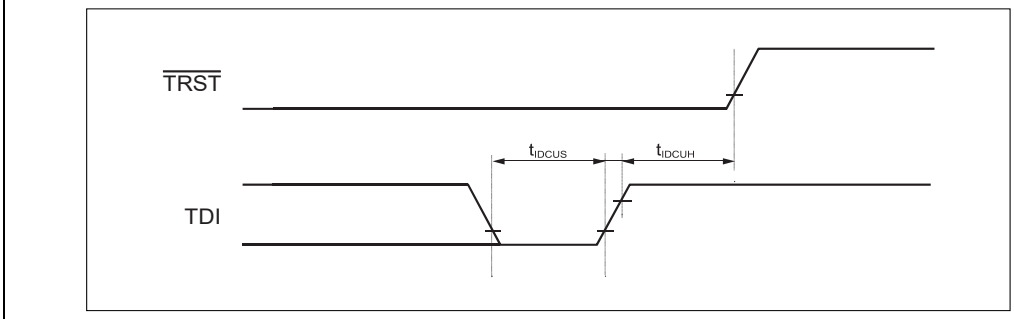


Figure 3.66 Debug wake-up timing

3.3.37 Flash Programming

3.3.37.1 Flash Programming Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.118 Flash Programming transfer rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Programming transfer rate	r_{FP}	2-wired UART mode			2.5	Mbps
FPCK cycle time	t_{KCYSF}	3-wired Clock Sync mode	100*1			ns
FPCK high level width	t_{KWHSF}	3-wired Clock Sync mode	$t_{KCYSF}/2 - 10$			ns
FPCK low level width	t_{KWLSF}	3-wired Clock Sync mode	$t_{KCYSF}/2 - 10$			ns
FPDR setup time	t_{SSISF}	3-wired Clock Sync mode	$2 \times t_{FPcyc}$*2			ns
FPDR hold time	t_{HSISF}	3-wired Clock Sync mode	$2 \times t_{FPcyc}$*2			ns
FPDT output delay	t_{DSOSF}	3-wired Clock Sync mode	$2 \times t_{FPcyc}$*2		$3 \times t_{FPcyc}$*2 + 32	ns
FPDT hold time	t_{HSOSF}	3-wired clock sync mode	$2 \times t_{FPcyc}$*2			ns

Note 1. Input the external clock data is more than or equal to 8 clocks of CLK_HSB.
Note 2. t_{FPcyc} is a period of CLK_HSB.

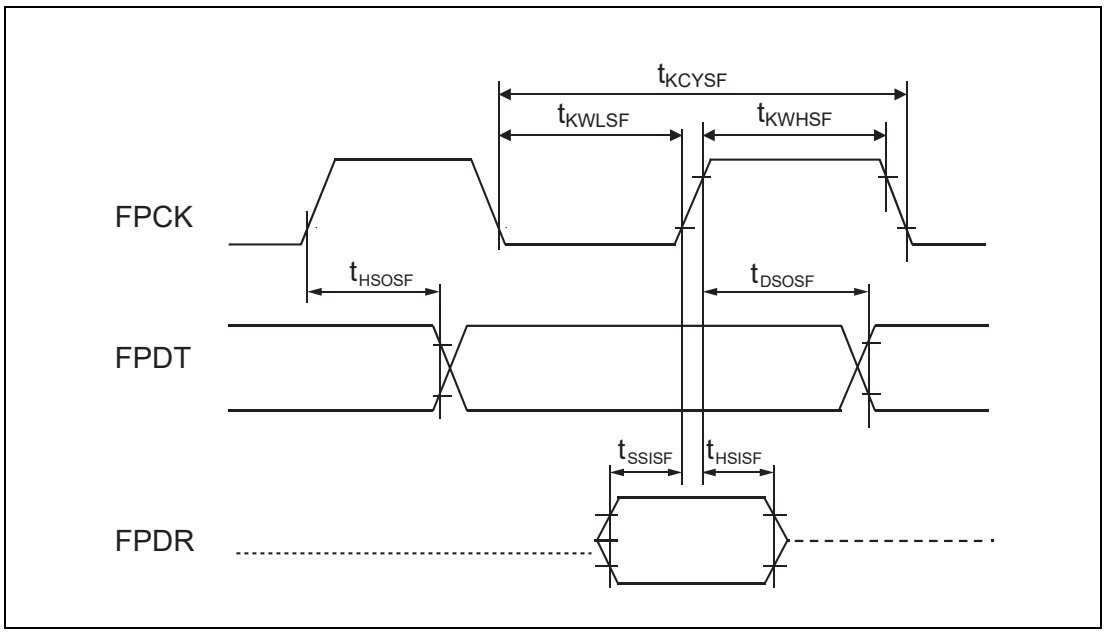


Figure 3.67 Flash Programming transfer rate

3.3.37.2 Serial Programming Setup Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.119 Serial Programming Setup Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{MD0IS}		2			ms
FLMD0 pulse input end time	t_{MD0IE}				100	ms
FLMD0 low/high level width	t_{MD0PWL}/ t_{MD0PWH}		4			µs
FLMD0 rise time	t_{MD0R}				20	ns
FLMD0 fall time	t_{MD0F}				20	ns

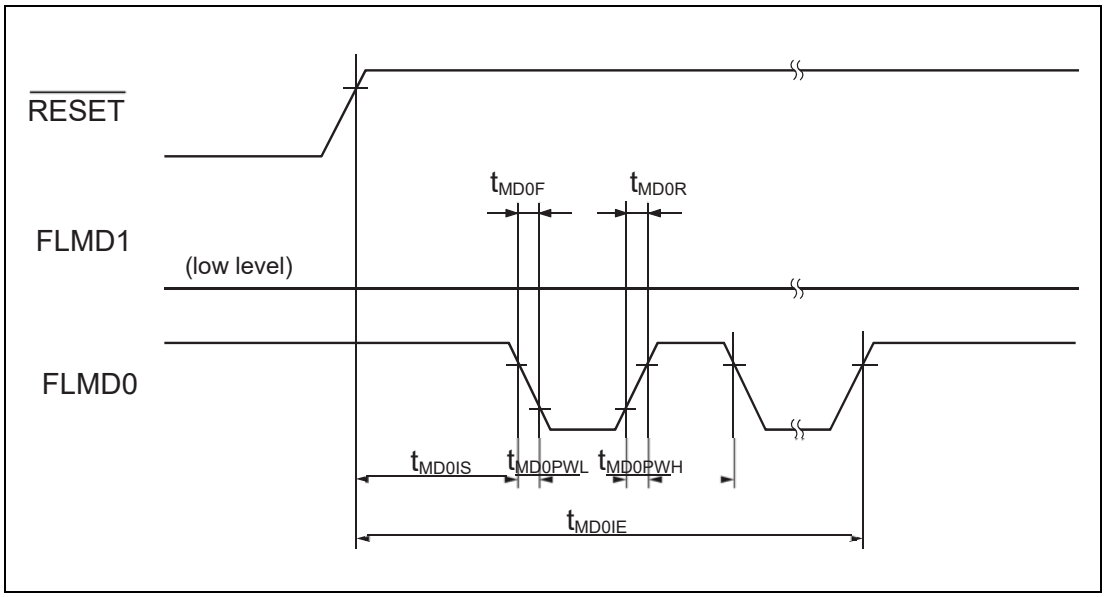


Figure 3.68 Flash Programming transfer rate

NOTE

For FLMD0 pulses, see RH850/U2B Group User's Manual:Hardware **Section 63.7.4, Selection of Flash Programming Interface.**

3.3.38 DSMIF Timing

Conditions:

See **Section 3.3.1, AC Characteristic Measurement Condition**

- Drive Strength=2 (High)
- CL=15pF

Buffer type = SHMT1

Table 3.120 DSMIF Timing (Normal mode, Master mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DSMIFn_DSMCLKOUTm cycle	$T_{DSMCLKOUTCYC}$		50	-	-	ns
DSMIFn_DSMCLKOUTm clock Low/High width	$T_{DSMCLKOUTWD}$		0.5 x $T_{DSMCLKOUTCYC}$ - 5	-	-	ns
Receive data setup time	$T_{DSMDATSU}$		20	-	-	ns
Receive data hold time	$T_{DSMDATHO}$		0	-	-	ns

Table 3.121 DSMIF Timing (Normal mode, Slave mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DSMIFn_DSMCLKINm cycle	$T_{DSMCLKINCYC}$		50	-	-	ns
DSMIFn_DSMCLKINm clock Low/High width	$T_{DSMCLKINWD}$		0.5 x $T_{DSMCLKINCYC}$ - 5	-	-	ns
Receive data setup time	$T_{DSMDATSU}$		6	-	-	ns
Receive data hold time	$T_{DSMDATHO}$		5	-	-	ns

Table 3.122 DSMIF Timing (DDR mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DSMIFn_DSMCLKOUTm cycle	$T_{DSMCLKOUTCYC}$		100	-	-	ns
DSMIFn_DSMCLKOUTm clock Low/High width	$T_{DSMCLKOUTWD}$		0.5 x $T_{DSMCLKOUTCYC}$ - 5	-	-	ns
Receive data setup time	$T_{DSMDATSU}$		20	-	-	ns
Receive data hold time	$T_{DSMDATHO}$		0	-	-	ns

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

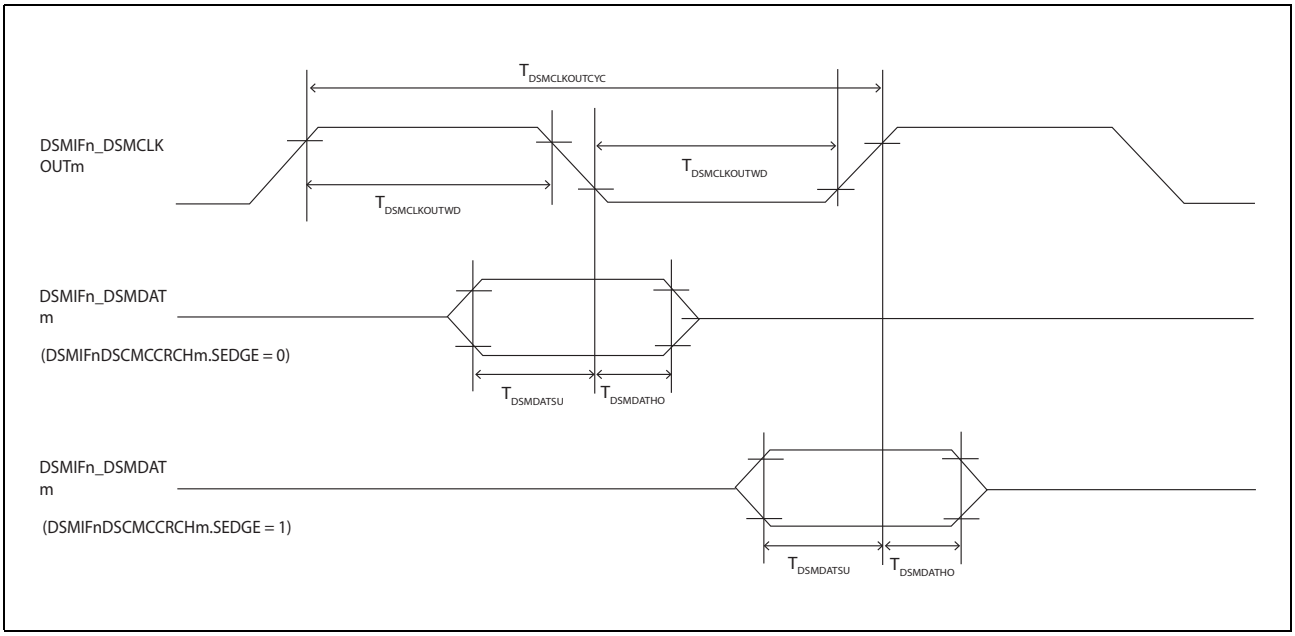


Figure 3.69 DSMIF Timing (Normal mode, Master mode)

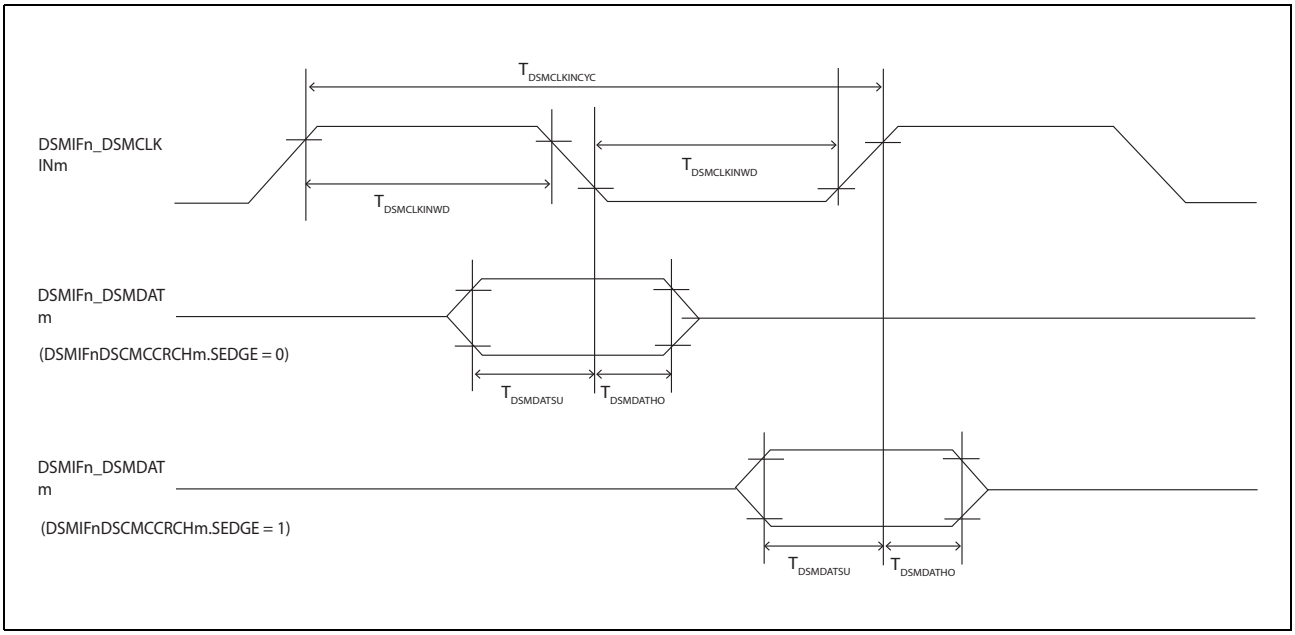


Figure 3.70 DSMIF Timing (Normal mode, Slave mode)

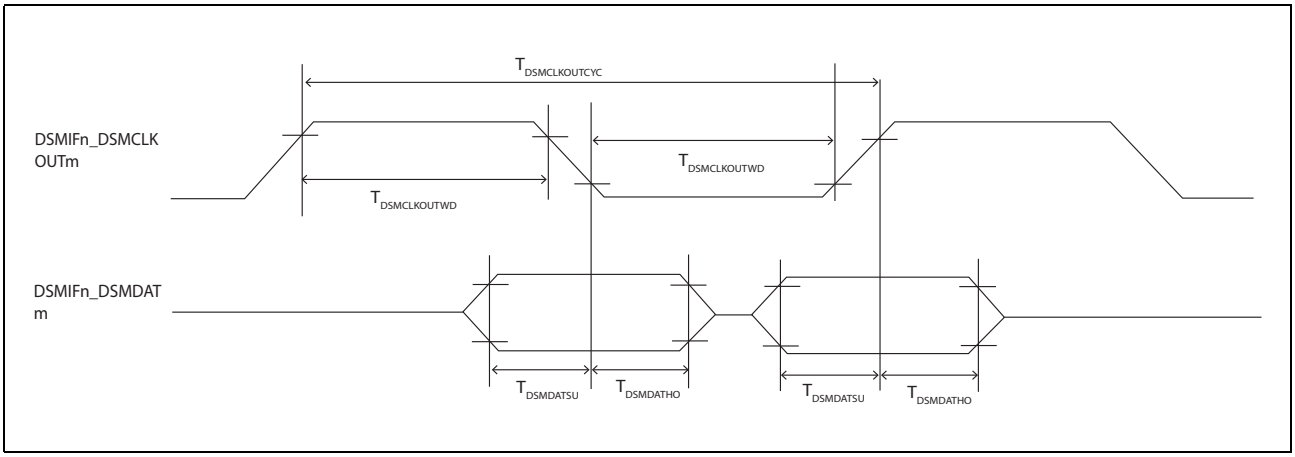


Figure 3.71 DSMIF Timing (DDR mode)

3.4 A/D Converter Characteristics

3.4.1 SAR A/D Converter Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.123 ADC Characteristics (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RESn		10		12	bit
Analog supply voltages	AnVCC		3.0		3.6	V
			4.5		5.5	V
Reference voltages	AnVREFH	AnVCC = 3.0 to 3.6 V	3.0		AnVCC	V
		AnVCC = 4.5 to 5.5 V	4.5		AnVCC	V
Analog input voltage	VIAN	ANnpq (T&H not used)	AnVSS		AnVREFH	V
		ANnpq (T&H used)	0.2		AnVREFH – 0.2	V
Operation frequency	fADCLK	AWO	10*6		40	MHz
Operation frequency	fADCLK	ISO		40*1		MHz
Conversion time	tCONV	t_{SPL} + t_{SAR}*2	1.0			µs
Sample time	tSPL*2		0.45			µs
T&H sampling time	tTHSMP	In self-diagnosis	0.45			µs
		First conversion (including after self-diagnosis	10			µs
		Other than above	0.45			µs
T&H hold time	tTHHOLD				10	µs
Slope of analog input voltage	tVSIAN	T&H used	-5		5	kV/s
Total error*3	TOE	ANnpq (T&H not used)	–4.0		4.0	LSB
		ANnpq (Either T&H group A or group B used)	–6.0		6.0	LSB
		ANnpq (Both T&H group A and group B used)	–8.0		8.0	LSB
Integral non-liniarity error*4	ILE	ANnpq (T&H not used)	–2.0		2.0	LSB
		ANnpq (T&H used)	–3.0		3.0	LSB
Differential non-liniarity error*4	DLE	ANnpq (T&H not used)	–1.0		2.0	LSB
		ANnpq (T&H used)	–1.0		2.0	LSB
Offset error*4 (Zero scale error)	OSE	ANnpq (T&H not used)	–3.5		3.5	LSB
		ANnpq (T&H used)	–5.5		5.5	LSB
Full-scale error*4	FSE	ANnpq (T&H not used)	–3.5		3.5	LSB
		ANnpq (T&H used)	–5.5		5.5	LSB
Pin self diagnosis			–40.0		40.0	LSB
AD core self-diagnosis Function			–8.0		8.0	LSB
Secondary power supply voltage monitor absolute error*5		for E0VCC, VCC*7	–16.0		16.0	LSB
		for AWOVDD, ISOVDD	–10.0		10.0	LSB

Table 3.123 ADC Characteristics (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input capacitance		Waiting				10	pF
		Sampling				20	pF
Pull-up resistor for wiring break detection	R_{PU}	ANnpq pin	VIAN = AnVSS	10		34	kΩ
			VIAN = AnVCC/2	5		22	kΩ
			VIAN = AnVCC	3		16	kΩ
Pull-down resistor for wiring break detection	R_{PD}	ANnpq pin	VIAN = AnVSS	1.5		10	kΩ
			VIAN = AnVCC/2	5		19	kΩ
			VIAN = AnVCC	10		34	kΩ
Strong Pull-down						300	Ω

Note 1. It is decided logically, so it has typical value only.

Note 2. For details of tSPL and tSAR, see RH850/U2B Group User's Manual:Hardware **Section 50.4.25, Analog Input Sampling and Scan Group Processing Time of Section 50, Analog to Digital Converter (ADCK).**

Note 3. Sampling error is not included.

Note 4. Quantization error (± 0.5 LSB) is not included.

Note 5. Error of only voltage monitor.

Note 6. 10MHz is typical value of CLK_HSIOSC/20.

Note 7. When the secondary power supply voltage monitor for E0VCC or VCC is used at A0VCC = 3.0 to 3.6 V, use this device with follwing condition.
A0VCC≧A0VREFH≧E0VCC, when E0VCC is monitored
A0VCC≧A0VREFH≧VCC, when VCC is monitored

Sampling Errors in the External Circuit of the A/D Converter

Sampling error is error to which “Errors (Sampling error 1) which depend on input leakage current of analog pin” and “Errors (Sampling error 2) which depend on conversion cycles with charge sharing” were added.

$$Sampling\ error\ =\ Sampling\ error\ 1\ +\ Sampling\ error\ 2$$

The external circuit of the A/D pin indicates below about the factor (sampling error 1 and sampling error 2) which becomes sampling error.

(a) Errors (Sampling error 1) which depend on input leakage current of analog pin

The error depends on the input leakage current (ILeak) of analog pin and external resistance (Re), and occurs.

The error which depends on the input leakage current is given by the formula of the following.

$$Sampling\ error\ 1\ (LSB)\ =\ Re \times ILeak \times \frac{4096}{V_{avrefh}}$$

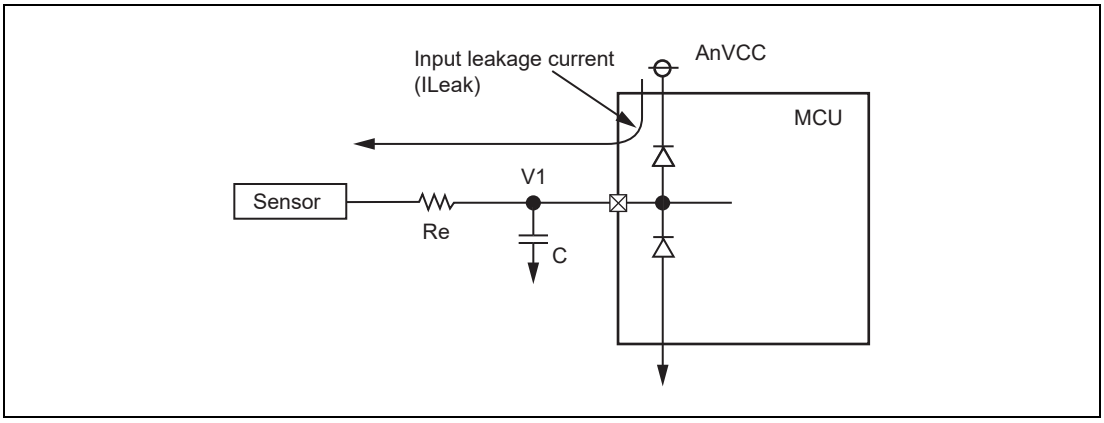


Figure 3.72 Errors (Sampling error 1) which Depend on Input Leakage Current of Analog Pin

(b) Errors (Sampling error 2) which depend on conversion cycles with charge sharing

A formula for errors in sampled values due to the external circuit of the A/D converter is given below. These errors will depend on the input circuit and conversion cycle. The formula given below for the errors is simplified for the calculation of sampling error based on internal stray capacitance, amplifier offset, resistance of the signal source, and conversion cycle. This formula can also be used to calculate the effects of the signal source resistance and conversion cycle on these errors.

The formula gives the error of analog input 2 as shown in the figure below when A/D conversion is performed in the order of analog input 1 then 2.

$$Sampling\ error\ 2\ (LSB) = \left[\left(\frac{|V2 - V1| \times CIN1}{Ce + CIN1} + \frac{|V_{vfaerr}| \times CIN2}{Ce + CIN2}\right) \times \frac{1}{1 - e^{(-T1)/(Re \times Ce)}} + \left(\frac{1}{T1} \times C1 \times V3 \times Re\right)\right] \times \frac{4096}{V_{avrefh}}$$

Table 3.124 Definition of the symbols for the Sampling Error Formula

Parameter	Symbol	Condition	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	AN0pq	1.8	pF
		AN1pq	1.8	pF
		AN2pq	1.8	pF
		AN3pq	1.8	pF
Common capacitance of the final stage of the amplifier	CIN2	AN0pq	10.8	pF
		AN1pq	10.8	pF
		AN2pq	10.8	pF
		AN3pq	10.8	pF
External capacitor on analog input pin	Ce		Depends on customer's environment	µF
Signal source impedance	Re			kΩ
Conversions cycle of analog Input pins	T1			ms
AnVREFH voltage	Vavrefh			V
Potential difference between V1 and V2	V2-V1			V
Offset voltage of the amplifier	Vvfaerr		50	mV
Parasitic capacitance in the channel multiplexer	C1		2	pF
|AnVCC voltage / 2.5 - measured pin voltage (V2)|	V3		Depends on customer's environment	V

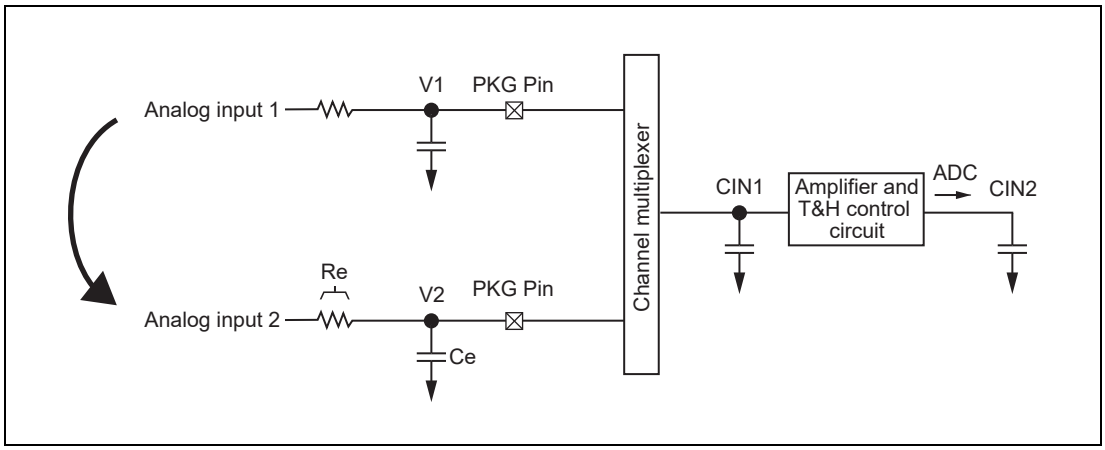


Figure 3.73 Schematic for Sampling Error 2 Formula

Values for conversion error calculated by using this formula do not include error (absolute error, etc.) specified in the A/D converter characteristics.

This formula is a desktop formula and is theoretical. When the signal source has an extremely high resistance or when the conversion cycle is too short, calculated and measured values may differ. Actual error depends on the external capacitor, external resistor, capacitance and resistance of board wiring, so please evaluate and verify the error on the user board is no greater than the value produced by this formula (Condition of this formula is “Re < 1.5 MΩ and T1 ≥ 10 µs”, or “1.5 MΩ ≤ Re ≤ 2 MΩ and T1 ≥ 512 µs”).

3.4.2 Delta-Sigma A/D Converter Characteristics

Conditions:

- See **Section 3.2.1, Operational Conditions**.

Table 3.125 Delta-Sigma A/D Converter Characteristics (High resolution mode) (ENOB, SNDR, input Impedance)

Parameter	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
ENOB[*1]	ENOB	differential	F1a, F1b, F2, F3a, F3b, F4	×1	13	—	—	bit
SNDR[*2]	SNDR	differential	F1a, F1b, F2, F3a, F3b, F4	×1	80	—	—	dB
				×2	80	—	—	dB
			F5	×1	65	—	—	dB
				×2	65	—	—	dB
			F6	×1	62	—	—	dB
				×2	62	—	—	dB
			F7	×1	56	—	—	dB
				×2	56	—	—	dB
		single-ended (reference of ADSVREFH/2)	F1a, F1b, F2, F3a, F3b, F4	×1	75	—	—	dB
				×2	80	—	—	dB
			F5	×1	59	—	—	dB
				×2	65	—	—	dB
			F6	×1	56	—	—	dB
				×2	62	—	—	dB
			F7	×1	50	—	—	dB
				×2	56	—	—	dB
		single-ended (reference of ADSVREFL)	F1a, F1b, F2, F3a, F3b, F4	×1	75	—	—	dB
				×2	75	—	—	dB
			F5	×1	59	—	—	dB
				×2	59	—	—	dB
			F6	×1	56	—	—	dB
				×2	56	—	—	dB
			F7	×1	50	—	—	dB
				×2	50	—	—	dB
Input impedance	—	—		×1	200	—	310	kΩ
				×2	100	—	155	kΩ

Note 1. Effective Number of Bits.

Note 2. Signal-to-Noise and Distortion Ratio.

Table 3.126 Delta-Sigma A/D Converter Characteristics (High resolution mode) (Offset error)

Parameter	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
Offset error *1	OSE	w/o calibration	differential	×1	−10.0	—	+10.0	mV
				×2	−10.0	—	+10.0	mV
			single-ended	×1	−10.0	—	+10.0	mV
				×2	−10.0	—	+10.0	mV
		w/ calibration (w/ conditions to temp. change*2)	differential	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
			single-ended	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
		w/ calibration (w/o conditions to temp. change*3)	differential	×1	−7.0	—	+7.0	mV
				×2	−7.0	—	+7.0	mV
			single-ended	×1	−7.0	—	+7.0	mV
				×2	−7.0	—	+7.0	mV

Note 1. Quantization error is not included.

Note 2. Temperature change after calibration is less than 50°C. (−50°C < Temperature change < +50°C).

Note 3. Temperature change after calibration is more than 50°C. (Temperature change ≥ +50°C or Temperature change ≤ −50°C).

Table 3.127 Delta-Sigma A/D Converter Characteristics (High impedance mode) (ENOB, SNDR, input Impedance) (1/2)

Parameter	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
ENOB[*1]	ENOB	differential	F1a, F1b, F2, F3a, F3b, F4	×1	12	—	—	bit
SNDR[*2]	SNDR	differential	F1a, F1b, F2, F3a, F3b, F4	×1	75	—	—	dB
				×2	75	—	—	dB
				×4	75	—	—	dB
				×8	69	—	—	dB
			F5	×1	65	—	—	dB
				×2	65	—	—	dB
				×4	65	—	—	dB
				×8	59	—	—	dB
			F6	×1	62	—	—	dB
				×2	62	—	—	dB
				×4	62	—	—	dB
				×8	56	—	—	dB
			F7	×1	50	—	—	dB
				×2	50	—	—	dB
				×4	50	—	—	dB
				×8	44	—	—	dB
		single-ended (reference of ADSVREFH/2)	F1a, F1b, F2, F3a, F3b, F4	×1	69	—	—	dB
				×2	75	—	—	dB
				×4	75	—	—	dB
				x8	69	—	—	dB
			F5	×1	59	—	—	dB
				×2	65	—	—	dB
				×4	65	—	—	dB
				×8	59	—	—	dB
			F6	×1	56	—	—	dB
				×2	62	—	—	dB
				×4	62	—	—	dB
				×8	56	—	—	dB
			F7	×1	44	—	—	dB
				×2	50	—	—	dB
				×4	50	—	—	dB
				×8	44	—	—	dB

Table 3.127 Delta-Sigma A/D Converter Characteristics (High impedance mode) (ENOB, SNDR, input Impedance) (2/2)

Parameter	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
		single-ended (reference of ADSVREFL)	F1a, F1b, F2, F3a, F3b, F4	×1	69	—	—	dB
				×2	69	—	—	dB
				×4	69	—	—	dB
				x8	63	—	—	dB
			F5	×1	59	—	—	dB
				×2	59	—	—	dB
				×4	59	—	—	dB
				×8	53	—	—	dB
			F6	×1	56	—	—	dB
				×2	56	—	—	dB
				×4	56	—	—	dB
				×8	50	—	—	dB
			F7	×1	44	—	—	dB
				×2	44	—	—	dB
				×4	44	—	—	dB
				×8	38	—	—	dB
Input impedance	—	—		×1	1000	—	2450	kΩ
				×2	500	—	1225	kΩ
				×4	250	—	612	kΩ
				×8	125	—	612	kΩ

Note 1. Effective Number of Bits.

Note 2. Signal-to-Noise and Distortion Ratio.

Table 3.128 Delta-Sigma A/D Converter Characteristics (High impedance mode) (Offset error)

Parameter	Symbol	Conditions			Value			Unit
		Calibration	Input	Gain	Min.	Typ.	Max.	
Offset error[*1]	OSE	w/o calibration	differential	×1	−25.0	—	+25.0	mV
				×2	−12.5	—	+12.5	mV
				×4	−10.0	—	+10.0	mV
				×8	−10.0	—	+10.0	mV
			single-ended	×1	−25.0	—	+25.0	mV
				×2	−12.5	—	+12.5	mV
				×4	−10.0	—	+10.0	mV
				×8	−10.0	—	+10.0	mV
		w/ calibration (w/ conditions to temp. change[*2])	differential	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
				×4	−5.0	—	+5.0	mV
				×8	−5.0	—	+5.0	mV
			single-ended	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
				×4	−5.0	—	+5.0	mV
				×8	−5.0	—	+5.0	mV
		w/ calibration (w/o conditions to temp. change[*3])	differential	×1	−7.0	—	+7.0	mV
				×2	−7.0	—	+7.0	mV
				×4	−7.0	—	+7.0	mV
				×8	−7.0	—	+7.0	mV
			single-ended	×1	−7.0	—	+7.0	mV
				×2	−7.0	—	+7.0	mV
				×4	−7.0	—	+7.0	mV
				×8	−7.0	—	+7.0	mV

Note 1. Quantization error is not included.

Note 2. Temperature change after calibration is less than 50°C. (−50°C < Temperature change < +50°C).

Note 3. Temperature change after calibration is more than 50°C. (Temperature change ≥ +50°C or Temperature change ≤ −50°C).

Table 3.129 Delta-Sigma A/D Converter Characteristics (Gain error)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain error[*1,*2,*3]	GE	DC input w/o calibration	−1.0	—	+1.0	%
		DC input w/ calibration (w/ conditions to temp. change[*4])	−0.1	—	+0.1	%
		DC input w/ calibration (w/o conditions to temp. change[*5])	−0.2	—	+0.2	%

Note 1. The gain error of F1a, F1b, F2, F3a, F3b, F4 specified in this table are the gain error of A/D conversion result corrected by software processing or by DFE.

Note 2. Excluding the influence of external input resistors.

Note 3. Quantization error is not included.

Note 4. Temperature change after calibration is less than 50°C. (−50°C < Temperature change < +50°C).

Note 5. Temperature change after calibration is more than 50°C. (Temperature change ≥ +50°C or Temperature change ≤ −50°C).

Table 3.130 Delta-Sigma A/D Converter Post Filter Characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Passband bandwidth	BW	Fs = 100 ksps, Ripple within ±1%	—	—	30	kHz
		Fs = 200 ksps, Ripple within ±1%*1	—	—	30	kHz
		Fs = 200 ksps, Ripple within ±1%*2	—	—	60	kHz
		Fs = 400 ksps, Fc = −3dB	—	—	90	kHz
		Fs = 800 ksps, Fc = −3dB	—	—	100	kHz
		Fs = 1600 ksps, Fc = −3dB	—	—	200	kHz
Initial delay	—	Fs = 100/200 ksps, BW = 30 kHz	—	—	65	µs
		Fs = 200 ksps, BW = 60 kHz	—	—	65	µs
		Fs = 400 ksps	—	—	8.75	µs
		Fs = 800 ksps	—	—	7.5	µs
		Fs = 1600 ksps	—	—	3.75	µs
Group delay	—	Fs = 100/200 ksps, BW = 30 kHz, Min. phase (Fin < 10 kHz)	—	—	15	µs
		Fs = 200 ksps, BW = 60 kHz, Min. phase (Fin < 10 kHz)	—	—	10	µs
		Fs = 100/200 ksps, BW = 30 kHz, Linear phase	—	—	32	µs
		Fs = 200 ksps, BW = 60 kHz, Linear phase	—	—	32	µs
		Fs = 400 ksps, Linear phase	—	—	4.5	µs
		Fs = 800 ksps, Linear phase	—	—	3.88	µs
		Fs = 1600 ksps, Linear phase	—	—	2.0 25	µs

Note 1. Filter type is 2nd Stage Use Case 2(F1b).
Refer to RH850/U2B Group User's Manual:Hardware **Section 51.6.2, Filter Type Setting** of **Section 51, Delta-Sigma Analog to Digital Converter (DSADC).**

Note 2. Filter type is 2nd Stage Use Case 3(F2).
Refer to RH850/U2B Group User's Manual:Hardware **Section 51.6.2, Filter Type Setting** of **Section 51, Delta-Sigma Analog to Digital Converter (DSADC)**.

Table 3.131 Delta-Sigma A/D Converter Analog Input Voltage Range Specifications

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input voltage specification with a single-ended reference of ADSVREFH/2	Vain	Gain = ×1	ADSVREFL	—	ADSVREFH	V
		Gain = ×2	ADSVREFL	—	ADSVREFH	V
		Gain = ×4	ADSVREFH × (1/4)	—	ADSVREFH × (3/4)	V
		Gain = ×8	ADSVREFH × (3/8)	—	ADSVREFH × (5/8)	V
Input voltage specification with a single-ended reference of ADSVREFL	Vain	Gain = ×1	ADSVREFL	—	ADSVREFH	V
		Gain = ×2	ADSVREFL	—	ADSVREFH × (1/2)	V
		Gain = ×4	ADSVREFL	—	ADSVREFH × (1/4)	V
		Gain = ×8	ADSVREFL	—	ADSVREFH × (1/8)	V
Input voltage specification with differential input[*1]	Vain	Gain = ×1	−ADSVREFH	—	ADSVREFH	V
		Gain = ×2	−ADSVREFH × (1/2)	—	ADSVREFH × (1/2)	V
		Gain = ×4	−ADSVREFH × (1/4)	—	ADSVREFH × (1/4)	V
		Gain = ×8	−ADSVREFH × (1/8)	—	ADSVREFH × (1/8)	V

Note 1. These indicates a difference voltage of the P side input voltage and N side input voltage (P side input voltage - N side input voltage). The respective input voltage range are ADSVREFL to ADSVREFH.

3.4.3 Cyclic A/D Converter Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.132 Cyclic A/D Converter Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ENOB[*1]	ENOB	differential, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	12[*3]	—	—	bit
		single-ended, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	11[*3]	—	—	bit
SNDR[*2]	SNDR	differential, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	74[*3]	—	—	dB
		single-ended, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	68[*3]	—	—	dB
Input impedance	—	Fs = 1000 ksps, w/ averaging	100	—	—	kΩ
Offset error[*5]	OSE	Fs = 1000 ksps, w/ averaging	−5.0[*3]	—	+5.0[*3]	mV
Gain error[*4,*5]	GE	Fs = 1000 ksps, w/ averaging, DC input	−1.0[*3]	—	+1.0[*3]	%
Passband bandwidth	BW	Fs = 1000 ksps, w/ averaging, Fc = −3dB	—	—	500	kHz
Initial delay	—	Fs = 1000 ksps, w/ averaging	—	—	25.0	µs
Group delay	—	Fs = 1000 ksps, w/ averaging, Linear phase	—	—	1.25	µs

Note 1. Effective Number of Bits.
Note 2. Signal-to-Noise and Distortion Ratio.
Note 3. These characteristics values are after calibration.
Note 4. Excluding the influence of external input resistors.
Note 5. Quantization error is not included.

Table 3.133 Cyclic A/D Converter Analog Input Voltage Range Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Reference
Input voltage specification with a single-ended reference of ADSVREFH/2	Vain		ADSVREFL	—	ADSVREFH	V	
Input voltage specification with a single-ended reference of ADSVREFL	Vain		ADSVREFL	—	ADSVREFH	V	
Input voltage specification with differential input [*1]	Vain		−ADSVREFH	—	ADSVREFH	V	

Note 1. These indicates a difference voltage of the P side input voltage and N side input voltage (P side input voltage - N side input voltage). The respective input voltage range are ADSVREFL to ADSVREFH.

3.4.4 Shared Analog and Digital Input Characteristics

Table 3.134 Digital Input Timing in Analog Input Pins

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Reference
ANDI*1 rising time	t_{ANDIr}	10 to 90%	1000	—	—	ns	
ANDI*1 falling time	t_{ANDIf}	90 to 10%	1000	—	—	ns	

Note 1. ANDI means digital input (general input or SENT input) in analog input pins.

CAUTION

When this regulation isn't maintained, A/D accuracy may be degraded.

3.5 R/D Converter Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

3.5.1 RDC Conversion Performance

Regarding RDC3AS, **Table 3.135, RDC Conversion Performance** lists the specifications of the conversion performance of the RDC when filter setting of ⊿ΣADC is set to F5.

Table 3.135 RDC Conversion Performance (1/2)

Parameter	Condition			Min.	Typ.	Max.	Unit
Resolution[*1]				-	-	16	bit
Conversion accuracy[*2]	Absolute error in electrical angle signal while operation is stopped (12-bit resolution)	RDC3AL		-4	-	+4	LSB
		RDC3AS		-4	-	+4	
Settling time (Response for input of electric angle of 180°)	Settling range within ±8 LSB(12-bit resolution)	Band 800 Hz		-	53	-	ms
		Band 1500 Hz			31		
		Band 1000 Hz		-	43	-	
		Band 500 Hz		-	85	-	
		Band 200 Hz		-	211	-	
		Automatic adjustment	RDC3AL	-	1.9[*7]	-	
			RDC3AS	-	2.2[*7]	-	
Maximum angular velocity[*3] (The values in parentheses apply when the bandwidth setting is automatic adjustment)	16-bit resolution			15000 (7500)	-	-	min^{-1}
	14-bit resolution			60000 (30000)	-	-	
	13-bit resolution			120000 (60000)	-	-	
	12-bit resolution			240000 (120000)	-	-	
	11-bit resolution			480000 (240000)	-	-	
	10-bit resolution			960000 (480000)	-	-	
Maximum angular acceleration (Range of trackable angular acceleration (electrical angle))			Band 800 Hz	-	146000	-	rad/s^2
			Band 1500 Hz	-	513000	-	
			Band 1000 Hz	-	183000	-	
			Band 500 Hz	-	46000	-	
			Band 200 Hz	-	5000	-	
			Automatic adjustment	-	3000000[*8]	-	
Response delay[*4]	Electrical angle output response delay in fixed angular velocity		RDC3AL	–0.2	-	0.2	
			RDC3AS	–0.2	-	0.2	°/ 10000 min^{-1}

Table 3.135 RDC Conversion Performance (2/2)

Parameter	Condition	Min.	Typ.	Max.	Unit
BIST determination time*5	Sum-of-squares amplitude error detection BIST (low side)	-	-	1	ms
	Sum-of-squares amplitude error detection BIST (high side)	-	-	1	ms
	ADBIST*9	-	-	32	us
	Angle conversion BIST (angle determination threshold is within ±16 LSB)	-	-	10	ms
	Resolver signal error detection BIST	-	-	0.5	ms
	Resolver signal cut off detection BIST	-	-	1	ms
	Conversion error BIST	-	-	10	ms
	Power_short error BIST*9	-	-	80	us
	Ground short error BIST*9	-	-	80	us
BIST recovery time*6	All kinds of BIST	-	-	10	ms

Note 1. The resolution is changed by the setting of the maximum angular velocity select bit in the RDC3n control gain selection register 1. The angle can be read with maximum 16-bit width by register access.

Note 2. This is the actual value when the waveform of analog input to the RDC is an ideal sine wave. R/D conversion result will differ from resolver machine angle with distortion or slippage of analog input signal or power supply voltage.

Note 3. Range of trackable angular velocity(electrical angle). It depends on the maximum angular velocity selection bit setting (MAXV[2:0]). When the band setting is set to automatic adjustment, the maximum angular velocity at each resolution will be half the value.

Note 4. PHI angle output from RDC is added accuracy error through analog circuit to this value. The read of PHI angle output register value with bus access needs access time. However, it does not need access time using PHI compare signal.
For RDC3AS, this response delay specification is applied at the excitation frequencyof 5kHz to 25kHz.

Note 5. It is the time to stabilize BIST determination.

Note 6. Recovery time from BIST operation to normal operation.
When the excitation frequency is under 9 kHz, BIST recovery time is maximum 15 ms.
When the conversion error determination time(EDPS[1:0]) is set to over 10 ms, BIST recovery time is also set to over the setting value.

Note 7. The time may be longer than the indicated value if the value of the HKVLM[3:0] bits (high gain-limit setting for the AGC) is low.

Note 8. The value may be lower than the indicated value if the value of the HKVLM[3:0] bits (high gain-limit setting for the AGC) is low.

Note 9. only RDC3AL has the Characteristics, RDC3AS has no the features.

3.5.2 RDC Analog Pin(RDC3AL only, RDC3AS no the feature)

Table 3.136 RDC Analog Pin Characteristics

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit
Signal source output for resolver excitation power supply[*1]	RSO	Frequency	5	-	40	kHz
		Output voltage[*2]	0.38 × AFCVCC	0.4 ×AFCVCC	0.42 ×AFCVCC	VP-P
		Load impedance	10	-	-	kΩ
		Output switching[*3]	–40	±0	+20	%
Common voltage output for resolver excitation power supply	COM	Output voltage	0.475 ×AFCVCC	0.5 ×AFCVCC	0.525 ×AFCVCC	V
		Load impedance	10	-	-	kΩ
Resolver excitation signal external input	R1E, R2E (RSO, COM)	Frequency [*4*10]	5	-	40	kHz
		Input voltage range	0	-	AFCVCC	V
		Input voltage differential amplitude	2	-	-	VP-P
		Input impedance[*11] (Ground pulldown resistor)	30	40	52	kΩ
Resolver signal input	S1, S2, S3, S4	Frequency[*10]	5	-	40	kHz
		Input voltage range[*5]	1.2	-	AFCVCC -1.2	V
		Input impedance RF[*6]	16.2	21	26.5	kΩ
		Input impedance RF switching[*7]	-40	±0	+40	%
		Actual gain when gain is set to 1 (PGAX1 = 1)[*12]	0.9	1	1.1	multiples
Resolver signal monitor output	COSMNT, SINMNT	Frequency[*8]	5	-	40	kHz
		Output voltage[*9]	0.32 ×AFCVCC		0.68 ×AFCVCC	VP-P
		Load impedance	100	-	-	kΩ

Note 1. Pseudo sine wave output, 7-bit D/A output.

Note 2. The center of output voltage is COM. Described values are the values when the output adjustment is set to default (±0%) .

Note 3. The output voltage can be adjusted in four steps of -40, -20, ±0, and +20% by adjust function.

Note 4. When the excitation frequency is over 22 kHz with resolver excitation signal external input (RDC3AnREF.EXIO = 0B), set RDC3nDIAG1.CVEDS = 1B, and do not set using RD conversion error detection circuit (for high-speed rotation).

Note 5. Depends on external circuit. Input voltage must be adjusted for COSMNT, SINMNT = 0.32 × AFCVCC to 0.68 × AFCVCC (VP-P).

Note 6. Input impedance of on-chip feed-back resistor (RF). This is the default value (±0%).

Note 7. Can be adjusted from -40 to +40% in step of 10% by using the adjustment function.

Note 8. Same as the frequency of resolver signal input.

Note 9. Must be adjusted within this range to keep angle conversion resolution.

Note 10. The phase error of the excitation component of the resolver excitation signal external input and the resolver signal input must be within 30º.

Note 11. When RDC3ALnREF.EXIO = 0B (i.e. the external excitation signal input is set), this impedance pulls the RSO (R1E) and COM (R2E) pins down to AFCVSS.

Note 12. When PGAX1 = 1, RE shown "**Section 49.1.5.1, Resolver Signal Input (Differential) Circuit** of the *RH850/U2B Group Resolver to Digital Converter User's Manual: Hardware*" becomes 21kΩ (typ), and the gain of the amplifier becomes 1x. However, in this case, it is necessary to set the RF resistance value to the same 21 kΩ (typ), so set IRSS1 = 0, IRSS0 = 1, IRSC [3: 0] = 0100. The gain can be changed from 1x by

changing the RF resistance value setting with IRSC [3: 0].

3.5.3 Error Detection Characteristics

Table 3.137 Error Detection Characteristics

Error Detection Parameter			Set Threshold (Default Setting)	Detection Time
Resolver signal error monitor output amplitude voltage[*1]	Set register RDC3AnDIAG0.EXCETH[7:0]	RDC3AL	0.102 × (AFCVCC±5%) [Vp-p]	220 [µs] (typ.), 2 [ms] (max.)
		RDC3AS	0.102 × (ADSVREFH ± 5%) [Vp-p]	300 [µs] (typ.), 2 [ms] (max.)
Disconnection of resolver signal (Direct current bias supply method) VSINMNT-VCOM or VCOSMNT-VCOM[*2*8]	The register used for setting threshold when DC resolver is selected RDC3AnDIAG0.SGBDTH[7:0]	RDC3AL	COM + 0.35 × (AFCVCC±5%) [VDC][*9]	10 [ms] (max.)
		RDC3AS	COM + 0.35 × (ADSVREFH ± 5%) [VDC]	
		RDC3AL	COM + 0.08 × (AFCVCC±5%) [VDC][*9]	
	The register used for setting threshold when VR resolver is selected RDC3AnDIAG0.SGBTH[7:0]	RDC3AS	COM + 0.08 × (ADSVREFH ± 5%) [VDC]	
R/D conversion error (over control declination) Recognition level for internal control deviation (f(t) ・ ε)[*3]	High side		$0CA8_H$	*4
	Low side		$F358_H$	
Resolver signal power short error*[6]	Pins S1, S2, S3, and S4		0.9 × (AFCVCC±5%) [VDC]	0.08 [ms] (max.)
	Pins RSO and COM		0.8 × (AFCVCC±5%) [VDC]	
Resolver signal ground short error*[6]	Pins S1, S2, S3, and S4		0.1 × (AFCVCC±5%) [VDC]	0.08 [ms] (max.)
	Pins RSO and COM		0.2 × (AFCVCC±5%) [VDC]	
Sum of square amplitude error Integral value of sum of square of SINMNT and COSMNT within the excitation period	High side	RDC3AL	0.8 × (AFCVCC±5%) [Vp-p]	*5
		RDC3AS	0.8 × (ADSVREFH ± 5%) [Vp-p]	
		RDC3AL	0.2 × (AFCVCC ± 5%) [Vp-p]	
	Low side	RDC3AS	0.2 × (ADSVREFH ± 5%) [Vp-p]	

Note 1. Determined as an error, when both of SINMNT and COSMNT become under threshold.

Note 2. Determined as an error, when common DC level changed over threshold.

Note 3. Determined as over, when control variation (f(t) ・ ε) becomes over high side threshold, or under low side threshold.

Note 4. Determined as an error, when the period of control variation (f(t) ・ ε) is above high side threshhold or below low side threshold exceeds 50% of the judgment cycle set by EDPS[1:0] bits in the RDC3AnDIAG1 register (default is about 7.37 ms). It might not be detected, when the continuous period is shorter than judgement cycle.

Note 5. Dependent on the excitation frequency and amplitude error excitation period count settings.
In RDC3AS, see the RH850/U2B Group Resolver to Digital Converter User's Manual: Hardware **Table 49.101**, Integrals of the Sums of Squares of SINMNT and COSMNT for One Cycle of Excitation for the relationship between the excitation frequency, the sin, cos differential signal amplitude

acquired by the ΔΣADC, and the sum of squares values at that time.

Note 6. Only RDC3AL has the Characteristics, RDC3AS has no the features.

Note 7. In RDC3AS, "AFCVCC" means "(ADSVREFH - ADSVREFL)".

Note 8. In RDC3AS, "VSINMNT-VCOM or VCOSMNT-VCOM" means "SINMNT or COSMNT".

Note 9. In RDC3AS, ignore "COM +".

3.6 Fast Comparator

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.138 Fast Comparator

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RES_{FC}	-	-	12		bit
Comparison voltage accuracy *1	ACC_{FC}	AFCVCC = 3.0 V to 3.6 V	-8	-	8	LSB
		AFCVCC = 4.5 V to 5.5 V	-6	-	6	LSB
Comparison time	T_{COMPFC}	-	-	200	-	ns
Measurement range *2	V_{IANFC}	-	AFCVSS	-	AFCVCC-1.0	V
Input Slew Rate	SR_{FC}	-	-45		45	V/ms

Note 1. Comparison voltage is the following.
Comparison voltage =(DAC Data value / 4096) × AFCVCC
DAC Data value means FCMPnDACCFG0.DACVH[11:0] or FCMPnDACCFG0.DACVL[11:0].

Note 2. Measurement range means analog input voltage range which Comparison accuracy is guaranteed. About analog input voltage range which Comparison accuracy is not guaranteed, See **Section 3.1, Absolute Maximum Ratings**.

3.7 Motor control signal timing

Refer to RH850/U2B Group User's Manual:Hardware "**Section 33.24, Timer Timing**" (Target TAPAn, TSGn)

3.8 Code Flash Characteristics

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.139 Code Flash Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLKFC} *1		8		40	MHz
Number of rewrites*2	CWRT	Data retention of 20 years*3	1000			times

Note 1. f_{CLKFC} is the frequency of CLK_LSB.

Note 2. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n”, the device can be erased “n” times for each block. For example, when a block of 64 KB is erased after 512 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 3. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Only the processing time of the hardware. The overhead required by the software is not included.

Table 3.140 Code Flash Programming Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming time		512 B	CWRT < 100 times		0.31	1.6		0.25	1.4		0.24	1.3	ms
			CWRT ≥ 100 times		0.39	1.9		0.3	1.7		0.29	1.6	ms
		8 KB	CWRT < 100 times		5.0	12.5		4.0	10.6		3.8	9.8	ms
			CWRT ≥ 100 times		6.0	15.0		4.8	12.7		4.6	11.8	ms
		64 KB	CWRT < 100 times		40	100		32	84.8		30.4	78.4	ms
			CWRT ≥ 100 times		48	120		38.4	101.6		36.8	94.4	ms
		1 MB	CWRT < 100 times		0.64	1.60		0.5	1.36		0.47	1.25	s
			CWRT ≥ 100 times		0.77	1.92		0.6	1.63		0.57	1.50	s
Erasure time*1		16 KB	CWRT < 100 times		26	108		24	98		24	96	ms
			CWRT ≥ 100 times		32	130		29	118		29	116	ms
		64 KB	CWRT < 100 times		88	374		81	340		78	330	ms
			CWRT ≥ 100 times		106	449		98	408		94	396	ms
		1 MB	CWRT < 100 times		1.4	6.0		1.3	5.4		1.25	5.3	s
			CWRT ≥ 100 times		1.7	7.2		1.6	6.5		1.5	6.4	s

Note 1. When erase counter function is used, add the erase counter update time. For detail, see **Table 3.144, Erase Counter update time Characteristics**.

Table 3.141 Code Flash Programming/Erasure suspend latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Suspend Latency	tSPD					150			120			120	µs
Erasure Suspend Latency	tSED					150			120			120	µs

Table 3.142 Code Flash Programming/Erasure resume latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Resume Latency	tRPT					80			50			50	µs
Erasure Resume Latency	tRECT					110			80			80	µs

Table 3.143 Code Flash Forced Stop command latency

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Forced Stop command Latency	tFD					28			20			20	µs

Table 3.144 Erase Counter update time Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Erase Counter update time					16.64	193.72		15.0	181.08		14.65	176.88	ms

3.9 Data Flash Characteristics

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.145 Data Flash Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLKFD} *1		8		40	MHz
Number of rewrites*2	DWRT	Data retention 20 years*3	125k			Times
		Data retention 3 years*3	250k			Times

Note 1. f_{CLKFD} is the frequency of CLK_LSB.

Note 2. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n”, the device can be erased “n” times for each block. For example, when a block of 4096 bytes is erased after 4 bytes of writing have been performed for different addresses 1024 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 3. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Only the processing time of the hardware. The overhead required by the software is not included.

Table 3.146 Data Flash Programming Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming time		4 B			0.12	0.82		0.09	0.70		0.08	0.66	ms
		8 B			0.13	0.88		0.09	0.73		0.08	0.67	ms
		16 B			0.14	0.97		0.09	0.76		0.08	0.70	ms
		32 B			0.14	0.97		0.09	0.76		0.08	0.70	ms
		64 B			0.14	0.97		0.10	0.76		0.09	0.70	ms
		128 B			0.17	1.20		0.13	0.95		0.11	0.89	ms
		2 KB			2.72	9.64		2.08	7.56		1.76	6.92	ms
		128 KB			0.174	0.62		0.13	0.48		0.11	0.44	s
Property Programming time		32 B			0.41	2.64		0.29	2.18		0.25	2.03	ms
Switch Programming time		32 B			0.26	1.79		0.18	1.46		0.16	1.36	ms
TAG Update time					0.30	1.70		0.21	1.43		0.18	1.34	ms
Erasure time		2 KB *1			11.1	105		9.9	95		9.6	92	ms
		4 KB			19.2	179		17	160		16.4	155	ms
		128 KB			0.62	5.73		0.55	5.12		0.53	4.96	s
Blank check command time		4 B				5.5			2.3			1.3	µs
		4 KB				1.8			0.8			0.5	ms
Property Erase time		2 KB			11.1	105		9.9	95		9.6	92	ms
Switch Erase time		2 KB			11.4	106.7		10.1	96.4		9.8	93.4	ms
TAG Erase time		2 KB			11.4	106.7		10.1	96.4		9.8	93.4	ms

Note 1. Extended Data Area Only

Table 3.147 Data Flash Programming/Erasure suspend latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Suspend Latency*1	tSPD					150			120			120	µs
Erase Suspend Latency*1	tSED					150			120			120	µs

Note 1. Data Area and Extended Data Area Only

Table 3.148 Data Flash Programming/Erasure resume latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Resume Latency*1	tRPDTS		After programming or erasing to programming suspending data flash			100			70			70	µs
	tRPT		Other than those above			80			50			50	µs
Erasure Resume Latency*1	tREDT					100			70			70	µs

Note 1. Data Area and Extended Data Area Only

Table 3.149 Forced Stop command latency

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Forced Stop command Latency	tFD					28			20			20	µs

3.10 Temperature Sensor Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.150 Temperature Sensor Characteristics*1*2*3

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature accuracy	A_{CCTS1}	- 40 °C ≤ Tj ≤ + 140 °C	–4		4	°C
	A_{CCTS2}	Tj > 140 °C	–2		2	°C
Temperature update period	t_{TSUP}		10			ms
Operation stabilization waiting time	t_{TSSB}				200	µs

Note 1. The temperature borders need to be set keeping the temperature range (Tj(min) to Tj(max)) including the temperature sensor accuracy.

Note 2. It does not include accuracy of measuring equipment.

Note 3. Temperature sensor cannot detect local heat generation inside the chip.

3.11 Thermal Characteristics

3.11.1 Thermal Characteristics Parameter

Table 3.151 Thermal Characteristics (2/2)[*1]

Parameter	Estimated value				Unit	Remark
	U2B10			U2B6		
	BGA468	BGA373	BGA292	BGA292		
θja	12.2	14.3	14.2	17.1	°C/W	JESD51-9 compliant (4 layers)
θjb	7.20	8.99	8.12	11.1	°C/W	JESD51-9 compliant (4 layers)
θjc	4.83	6.01	6.17	8.45	°C/W	JESD51-9 compliant (4 layers)
θjcbot	4.95	5.84	5.47	8.12	°C/W	JESD51-9 compliant (4 layers)
Ψjb	6.87	8.59	7.86	10.8	°C/W	JESD51-9 compliant (4 layers)
Ψjmb[*2]	4.29	5.01	4.80	7.27	°C/W	JESD51-9 compliant (4 layers)
Ψjt	0.13	0.15	0.15	0.21	°C/W	JESD51-9 compliant (4 layers)
4Lθja	14.0	16.9	17.0	20.1	°C/W	L board (4 layers)
4Lθjb	8.26	10.6	9.62	12.8	°C/W	L board (4 layers)
4LΨjb	7.76	10.0	9.17	12.3	°C/W	L board (4 layers)
4LΨjmb[*2]	4.18	4.74	4.69	7.07	°C/W	L board (4 layers)
4LΨjt	0.15	0.18	0.18	0.25	°C/W	L board (4 layers)
4LTb_inc	6.32	6.95	8.00	7.92	°C/W	L board (4 layers)

Note 1. The thermal characterization parameters depends on the usage environment

Note 2. Ψjmb shows thermal characterization parameter from junction to board surface (center of the PKG on layer-1; Tmb).
Ψjmb = (Tj-Tmb)/Pd (Pd: power consumption of the chip)

3.11.2 Assumed board

Table 3.152 JESD51-9 Compliant oard (4 Layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board Size	101.5	114.5	11621.75
Remaining copper rate		Conductor thickness	
50 - 95 - 95 - 50%		70 - 35 - 35 - 70 µm	

Table 3.153 L board (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board Size	90	160	14400
Remaining copper rate		Conductor thickness	
30 - 80 - 80 - 30%		35 - 35 - 35 - 35 µm	

Section 4 Package

NOTE

Please skip the contents related U2B24/U2B20/U2B20-FCC.

4.1 Package Outline

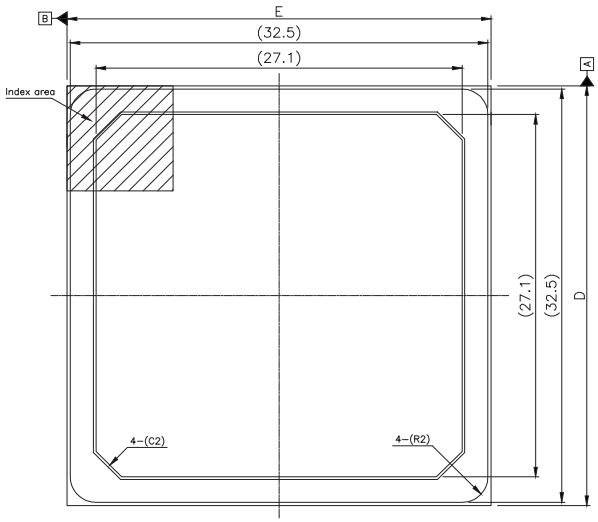
Table 4.1 RH850/U2B Package list

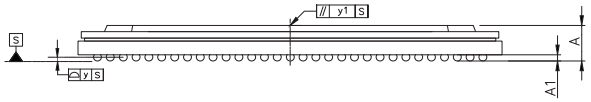
Package	RH850/ U2B-EVA	RH850/ U2B-FCC	RH850/ U2B24	RH850/ U2B20	RH850/ U2B10	RH850/ U2B6
FCBGA-600 1.0-mm ball pitch 33 mm × 33 mm	√					
FCBGA-468 0.8-mm ball pitch 25 mm × 25 mm		√	√			
FCBGA-373 0.8-mm ball pitch 21 mm × 21 mm		√	√			
FCBGA-292 0.8-mm ball pitch 17 mm × 17 mm		√				
Plastic FBGA-468 0.8-mm ball pitch 25 mm × 25 mm				√	√	
Plastic FBGA-373 0.8-mm ball pitch 21 mm × 21 mm				√	√	
Plastic FBGA-292 0.8-mm ball pitch 17 mm × 17 mm					√	√

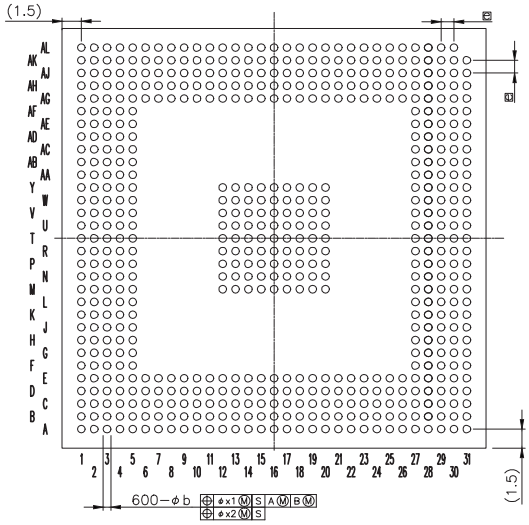
4.1.1 FCBGA600 Package Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HBGA600-33x33-1.00	PRBG0600FB-A	—	8.6

Unit:mm







Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	32.8	33.0	33.2
E	32.8	33.0	33.2
A	–	–	3.05
A1	0.35	0.45	0.55
e	–	1.00	–
b	0.50	0.60	0.70
X1	–	–	0.25
X2	–	–	0.10
y	–	–	0.20
y1	–	–	0.35

Note: • INDEX AREA is on the corner near a ball A1 (Top View side).

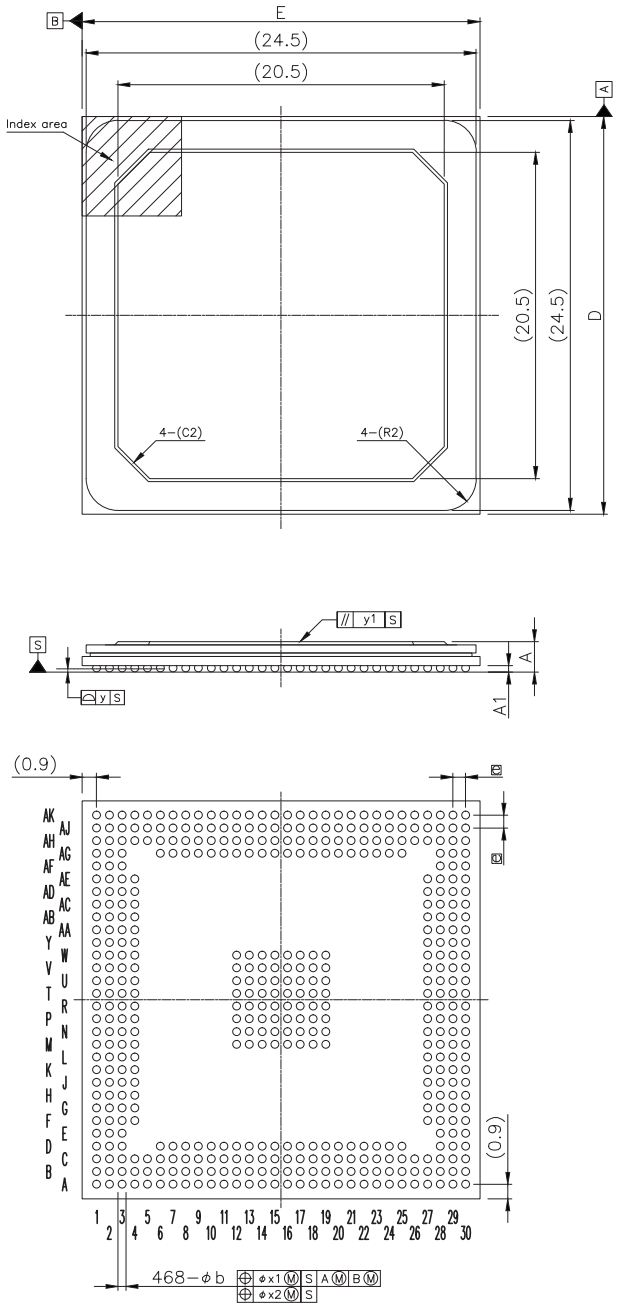
Figure 4.1 FCC-FCBGA (600pin) outline

4.1.2 FCBGA468 Package Drawing

4.1.2.1 FCBGA468 Package Drawing for U2B24-FCC

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HFBGA468-25x25-0.80	PRBG0468GF-A	—	4.4

Unit:mm



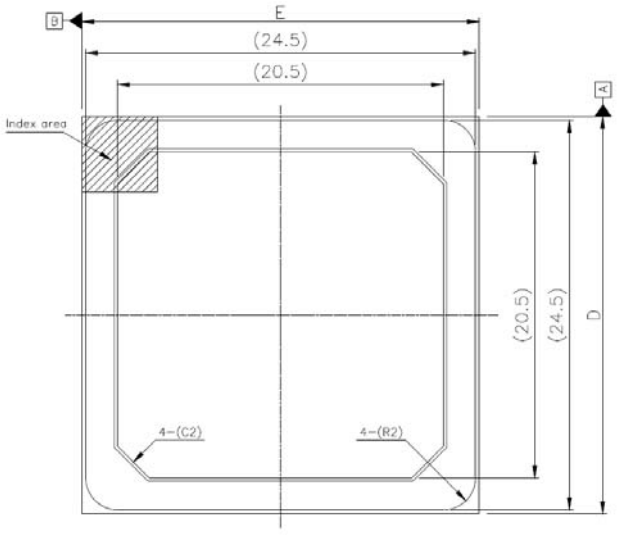
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	24.8	25.0	25.2
E	24.8	25.0	25.2
A	–	–	2.2
A1	0.31	0.36	0.41
e	–	0.80	–
b	0.45	0.50	0.55
X1	–	–	0.20
X2	–	–	0.08
y	–	–	0.20
y1	–	–	0.35

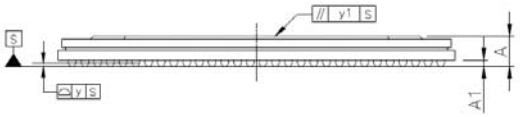
Note: • INDEX AREA is on the corner near a ball A1 (Top View side).

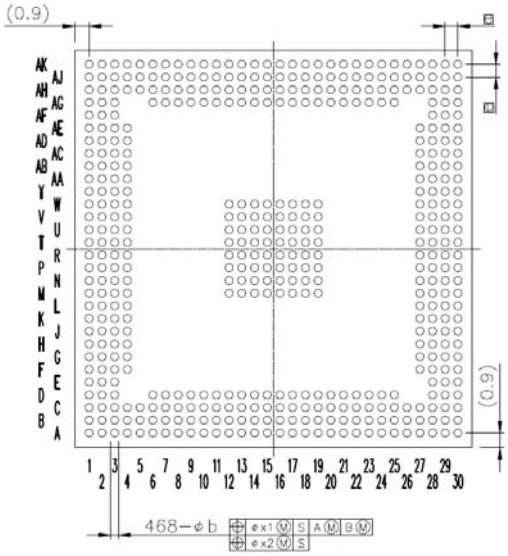
Figure 4.2 FCC-FCBGA (468pin) outline

4.1.2.2 FCBGA468 Package Drawing for U2B24

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HFBGA468-25x25-0.80	PRBG0468GG-A	————	TBD







T.B.D.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	24.8	25.0	25.2
E	24.8	25.0	25.2
A	–	–	2.1
A1	0.33	0.38	0.43
⊡	–	0.80	–
b	0.45	0.50	0.55
X1	–	–	0.20
X2	–	–	0.08
y	–	–	0.20
y1	–	–	0.35

Note: • INDEX AREA is on the corner near a ball A1 (Top View side).
• Each value will be fixed after Package qualification.

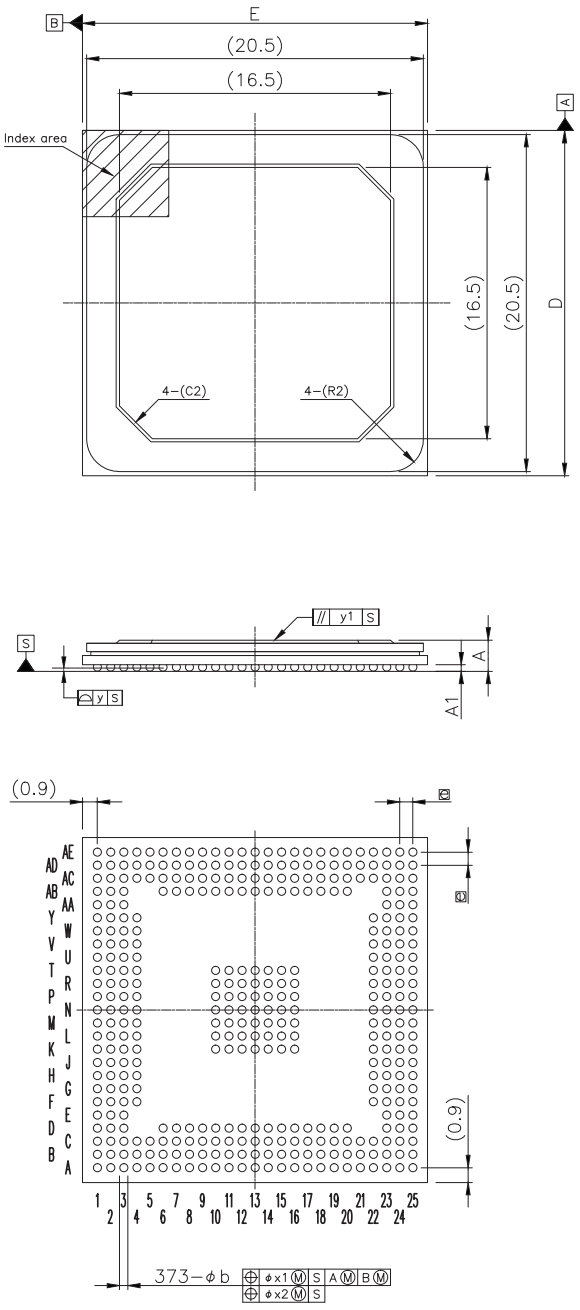
Figure 4.3 FCBGA (468pin) outline

4.1.3 FCBGA373 Package Drawing

4.1.3.1 FCBGA373 Package Drawing for U2B24-FCC

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HFBGA373-21x21-0.80	PRBG0373GC-A	—	3.0

Unit:mm



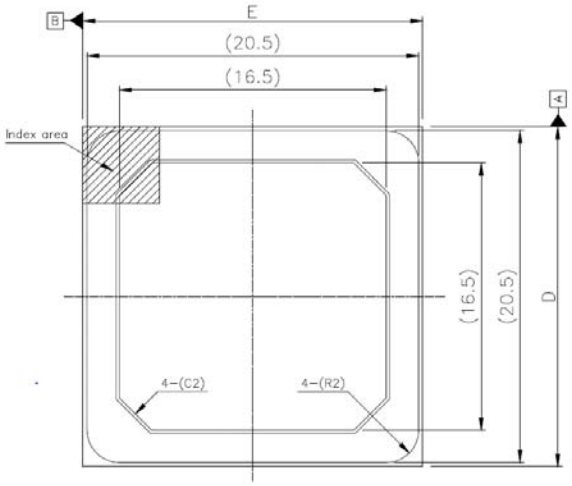
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	20.85	21.0	21.15
E	20.85	21.0	21.15
A	–	–	2.2
A1	0.31	0.36	0.41
e	–	0.80	–
b	0.45	0.50	0.55
X1	–	–	0.20
X2	–	–	0.08
y	–	–	0.15
y1	–	–	0.35

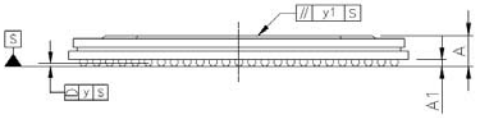
Note: • INDEX AREA is on the corner near a ball A1 (Top View side).

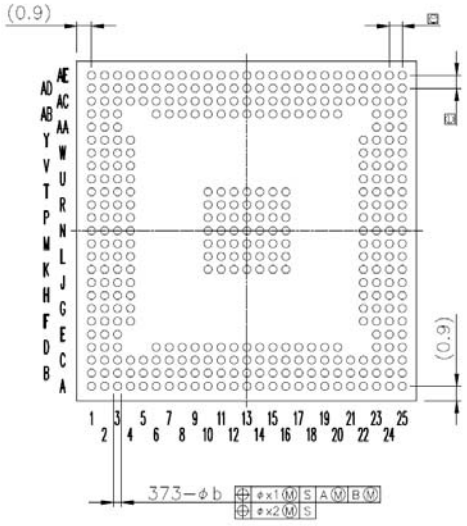
Figure 4.4 FCC-FCBGA (373pin) outline

4.1.3.2 FCBGA373 Package Drawing for U2B24

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HFBGA373-21x21-0.80	PRBG0373GD-A	————	TBD







T.B.D.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	20.85	21.0	21.15
E	20.85	21.0	21.15
A	–	–	2.1
A1	0.33	0.38	0.43
e	–	0.80	–
b	0.45	0.50	0.55
X1	–	–	0.20
X2	–	–	0.08
y	–	–	0.15
y1	–	–	0.35

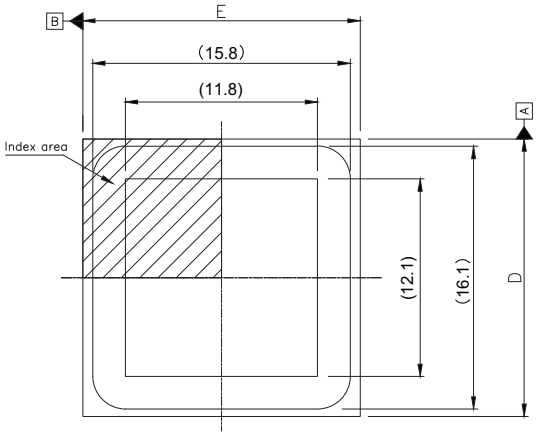
Note: • INDEX AREA is on the corner near a ball A1 (Top View side).
• Each value will be fixed after Package qualification.

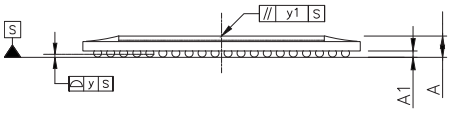
Figure 4.5 FCBGA (373pin) outline

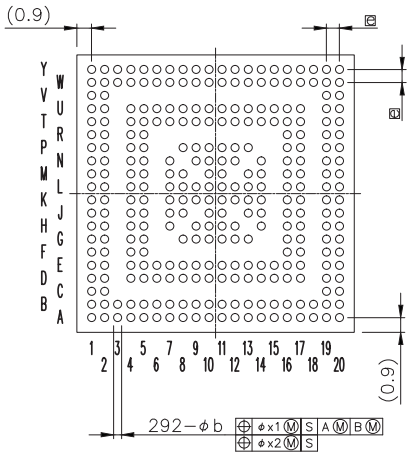
4.1.4 FCBGA292 Package Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA292-17x17-0.80	PRBG0292GF-A	—	0.79

Unit:mm







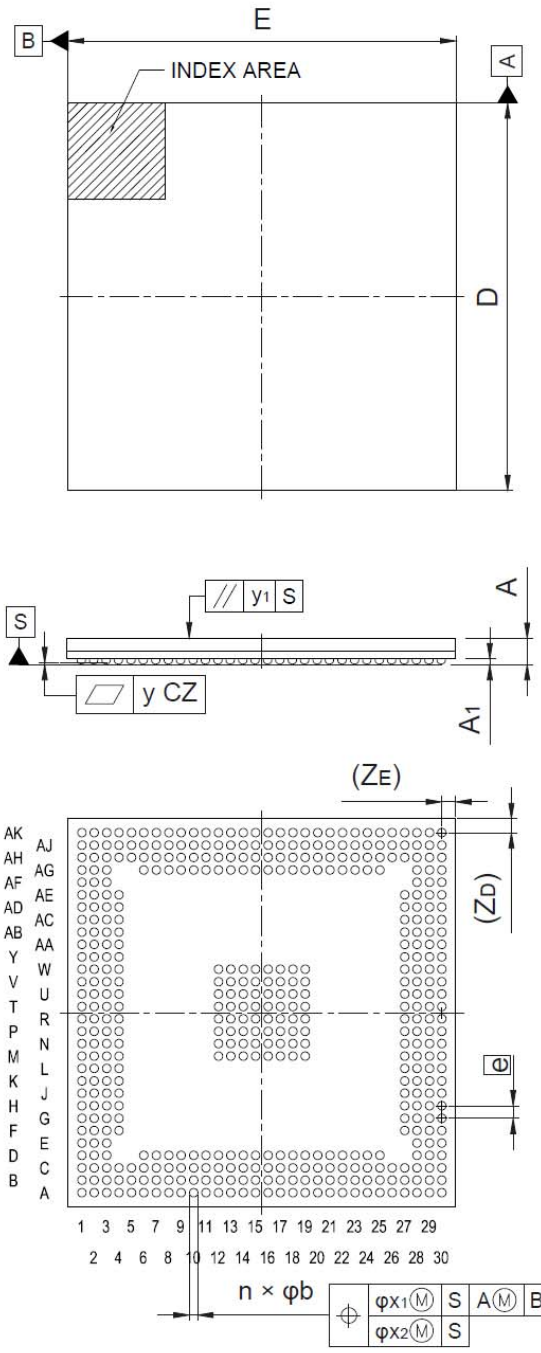
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	16.85	17.0	17.15
E	16.85	17.0	17.15
A	–	–	1.65
A1	0.31	0.36	0.41
e	–	0.80	–
b	0.45	0.50	0.55
X1	–	–	0.20
X2	–	–	0.08
y	–	–	0.15
y1	–	–	0.35

Note: • INDEX AREA is on the corner near a ball A1 (Top View side).

Figure 4.6 FCC-FCBGA (292pin) outline

4.1.5 FPBGA468 Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA468-25x25-0.80	PRBG0468GD-A	2.00



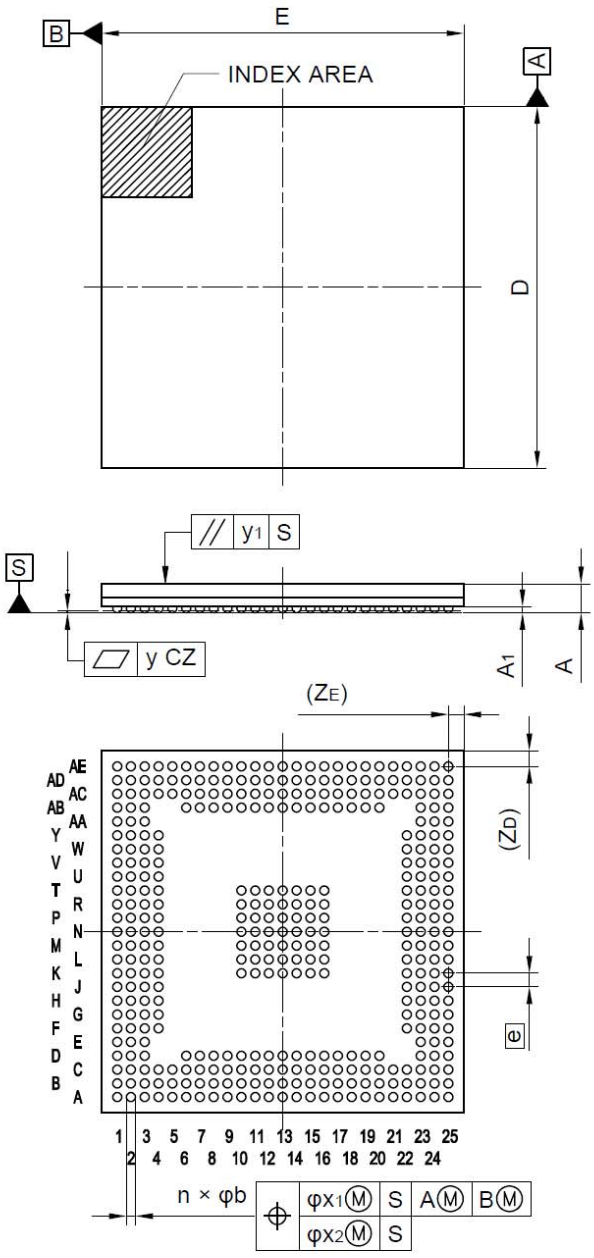
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	24.90	25.00	25.10
E	24.90	25.00	25.10
A	—	—	2.00
A_1	0.29	0.34	0.39
e	—	0.80	—
b	0.50	0.55	0.60
x_1	—	—	0.20
x_2	—	—	0.08
y	—	—	0.15
y_1	—	—	0.20
n	—	468	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Note: • INDEX AREA is on the corner near a ball A1 (Top View side).
• Each value will be fixed after Package qualification.

Figure 4.7 FPBGA (468pin) outline

4.1.6 FPBGA373 Package Drawing

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA373-21x21-0.80	PRBG0373GB-A	1.4



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	20.90	21.00	21.10
E	20.90	21.00	21.10
A	—	—	2.00
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.49	0.54	0.59
x_1	—	—	0.20
x_2	—	—	0.08
y	—	—	0.10
y_1	—	—	0.20
Z_D	—	0.90	—
Z_E	—	0.90	—
n	—	373	—

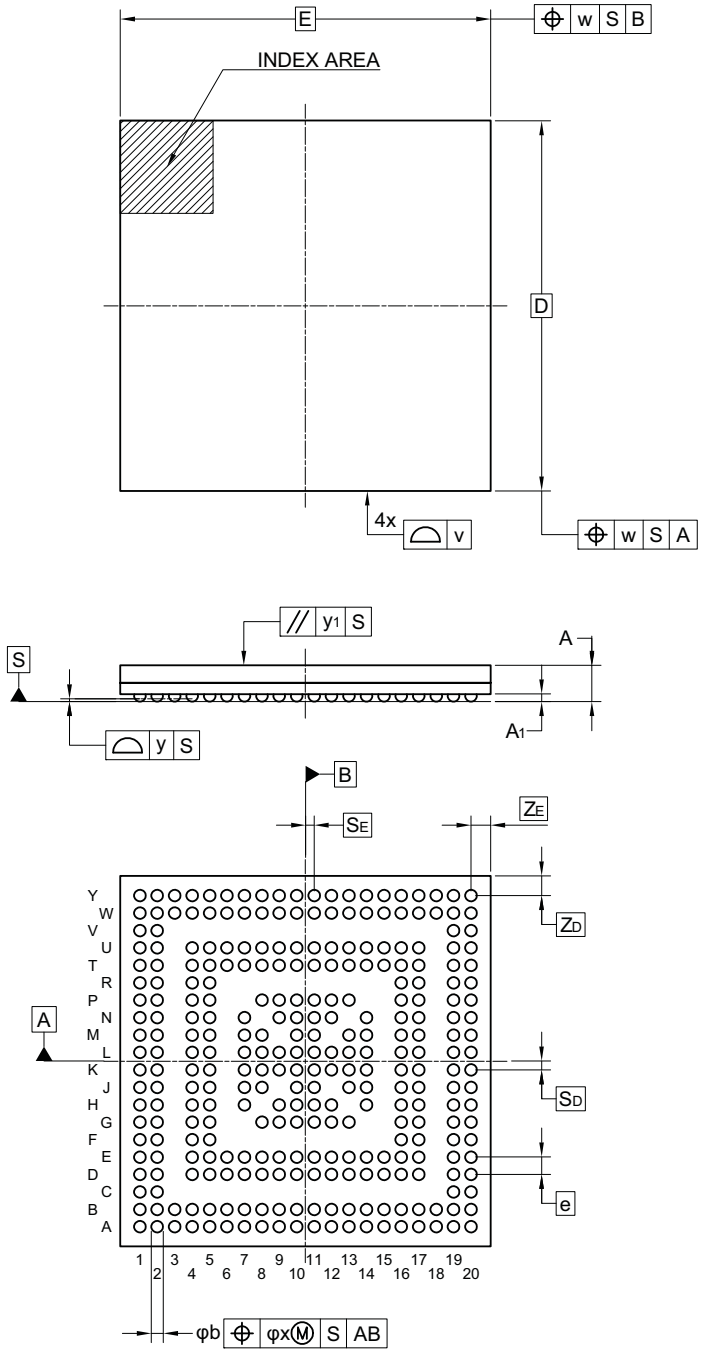
Note: • INDEX AREA is on the corner near a ball A1 (Top View side).
• Each value will be fixed after Package qualification.

Figure 4.8 FPBGA (373pin) outline

4.1.7 FPBGA292 Package Drawing

4.1.7.1 FPBGA292 Package Drawing for U2B10, U2B6

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA292-17x17-0.80	PRBG0292GC-A	T292F1-80-GNP	0.9



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	-	17.00	-
E	-	17.00	-
A	-	-	1.90
A_1	0.30	0.35	0.40
e	-	0.80	-
b	0.50	0.55	0.60
x	-	-	0.12
y	-	-	0.10
y_1	-	-	0.20
Z_D	-	0.90	-
Z_E	-	0.90	-
v	-	-	0.15
w	-	-	0.20
S_D	-	0.40	-
S_E	-	0.40	-

Note: • INDEX AREA is on the corner near a ball A1 (Top View side).

Figure 4.9 FPBGA (292pin) outline

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.03.31	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

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(Rev.5.0-1 October 2020)

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