

RJF0626JNS

N Channel Thermal FET
Power Switching

R07DS1559EJ0100
Rev.1.00
May 28, 2024

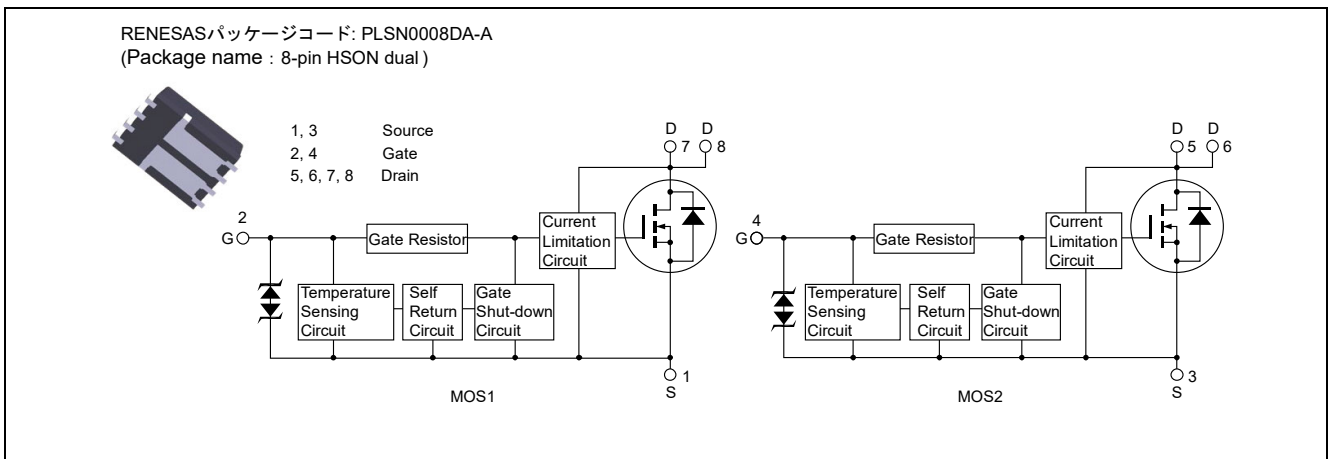
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation. (4 V Gate drive).
- Built-in the over temperature shut-down circuit and current limitation circuit.
- High endurance capability against to the short circuit.
- Temperature hysteresis type.
- High density mounting
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101Rev-E compliant.

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	16	V
Gate to source voltage	V _{GSS}	-2.5	V
Drain current	I _D ^{Note4}	7	A
Body-drain diode reverse drain current	I _{DR}	7	A
Avalanche current	I _{AF} ^{Note 3}	7	A
Avalanche energy	E _{AR} ^{Note 3}	14.7	mJ
Channel dissipation	P _{ch} ^{Note 1}	30	W
Channel dissipation	P _{ch} ^{Note 2}	1	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. T_{ch} = 25°C, 1 Drive operation.
 2. 1 Drive operation : When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)
 3. T_{ch} = 25°C, R_g ≥ 50 Ω
 4. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	—	—	V	
	V _{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	100	μA	V _i = 8 V, V _{DS} = 0
	I _{IH2}	—	—	50	μA	V _i = 3.5 V, V _{DS} = 0
	I _{IL}	—	—	1	μA	V _i = 1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sd)1}	—	0.8	—	mA	V _i = 8 V, V _{DS} = 0
	I _{IH(sd)2}	—	0.35	—	mA	V _i = 3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature
Return temperature	Thr	—	120	—	°C	Channel temperature
Gate operation voltage	V _{op}	3.5	—	12	V	
Drain current (Current limitation value)	I _{D limit}	7	—	—	A	V _i = 5 V, V _{DS} = 10 V ^{Note 5}

Notes: 5. Pulse test

Electrical Characteristics

(Ta = 25°C)

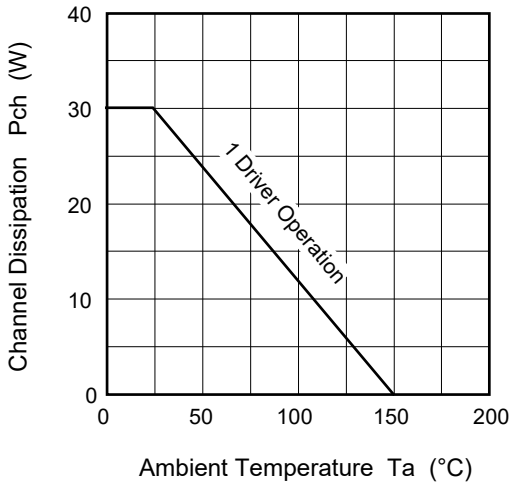
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	10	mA	V _{GS} = 1.2 V, V _{DS} = 10 V
	I _{D2}	7	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 6}
Drain to source breakdown voltage	V _{(BR)DSS}	60	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	16	—	—	V	I _G = 800 μA, V _{DS} = 0
	V _{(BR)GSS}	-2.5	—	—	V	I _G = -100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	100	μA	V _{GS} = 8 V, V _{DS} = 0
	I _{GSS}	—	—	50	μA	V _{GS} = 3.5 V, V _{DS} = 0
	I _{GSS}	—	—	1	μA	V _{GS} = 1.2 V, V _{DS} = 0
	I _{GSS}	—	—	-100	μA	V _{GS} = -2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)}	—	0.8	—	mA	V _{GS} = 8 V, V _{DS} = 0
	I _{GS(OP)}	—	0.35	—	mA	V _{GS} = 3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.1	—	2.1	V	V _{DS} = 10 V, I _D = 1 mA
Static drain to source on state resistance	R _{DS(on)}	—	79.9	100	mΩ	I _D = 3.5 A, V _{GS} = 4V ^{Note 6}
	R _{DS(on)}	—	64.9	80	mΩ	I _D = 3.5 A, V _{GS} = 10 V ^{Note 6}
Forward transfer admittance	y _{fs}	3.3	10.3	—	S	I _D = 3.5 A, V _{GS} = 10 V ^{Note 6}
Output capacitance	C _{oss}	—	286	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	3.9	—	μs	V _{GS} = 5 V, I _D = 3.5 A, R _L = 8.5 Ω
Rise time	t _r	—	18.6	—	μs	
Turn-off delay time	t _{d(off)}	—	3.2	—	μs	
Fall time	t _f	—	6.4	—	μs	
Body-drain diode forward voltage	V _{DF}	—	0.8	—	V	I _F = 7 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	134	—	ns	I _F = 7 A, V _{GS} = 0 di _F /dt = 50 A/μs
Over load shut down operation time ^{Note 7}	t _{os1}	—	0.42	—	ms	V _{GS} = 5 V, V _{DD} = 16 V
Over load shut down operation time ^{Note 7}	t _{os2}	—	0.27	—	ms	V _{GS} = 5 V, V _{DD} = 24 V

Notes: 6. Pulse test

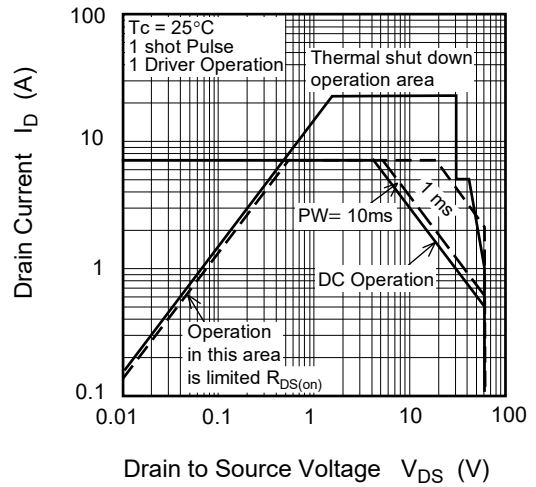
7. Including the junction temperature rise of the over loaded condition.

Main Characteristics

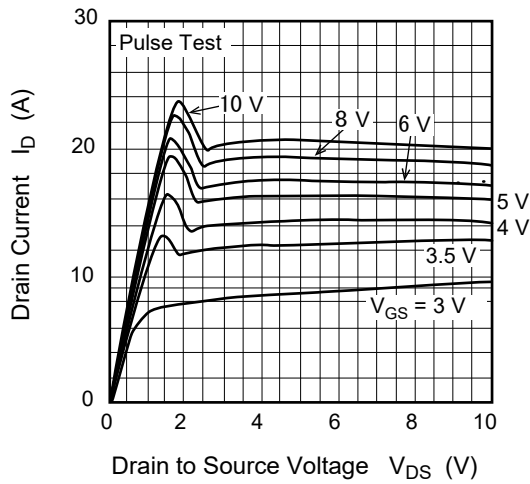
Power vs. Temperature Derating



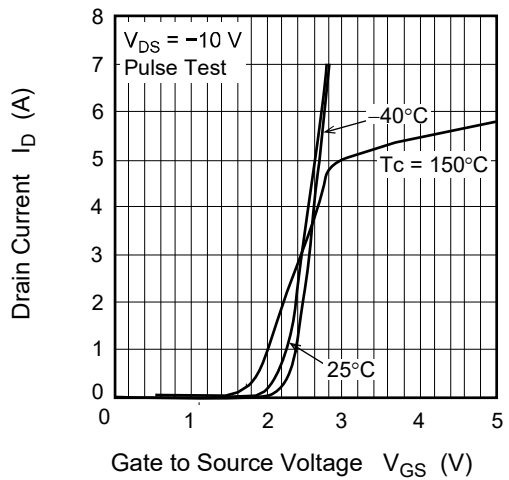
Maximum Safe Operation Area



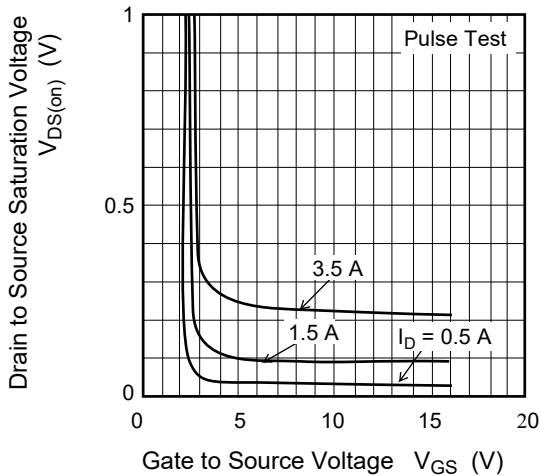
Typical Output Characteristics



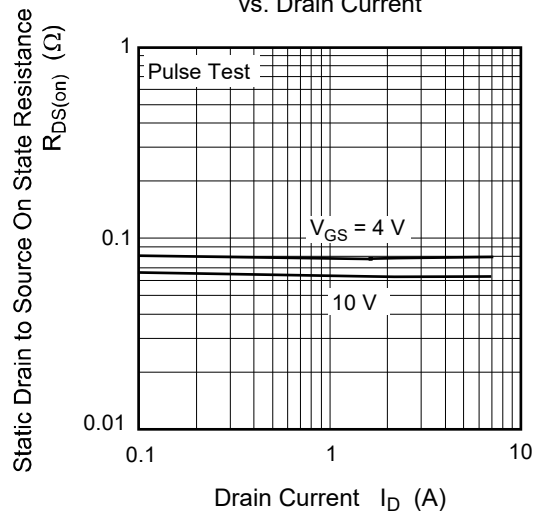
Typical Transfer Characteristics



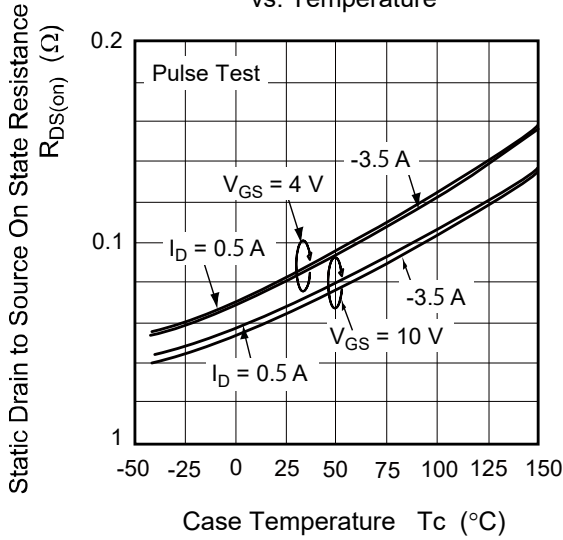
Drain to Source Saturation Voltage vs. Gate to Source Voltage



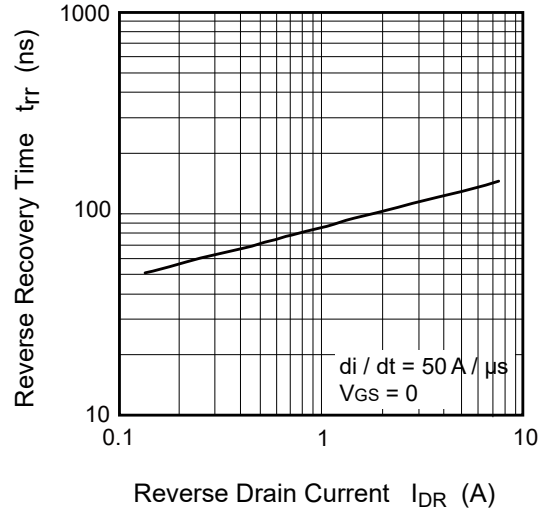
Static Drain to Source On State Resistance vs. Drain Current



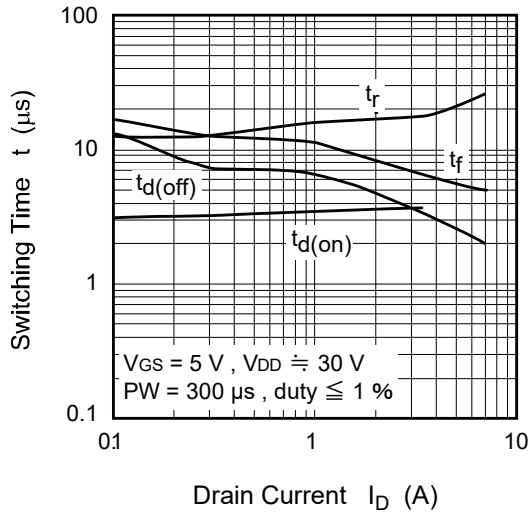
Static Drain to Source On State Resistance vs. Temperature



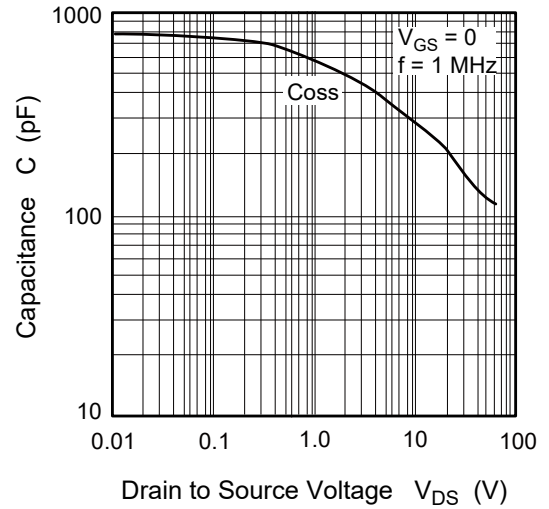
Body-Drain Diode Reverse Recovery Time



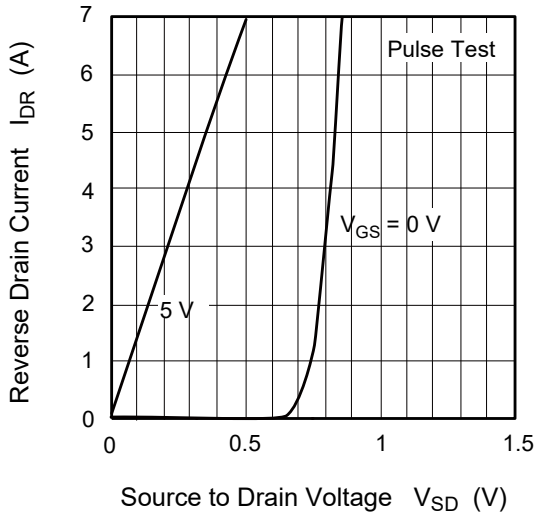
Switching Characteristics



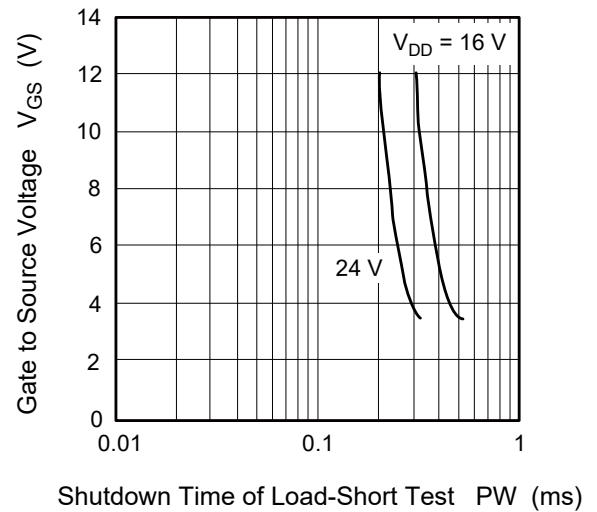
Typical Capacitance vs. Drain to Source Voltage

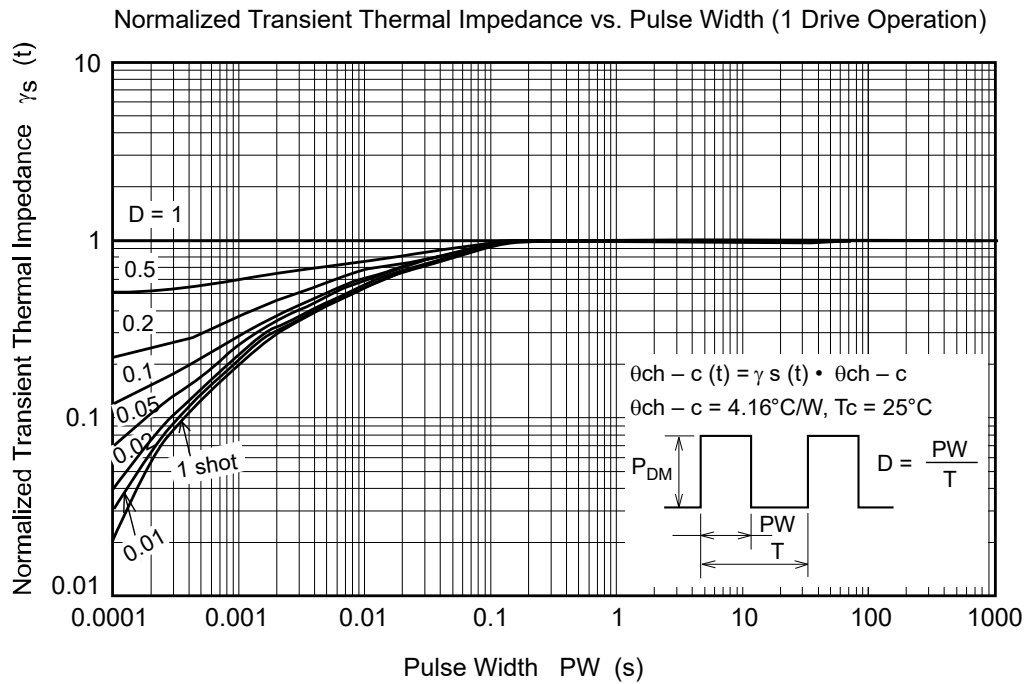
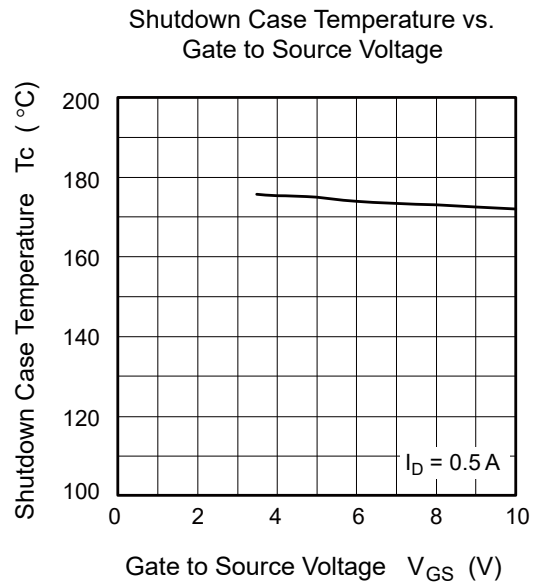
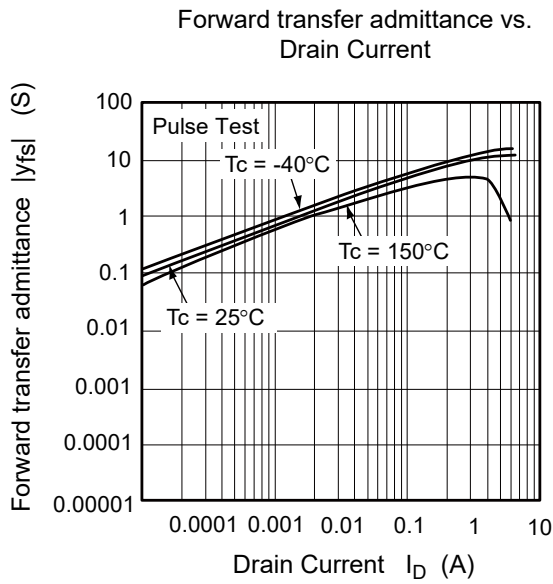


Reverse Drain Current vs. Source to Drain Voltage

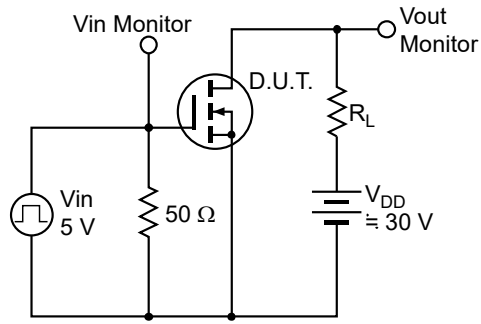


Gate to Source Voltage vs. Shutdown Time of Load-Short Test

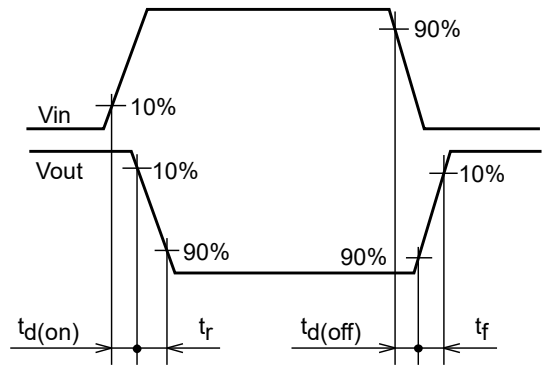




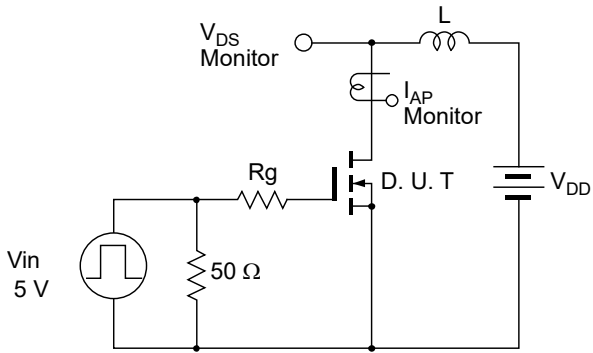
Switching Time Test Circuit



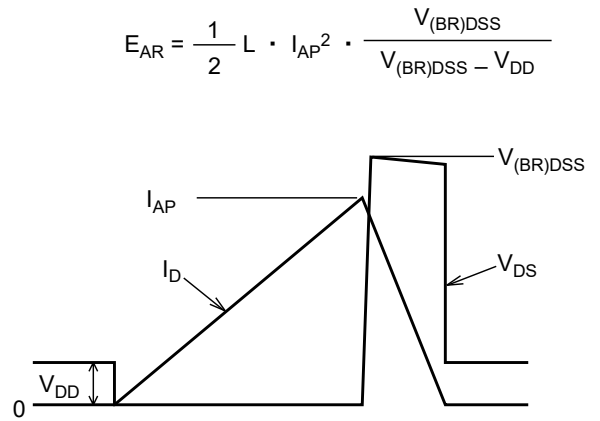
Waveform



Avalanche Test Circuit



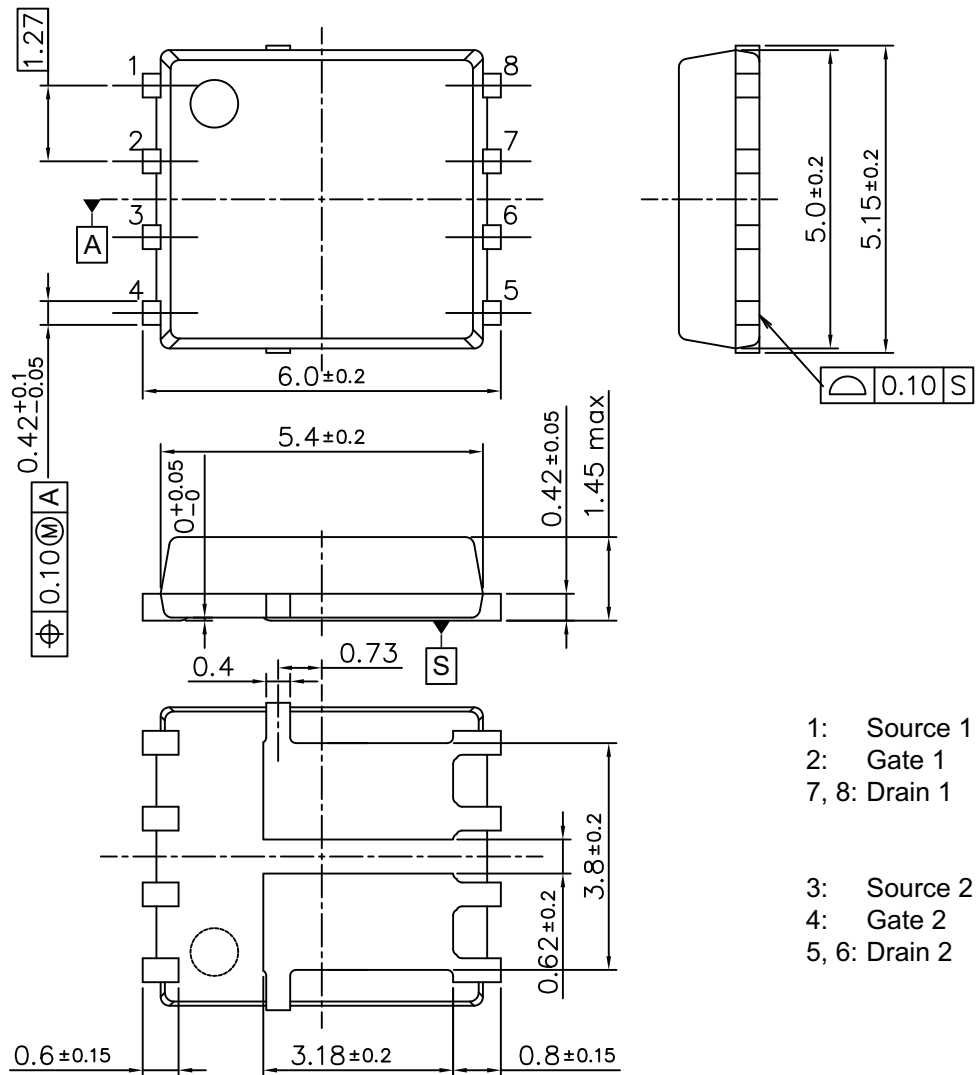
Avalanche Waveform



Package Dimensions

8-pin HSON Dual (Mass: 0.12 g TYP.)

Renesas package code: PLSN0008DA-A



- 1: Source 1
- 2: Gate 1
- 7, 8: Drain 1

- 3: Source 2
- 4: Gate 2
- 5, 6: Drain 2

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJF0626JNS-00-Q7	2500 pcs/reel	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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