

RJK0369DSP

Silicon N Channel Power MOS FET Power Switching

REJ03G1662-0201

Rev.2.01

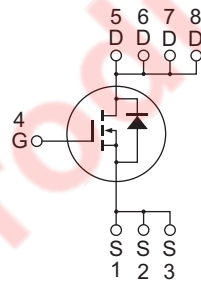
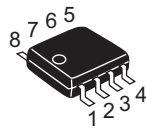
Apr 24, 2008

Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 12.0 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8<FP-8DAV>)



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	9	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	72	A
Body-drain diode reverse drain current	I_{DR}	9	A
Avalanche current	I_{AP} ^{Note 2}	8	A
Avalanche energy	E_{AR} ^{Note 2}	6.4	mJ
Channel dissipation	P_{ch} ^{Note 3}	1.8	W
Channel to ambient thermal impedance	θ_{ch-a} ^{Note 3}	69.4	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{s}$

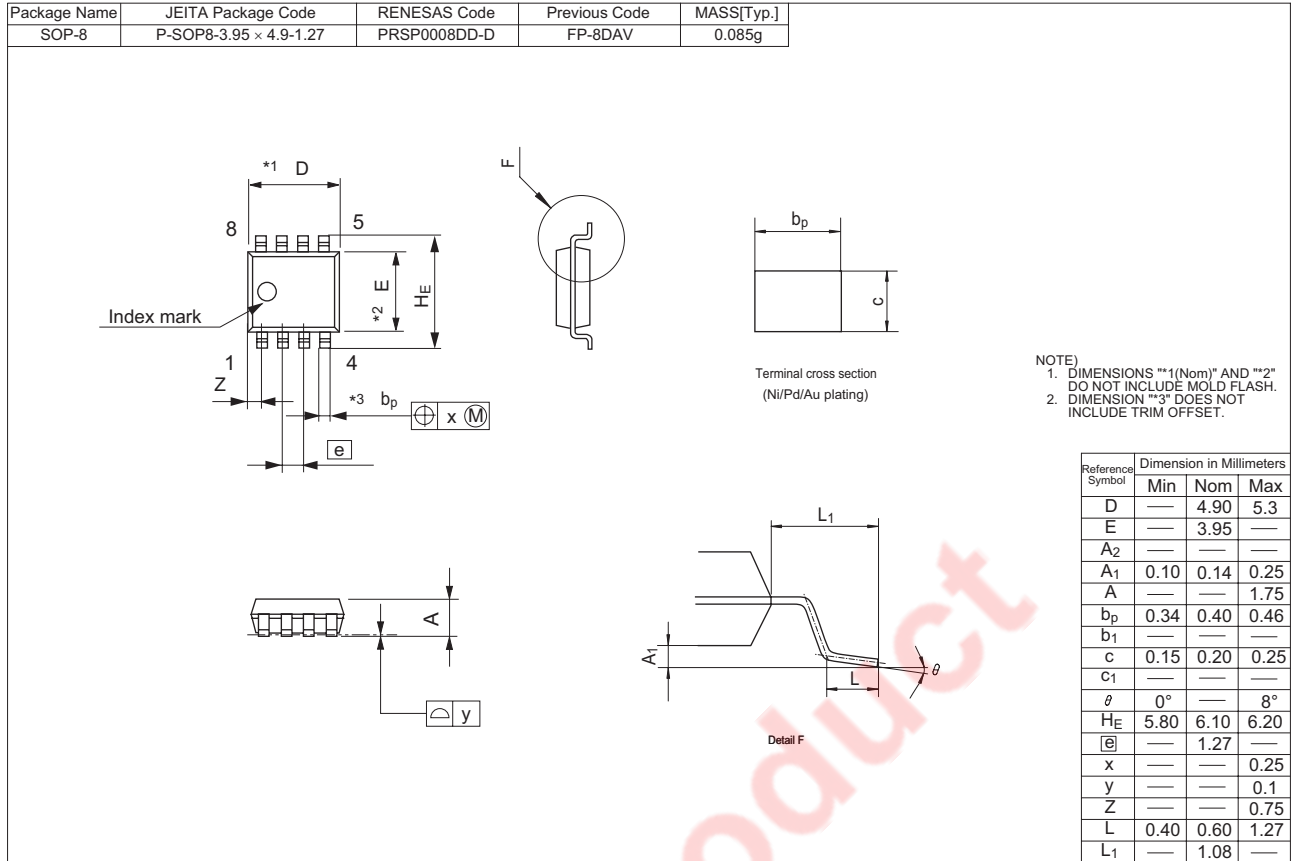
Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	12	15.6	$\text{m}\Omega$	$I_D = 4.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	16	22.5	$\text{m}\Omega$	$I_D = 4.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	20	—	S	$I_D = 4.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	810	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	155	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	50	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.4	—	Ω	
Total gate charge	Q_g	—	5.6	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	2.1	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	1.2	—	nC	$I_D = 4.5 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	5.0	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$
Rise time	t_r	—	3.0	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	33	—	ns	$R_L = 2.22 \Omega$
Fall time	t_f	—	4.1	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 9 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	15	—	ns	$I_F = 9 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJK0369DSP-00-J0	2500 pcs	Taping

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April 1st, 2010
Renesas Electronics Corporation

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