

# RJK5012DPP

Silicon N Channel MOS FET  
High Speed Power Switching

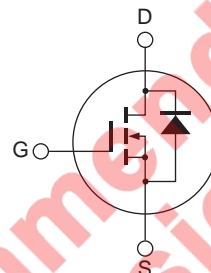
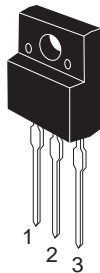
REJ03G1545-0200  
Rev.2.00  
Jun 30, 2010

## Features

- Low on-resistance
- Low leakage current
- High speed switching

## Outline

RENESAS Package code: PRSS0003AB-A  
(Package name: TO-220FN)



1. Gate
2. Drain
3. Source

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	500	V
Gate to source voltage	$V_{GSS}$	±30	V
Drain current	$I_D$ <sup>Note4</sup>	12	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	24	A
Body-drain diode reverse drain current	$I_{DR}$	12	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ <sup>Note1</sup>	24	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	4	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	0.88	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	30	W
Channel to case thermal impedance	$\theta_{ch-c}$	4.17	°C/W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

- Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_c = 25^\circ C$   
 3.  $ST_{ch} = 25^\circ C$ ,  $T_{ch} \leq 150^\circ C$   
 4. Limited by maximum safe operation area

## Electrical Characteristics

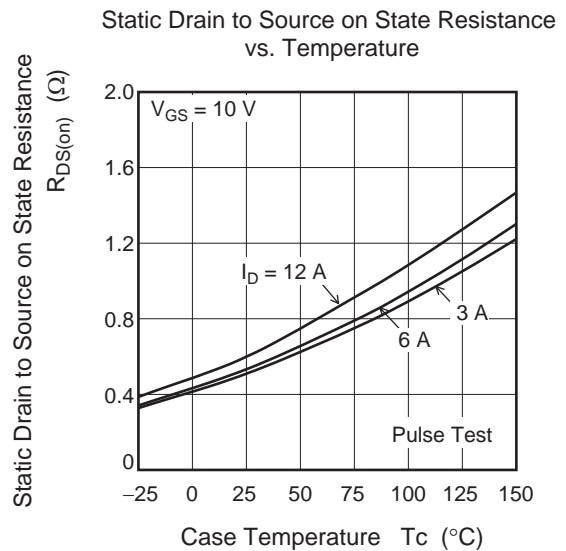
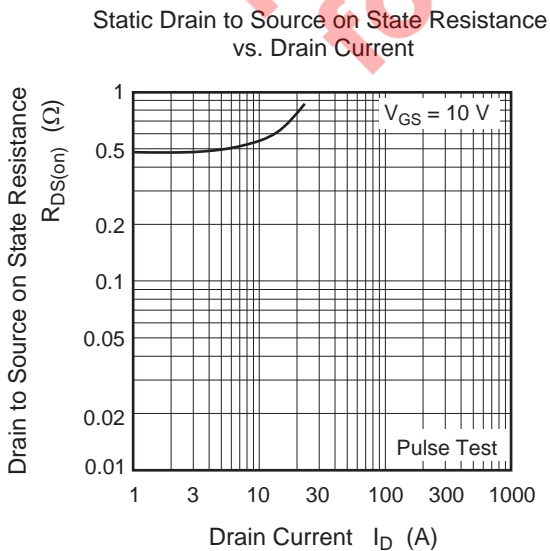
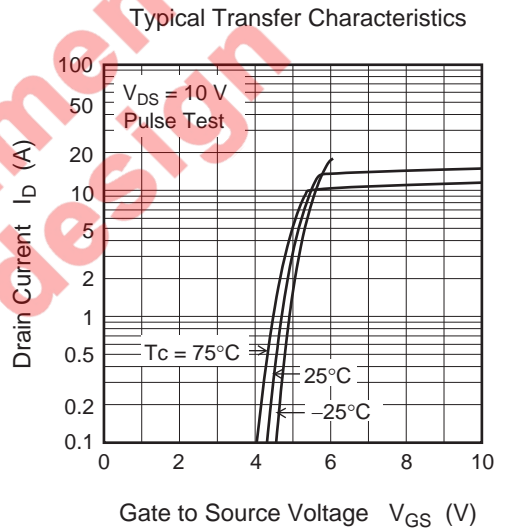
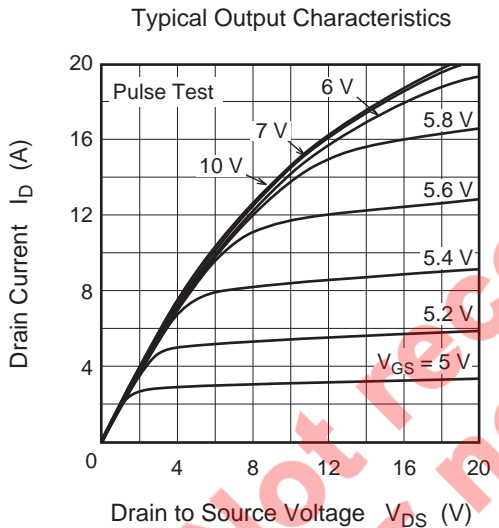
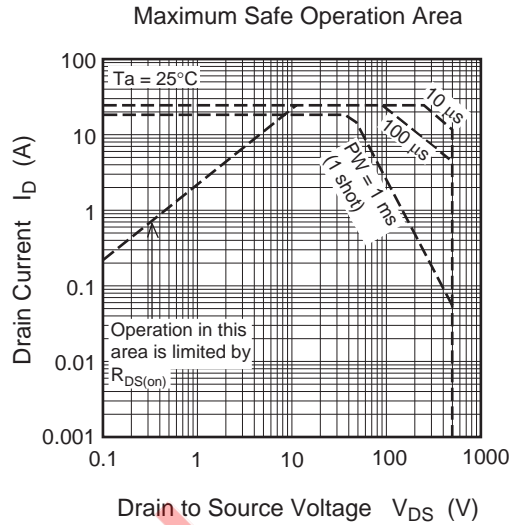
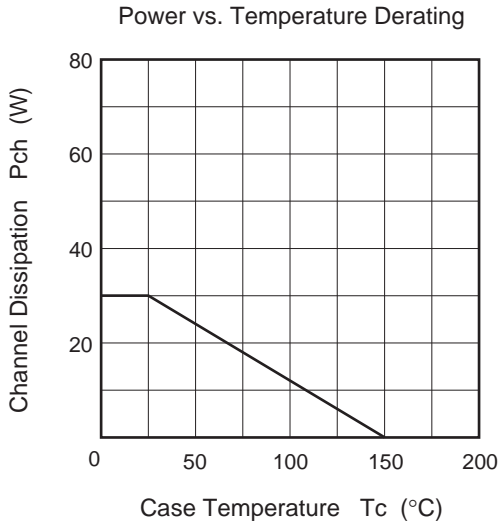
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 500 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.515	0.620	$\Omega$	$I_D = 6 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note5</sup>
Input capacitance	$C_{iss}$	—	1100	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	120	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	15	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = 6 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 41.6 \Omega$ $R_g = 10 \Omega$
Rise time	$t_r$	—	23	—	ns	
Turn-off delay time	$t_{d(off)}$	—	77	—	ns	
Fall time	$t_f$	—	16	—	ns	
Total gate charge	$Q_g$	—	29	—	nC	$V_{DD} = 400 \text{ V}$
Gate to source charge	$Q_{gs}$	—	5.5	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	13	—	nC	$I_D = 12 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.89	1.50	V	$I_F = 12 \text{ A}$ , $V_{GS} = 0$ <sup>Note5</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	280	—	ns	$I_F = 12 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

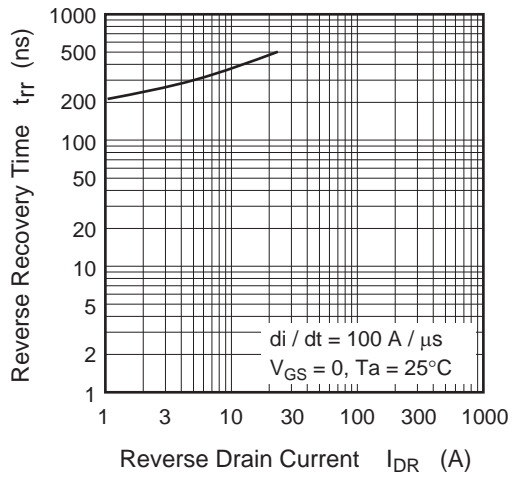
Notes: 5. Pulse test

Not recommended  
for new design

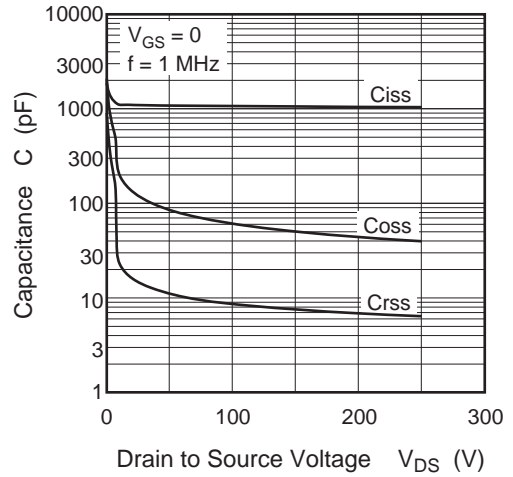
Main Characteristics



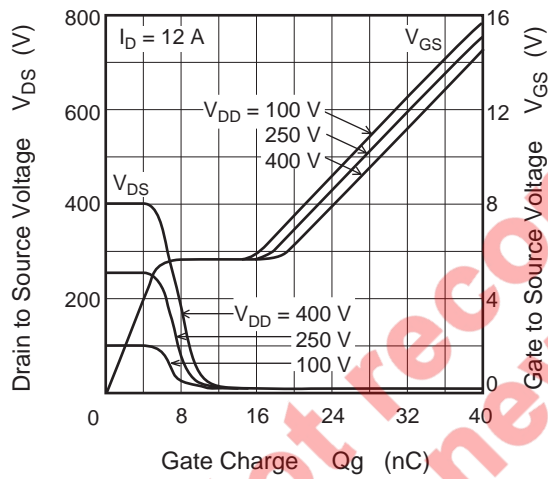
Body-Drain Diode Reverse Recovery Time



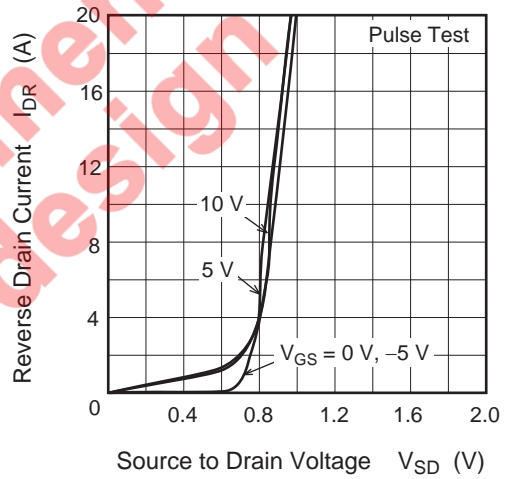
Typical Capacitance vs. Drain to Source Voltage



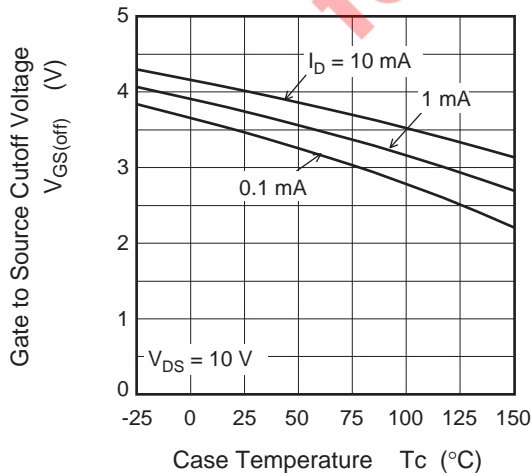
Dynamic Input Characteristics



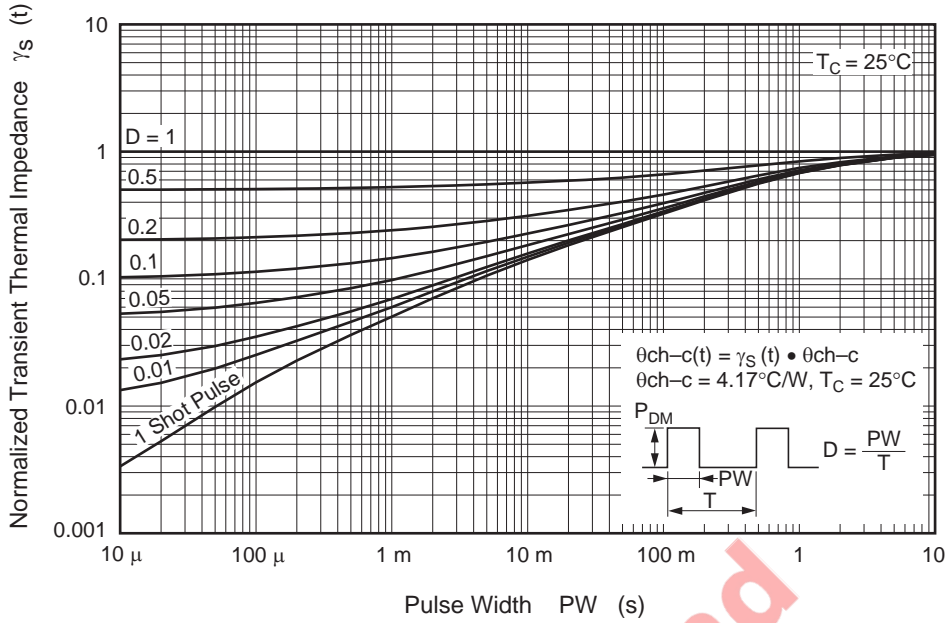
Reverse Drain Current vs. Source to Drain Voltage



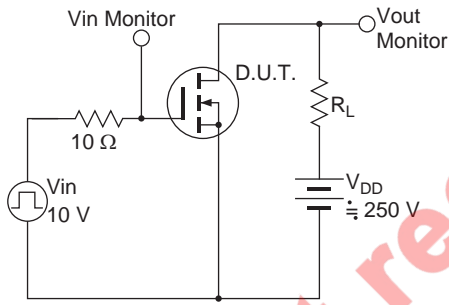
Gate to Source Cutoff Voltage vs. Case Temperature



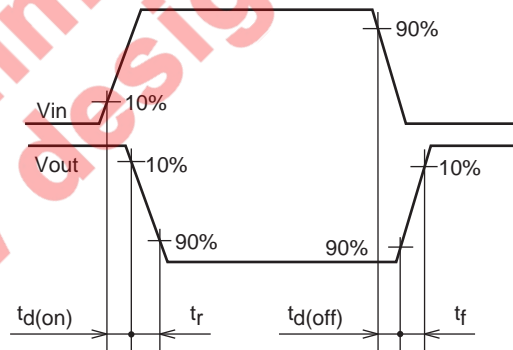
Normalized Transient Thermal Impedance vs. Pulse Width



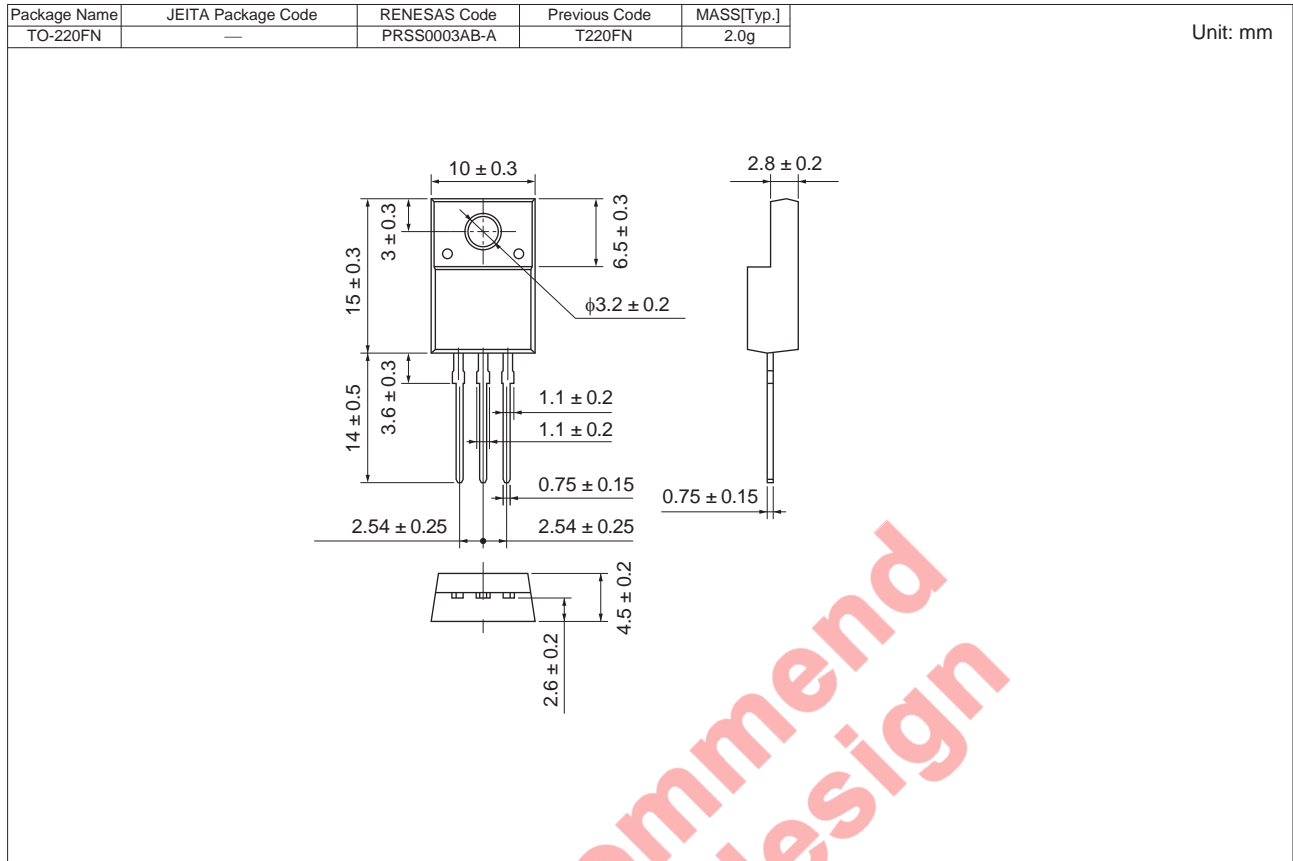
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJK5012DPP-00-T2	1050 pcs	Box (Tube)

Not recommend for new design

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**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
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Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852-2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**  
7F, No. 363 Fu Shing North Road Taipei, Taiwan  
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**Renesas Electronics Korea Co., Ltd.**  
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Tel: +82-2-558-3737, Fax: +82-2-558-5141