

# RJK6029DJA

Silicon N Channel MOS FET  
High Speed Power Switching

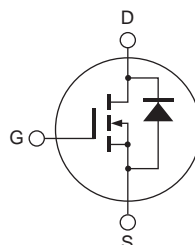
REJ03G1895-0100  
Rev.1.00  
Jun 18, 2010

## Features

- Low on-resistance  
 $R_{DS(on)} = 13.5 \Omega$  typ. (at  $I_D = 0.1 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Low drive current
- High density mounting

## Outline

RENESAS Package code: PRSS0003DA-A  
(Package name: TO-92(1))



1. Source
2. Drain
3. Gate

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	600	V
Gate to source voltage	$V_{GSS}$	$\pm 30$	V
Drain current	$I_D$	0.2	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	0.8	A
Body-drain diode reverse drain current	$I_{DR}$	0.2	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ <sup>Note1</sup>	0.8	A
Channel dissipation	Pch	0.75	W
Channel to ambient thermal impedance	$\theta_{ch-a}$	166.7	$^\circ\text{C}/\text{W}$
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

## Electrical Characteristics

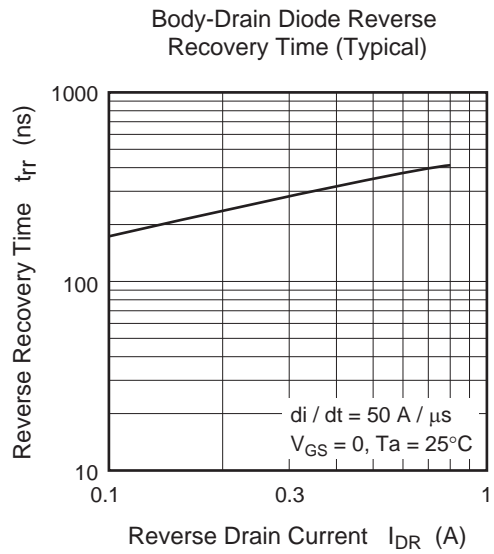
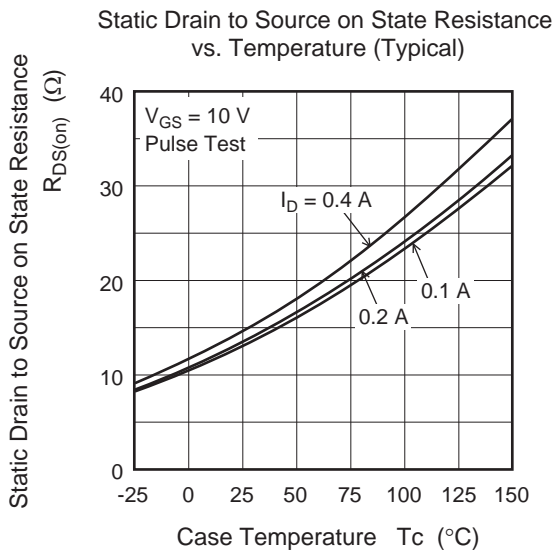
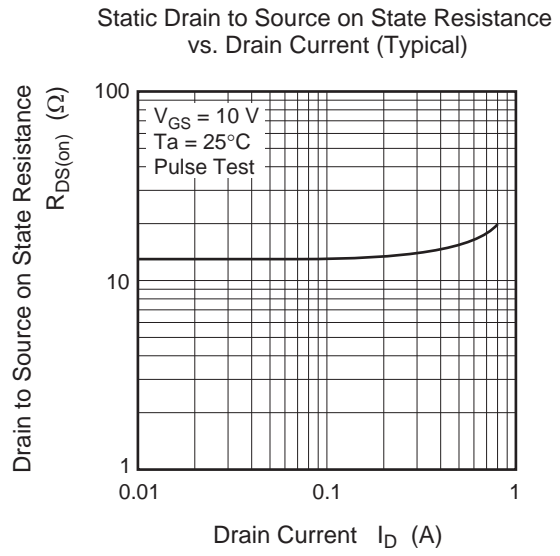
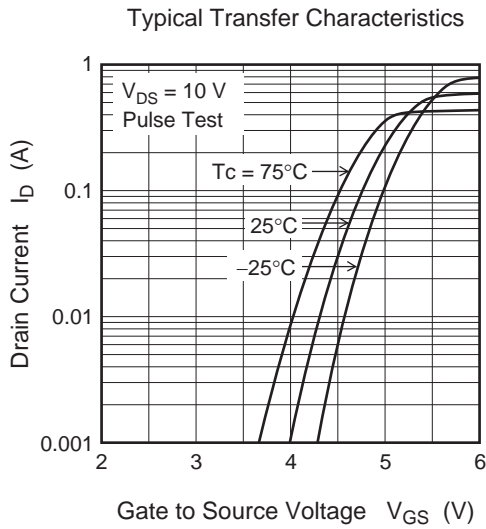
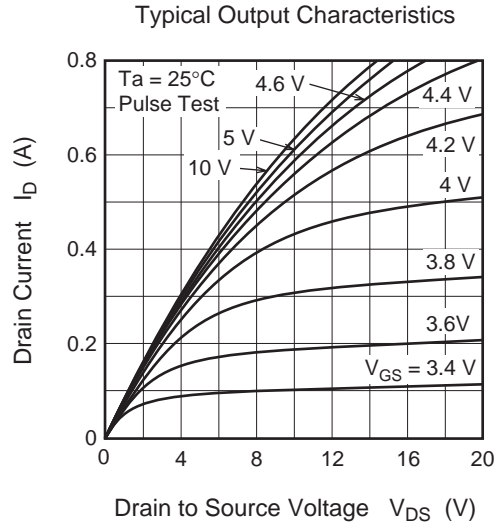
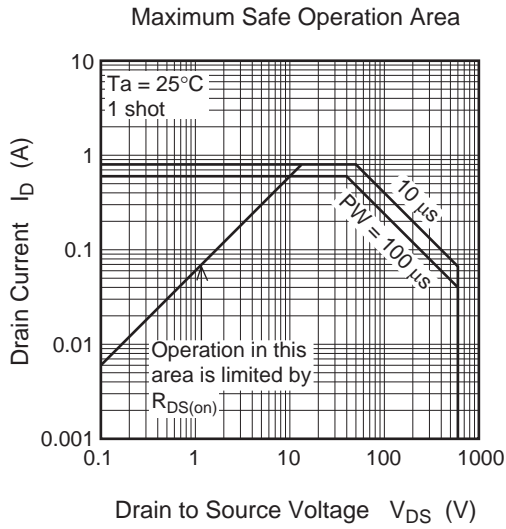
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	600	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 600 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	13.5	16.5	$\Omega$	$I_D = 0.1 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note2</sup>
Input capacitance	$C_{iss}$	—	66	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	$C_{oss}$	—	8.7	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	1.3	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = 0.1 \text{ A}$
Rise time	$t_r$	—	15	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	51	—	ns	$R_L = 3000 \Omega$
Fall time	$t_f$	—	175	—	ns	$R_g = 10 \Omega$
Total gate charge	$Q_g$	—	4.8	—	nC	$V_{DD} = 480 \text{ V}$
Gate to source charge	$Q_{gs}$	—	0.6	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	3.2	—	nC	$I_D = 0.2 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.77	1.30	V	$I_F = 0.2 \text{ A}$ , $V_{GS} = 0$ <sup>Note2</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	220	—	ns	$I_F = 0.2 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

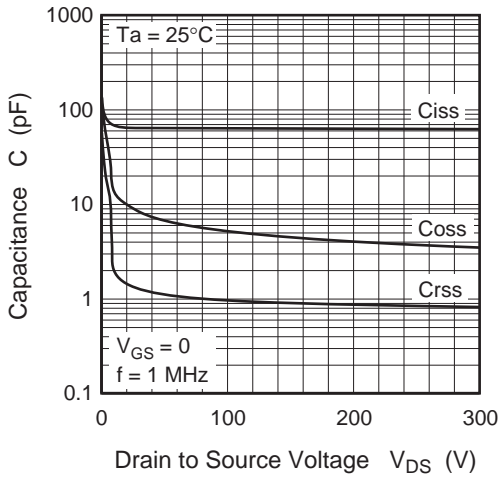
Notes: 2. Pulse test

3. Since this device is equipped with high voltage FET chip ( $V_{DSS} \geq 600 \text{ V}$ ), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.
4. This device is sensitive to electrostatic discharge. It is recommended to adopt appropriate cautions when handling this product.

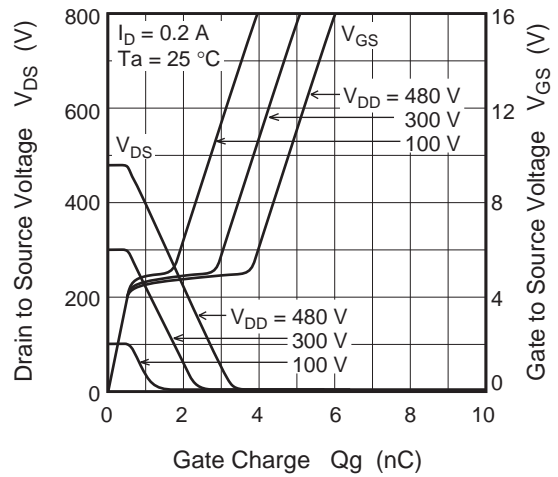
Main Characteristics



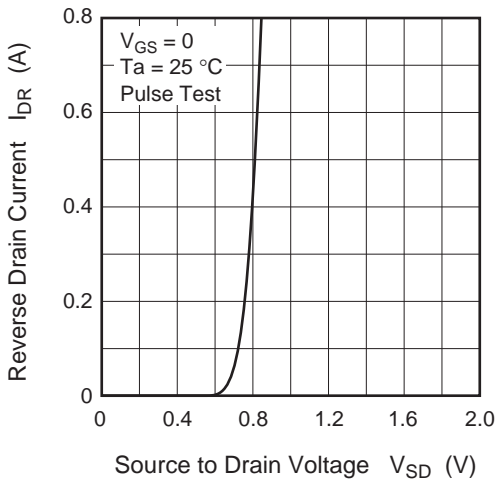
Typical Capacitance vs. Drain to Source Voltage



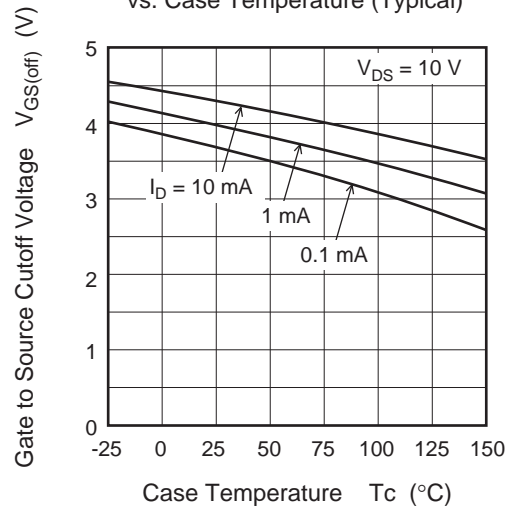
Dynamic Input Characteristics (Typical)

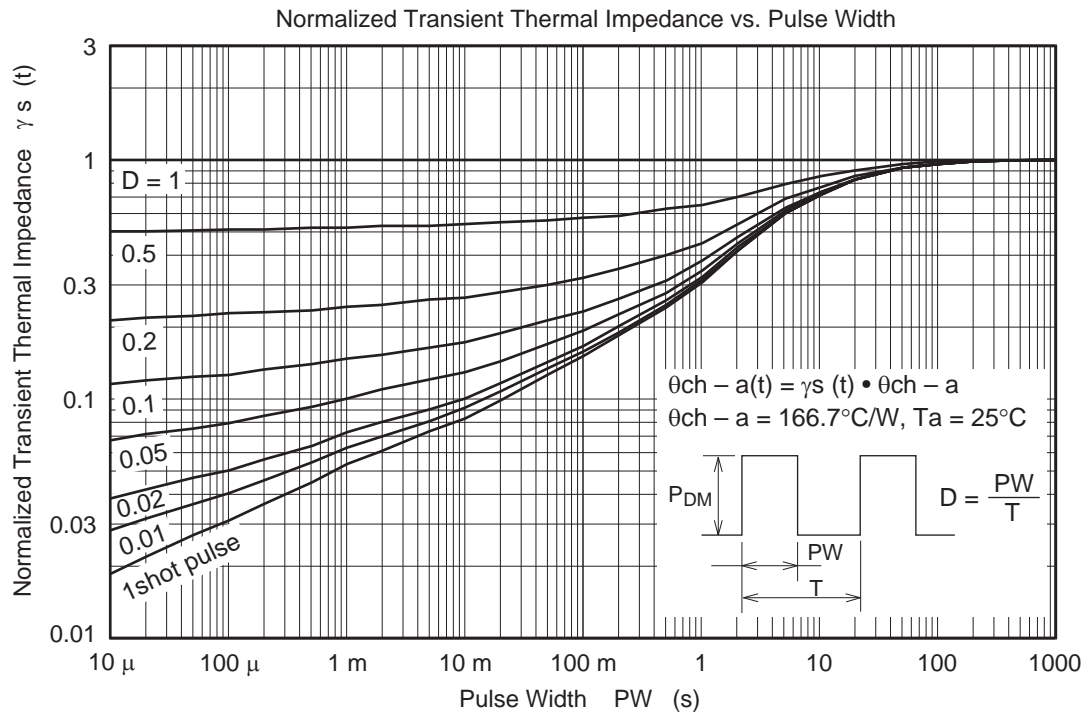


Reverse Drain Current vs. Source to Drain Voltage (Typical)

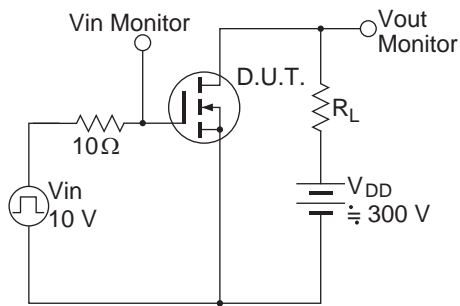


Gate to Source Cutoff Voltage vs. Case Temperature (Typical)

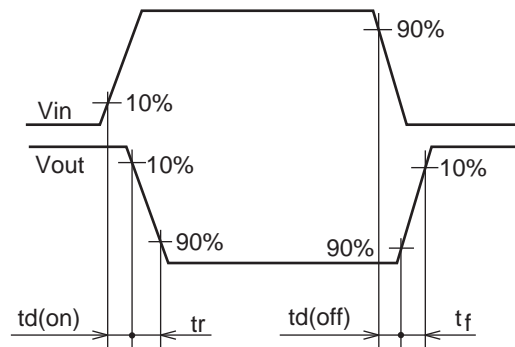




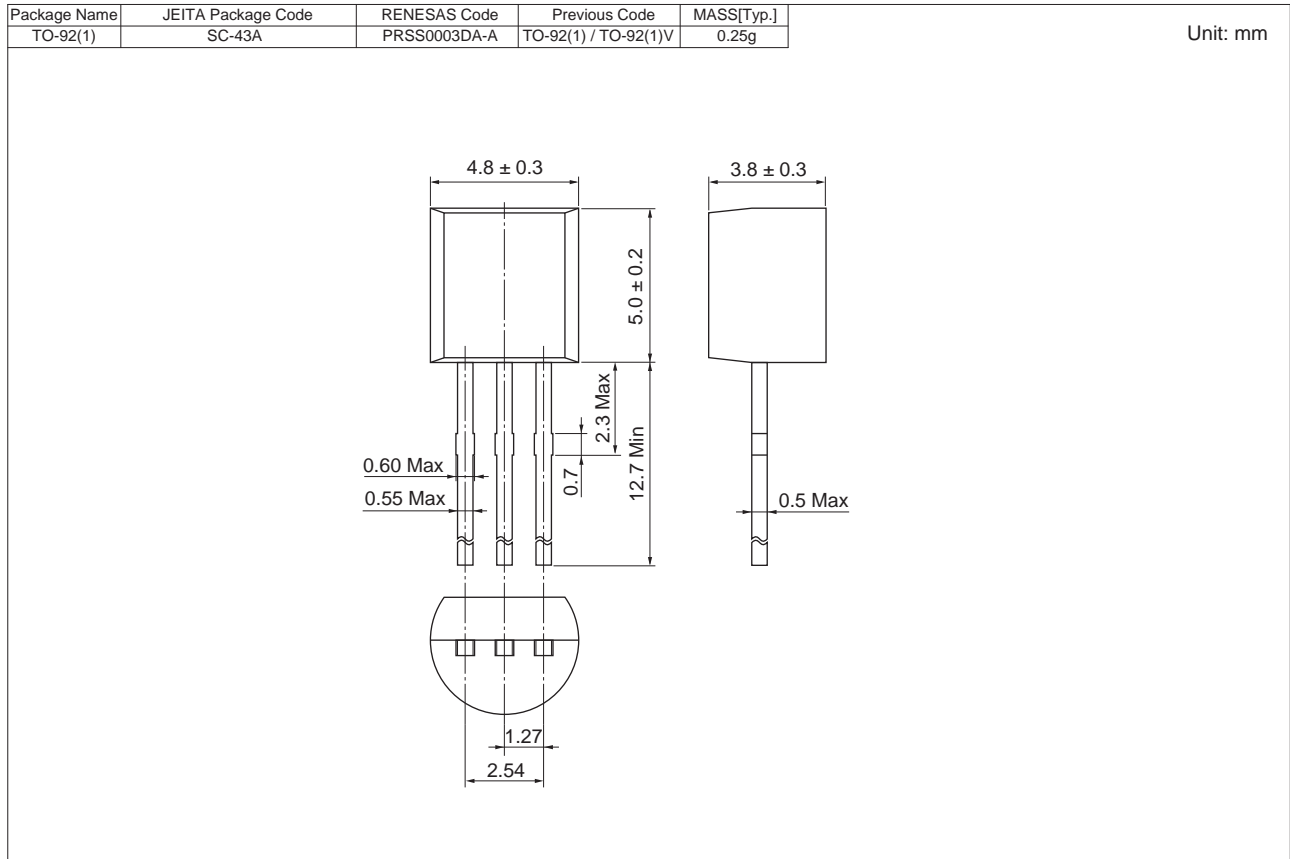
Switching Time Test Circuit



Waveform



Package Dimensions

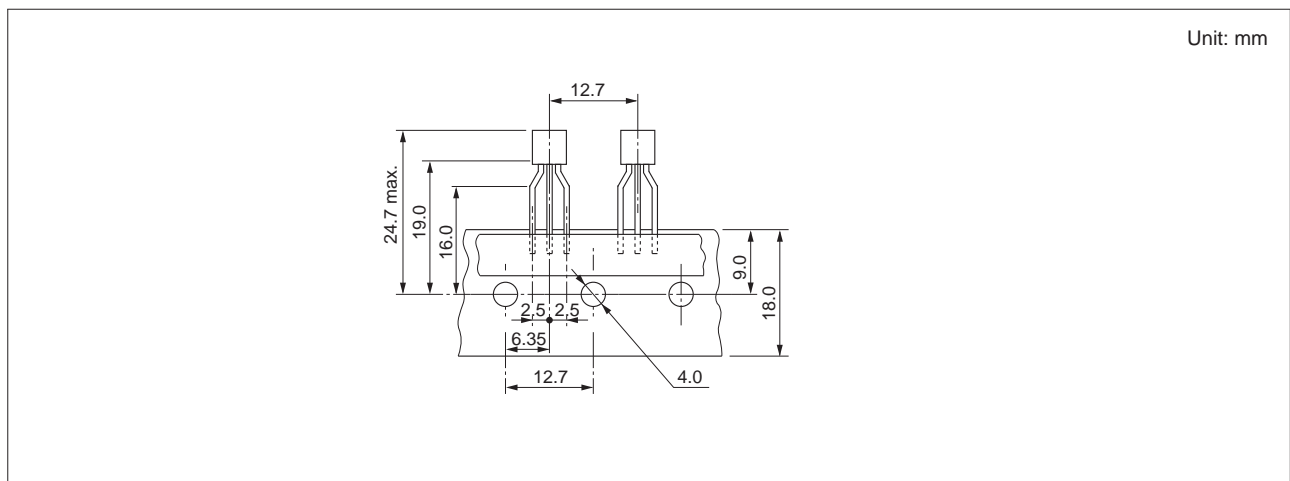


Since RJK6029DJA is equipped with high voltage FET chip ( $V_{DSS} \geq 600$  V), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.

Ordering Information

Part No.	Quantity	Shipping Container
RJK6029DJA-00-Z0	2500 pcs	Hold Box, Radial Taping

Note: Leads is forming applied as following figure.



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