

RMLV0816BGSB - 4S2

8Mb Advanced LPSRAM (512k word × 16bit)

R10DS0231EJ0201
Rev.2.01
2020.02.20

Description

The RMLV0816BGSB is a family of 8-Mbit static RAMs organized 524,288-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0816BGSB has realized higher density, higher performance and low power consumption. The RMLV0816BGSB offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44pin TSOP (II).

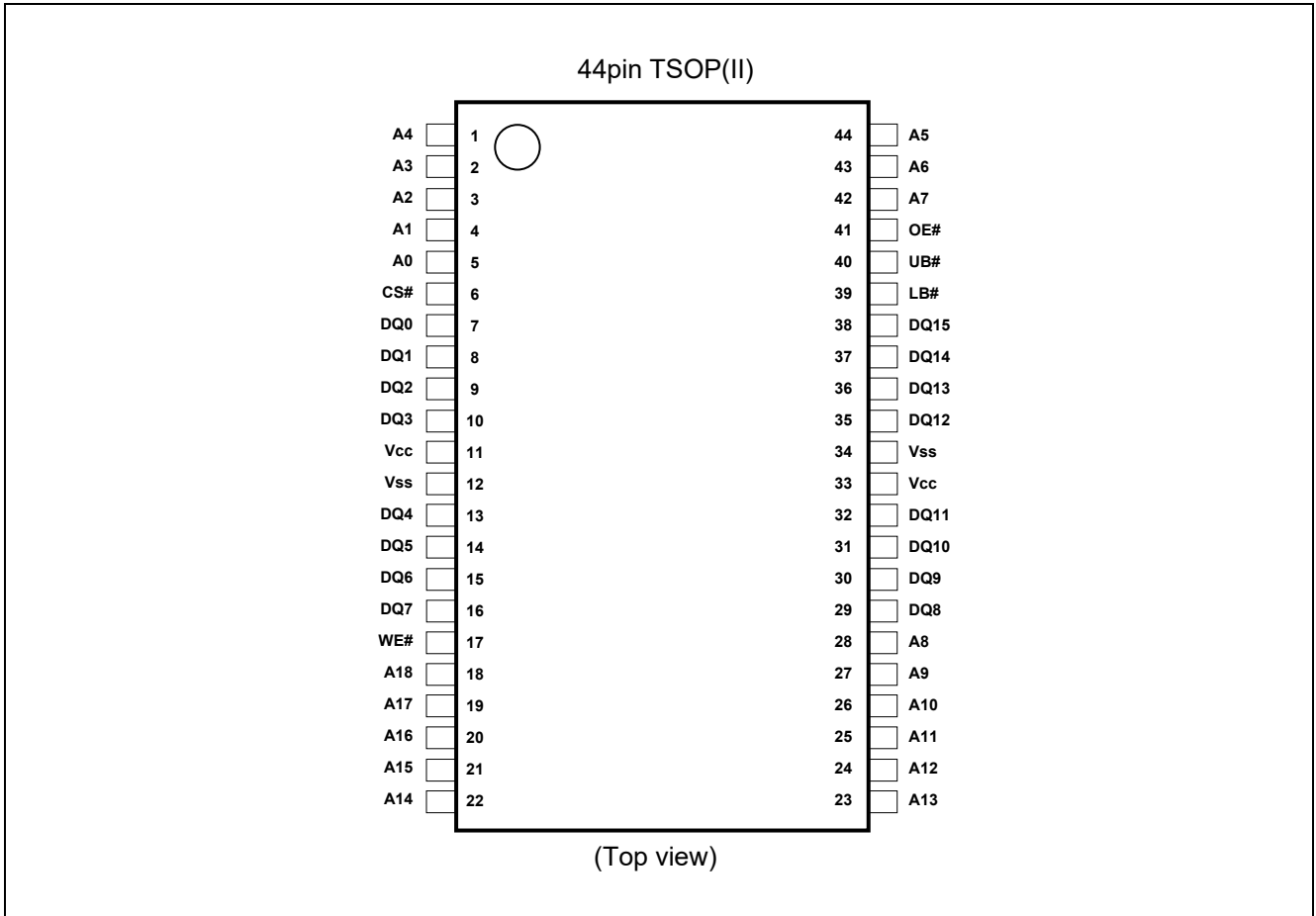
Features

- Single 3V supply: 2.4V to 3.6V
- Access time:
 - Power supply voltage from 2.7V to 3.6V: 45ns (max.)
 - Power supply voltage from 2.4V to 2.7V: 55ns (max.)
- Current consumption:
 - Standby: 0.45μA (typ.)
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Power supply	Access time	Temperature Range	Package
RMLV0816BGSB-4S2	2.7V to 3.6V	45 ns	-40 ~ +85°C	11.76mm×18.41mm 44pin plastic TSOP(II)
	2.4V to 2.7V	55 ns		

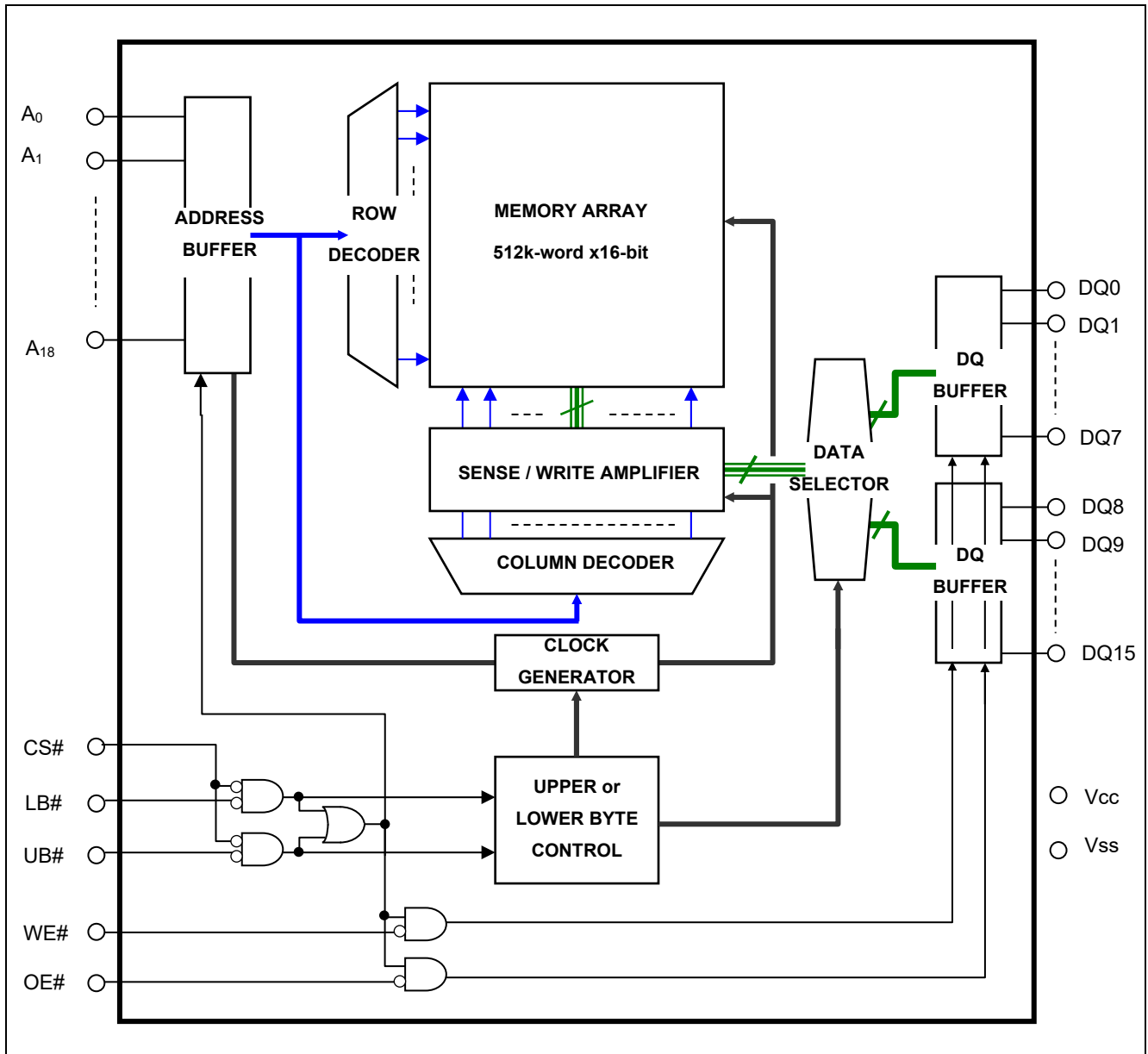
Pin Arrangement



Pin Description

Pin name	Function
V _{cc}	Power supply
V _{ss}	Ground
A0 to A18	Address input
DQ0 to DQ15	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select

Block Diagram



Operation Table

CS#	WE#	OE#	UB#	LB#	DQ0 to DQ7	DQ8 to DQ15	Operation
H	X	X	X	X	High-Z	High-Z	Standby
X	X	X	H	H	High-Z	High-Z	Standby
L	H	L	L	L	Dout	Dout	Read
L	H	L	H	L	Dout	High-Z	Lower byte read
L	H	L	L	H	High-Z	Dout	Upper byte read
L	L	X	L	L	Din	Din	Write
L	L	X	H	L	Din	High-Z	Lower byte write
L	L	X	L	H	High-Z	Din	Upper byte write
L	H	H	X	X	High-Z	High-Z	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V _{SS}	V _{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V _{SS}	V _T	-0.5 ² to V _{CC} +0.3 ³	V
Power dissipation	P _T	0.7	W
Operation temperature	T _{opr}	-40 to +85	°C
Storage temperature range	T _{stg}	-65 to +150	°C
Storage temperature range under bias	T _{bias}	-40 to +85	°C

Note 2. -3.0V for pulse ≤ 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	V _{CC}	2.4	3.0	3.6	V		
	V _{SS}	0	0	0	V		
Input high voltage	V _{IH}	2.0	—	V _{CC} +0.2	V	V _{CC} =2.4V to 2.7V	
		2.2	—	V _{CC} +0.2	V	V _{CC} =2.7V to 3.6V	
Input low voltage	V _{IL}	-0.2	—	0.4	V	V _{CC} =2.4V to 2.7V	4
		-0.2	—	0.6	V	V _{CC} =2.7V to 3.6V	4
Ambient temperature range	T _a	-40	—	+85	°C		

Note 4. -3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	CS# = V _{IH} or OE# = V _{IH} or WE# = V _{IL} or LB# = UB# = V _{IH} , V _{I/O} = V _{SS} to V _{CC}
Average operating current	I _{CC1}	—	20 ^{*5}	25	mA	Cycle = 55ns, duty = 100%, I _{I/O} = 0mA, CS# = V _{IL} , Others = V _{IH} /V _{IL}
		—	25 ^{*5}	30	mA	Cycle = 45ns, duty = 100%, I _{I/O} = 0mA, CS# = V _{IL} , Others = V _{IH} /V _{IL}
	I _{CC2}	—	1.5 ^{*5}	3	mA	Cycle = 1μs, duty = 100%, I _{I/O} = 0mA CS# ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V, V _{IL} ≤ 0.2V
Standby current	I _{SB}	—	—	0.3	mA	CS# = V _{IH} , Others = V _{SS} to V _{CC}
Standby current	I _{SB1}	—	0.45 ^{*5}	2	μA	~+25°C
		—	0.6 ^{*6}	4	μA	~+40°C
		—	—	7	μA	~+70°C
		—	—	10	μA	~+85°C
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1mA V _{CC} ≥ 2.7V
	V _{OH2}	2.0	—	—	V	I _{OH} = -0.1mA
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2mA V _{CC} ≥ 2.7V
	V _{OL2}	—	—	0.4	V	I _{OL} = 0.1mA

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=25°C), and not 100% tested.

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=40°C), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

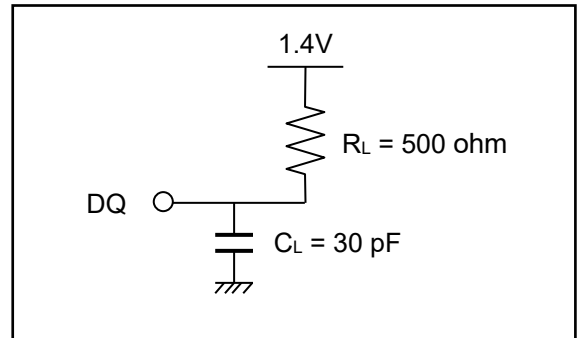
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C _{in}	—	—	8	pF	V _{in} =0V	7
Input / output capacitance	C _{I/O}	—	—	10	pF	V _{I/O} =0V	7

Note 7. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (V_{cc} = 2.4V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels:
 $V_{IL} = 0.4V, V_{IH} = 2.4V$ (V_{cc}=2.7V to 3.6V)
 $V_{IL} = 0.4V, V_{IH} = 2.2V$ (V_{cc}=2.4V to 2.7V)
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	V _{cc} =2.7V to 3.6V		V _{cc} =2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t _{RC}	45	—	55	—	ns	
Address access time	t _{AA}	—	45	—	55	ns	
Chip select access time	t _{ACS}	—	45	—	55	ns	
Output enable to output valid	t _{OE}	—	22	—	30	ns	
Output hold from address change	t _{OH}	10	—	10	—	ns	
LB#, UB# access time	t _{BA}	—	45	—	55	ns	
Chip select to output in low-Z	t _{C LZ}	10	—	10	—	ns	8,9
LB#, UB# enable to low-Z	t _{B LZ}	5	—	5	—	ns	8,9
Output enable to output in low-Z	t _{O LZ}	5	—	5	—	ns	8,9
Chip deselect to output in high-Z	t _{CHZ}	0	18	0	20	ns	8,9,10
LB#, UB# disable to high-Z	t _{BHZ}	0	18	0	20	ns	8,9,10
Output disable to output in high-Z	t _{O HZ}	0	18	0	20	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.

- At any given temperature and voltage condition, t_{CHZ} max is less than t_{C LZ} min, t_{BHZ} max is less than t_{B LZ} min, and t_{O HZ} max is less than t_{O LZ} min, for any device.
- t_{CHZ}, t_{BHZ} and t_{O HZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	V _{CC} =2.7V to 3.6V		V _{CC} =2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t _{WC}	45	—	55	—	ns	
Address valid to write end	t _{AW}	35	—	50	—	ns	
Chip select to write end	t _{CW}	35	—	50	—	ns	
Write pulse width	t _{WP}	35	—	40	—	ns	11
LB#,UB# valid to write end	t _{BW}	35	—	50	—	ns	
Address setup time to write start	t _{AS}	0	—	0	—	ns	
Write recovery time from write end	t _{WR}	0	—	0	—	ns	
Data to write time overlap	t _{DW}	25	—	25	—	ns	
Data hold from write end	t _{DH}	0	—	0	—	ns	
Output enable from write end	t _{OW}	5	—	5	—	ns	12
Output disable to output in high-Z	t _{OHZ}	0	18	0	20	ns	12,13
Write to output in high-Z	t _{WHZ}	0	18	0	20	ns	12,13

Note 11. t_{WP} is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

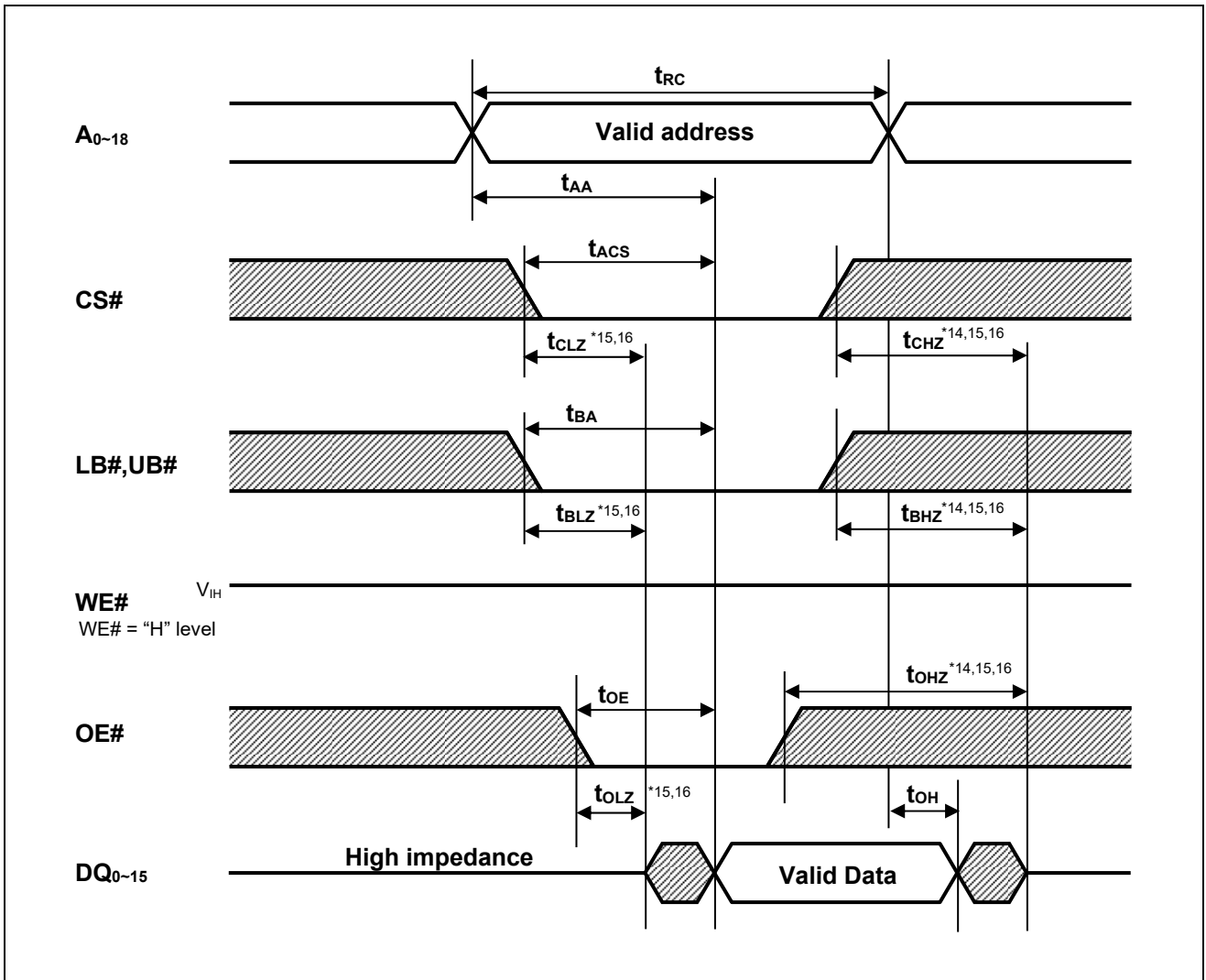
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

12. This parameter is sampled and not 100% tested.

13. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Timing Waveforms

Read Cycle

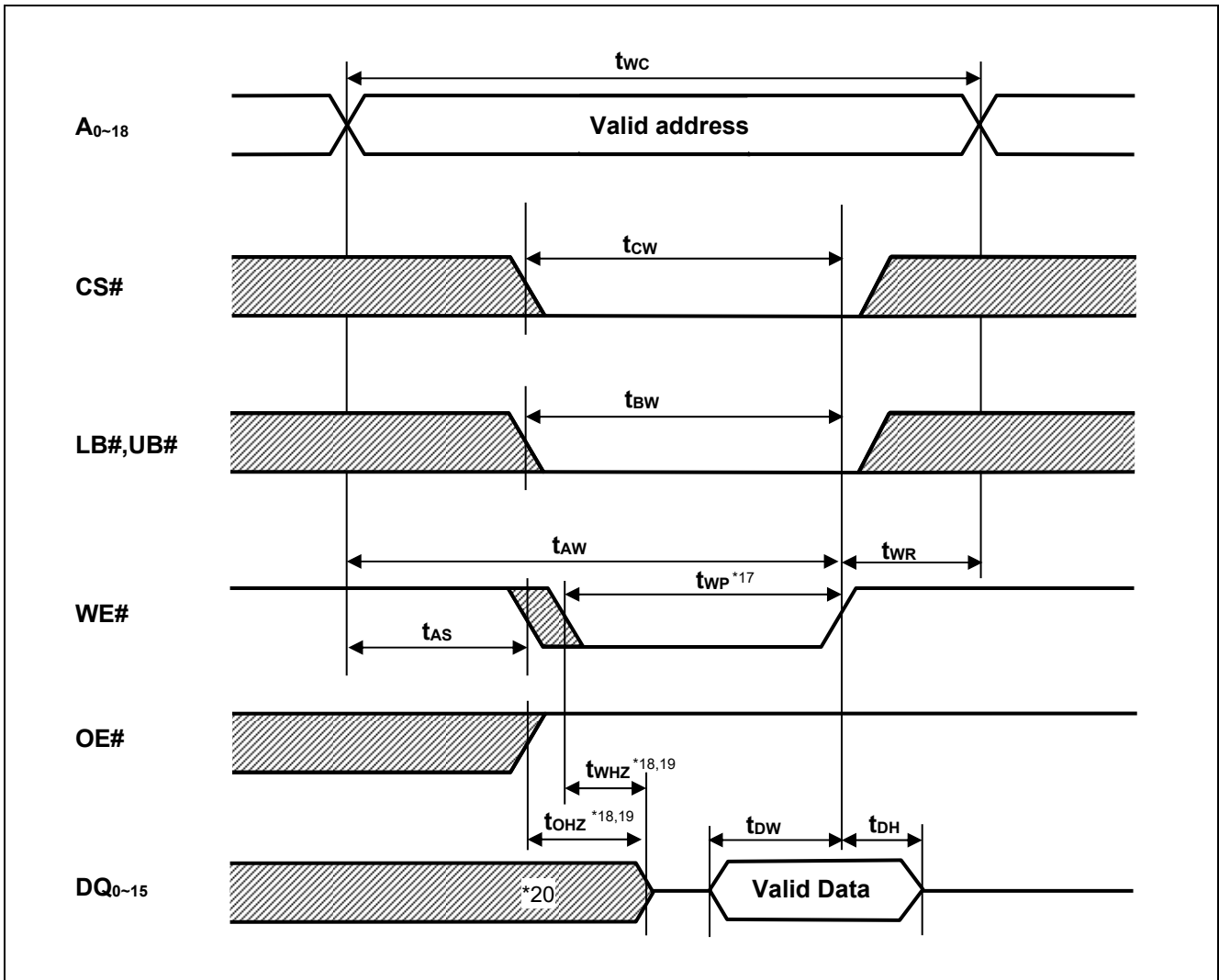


Note 14. t_{CHZ} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

15. This parameter is sampled and not 100% tested

16. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 17. t_{WP} is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

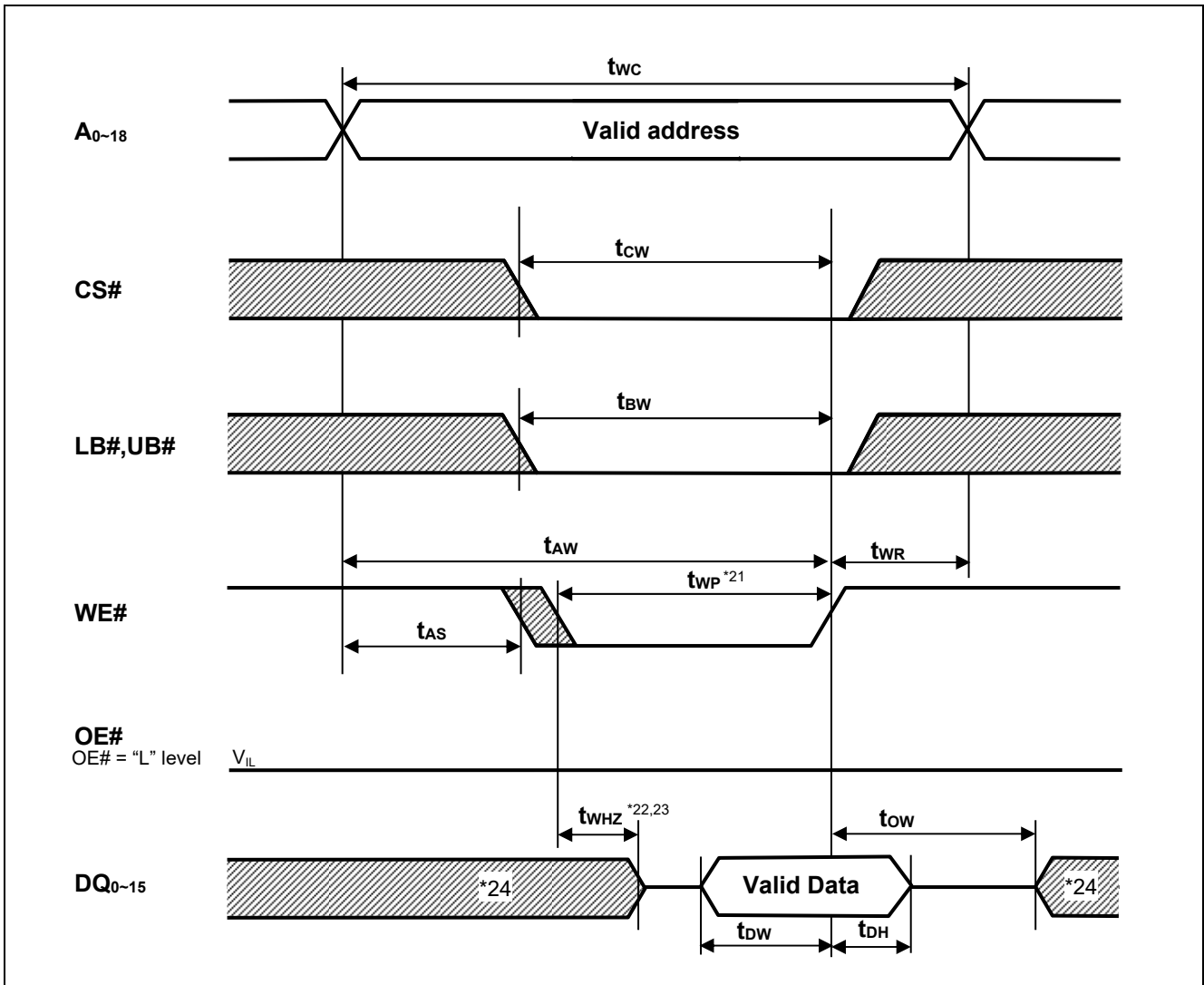
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

18. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

19. This parameter is sampled and not 100% tested

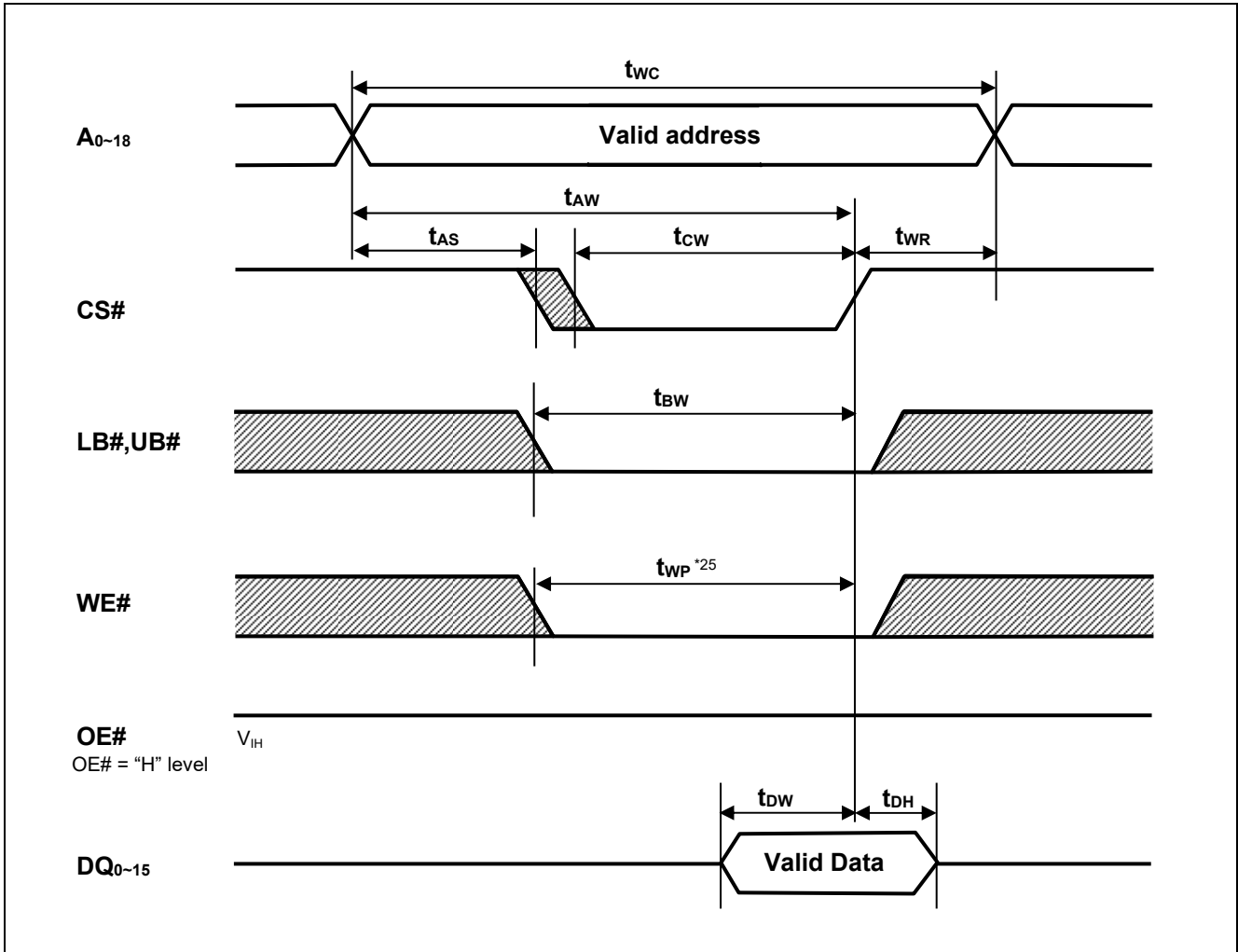
20. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



- Note 21. t_{WP} is the interval between write start and write end.
 A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.
 A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
 A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.
22. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.
23. This parameter is sampled and not 100% tested.
24. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3) (CS# CLOCK)



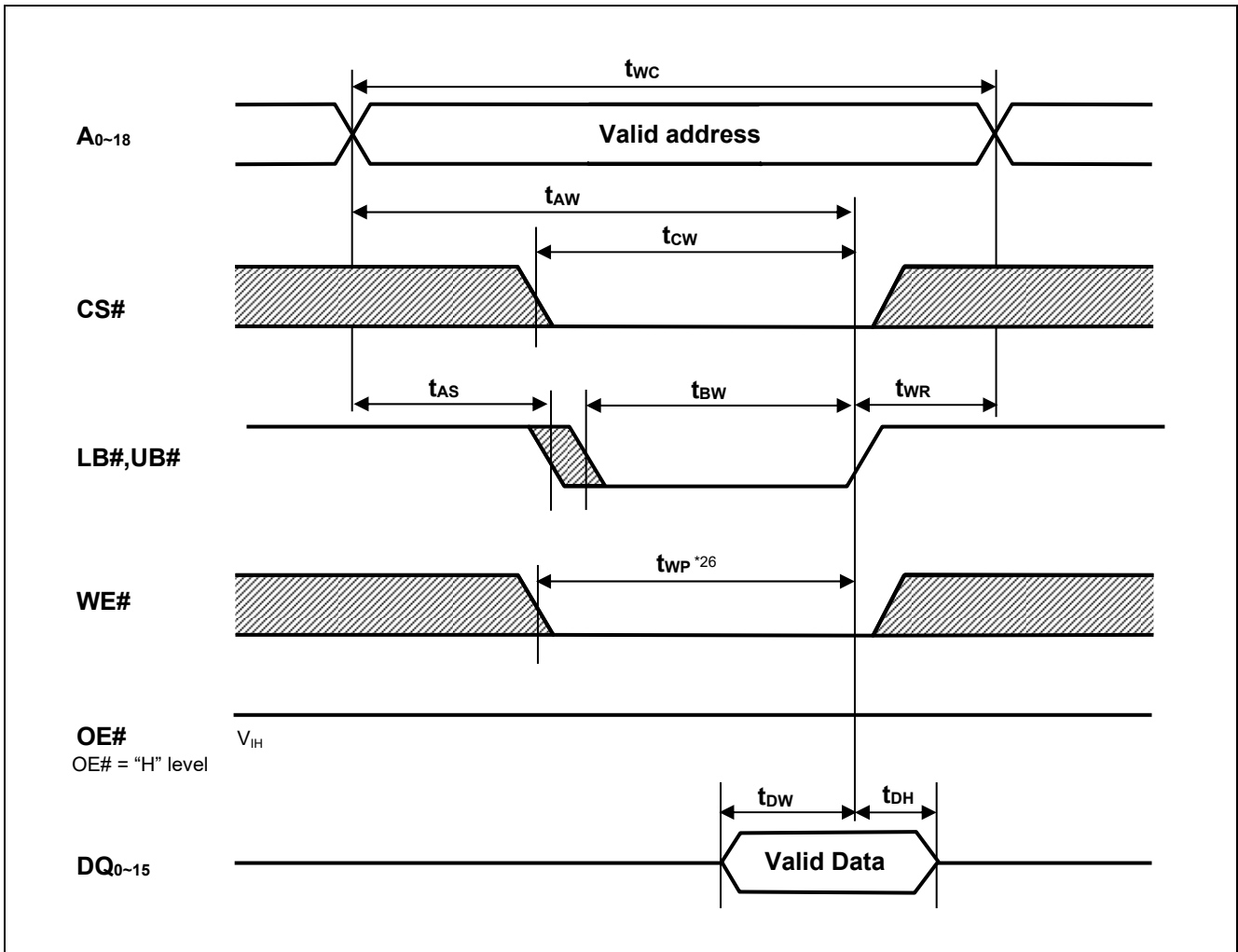
Note 25. t_{WP} is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4) (LB#, UB# CLOCK)



Note 26. t_{WP} is the interval between write start and write end.

A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

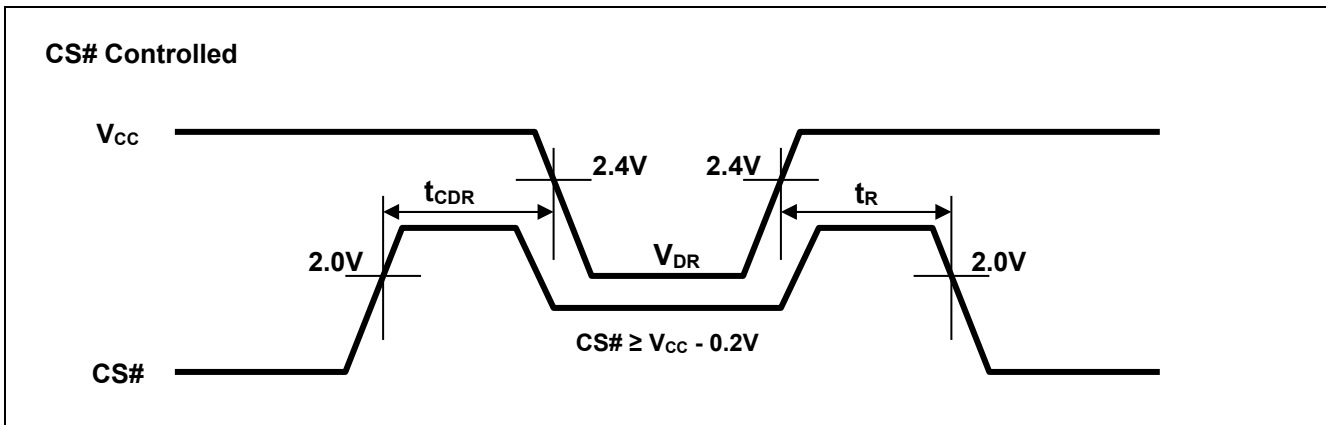
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*29}
V _{CC} for data retention	V _{DR}	1.5	—	3.6	V	V _{in} ≥ 0V, (1) CS# ≥ V _{CC} -0.2V or (2) LB# = UB# ≥ V _{CC} -0.2V, CS# ≤ 0.2V
Data retention current	I _{CCDR}	—	0.45 ^{*27}	2	μA	~+25°C
		—	0.6 ^{*28}	4	μA	~+40°C
		—	—	7	μA	~+70°C
		—	—	10	μA	~+85°C
Chip deselect time to data retention	t _{CDR}	0	—	—	ns	See retention waveform.
Operation recovery time	t _R	5	—	—	ms	

Note 27. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=25°C), and not 100% tested.

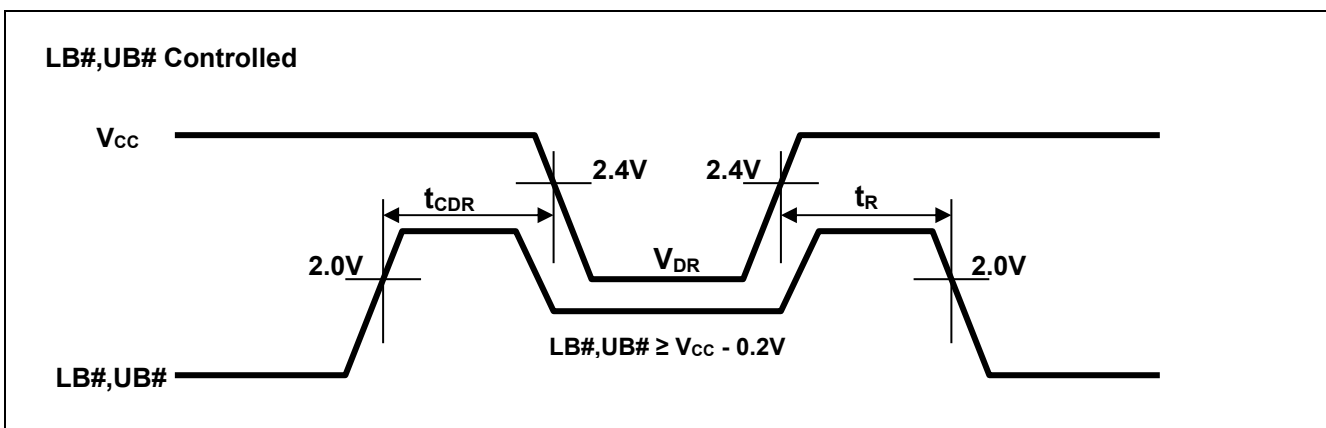
28. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=40°C), and not 100% tested.

29. CS# controls address buffer, WE# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer. If CS# controls data retention mode, V_{in} levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveforms (CS# controlled)



Low V_{CC} Data Retention Timing Waveforms (LB#,UB# controlled)



Revision History	RMLV0816BGSB Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2014.11.28	—	First Edition issued
2.00	2015.06.26	P.1, 4 P.2 P.4 P.12	Standby current I_{SB1} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.) Modify Pin Arrangement : Add 1pin Mark Average operating current I_{CC2} : 25°C 2mA ->1.5mA (typ.) Data retention current I_{CCDR} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.)
2.01	2020.02.20	Last page	Updated the Notice to the latest version

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