

RMWV3216A Series

32Mb Advanced LPSRAM (2M word × 16bit)

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Description

The RMWV3216A Series is a family of 32-Mbit static RAMs organized 2,097,152-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMWV3216A Series has realized higher density, higher performance and low power consumption. The RMWV3216A Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 48-ball fine pitch ball grid array.

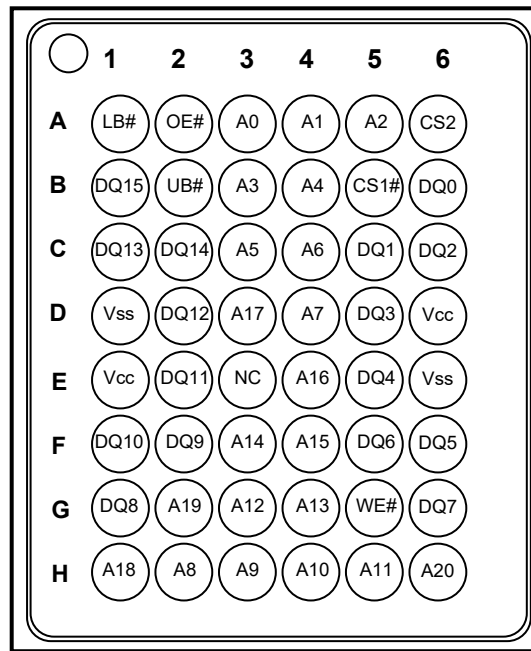
Features

- Single 3V supply: 2.7V to 3.6V
- Access time: 55ns (max.)
- Current consumption:
 - Standby: 1.0μA (typ.)
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation

Part Name Information

| Part Name | Access time | Temperature Range | Package |
|------------------|-------------|-------------------|-------------------------------------|
| RMWV3216AGBG-5S2 | 55 ns | -40 ~ +85°C | 48-ball FBGA with 0.75mm ball pitch |

Pin Arrangement

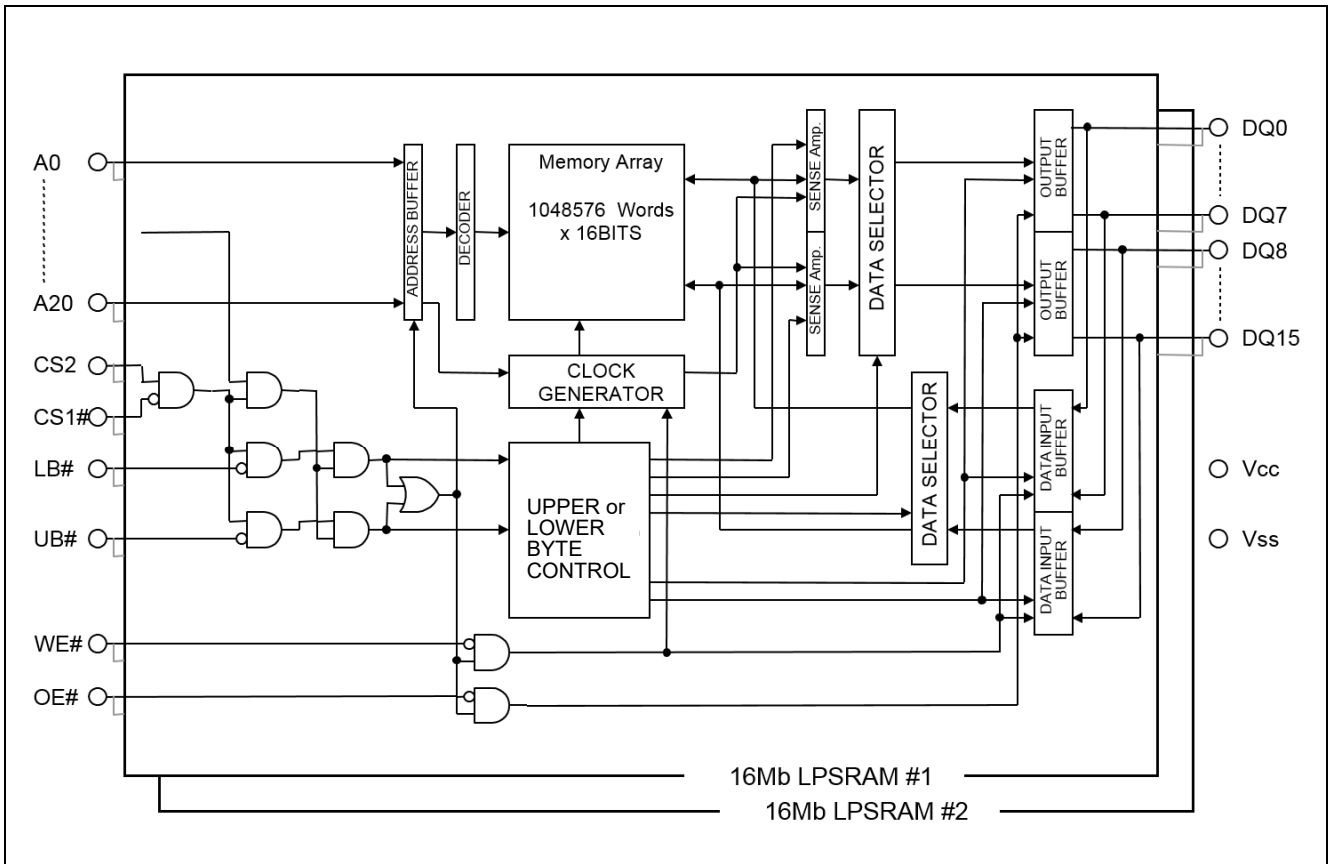


48-ball FBGA (TOP VIEW)

Pin Description

| Pin name | Function |
|-----------------|-------------------|
| V _{cc} | Power supply |
| V _{ss} | Ground |
| A0 to A20 | Address input |
| DQ0 to DQ15 | Data input/output |
| CS1# | Chip select 1 |
| CS2 | Chip select 2 |
| OE# | Output enable |
| WE# | Write enable |
| LB# | Lower byte select |
| UB# | Upper byte select |
| NC | No connection |

Block Diagram



Operation Table

| CS1# | CS2 | WE# | OE# | UB# | LB# | DQ0~7 | DQ8~15 | Operation |
|------|-----|-----|-----|-----|-----|--------|--------|---------------------|
| H | X | X | X | X | X | High-Z | High-Z | Stand-by |
| X | L | X | X | X | X | High-Z | High-Z | Stand-by |
| X | X | X | X | H | H | High-Z | High-Z | Stand-by |
| L | H | H | L | L | L | Dout | Dout | Read read |
| L | H | H | L | H | L | Dout | High-Z | Read in lower byte |
| L | H | H | L | L | H | High-Z | Dout | Read in upper byte |
| L | H | L | X | L | L | Din | Din | Write |
| L | H | L | X | H | L | Din | High-Z | Write in lower byte |
| L | H | L | X | L | H | High-Z | Din | Write in upper byte |
| L | H | H | H | X | X | High-Z | High-Z | Output disable |

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

| Parameter | Symbol | Value | unit |
|---|-------------------|--|------|
| Power supply voltage relative to V _{SS} | V _{CC} | -0.5 to +4.6 | V |
| Terminal voltage on any pin relative to V _{SS} | V _T | -0.5 ² to V _{CC} +0.3 ³ | V |
| Power dissipation | P _T | 0.7 | W |
| Operation temperature | T _{opr} | -40 to +85 | °C |
| Storage temperature range | T _{stg} | -65 to +150 | °C |
| Storage temperature range under bias | T _{bias} | -40 to +85 | °C |

Note 2. -2.0V for pulse ≤ 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.

DC Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---------------------------|-----------------|------|------|----------------------|------|------|
| Supply voltage | V _{CC} | 2.7 | 3.0 | 3.6 | V | |
| | V _{SS} | 0 | 0 | 0 | V | |
| Input high voltage | V _{IH} | 2.2 | — | V _{CC} +0.3 | V | |
| Input low voltage | V _{IL} | -0.3 | — | 0.6 | V | 4 |
| Ambient temperature range | T _a | -40 | — | +85 | °C | |

Note 4. -2.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions | |
|---------------------------|------------------|------|------------------|------|------|--|--|
| Input leakage current | I _{LI} | — | — | 1 | μA | V _{in} = V _{SS} to V _{CC} | |
| Output leakage current | I _{LO} | — | — | 1 | μA | CS1# = V _{IH} or CS2 = V _{IL} or OE# = V _{IH} or WE# = V _{IL} or LB# = UB# = V _{IH} , V _{I/O} = V _{SS} to V _{CC} | |
| Average operating current | I _{CC1} | — | 25 ⁵ | 30 | mA | Cycle = 55ns, duty = 100%, I _{I/O} = 0mA, CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL} | |
| | I _{CC2} | — | 2 ⁵ | 4 | mA | Cycle = 1μs, duty = 100%, I _{I/O} = 0mA, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V, V _{IH} ≥ V _{CC} -0.2V, V _{IL} ≤ 0.2V | |
| Standby current | I _{SB} | — | — | 0.3 | mA | CS2 = V _{IL} , Others = V _{SS} to V _{CC} | |
| Standby current | I _{SB1} | — | 1.0 ⁵ | 6 | μA | ~+25°C | V _{in} = V _{SS} to V _{CC} , (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V |
| | | — | 1.6 ⁶ | 12 | μA | ~+40°C | |
| | | — | 5 ⁷ | 24 | μA | ~+70°C | |
| | | — | 10 ⁸ | 32 | μA | ~+85°C | |
| Output high voltage | V _{OH} | 2.4 | — | — | V | I _{OH} = -1mA | |
| Output low voltage | V _{OL} | — | — | 0.4 | V | I _{OL} = 2mA | |

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=25°C), and not 100% tested.

6. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=40°C), and not 100% tested.

7. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=70°C), and not 100% tested.

8. Typical parameter indicates the value for the center of distribution at 3.0V (T_a=85°C), and not 100% tested.

Capacitance

(T_a =25°C, f =1MHz)

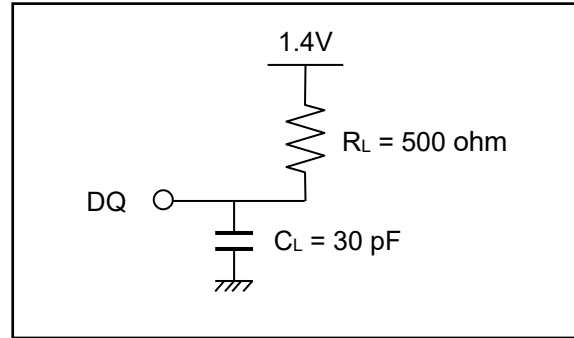
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions | Note |
|----------------------------|------------------|------|------|------|------|----------------------|------|
| Input capacitance | C _{in} | — | — | 10 | pF | V _{in} =0V | 9 |
| Input / output capacitance | C _{I/O} | — | — | 10 | pF | V _{I/O} =0V | 9 |

Note 9. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.7V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels:
 $V_{IL} = 0.4V$, $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

| Parameter | Symbol | Min. | Max. | Unit | Note |
|------------------------------------|------------|------|------|------|----------|
| Read cycle time | t_{RC} | 55 | | ns | |
| Address access time | t_{AA} | — | 55 | ns | |
| Chip select access time | t_{ACS1} | — | 45 | ns | |
| | t_{ACS2} | — | 45 | ns | |
| Output enable to output valid | t_{OE} | — | 22 | ns | |
| Output hold from address change | t_{OH} | 10 | — | ns | |
| LB#, UB# access time | t_{BA} | — | 45 | ns | |
| Chip select to output in low-Z | t_{CLZ1} | 10 | — | ns | 10,11 |
| | t_{CLZ2} | 10 | — | ns | 10,11 |
| LB#, UB# enable to low-Z | t_{BLZ} | 5 | — | ns | 10,11 |
| Output enable to output in low-Z | t_{OLZ} | 5 | — | ns | 10,11 |
| Chip deselect to output in high-Z | t_{CHZ1} | 0 | 18 | ns | 10,11,12 |
| | t_{CHZ2} | 0 | 18 | ns | 10,11,12 |
| LB#, UB# disable to high-Z | t_{BHZ} | 0 | 18 | ns | 10,11,12 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 18 | ns | 10,11,12 |

Note 10. This parameter is sampled and not 100% tested.

- At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.
- t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

| Parameter | Symbol | Min. | Max. | Unit | Note |
|------------------------------------|-----------|------|------|------|-------|
| Write cycle time | t_{WC} | 55 | — | ns | |
| Address valid to write end | t_{AW} | 35 | — | ns | |
| Chip select to write end | t_{CW} | 35 | — | ns | |
| Write pulse width | t_{WP} | 35 | — | ns | 13 |
| LB#,UB# valid to write end | t_{BW} | 35 | — | ns | |
| Address setup time to write start | t_{AS} | 0 | — | ns | |
| Write recovery time from write end | t_{WR} | 0 | — | ns | |
| Data to write time overlap | t_{DW} | 25 | — | ns | |
| Data hold from write end | t_{DH} | 0 | — | ns | |
| Output enable from write end | t_{OW} | 5 | — | ns | 13 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 18 | ns | 14,15 |
| Write to output in high-Z | t_{WHZ} | 0 | 18 | ns | 14,15 |

Note 13. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

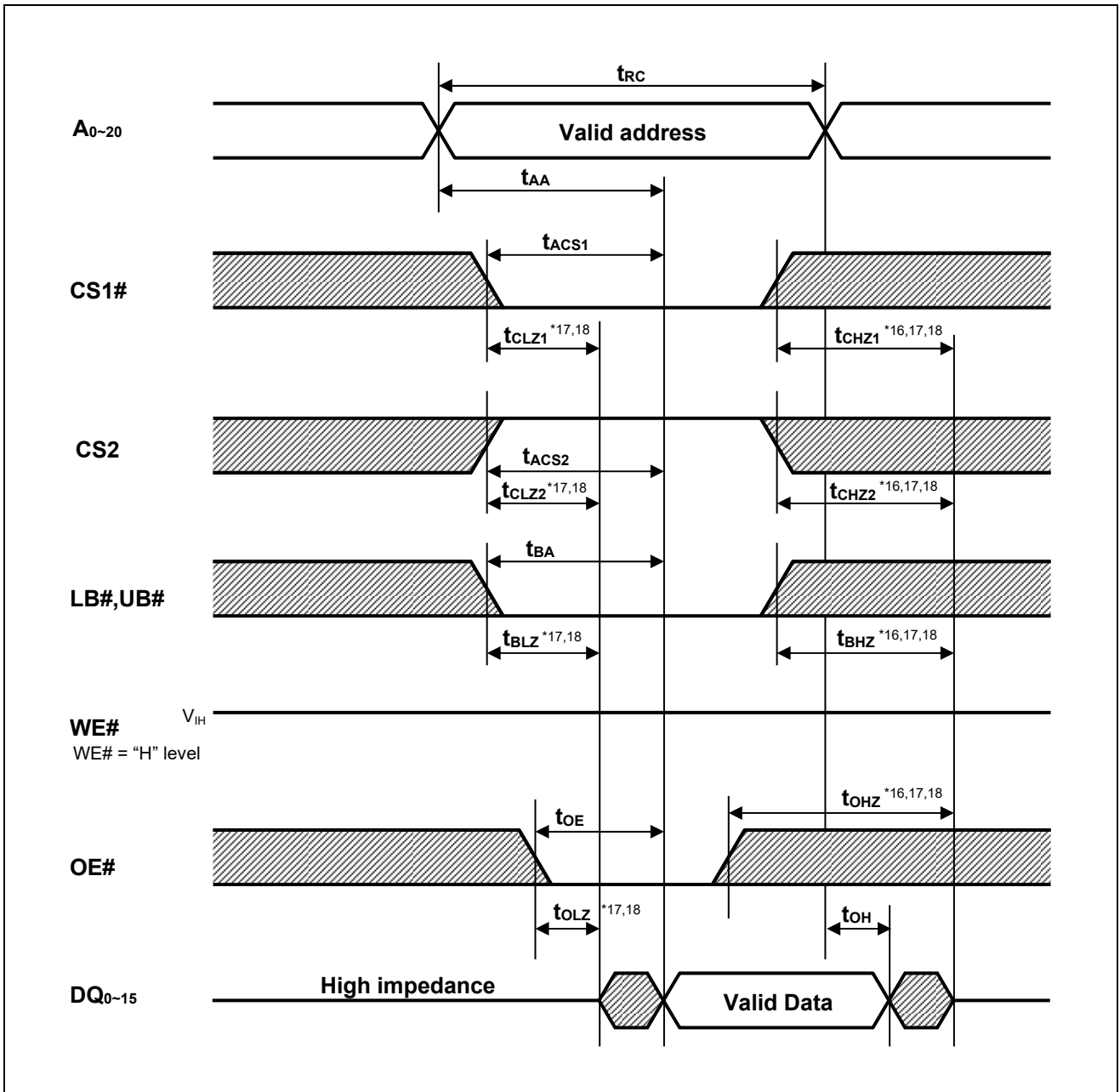
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

14. This parameter is sampled and not 100% tested.

15. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Timing Waveforms

Read Cycle

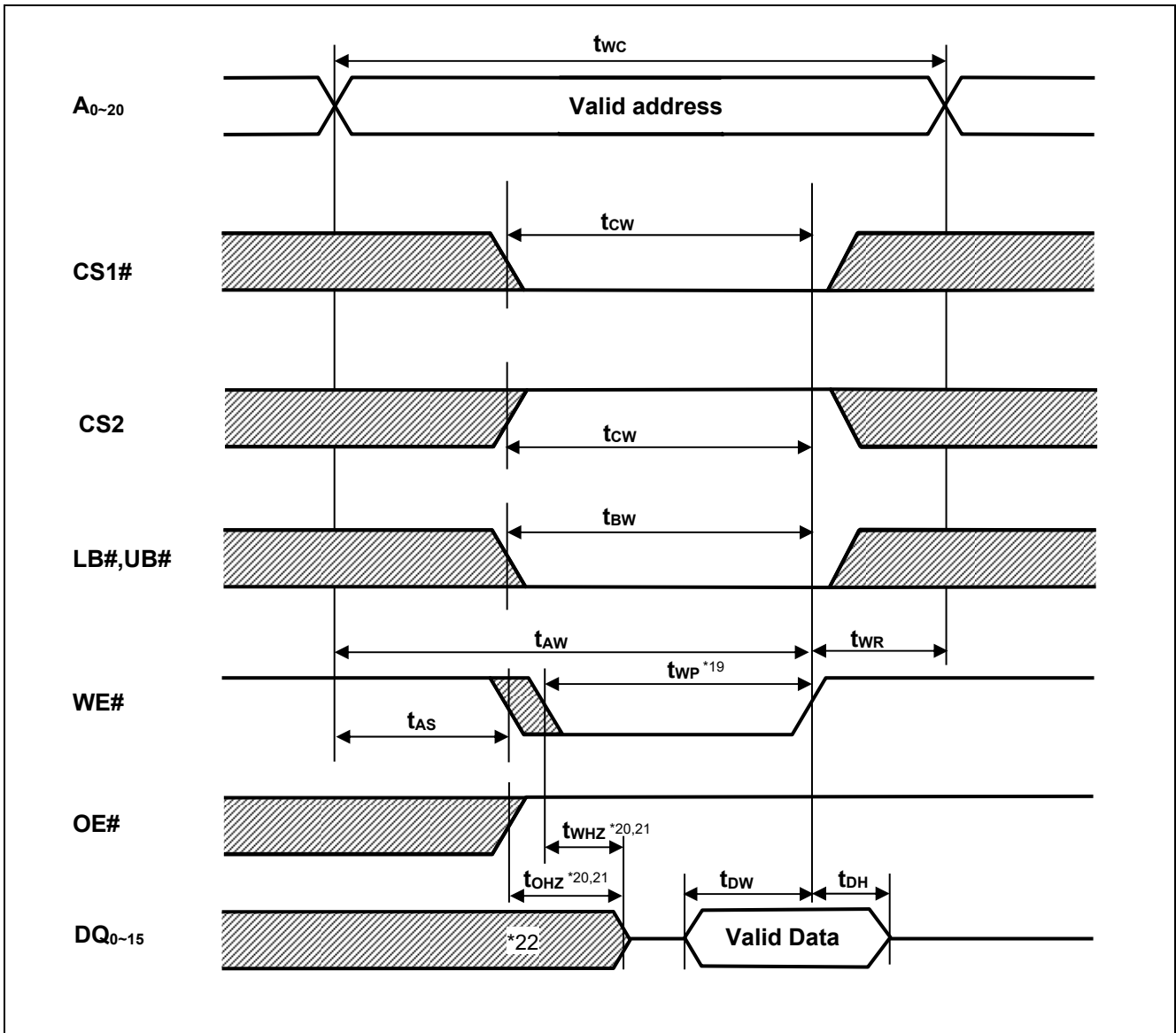


Note 16. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

17. This parameter is sampled and not 100% tested.

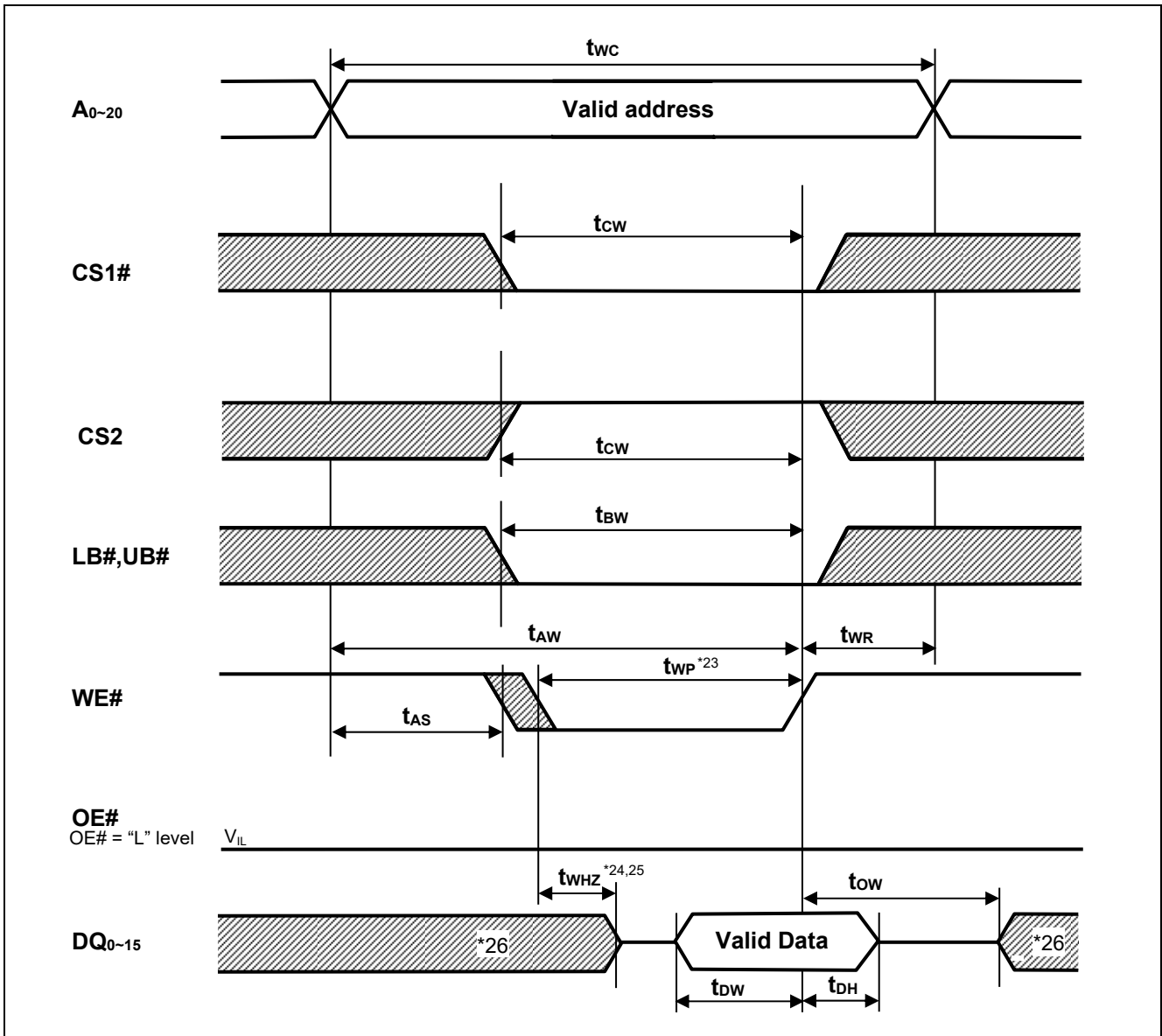
18. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



- Note 19. t_{wp} is the interval between write start and write end.
 A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
 A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
 A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.
20. t_{ohz} and t_{whz} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.
21. This parameter is sampled and not 100% tested.
22. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 23. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

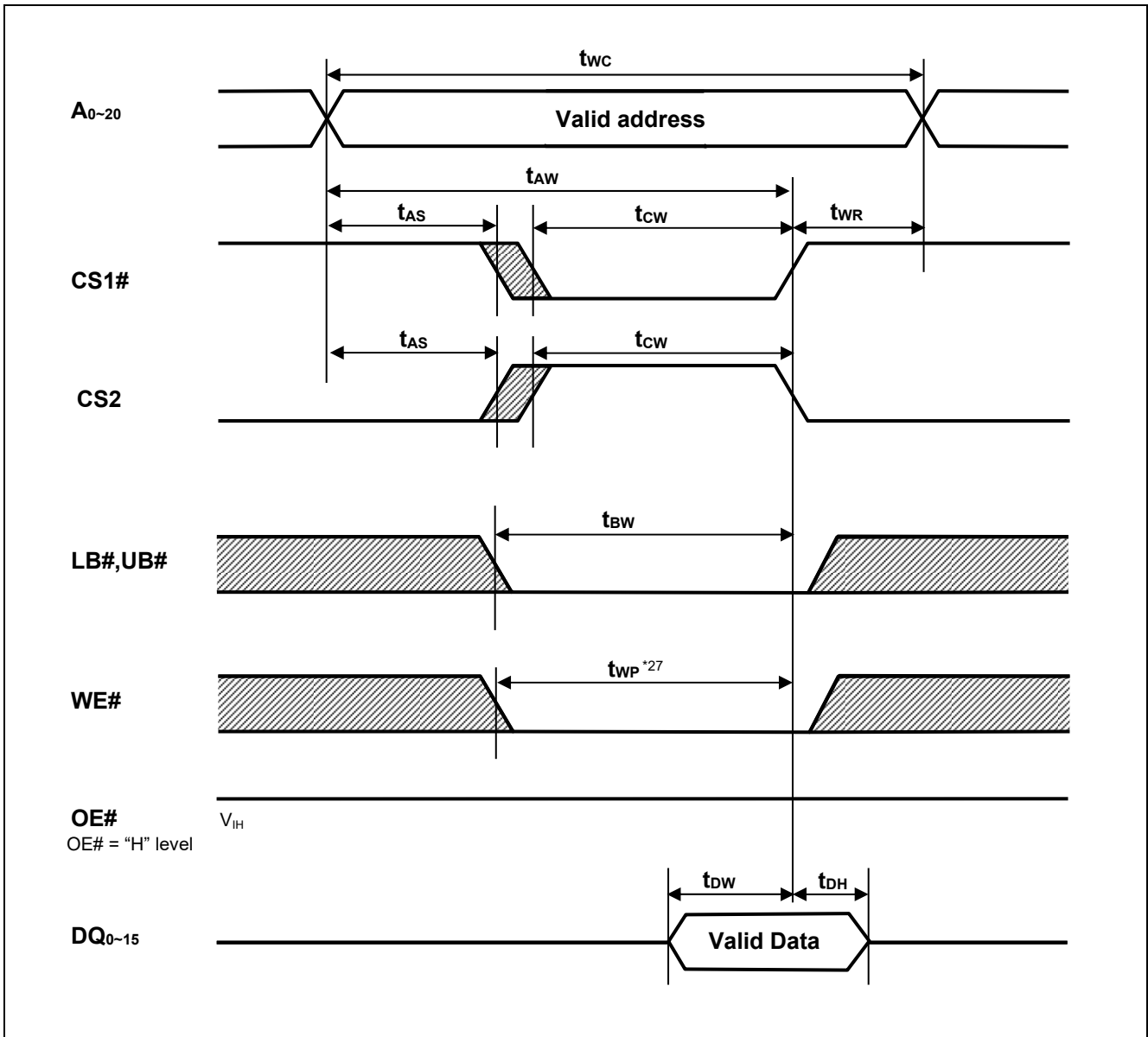
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

24. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

25. This parameter is sampled and not 100% tested.

26. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3) (CS1#, CS2 CLOCK)



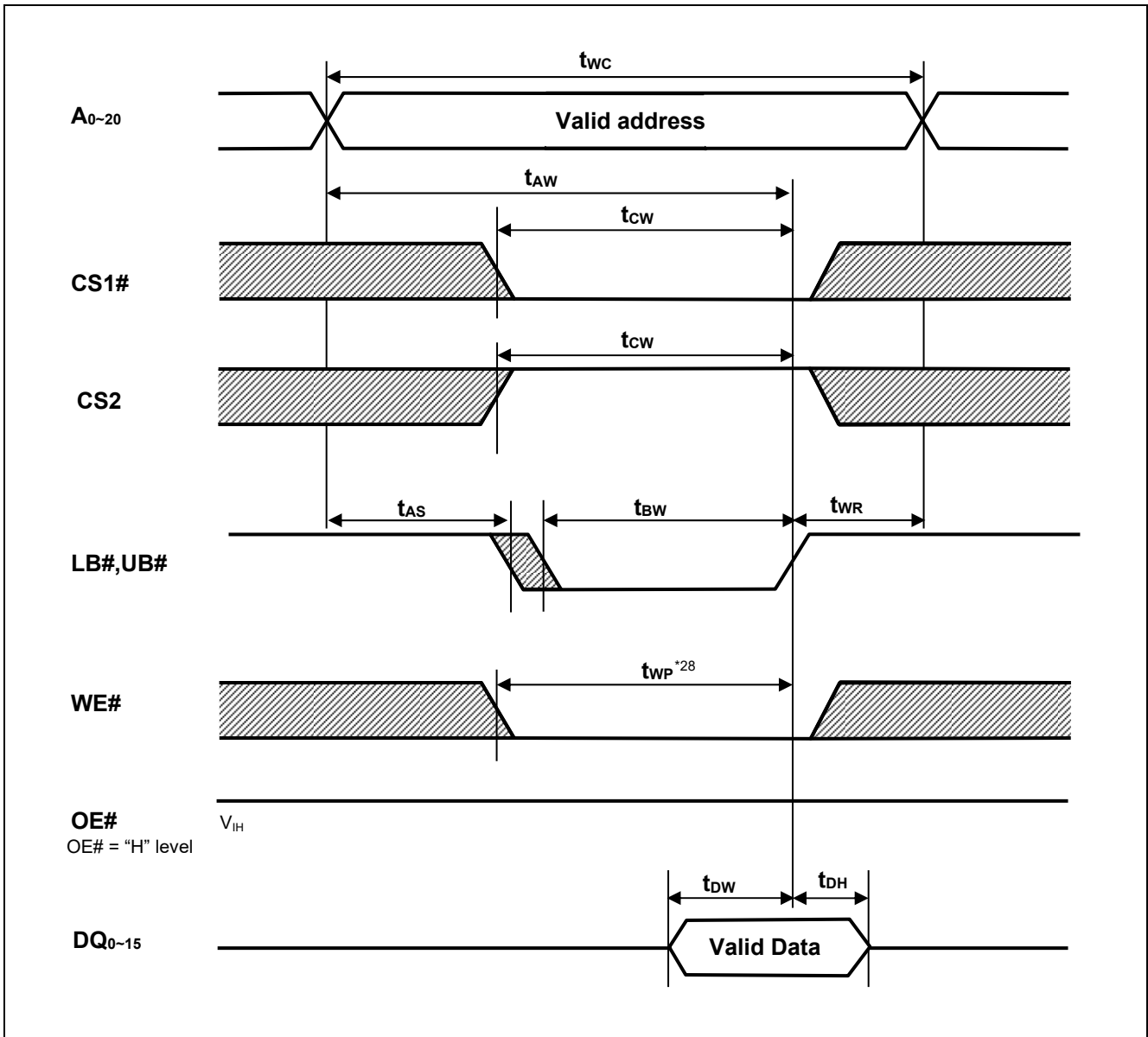
Note 27. **t_{WP}** is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4) (LB#, UB# CLOCK)



Note 28. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

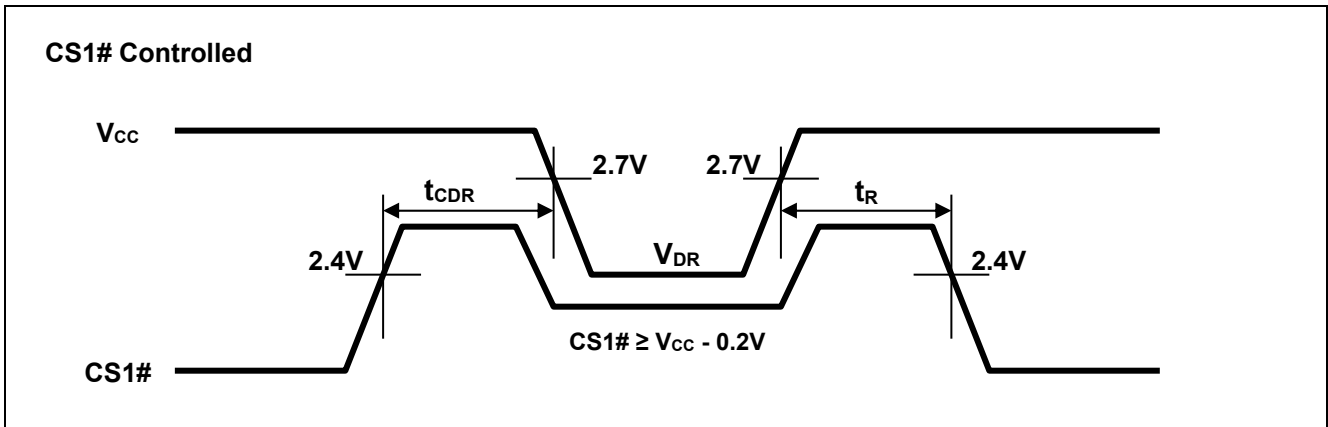
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

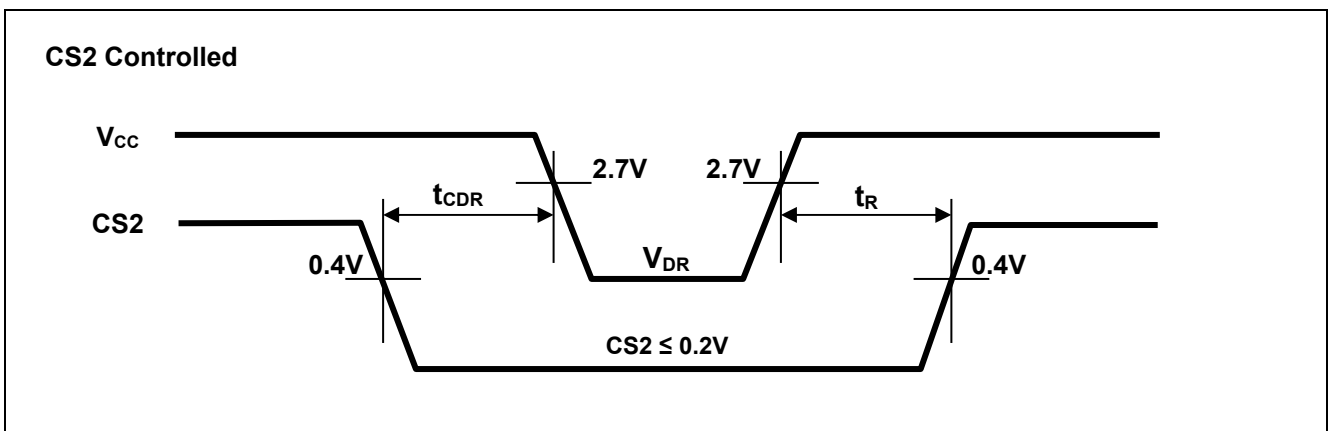
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions ^{*29} | |
|--------------------------------------|-------------------|------|--------------------|------|------|--|---|
| V _{CC} for data retention | V _{DR} | 1.5 | — | 3.6 | V | Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V | |
| Data retention current | I _{CCDR} | — | 1.0 ^{*30} | 6 | μA | ~+25°C | V _{CC} = 3.0V, Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V |
| | | — | 1.6 ^{*31} | 12 | μA | ~+40°C | |
| | | — | 5 ^{*32} | 24 | μA | ~+70°C | |
| | | — | 10 ^{*33} | 32 | μA | ~+85°C | |
| Chip deselect time to data retention | t _{CDR} | 0 | — | — | ns | See retention waveform. | |
| Operation recovery time | t _R | 5 | — | — | ms | | |

- Note 29. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer.
 If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V.
 The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.
30. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.
31. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40°C), and not 100% tested.
32. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=70°C), and not 100% tested.
33. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=85°C), and not 100% tested.

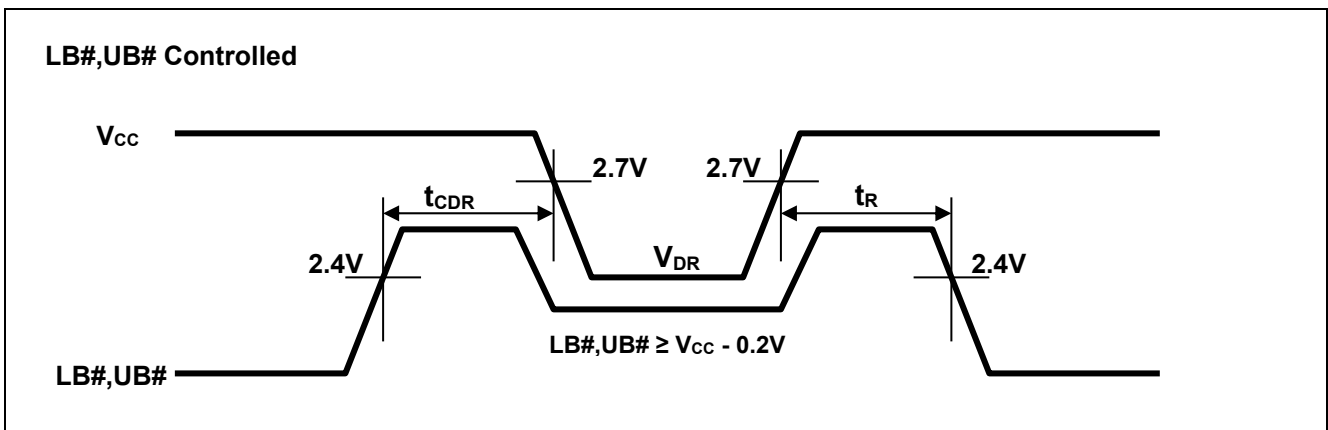
Low Vcc Data Retention Timing Waveforms (CS1# controlled)



Low Vcc Data Retention Timing Waveforms (CS2 controlled)



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled)



| | |
|------------------|-----------------------------|
| Revision History | RMWV3216A Series Data Sheet |
|------------------|-----------------------------|

| Rev. | Date | Description | |
|------|------------|-------------|--|
| | | Page | Summary |
| 1.00 | 2016.01.06 | — | First Edition issued |
| 1.01 | 2020.02.20 | Last page | Updated the Notice to the latest version |
| | | | |

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