RRP51035

Ultra-Low Dropout, Low VIN, Ultra-Low Noise, High PSRR, 3A LDO

The RRP51035 is an ultra-low noise, high PSRR, low dropout regulator capable of sourcing up to 3A of load current with only 180mV dropout voltage. It operates from an input voltage of 1.1V for extremely low voltage applications to 6.5V.

The LDO output voltage can be programmed from 0.5V to 2.075V using voltage setting pins on the IC in 25mV steps, eliminating the need for traditional external feedback resistors and saving PCB space. External feedback resistors can still be used for higher output voltage applications, allowing the output voltage to be programmed anywhere from 0.5V to 5.1V.

The RRP51035 has an ultra-low output noise and high PSRR without a feed-forward capacitor. It only requires a single 1µF noise-reduction capacitor to achieve 7µVRMS output noise, making it great for noise-sensitive and space-constrained applications.

The LDO features a ±1% output voltage accuracy, input voltage, and BIAS voltage UVLO with hysteresis, enable control, internal current limit, over-temperature shutdown protection with hysteresis, power-good indication, voltage BIAS pin, and fast-start up.

The RRP51035 is stable with a minimum 22µF ceramic output capacitor and is available in a 20-Ld 3.5mm×3.5mm QFN package.

Features

- Maximum dropout: 180mV at 3A with BIAS
- Output voltage accuracy: ±1%
- Ultra-low output noise: 7µVRMS
- Input voltage range:
    - Without BIAS: 1.4V to 6.5V
    - With BIAS: 1.1V to 6.5V
- Output voltage range:
    - Using PCB layout and voltage set pins: 0.5V to 2.075V
    - External FB resistors: 0.5V to 5.1V
- BIAS voltage range: 3V to 6.5V
- Max operating load current: 3A
- High PSRR at $V_{HEADROOM}$ = 0.5V
    - 100kHZ: 35dB at 3A
- Enable control and power-good indication
- Overcurrent, short-circuit, and over-temperature fault protection
- Excellent load transient response

Applications

- Sensor, imaging, and radar
- Test and measurement
- Instrumentation, medical, and audio
- RF power supplies

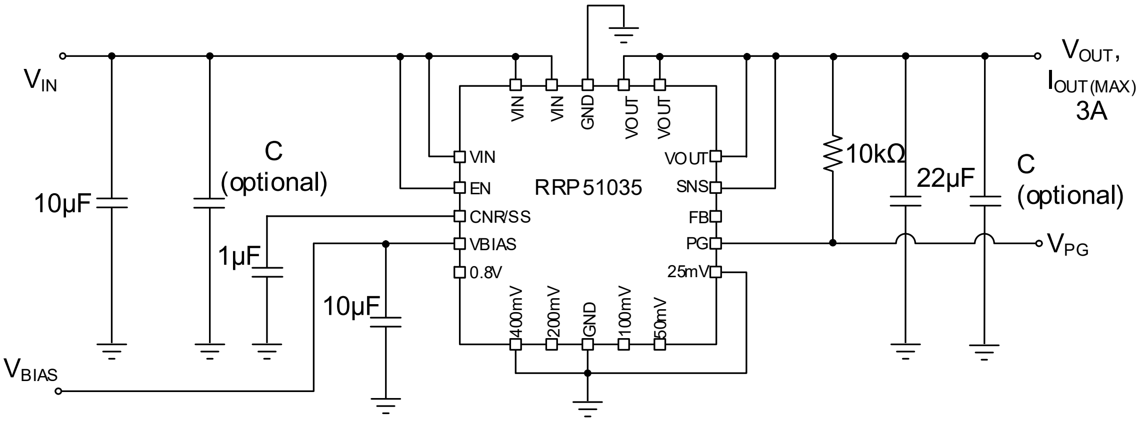


Figure 1. Typical Application Schematic

Contents

1. Overview

1.1 Block Diagram

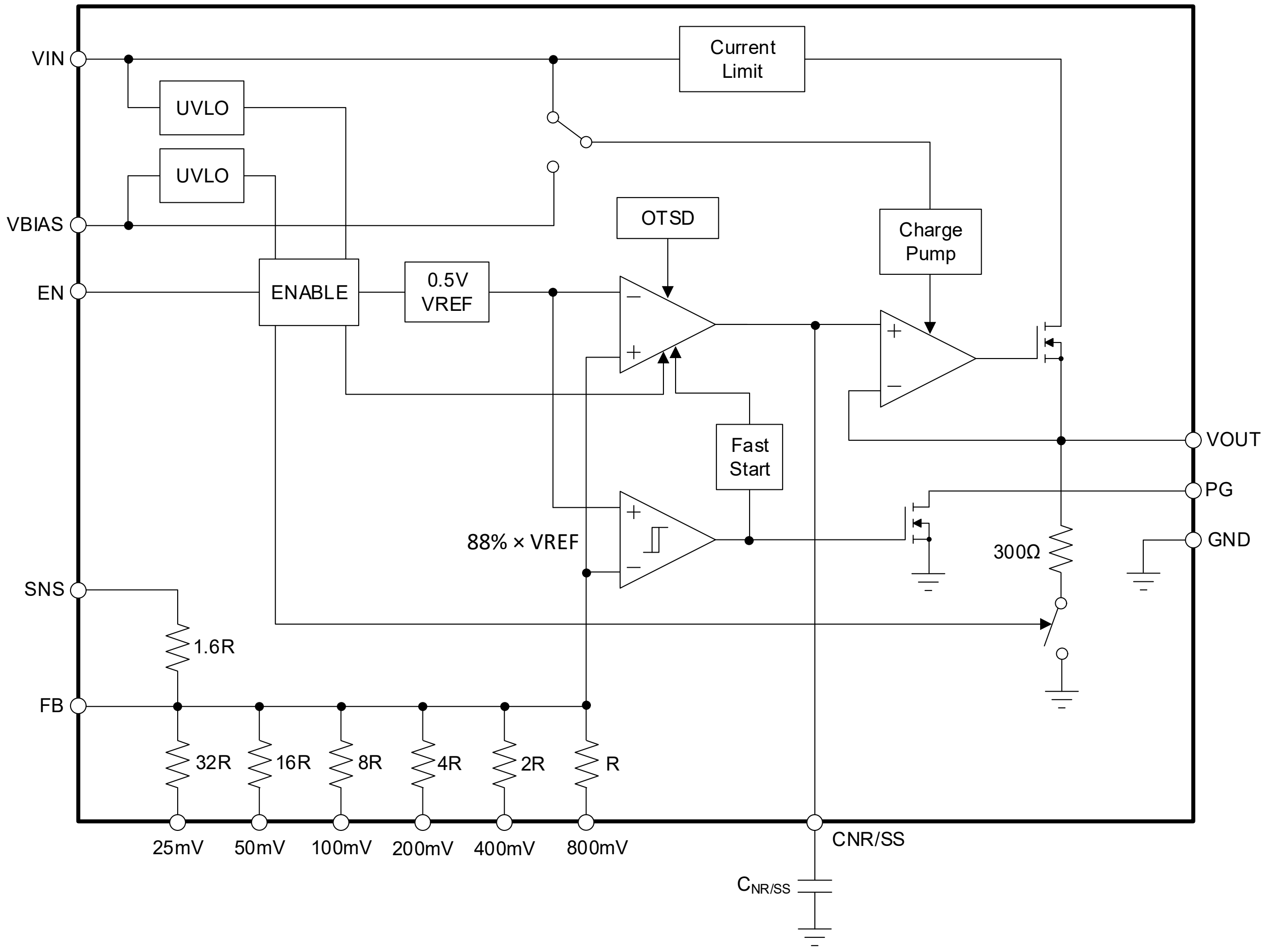


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

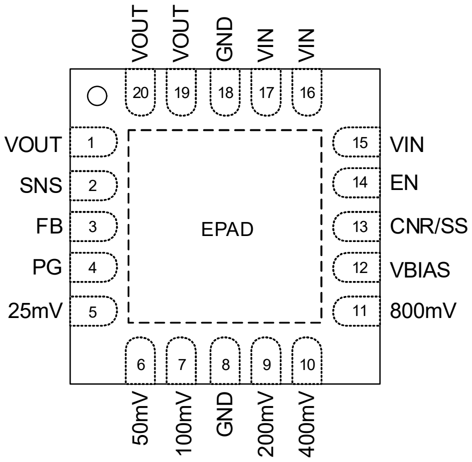


Figure 3. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 19, 20	VOUT	VOUT are the output pins that supply power to the load. The recommended operating output voltage for these pins is 0.5V to 5.1V. The maximum current that these pins can source is 3A. Renesas recommends tying all three pins to the same output PCB plane. A minimum 22µF ceramic capacitor is required from these pins to GND for stable operation. Place the output capacitor as close as possible to the OUT pins. Add an optional 100nF bypass capacitor parallel with the 22µF to reduce higher-frequency noise and supply higher-frequency load currents if required. See Programming the Output Voltage for programming the output voltage and Output Capacitor (C_{OUT}) for selecting COUT.
2	SNS	SNS is the output voltage sense pin. Connect this pin to the OUT pins (1, 19, 20) if the output voltage set IC pins (25mV, 50mV, 100mV, 200mV, 400mV, and 800mV pins) are used to program the output voltage. If external feedback resistors are used to program the output voltage, leave this pin floating.
3	FB	FB is the output voltage feedback pin. This pin is internally connected to the error amplifier and is compared with 0.5V of the voltage reference circuitry. The voltage divider formed around this pin with either the internal or external feedback resistors programs the LDO output voltage. See Internal Feedback Resistors and Output Voltage Set Pins for using the internal FB resistors and External Feedback Resistors for using the external FB resistors to program the output voltage.
4	PG	PG is the power good pin. This pin monitors the output voltage and signals other circuit ICs in a system connected to this pin when the output voltage is at or near its programmed value. When the output voltage exceeds -12% of its programmed value, this pin pulls LOW, indicating a fault. When the output voltage is within -12% of its programmed value, the pin is open-circuit (high Z) without a pull-up resistor. Therefore, to ensure a proper logic HIGH to devices connected to this pin, Renesas recommends tying a 10kΩ (minimal) pull-up resistor. If this pin is not being used, it can be left floating.

Pin Number	Pin Name	Description
5	25mV	These are the output voltage set pins. These pins can either be grounded or left floating. Connecting any pin to ground increases the output voltage by the value of the pin name. With all the pins left floating, the output voltage equals V_{REF}, which is 0.5V. With all the pins grounded, the output voltage is 2.075V. See Internal Feedback Resistors and Output Voltage Set Pins for more detail on how to use these pins to program the output voltage.
6	50mV	
7	100mV	
9	200mV	
10	400mV	
11	800mV	
8, 18	GND	GND is the ground pin. Tie this pin to the PCB ground plane and the EPAD.
12	VBIAS	VBIAS is the BIAS pin. This pin enables low-input voltage (V_{IN} < 1.4V) to reduce power dissipation for low-voltage applications. It also improves DC and AC performance for $V_{IN} \leq 1.4V$. A minimum 1µF capacitor must be connected between this pin and GND. Place this capacitor as close as possible to the BIAS pin. If not using this pin, it can be left floating or tied to GND without impacting performance.
13	CNR/SS	CNR/SS is the noise-reduction and soft-start pin. A 100nF capacitor is required between this pin and GND for LDO stability and to help reduce low-to-mid frequency noise and increase low-to-mid frequency PSRR. For optimal noise/PSRR performance, Renesas recommends using a 1µF capacitor on this pin. Using a larger capacitor can increase the soft-start time to reduce in-rush current. See Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$) for more details on selecting $C_{NR/SS}$.
14	EN	EN is the enable pin. This pin can enable or disable the LDO. If the voltage on this pin is LOW, the LDO is disabled and shuts down. When the voltage is HIGH, the LDO is enabled. ***Important***: This pin must not be left floating. Instead, tie it to the VIN pins for automatic enabling. See Enable Control for more details on the EN function.
15, 16, 17	VIN	VIN are the input voltage pins that supply power to the LDO and the LDO load. The recommended operating input voltage for these pins is 1.4V to 6.5V without BIAS and down to 1.1V with BIAS. Renesas recommends tying all three pins to the same input PCB plane. A minimum 10µF ceramic capacitor is required between these pins to GND to minimize the impedance of the input supply. The input capacitor also helps reduce high-frequency input noise. Place this capacitor as close as possible to the VIN pins. Add an optional 100nF bypass capacitor in parallel with the 10µF to reduce higher-frequency input noise and further reduce input supply impedance supply if required. See Input Capacitor (C_{IN}) for more details selecting C_{IN}.
-	EPAD	EPAD is the exposed pad on the bottom of the package. Solder the exposed pad to the PCB ground plane and tie it directly to pins 8 and 18 to ensure the best electrical and thermal performance. See Layout Guidelines for more layout guidelines for this pin.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
VIN, EN, BIAS	-0.3	+7.5	V
VOUT, PG, NR/SS	-0.3	+6.5	V
25mV, 50mV, 100mV, 200mV, 400mV, and 800mV	-0.3	+6.5	V
FB	-0.3	+3.3	V
Maximum Junction Temperature	-40	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. All voltages referenced to GND unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, V_{IN}	1.1	6.5	V
Bias Voltage, V_{BIAS}	3	6.5	V
Enable Voltage, V_{EN}	0	6.5	V
Output Voltage, V_{OUT}	0.5	5.1	V
Output Current, I_{OUT}	0	3	A
Output Capacitor, C_{OUT}	22	-	µF
Input Capacitor, C_{IN}	10	-	µF
Bias Capacitor, C_{BIAS}	1	-	µF
Power-Good Pull-Up Resistance, R_{PG}	10	-	kΩ
Noise Reduction Capacitor, $C_{NR/SS}$	0.1	-	µF
Junction Temperature	-40	+125	°C

1. All voltages referenced to GND unless otherwise specified.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	20-Ld 3.5mm×3.5mm QFN Package	θ_{JA}[1]	Junction to ambient	42	°C/W
		θ_{JC}[2]	Junction to case	4.5	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT}+400mV or 1.4V whichever is greater, V_{BIAS} = OPEN, V_{OUT} = 0.5V, V_{EN} = 5V, I_{OUT} = 0mA, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 100nF. Typical values are at T_A = +25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ.	Max[1]	Unit
Input						
Input Voltage Range	V_{IN}	With V_{BIAS} between 3V and 6.5V	1.1	-	6.5	V
		Without V_{BIAS}	1.4	-	6.5	
Input Voltage UVLO without BIAS	V_{IN_UVLO}	-	-	1.33	1.4	V
Input Voltage UVLO Hysteresis without BIAS	$V_{IN\_UVLO\_HYS}$	-	-	100	-	mV
Input Voltage UVLO with BIAS	$V_{IN\_UVLO(BIAS)}$	V_{IN} Rising, V_{BIAS} = 3V	-	1	1.1	V
Input Voltage UVLO Hysteresis with BIAS	$V_{IN\_UVLO\_HYS(BIAS)}$	V_{BIAS} = 3V	-	33	-	mV
BIAS voltage UVLO	V_{BIAS_UVLO}	-			3.0	V
BIAS voltage UVLO Hysteresis	$V_{BIAS\_UVLO\_HYS}$	-	-	100	-	mV
V_{IN} Quiescent Current	$I_{Q(VIN)}$	I_{OUT} = 0A, V_{IN} = 1.4V, V_{OUT} = 0.5V, PG is floating	-	0.9	-	mA
V_{BIAS} Quiescent Current	$I_{Q(VBIAS)}$	V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V, PG is floating	-	1	-	mA
Shutdown Current	I_{SHTD}	V_{IN} = 6.5V, V_{EN} = 0V, C_{IN} = 100nF	-	9	25	µA
Output						
Output Voltage Range	V_{OUT}	-	0.5	-	5.1	V
Output Current	I_{OUT}	-	0	-	3	A
FB Voltage	V_{FB}	For configuration using external resistor divider	-	0.5	-	V
Output Voltage Accuracy	-	V_{OUT} = 0.5V, I_{OUT} = 10mA	-1.25	-	1.25	%
		V_{OUT} = 0.8V to 2.075V, I_{OUT} = 10mA	-1	-	1	
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 1.4V to 6.5V, I_{OUT} = 5mA	-	0.1	-	mV/V
		V_{IN} = 1.1V to 4V, I_{OUT} = 5mA, V_{BIAS} = 5V	-	0.1	-	
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 1.4V, V_{OUT} = 0.5V, I_{OUT} = 1mA to 3A	-	1.2	-	mV/A
		V_{IN} = 1.1V, V_{OUT} = 0.5V, I_{OUT} = 1mA to 3A, V_{BIAS} = 5V	-	1.2	-	
Dropout Voltage[2]	V_{DO}	V_{IN} = 1.1V, V_{BIAS} = 5V, V_{FB} forced to 97% of V_{REF},3A I_{OUT}	-	70	180	mV
		V_{IN} = 1.4V, V_{FB} forced to 97% of V_{REF}, 3A I_{OUT}	-	100	200	
		V_{IN} = 5.5V, V_{FB} forced to 97% of V_{REF}, 3A I_{OUT}	-	70	200	

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT}+400mV or 1.4V whichever is greater, V_{BIAS} = OPEN, V_{OUT} = 0.5V, V_{EN} = 5V, I_{OUT} = 0mA, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 100nF. Typical values are at T_A = +25°C, unless otherwise specified. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ.	Max[1]	Unit
Start-Up Time	-	V_{IN} = 5.5V, V_{OUT} = 1.8V, I_{OUT} = 10mA, CNR/SS =1µF	-	-	800	µs
Noise Spectral Density						
Noise with BIAS	$V_{n(BIAS)}$	V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 10Hz	-	800	-	nV/√Hz
		V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 100Hz	-	140	-	
		V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 1kHz	-	40	-	
		V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 10kHz	-	20	-	
Noise without BIAS	V_n	V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 10Hz	-	800	-	nV/√Hz
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 100Hz	-	140	-	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 1kHz	-	40	-	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 10kHz	-	20	-	
Output RMS Noise with BIAS	V_n	V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, BW = 10Hz to 100kHz	-	7	-	µVRMS
Output RMS Noise without BIAS	V_n	V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS = 1µF, C_{OUT} = 47µF || 10µF || 10µF, BW = 10Hz to 100kHz	-	7	-	µVRMS

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT}+400mV or 1.4V whichever is greater, V_{BIAS} = OPEN, V_{OUT} = 0.5V, V_{EN} = 5V, I_{OUT} = 0mA, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 100nF. Typical values are at T_A = +25°C, unless otherwise specified. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ.	Max[1]	Unit
PSRR						
PSRR with BIAS	-	V_{IN} = 1.2V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{IN} = None, COUT = 47µF || 10µF || 10µF, FREQ = 120Hz, V_{RIPPLE} = 150mV_{P-P}	-	85	-	dB
		V_{IN} = 1.2V, V_{BIAS}= 5V, V_{OUT} = 0.5V, I_{OUT}= 3A, CNR/SS = 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 10kHz, V_{RIPPLE} = 150mV_{P-P}	-	50	-	
		V_{IN} = 1.2V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 100kHz, V_{RIPPLE} = 150mV_{P-P}	-	35	-	
		V_{IN} = 1.2V, V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 3A, CNR/SS = 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 1MHz, V_{RIPPLE} = 150mV_{P-P}	-	25	-	
PSRR without BIAS	-	V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS = 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ= 120Hz, V_{RIPPLE} = 150mV_{P-P}	-	85	-	dB
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS= 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ= 10kHz, V_{RIPPLE} = 150mV_{P-P}	-	50	-	
		V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 3A, CNR/SS= 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 100kHz, V_{RIPPLE} = 150mV_{P-P}	-	35	-	
		V_{IN}= 3.8V, V_{OUT}= 3.3V, I_{OUT} = 3A, CNR/SS= 1µF, C_{IN} = None, C_{OUT} = 47µF || 10µF || 10µF, FREQ = 1MHz, V_{RIPPLE} = 150mV_{P-P}	-	25	-	
EN						
EN Voltage Rising Threshold	V_{EN}	V_{EN} Rising	0.75	1.0	1.05	V
EN Hysteresis	V_{EN_HYS}	-	-	100	-	mV
EN Leakage	I_{EN}	V_{EN} = 5.5V	-100	-	100	nA

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT}+400mV or 1.4V whichever is greater, V_{BIAS} = OPEN, V_{OUT} = 0.5V, V_{EN} = 5V, I_{OUT} = 0mA, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 100nF. Typical values are at T_A = +25°C, unless otherwise specified. (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ.	Max[1]	Unit
PG						
PG Rising Threshold	PG_{TH}	w.r.t. VOUT	-	-12	-	%
PG Hysteresis	PG_{HYS}	-	-	1	-	%
PG Voltage during VOUT low	PG_{VOL}	I_{PG} = 1mA	-	150	400	mV
Protection						
Internal Current Limit	I_{LIM}	V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} forced to 90% of $V_{OUT\_PROGRAMMED}$	-	5.5	-	A
Thermal Shutdown	T_{OTSD}	Temperature Rising	-	165	-	°C
Thermal Shutdown Hysteresis	T_{OTSD_HYST}	-	-	15	-	°C

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. Compliance to limits is assured by characterization and design.
2. Dropout Voltage is measured with the LDO in an open-loop configuration where FB is disconnected from VOUT. A V_{FB} lower than the reference voltage is applied to the FB pin which causes the error amplifier to drive the main pass-transistor into saturation to try and bring the output voltage (which is sensed through FB) back up into regulation. Because VOUT is disconnected from FB, the output voltage rails up to a margin below V_{IN} and the V_{IN}-V_{OUT} differential is taken to be the dropout voltage.

4. Typical Performance Curves

4.1 PSRR

Operating conditions unless otherwise noted: T_A = 25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = None, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

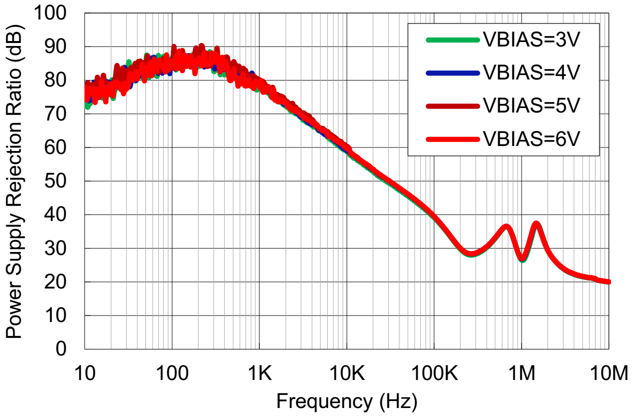


Figure 4. PSRR vs Frequency for Various Bias
(V_{IN} = 1.1V, V_{OUT} = 0.5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

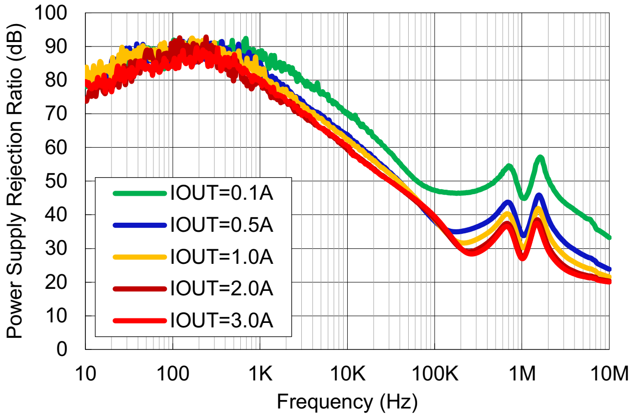


Figure 5. PSRR vs Frequency for Various I_{OUT}
(V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5V, $C_{NR/SS}$ = 1µF)

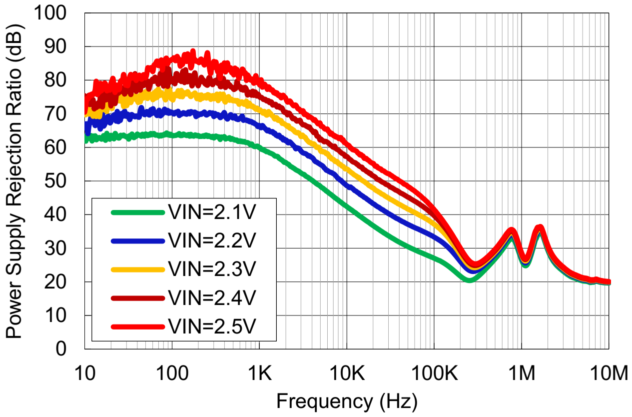


Figure 6. PSRR vs Frequency for Various V_{IN}
(V_{OUT} = 1.8V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

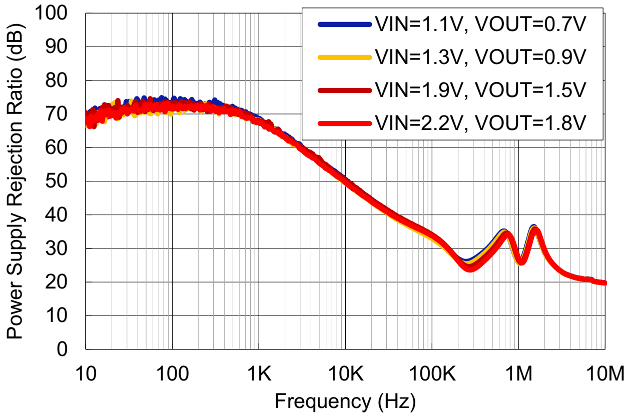


Figure 7. PSRR vs Frequency for Various V_{OUT}
(V_{IN} = V_{OUT} + 0.4V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

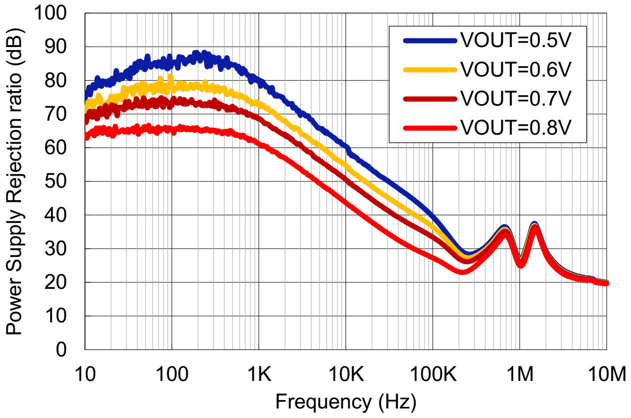


Figure 8. PSRR vs Frequency for Various V_{OUT}
(V_{IN} = 1.1V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

4.2 Output Noise

Operating conditions unless otherwise noted: T_A = 25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

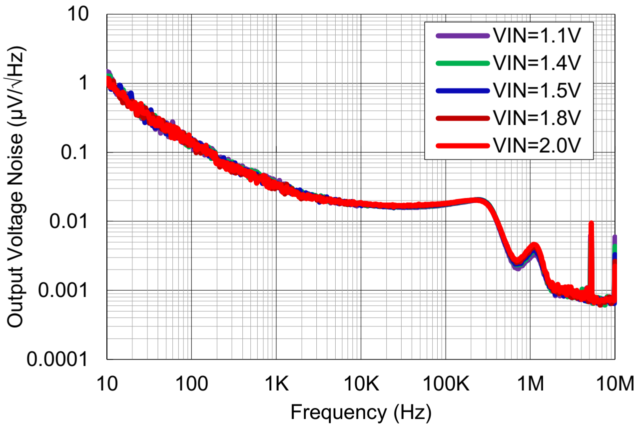


Figure 9. Output Voltage Noise for Various V_{IN} (V_{OUT} = 0.5V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

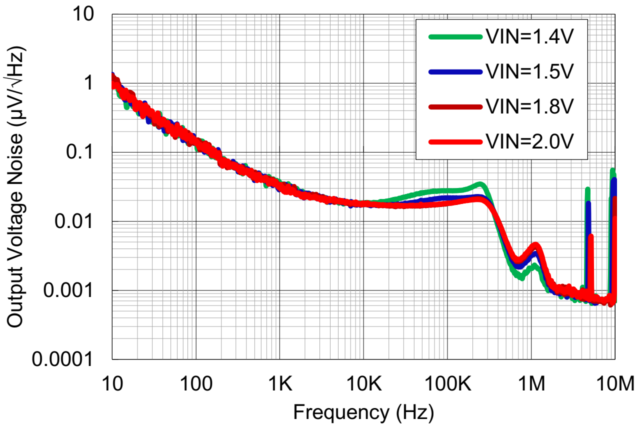


Figure 10. Output Voltage Noise for Various V_{IN} (V_{OUT} = 0.5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

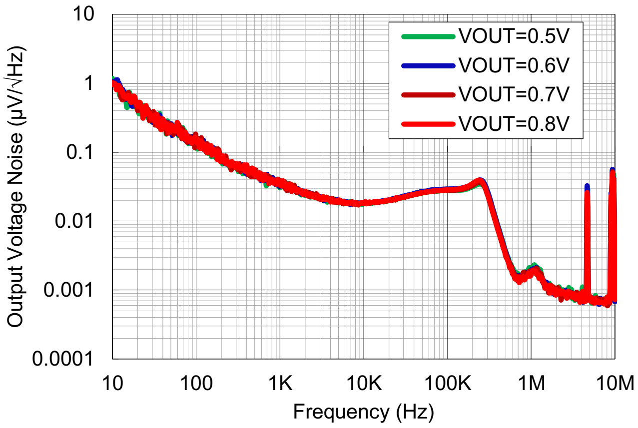


Figure 11. Output Voltage Noise for Various V_{OUT} (V_{IN} = 1.4V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

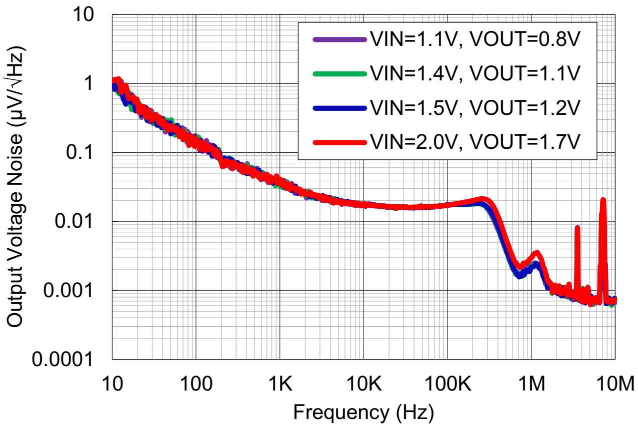


Figure 12. Output Voltage Noise for Various V_{OUT} (V_{IN} = V_{OUT} + 0.3V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

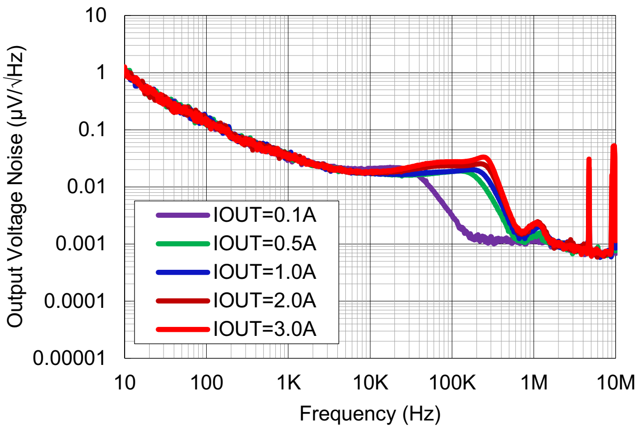


Figure 13. Output Voltage Noise for Various I_{OUT} (V_{IN} = 1.4V, V_{OUT} = 0.5V, $C_{NR/SS}$ = 1µF)

4.3 Start-Up

Operating conditions unless otherwise noted: T_A=25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

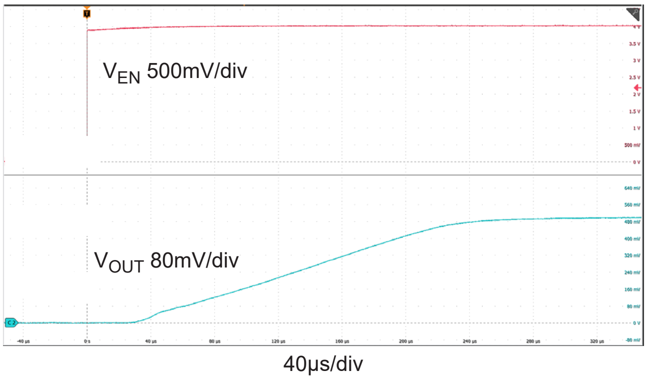


Figure 14. Start-Up (V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

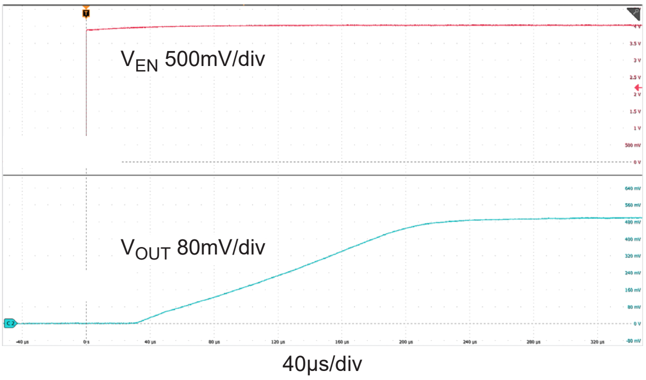


Figure 15. Start-Up (V_{IN} = 1.4V, V_{OUT} = 0.5V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

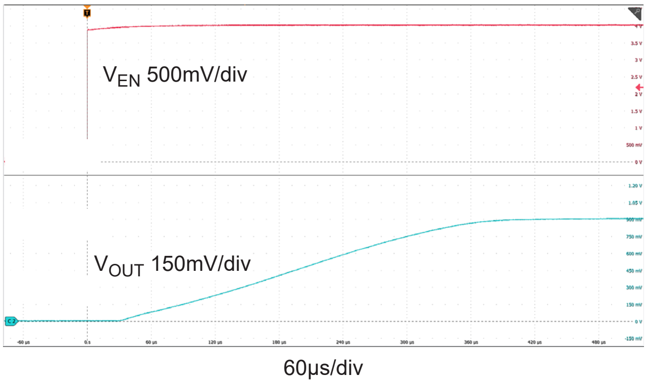


Figure 16. Start-Up (V_{IN} = 1.4V, V_{OUT} = 0.9V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

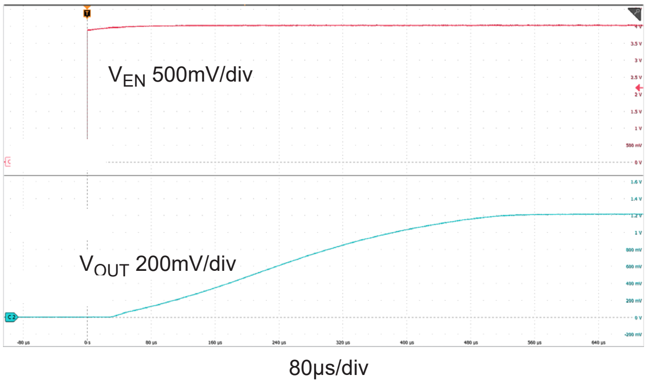


Figure 17. Start-Up (V_{IN} = 1.5V, V_{OUT} = 1.2V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

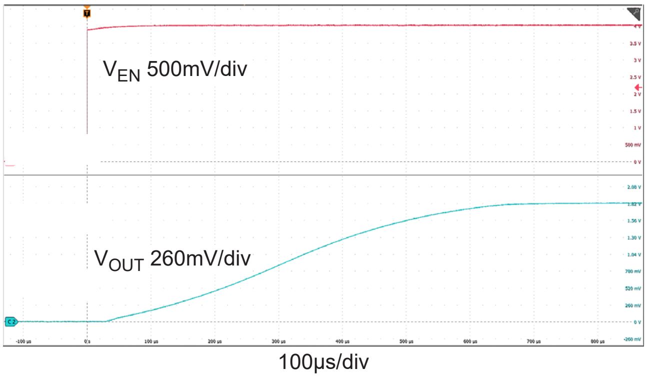


Figure 18. Start-Up (V_{IN} = 2.1V, V_{OUT} = 1.8V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

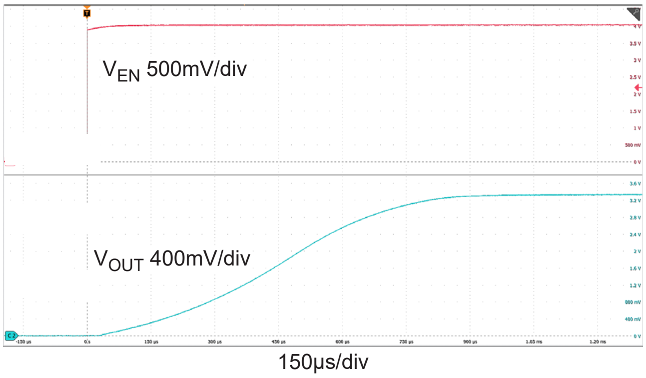


Figure 19. Start-Up (V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 3A, $C_{NR/SS}$ = 1µF)

4.4 Load Transient Response

Operating conditions unless otherwise noted: $T_A = 25°C$, $V_{IN} = V_{OUT}$+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

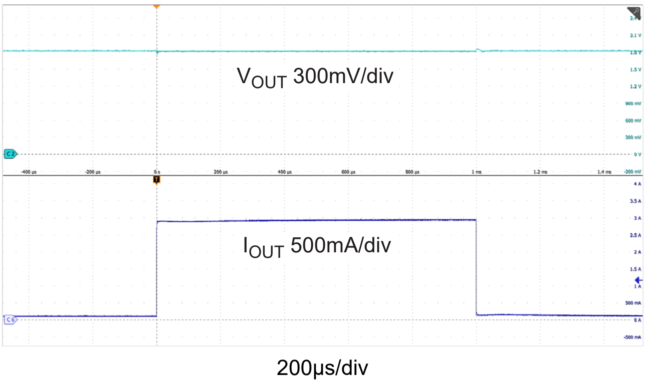


Figure 20. Load Transient Response (V_{IN} = 2.2V, V_{OUT} = 1.8V, ΔI_{OUT} = 0.1A to 3A at 1A/µs, $C_{NR/SS}$ = 1µF)

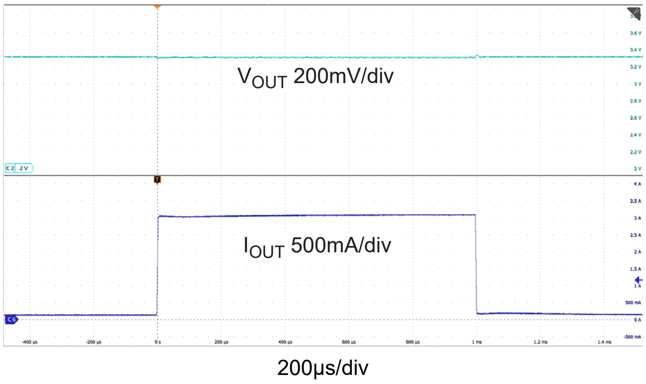


Figure 21. Load Transient Response (V_{IN} = 3.7V, V_{OUT} = 3.3V, ΔI_{OUT} = 0.1A to 3A at 1A/µs, $C_{NR/SS}$ = 1µF)

4.5 Short-Circuit

Operating conditions unless otherwise noted: $T_A = 25°C$, $V_{IN} = V_{OUT}$+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

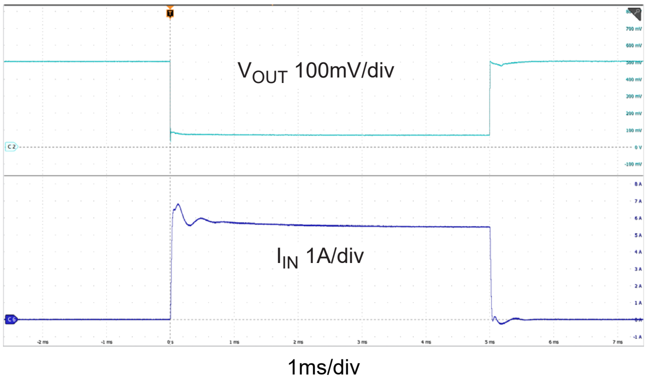


Figure 22. Short-Circuit after Start-Up (V_{IN} = 1.4V, V_{OUT} = 0.5V, $C_{NR/SS}$ = 1µF)

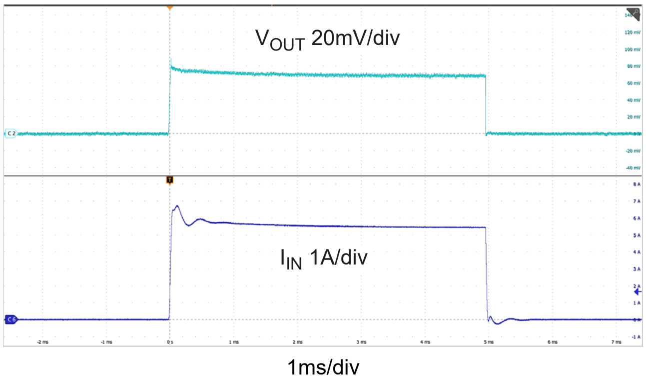


Figure 23. Short-Circuit before Start-Up (V_{IN} = 1.4V, V_{OUT} = 0.5V, $C_{NR/SS}$ = 1µF)

4.6 Dropout Voltage

Operating conditions unless otherwise noted: T_A = 25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = Open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

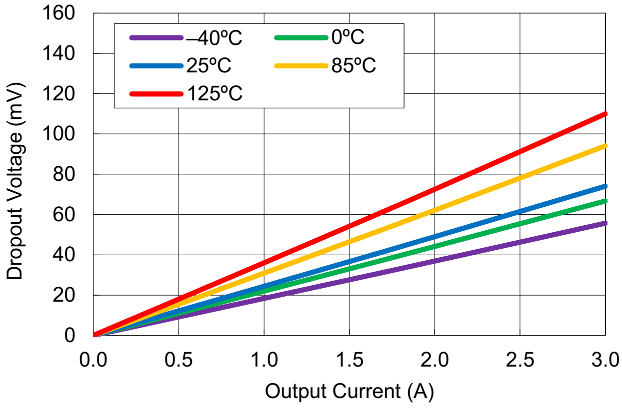


Figure 24. Dropout Voltage vs Output Current (V_{IN} = 1.1V, V_{BIAS} = 5V)

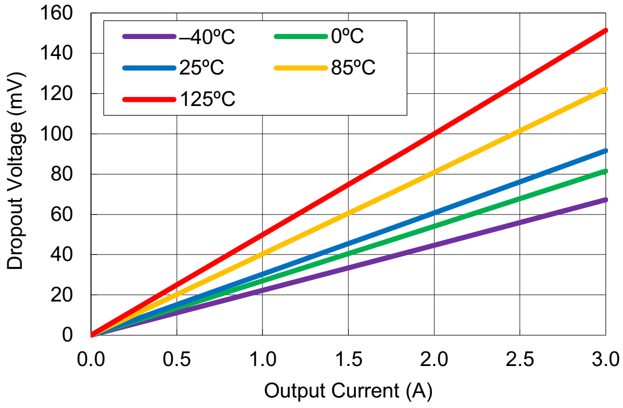


Figure 25. Dropout Voltage vs Output Current (V_{IN} = 1.4V without Bias)

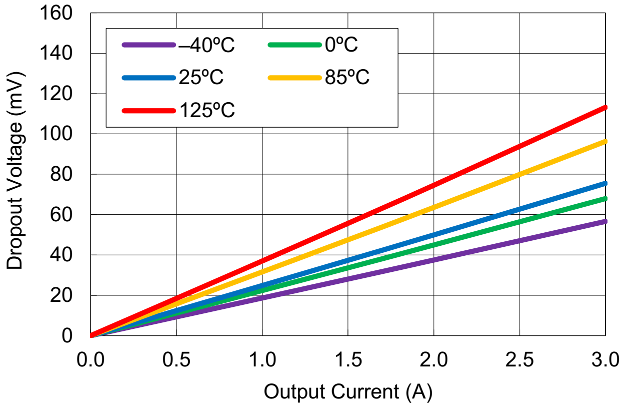


Figure 26. Dropout Voltage vs Output Current (V_{IN} = 3.5V without Bias)

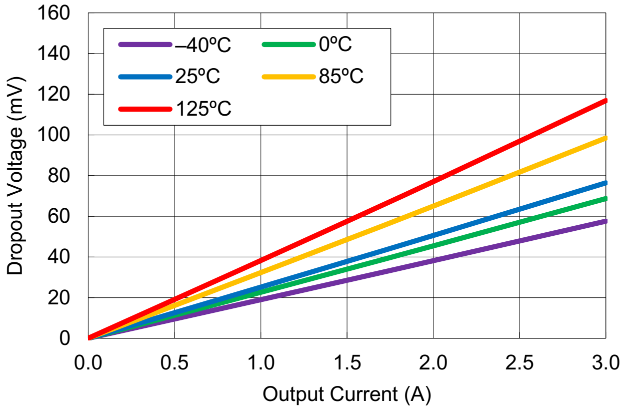


Figure 27. Dropout Voltage vs Output Current (V_{IN} = 5.5V without Bias)

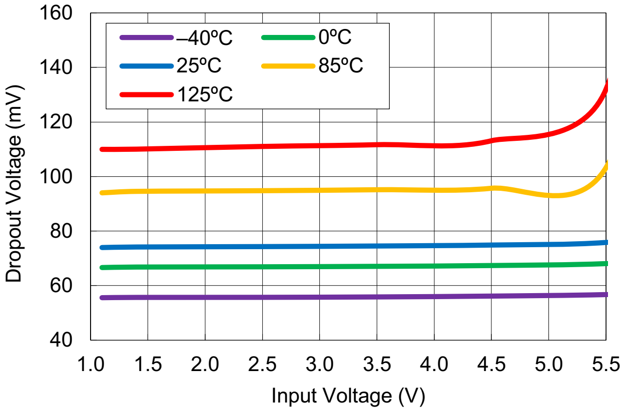


Figure 28. Dropout Voltage vs Input Voltage (V_{BIAS} = 6.5V, I_{OUT} = 3A)

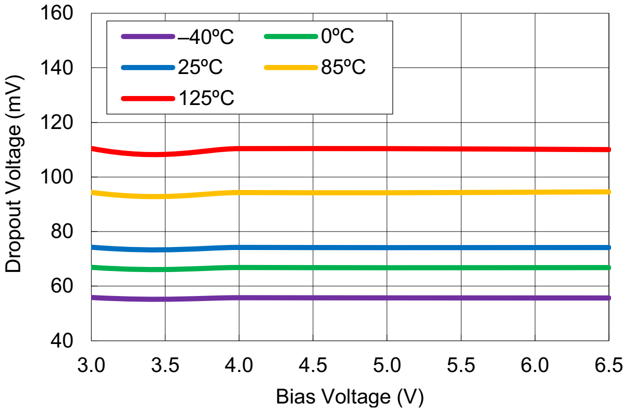


Figure 29. Dropout Voltage vs Bias Voltage (V_{IN} = 1.4V, I_{OUT} = 3A)

4.7 Load and Line Regulation

Operating conditions unless otherwise noted: T_A = 25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

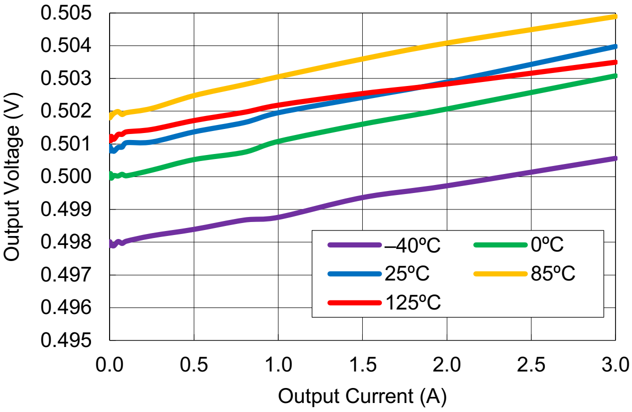


Figure 30. Load Regulation vs Output Current (V_{IN} = 1.1V, V_{BIAS} = 5V, V_{OUT} = 0.5V)

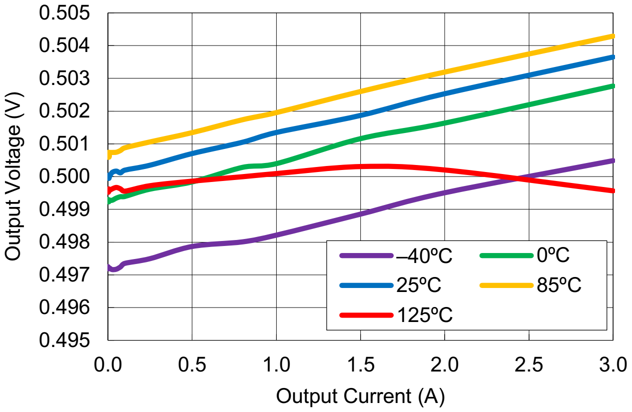


Figure 31. Load Regulation vs Output Current (V_{IN} = 1.4V, V_{OUT} = 0.5V)

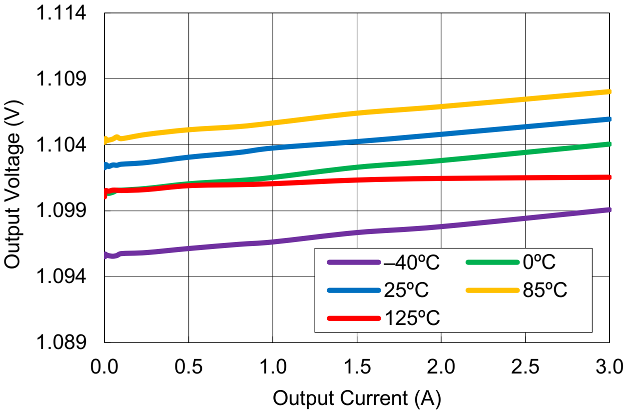


Figure 32. Load Regulation vs Output Current (V_{IN} = 1.5V, V_{OUT} = 1.1V)

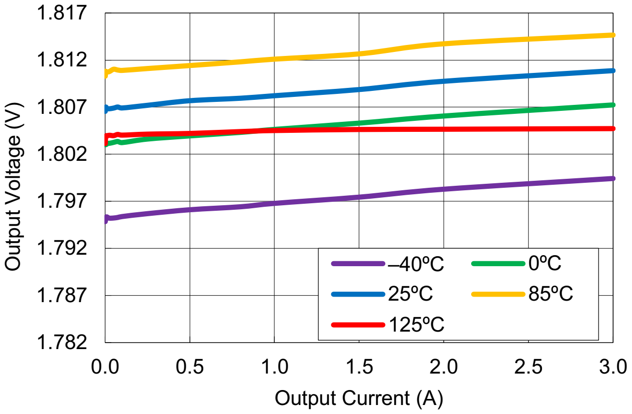


Figure 33. Load Regulation vs Output Current (V_{IN} = 2.2V, V_{OUT} = 1.8V)

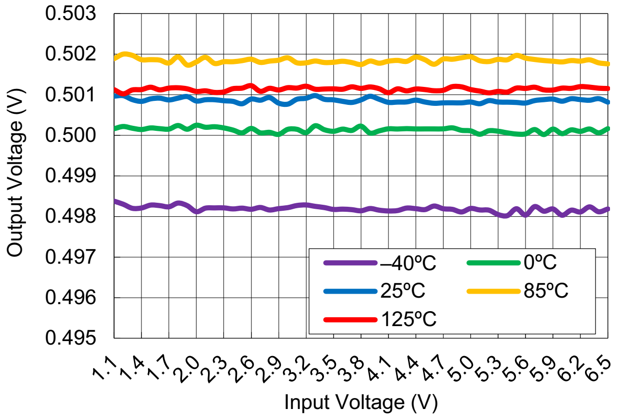


Figure 34. Line Regulation vs Input Voltage (V_{BIAS} = 5V, V_{OUT} = 0.5V, I_{OUT} = 5mA)

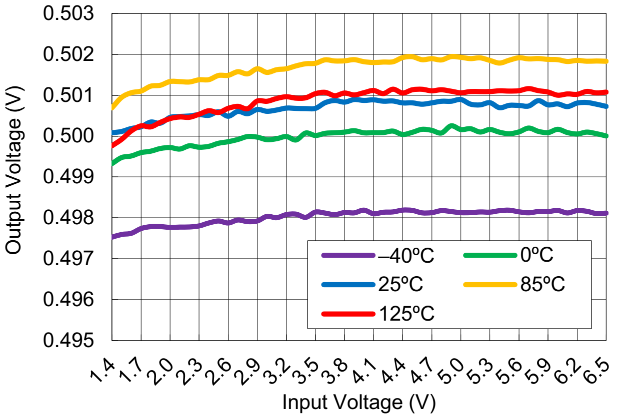


Figure 35. Line Regulation vs Input Voltage (V_{OUT} = 0.5V, I_{OUT} = 5mA)

Operating conditions unless otherwise noted: T_A = 25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ. (Cont.)

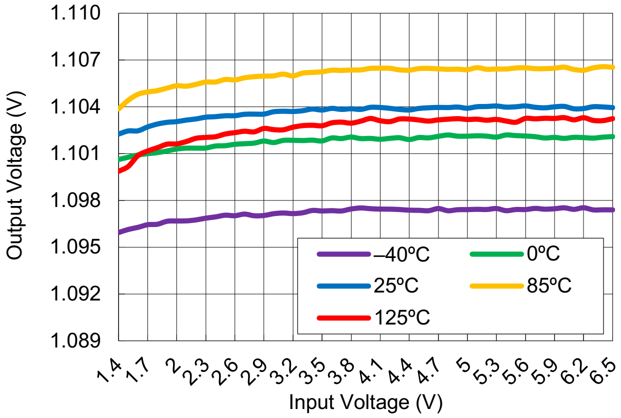


Figure 36. Line Regulation vs Input Voltage (V_{OUT} = 1.1V, I_{OUT} = 5mA)

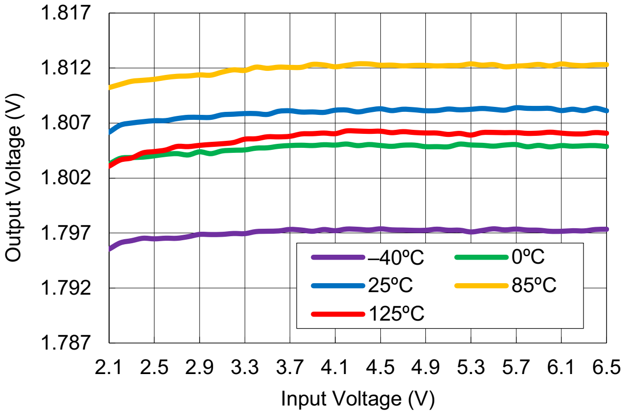


Figure 37. Line Regulation vs Input Voltage (V_{OUT} = 1.8V, I_{OUT} = 5mA)

4.8 Other Typical Performance Curves

Operating conditions unless otherwise noted: T_A = 25°C, V_{IN} = V_{OUT}+0.4V or 1.4V whichever is greater, V_{BIAS} = open, V_{OUT} = 0.5V, VEN tied directly to VIN, C_{IN} = 47||10||10µF, C_{OUT} = 47||10||10µF, $C_{NR/SS}$ = 1µF, and PG pulled up to VIN with 10kΩ.

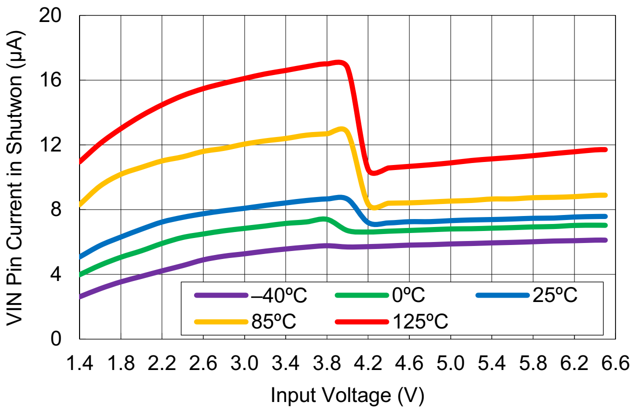


Figure 38. Shutdown Current vs Input Voltage for Various Temperatures

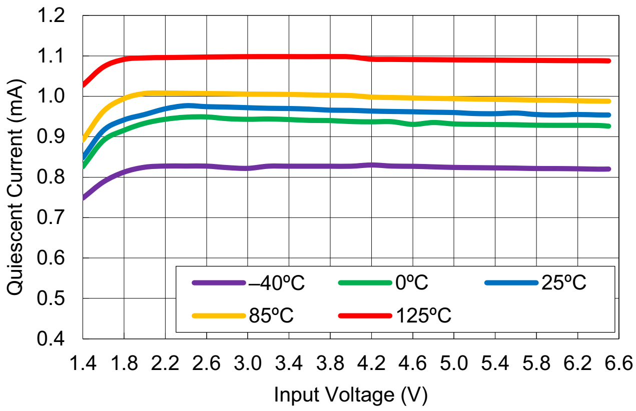


Figure 39. Quiescent Current vs Input Voltage for Various Temperatures

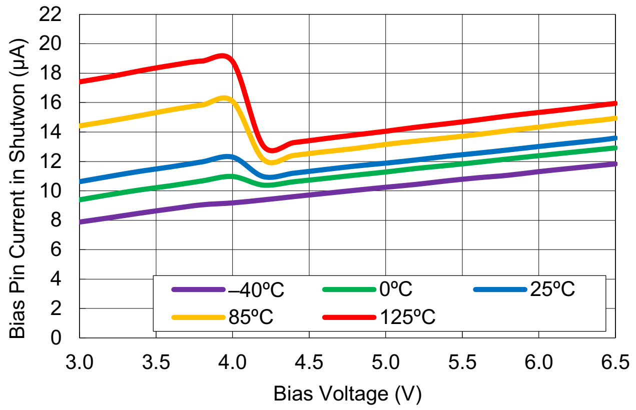


Figure 40. Bias Pin Current in Shutdown vs Bias Voltage for Various Temperatures (V_{IN} = 1.1V)

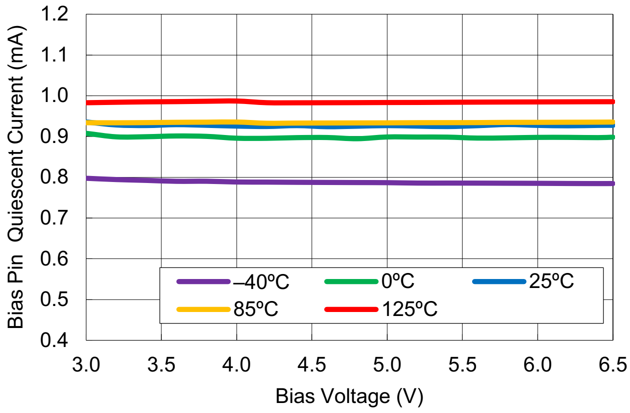


Figure 41. Bias Pin Quiescent Current vs Bias Voltage for Various Temperatures (V_{IN} = 1.1V)

5. Applications Information

5.1 Overview

The RRP51035 is a low-noise, high PSRR, low-dropout (LDO) regulator. The LDO can source up to 3A load current with only 180mV dropout voltage. It operates from an input voltage of 1.1V to 6.5V (with a minimum 3V BIAS) for very low input voltage applications with ±1% accuracy over line, load, and temperature. The output voltage can be programmed from 0.5V to 2.075V using output voltage setting pins on the IC in 25mV steps or from 0.5V to 5.1V using external feedback resistors.

The RRP51035 is designed and tested with a 10µF ceramic input capacitor, 22µF ceramic output capacitor, a 1µF noise-reduction, a soft-start capacitor ($C_{NR/SS}$), and a 10µF BIAS capacitor if VBIAS is being used. The LDO is available in a 20-Ld 3.5mm×3.5mm QFN package.

The RRP51035 integrates the following additional features in this package:

- High Output Accuracy (±1%)
- Low Output Noise
- High PSRR
- No sequencing requirement between VBIAS, VIN, and VEN
- Power-Good Indication
- Convenient Output Voltage Set Pins to program the LDO output
- Undervoltage Lockout (UVLO)
- Enable Control
- Internal Current Limit Protection
- Thermal Shutdown Protection
- Minimum 22µF ceramic output capacitor for stability
- Output Capacitor automatic discharge
- BIAS Pin for lower dropout voltage and lower VIN performance

5.2 Theory of Operation of NMOS LDOs

Like the majority of LDOs with an NMOS pass transistor, the RRP51035 output voltage (V_{OUT}) regulation can be modeled with a voltage reference (V_{REF}), feedback (FB) resistors, error amplifier, and NMOS pass-transistor as shown in Figure 42.

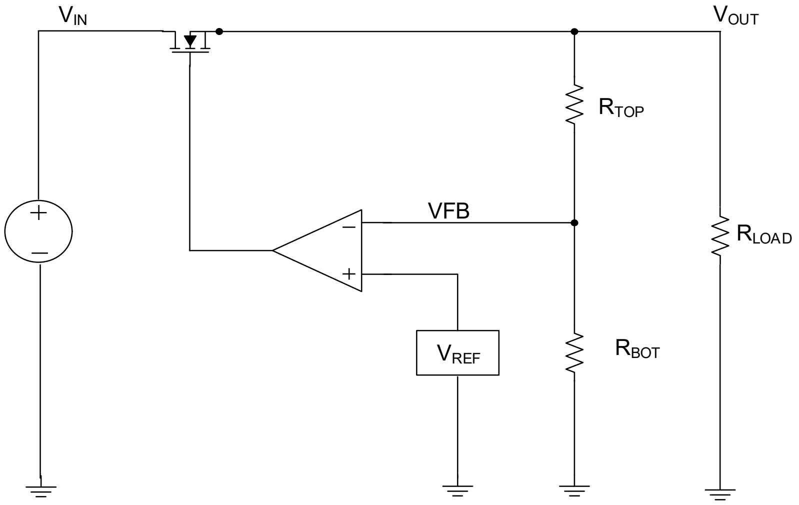


Figure 42. Simple NMOS LDO Regulator Block Diagram

The NMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assume the input voltage (V_{IN}) remains constant and the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}.

Equation 1 summarizes this relationship.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times r_{DS(ON)}$$

V_{OUT} is set using the FB resistor divider, which sets V_{OUT} to a value that corresponds to Equation 2.

(EQ. 2) $$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

The error amplifier compares V_{FB} with the fixed V_{REF} voltage and works to minimize the difference between VFB and VREF by changing the gate voltage of the NMOS pass transistor and, therefore, the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} decreases because the regulator has not responded to the change, and the $r_{DS(ON)}$ is set too high. V_{FB} correspondingly decreases and is below the V_{REF} voltage, therefore increasing the error voltage. The error amplifier senses and minimizes the error by driving the NMOS gate voltage more positively relative to the FET source to decrease the $R_{DS(ON)}$, which increases the output voltage, bringing it back into regulation.

By similar logic, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to increase because the $r_{DS(ON)}$ is set too low. V_{FB} is then higher than the fixed V_{REF} voltage, increasing the error. The error amplifier senses and minimizes the error by driving the NMOS gate voltage more negatively relative to the FET source to increase the $r_{DS(ON)}$, which decreases the output voltage, bringing it back into regulation.

6. Functional Description

6.1 Low Output Noise

The LDO output noise is the internally generated noise created largely by the band-gap voltage reference and the error amplifier. The output noise is commonly represented in units of nV/√Hz for a specific frequency or as an integrated root-mean square (RMS) value in µV over a range of frequencies typically 10Hz to 100kHz or 100Hz to 100kHZ.

The RRP51035 output noise is largely independent of the output voltage and does not require a feed-forward capacitor to achieve very low output noise. On the other hand, it depends on the output current, $C_{NR/SS}$, and C_{OUT} capacitor. The CNR/SS improves the low-frequency output noise of the LDO. Renesas recommends using a 1µF $C_{NR/SS}$ capacitor for the best low-output noise. See $C_{NR/SS}$ Capacitor for selecting the correct noise-reduction and soft-start capacitor. C_{OUT} improves the noise at high-frequencies by reducing the high-frequency output impedance of the LDO. See the Output Capacitor (C_{OUT}) section for selecting the correct output capacitor.

6.2 High Power-Supply Ripple-Rejection (PSRR)

The PSRR is how much attenuation or rejection the LDO control loop gives to externally generated input voltage noise, such as from a switching regulator. Although PSRR represents a loss in the input noise signal, it is common to see it as a positive decibel (dB) number. Mathematically, PSRR is represented as a logarithmic ratio between an input and output ripple sinusoid signal at a specific frequency as shown in Equation 3.

(EQ. 3) $$PSRR(dB) = 20 \times \log\left(\frac{V_{IN(RIPPLE)}}{V_{OUT(RIPPLE)}}\right)$$

The PSRR for the RRP51035 is largely independent of the output voltage and does not require a feed-forward capacitor. On the other hand, it depends on the output current, headroom voltage (V_{IN}-V_{OUT}), $C_{NR/SS}$ capacitor, C_{OUT} capacitor, and PCB layout.

The higher the output current, the lower the PSRR is across all frequencies compared to a lower output current. The PSRR at low- and mid-frequencies can be improved by increasing the headroom voltage, but this comes at the cost of increased power dissipation. If the headroom is lowered, it decreases the power dissipation and lowers the PSRR at low- to mid-frequencies.

6.3 VBIAS, VIN, and VEN Sequencing

The RRP51035 the VBIAS, VIN, and VEN pins do not need to be powered on in any specific order. Table 1 gives the status of the LDO and various circuits depending on the status of VBIAS, VIN, and VEN.

Table 1. VBIAS, VIN, and VEN Functionality

VIN Status	VBIAS Status	VEN Status	LDO Status	Active Discharge	V_{PG} Status
$V_{IN} \geq V_{UVLO(RISING)}$	$V_{BIAS} \geq V_{UVLO(BIAS)(RISING)}$	V_{EN} = HIGH	ON	OFF	V_{PG} = HIGH or High-Z when $V_{OUT} \geq 0.88 \times V_{OUT\_SET}$
		V_{EN} = LOW	OFF	ON[1]	V_{PG}= LOW
	$V_{BIAS} < V_{UVLO(BIAS)(RISING)}$	Status does not matter			
$V_{IN} \leq V_{UVLO(FALLING)}$	Status does not matter				

1. The output discharge circuitry remains enabled if V_{IN} does not drop below 0.9V (typical) or V_{BIAS} does not drop below 2.75V (typical).

6.4 UVLO

The RRP51035 integrates an internal UVLO circuit to keep the output voltage safely DISABLED if the input voltage or bias voltage is below the UVLO threshold. When the input voltage is above the UVLO threshold, the part is ENABLED, and the output voltage ramps up into regulation. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate.

When the input voltage is below the UVLO, an internal 300Ω discharge resistor connects the LDO output to ground to quickly discharge the output capacitor. The resistor is connected to the output capacitor when the input voltage exceeds 0.9V but less than the UVLO threshold of 1V (typical). Figure 43 illustrates the UVLO operation.

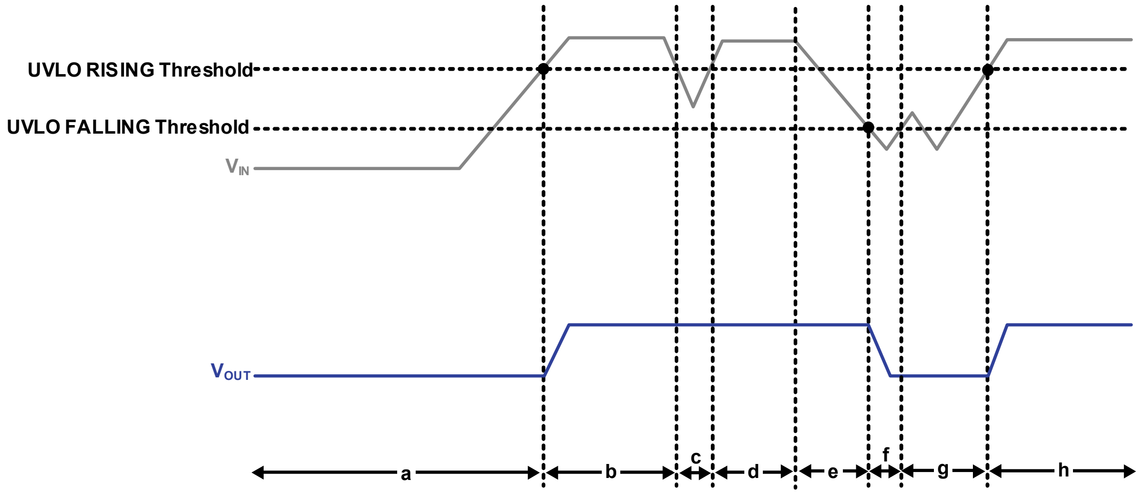


Figure 43. UVLO Operation

- a – The input voltage has not reached the UVLO Rising threshold (1V), so the LDO remains disabled. The 300Ω internal discharge resistor is connected to the output voltage if the input voltage is above the UVLO riding threshold between 0.9V and 1V.
- b – The LDO is enabled, and the output rises to its regulated programmed value when the UVLO RISING threshold is reached by the input voltage (1V). At the same time, the 300Ω discharge resistor is disconnected from VOUT.
- c – A brownout occurs, but the LDO remains enabled, and the 300Ω discharge resistor remains disconnected because the input voltage has not reached the UVLO FALLING threshold (0.9V). The output voltage can still fall out of regulation.
- d – Output is regulated to its programmed output voltage value.
- e – The input voltage is turned OFF but has not yet crossed the UVLO FALLING threshold (0.9V), so the LDO is still enabled, and the 300Ω discharge resistor remains disconnected. The output voltage can fall out of regulation.
- f – The input voltage turns OFF, and the output voltage falls due to the load and 300Ω discharge resistor, which remains connected to VOUT if the input voltage is between 0.9V and 1V. The LDO is disabled.
- g – The LDO remains disabled because the input voltage has not reached the UVLO RISING threshold (1V). The 300Ω internal discharge resistor remains connected to the output voltage if the input voltage is between 0.9V and 1V.
- h – Output is regulated to its programmed output voltage value.

6.5 Power-Good (PG) Indication

The Power-Good (PG) pin is an open-drain NMOS-FET. The PG pin circuitry monitors the FB pin voltage to indicate whether the output voltage is 12% below its programmed value (Undervoltage (UV) threshold). When the output voltage is 12% below its programmed value, the PG circuitry drives the NMOS FET ON and indicates LOW on the PG pin. If the output voltage exceeds 88% of its programmed value, the PG circuitry drives the NMOS-FET OFF, and the PG pin becomes HIGH. When the output voltage is below the PG UV thresholds, the fast-start-up circuitry is activated to bring the output voltage above the 88% nominal value.

Renesas recommends using a 10kΩ or greater pull-up resistor to tie the PG pin to VIN, VOUT, or an external supply to ensure a proper HIGH voltage to any downstream logic device such as an MCU or FPGA. If the PG pin is not used, it can be left floating. The 10kΩ lower limit results from the maximum pull-down strength of the NMOS-FET. Working outside of this range may result in invalid digital logic level readings.

6.6 Enable Control

The RRP51035 uses the EN pin voltage (V_{EN}) to enable or disable the LDO. On power-up, if the enable voltage remains lower than the V_{EN} Rising threshold ($V_{EN} \le 1V$), the LDO remains DISABLED. If V_{EN} exceeds the V_{EN} Rising threshold ($V_{EN} \ge 1V$ typical), the LDO is ENABLED. When V_{EN} falls below the V_{EN} falling threshold (VEN ≤ 0.9V), the LDO is DISABLED. The V_{EN} hysteresis (100mV) prevents the enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically 9µA.

When the LDO is disabled, and the input voltage is greater than or equal to 0.9V, the same 300Ω discharge resistor controlled by the UVLO circuitry is connected between the LDO output and GND to discharge the output capacitor quickly.

Connect the EN pin directly to the input voltage for automatic start-up or to a logic controller such as an MCU of FPGA. Some logic pins use an open-collector or open-drain transistor to pull LOW and float when HIGH. Make sure to connect a 10kΩ pull-up resistor to ensure proper logic HIGH. To ensure proper Enable control operation, ensure the V_{EN} signal source can swing above and below the threshold values.

6.7 Internal Current Limit (I_{LIM})

The internal current limit (ILIM) circuitry limits the maximum output current the RRP51035 can source to the load during start-up due to in-rush current or during faults such as output short-circuits. ILIM is set above the maximum recommended output current of the RRP51035 (3A).

During in-rush current or fault events, the LDO becomes a constant current source, and as a result, any decrease in load resistance causes a decrease in the output voltage. The LDO returns to regulation when the short or overcurrent condition is removed. Because of the high power dissipation caused by overcurrent faults, the LDO may begin to cycle ON and OFF due to the thermal shutdown circuitry. The thermal shutdown circuitry turns the LDO OFF when the die junction temperature exceeds thermal fault conditions (+165°C) and turns the LDO ON after cooling to +150°C when the LDO output is OFF.

6.8 Thermal Protection

The RRP51035 is protected against thermal overloads caused by excessive power dissipation, such as during overcurrent conditions or high ambient temperatures.

When the die junction temperature exceeds +165°C, the thermal shutdown circuit disables the LDO, shutting off the output and allowing the LDO to cool. A 15°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a junction temperature exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, the design must consider the ambient temperature that the LDO works in, the junction-to-ambient thermal resistance (θ_{JA}), and any fault conditions that can cause the junction to exceed the recommended operating range. In some applications, a heat sink may need to be implemented. See Power Dissipation and Thermals to approximate the maximum junction temperature for an application.

6.9 Output Capacitor Automatic Discharge

The RRP51035 features a 300Ω discharge resistor that rapidly discharges the output capacitor when the LDO is disabled. The UVLO and ENABLE circuitry control the 300Ω discharge resistor.

The 300Ω discharge resistor is connected to the LDO output when the LDO is disabled using the ENABLE or UVLO circuitry and when the input voltage or VBIAS voltage is greater than or equal to 1V. If the input voltage collapses faster than the discharge circuitry can discharge the output capacitor, the output voltage may be greater than the input voltage. In this case, C_{OUT} discharges through the NMOS transistor body diode.

6.10 BIAS

Using a BIAS voltage ≥ 3.3V for V_{IN}s less than 3.3V improves the dropout voltage and PSRR.

6.11 Output Accuracy

The RRP51035 features an output voltage accuracy of 1% maximum, including the errors introduced by the internal reference, load regulation, line regulation, and operating temperature as specified by the Electrical Characteristics tables. The output voltage accuracy specifies minimum and maximum output voltage error, with respect to the nominal output voltage stated as a percent.

7. Application Requirements

7.1 Input Voltage

The RRP51035 operates with an input voltage of 1.4V to 6.5V on the VIN pin (without BIAS) and from 1.1V to 6.5V on the VIN pin (with a minimum of 3V BIAS). If $V_{IN} \geq V_{BIAS}$, it is pointless to use the BIAS pin.

The input supply must be able to supply the required current the LDO needs to supply to the load. For proper regulation, ensure the input voltage is higher than the sum of the output voltage and the maximum dropout voltage expected for a given application as expressed in Equation 4.

(EQ. 4) $$V_{IN} > V_{OUT} + V_{DROPOUT(max)}$$

7.2 Programming the Output Voltage

The output voltage can be programmed using convenient output voltage set pins on the IC or traditional external feedback resistors.

7.2.1 Internal Feedback Resistors and Output Voltage Set Pins

The RRP51035 has convenient IC pins that connect an array of internal FB resistors to program the output voltage easily. In this configuration, the output voltage can be programmed from 0.5V to 2.075V in steps of 25mV.

Important: To use the internal FB resistors and convenient IC voltage set pins to program the output voltage, the SNS pin must be shorted to the VOUT(s) pins.

The Voltage Set pins are labeled 25mV (Pin 5), 50mV (pin 6), 100mV (Pin 7), 200mV (Pin 9), 400mV (Pin 10) and 800mV (Pin 11). These pins are either grounded or left floating using the PCB layout. Grounding these pins adds the voltages assigned to each grounded pin to the 0.5V reference voltage as shown in Equation 5.

(EQ. 5) $$V_{OUT} = 0.5V + \Sigma(\text{Grounded Output Voltage Set Pins})$$

For example, to program the output voltage to 1.8V, ground the 800mV, 400mV, and 100mV pins. The sum of these three pins (1.3V) added to the 0.5V reference equals the required 1.8V output. Figure 44 through Figure 53 illustrate how to connect the LDO output voltage set pins to get various common output voltage rails.

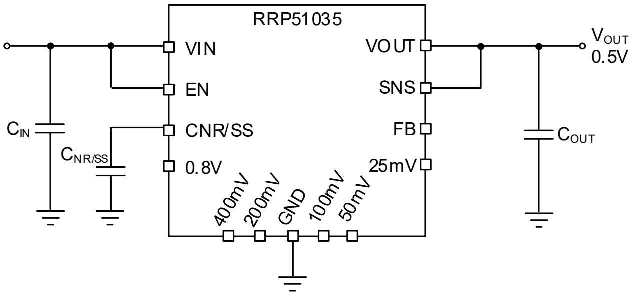


Figure 44. Internal FB Resistor Configuration for 0.5V (V_{OUT} = 0.5VREF)

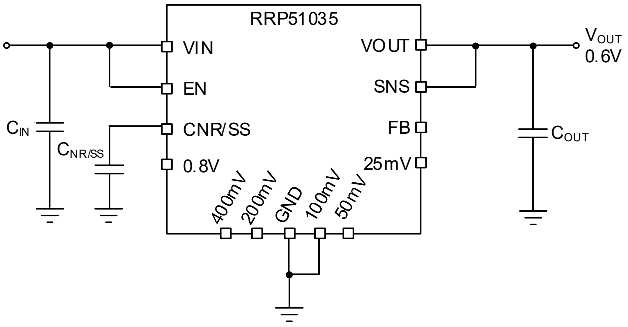


Figure 45. Internal FB Resistor Configuration for 0.6V (V_{OUT} = 0.5VREF + 100mV)

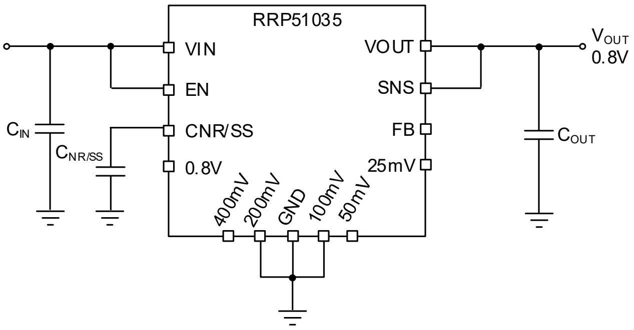


Figure 46. Internal FB Resistor Configuration for 0.8V (V_{OUT} = 0.5VREF + 200mV + 100mV)

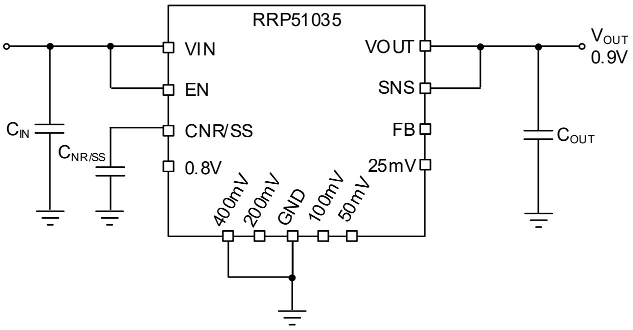


Figure 47. Internal FB Resistor Configuration for 0.9V (V_{OUT} = 0.5VREF + 400mV)

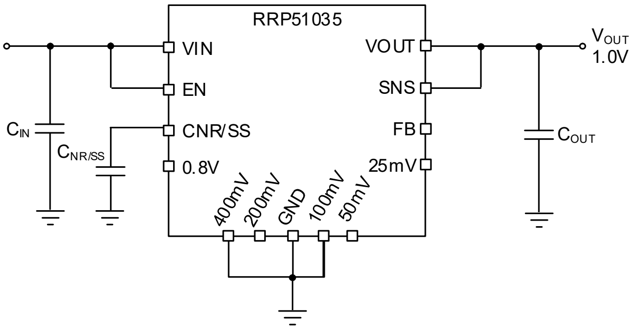


Figure 48. Internal FB Resistor Configuration for 1.0V (V_{OUT} = 0.5VREF + 400mV + 100mV)

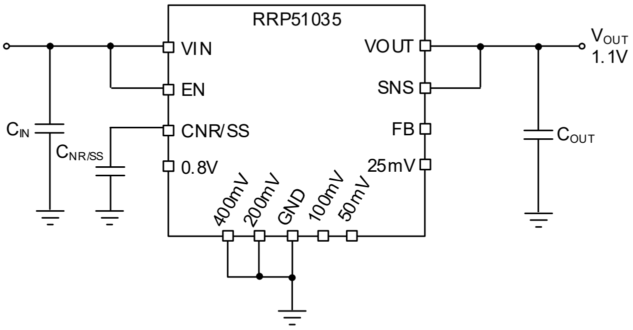


Figure 49. Internal FB Resistor Configuration for 1.1V (V_{OUT} = 0.5VREF + 400mV + 200mV)

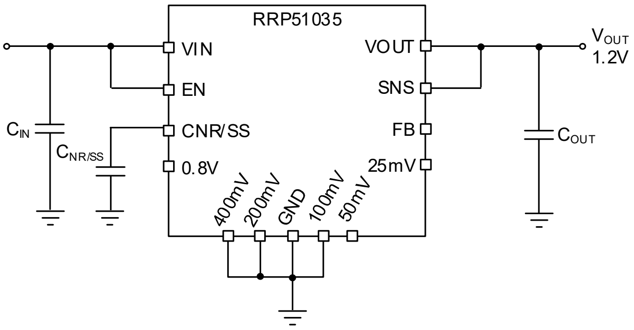


Figure 50. Internal FB Resistor Configuration for 1.2V (V_{OUT} = 0.5VREF + 400mV + 200mV + 100mV)

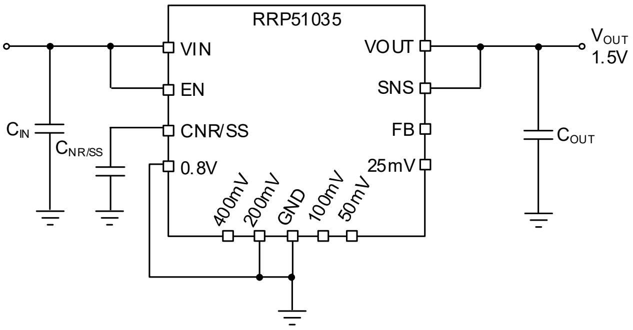


Figure 51. Internal FB Resistor Configuration for 1.5V (V_{OUT} = 0.5VREF + 800mV + 200mV)

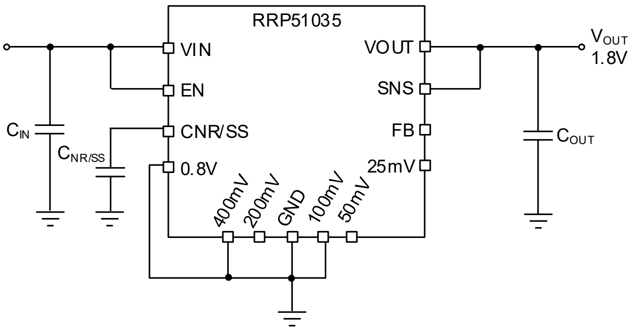


Figure 52. Internal FB Resistor Configuration for 1.8V (V_{OUT} = 0.5VREF + 800mV + 400mV + 100mV)

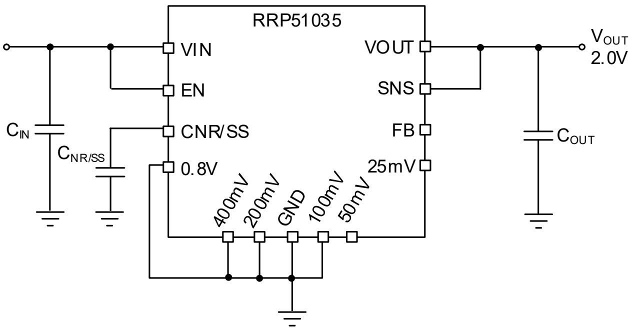


Figure 53. Internal FB Resistor Configuration for 2.0V (V_{OUT} = 0.5VREF + 800mV+ 400mV + 200mV + 100mV)

Table 2 shows all possible output voltages and the corresponding Voltage Set pins to short to GND or leave floating.

Table 2. Output Voltage Set Pin Configuration and corresponding Output Voltages (V_{REF} = 0.5V)

V_{OUT} (V)	25mV	50mV	100mV	200mV	400mV	800mV
0.500	Open	Open	Open	Open	Open	Open
0.525	GND	Open	Open	Open	Open	Open
0.550	Open	GND	Open	Open	Open	Open
0.575	GND	GND	Open	Open	Open	Open
0.600	Open	Open	GND	Open	Open	Open
0.625	GND	Open	GND	Open	Open	Open
0.650	Open	GND	GND	Open	Open	Open
0.675	GND	GND	GND	Open	Open	Open
0.700	Open	Open	Open	GND	Open	Open
0.725	GND	Open	Open	GND	Open	Open
0.750	Open	GND	Open	GND	Open	Open
0.775	GND	GND	Open	GND	Open	Open
0.800	Open	Open	GND	GND	Open	Open
0.825	GND	Open	GND	GND	Open	Open
0.850	Open	GND	GND	GND	Open	Open
0.875	GND	GND	GND	GND	Open	Open
0.900	Open	Open	Open	Open	GND	Open
0.925	GND	Open	Open	Open	GND	Open
0.950	Open	GND	Open	Open	GND	Open
0.975	GND	GND	Open	Open	GND	Open
1.300	Open	Open	Open	Open	Open	GND
1.325	GND	Open	Open	Open	Open	GND
1.350	Open	GND	Open	Open	Open	GND
1.375	GND	GND	Open	Open	Open	GND
1.400	Open	Open	GND	Open	Open	GND
1.425	GND	Open	GND	Open	Open	GND
1.450	Open	GND	GND	Open	Open	GND
1.475	GND	GND	GND	Open	Open	GND
1.500	Open	Open	Open	GND	Open	GND
1.525	GND	Open	Open	GND	Open	GND
1.550	Open	GND	Open	GND	Open	GND
1.575	GND	GND	Open	GND	Open	GND
1.600	Open	Open	GND	GND	Open	GND
1.625	GND	Open	GND	GND	Open	GND
1.650	Open	GND	GND	GND	Open	GND
1.675	GND	GND	GND	GND	Open	GND
1.700	Open	Open	Open	Open	GND	GND
1.725	GND	Open	Open	Open	GND	GND
1.750	Open	GND	Open	Open	GND	GND
1.775	GND	GND	Open	Open	GND	GND

Table 2. Output Voltage Set Pin Configuration and corresponding Output Voltages (V_{REF} = 0.5V) (Cont.)

V_{OUT} (V)	25mV	50mV	100mV	200mV	400mV	800mV
1.000	Open	Open	GND	Open	GND	Open
1.025	GND	Open	GND	Open	GND	Open
1.050	Open	GND	GND	Open	GND	Open
1.075	GND	GND	GND	Open	GND	Open
1.100	Open	Open	Open	GND	GND	Open
1.125	GND	Open	Open	GND	GND	Open
1.150	Open	GND	Open	GND	GND	Open
1.175	GND	GND	Open	GND	GND	Open
1.200	Open	Open	GND	GND	GND	Open
1.225	GND	Open	GND	GND	GND	Open
1.250	Open	GND	GND	GND	GND	Open
1.275	GND	GND	GND	GND	GND	Open
1.800	Open	Open	GND	Open	GND	GND
1.825	GND	Open	GND	Open	GND	GND
1.850	Open	GND	GND	Open	GND	GND
1.875	GND	GND	GND	Open	GND	GND
1.900	Open	Open	Open	GND	GND	GND
1.925	GND	Open	Open	GND	GND	GND
1.950	Open	GND	Open	GND	GND	GND
1.975	GND	GND	Open	GND	GND	GND
2.000	Open	Open	GND	GND	GND	GND
2.025	GND	Open	GND	GND	GND	GND
2.050	Open	GND	GND	GND	GND	GND
2.075	GND	GND	GND	GND	GND	GND

7.2.2 External Feedback Resistors

The RRP51035 output voltage can be programmed down to 0.5V and up to 5.1V using external FB resistors (R_{TOP} and R_{BOT}) as shown in Figure 54.

Important: The SNS pin must be left floating to use the external FB resistors to program the output voltage.

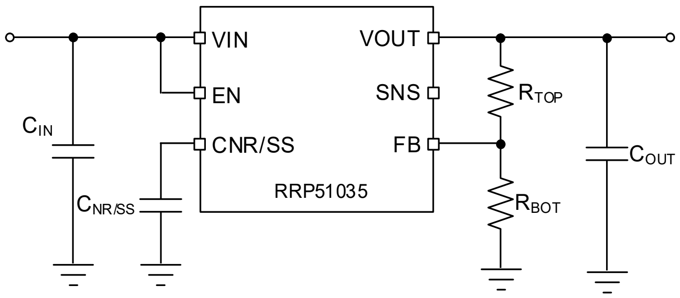


Figure 54. Simplified External FB Resistor Schematic

Use Equation 6 to calculate V_{OUT}.

(EQ. 6)

$$V_{OUT} = 0.5V \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Calculate the R_{BOT} resistor for any target output voltage by rearranging Equation 6 to get Equation 7.

(EQ. 7)

$$R_{BOT} = R_{TOP} \times \left(\frac{0.5V}{V_{OUT} - 0.5V}\right)$$

Similarly, use Equation 8 to calculate the R_{TOP} resistor.

(EQ. 8)
$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OUT}}{0.5V} - 1\right)$$

Table 3 lists recommended FB resistor values to obtain some standard output voltages for the RRP51035. The FB resistors are commercially available in 1% tolerances. This list is non-exhaustive.

Table 3. Recommended FB Resistor Values for Common Output Voltages for the RRP51035 (V_{REF}= 0.5V)

$V_{OUT(TARGET)}$ (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	$V_{OUT(CALCULATED)}$ (V)	Accuracy
0.5	0	DNP	0.500	0.00%
0.6	11.0	54.9	0.600	0.03%
0.7	10.2	25.5	0.700	0.00%
0.75	10.0	20.0	0.750	0.00%
0.8	10.7	17.8	0.801	0.07%
0.9	11.0	13.7	0.901	0.16%
1	12.4	12.4	1.000	0.00%
1.05	11.0	10.0	1.050	0.00%
1.1	10.7	8.9	1.101	0.10%
1.2	9.31	6.7	1.195	-0.44%
1.5	12.4	6.19	1.502	0.11%
1.8	10.2	3.92	1.801	0.06%
1.9	12.4	4.42	1.903	0.14%
2.5	12.4	3.09	2.506	0.26%
3	12.4	2.49	2.990	-0.33%
3.3	10.7	1.91	3.301	-0.03%
3.6	12.4	2.00	3.600	0.00%
4.2	12.1	1.64	4.189	-0.26%
4.5	14.7	1.84	4.495	-0.12%
5	12.7	1.41	5.004	0.07%
5.1	20.5	2.23	5.096	-0.07%

7.3 Bias Voltage

A 3V to 6.5V voltage must be applied to VBIAS to lower the minimum input voltage from 1.4V to 1.1V. For lower dropout voltages when V_{IN} > 1.4V, apply a 3V to 6.5V voltage to VBIAS.

7.4 External Bypass Capacitor Selection

The RRP51035 requires using C_{IN}, C_{OUT}, and $C_{NR/SS}$ bypass capacitors to operate properly. The C_{BIAS} bypass capacitor is only required if using BIAS. Otherwise, it can be left out with no impact on LDO performance.

Multi-layer ceramic capacitors (MLCC) are a great choice for bypass capacitors because of their small size, low ESR, low ESL, and wider operating temperature than tantalums and aluminum capacitors. When choosing a ceramic capacitor for an application it’s important to consider the voltage rating, voltage coefficient, and temperature coefficient.

During PCB layout, place C_{IN}, C_{OUT}, $C_{NR/SS,}$ and C_{BIAS} as close as practical to their respective pins to minimize trace inductance. Renesas recommends verifying the expected capacitance and capacitor performance in the circuit before production.

7.4.1 Input Capacitor (C_{IN})

The minimum input capacitor required on the VIN pin for proper operation and stability is 10µF. A 10µF input capacitor also helps reduce the damaging effects of large input impedances because of long input traces or high source impedances. Additional bypass capacitors with different self-resonant frequencies can be paralleled with 10µF to keep the input impedance low across a wider frequency range if required.

Input capacitors greater than 10µF can also help minimize input voltage drops during significant changes in load current and during start-up and do not affect stability.

Important: Ensure that the combination of trace and wire inductance and the input capacitor chosen do not cause unwanted ringing because of the resonance formed by the LC tank circuit. Keep input traces and wires short to minimize resonance.

7.4.2 Output Capacitor (C_{OUT})

The RRP51035 is stable with a 22µF minimum ceramic output capacitor on the VOUT pin.

A larger value output capacitor generally improves the transient response because of significant changes in load current. Still, it can also increase the load transient response time because of the decreased loop bandwidth.

The high-frequency PSRR can be improved to target specific frequencies, such as from a switching regulator if the output capacitor PSRR peak is chosen to equal the switching frequency of the upstream supply noise.

Additional output capacitors can be paralleled with the 22µF to improve PSRR and output noise performance across a wider frequency range.

7.4.3 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The minimum noise-reduction and soft-start bypass capacitor ($C_{NR/SS}$) required for LDO stability on the NR/SS pin is 100nF. This capacitor also helps reduce the low-to-mid frequency output noise and increase the low-to-mid frequency PSRR. Renesas recommends using a 1µF $C_{NR/SS}$ for the best noise and PSRR performance. During the layout of this capacitor, minimize leakage currents around the NR/SS pin, as large leakage currents can cause DC offsets and add additional noise to the LDO output.

Note: A $C_{NR/SS}$ less than 1µF does not give the best possible noise and PSRR performance.

The soft start-up time of the RRP51035 can be estimated with the value of the capacitor $C_{NR/SS}$ along with the output voltage (V_{OUT}) using Equation 9, where T_{SS} is in µs, V_{OUT} is in V, and $C_{NR/SS}$ is in µF.

(EQ. 9)
$$T_{SS} = 140 \times V_{OUT} \times C_{NR/SS} + 34 + 3 \times \frac{V_{OUT} - 1.1}{C_{NR/SS}}$$

The soft start-up time of the RRP51035 is defined as the time it takes for the output voltage to rise from 10% to 90% of its final value as soon as the V_{EN} crosses its threshold.

Table 4 shows the measured start-up time. A difference between the estimated and measured start-up time may exist, which is mainly caused by the current charging $C_{NR/SS}$ changes when the V_{OUT} changes.

Table 4. Measured Start-Up Time Based on V_{OUT} and $C_{NR/SS}$

$C_{NR/SS}$ Option	Measured Start-Up Time (µs)			
	0.5V	**0.9V**	**1.8V**	**3.3V**
0.1µF	18	36	66	195
1µF	152	264	428	550

Some ceramic capacitors experience a piezoelectric response that causes the capacitor to generate noise when exposed to mechanical stress or thermal transients. In the LDO, this appears as increased low-frequency noise on the output. The cause of this is the dielectric material used in the capacitor. Most high-dielectric type capacitors like X5R and X7R have a significant piezoelectric response. Low-dielectric ceramic capacitors such as NP0 or C0G do not have piezoelectric properties and are recommended to solve piezoelectric problems. The drawback of NP0 or C0G capacitors is that they are expensive and large if commercially available.

7.4.4 Bias Capacitor (C_{BIAS})

The minimum BIAS bypass capacitor required when using BIAS for low input voltage applications (<1.4V) is 10µF.

7.5 Power Dissipation and Thermals

In applications with high ambient temperatures, large headroom voltages, and large load currents, the heat dissipated inside the package can become large enough to cause the junction temperature to exceed the maximum recommended operating temperature of +125C. The die junction temperature of the RRP51035 must not exceed +125°C to ensure reliable operation. Therefore, getting a rough estimate of the expected LDO thermal performance in a system PCB is critical. To do this properly, a designer must determine the maximum expected power dissipation, the operating ambient temperature, and the PCB+package thermal resistance.

7.5.1 Power Dissipation

Use Equation 10 to calculate the power dissipation (PD).

(EQ. 10) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

Because the power dissipation contribution from the quiescent (or ground) current (I_Q) is typically very small compared to the current the LDO needs to supply to the load, Equation 10 can be simplified to Equation 11

(EQ. 11) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, the headroom voltage (V_{IN}-V_{OUT}) and the output current determine the power dissipated inside the die.

7.5.2 The Junction Temperature (T_J) and Thermal Resistance (θ_{JA})

The Junction temperature is the sum of the environmental temperature and the junction temperature rise due to power dissipation. The junction temperature is typically calculated with Equation 12 if the ambient temperature, power dissipation, and junction-to-ambient thermal resistance of the PCB+LDO (θ_{JA}).

(EQ. 12) $$T_J = T_A + \theta_{JA} \times P_D$$

The θ_{JA} is the resistance to heat flow between the junction and the outside environment and largely depends on the device package and the PCB design. The θ_{JA} includes the junction-to-EPAD thermal resistance and junction-to-package top thermal resistance. Both are determined by the package features, dimensions, areas, thicknesses, and materials and are therefore fixed. The remaining θ_{JA} largely depends on the total PCB copper area, copper weight, location of thermal planes, PCB layout, and location of the LDO on the PCB, amongst other things. Therefore, to compare the θ_{JA} of different products, it is important to ensure the products were tested on similar PCBs, which is why the JEDEC standard exists.

7.5.3 Approximating the θ_{JA} using Thermal Shutdown

The thermal shutdown circuitry inside the LDO can determine the θ_{JA} of a PCB design and how the θ_{JA} of the lab evaluation PCBs were determined. The test requires the PCB to be exposed to temperatures near +165°C and, therefore, is not a valid test method for everyone.

The following is needed to run the test:

- A way to power the LDO, which could be the system PCB itself or a power supply that powers the LDO only.

- A light load that dissipates ~500mW across the LDO pass transistor. Use an electronic load or a resistor load.
- A way to heat the entire PCB in a controlled way until the LDO thermal shutdown circuitry is triggered, such as a lab oven.
- A way to monitor and/or trigger on the LDO VOUT to capture when the thermal shutdown circuitry has triggered, as an oscilloscope trigger, multimeter.
- A way to measure the temperature of the PCB, such as a thermocouple.

Complete the following steps if using an oscilloscope:

1. Power up the LDO in the oven at room temperature.
2. Set the oscilloscope to measure VOUT. Verify that the voltage makes sense before starting the test.
3. Set the oscilloscope to trigger at about ½ of the programmed output voltage. Set the oscilloscope to trigger on the FALLING edge of the trigger voltage.
4. Take the oven temperature to +125°C and let the PCB soak at that for 3-5 minutes
5. Increment the oven by +1C and soak for 15-30 seconds.
6. Stop when the voltmeter reads roughly 0V and record the ambient temperature ($T_{AMBIENT}$) from the temperature sensor.
7. Calculate the θ_{JA} using Equation 13 where $T_{AMBIENT}$ is the oven temperature which caused the LDO to thermally shutdown recorded in step 6, $T_{SHUTDOWN}$ is the thermal shutdown RISING threshold which can be found in the electrical specifications table (+165°C), and PD is the ~500mW power dissipated by the LDO.

(EQ. 13) $$\theta_{JA} = \frac{T_{SHUTDOWN} - T_{AMBIENT}}{P_D}$$

Complete the following steps if using a multimeter:

1. Power up the LDO in the oven at room temperature.
2. Set the multimeter to measure VOUT. Verify that the voltage makes sense before starting the test.
3. Take the oven temperature to +125°C and let the PCB soak at that for 3-5 minutes.
4. Increment the oven by +1C and soak for 15-30 seconds.
5. Stop when the oscilloscope triggers and record the ambient temperature ($T_{AMBIENT}$) from the temperature sensor.
6. Calculate the θ_{JA} using Equation 13 where $T_{AMBIENT}$ is the oven temperature which caused the LDO to thermally shutdown recorded in step 5, and $T_{SHUTDOWN}$ is the thermal shutdown RISING threshold which can be found in the electrical specifications table (+165°C), and PD is the ~500mW power dissipated by the LDO.

7.5.4 Psi (Ψ) Thermal Estimation

When the board temperature (T_B) is known use the Ψ metrics to estimate the junction temperature rise. These metrics are supposed to be independent of copper area. The typical Ψ_{JB} for the 20-Ld 3.5mm x 3.5mm QFN package is 16 °C/W.

(EQ. 14) $$T_J = T_B + (P_D \times \psi_{JB})$$

8. Layout Guidelines

The following are recommendations for the RRP51035 to achieve optimal electrical and thermal performance:

- Place all the required components for the LDO on the same layer as the IC.
- Place a minimum 10µF ceramic input bypass capacitor as close as practical between the VIN pins and GND.

- Place a minimum 22µF ceramic output bypass capacitor as close as practical between the VOUT pins and GND.
- Place a minimum 1µF ceramic bypass capacitor as close as practical between the BIAS pin and GND.
- Place the CNR/SS bypass capacitor as close as practical between the NR/SS pin and GND.
- The feedback trace should be short, direct, and away from other noisy traces.
- Place the feedback resistors as close as possible to the IC.
- The package thermal EPAD is the largest heat conduction path for the LDO package. It should be soldered to a copper pad on the PCB underneath the IC.
- The PCB thermal copper pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner/bottom GND PCB areas.
- Keep the PCB thermal copper pad vias small but not so small that their inside diameter prevents solder from wicking through during reflow.
- It is important to have a complete connection of the plated through-hole to each plane.
- If possible, add thermal vias around the PCB package to help improve heat spread from areas around the IC to other layers of the board.
- The top copper GND layer that the EPAD is connected to is the least thermally resistant path for heat flow. Therefore, minimize the components and traces that cut this layer.

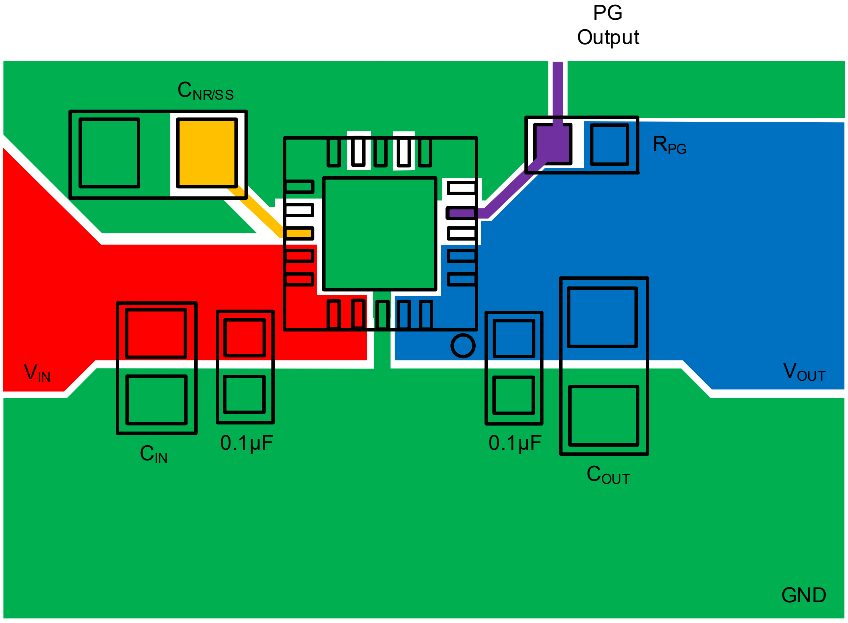
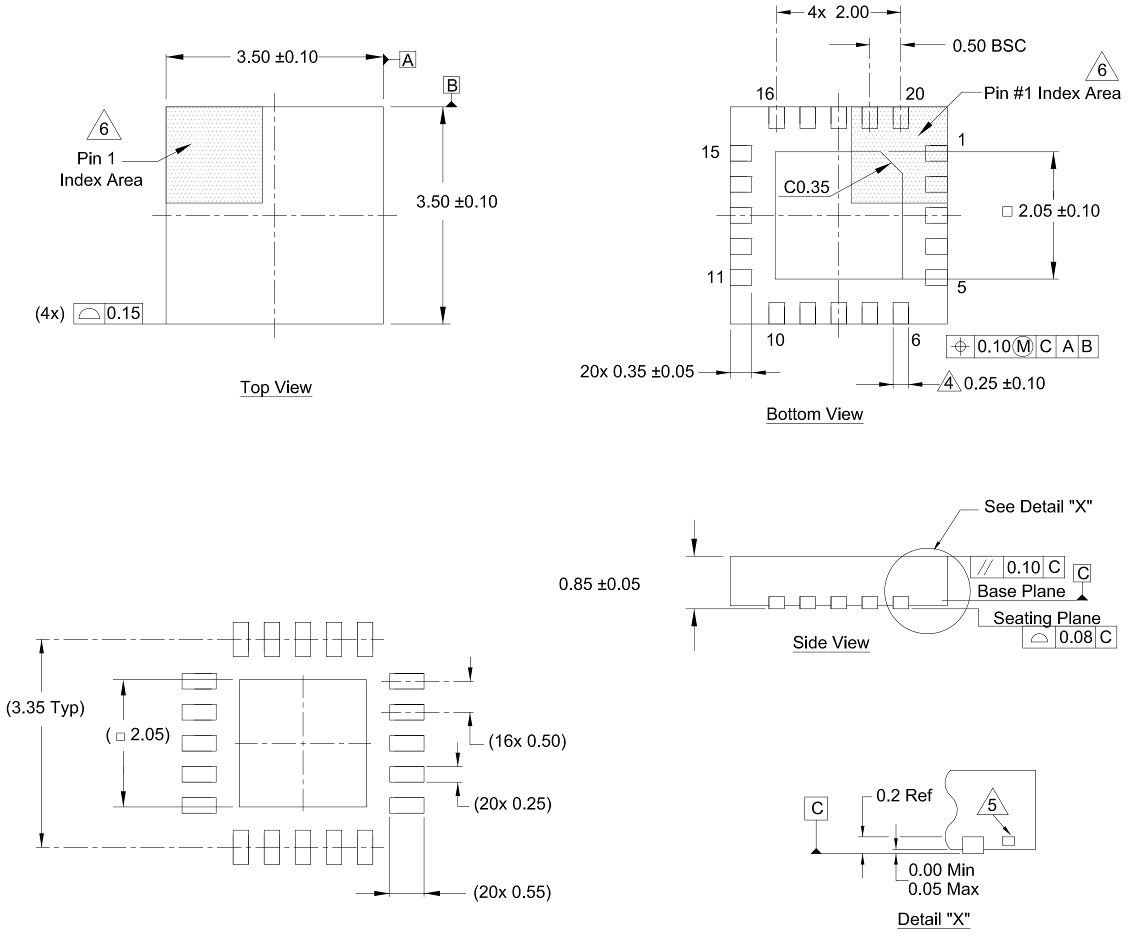


Figure 55. Layout Example

9. Package Outline Drawing

For the most recent package outline drawing, see L20.3.5x3.5.

L20.3.5x3.5
20 Lead Quad Flat No-Lead Package (QFN)
Rev 0, 10/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier is either a mold or mark feature.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Junction Temperature Range
RRP51035-Q10	RRP51 035	20-QFN, 3.5×3.5 mm	L20.3.5x3.5	Reel, 3k	-40 to +125°C
RRP51035-Q20				Reel, 6k	

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RRP51035 product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

11. Revision History

Revision	Date	Description
1.00	Sep 4, 2024	Initial release.

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