Datasheet

RX260 Group, RX261 Group

Renesas MCUs

R01DS0430EJ0100
Rev.1.00
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64-MHz, 32-bit RX MCUs, on-chip FPU, 355 Coremark, up to 512-KB flash memory, up to 36 pins capacitive touch sensing unit, up to 11 comms channels, 12-bit A/D, D/A, RTC, IEC60730 compliance, 1.6-V to 5.5-V single supply, Encryption functions (optional)

Features

PLQP0100KB-B 14 × 14mm, 0.5mm pitch
PLQP0080KB-B 12 × 12mm, 0.5mm pitch
PLQP0064KB-C 10 × 10mm, 0.5mm pitch
PLQP0048KB-B 7 × 7mm, 0.5mm pitch

PWQN0048KC-A 7 × 7mm, 0.5mm pitch

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 64 MHz
  Capable of 355 Coremark in operation at 64 MHz
- Enhanced DSP instructions: 32-bit multiply-accumulate instructions, and 16-bit multiply-subtract instructions are supported.
- On-chip FPU: 32-bit single-precision floating point compliant with IEEE-754
- On-chip divider that operated at the fastest of two clock cycles
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture
- Operation from a single 1.6-V to 5.5-V supply
- Four low power consumption modes
- Low power timer (LPT) that operates during the software standby state
- Supply current
  High-speed operating mode: 84 µA/MHz
  Supply current in software standby mode: 1.01 µA (typ.) (T_a = 25°C)
- Recovery time from software standby mode: 6.3 µs (typ.) (Clock Source: HOCO 64 MHz, T_a = 25°C)

■ On-chip flash memory for code
- 256 K/384 K/512 Kbytes size capacities
- User code is programmable by on-board programming.
- Programmable at 1.6 V
- For instructions and operands

■ On-chip data flash memory
- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states
- 128 Kbytes size capacities

■ Data transfer functions
- DMAC: Incorporates four channels
- DTC: Five transfer modes

■ ELC
- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management
- Eight types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External main clock input frequency: Up to 20 MHz
- External sub clock input frequency: 32.768 kHz
- Main clock oscillator frequency: 1 to 20 MHz
- Sub clock oscillator frequency: 32.768 kHz
- PLL/PLL2 circuit input: 4 MHz to 12.5 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 24/32/48/64 MHz ± 1%
- IWDT-dedicated on-chip oscillator: 15 kHz
- Generate a 32.768 kHz clock for the real-time clock
- On-chip clock frequency accuracy measurement circuit (CAC)

■ Realtime clock
- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable
- Time capture function
- Time capture on event-signal input through external pins

■ Independent watchdog timer
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ MPC
- Input/output functions selectable from multiple pins

■ Up to 11 communication functions
- USB 2.0 full-speed host/function/On-The-Go (OTG) (1 channel), full-speed = 12 Mbps, low-speed = 1.5 Mbps (host only), and isochronous transfer
- CAN FD: Compliant with ISO11898-1:2015, standard frame and extended frame (1 channel)
- SCI with multiple functionalities (up to 4 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- Up to three RSCIs with Manchester encoding and HBS functionality
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps

■ Remote control signal reception

■ Up to 16 extended-function timers
- 32-bit (2 channels) or 16-bit (6 channels) GPTW: operation at 64 MHz, input capture, output compare, PWM waveforms: 10 output channels in single-phase complementary PWM mode/3 output channels in 3-phase complementary PWM mode/2 output channels in 5-phase complementary PWM mode, phase-counting mode, linkage with comparator (counting operation, PWM negate control)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (four channels)

■ 12-bit A/D converter
- Capable of conversion within 0.5 µs
- 24 (external pin input) +1 (internal input) channels
- Sampling time can be set for each channel
- Conversion results compare features
- Self-diagnostic function and analog input disconnection detection assistance function
- Double trigger (data duplication) function for motor control

■ D/A converter
- Two channels

■ Capacitive touch sensing unit
- Self-capacitance method: A single pin configures a single key, supporting up to 36 keys
- Mutual capacitance method: Matrix configuration with 8 × 8, supporting up to 64 keys

■ Comparator B
- Two channels

■ General I/O ports
- 5-V tolerant, open drain, input pull-up

■ Renesas Secure IP (RSIP-E11A) (optional)
- AES128/256, ECC, True-random number generator (TRNG), SHA224, and SHA256

■ Temperature sensor

■ Unique ID
- 32-byte ID code for the MCU

■ Operating temperature range
- –40 to +85°C
- –40 to +105°C

■ Applications
- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 shows the outline of maximum specifications. The peripheral functions and the number of their channels vary depending on the number of pins of the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/6)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 64 MHz • 32-bit RX CPU (RX v3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • 111 instructions Standard provided instructions: 111 Basic instructions: 77 Single precision floating point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision (32-bit) floating-point number • Data types and exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 512 Kbytes, 384 Kbytes, 256 Kbytes • 32 MHz ≤: No-wait cycle access • 32 MHz to 64 MHz: One-wait cycle access • Programming/erasing method: Serial programming (asynchronous serial communication/USB communication), self-programming
	RAM	• Capacity: 128 Kbytes • 64 MHz, no-wait memory access • Parity error detection
	E2 DataFlash	• Capacity: 8 Kbytes • Number of erase/write cycles: 1,000,000 (typ.)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, PLL2 frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 64 MHz (at max.) Peripheral modules of GPTW, and the ECC function control registers in the CANFD module run in synchronization with PCLKA: 64 MHz (at max.) ADCLK in the S12AD runs in synchronization with PCLKD: 64 MHz (at max.) Other peripheral modules run in synchronization with PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 64 MHz (at max.)

Table 1.1 Outline of Specifications (2/6)

Classification	Module/Function	Description
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset
Voltage detection circuit (LVDAb)		When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. • Voltage detection circuit 0 is capable of selecting the detection voltage from 5 levels • Voltage detection circuit 1 is capable of selecting the detection voltage from 16 levels • Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Four low power consumption modes Sleep mode, deep sleep mode, software standby mode, and snooze mode
	Function for lower operating power consumption	Operating power control modes • High-speed operating mode • middle-speed operating mode (default) • middle-speed operating mode 2 • low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 256 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 7 (The NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, IWDT interrupt, and RAM error interrupt) • 16 levels specifiable for the order of priority
DMA	DMA controller (DMACA)	• 4 channels • Transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCb)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions • Sequence transfer
I/O ports	General I/O ports	• I/O ports for the 100-pin LFQFP I/O pins: 89 (RX260 group), 87 (RX261 group) Input pin: 3 Pull-up resistors: 89 (RX260 group), 87 (RX261 group) Open-drain outputs: 63 5-V tolerance: 4 • I/O ports for the 80-pin LFQFP I/O pins: 69 (RX260 group), 67 (RX261 group) Input pin: 3 Pull-up resistors: 69 (RX260 group), 67 (RX261 group) Open-drain outputs: 47 5-V tolerance: 4 • I/O ports for the 64-pin LFQFP I/O pins: 53 (RX260 group), 51 (RX261 group) Input pin: 3 Pull-up resistors: 53 (RX260 group), 51 (RX261 group) Open-drain outputs: 35 5-V tolerance: 2 • I/O ports for the 48-pin LFQFP, 48-pin HWQFN I/O pins: 39 (RX260 group), 37 (RX261 group) Input pin: 1 Pull-up resistors: 39 (RX260 group), 37 (RX261 group) Open-drain outputs: 27 5-V tolerance: 2
Event link controller (ELC)		• Event signals of 116 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for ports B and E
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins

Table 1.1 Outline of Specifications (3/6)

Classification	Module/Function	Description
Timers	General PWM timer (GPTWa)	• (32 bits × 2 channels, 16 bits × 6 channels) × 1 unit • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Capable of synchronous start, stop, or clearing of counter for any channel • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 8 ELC events • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 4 external triggers • Output pin disabling function by a short circuit detection among output pins • Capable of generating conversion start triggers for the A/D converters • Capable of outputting events, such as compare-match from A to F and overflow/ underflow, to ELC • Capable of using noise filter of input capture
	Port output enable for GPTW (POEGc)	• Controlling the output disable for GPTW waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPTW • Initiation by detection of comparator interrupt request • Initiation by detection of oscillation stop or by software
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCBa)	• Clock source: Sub-clock • Clock and calendar functions • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt • Time capture function (up to 3 pins)
	Low power timer (LPTa)	• 16 bits × 1 channel • Clock source: Sub-clock, LOCO clock divided by 4, or dedicated low-speed clock for the IWDT selectable • Clock division ratio: Frequency divided by 1, 2, 4, 8, 16, or 32 selectable • PWM output mode
	8-bit timer (TMRa)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer

Table 1.1 Outline of Specifications (4/6)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (SCIk, SCIh)	• 4 channels SCIk: SCI1, SCI5, SCI6 SCIh: SCI12 • SCIk, SCIh Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 7, 8, 9-bit transfer mode Bit rate modulation Double-speed mode Data match detection (SCI12 is not supported) Event linking by the ELC (supported by SCI5 only) • SCIk Only Data match detection Adjustment of the timing of sampling of the RXD signals • SCIh Only Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format

Table 1.1 Outline of Specifications (5/6)

Classification	Module/Function	Description
Communication functions	Serial communications interfaces (RSCI)	• 3 channels (RSCI0, RSCI8, RSCI9) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Start-bit detection: Level or edge detection is selectable. • Simple I^2C • Simple SPI • 9-bit transfer mode • Bit rate modulation • Double-speed mode • Supports the serial communications protocol, which contains the start frame and information frame • Supports the LIN format (RSCI9) • Data can be transmitted or received in sequence by the 32-byte FIFO buffers of the transmission and reception unit • Manchester encoding is supported (RSCI9). • RSCI has some home bus system (HBS) functionality. • Data match detection • Adjustment of the timing of sampling of the RXD signals
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	Serial peripheral interface (RSPIc)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Transit/receive data can be swapped in byte units • Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception.
	CANFD module (CANFD)	• 1 channel • Compliance with the ISO11898-1:2015 specification (standard frame and extended frame)
	USB 2.0 FS host/ function module (USBe)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-powered mode and bus-powered mode are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	Remote control signal receiver (REMCa)	• 1 channel • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLKB, sub-clock, IWDTCLK, and TMR.

Table 1.1 Outline of Specifications (6/6)

Classification	Module/Function	Description
12-bit A/D converter (S12ADE)		• 12 bits (25 channels × 1 unit*1) • 12-bit resolution • Minimum conversion time: 0.50 µs per channel when the ADCLK is operating at 64 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (GPTW), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DAa)		• 2 channels • 8-bit resolution • Output voltage: 0V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSU2SLa)		• Self-capacitance method: A single pin configures a single key, supporting up to 36 keys • Mutual capacitance method: Matrix configuration with 8 × 8, supporting up to 64 keys • Automatic correction • Automatic judgment
Encryption function	Unique ID	32-byte ID code for the MCU
	Renesas Secure IP (RSIP-E11A)	• Symmetric-key cryptography: AES • Public-key cryptography: ECC • Hash functions: SHA224, SHA256 • True-random number generator
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.6 to 1.8 V: 4 MHz, VCC = 1.8 to 2.4 V: 48 MHz, VCC = 2.4 to 5.5 V: 64 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KC-A) 7 × 7 mm, 0.5 mm pitch
Debugging interfaces		FINE interface

Note 1. 25 channel pins consist of 24 external input pins, and an internal input pin for the CTSU.

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX260 Group				RX261 Group			
		100 Pins	**80 Pins**	**64 Pins**	**48 Pins**	**100 Pins**	**80 Pins**	**64 Pins**	**48 Pins**
Interrupts	External interrupts	NMI, IRQ0 to IRQ7		NMI, IRQ0 to IRQ2, IRQ4 to IRQ7		NMI, IRQ0 to IRQ7		NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	
DMA	DMA controller	4 channels (DMAC0 to DMAC3)				4 channels (DMAC0 to DMAC3)			
	Data transfer controller	Available				Available			
Timers	General PWM timer	8 channels				8 channels			
	Port output enable for GPTW	Available				Available			
	8-bit timer	2 channels × 2 units				2 channels × 2 units			
	Compare match timer	2 channels × 2 units				2 channels × 2 units			
	Low power timer	1 channel				1 channel			
	Realtime clock	Available			Not available	Available			Not available
	Watchdog timer	Available				Available			
	Independent watchdog timer	Available				Available			
Communication functions	Serial communications interfaces (SCIk)	Ch. 1, 5, and 6				Ch. 1, 5, and 6			
	Serial communications interfaces (SCIh)	Ch. 12				Ch. 12			
	Serial communications interfaces (RSCI)	Ch. 0, 8, and 9			Ch. 0 and 8	Ch. 0, 8, and 9			Ch. 0 and 8
	I^2C bus interface	1 channel				1 channel			
	Serial peripheral interface	1 channel				1 channel			
	CANFD module (CANFD)	Not available				1 channel			
	USB 2.0 FS host/ function module	Not available				1 channel			
	Remote control signal receiver (REMC)	1 channel				1 channel			
Capacitive touch sensing unit		36 channels		32 channels	24 channels	34 channels		30 channels	22 channels
12-bit A/D converter		25 channels	18 channels	15 channels	11 channels	25 channels	18 channels	15 channels	11 channels
Temperature sensor		Available				Available			
D/A converter		2 channels			Not available	2 channels			Not available
CRC calculator		Available				Available			
Event link controller		Available				Available			
Comparator B		2 channels				2 channels			
Renesas Secure IP (RSIP-E11A)		Not available				Available/Not available			
Packages		100-pin LFQFP	80-pin LFQFP	64-pin LFQFP	48-pin LFQFP 48-pin HWQFN	100-pin LFQFP	80-pin LFQFP	64-pin LFQFP	48-pin LFQFP 48-pin HWQFN

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/3)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Encryption Module	CANFD	USB	Operating Temperature
RX261 (D-version)	R5F52618ADFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	8 Kbytes	64 MHz	Not available	Available*1	Available	–40 to +85°C
	R5F52618BDFP	PLQP0100KB-B					Available	Available	Available	
	R5F52618ADFN	PLQP0080KB-B					Not available	Available*1	Available	
	R5F52618BDFN	PLQP0080KB-B					Available	Available	Available	
	R5F52618ADFM	PLQP0064KB-C					Not available	Available*1	Available	
	R5F52618BDFM	PLQP0064KB-C					Available	Available	Available	
	R5F52618ADFL	PLQP0048KB-B					Not available	Available*1	Available	
	R5F52618BDFL	PLQP0048KB-B					Available	Available	Available	
	R5F52618ADNE	PWQN0048KC-A					Not available	Available*1	Available	
	R5F52618BDNE	PWQN0048KC-A					Available	Available	Available	
	R5F52617ADFP	PLQP0100KB-B	384 Kbytes				Not available	Available*1	Available	
	R5F52617BDFP	PLQP0100KB-B					Available	Available	Available	
	R5F52617ADFN	PLQP0080KB-B					Not available	Available*1	Available	
	R5F52617BDFN	PLQP0080KB-B					Available	Available	Available	
	R5F52617ADFM	PLQP0064KB-C					Not available	Available*1	Available	
	R5F52617BDFM	PLQP0064KB-C					Available	Available	Available	
	R5F52617ADFL	PLQP0048KB-B					Not available	Available*1	Available	
	R5F52617BDFL	PLQP0048KB-B					Available	Available	Available	
	R5F52617ADNE	PWQN0048KC-A					Not available	Available*1	Available	
	R5F52617BDNE	PWQN0048KC-A					Available	Available	Available	
	R5F52616ADFP	PLQP0100KB-B	256 Kbytes				Not available	Available*1	Available	
	R5F52616BDFP	PLQP0100KB-B					Available	Available	Available	
	R5F52616ADFN	PLQP0080KB-B					Not available	Available*1	Available	
	R5F52616BDFN	PLQP0080KB-B					Available	Available	Available	
	R5F52616ADFM	PLQP0064KB-C					Not available	Available*1	Available	
	R5F52616BDFM	PLQP0064KB-C					Available	Available	Available	
	R5F52616ADFL	PLQP0048KB-B					Not available	Available*1	Available	
	R5F52616BDFL	PLQP0048KB-B					Available	Available	Available	
	R5F52616ADNE	PWQN0048KC-A					Not available	Available*1	Available	
	R5F52616BDNE	PWQN0048KC-A					Available	Available	Available	

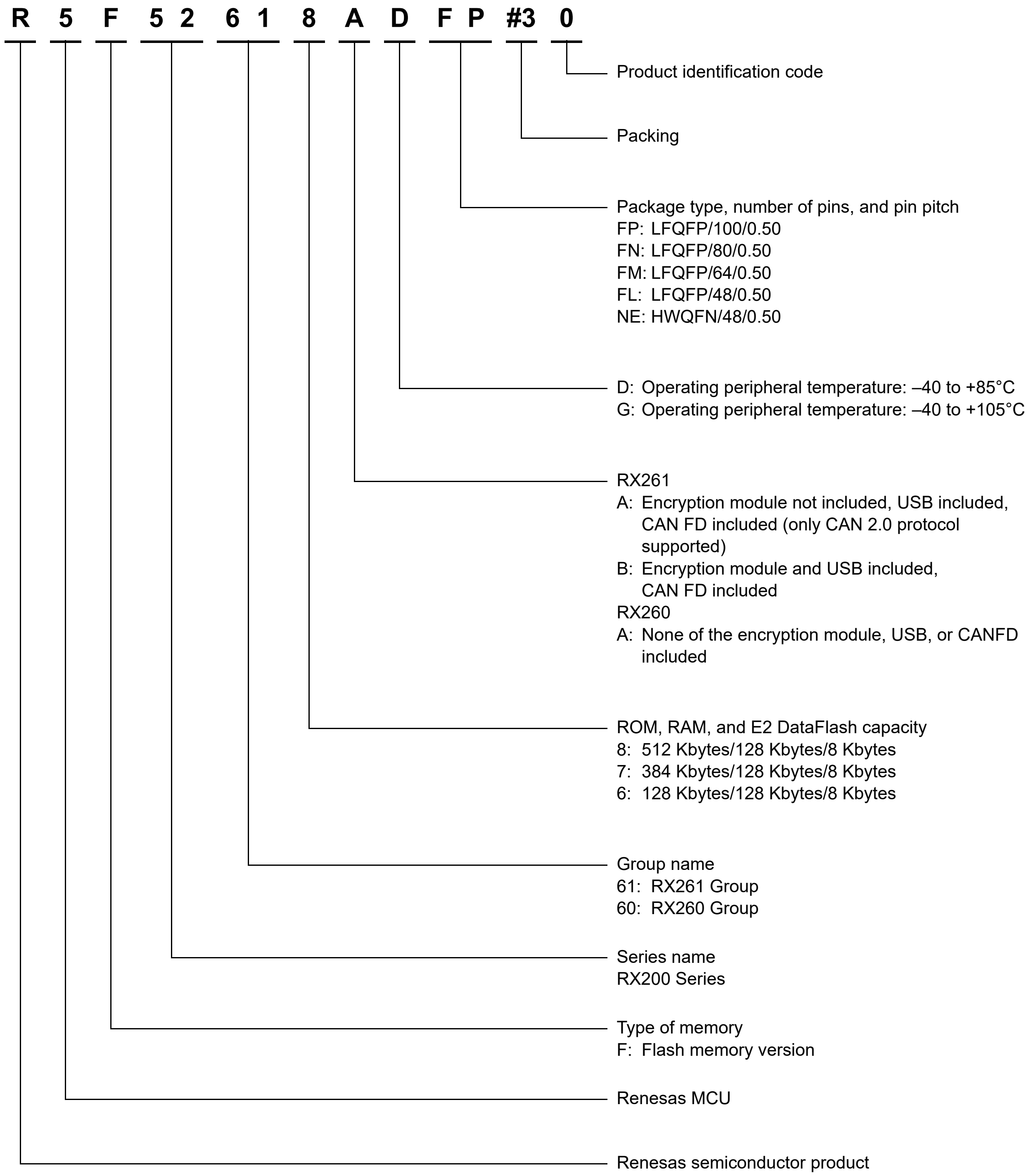
Table 1.3 List of Products (2/3)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Encryption Module	CANFD	USB	Operating Temperature
RX261 (G-version)	R5F52618AGFP	PLQP0100KB-B	512 Kbytes	128 Kbytes	8 Kbytes	64 MHz	Not available	Available*1	Available	–40 to +105°C
	R5F52618BGFP	PLQP0100KB-B					Available	Available	Available	
	R5F52618AGFN	PLQP0080KB-B					Not available	Available*1	Available	
	R5F52618BGFN	PLQP0080KB-B					Available	Available	Available	
	R5F52618AGFM	PLQP0064KB-C					Not available	Available*1	Available	
	R5F52618BGFM	PLQP0064KB-C					Available	Available	Available	
	R5F52618AGFL	PLQP0048KB-B					Not available	Available*1	Available	
	R5F52618BGFL	PLQP0048KB-B					Available	Available	Available	
	R5F52618AGNE	PWQN0048KC-A					Not available	Available*1	Available	
	R5F52618BGNE	PWQN0048KC-A					Available	Available	Available	
	R5F52617AGFP	PLQP0100KB-B	384 Kbytes				Not available	Available*1	Available	
	R5F52617BGFP	PLQP0100KB-B					Available	Available	Available	
	R5F52617AGFN	PLQP0080KB-B					Not available	Available*1	Available	
	R5F52617BGFN	PLQP0080KB-B					Available	Available	Available	
	R5F52617AGFM	PLQP0064KB-C					Not available	Available*1	Available	
	R5F52617BGFM	PLQP0064KB-C					Available	Available	Available	
	R5F52617AGFL	PLQP0048KB-B					Not available	Available*1	Available	
	R5F52617BGFL	PLQP0048KB-B					Available	Available	Available	
	R5F52617AGNE	PWQN0048KC-A					Not available	Available*1	Available	
	R5F52617BGNE	PWQN0048KC-A					Available	Available	Available	
	R5F52616AGFP	PLQP0100KB-B	256 Kbytes				Not available	Available*1	Available	
	R5F52616BGFP	PLQP0100KB-B					Available	Available	Available	
	R5F52616AGFN	PLQP0080KB-B					Not available	Available*1	Available	
	R5F52616BGFN	PLQP0080KB-B					Available	Available	Available	
	R5F52616AGFM	PLQP0064KB-C					Not available	Available*1	Available	
	R5F52616BGFM	PLQP0064KB-C					Available	Available	Available	
	R5F52616AGFL	PLQP0048KB-B					Not available	Available*1	Available	
	R5F52616BGFL	PLQP0048KB-B					Available	Available	Available	
	R5F52616AGNE	PWQN0048KC-A					Not available	Available*1	Available	
	R5F52616BGNE	PWQN0048KC-A					Available	Available	Available	

Table 1.3 List of Products (3/3)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Encryption Module	CANFD	USB	Operating Temperature
RX260 (D-version)	R5F52608ADFP	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52608ADFN	PLQP0080KB-B					Not available	Not available	Not available	
	R5F52608ADFM	PLQP0064KB-C	512 Kbytes				Not available	Not available	Not available	
	R5F52608ADFL	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52608ADNE	PWQN0048KC-A					Not available	Not available	Not available	
	R5F52607ADFP	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52607ADFN	PLQP0080KB-B					Not available	Not available	Not available	
	R5F52607ADFM	PLQP0064KB-C	384 Kbytes	128 Kbytes	8 Kbytes	64 MHz	Not available	Not available	Not available	–40 to +85°C
	R5F52607ADFL	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52607ADNE	PWQN0048KC-A					Not available	Not available	Not available	
	R5F52606ADFP	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52606ADFN	PLQP0080KB-B					Not available	Not available	Not available	
	R5F52606ADFM	PLQP0064KB-C	256 Kbytes				Not available	Not available	Not available	
	R5F52606ADFL	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52606ADNE	PWQN0048KC-A					Not available	Not available	Not available	
RX260 (G-version)	R5F52608AGFP	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52608AGFN	PLQP0080KB-B					Not available	Not available	Not available	
	R5F52608AGFM	PLQP0064KB-C	512 Kbytes				Not available	Not available	Not available	
	R5F52608AGFL	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52608AGNE	PWQN0048KC-A					Not available	Not available	Not available	
	R5F52607AGFP	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52607AGFN	PLQP0080KB-B					Not available	Not available	Not available	
	R5F52607AGFM	PLQP0064KB-C	384 Kbytes	128 Kbytes	8 Kbytes	64 MHz	Not available	Not available	Not available	–40 to +105°C
	R5F52607AGFL	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52607AGNE	PWQN0048KC-A					Not available	Not available	Not available	
	R5F52606AGFP	PLQP0100KB-B					Not available	Not available	Not available	
	R5F52606AGFN	PLQP0080KB-B					Not available	Not available	Not available	
	R5F52606AGFM	PLQP0064KB-C	256 Kbytes				Not available	Not available	Not available	
	R5F52606AGFL	PLQP0048KB-B					Not available	Not available	Not available	
	R5F52606AGNE	PWQN0048KC-A					Not available	Not available	Not available	

Note 1. Products with this part number support only CAN 2.0 protocol.

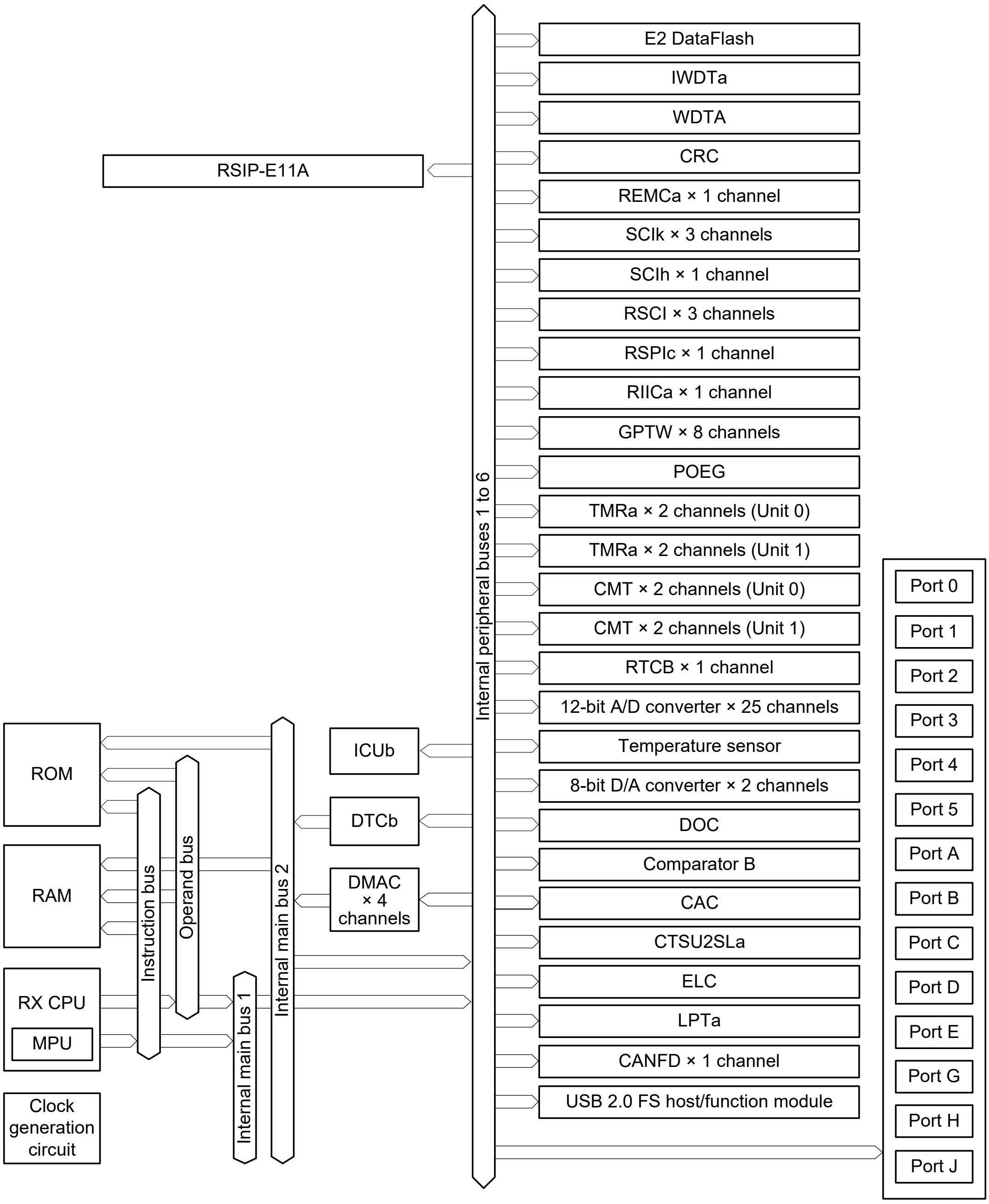


Note: Visit the Renesas Electronics Web site to check and obtain the ordering part numbers.

Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCb: Data transfer controller
DMAC: DMA controller
WDT: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIk, SCIh: Serial communications interface
RSCI: Serial communications interface
RSPI: Serial peripheral interface
RIICa: I^{2}C bus interface
REMCa: Remote control signal receiver
CANFD: CANFD module
GPTW: General PWM timer
POEG: Port output enable for GPTW
CMT: Compare match timer
RTCB: Realtime clock
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit
CTSU2SLa: Capacitive touch sensing unit
TMRa: 8-bit timer
LPTa: Low power timer
RSIP-E11A: Renesas Secure IP

Note: Available functions depend on the product.

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to the VSS pin via the 4.7 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	EXCIN	Input	External clock input pin for the sub-clock oscillator
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	This pin is used in boot mode (USB interface).
	UPSEL	Input	This pin is used in boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
Voltage detection circuit	CMPA2	Input	Detection target voltage pin for voltage detection 2.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit
On-chip emulator	FINED	I/O	FINE interface pin
Interrupts	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Interrupt request pins
General PWM timer	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC7A, GTIOC0B to GTIOC7B	I/O	Input capture input/output compare output/PWM output pins
	GTIOC0A# to GTIOC7A#, GTIOC0B# to GTIOC7B#	I/O	Input capture inverted input/output compare inverted output/PWM inverted output pins
	GTCPPO0	Output	Synchronized PWM output
	GTIU, GTIV, GTIW	Input	Hall sensor input pins
	GTOUUP	Output	A three-phase PWM output for controlling a brushless DC motor (positive U-phase)
	GTOULO	Output	A three-phase PWM output for controlling a brushless DC motor (negative U-phase)
	GTOVUP	Output	A three-phase PWM output for controlling a brushless DC motor (positive V-phase)
	GTOVLO	Output	A three-phase PWM output for controlling a brushless DC motor (negative V-phase)
	GTOWUP	Output	A three-phase PWM output for controlling a brushless DC motor (positive W-phase)
	GTOWLO	Output	A three-phase PWM output for controlling a brushless DC motor (negative W-phase)
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins

Table 1.4 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter
	TMRI0 to TMRI3	Input	Counter reset input pins
Low power timer	LPTO	Output	PWM output pin
Serial communications interface (SCIk)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock
	RXD1, RXD5, RXD6	Input	Input pins for received data
	TXD1, TXD5, TXD6	Output	Output pins for transmitted data
	CTS1#, CTS5#, CTS6#	Input	Input pins for controlling the start of transmission and reception
	RTS1#, RTS5#, RTS6#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6	I/O	Input/output pins for the I^2C clock
	SSDA1, SSDA5, SSDA6	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock
	SMISO1, SMISO5, SMISO6	I/O	Input/output pins for slave transmit data
	SMOSI1, SMOSI5, SMOSI6	I/O	Input/output pins for master transmit data
	SS1#, SS5#, SS6#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for receiving data
	TXD12	Output	Output pin for transmitting data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmit data
	SMOSI12	I/O	Input/output pin for master transmit data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data

Table 1.4 Pin Functions (3/4)

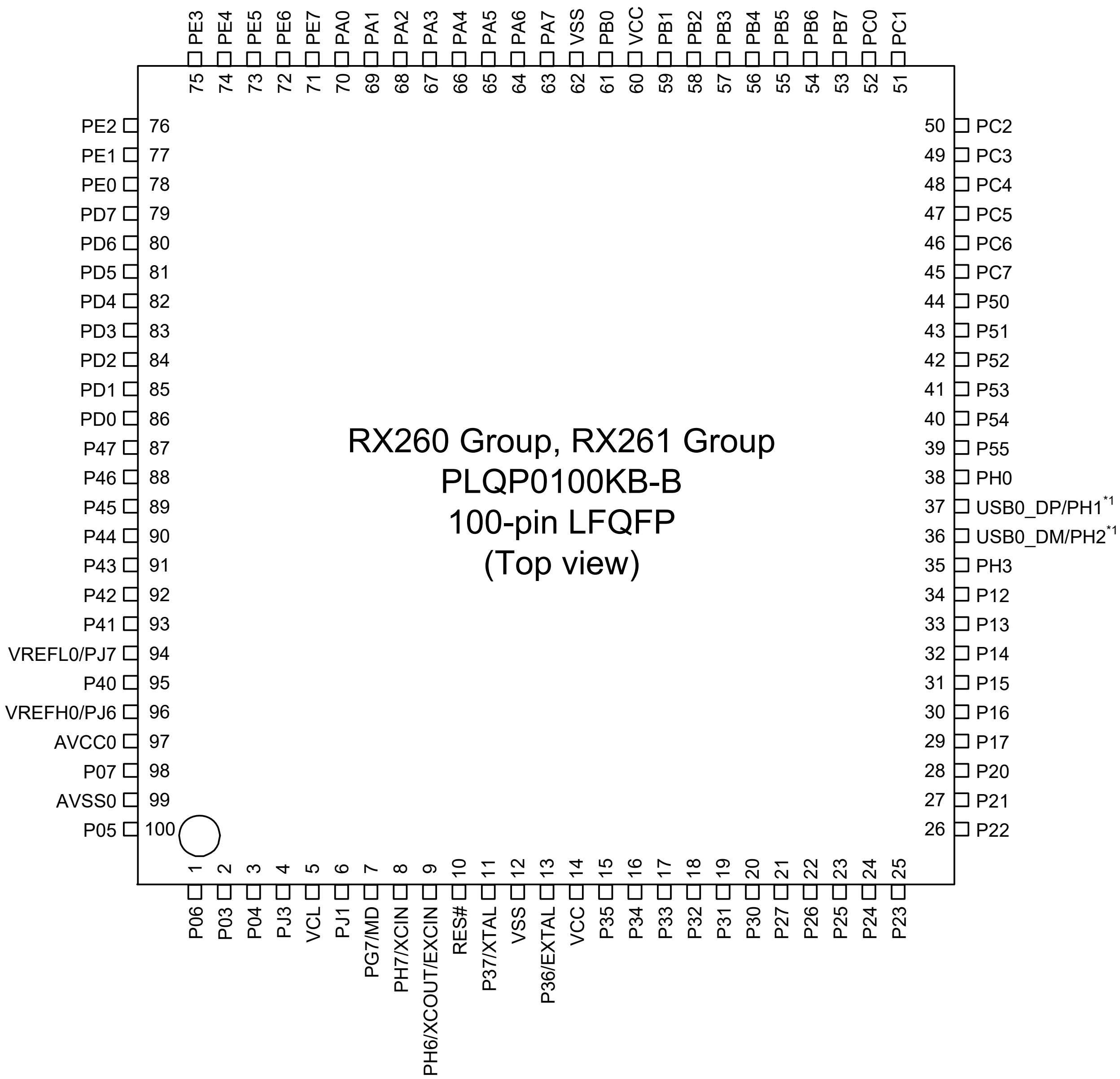
Classifications	Pin Name	I/O	Description
Serial communications interface (RSCI)	• Asynchronous mode/clock synchronous mode		
	SCK000, SCK008, SCK009	I/O	Input/output pins for the clock
	RXD000, RXD008, RXD009	Input	Input pins for received data
	TXD000, TXD008, TXD009	Output	Output pins for transmitted data
	CTS000#, CTS008#, CTS009#	Input	Input pins for controlling the start of transmission and reception
	RTS000#, RTS008#, RTS009#	Output	Output pins for controlling the start of transmission and reception
	DE000, DE008, DE009	Output	DriveEnable output pins
	• Simple I²C mode		
	SSCL000, SSCL008, SSCL009	I/O	Input/output pins for the I²C clock
	SSDA000, SSDA008, SSDA009	I/O	Input/output pins for the I²C data
Serial communications interface (RSCI)	• Simple SPI mode		
	SCK000, SCK008, SCK009	I/O	Input/output pins for the clock
	SMISO000, SMISO008, SMISO009	I/O	Input/output pins for slave transmission of data
	SMOSI000, SMOSI008, SMOSI009	I/O	Input/output pins for master transmission of data
	SS000#, SS008#, SS009#	Input	Chip-select input pins
	• HBS support mode		
	RXD000, RXD008, RXD009	Input	Input pins for received data
	TXDA000, TXDA008, TXDA009	Output	Output pins for transmitted data
	TXDB000, TXDB008, TXDB009	Output	Output pins for transmitted data
Remote control signal receiver (REMC)	PMC0	Input	Input pin for external pulse signal
I²C bus interface	SCL0	I/O	Input/output pin for I²C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I²C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave
	SSLA0	I/O	Input/output pin to select the slave for the RSPI
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI
USB 2.0 FS host/function module	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver
	USB0_VBUS	Input	USB cable connection monitor pin
	USB0_EXICEN	Output	Low-power control signal for the OTG chip
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode
CANFD module	CRX0	Input	Pin for receiving data
	CTX0	Output	Pin for transmitting data

Table 1.4 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion
8-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter
Comparator B	CMPB0, CMPB1	Input	Input pins for the analog signal to be processed by comparator B
	CVREFB0, CVREFB1	Input	Analog reference voltage supply pins for comparator B
	CMPOB0, CMPOB1	Output	Output pins for comparator B
Capacitive touch sensing unit (CTSU)	TS0 to TS35	I/O	Electrostatic capacitance measurement pins (touch pins)
	TSCAP	—	Connect to the VSS via a decoupling capacitor (0.01 μF) for stabilizing the internal voltage
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
I/O ports	P03 to P07	I/O	5-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PG7	I/O	1-bit input/output pin.
	PH0 to PH3, PH6, PH7	I/O	6-bit input/output pins (PH6, PH7: input pins).
	PJ1, PJ3, PJ6, PJ7	I/O	4-bit input/output pins.

1.5 Pin Assignments

1.5.1 100-Pin LFQFP

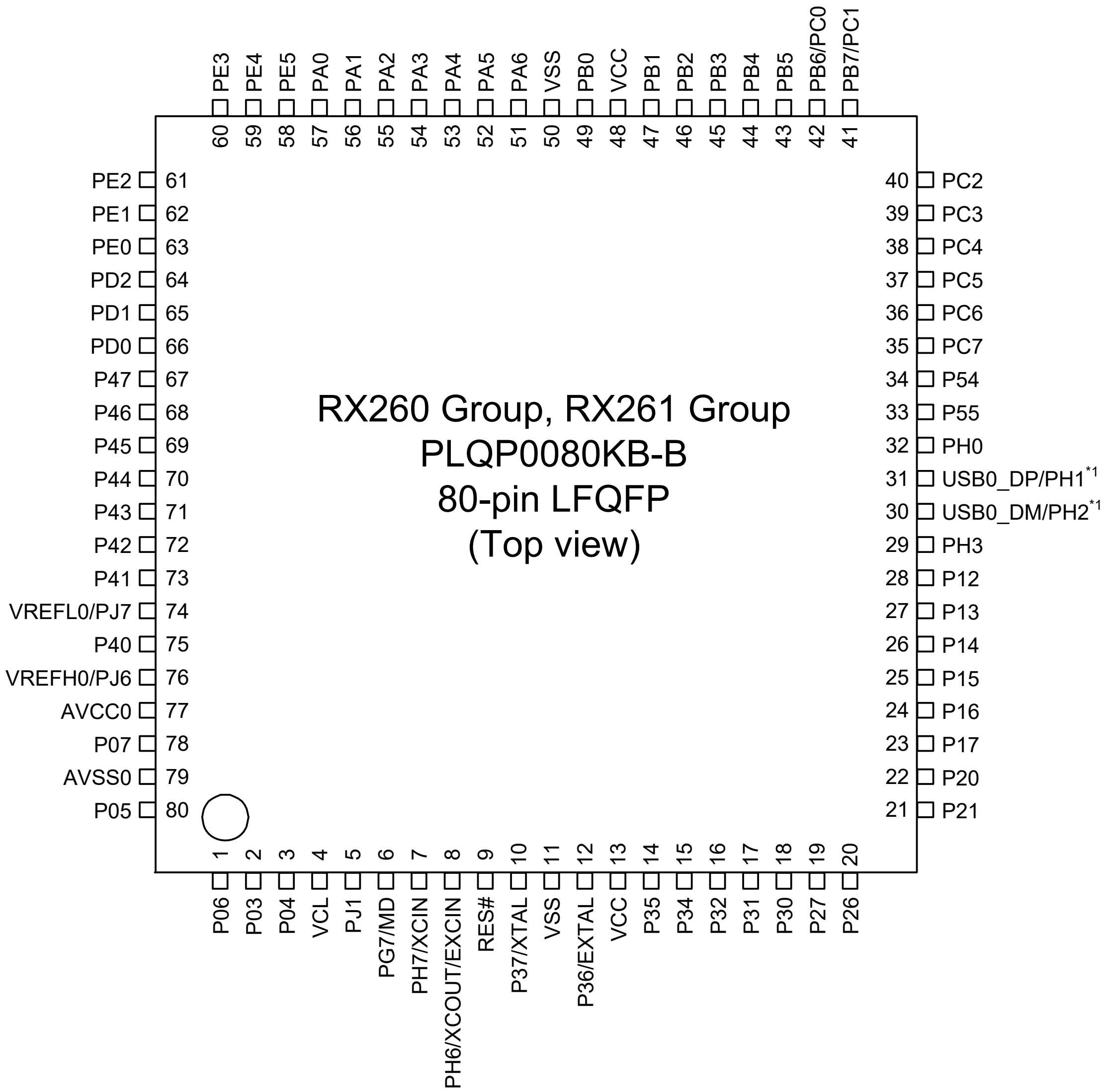


Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (100-Pin LFQFP).

Note 1. These pins function as PH1 and PH2 in the RX260, or as USB0_DP and USB0_DM in the RX261.

Figure 1.3 Pin Assignments (100-Pin LFQFP)

1.5.2 80-Pin LFQFP

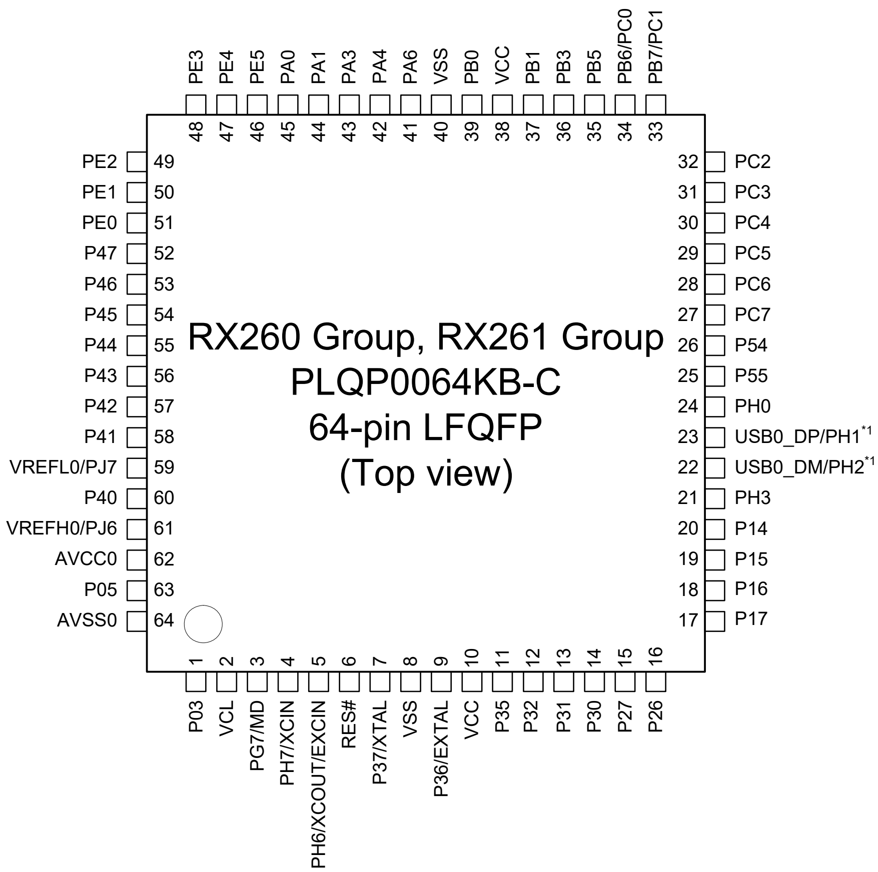


Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (80-Pin LFQFP).

Note 1. These pins function as PH1 and PH2 in the RX260, or as USB0_DP and USB0_DM in the RX261.

Figure 1.4 Pin Assignments (80-Pin LFQFP)

1.5.3 64-Pin LFQFP

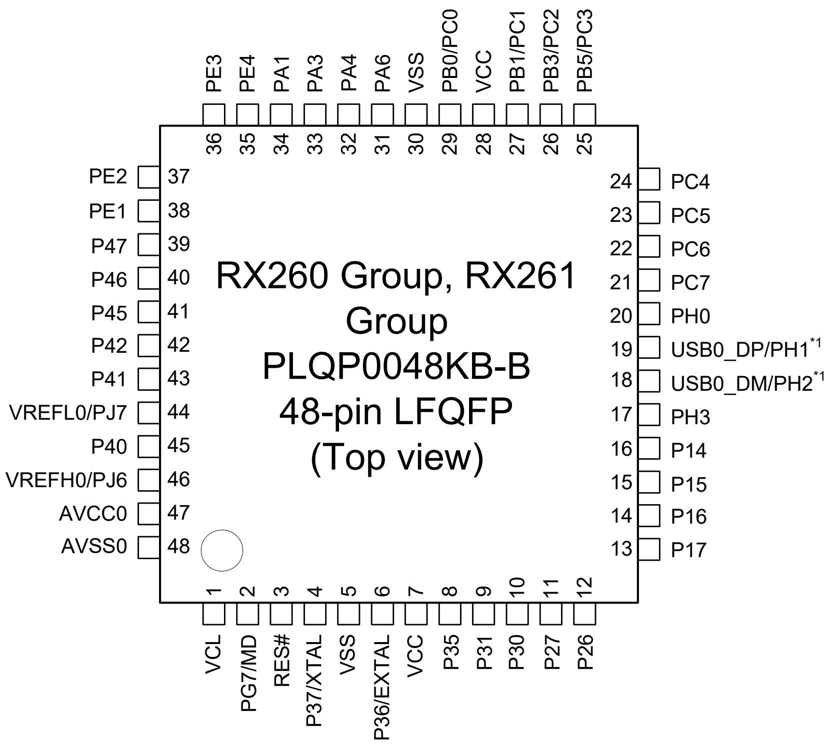


Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (64-Pin LFQFP).

Note 1. These pins function as PH1 and PH2 in the RX260, or as USB0_DP and USB0_DM in the RX261.

Figure 1.5 Pin Assignments (64-Pin LFQFP)

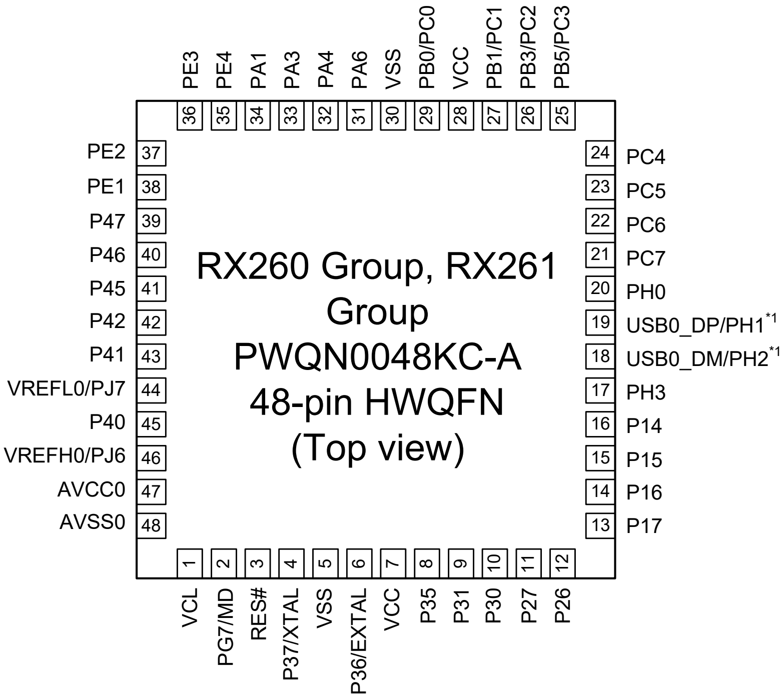
1.5.4 48-Pin LFQFP, 48-Pin HWQFN



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN).

Note 1. These pins function as PH1 and PH2 in the RX260, or as USB0_DP and USB0_DM in the RX261.

Figure 1.6 Pin Assignments (48-Pin LFQFP)



Note: We recommend connecting the exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN).
Note 1. These pins function as PH1 and PH2 in the RX260, or as USB0_DP and USB0_DM in the RX261.

Figure 1.7 Pin Assignments (48-Pin HWQFN)

1.6 List of Pins and Pin Functions

1.6.1 100-Pin LFQFP

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (1/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
1		P06*1					
2		P03*1					DA0
3		P04*1					
4		PJ3	GTIOC6B/GTIOC6B#	CTS6#/RTS6#/SS6#			
5	VCL						
6		PJ1	GTIOC6A/GTIOC6A#/ GTCPPO0				
7	MD/FINED	PG7					
8	XCIN	PH7					
9	XCOUT/ EXCIN	PH6					
10	RES#						
11	XTAL	P37				IRQ4	
12	VSS						
13	EXTAL	P36				IRQ2	
14	VCC						
15	UPSEL	P35				NMI	
16		P34	GTIOC3A/GTIOC3A#/ GTIU/TMCI3	SCK6		IRQ4	
17		P33	GTIOC1B/GTIOC7B/ GTIOC1B#/GTIOC7B#/ TMRI3	RXD6/SMISO6/SSCL6/ CRX0*2		IRQ3	
18		P32	GTIOC1A/GTIOC7A/ GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/ RTCIC2	TXD6/SMOSI6/SSDA6/ CTX0*2/ USB0_VBUSEN*2	TS0	IRQ2	
19		P31	GTIOC2B/GTIOC2B#/ GTOWLO/TMCI2/ RTCIC1	CTS1#/RTS1#/SS1#	TS1	IRQ1	
20		P30	GTIOC2A/GTIOC2A#/ GTOWUP/TMRI3/ RTCIC0	RXD1/SMISO1/SSCL1	TS2	IRQ0	
21		P27	GTIOC5B/GTIOC5B#/ TMCI3	SCK1	TS3		
22		P26	GTIOC5A/GTIOC5A#/ TMO1/LPTO	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN*2	TS4		
23		P25	GTIOC1B/GTIOC6A/ GTIOC1B#/GTIOC6A#/ GTETRGB				ADTRG0#
24		P24	GTIOC1A/GTIOC6B/ GTIOC1A#/GTIOC6B#/ GTETRGA/TMRI1	USB0_VBUSEN*2			
25		P23	GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ GTETRGD	CTS000#/RTS000#/ SS000#/DE000			

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (2/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
26		P22	GTIOC0A/GTIOC3A/ GTIOC0A#/GTIOC3A#/ GTETRGC/TMO0	SCK000/TXDB000/ USB0_OVRCURB*2			
27		P21	GTIOC2A/GTIOC4B/ GTIOC2A#/GTIOC4B#/ TMCI0	RXD000/SMISO000/ SSCL000/ USB0_EXICEN*2			
28		P20	GTIOC2B/GTIOC4A/ GTIOC2B#/GTIOC4A#/ TMRI0	TXD000/TXDA000/ SMOSI000/SSDA000/ USB0_ID*2			
29		P17	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/ GTETRGD/GTCPPO0/ GTOUUP/TMO1	SCK1/MISOA/SDA0		IRQ7	
30		P16	GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/ GTETRGC/GTOULO/ TMO2/RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0/ USB0_VBUS*2/ USB0_VBUSEN*2/ USB0_OVRCURB*2		IRQ6	ADTRG0#
31		P15	GTIOC3B/GTIOC5B/ GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2	RXD1/SMISO1/SSCL1/ CRX0*2	TS5	IRQ5	
32		P14	GTIOC6A/GTIOC7B/ GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0*2/ USB0_OVRCURA*2	TS6	IRQ4	
33		P13	GTIOC3B/GTIOC7A/ GTIOC3B#/GTIOC7A#/ GTIV/TMO3	SDA0		IRQ3	
34		P12	TMCI1	SCL0		IRQ2	
35		PH3	GTIOC2B/GTIOC2B#/ TMCI0		TS7		
36		PH2*3	GTIOC1B*3/ GTIOC1B#*3/TMRI0*3	USB0_DM*2	TS8*3	IRQ1*3	
37		PH1*3	GTIOC0B*3/ GTIOC0B#*3/GTOULO*3/ TMO0*3	USB0_DP*2	TS9*3	IRQ0*3	
38		PH0	GTIOC0A/GTIOC0A#/ GTOUUP/CACREF		TS10		
39		P55	GTIOC1A/GTIOC2B/ GTIOC1A#/GTIOC2B#/ TMO3	CRX0*2	TS11		
40		P54	GTIOC2A/GTIOC2A#/ TMCI1	CTX0*2	TS12		
41		P53		PMC0			
42		P52					
43		P51		PMC0			
44		P50					
45	UB	PC7	GTIOC6A/GTIOC6A#/ GTETRGB/GTCPPO0/ TMO2/LPTO/CACREF	TXD008/TXDA008/ SMOSI008/SSDA008/ MISOA	TS13		
46		PC6	GTIOC6B/GTIOC6B#/ GTETRGA/TMCI2	RXD008/SMISO008/ SSCL008/MOSIA/ USB0_EXICEN*2	TS14		

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (3/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
47		PC5	GTIOC0A/GTIOC7A/ GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/ GTIW/TMRI2	SCK008/TXDB008/ RSPCKA/USB0_ID*2/ PMC0	TS15		
48		PC4	GTIOC0B/GTIOC3A/ GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/ GTOULO/TMCI1	SCK5/CTS008#/ RTS008#/SS008#/ DE008/SSLA0/PMC0	TSCAP		
49		PC3	GTIOC2B/GTIOC2B#/ GTETRGB	TXD5/SMOSI5/SSDA5/ PMC0	TS16		
50		PC2	GTIOC2A/GTIOC2A#/ GTETRGA/GTOWUP	RXD5/SMISO5/SSCL5/ SSLA3	TS17		
51		PC1	GTIOC6A/GTIOC6A#/ GTETRGD/GTCPPO0	SCK5/SSLA2			
52		PC0	GTIOC6B/GTIOC6B#/ GTETRGC	CTS5#/RTS5#/SS5#/ SSLA1			
53		PB7	GTIOC0A/GTIOC7B/ GTIOC0A#/GTIOC7B#	TXD009/TXDA009/ SMOSI009/SSDA009	TS18		
54		PB6	GTIOC0B/GTIOC7A/ GTIOC0B#/GTIOC7A#	RXD009/SMISO009/ SSCL009	TS19		
55		PB5	GTIOC4B/GTIOC5A/ GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/ TMRI1	SCK009/TXDB009/ USB0_VBUS*2	TS20		
56		PB4	GTIOC6A/GTIOC6A#	CTS009#/RTS009#/ SS009#/DE009	TS21		
57		PB3	GTIOC1A/GTIOC3A/ GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/ GTETRGD/GTIU/ GTOVUP/TMO0/LPTO	SCK6/PMC0	TS22		
58		PB2	GTIOC3A/GTIOC3A#/ GTETRGC	CTS6#/RTS6#/SS6#	TS23		
59		PB1	GTIOC1B/GTIOC2B/ GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/ GTOVLO/GTIW/ GTOWLO/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4	CMPOB1
60	VCC						
61		PB0	GTIOC0B/GTIOC2A/ GTIOC0B#/GTIOC2A#/ GTOWUP	RXD6/SMISO6/SSCL6/ RSPCKA	TS25		
62	VSS						
63		PA7	GTIOC5B/GTIOC5B#	MISOA			
64		PA6	GTIOC0B/GTIOC5A/ GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/ TMCI3	CTS5#/RTS5#/SS5#/ MOSIA	TS26		
65		PA5	GTIOC4B/GTIOC4B#	RSPCKA	TS27		
66		PA4	GTIOC1B/GTIOC4A/ GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	TS28	IRQ5	CVREFB1

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (4/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
67		PA3	GTIOC1B/GTIOC2B/ GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/ GTETRGB/GTETRGD/ GTOVLO/GTOWLO	RXD5/SMISO5/SSCL5	TS29	IRQ6	CMPB1
68		PA2		RXD5/SMISO5/SSCL5/ SSLA3	TS30		
69		PA1	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/ GTETRGC/GTIV/ GTOUUP	SCK5/SSLA2	TS31		
70		PA0	GTIOC0A/GTIOC1A/ GTIOC0A#/GTIOC1A#/ GTOVUP/CACREF	SSLA1	TS32		
71		PE7				IRQ7	AN023
72		PE6				IRQ6	AN022
73		PE5	GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#			IRQ5	AN021/ CMPOB0
74	CLKOUT	PE4	GTIOC1A/GTIOC2B/ GTIOC1A#/GTIOC2B#/ GTIOC4A/GTIOC4A#/ GTOVUP/GTOWLO		TS33		AN020/ CMPA2
75	CLKOUT	PE3	GTIOC2A/GTIOC4B/ GTIOC2A#/GTIOC4B#/ GTOWUP	CTS12#/RTS12#/SS12#	TS34		AN019
76		PE2	GTIOC1A/GTIOC1A#/ GTOVUP	RXD12/SMISO12/ SSCL12/RXDX12	TS35	IRQ7	AN018/ CVREFB0
77		PE1	GTIOC1B/GTIOC1B#/ GTOVLO	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12			AN017/ CMPB0
78		PE0		SCK12			AN016
79		PD7				IRQ7	AN031
80		PD6				IRQ6	AN030
81		PD5				IRQ5	AN029
82		PD4				IRQ4	AN028
83		PD3				IRQ3	AN027
84		PD2	GTIOC2B/GTIOC2B#	SCK6/CRX0*2		IRQ2	AN026
85		PD1	GTIOC2A/GTIOC2A#	RXD6/SMISO6/SSCL6/ CTX0*2		IRQ1	AN025
86		PD0		TXD6/SMOSI6/SSDA6		IRQ0	AN024
87		P47*1					AN007
88		P46*1					AN006
89		P45*1					AN005
90		P44*1					AN004
91		P43*1					AN003
92		P42*1					AN002
93		P41*1					AN001
94	VREFL0	PJ7*1					
95		P40*1					AN000

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (5/5)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
96	VREFH0	PJ6*1					
97	AVCC0						
98		P07*1					ADTRG0#
99	AVSS0						
100		P05*1					DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. Not present in the RX260.
Note 3. Not present in the RX261.

1.6.2 80-Pin LFQFP

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (1/4)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
1		P06*1					
2		P03*1					DA0
3		P04*1					
4	VCL						
5		PJ1	GTIOC6A/GTIOC6A#/ GTCPPO0				
6	MD/FINED	PG7					
7	XCIN	PH7					
8	XCOUT/ EXCIN	PH6					
9	RES#						
10	XTAL	P37				IRQ4	
11	VSS						
12	EXTAL	P36				IRQ2	
13	VCC						
14	UPSEL	P35				NMI	
15		P34	GTIOC3A/GTIOC3A#/ GTIU/TMCI3	SCK6		IRQ4	
16		P32	GTIOC1A/GTIOC7A/ GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/ RTCIC2	TXD6/SMOSI6/SSDA6/ CTX0*2/ USB0_VBUSEN*2	TS0	IRQ2	
17		P31	GTIOC2B/GTIOC2B#/ GTOWLO/TMCI2/ RTCIC1	CTS1#/RTS1#/SS1#	TS1	IRQ1	
18		P30	GTIOC2A/GTIOC2A#/ GTOWUP/TMRI3/ RTCIC0	RXD1/SMISO1/SSCL1	TS2	IRQ0	
19		P27	GTIOC5B/GTIOC5B#/ TMCI3	SCK1	TS3		
20		P26	GTIOC5A/GTIOC5A#/ TMO1/LPTO	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN*2	TS4		
21		P21	GTIOC2A/GTIOC4B/ GTIOC2A#/GTIOC4B#/ TMCI0	RXD000/SMISO000/ SSCL000/ USB0_EXICEN*2			
22		P20	GTIOC2B/GTIOC4A/ GTIOC2B#/GTIOC4A#/ TMRI0	TXD000/SMOSI000/ SSDA000/USB0_ID*2			
23		P17	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/ GTETRGD/GTCPPO0/ GTOUUP/TMO1	SCK1/MISOA/SDA0		IRQ7	
24		P16	GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/ GTETRGC/GTOULO/ TMO2/RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0/ USB0_VBUS*2/ USB0_VBUSEN*2/ USB0_OVRCURB*2		IRQ6	ADTRG0#

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (2/4)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
25		P15	GTIOC3B/GTIOC5B/ GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2	RXD1/SMISO1/SSCL1/ CRX0*2	TS5	IRQ5	
26		P14	GTIOC6A/GTIOC7B/ GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0*2/ USB0_OVRCURA*2	TS6	IRQ4	
27		P13	GTIOC3B/GTIOC7A/ GTIOC3B#/GTIOC7A#/ GTIV/TMO3	SDA0		IRQ3	
28		P12	TMCI1	SCL0		IRQ2	
29		PH3	GTIOC2B/GTIOC2B#/ TMCI0		TS7		
30		PH2*3	GTIOC1B*3/ GTIOC1B#*3/TMRI0*3	USB0_DM*2	TS8*3	IRQ1*3	
31		PH1*3	GTIOC0B*3/ GTIOC0B#*3/GTOULO*3/ TMO0*3	USB0_DP*2	TS9*3	IRQ0*3	
32		PH0	GTIOC0A/GTIOC0A#/ GTOUUP/CACREF		TS10		
33		P55	GTIOC1A/GTIOC2B/ GTIOC1A#/GTIOC2B#/ TMO3	CRX0*2	TS11		
34		P54	GTIOC2A/GTIOC2A#/ TMCI1	CTX0*2	TS12		
35	UB	PC7	GTIOC6A/GTIOC6A#/ GTETRGB/GTCPPO0/ TMO2/LPTO/CACREF	TXD008/TXDA008/ SMOSI008/SSDA008/ MISOA	TS13		
36		PC6	GTIOC6B/GTIOC6B#/ GTETRGA/TMCI2	RXD008/SMISO008/ SSCL008/MOSIA/ USB0_EXICEN*2	TS14		
37		PC5	GTIOC0A/GTIOC7A/ GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/ GTIW/TMRI2	SCK008/TXDB008/ RSPCKA/USB0_ID*2/ PMC0	TS15		
38		PC4	GTIOC0B/GTIOC3A/ GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/ GTOULO/TMCI1	SCK5/CTS008#/ RTS008#/SS008#/ DE008/SSLA0/PMC0	TSCAP		
39		PC3	GTIOC2B/GTIOC2B#/ GTETRGB	TXD5/SMOSI5/SSDA5/ PMC0	TS16		
40		PC2	GTIOC2A/GTIOC2A#/ GTETRGA/GTOWUP	RXD5/SMISO5/SSCL5/ SSLA3	TS17		
41		PB7/PC1*4	GTIOC0A/GTIOC7B/ GTIOC0A#/GTIOC7B#	TXD009/TXDA009/ SMOSI009/SSDA009	TS18		
42		PB6/PC0*4	GTIOC0B/GTIOC7A/ GTIOC0B#/GTIOC7A#	RXD009/SMISO009/ SSCL009	TS19		
43		PB5	GTIOC4B/GTIOC5A/ GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/ TMRI1	SCK009/TXDB009/ USB0_VBUS*2	TS20		
44		PB4	GTIOC6A/GTIOC6A#	CTS009#/RTS009#/ SS009#/DE009	TS21		

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (3/4)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
45		PB3	GTIOC1A/GTIOC3A/ GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/ GTETRGD/GTIU/ GTOVUP/TMO0/LPTO	SCK6/PMC0	TS22		
46		PB2	GTIOC3A/GTIOC3A#/ GTETRGC	CTS6#/RTS6#/SS6#	TS23		
47		PB1	GTIOC1B/GTIOC2B/ GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/ GTOVLO/GTIW/ GTOWLO/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4	CMPOB1
48	VCC						
49		PB0	GTIOC0B/GTIOC2A/ GTIOC0B#/GTIOC2A#/ GTOWUP	RXD6/SMISO6/SSCL6/ RSPCKA	TS25		
50	VSS						
51		PA6	GTIOC0B/GTIOC5A/ GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/ TMCI3	CTS5#/RTS5#/SS5#/ MOSIA	TS26		
52		PA5	GTIOC4B/GTIOC4B#	RSPCKA	TS27		
53		PA4	GTIOC1B/GTIOC4A/ GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	TS28	IRQ5	CVREFB1
54		PA3	GTIOC1B/GTIOC2B/ GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/ GTETRGB/GTETRGD/ GTOVLO/GTOWLO	RXD5/SMISO5/SSCL5	TS29	IRQ6	CMPB1
55		PA2		RXD5/SMISO5/SSCL5/ SSLA3	TS30		
56		PA1	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/ GTETRGC/GTIV/ GTOUUP	SCK5/SSLA2	TS31		
57		PA0	GTIOC0A/GTIOC1A/ GTIOC0A#/GTIOC1A#/ GTOVUP/CACREF	SSLA1	TS32		
58		PE5	GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#			IRQ5	AN021/ CMPOB0
59	CLKOUT	PE4	GTIOC1A/GTIOC2B/ GTIOC1A#/GTIOC2B#/ GTIOC4A/GTIOC4A#/ GTOVUP/GTOWLO		TS33		AN020/ CMPA2
60	CLKOUT	PE3	GTIOC2A/GTIOC4B/ GTIOC2A#/GTIOC4B#/ GTOWUP	CTS12#/RTS12#/SS12#	TS34		AN019
61		PE2	GTIOC1A/GTIOC1A#/ GTOVUP	RXD12/SMISO12/ SSCL12/RXDX12	TS35	IRQ7	AN018/ CVREFB0
62		PE1	GTIOC1B/GTIOC1B#/ GTOVLO	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12			AN017/ CMPB0

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (4/4)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
63		PE0		SCK12			AN016
64		PD2	GTIOC2B/GTIOC2B#	SCK6/CRX0*2		IRQ2	AN026
65		PD1	GTIOC2A/GTIOC2A#	RXD6/SMISO6/SSCL6/ CTX0*2		IRQ1	AN025
66		PD0		TXD6/SMOSI6/SSDA6		IRQ0	AN024
67		P47*1					AN007
68		P46*1					AN006
69		P45*1					AN005
70		P44*1					AN004
71		P43*1					AN003
72		P42*1					AN002
73		P41*1					AN001
74	VREFL0	PJ7*1					
75		P40*1					AN000
76	VREFH0	PJ6*1					
77	AVCC0						
78		P07*1					ADTRG0#
79	AVSS0						
80		P05*1					DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. Not present in the RX260.
Note 3. Not present in the RX261.
Note 4. PC0 and PC1 are valid only when the port switching function is selected.

1.6.3 64-Pin LFQFP

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP) (1/3)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
1		P03*1					DA0
2	VCL						
3	MD/FINED	PG7					
4	XCIN	PH7					
5	XCOUT/ EXCIN	PH6					
6	RES#						
7	XTAL	P37				IRQ4	
8	VSS						
9	EXTAL	P36				IRQ2	
10	VCC						
11	UPSEL	P35				NMI	
12		P32	GTIOC1A/GTIOC7A/ GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/ RTCIC2	TXD6/SMOSI6/SSDA6/ CTX0*2/ USB0_VBUSEN*2	TS0	IRQ2	
13		P31	GTIOC2B/GTIOC2B#/ GTOWLO/TMCI2/ RTCIC1	CTS1#/RTS1#/SS1#	TS1	IRQ1	
14		P30	GTIOC2A/GTIOC2A#/ GTOWUP/TMRI3/ RTCIC0	RXD1/SMISO1/SSCL1	TS2	IRQ0	
15		P27	GTIOC5B/GTIOC5B#/ TMCI3	SCK1	TS3		
16		P26	GTIOC5A/GTIOC5A#/ TMO1/LPTO	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN*2	TS4		
17		P17	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/ GTETRGD/GTCPPO0/ GTOUUP/TMO1	SCK1/MISOA/SDA0		IRQ7	
18		P16	GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/ GTETRGC/GTOULO/ TMO2/RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0/ USB0_VBUS*2/ USB0_VBUSEN*2/ USB0_OVRCURB*2		IRQ6	ADTRG0#
19		P15	GTIOC3B/GTIOC5B/ GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2	RXD1/SMISO1/SSCL1/ CRX0*2	TS5	IRQ5	
20		P14	GTIOC6A/GTIOC7B/ GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0*2/ USB0_OVRCURA*2	TS6	IRQ4	
21		PH3	GTIOC2B/GTIOC2B#/ TMCI0		TS7		
22		PH2*3	GTIOC1B*3/ GTIOC1B#*3/ TMRI0*3	USB0_DM*2	TS8*3	IRQ1*3	

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP) (2/3)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
23		PH1*3	GTIOC0B*3/ GTIOC0B#*3/GTOULO*3/ TMO0*3	USB0_DP*2	TS9*3	IRQ0*3	
24		PH0	GTIOC0A/GTIOC0A#/ GTOUUP/CACREF		TS10		
25		P55	GTIOC1A/GTIOC2B/ GTIOC1A#/GTIOC2B#/ TMO3	CRX0*2	TS11		
26		P54	GTIOC2A/GTIOC2A#/ TMCI1	CTX0*2	TS12		
27	UB	PC7	GTIOC6A/GTIOC6A#/ GTETRGB/GTCPPO0/ TMO2/LPTO/CACREF	TXD008/TXDA008/ SMOSI008/SSDA008/ MISOA	TS13		
28		PC6	GTIOC6B/GTIOC6B#/ GTETRGA/TMCI2	RXD008/SMISO008/ SSCL008/MOSIA/ USB0_EXICEN*2	TS14		
29		PC5	GTIOC0A/GTIOC7A/ GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/ GTIW/TMRI2	SCK008/TXDB008/ RSPCKA/USB0_ID*2/ PMC0	TS15		
30		PC4	GTIOC0B/GTIOC3A/ GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/ GTOULO/TMCI1	SCK5/CTS008#/ RTS008#/SS008#/ DE008/SSLA0/PMC0	TSCAP		
31		PC3	GTIOC2B/GTIOC2B#/ GTETRGB	TXD5/SMOSI5/SSDA5/ PMC0	TS16		
32		PC2	GTIOC2A/GTIOC2A#/ GTETRGA/GTOWUP	RXD5/SMISO5/SSCL5/ SSLA3	TS17		
33		PB7/PC1*4	GTIOC0A/GTIOC7B/ GTIOC0A#/GTIOC7B#	TXD009/TXDA009/ SMOSI009/SSDA009	TS18		
34		PB6/PC0*4	GTIOC0B/GTIOC7A/ GTIOC0B#/GTIOC7A#	RXD009/SMISO009/ SSCL009	TS19		
35		PB5	GTIOC4B/GTIOC5A/ GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/ TMRI1	SCK009/TXDB009/ USB0_VBUS*2	TS20		
36		PB3	GTIOC1A/GTIOC3A/ GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/ GTETRGD/GTIU/ GTOVUP/TMO0/LPTO	SCK6/PMC0	TS22		
37		PB1	GTIOC1B/GTIOC2B/ GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/ GTOVLO/GTIW/ GTOWLO/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4	CMPOB1
38	VCC						
39		PB0	GTIOC0B/GTIOC2A/ GTIOC0B#/GTIOC2A#/ GTOWUP	RXD6/SMISO6/SSCL6/ RSPCKA	TS25		
40	VSS						
41		PA6	GTIOC0B/GTIOC5A/ GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/ TMCI3	CTS5#/RTS5#/SS5#/ MOSIA	TS26		

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP) (3/3)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
42		PA4	GTIOC1B/GTIOC4A/ GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/ TMRI0	TXD5/SMOSI5/SSDA5/ SSLA0	TS28	IRQ5	CVREFB1
43		PA3	GTIOC1B/GTIOC2B/ GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/ GTETRGB/GTETRGD/ GTOVLO/GTOWLO	RXD5/SMISO5/SSCL5	TS29	IRQ6	CMPB1
44		PA1	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/ GTETRGC/GTIV/ GTOUUP	SCK5/SSLA2	TS31		
45		PA0	GTIOC0A/GTIOC1A/ GTIOC0A#/GTIOC1A#/ GTOVUP/CACREF	SSLA1	TS32		
46		PE5	GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#			IRQ5	AN021/ CMPOB0
47	CLKOUT	PE4	GTIOC1A/GTIOC2B/ GTIOC1A#/GTIOC2B#/ GTIOC4A/GTIOC4A#/ GTOVUP/GTOWLO		TS33		AN020/ CMPA2
48	CLKOUT	PE3	GTIOC2A/GTIOC4B/ GTIOC2A#/GTIOC4B#/ GTOWUP	CTS12#/RTS12#/SS12#	TS34		AN019
49		PE2	GTIOC1A/GTIOC1A#/ GTOVUP	RXD12/SMISO12/ SSCL12/RXDX12	TS35	IRQ7	AN018/ CVREFB0
50		PE1	GTIOC1B/GTIOC1B#/ GTOVLO	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12			AN017/ CMPB0
51		PE0		SCK12			AN016
52		P47*1					AN007
53		P46*1					AN006
54		P45*1					AN005
55		P44*1					AN004
56		P43*1					AN003
57		P42*1					AN002
58		P41*1					AN001
59	VREFL0	PJ7*1					
60		P40*1					AN000
61	VREFH0	PJ6*1					
62	AVCC0						
63		P05*1					DA1
64	AVSS0						

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. Not present in the RX260.
Note 3. Not present in the RX261.
Note 4. PC0 and PC1 are valid only when the port switching function is selected.

1.6.4 48-Pin LFQFP, 48-Pin HWQFN

Table 1.8 List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (1/3)

Pin Number 48-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
1	VCL						
2	MD/FINED	PG7					
3	RES#						
4	XTAL	P37				IRQ4	
5	VSS						
6	EXTAL	P36				IRQ2	
7	VCC						
8	UPSEL	P35				NMI	
9		P31	GTIOC2B/GTIOC2B#/ GTOWLO/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1	
10		P30	GTIOC2A/GTIOC2A#/ GTOWUP/TMRI3	RXD1/SMISO1/SSCL1	TS2	IRQ0	
11		P27	GTIOC5B/GTIOC5B#/ TMCI3	SCK1	TS3		
12		P26	GTIOC5A/GTIOC5A#/ TMO1/LPTO	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN*1	TS4		
13		P17	GTIOC0A/GTIOC0B/ GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/ GTETRGD/GTCPPO0/ GTOUUP/TMO1	SCK1/MISOA/SDA0		IRQ7	
14		P16	GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/ GTETRGC/GTOULO/ TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0/ USB0_VBUS*1/ USB0_VBUSEN*1/ USB0_OVRCURB*1		IRQ6	ADTRG0#
15		P15	GTIOC3B/GTIOC5B/ GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2	RXD1/SMISO1/SSCL1/ CRX0*1	TS5	IRQ5	
16		P14	GTIOC6A/GTIOC7B/ GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/ TMRI2	CTS1#/RTS1#/SS1#/ CTX0*1/ USB0_OVRCURA*1	TS6	IRQ4	
17		PH3	GTIOC2B/GTIOC2B#/ TMCI0		TS7		
18		PH2*2	GTIOC1B*2/ GTIOC1B#*2/TMRI0*2	USB0_DM*1	TS8*2	IRQ1*2	
19		PH1*2	GTIOC0B*2/ GTIOC0B#*2/GTOULO*2/ TMO0*2	USB0_DP*1	TS9*2	IRQ0*2	
20		PH0	GTIOC0A/GTIOC0A#/ GTOUUP/CACREF		TS10		
21	UB	PC7	GTIOC6A/GTIOC6A#/ GTETRGB/GTCPPO0/ TMO2/LPTO/CACREF	TXD008/TXDA008/ SMOSI008/SSDA008/ MISOA	TS13		
22		PC6	GTIOC6B/GTIOC6B#/ GTETRGA/TMCI2	RXD008/SMISO008/ SSCL008/MOSIA/ USB0_EXICEN*1	TS14		

Table 1.8 List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (2/3)

Pin Number 48-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
23		PC5	GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/GTETRGD/GTOUUP/GTIW/TMRI2	SCK008/TXDB008/RSPCKA/USB0_ID*1/PMC0	TS15		
24		PC4	GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/GTETRGC/GTIU/GTOULO/TMCI1	SCK5/CTS008#/RTS008#/SS008#/DE008/SSLA0/PMC0	TSCAP		
25		PB5/PC3*3	GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1	USB0_VBUS*1	TS20		
26		PB3/PC2*3	GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO	SCK6/PMC0	TS22		
27		PB1/PC1*3	GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4	CMPOB1
28	VCC						
29		PB0/PC0*3	GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP	RXD6/SMISO6/SSCL6/RSPCKA	TS25		
30	VSS						
31		PA6	GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3	CTS5#/RTS5#/SS5#/MOSIA	TS26		
32		PA4	GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/GTETRGA/GTOVLO/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5	CVREFB1
33		PA3	GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/GTOVLO/GTOWLO	RXD5/SMISO5/SSCL5	TS29	IRQ6	CMPB1
34		PA1	GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP	SCK5/SSLA2	TS31		
35	CLKOUT	PE4	GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO		TS33		AN020/CMPA2
36	CLKOUT	PE3	GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP	CTS12#/RTS12#	TS34		AN019
37		PE2	GTIOC1A/GTIOC1A#/GTOVUP	RXD12/SSCL12/RXDX12	TS35	IRQ7	AN018/CVREFB0

Table 1.8 List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (3/3)

Pin Number 48-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (GPTW, POEG, TMR, LPT, CAC)	Communications (SCI, RSCI, RSPI, RIIC, CANFD, USB, REMC)	Touch sensing	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPB)
38		PE1	GTIOC1B/GTIOC1B#/ GTOVLO	TXD12/SSDA12/ TXDX12/SIOX12			AN017/ CMPB0
39		P47*4					AN007
40		P46*4					AN006
41		P45*4					AN005
42		P42*4					AN002
43		P41*4					AN001
44	VREFL0	PJ7*4					
45		P40*4					AN000
46	VREFH0	PJ6*4					
47	AVCC0						
48	AVSS0						

Note 1. Not present in the RX260.
Note 2. Not present in the RX261.
Note 3. PC0 to PC3 are valid only when the port switching function is selected.
Note 4. The power source of the I/O buffer for these pins is AVCC0.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Ports for 5 V tolerant*[1]	V_{in}	–0.3 to +6.5	V
	P03 to P07, P40 to P47, PJ6, PJ7		–0.3 to AVCC0 + 0.3	V
	Ports other than above		–0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to +6.5	V
Analog input voltage	AN000 to AN007 are in use.	V_{AN}	–0.3 to AVCC0 + 0.3	V
	AN016 to AN031 are in use.		–0.3 to VCC + 0.3	
Junction temperature	D-version	T_j	–40 to +105	°C
	G-version		–40 to +112	
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin, refer to section 2.16.1, Connecting VCL Capacitor and Bypass Capacitors.
Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. P12, P13, P16, and P17 are 5 V tolerant.

2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages		VCC*1, *2	USB is in use.	3.0	—	3.6	V
			One or more of PLL, PLL2, RSIP, CTSU, internal reference voltage, and temperature sensor are in use.	1.8	—	5.5	
			Other than above	1.6	—	5.5	
		VSS		—	0	—	
Analog power supply voltages		AVCC0*1		1.6	—	5.5	V
		AVSS0		—	0	—	
		VREFH0		1.6	—	AVCC0	
		VREFL0		—	0	—	
Input voltage	Ports for 5 V tolerant: P12, P13, P16, P17	V_{in}		–0.3	—	5.8	V
	P03 to P07, P40 to P47, PJ6, PJ7			–0.3	—	AVCC0 + 0.3	
	Ports other than above			–0.3	—	VCC + 0.3	
Operating temperature*3	D version	T_{opr}		–40	—	85	°C
	G version			–40	—	105	

Note 1. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.
Note 2. When VCC < 2.4 V, normal operating mode functions of the CTSU are restricted. For details, refer to section 39, Capacitive Touch Sensing Unit (CTSU2SLa) in the User's Manual: Hardware.
Note 3. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, refer to section 1.2, List of Products.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	4.7μF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 4.7 μF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—	V	
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	IRQ input pin, GPTW input pin, POEG input pin, TMR input pin, SCI input pin, RSCI input pin, RSPI input pin, CAC input pin, CANFD input pin, RTC input pin, USB pin, REMC input pin, ADTRG0# input pin*1, RES#, NMI, MD	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.1 × VCC	—	—		
	ADTRG0# input pin*2	V_{IH}	0.8 × AVCC0	—	—		
		V_{IL}	—	—	0.2 × AVCC0		
		ΔV_T	0.1 × AVCC0	—	—		
Input level voltage (except for schmitt trigger input pins)	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
	RIIC input pin (SMBus)	V_{IH}	2.2	—	—		VCC = 3.6 to 5.5 V
			2.0	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.8		VCC = 3.6 to 5.5 V
			—	—	0.5		VCC = 2.7 to 3.6 V
	P12 to P17, P20 to P27, P30 to P37, P50 to P55, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PH6, PH7, PJ1, PJ3, PG7	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	P03 to P07, P40 to P47, PJ6, PJ7	V_{IH}	0.8 × AVCC0	—	—		
		V_{IL}	—	—	0.2 × AVCC0		

Note 1. The ADTRG0# input pin is assigned to P16 and P25.
Note 2. The ADTRG0# input pin is assigned to P07.

Table 2.5 DC Characteristics (2)

Conditions: 1.6 V ≤ VCC < 2.7 V, 1.6 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin, GPTW input pin, POEG input pin, TMR input pin, SCI input pin, RSCI input pin, RSPI input pin, CAC input pin, CANFD input pin, RTC input pin, USB pin, REMC input pin, ADTRG0# input pin*1, RES#, NMI, MD	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		$ΔV_T$	0.01 × VCC	—	—		
	ADTRG0# input pin*2	V_{IH}	0.8 × AVCC0	—	—		
		V_{IL}	—	—	0.2 × AVCC0		
		$ΔV_T$	0.01 × AVCC0	—	—		
Input level voltage (except for schmitt trigger input pins)	EXTAL (external clock input)	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
	P12 to P17, P20 to P27, P30 to P37, P50 to P55, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH0 to PH3, PH6, PH7, PJ1, PJ3, PG7	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	P03 to P07, P40 to P47, PJ6, PJ7	V_{IH}	0.8 × AVCC0	—	—		
		V_{IL}	—	—	0.2 × AVCC0		

Note 1. The ADTRG0# input pin is assigned to P16 and P25.
Note 2. The ADTRG0# input pin is assigned to P07.

Table 2.6 DC Characteristics (3)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, P35, PH6, PH7	$\| I_{in} \|$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports for 5-V tolerant	$\| I_{TSI} \|$	—	—	1.0	μA	V_{in} = 0 V, 5.8 V
	PJ6, PJ7, USB0_DM, USB0_DP		—	—	1.0		V_{in} = 0 V, VCC
	Other than ports for 5 V tolerant and PJ6, PJ7		—	—	0.2		V_{in} = 0 V, VCC
Input capacitance	All input pins (except for P35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
	P35, USB0_DM, USB0_DP		—	—	30		

Table 2.7 DC Characteristics (4)

Conditions: 1.6 V ≤ VCC < 5.5 V, 1.6 V ≤ AVCC0 < 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for P35, PH6, PH7)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 2.8 DC Characteristics (5) (1/3)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 64 MHz	I_{CC}	4.4	—	mA	
				ICLK = 48 MHz		3.4	—		
				ICLK = 32 MHz		2.7	—		
				ICLK = 16 MHz		1.8	—		
				ICLK = 8 MHz		1.4	—		
				ICLK = 4 MHz		1.2	—		
			All peripheral operation: Normal*3	ICLK = 64 MHz		19.5	—		
				ICLK = 48 MHz		14.8	—		
				ICLK = 32 MHz		12.3	—		
				ICLK = 16 MHz		6.8	—		
				ICLK = 8 MHz		4.1	—		
				ICLK = 4 MHz		2.7	—		
			All peripheral operation: Max.*3	ICLK = 64 MHz		—	34.5		
				ICLK = 32 MHz		—	21.7		
		Sleep mode	No peripheral operation*2	ICLK = 64 MHz		2.4	—		
				ICLK = 48 MHz		1.9	—		
				ICLK = 32 MHz		1.6	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.1	—		
				ICLK = 4 MHz		1.0	—		
			All peripheral operation: Normal*3	ICLK = 64 MHz		11.0	—		
				ICLK = 48 MHz		8.4	—		
				ICLK = 32 MHz		7.8	—		
				ICLK = 16 MHz		4.5	—		
				ICLK = 8 MHz		2.8	—		
				ICLK = 4 MHz		2.0	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 64 MHz		1.6	—		
				ICLK = 48 MHz		1.3	—		
				ICLK = 32 MHz		1.2	—		
				ICLK = 16 MHz		1.0	—		
				ICLK = 8 MHz		0.9	—		
				ICLK = 4 MHz		0.9	—		
			All peripheral operation: Normal*3	ICLK = 64 MHz		9.2	—		
				ICLK = 48 MHz		7.0	—		
				ICLK = 32 MHz		6.6	—		
				ICLK = 16 MHz		3.9	—		
				ICLK = 8 MHz		2.5	—		
				ICLK = 4 MHz		1.8	—		
		Increase during flash rewrite*5				2.6	—		

Table 2.8 DC Characteristics (5) (2/3)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 24 MHz	I_{CC}	1.8	—	mA	
				ICLK = 12 MHz		1.2	—		
				ICLK = 8 MHz		1.0	—		
				ICLK = 4 MHz		0.4	—		
				ICLK = 1 MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		9.1	—		
				ICLK = 12 MHz		5.0	—		
				ICLK = 8 MHz		3.7	—		
				ICLK = 4 MHz		2.2	—		
				ICLK = 1 MHz		1.2	—		
			All peripheral operation: Max.*7	ICLK = 24 MHz		—	18.1		
		Sleep mode	No peripheral operation*6	ICLK = 24 MHz		1.1	—		
				ICLK = 12 MHz		0.8	—		
				ICLK = 8 MHz		0.7	—		
				ICLK = 4 MHz		0.2	—		
				ICLK = 1 MHz		0.2	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		5.8	—		
				ICLK = 12 MHz		3.3	—		
				ICLK = 8 MHz		2.7	—		
				ICLK = 4 MHz		1.7	—		
				ICLK = 1 MHz		1.1	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 24 MHz		0.8	—		
				ICLK = 12 MHz		0.6	—		
				ICLK = 8 MHz		0.6	—		
				ICLK = 4 MHz		0.1	—		
				ICLK = 1 MHz		0.1	—		
			All peripheral operation: Normal*7	ICLK = 24 MHz		4.9	—		
				ICLK = 12 MHz		2.8	—		
				ICLK = 8 MHz		2.3	—		
				ICLK = 4 MHz		1.5	—		
				ICLK = 1 MHz		1.0	—		
		Increase during flash rewrite*5				2.1	—		

Table 2.8 DC Characteristics (5) (3/3)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ.*4	Max.	Unit	Test Conditions
Supply current*1	Middle-speed operating mode 2	Normal operating mode	No peripheral operation*8	ICLK = 1 MHz	I_{CC}	160	—	μA	
			All peripheral operation: Normal*9	ICLK = 1 MHz		1170	—		
			All peripheral operation: Max.*9	ICLK = 1 MHz		—	4520		
		Sleep mode	No peripheral operation*8	ICLK = 1 MHz		120	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		1030	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 1 MHz		110	—		
			All peripheral operation: Normal*9	ICLK = 1 MHz		990	—		
		Increase during flash rewrite*5				1420	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*10	ICLK = 32.768 kHz		4.3	—		
			All peripheral operation: Normal*11, *12	ICLK = 32.768 kHz		13.9	—		
			All peripheral operation: Max. *11, *12	ICLK = 32.768 kHz		—	1500		
		Sleep mode	No peripheral operation*10	ICLK = 32.768 kHz		2.9	—		
			All peripheral operation: Normal*11	ICLK = 32.768 kHz		9.0	—		
		Deep sleep mode	No peripheral operation*10	ICLK = 32.768 kHz		2.5	—		
			All peripheral operation: Normal*11	ICLK = 32.768 kHz		7.8	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK, PCLKA, and PCLKD are set to the same frequency as ICLK and PCLKB is set to divided by 2 when ICLK is 64 MHz or 48 MHz. FCLK and PCLK are set to the same frequency as ICLK when ICLK is 32 MHz or less.

Note 4. Values when VCC = 3.3 V.

Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral function is stopped. The clock source is PLL when ICLK is 24 MHz, HOCO when ICLK is 8 MHz, and LOCO otherwise. FCLK and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 24 MHz, HOCO when ICLK is (MHz, and LOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.

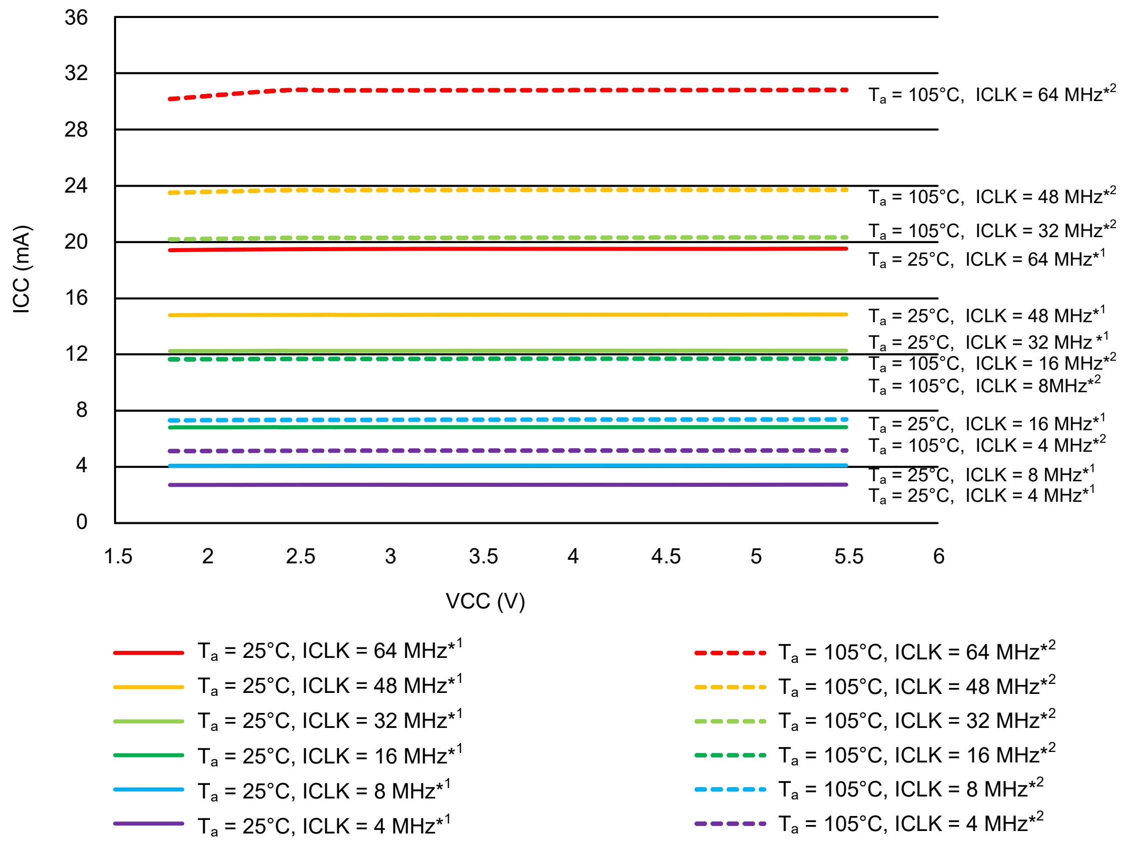
Note 8. Clock supply to the peripheral function is stopped. The clock source is LOCO when ICLK is 1 MHz, FCLK and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is LOCO when ICLK is 1 MHz, FCLK and PCLK are set to the same frequency as ICLK.

Note 10. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.

Note 11. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.

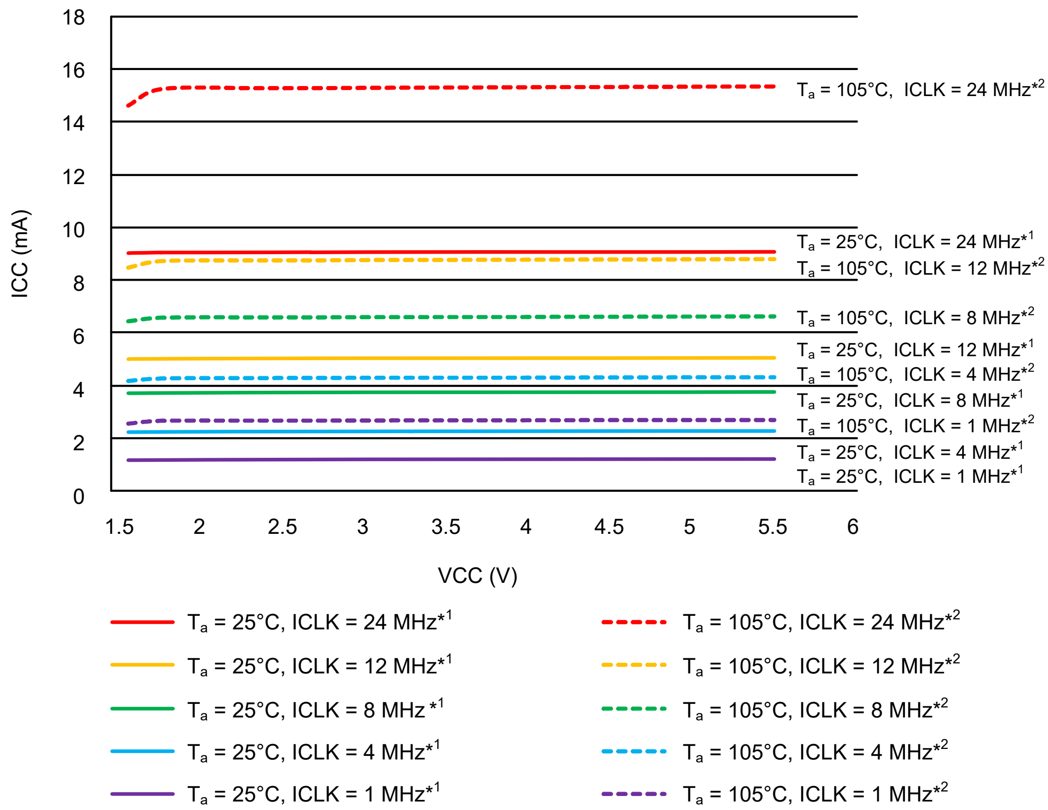
Note 12. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

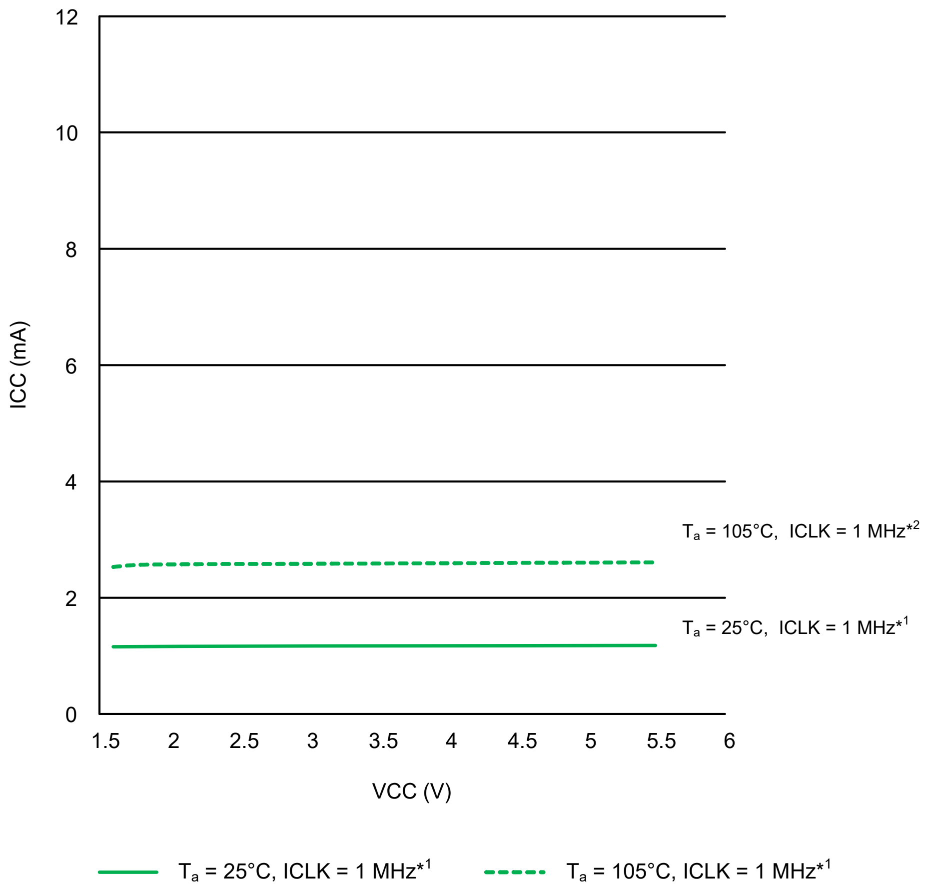
Figure 2.1 Voltage Dependency in High-Speed Operating Mode



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

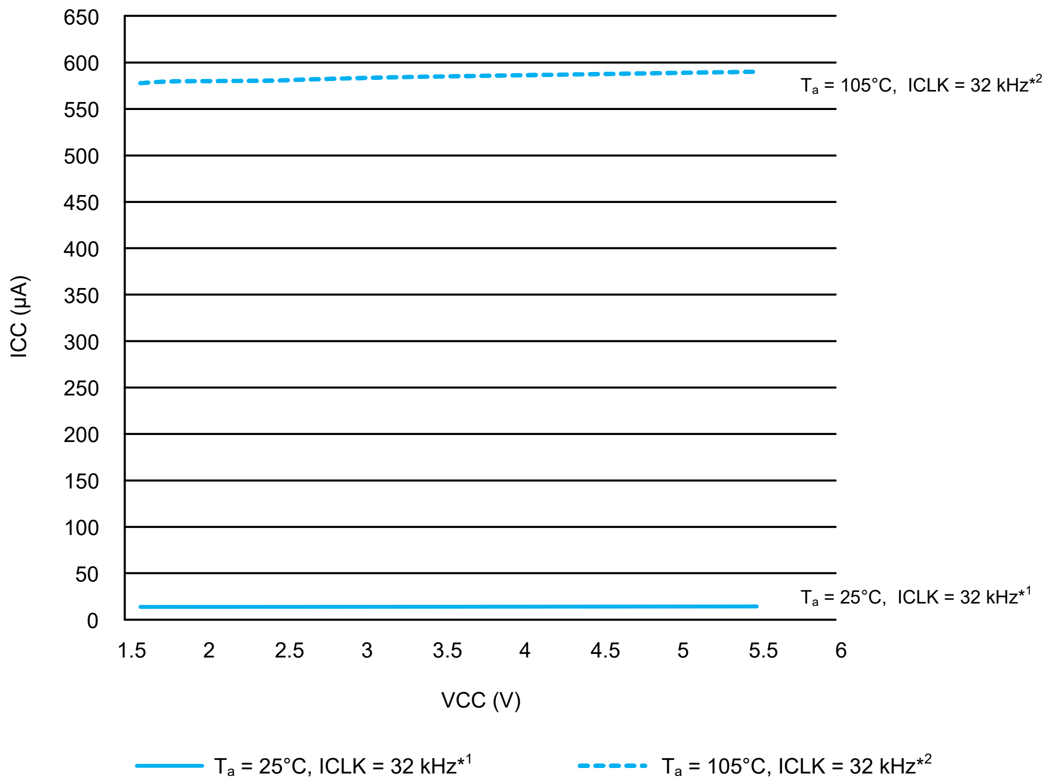
Figure 2.2 Voltage Dependency in Middle-Speed Operating Mode



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 2.3 Voltage Dependency in Middle-Speed Operating Mode 2



Note 1. All peripheral operation is normal. This does not include BGO operation. Average value of the tested middle samples during product evaluation.

Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

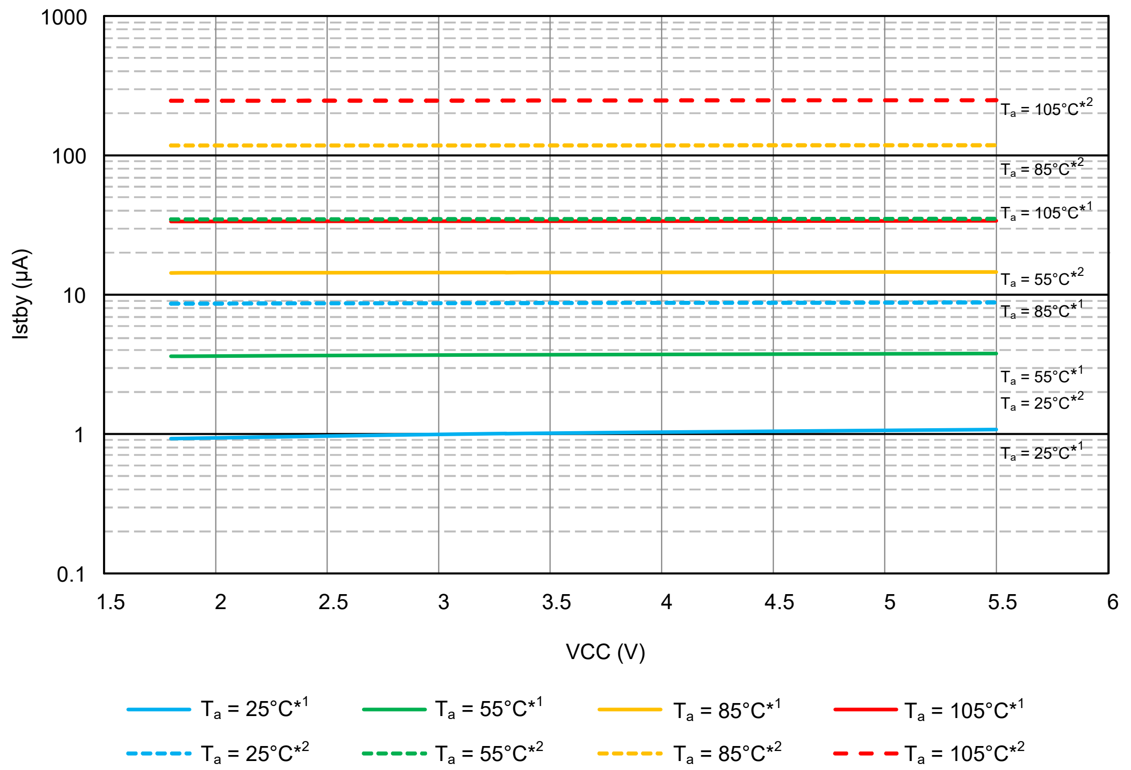
Figure 2.4 Voltage Dependency in Low-Speed Operating Mode

Table 2.9 DC Characteristics (6)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

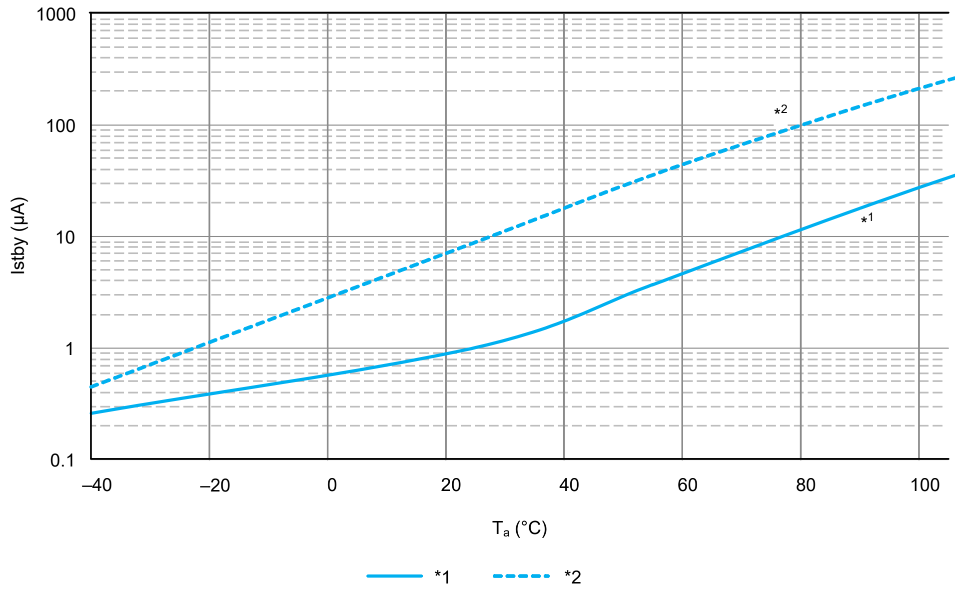
Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	RAM Power Saving disabled	T_a = 25°C	I_{CC}	1.01	19.54	μA	
			T_a = 55°C		3.71	73.97		
			T_a = 85°C		14.44	229.58		
			T_a = 105°C		33.81	470.46		
	Increment for RTC operation*4				0.99	—		SOMCR.SODRV[1:0] set to drive capacity for standard CL
					0.55	—		SOMCR.SODRV[1:0] set to high drive capacity for low CL
					0.32	—		SOMCR.SODRV[1:0] set to middle drive capacity for low CL
					0.22	—		SOMCR.SODRV[1:0] set to low drive capacity for low CL
	Increment for low-power timer operation				0.33	—		LPTCR1.LPCNTCKSEL set to IWDT-dedicated on-chip oscillator
					16.00	—		LPTCR1.LPCNTCKSEL 2 set to Low-speed on-chip oscillator
	Increment for independent watchdog timer operation				0.32	—		
	Increment for REMC operation*4				0.98	—		REMCON1.CSRC[3:0] set to Sub-clock SOMCR.SODRV[1:0] set to drive capacity for standard CL
					0.60	—		REMCON1.CSRC[3:0] set to Sub-clock SOMCR.SODRV[1:0] set to high drive capacity for low CL
					0.42	—		REMCON1.CSRC[3:0] set to Sub-clock SOMCR.SODRV[1:0] set to middle drive capacity for low CL
					0.31	—		REMCON1.CSRC[3:0] set to Sub-clock SOMCR.SODRV[1:0] set to low drive capacity for low CL
					0.29	—		REMCON1.CSRC[3:0] set to IWDT-dedicated on-chip oscillator

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. VCC = 3.3 V.
Note 4. Includes the oscillation circuit.



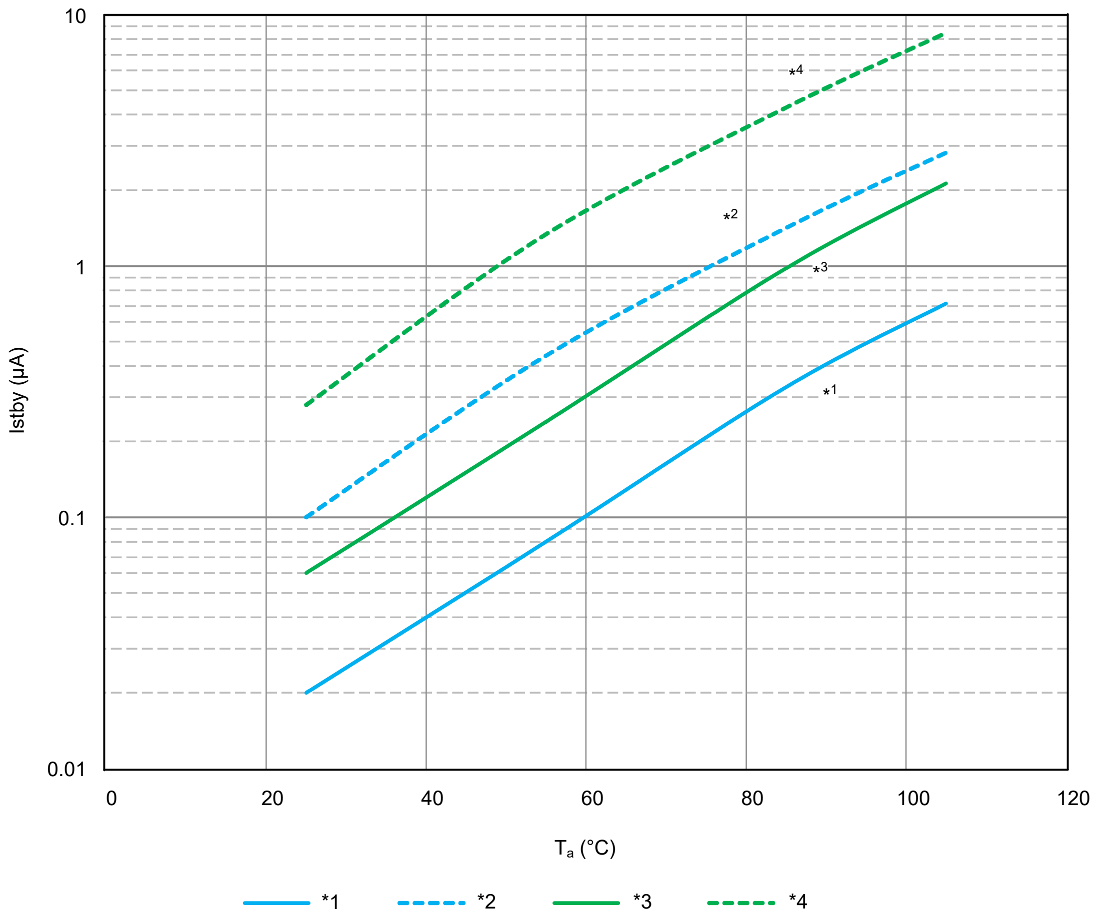
Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.5 Voltage Dependency in Software Standby Mode (Reference Data with RAM Power Saving Disabled)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

Figure 2.6 Temperature Dependency in Software Standby Mode (Reference Data with RAM Power Saving Disabled)



Note 1. Average difference of middle samples tested during product evaluation with and without 32 Kbytes of RAM power savings.
Note 2. Average difference of upper-limt samples tested during product evaluation with and without 32 Kbytes of RAM power savings.
Note 3. Average difference of middle samples tested during product evaluation with and without 96 Kbytes of RAM power savings.
Note 4. Average difference of upper-limt samples tested during product evaluation with and without 96 Kbytes of RAM power savings.

Figure 2.7 Temperature Dependency in Software Standby Mode (Reference Data with RAM Power Saving Enabled)

Table 2.10 DC Characteristics (7)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*4	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.4	mA	
	During A/D conversion (at low-speed conversion)		—	0.3	0.7		
	During D/A conversion (per channel)*1		—	—	0.5		
	Waiting for A/D and D/A conversion		—	—	2.0	μA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	53	122	μA	
	Waiting for A/D conversion		—	—	0.3	μA	
LVD0	—	I_{LVD}	—	0.04	—	μA	
LVD1, LVD2	Per channel		—	0.12	—	μA	
Temperature sensor*3	—	I_{TEMP}	—	120	—	μA	
Comparator B operating current*3	Window function enabled	I_{CMP}*2	—	7.5	12.5	μA	
	Comparator high-speed mode (per channel)		—	5.0	10.0	μA	
	Comparator low-speed mode (per channel)		—	1.5	3.0	μA	
USB operating current*3	During USB communication operation under the following settings and conditions • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.	I_{USBH}*5	—	3.5	—	μA	
	During USB communication operation under the following settings and conditions • Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.	I_{USBF}*5	—	4.0	—	mA	
	During suspended state under the following setting and conditions • Function controller operation is set to full-speed mode (pull up the USB0_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.	I_{SUSP}*6	—	160	—	μA	
RSIP operating current*3	During a self-test	I_{RSIP}*7	—	—	11.3	mA	PCLKB = 32 MHz
	After release from the module-stop state		—	3.6	—	mA	

Note 1. The value for the D/A converter is the value of the power supply current, including the reference current.
Note 2. The values are only for the current drawn by the comparator B module.
Note 3. The values are for the current drawn by the power supply (VCC).
Note 4. The values apply when VCC = AVCC0 = 3.3 V.
Note 5. The value is only for the current drawn by the USB module.
Note 6. The value includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current drawn by this MCU in the suspended state.
Note 7. The values are only for the current drawn by the RSIP module.

Table 2.11 DC Characteristics (8)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.6	—	—	V	

Table 2.12 DC Characteristics (9)

Conditions: 0 V ≤ VCC ≤ 5.5 V, 0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) = 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) = 01b.
Note 3. When OFS1.LVDAS = 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

Table 2.13 DC Characteristics (10)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 2.8 $V_{r\,(VCC)}$ ≤ 0.2 × VCC
		—	—	1	MHz	Figure 2.8 $V_{r\,(VCC)}$ ≤ 0.08 × VCC
		—	—	10	MHz	Figure 2.8 $V_{r\,(VCC)}$ ≤ 0.06 × VCC
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

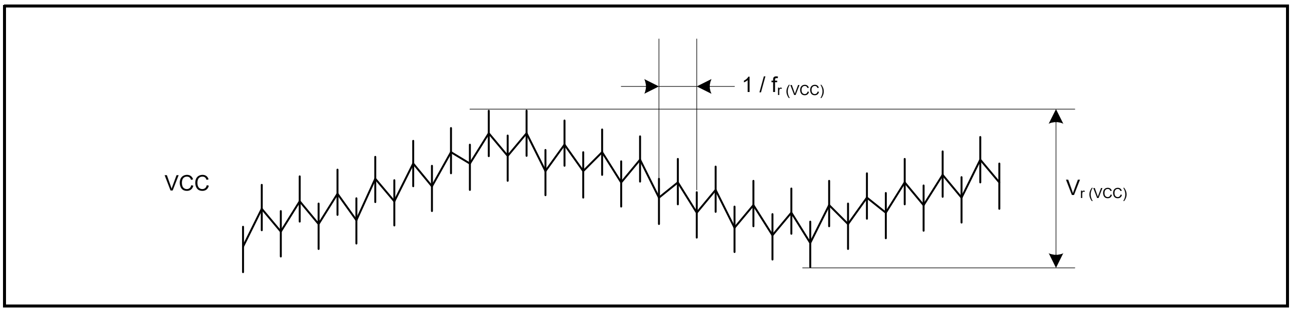


Figure 2.8 Ripple Waveform

Table 2.14 Permissible Output Currents (1)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OL}	8.0	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		8.0	
	Ports other than above		8.0	
Permissible output low current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OL}	40	
	Total of P12 to P17, P20 to P27, P30 to P37, PG7, PH2, PH3, PH6, PH7, PJ1, PJ3		40	
	Total of P50 to P55, PB0 to PB7, PC0 to PC7, PH0, PH1		40	
	Total of PA0 to PA7, PD0 to PD7, PE0 to PE7		40	
	Total of all output pins		80	
Permissible output high current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OH}	–4.0	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		–4.0	
	Ports other than above		–4.0	
Permissible output high current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OH}	–40	
	Total of P12 to P17, P20 to P27, P30 to P37, PG7, PH2, PH3, PH6, PH7, PJ1, PJ3		–40	
	Total of P50 to P55, PB0 to PB7, PC0 to PC7, PH0, PH1		–40	
	Total of PA0 to PA7, PD0 to PD7, PE0 to PE7		–40	
	Total of all output pins		–80	

Note: Do not exceed the permissible total supply current.

Table 2.15 Permissible Output Currents (2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Max.	Unit
Permissible output low current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OL}	8.0	mA
	Ports other than above		8.0	
Permissible output low current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		8.0	
	Ports other than above		8.0	
Permissible output low current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OL}	30	
	Total of P12 to P17, P20 to P27, P30 to P37, PG7, PH2, PH3, PH6, PH7, PJ1, PJ3		30	
	Total of P50 to P55, PB0 to PB7, PC0 to PC7, PH0, PH1		30	
	Total of PA0 to PA7, PD0 to PD7, PE0 to PE7		30	
	Total of all output pins		60	
Permissible output high current (average value per pin)	P03 to P07, P40 to P47, PJ6, PJ7	I_{OH}	–4.0	
	Ports other than above		–4.0	
Permissible output high current (maximum value per pin)	P03 to P07, P40 to P47, PJ6, PJ7		–4.0	
	Ports other than above		–4.0	
Permissible output high current	Total of P03 to P07, P40 to P47, PJ6, PJ7	ΣI_{OH}	–30	
	Total of P12 to P17, P20 to P27, P30 to P37, PG7, PH2, PH3, PH6, PH7, PJ1, PJ3		–30	
	Total of P50 to P55, PB0 to PB7, PC0 to PC7, PH0, PH1		–30	
	Total of PA0 to PA7, PD0 to PD7, PE0 to PE7		–30	
	Total of all output pins		–60	

Note: Do not exceed the permissible total supply current.

Table 2.16 Output Values of Voltage (1)

Conditions: 1.6 V ≤ VCC < 1.8 V, 1.6 V ≤ AVCC0 < 1.8 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.3	V	I_{OL} = 0.3 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.3	—	V	I_{OH} = –0.5 mA
		Ports other than above		VCC – 0.3	—		

Table 2.17 Output Values of Voltage (2)

Conditions: 1.8 V ≤ VCC < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.3	V	I_{OL} = 1.0 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.3	—	V	I_{OH} = –0.5 mA
		Ports other than above		VCC – 0.3	—		

Table 2.18 Output Values of Voltage (3)

Conditions: 2.7 V ≤ VCC < 4.0 V, 2.7 V ≤ AVCC0 < 4.0 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.5	V	I_{OL} = 2.0 mA
	RIIC pins			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = –1.0 mA
		Ports other than above		VCC – 0.5	—		

Table 2.19 Output Values of Voltage (4)

Conditions: 4.0 V ≤ VCC ≤ 5.5 V, 4.0 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC)		V_{OL}	—	0.8	V	I_{OL} = 4.0 mA
	RIIC pins			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports	P03 to P07, P40 to P47, PJ6, PJ7	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –2.0 mA
		Ports other than above		VCC – 0.8	—		

Table 2.20 Thermal Resistance Value (Reference Values)

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal resistance	100-pin LFQFP(PLQP0100KB-B)	θja	—	—	47.9	°C/W	JESD51-2 and JESD51-7 compliant
	80-pin LFQFP (PLQP0080KB-B)		—	—	46.0		
	64-pin LFQFP (PLQP0064KB-C)		—	—	44.8		
	48-pin LFQFP (PLQP0048KB-B)		—	—	53.6		
	48-pin HWQFN (PWQN0048KC-A)		—	—	20.0*1		
	100-pin LFQFP(PLQP0100KB-B)	Ψjt	—	—	0.81		
	80-pin LFQFP (PLQP0080KB-B)		—	—	0.81		
	64-pin LFQFP (PLQP0064KB-C)		—	—	0.81		
	48-pin LFQFP (PLQP0048KB-B)		—	—	1.30		
	48-pin HWQFN (PWQN0048KC-A)		—	—	0.11*1		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the exposed die pad for this purpose is connected to VSS.

2.4 Normal I/O Pin Output Characteristics

Table 2.21 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.05	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.09	—		I_{OH} = –1.0 mA
			—	VCC – 0.20	—		I_{OH} = –2.0 mA
			—	VCC – 0.49	—		I_{OH} = –4.0 mA

Table 2.22 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.02	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.05	—		I_{OH} = –1.0 mA
			—	VCC – 0.10	—		I_{OH} = –2.0 mA
			—	VCC – 0.22	—		I_{OH} = –4.0 mA

Table 2.23 Normal I/O Pin VOH Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	All output pins	V_{OH}	—	VCC – 0.02	—	V	I_{OH} = –0.5 mA
			—	VCC – 0.04	—		I_{OH} = –1.0 mA
			—	VCC – 0.08	—		I_{OH} = –2.0 mA
			—	VCC – 0.15	—		I_{OH} = –4.0 mA

Table 2.24 Normal I/O Pin VOL Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 2.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.08	—		I_{OL} = 2.0 mA
			—	0.17	—		I_{OL} = 4.0 mA
			—	0.43	—		I_{OL} = 8.0 mA

Table 2.25 Normal I/O Pin VOL Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 3.3 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.04	—		I_{OL} = 2.0 mA
			—	0.08	—		I_{OL} = 4.0 mA
			—	0.17	—		I_{OL} = 8.0 mA

Table 2.26 Normal I/O Pin VOL Voltage Characteristics (Reference Values)

Conditions: VCC = AVCC0 = 5.0 V, VSS = AVSS0 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	0.01	—	V	I_{OL} = 0.5 mA
			—	0.01	—		I_{OL} = 1.0 mA
			—	0.03	—		I_{OL} = 2.0 mA
			—	0.06	—		I_{OL} = 4.0 mA
			—	0.12	—		I_{OL} = 8.0 mA

2.5 AC Characteristics

2.5.1 Clock Timing

Table 2.27 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V*5	1.8 V ≤ VCC < 2.4 V*6	2.4 V ≤ VCC ≤ 5.5 V	When USB is in Use, 3.0 V ≤ VCC ≤ 3.6 V	
Maximum operating frequency *4	System clock (ICLK)	f_{max}	16	48	64	64	MHz
	FlashIF clock (FCLK) *1, *2		16	48	64	64	
	Peripheral module clock (PCLKA)		16	48	64	64	
	Peripheral module clock (PCLKB)		16	32	32	32	
	Peripheral module clock (PCLKD)*3		16	48	64	64	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 2.34, HOCO Clock Timing, Table 2.35, PLL Clock Timing and Table 2.36, PLL2 Clock Timing.
Note 5. This is applicable when the RSIP module is to be used.
Note 6. The RSIP module cannot be used. Do not make the settings for release from the module-stop state.

Table 2.28 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC					Unit
			1.6 V ≤ VCC < 1.8 V*6	1.8 V ≤ VCC < 2.4 V*5	1.8 V ≤ VCC < 2.4 V*6	2.4V ≤ VCC ≤ 5.5 V	When USB is in Use, 3.0 V ≤ VCC ≤ 3.6 V	
Maximum operating frequency *4	System clock (ICLK)	f_{max}	4	16	24	24	24	MHz
	FlashIF clock (FCLK) *1, *2		4	16	24	24	24	
	Peripheral module clock (PCLKA)		4	16	24	24	24	
	Peripheral module clock (PCLKB)		4	16	24	24	24	
	Peripheral module clock (PCLKD)*3		4	16	24	24	24	
	USB clock (UCLK)	f_{usb}	—	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. The maximum operating frequency does not include HOCO error or PLL jitter. See Table 2.34, HOCO Clock Timing, Table 2.35, PLL Clock Timing and Table 2.36, PLL2 Clock Timing.
Note 5. This is applicable when the RSIP module is to be used.
Note 6. The RSIP module cannot be used. Do not make the settings for release from the module-stop state.

Table 2.29 Operating Frequency Value (Middle-Speed Operating Mode 2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.6 V ≤ VCC < 1.8 V*4	1.8 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	1	1	MHz
	FlashIF clock (FCLK)*1, *2		1	1	
	Peripheral module clock (PCLKA)		1	1	
	Peripheral module clock (PCLKB)		1	1	
	Peripheral module clock (PCLKD)*3		1	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory.
Note 2. The frequency accuracy of FCLK should be ±3.5%.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. The RSIP module cannot be used. Do not make the settings for release from the module-stop state.

Table 2.30 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	VCC	Unit
			1.6 V ≤ VCC ≤ 5.5 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	
	Peripheral module clock (PCLKA)		32.768	
	Peripheral module clock (PCLKB)		32.768	
	Peripheral module clock (PCLKD)*2		32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.

Table 2.31 EXTAL Clock Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	1.8 V ≤ VCC ≤ 5.5 V	t_{Xcyc}	50	—	—	ns	Figure 2.9
	1.6 V ≤ VCC < 1.8 V		250	—	—	ns	
EXTAL external clock input high pulse width	1.8 V ≤ VCC ≤ 5.5 V	t_{XH}	20	—	—	ns	
	1.6 V ≤ VCC < 1.8 V		120	—	—	ns	
EXTAL external clock input low pulse width	1.8 V ≤ VCC ≤ 5.5 V	t_{XL}	20	—	—	ns	
	1.6 V ≤ VCC < 1.8 V		120	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

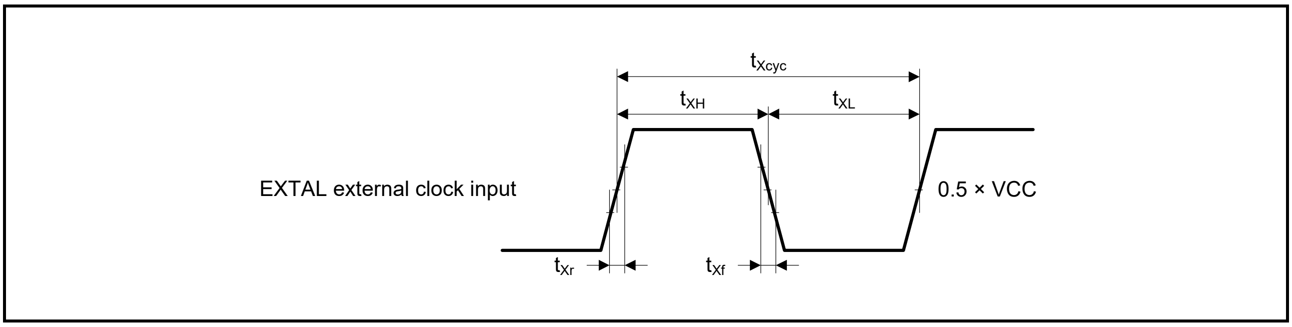


Figure 2.9 EXTAL External Clock Input Timing

Table 2.32 Main Clock Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*1	$t_{MAINOSC}$	—	3	—	ms	Figure 2.10
Main clock oscillation stabilization time (ceramic resonator)*1	$t_{MAINOSC}$	—	50	—	μs	

Note 1. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

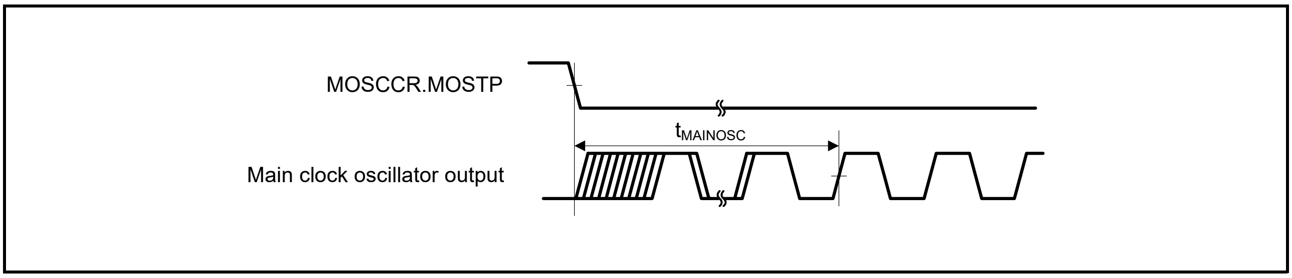


Figure 2.10 Main Clock Oscillation Start Timing

Table 2.33 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation frequency error	Δf_{LOCO}	—	—	±14	%	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 2.11
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation frequency error	Δf_{ILOCO}	—	—	±15	%	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	80	μs	Figure 2.12

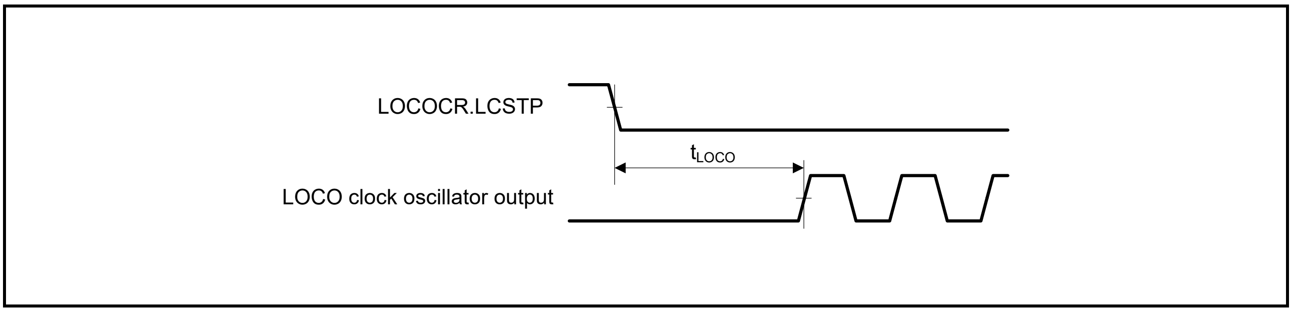


Figure 2.11 LOCO Clock Oscillation Start Timing

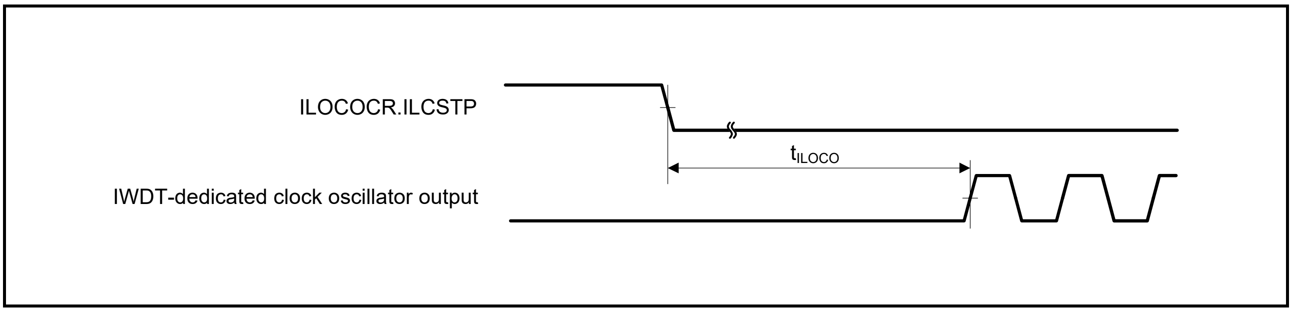


Figure 2.12 IWDT-Dedicated Clock Oscillation Start Timing

Table 2.34 HOCO Clock Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	23.76 (–1.0%)	24	24.24 (+1.0%)	MHz	T_a = –40 to +105°C
		31.68 (–1.0%)	32	32.32 (+1.0%)		
		47.52 (–1.0%)	48	48.48 (+1.0%)		
		63.36 (–1.0%)	64	64.64 (+1.0%)		
HOCO oscillation frequency error	Δf_{HOCO}	—	—	±1.0	%	T_a = –40 to +105°C
HOCO clock oscillation stabilization time	t_{HOCO}	—	—	4.95	μs	Figure 2.14

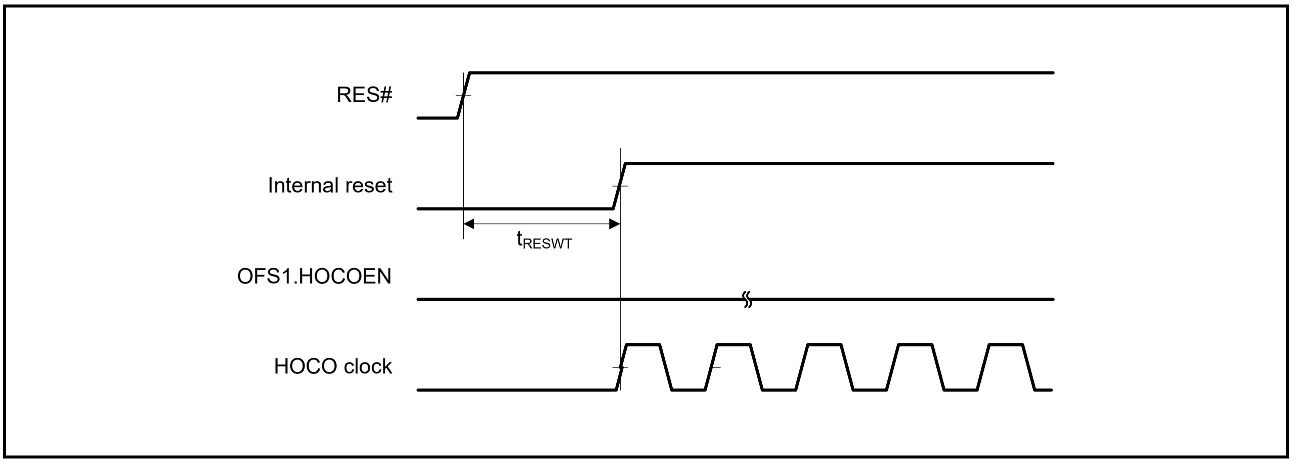


Figure 2.13 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

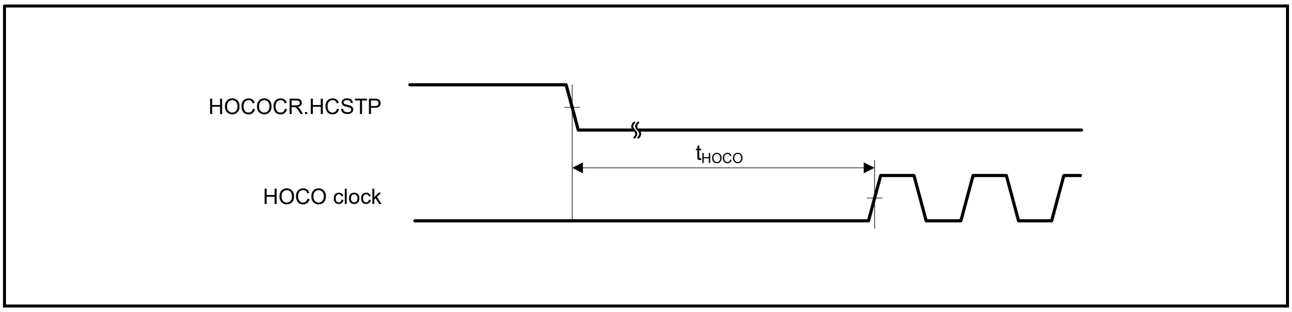


Figure 2.14 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

Table 2.35 PLL Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL input frequency	f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency	f_{PLL}	24	—	64	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	81.4	μs	Figure 2.15
PLL free-running oscillation frequency	f_{PLLFR}	—	9	—	MHz	

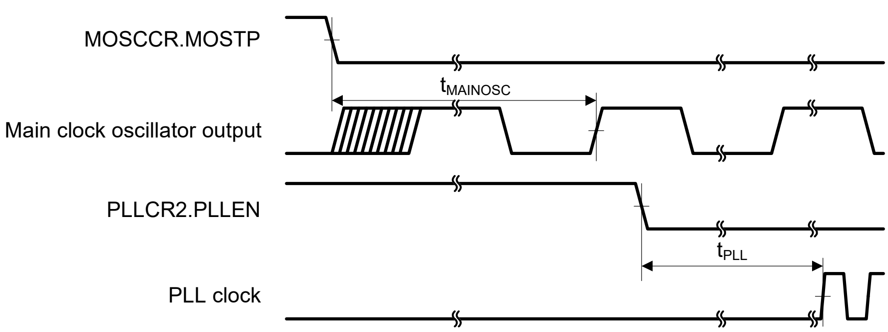


Figure 2.15 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

Table 2.36 PLL2 Clock Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL2 input frequency	f_{PLLIN}	4	—	12.5	MHz	
PLL2 circuit oscillation frequency	f_{PLL}	24	—	64	MHz	
PLL2 clock oscillation stabilization time	t_{PLL}	—	—	81.4	μs	Figure 2.16

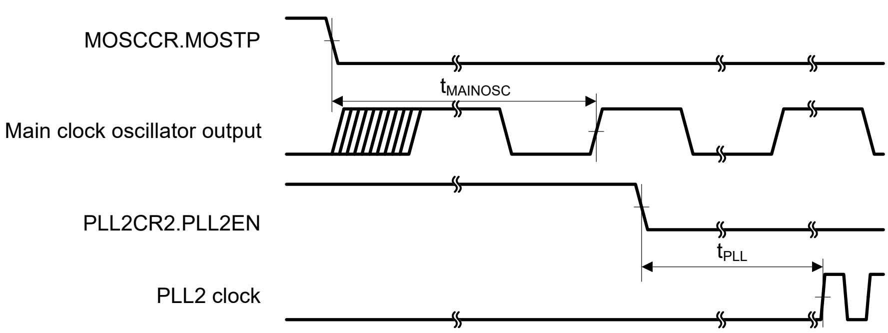


Figure 2.16 PLL2 Clock Oscillation Start Timing (PLL2 is Operated after Main Clock Oscillation Has Settled)

Table 2.37 EXCIN Clock Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXCIN external clock input cycle time	t_{Xcyc}	31.25	—	—	μs	Figure 2.17
EXCIN external clock input high pulse width	t_{XH}	15.62	—	—	μs	
EXCIN external clock input low pulse width	t_{XL}	15.62	—	—	μs	
EXCIN external clock rise time	t_{Xr}	—	—	5.0	ns	
EXCIN external clock fall time	t_{Xf}	—	—	5.0	ns	
EXCIN external clock input wait time*1	t_{XWT}	0.2	—	—	ms	

Note 1. Time until the clock can be used after the sub-clock oscillator stop bit (SOSCCR.SOSTP) is set to 0 (operating).

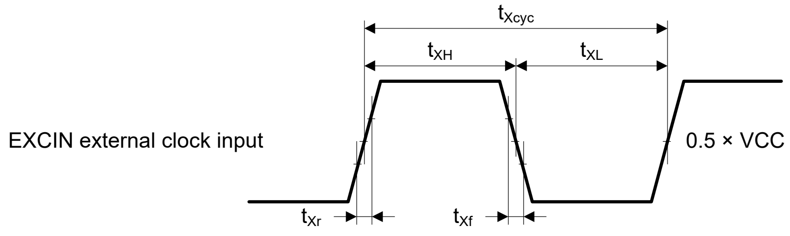


Figure 2.17 EXCIN External Clock Input Timing

Table 2.38 Sub-Clock Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillator oscillation frequency*2	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*1	t_{SUBOSC}	—	0.5	—	s	Figure 2.18

Note 1. Reference value when a 32.768-kHz resonator is used.
After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.

Note 2. Only 32.768-kHz can be used.

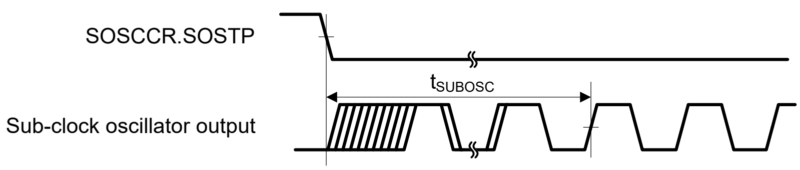


Figure 2.18 Sub-Clock Oscillation Start Timing

2.5.2 Reset Timing

Table 2.39 Reset Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	10.5	—	—	ms	Figure 2.19
	Other than above	t_{RESW}	30	—	—	µs	Figure 2.20
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 2.19
	During fast startup time*2	t_{RESWT}	—	850	—	µs	
Wait time after RES# cancellation (during powered-on state)	LVD0 disabled*3	t_{RESWT}	—	140	—	µs	Figure 2.20
	LVD0 enabled*4		—	850	—	µs	
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)	LVD0 disabled*3	t_{RESWT2}	—	210	—	µs	
	LVD0 enabled*4		—	910	—	µs	

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) = a value other than 11b.
Note 3. When OFS1.LVDAS = 1b.
Note 4. When OFS1.LVDAS = 0b.

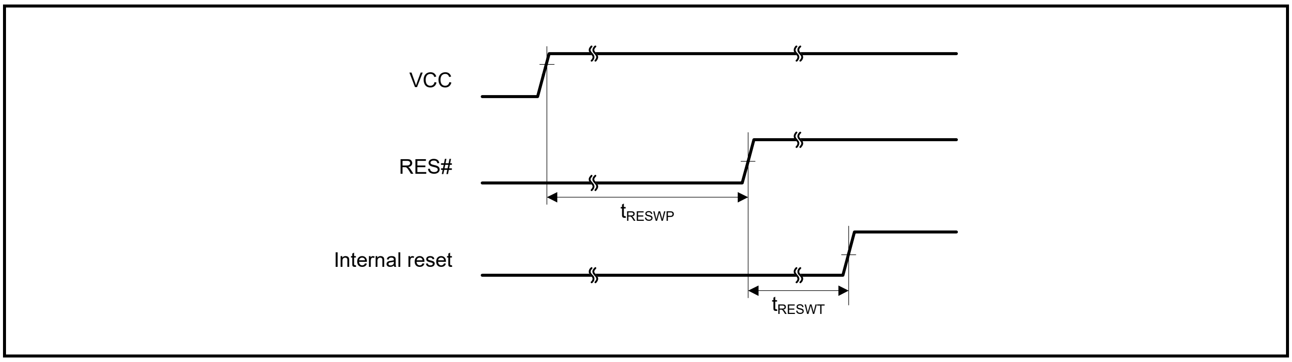


Figure 2.19 Reset Input Timing at Power-On

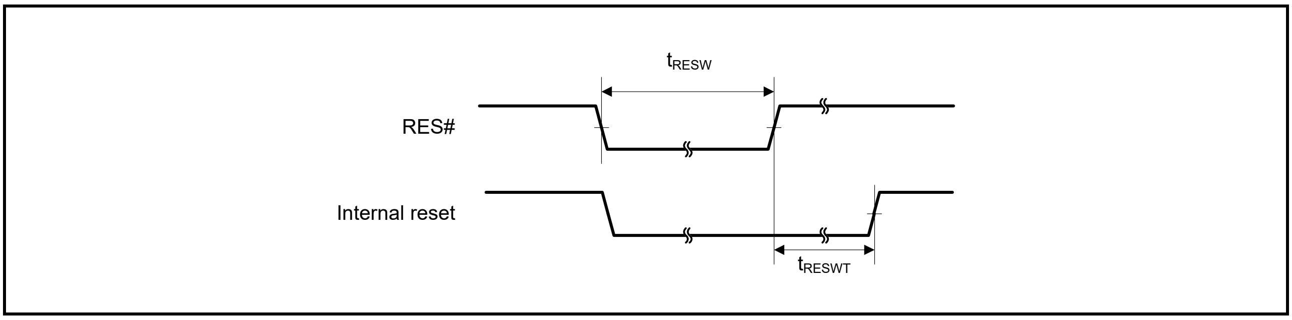


Figure 2.20 Reset Input Timing (1)

2.5.3 Timing of Recovery from Low Power Consumption Modes

Table 2.40 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
The oscillation stabilization wait time*1	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	$0.65 + t_{LOCO}$ + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	μs	
			Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	$0.65 + t_{LOCO}$ + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
		Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	$0.65 + 3 / f_{SOSC} + 1 / f_{ICLK}$		
		High-speed on-chip oscillator		$t_{SBYOSCWTHO}$	—	—	$0.65 + t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}$		
		Low-speed on-chip oscillator		$t_{SBYOSCWTLO}$	—	—	$0.65 + t_{LOCO} + 1 / f_{ICLK}$		
The time required for operations by the software standby release sequencer*2				t_{SBYSEQ}	—	—	$4 / f_{LOCO} + 11 / f_{ICLK} + 3 / f_{PCLKB} + 3n / f_{source\ clock}$		
Recovery time from software standby mode*3	High-speed operating mode/ Middle-speed operating mode	Main clock oscillator operating	Main clock oscillator operating	t_{SBYMC}	—	—	$t_{SBYOSCWTMC} + t_{SBYSEQ}$		Figure 2.21
			Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	$t_{SBYOSCWTPC} + t_{SBYSEQ}$		
		Sub-clock oscillator operating		t_{SBYSC}	—	—	$t_{SBYOSCWTSC} + t_{SBYSEQ}$		
		High-speed on-chip oscillator		t_{SBYHO}	—	—	$t_{SBYOSCWTHO} + t_{SBYSEQ}$		
		Low-speed on-chip oscillator		t_{SBYLO}	—	—	$t_{SBYOSCWTLO} + t_{SBYSEQ}$		

Note 1. When multiple oscillators are operating before entering software standby mode, the oscillation stabilization wait time will be selected from the largest value among the operating oscillators.

Note 2. For n, the greatest value is selected from among the internal clock division settings.

Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time and the time required for operations by the software standby release sequencer.

Table 2.41 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
The oscillation stabilization wait time*1	Middle-speed operating mode 2	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	0.65 + t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	μs	
			Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	0.65 + t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
		Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	0.65 + 3 / f_{SOSC} + 1 / f_{ICLK}		
		High-speed on-chip oscillator		$t_{SBYOSCWTHO}$	—	—	0.65 + t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
		Low-speed on-chip oscillator		$t_{SBYOSCWTLO}$	—	—	0.65 + t_{LOCO} + 1 / f_{ICLK}		
The time required for operations by the software standby release sequencer*2				t_{SBYSEQ}	—	—	9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / $f_{source\ clock}$		
Recovery time from software standby mode*3	Middle-speed operating mode 2	Main clock oscillator operating	Main clock oscillator operating	t_{SBYMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 2.21
			Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
		Sub-clock oscillator operating		t_{SBYSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
		High-speed on-chip oscillator		t_{SBYHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
		Low-speed on-chip oscillator		t_{SBYLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entering software standby mode, the oscillation stabilization wait time will be selected from the largest value among the operating oscillators.

Note 2. For n, the greatest value is selected from among the internal clock division settings.

Note 3. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time and the time required for operations by the software standby release sequencer.

Table 2.42 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
The oscillation stabilization wait time*1	Low-speed operating mode	Sub-clock oscillator operating	$t_{SBYOSCWTSC}$	—	—	$0.65 + 3 / f_{SOSC} + 1 / f_{ICLK}$	μs	
The time required for operations by the software standby release sequencer*1			t_{SBYSEQ}	—	—	$9 / f_{ICLK} + 3 / f_{PCLKB} + 3n / f_{source\ clock}$		
Recovery time from software standby mode*2	Low-speed operating mode	Sub-clock oscillator operating	t_{SBYSC}	—	—	$t_{SBYOSCWTSC} + t_{SBYSEQ}$		Figure 2.21

Note 1. For n, the greatest value is selected from among the internal clock division settings.
Note 2. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time and the time required for operations by the software standby release sequencer.

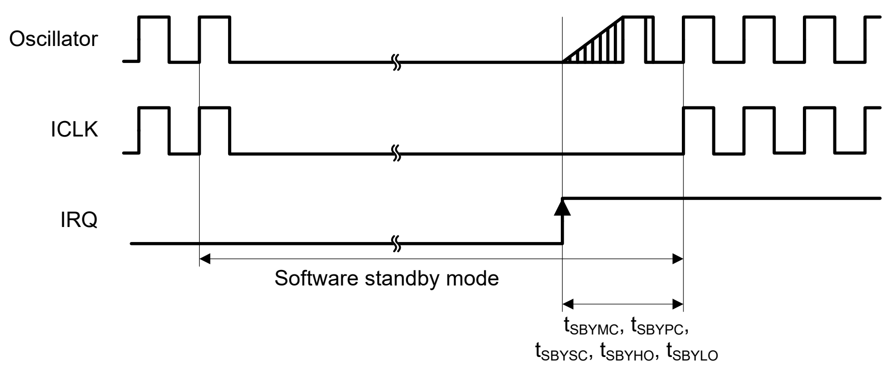


Figure 2.21 Software Standby Mode Recovery Timing

Table 2.43 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
The oscillation stabilization wait time*1	Main clock oscillator operating	Main clock oscillator operating	$t_{SBYOSCWTMC}$	—	—	0.65 + t_{LOCO} + (16 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{MOSC} + 1 / f_{ICLK}	μs	
		Main clock oscillator and PLL circuit operating	$t_{SBYOSCWTPC}$	—	—	0.65 + t_{LOCO} + (288 + Number of cycles specified in MOSCWTCR) / f_{LOCO} + 2 / f_{PLL} + 1 / f_{ICLK}		
	Sub-clock oscillator operating		$t_{SBYOSCWTSC}$	—	—	0.65 + 3 / f_{SOSC} + 1 / f_{ICLK}		
	High-speed on-chip oscillator		$t_{SBYOSCWTHO}$	—	—	0.65 + t_{LOCO} + 16 / f_{LOCO} + 2 / f_{HOCO} + 1 / f_{ICLK}		
	Low-speed on-chip oscillator		$t_{SBYOSCWTLO}$	—	—	0.65 + t_{LOCO} + 1 / f_{ICLK}		
The time required for operations by the software standby release sequencer*2			t_{SBYSEQ}	—	—	3 / f_{ICLK} + 2n / $f_{source\ clock}$		
Time to shift to the snooze mode from the software standby mode*3	Main clock oscillator operating	Main clock oscillator operating	t_{SNZMC}	—	—	$t_{SBYOSCWTMC}$ + t_{SBYSEQ}		Figure 2.22
		Main clock oscillator and PLL circuit operating	t_{SNZPC}	—	—	$t_{SBYOSCWTPC}$ + t_{SBYSEQ}		
	Sub-clock oscillator operating		t_{SNZSC}	—	—	$t_{SBYOSCWTSC}$ + t_{SBYSEQ}		
	High-speed on-chip oscillator		t_{SNZHO}	—	—	$t_{SBYOSCWTHO}$ + t_{SBYSEQ}		
	Low-speed on-chip oscillator		t_{SNZLO}	—	—	$t_{SBYOSCWTLO}$ + t_{SBYSEQ}		

Note 1. When multiple oscillators are operating before entering software standby mode, the oscillation stabilization wait time will be selected from the largest value among the operating oscillators.

Note 2. For n, the greatest value is selected from among the internal clock division settings.

Note 3. Time to shift to the snooze mode from the software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time and the time required for operations by the software standby release sequencer.

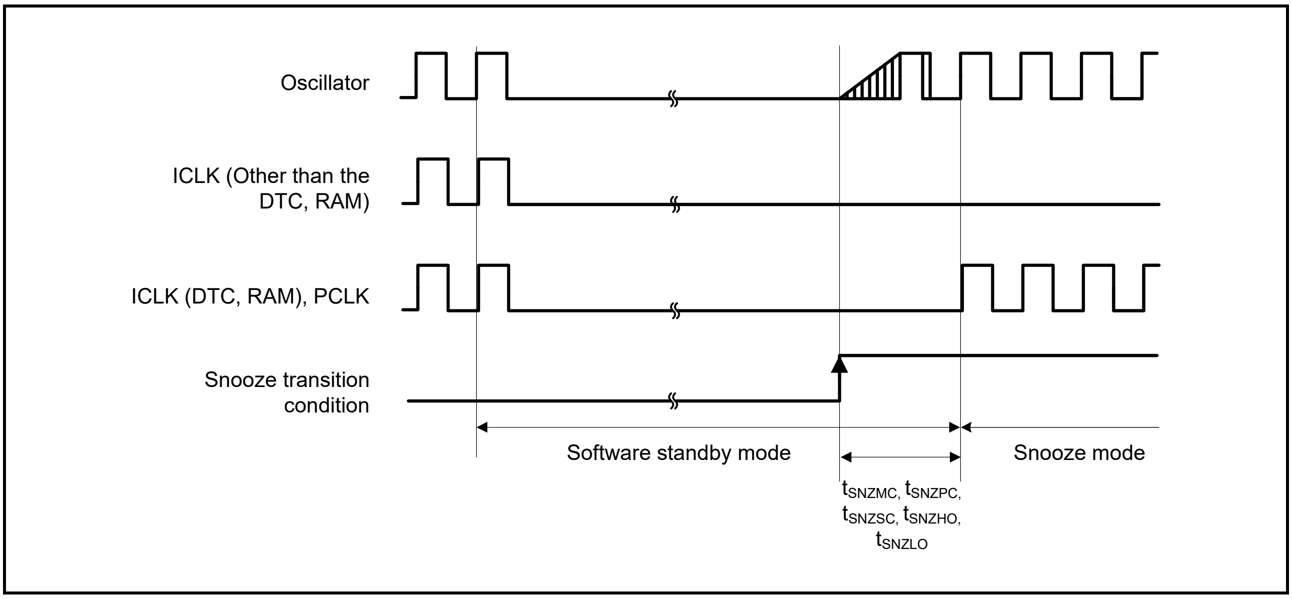


Figure 2.22 Timing to shift to the Snooze Mode from the Software Standby Mode

Table 2.44 Timing of Recovery from Low Power Consumption Modes (5)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.*2	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed operating mode	t_{DSLP}	—	—	$4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$	μs	Figure 2.23
	Middle-speed operating mode				$4 / f_{LOCO} + 8 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$		
	Middle-speed operating mode 2				$6 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$		
	Low-speed operating mode				$6 / f_{ICLK} + 2 / f_{PCLKB} + 3n / f_{source\ clock}$		

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. n represents the largest frequency divisor among those for the internal clock signals.

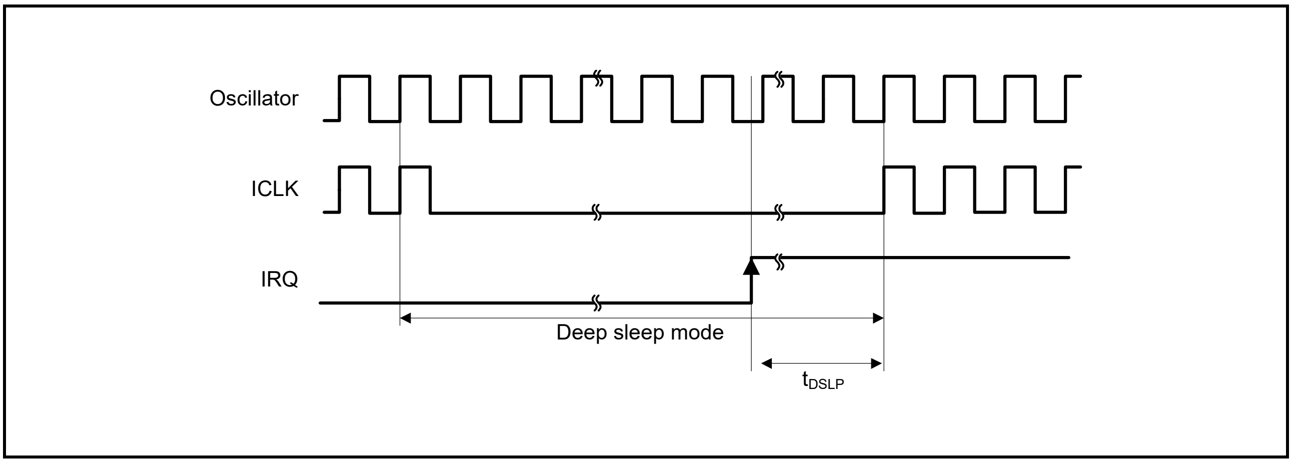


Figure 2.23 Deep Sleep Mode Recovery Timing

2.5.4 Operating Mode Transition Time

Table 2.45 Operating Mode Transition Time

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Mode before Transition	Mode after Transition	Transition Time				Unit
		Min.	Typ.		Max.	
			$f_{ICLK} \geq f_{FCLK}$	$f_{ICLK} < f_{FCLK}$		
High-speed operating mode	Middle-speed operating mode	—	$5 / f_{ICLK} + 3 / f_{FCLK}$	$8 / f_{ICLK}$	—	μs
	Middle-speed operating mode 2	—	$5 / f_{ICLK} + 3 / f_{FCLK}$	$8 / f_{ICLK}$	—	
	Low-speed operating mode	—	$3 / f_{ICLK} + 2 / f_{FCLK}$	$5 / f_{ICLK}$	—	
Middle-speed operating mode	High-speed operating mode	—	$5 / f_{ICLK} + 3 / f_{FCLK}$	$8 / f_{ICLK}$	—	
	Middle-speed operating mode 2	—	$5 / f_{ICLK} + 3 / f_{FCLK}$	$8 / f_{ICLK}$	—	
	Low-speed operating mode	—	$3 / f_{ICLK} + 2 / f_{FCLK}$	$5 / f_{ICLK}$	—	
Middle-speed operating mode 2	High-speed operating mode	—	$5 / f_{ICLK} + 3 / f_{FCLK}$	$8 / f_{ICLK}$	—	
	Middle-speed operating mode	—	$5 / f_{ICLK} + 3 / f_{FCLK}$	$8 / f_{ICLK}$	—	
	Low-speed operating mode	—	$3 / f_{ICLK} + 2 / f_{FCLK}$	$5 / f_{ICLK}$	—	
Low-speed operating mode	High-speed operating mode	—	$3 / f_{ICLK} + 3 / f_{FCLK}$	$6 / f_{ICLK}$	—	
	Middle-speed operating mode	—	$3 / f_{ICLK} + 3 / f_{FCLK}$	$6 / f_{ICLK}$	—	
	Middle-speed operating mode 2	—	$3 / f_{ICLK} + 3 / f_{FCLK}$	$6 / f_{ICLK}$	—	

2.5.5 Control Signal Timing

Table 2.46 Control Signal Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{PBcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{PBcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{PBcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

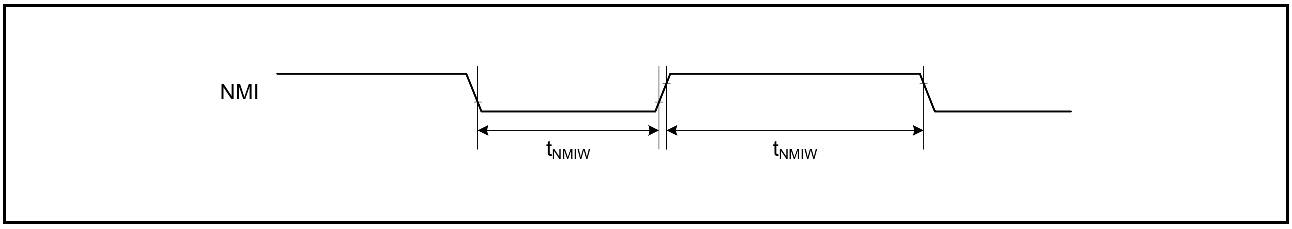


Figure 2.24 NMI Interrupt Input Timing

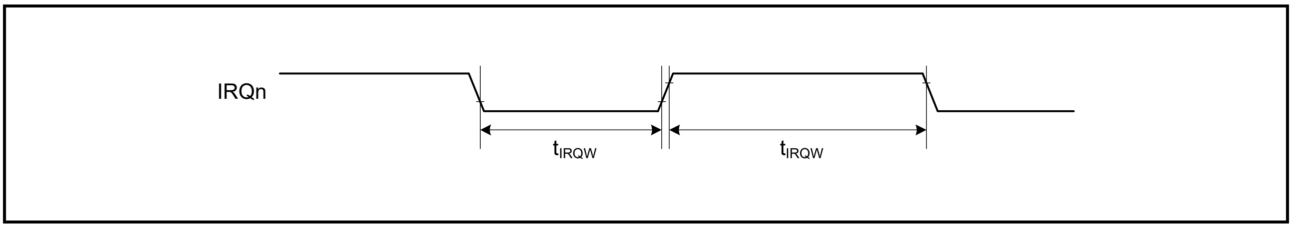


Figure 2.25 IRQ Interrupt Input Timing

2.5.6 Timing of On-Chip Peripheral Modules

2.5.6.1 I/O Port Input Timing

Table 2.47 I/O Port Input Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.26

Note 1. t_{PBcyc}: PCLKB cycle

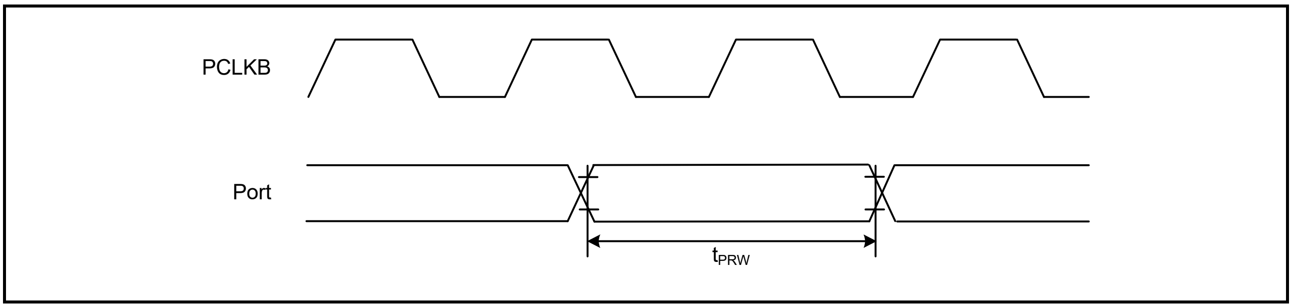


Figure 2.26 I/O Port Input Timing

2.5.6.2 GPTW

Table 2.48 GPTW Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
GPTW	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 2.27
		Both-edge setting		2.5	—		
	Input capture rise/fall time		t_{GTICr}/ t_{GTICf}	—	0.1	μs/V	Figure 2.27
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PAcyc}	Figure 2.28
		Both-edge setting		2.5	—		
	Timer clock pulse width		t_{GTCKWH}	1.5	—	t_{PAcyc}	Figure 2.29
			t_{GTCKWL}				
	Timer clock rise/fall time		t_{GTCKr}/ t_{GTCKf}	—	0.1	μs/V	Figure 2.29

Note 1. t_{PAcyc}: PCLKA cycle

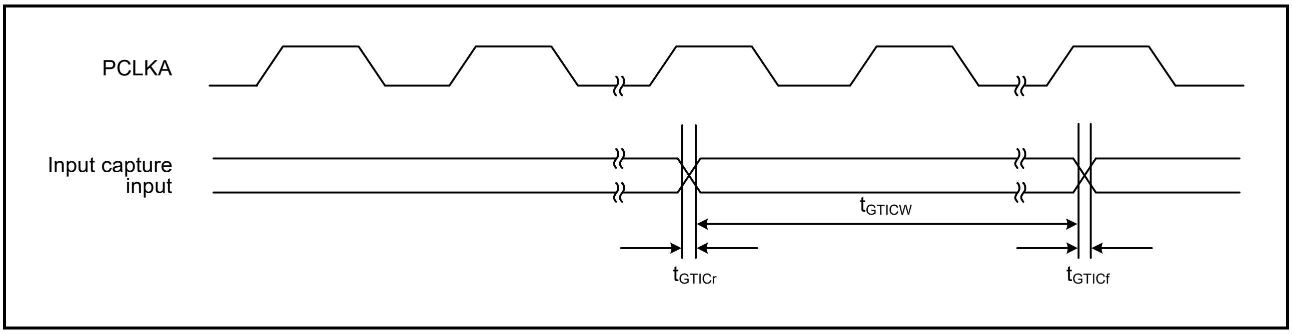


Figure 2.27 GPTW Input Capture Input Timing

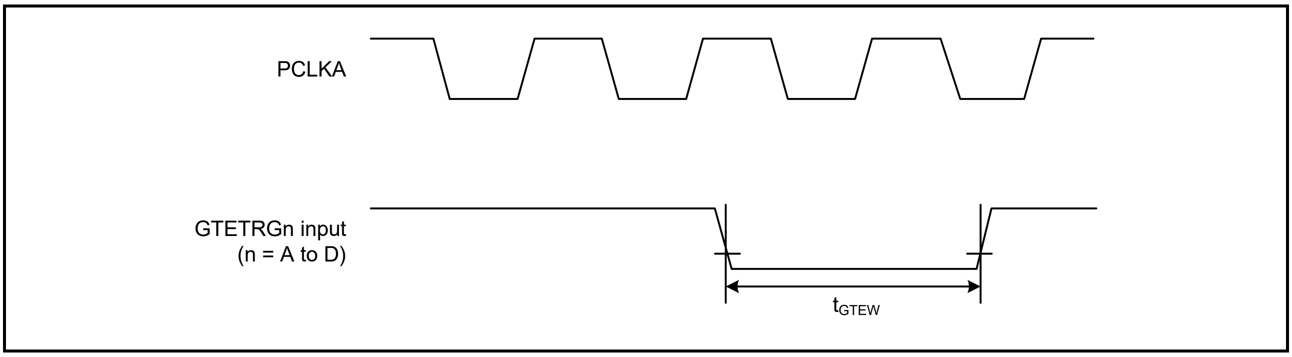


Figure 2.28 GPTW External Trigger Input Timing

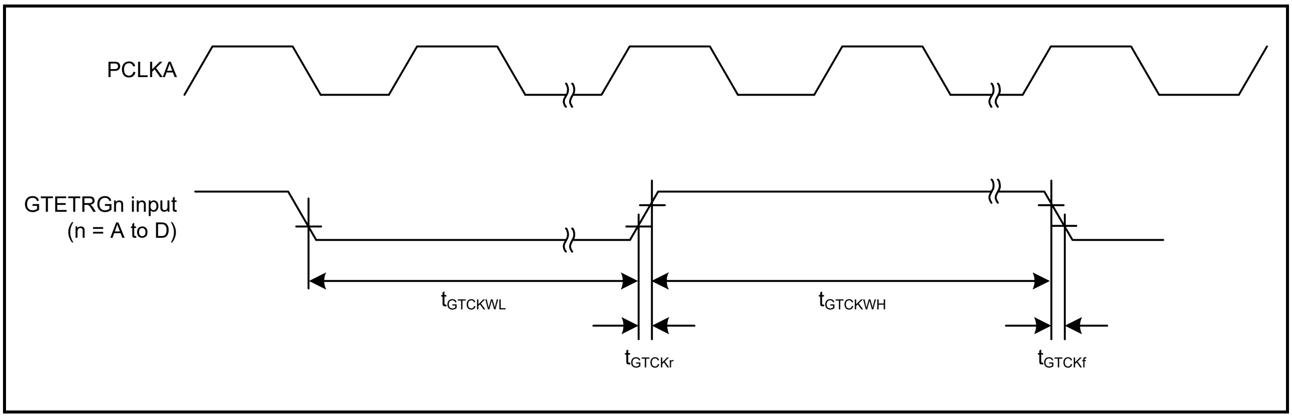


Figure 2.29 GPTW Clock Input Timing

2.5.6.3 POEG

Table 2.49 POEG Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	1.5	—	—	t_{PBcyc}	Figure 2.30
	GTERGn input rise/fall time		t_{POEGr}/ t_{POEGf}	—	—	0.1	μs/V	Figure 2.30
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	μs	Figure 2.31 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPTW (simultaneous high output or simultaneous low output)	t_{POEGDE}	—	—	0.5	μs	Figure 2.32
		Edge detection signal from a comparator	t_{POEGDC}	—	—	4 PCLKB + 0.5	μs	Figure 2.33 The time is that when the noise filter for comparator B is not in use (CPBF.CPB0FEN = 0 and CPBF.CPB1FEN = 0) and excludes the time for detection by comparator B.
		Register setting	t_{POEGDS}	—	—	1 PCLKB + 0.3	μs	Figure 2.34 Time for access to the register is not included.
		Oscillation stop detection	$t_{POEGDOS}$	—	—	21	μs	Figure 2.35

Note 1. t_{PBcyc}: PCLKB cycle

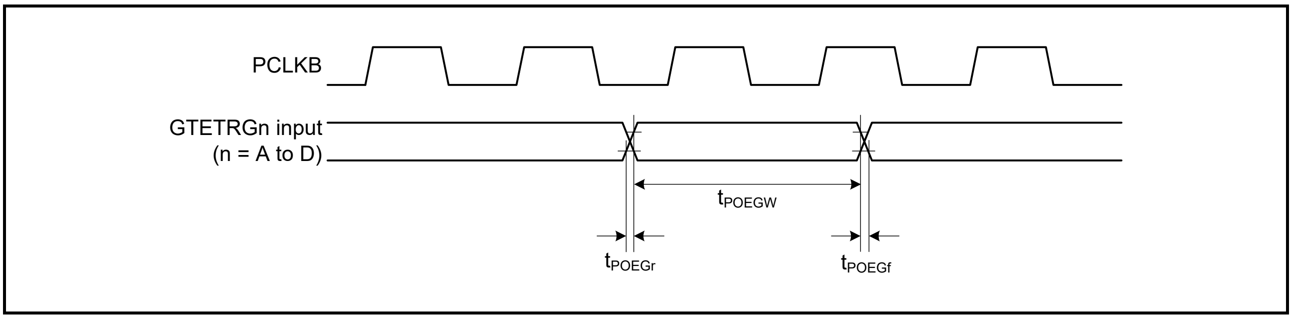


Figure 2.30 POEG Input Timing

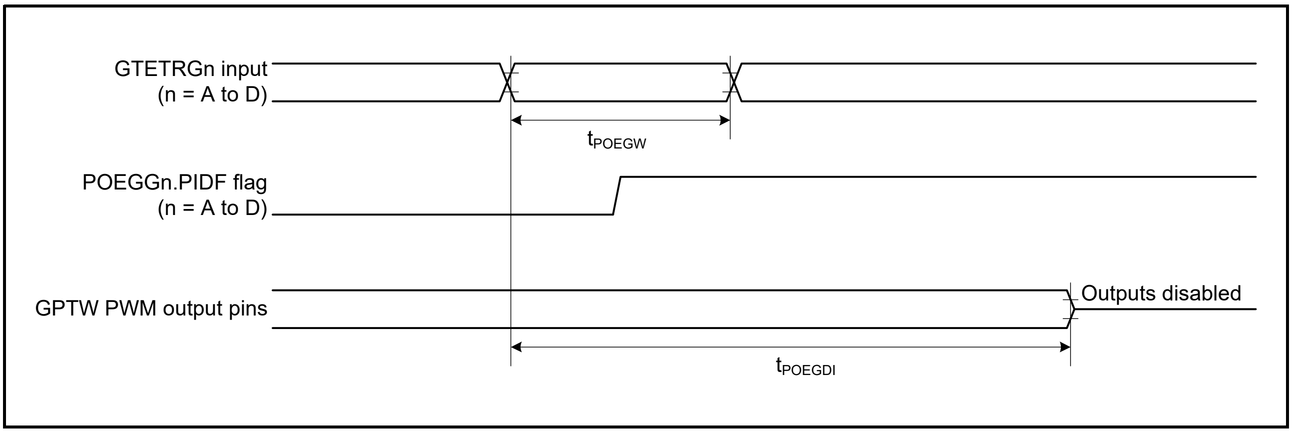


Figure 2.31 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin

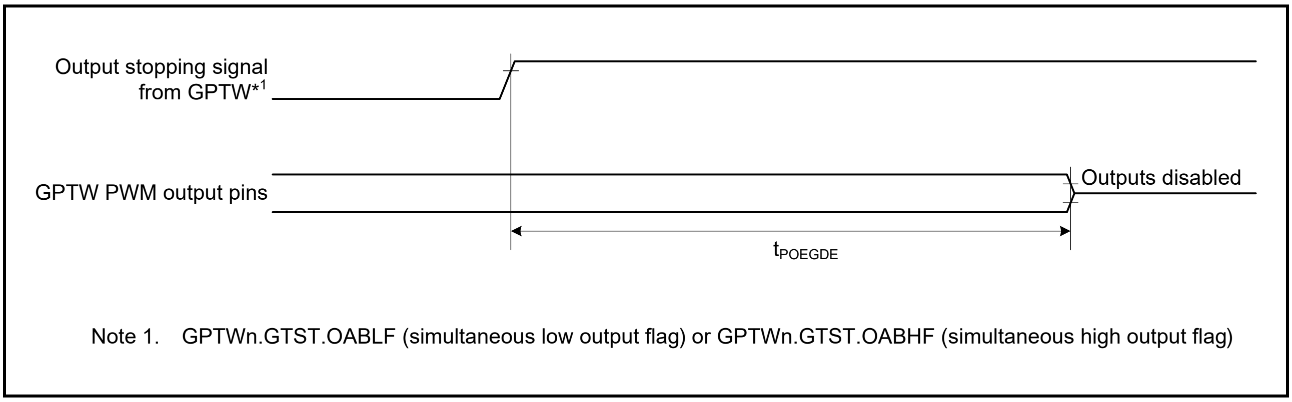


Figure 2.32 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

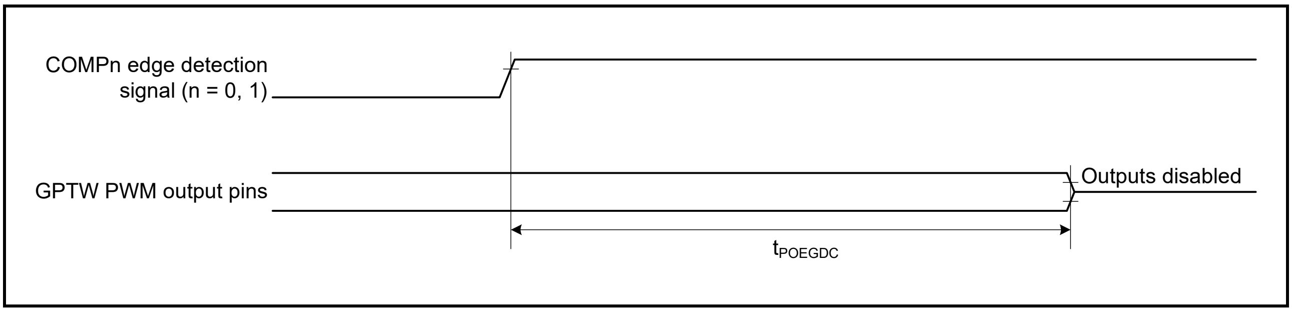


Figure 2.33 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

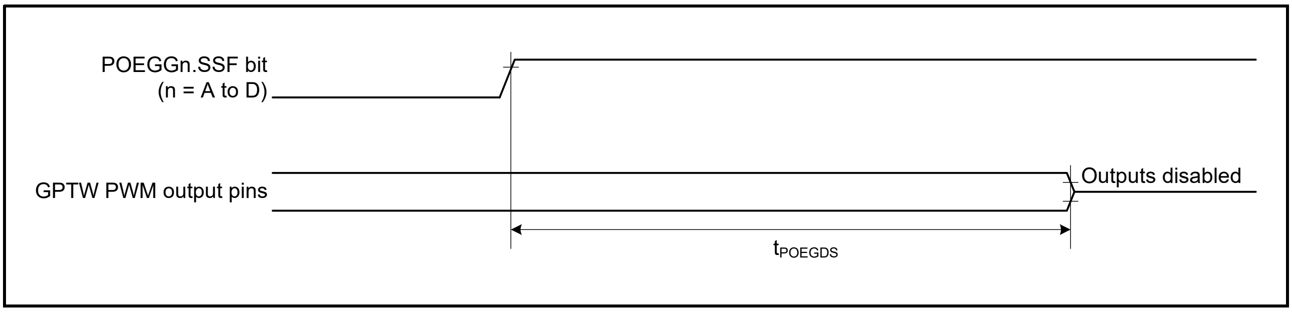


Figure 2.34 Output Disable Time for POEG in Response to the Register Setting

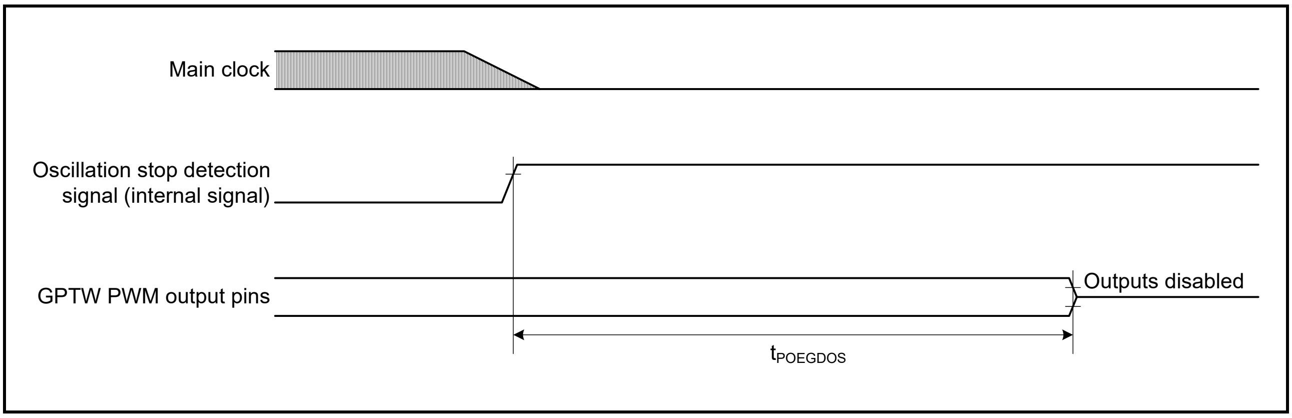


Figure 2.35 Output Disable Time of POEG in Response to the Oscillation Stop Detection

2.5.6.4 TMR

Table 2.50 TMR Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.36
		Both-edge setting		2.5	—		
	Timer clock rise/fall time		t_{TMCr}, t_{TMCf}	—	0.1	μs/V	

Note 1. t_{PBcyc}: PCLKB cycle

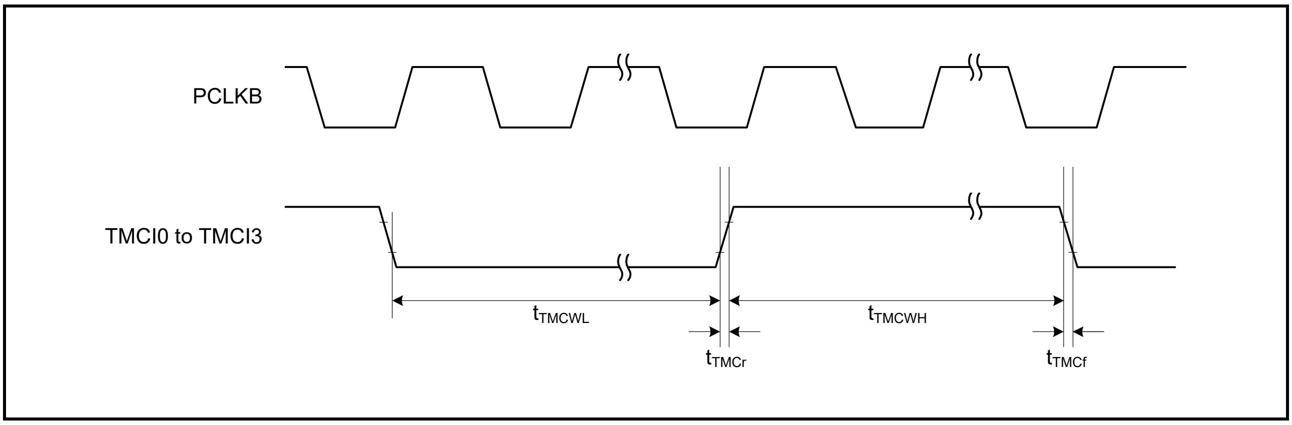


Figure 2.36 TMR Clock Input Timing

2.5.6.5 SCI

Table 2.51 SCI Timing (1/2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
SCI (channel 1, 5, 6)	Input clock cycle time	Asynchronous		t_{Scyc}	4	—	t_{PBcyc}	Figure 2.37
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		6	—		
			1.8 V ≤ VCC < 2.4 V		8	—		
			1.6 V ≤ VCC < 1.8 V		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous		t_{Scyc}	6	—	t_{PBcyc}	Figure 2.38
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		4	—		
			1.8 V ≤ VCC < 2.4 V		8	—		
			1.6 V ≤ VCC < 1.8 V		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	45	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60	ns	
			1.8 V ≤ VCC < 2.4 V		—	100	ns	
			1.6 V ≤ VCC < 1.8 V		—	125	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—	ns	
			1.8 V ≤ VCC < 2.4 V		90	—	ns	
			1.6 V ≤ VCC < 1.8 V		110	—	ns	
	Receive data setup time (slave)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 1.8 V		45	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

Table 2.51 SCI Timing (2/2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
SCI (channel 12)	Input clock cycle time	Asynchronous		t_{Scyc}	4	—	t_{PBcyc}	Figure 2.37
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		6	—		
			1.8 V ≤ VCC < 2.4 V		8	—		
			1.6 V ≤ VCC < 1.8 V		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous*2		t_{Scyc}	8	—	t_{PBcyc}	Figure 2.38
		Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		4	—		
			1.8 V ≤ VCC < 2.4 V		8	—		
			1.6 V ≤ VCC < 1.8 V		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	45	ns	
	Transmit data delay time (slave)	Clock synchronous	2.4 V ≤ VCC ≤ 5.5 V		—	65	ns	
			1.8 V ≤ VCC < 2.4 V		—	100	ns	
			1.6 V ≤ VCC < 1.8 V		—	125	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—	ns	
			1.8 V ≤ VCC < 2.4 V		90			
			1.6 V ≤ VCC < 1.8 V		110	—	ns	
	Receive data setup time (slave)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 1.8 V		45	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. When SEMR.ABCS = 1 and SEMR.BGDM = 1

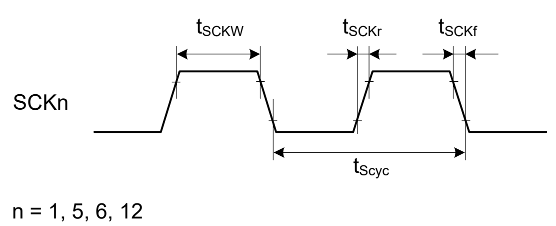


Figure 2.37 SCK Clock Input Timing

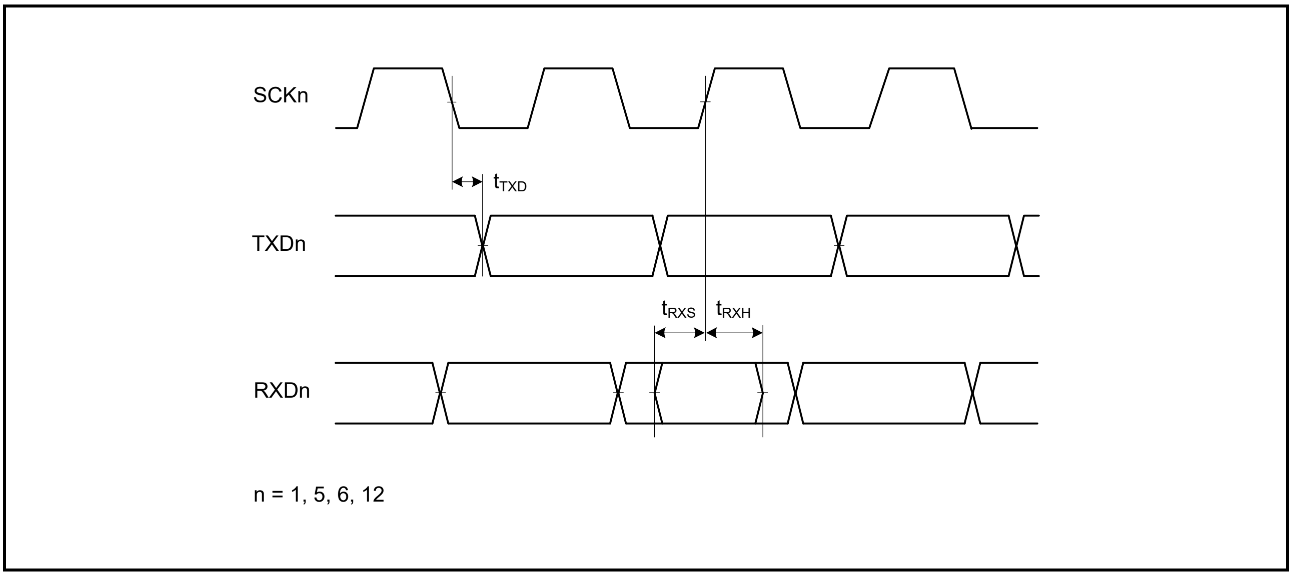


Figure 2.38 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.52 Simple I²C Timing

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 2.39
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple I²C (fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 2.39
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{PBcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{PBcyc}: PCLKB cycle
Note 1. C_b is the total capacitance of the bus lines.

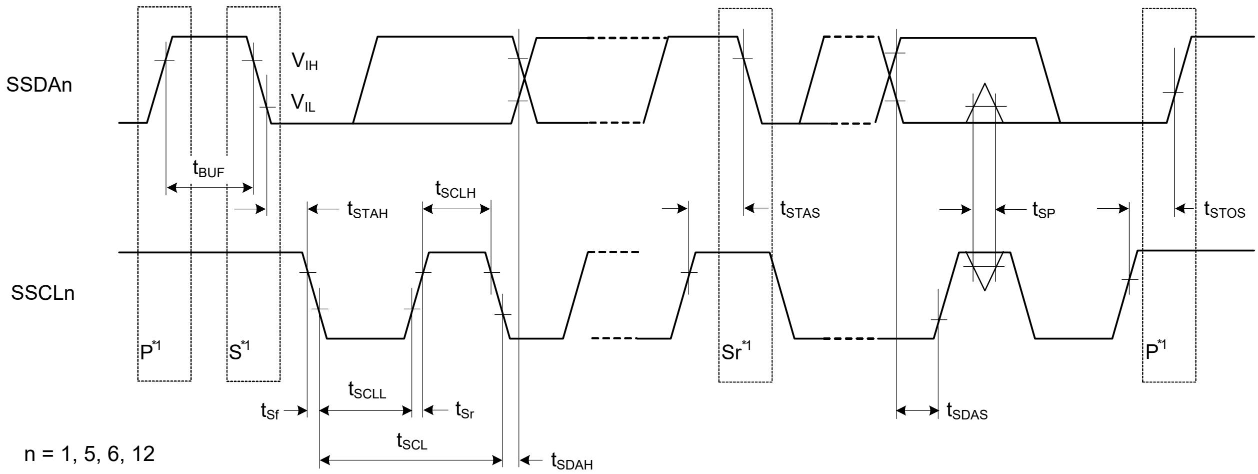


Figure 2.39 Output Timing and Simple I²C Bus Interface Input/Output Timing

Table 2.53 Simple SPI Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		2.4 V ≤ VCC ≤ 5.5 V	t_{SPBcyc}	4	65536	t_{PBcyc}	Figure 2.40
			1.8 V ≤ VCC < 2.4 V		8	65536		
			1.6 V ≤ VCC < 1.8 V		4	65536		
	SCK clock cycle input (slave)		2.4 V ≤ VCC ≤ 5.5 V	t_{SPBcyc}	6	—	t_{PBcyc}	
			1.8 V ≤ VCC < 2.4 V		8	—		
			1.6 V ≤ VCC < 1.8 V		6	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPBcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPBcyc}	
	SCK clock rise/fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Data input setup time (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 2.41, Figure 2.42
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Data input setup time (slave)		1.8 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 1.8 V		45	—		
	Data input hold time			t_H	40	—	ns	
	SSL input setup time			t_{LEAD}	1	—	t_{SPBcyc}	
	SSL input hold time			t_{LAG}	1	—	t_{SPBcyc}	
	Data output delay time (master)		1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
	Data output delay time (slave)		2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	–10	—	ns	
			1.8 V ≤ VCC < 2.7 V		–20	—		
			1.6 V ≤ VCC < 1.8 V		–40	—		
	Data output hold time (slave)				–10	—		
	Data rise/fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	SSL input rise/fall time			t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{PBcyc}	Figure 2.43, Figure 2.44
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		—	7		
			PCLKB ≤ 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{PBcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		—	7		
			PCLKB ≤ 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

Note 1. t_{PBcyc}: PCLKB cycle

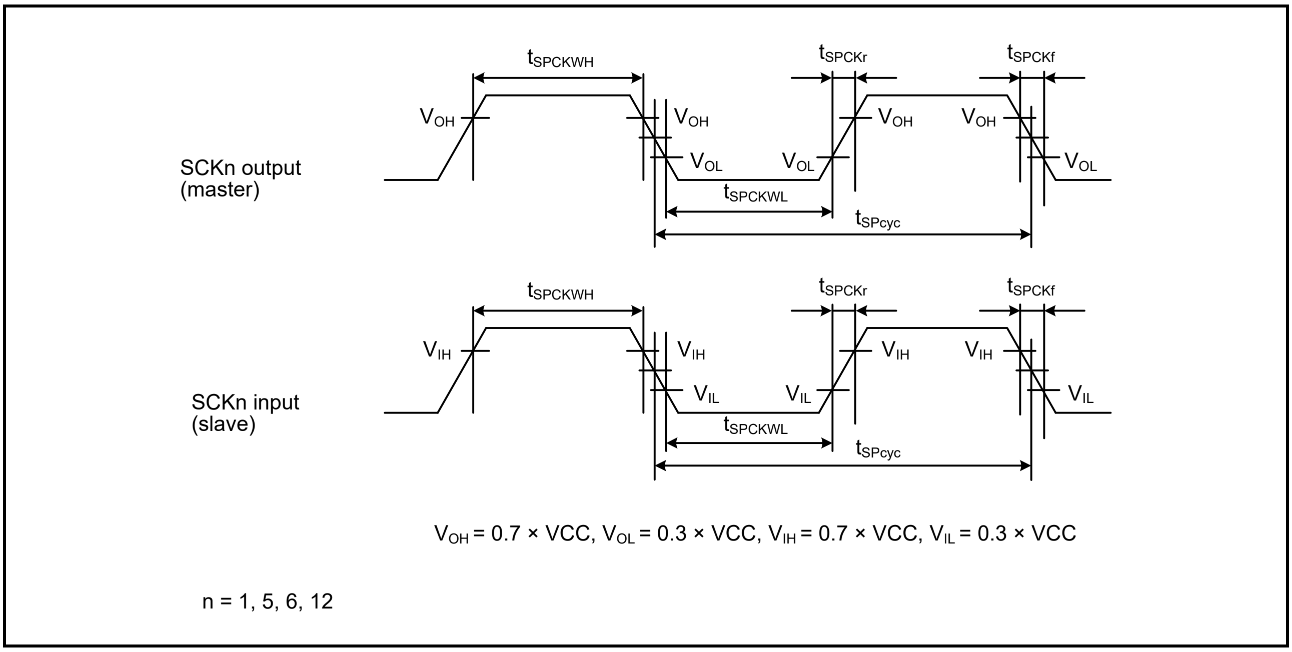


Figure 2.40 Simple SPI Clock Timing

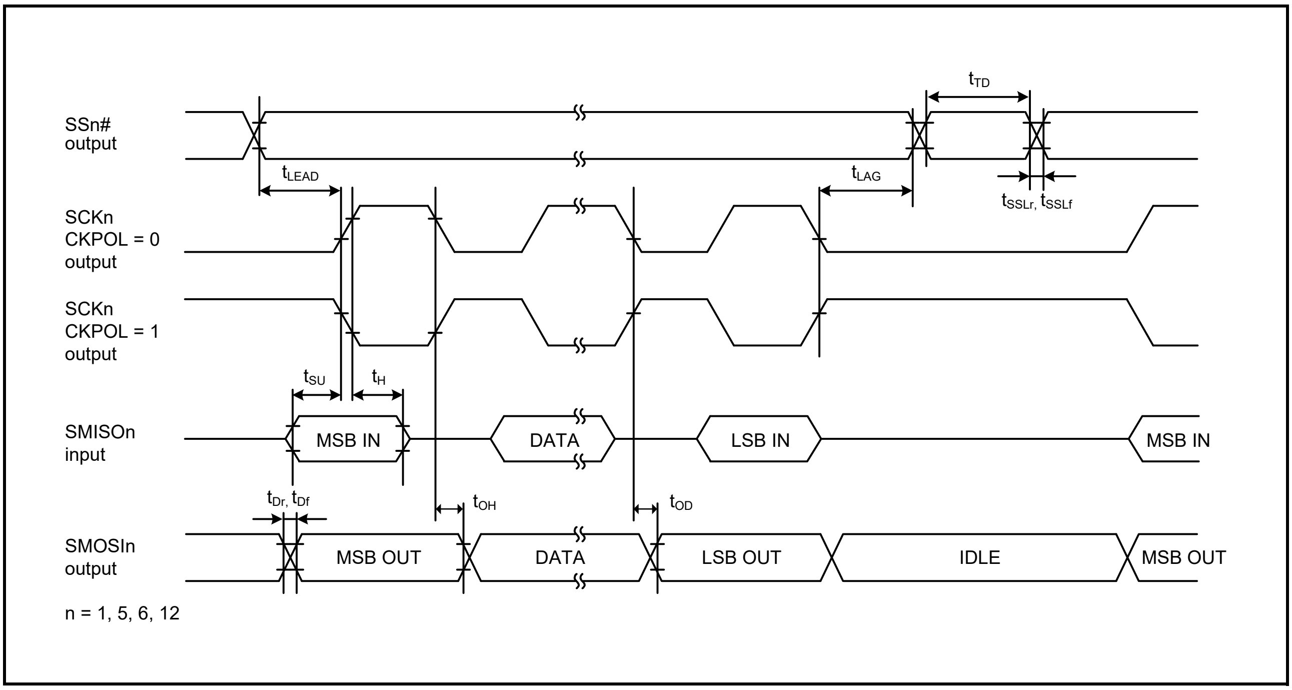


Figure 2.41 Simple SPI Clock Timing (Master, CKPH = 1)

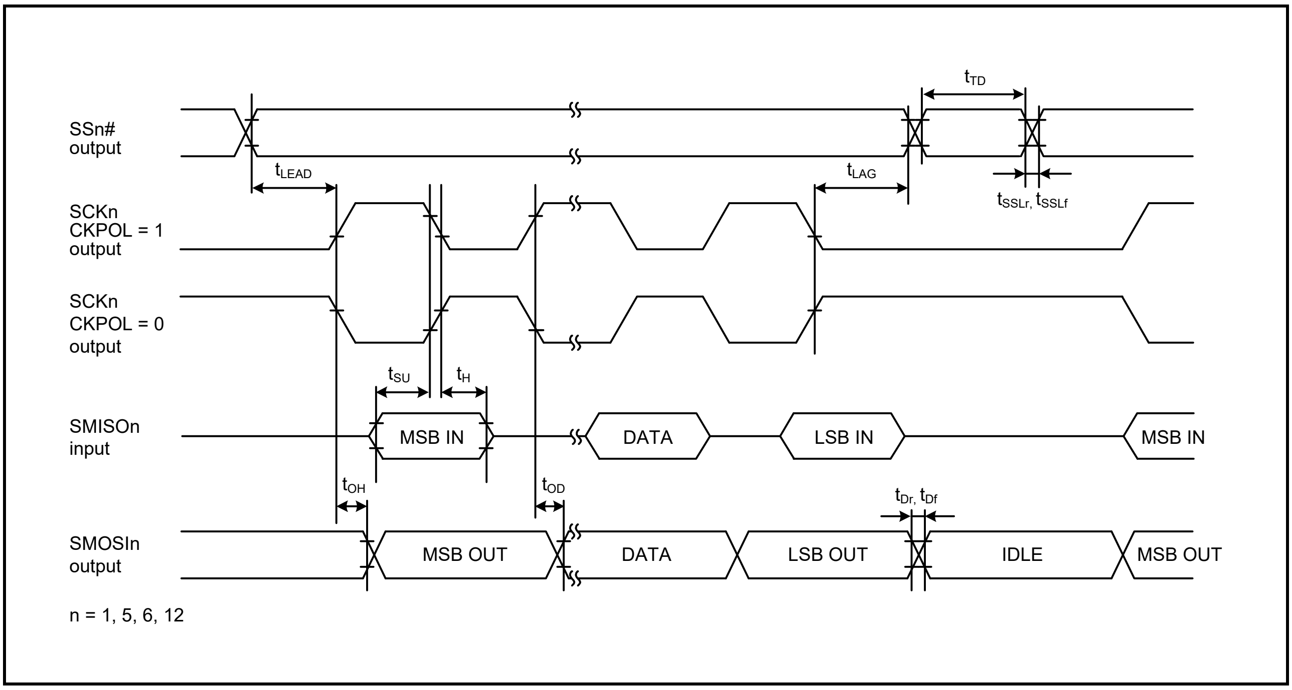


Figure 2.42 Simple SPI Clock Timing (Master, CKPH = 0)

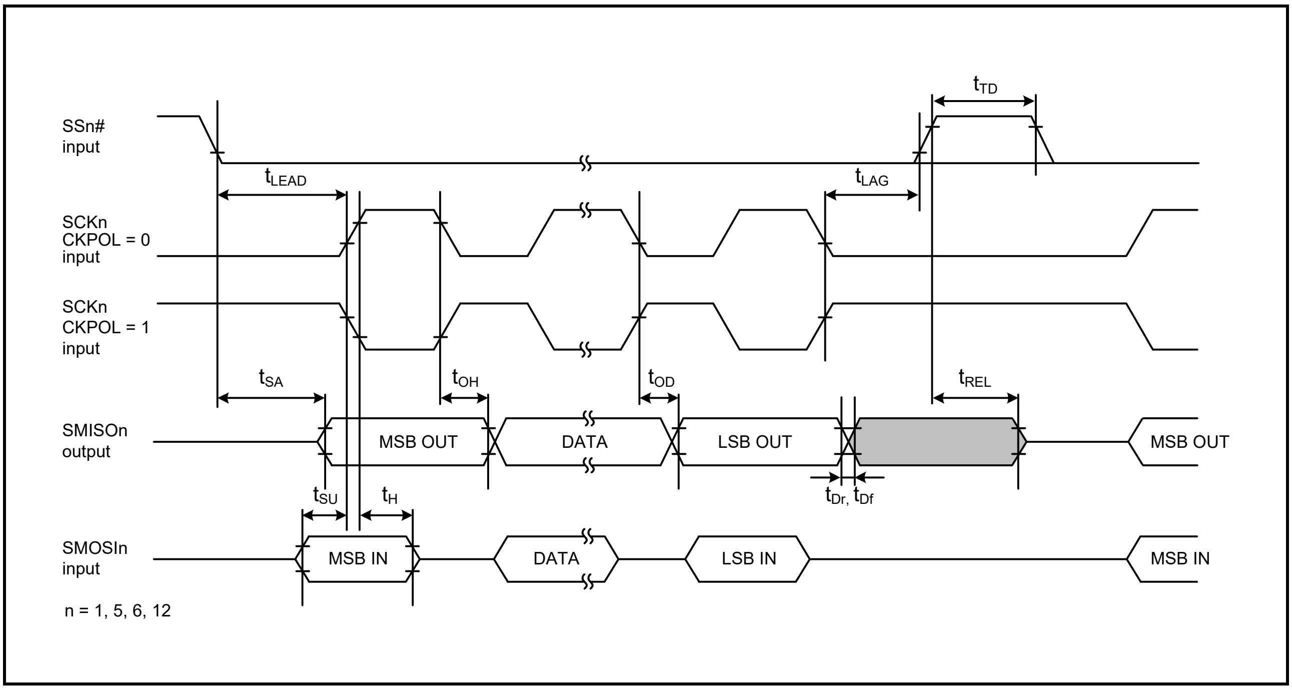


Figure 2.43 Simple SPI Clock Timing (Slave, CKPH = 1)

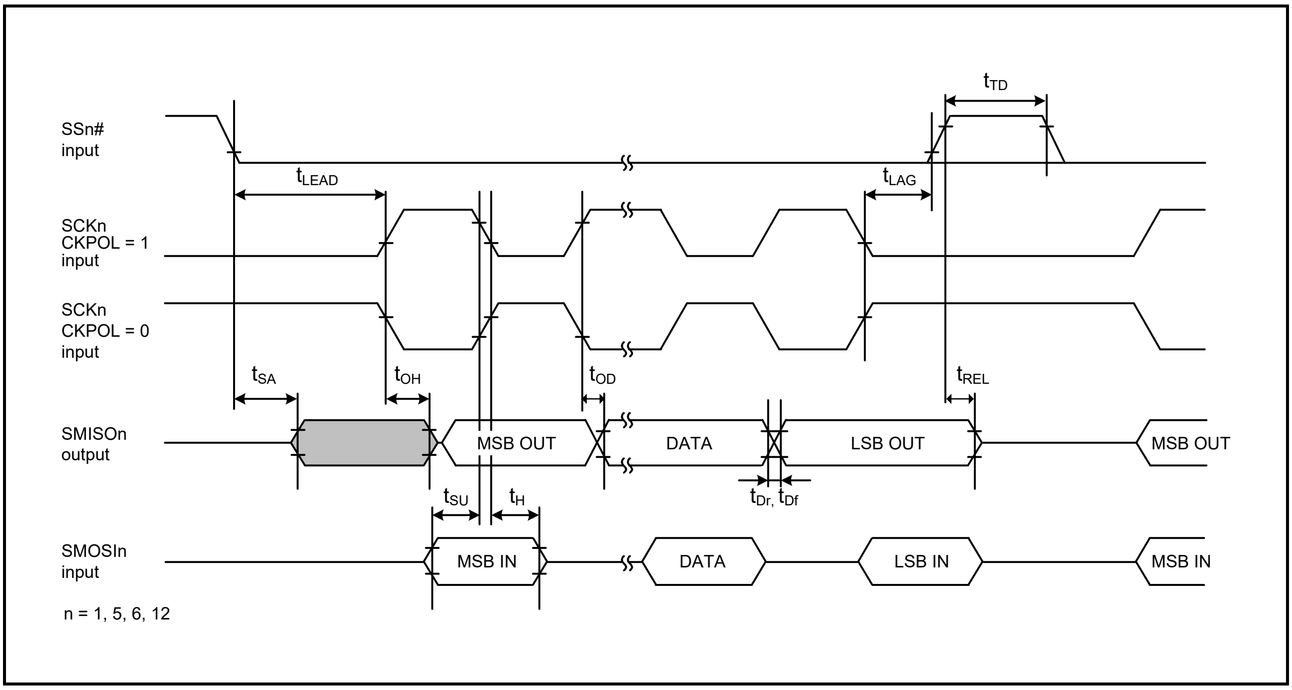


Figure 2.44 Simple SPI Clock Timing (Slave, CKPH = 0)

2.5.6.6 RSCI

Table 2.54 RSCI Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF

Item					Symbol	Min.	Max.	Unit *1	Test Conditions
RSCI (channel 0, 8, 9)	Input clock cycle time	Asynchronous			t_{Scyc}	4	—	t_{PBcyc}	Figure 2.45
		Clock synchronous	4.5 V ≤ VCC ≤ 5.5 V	24 MHz < PCLKB ≤ 32 MHz		4	—		
				PCLKB ≤ 24 MHz		2	—		
			2.4 V ≤ VCC < 4.5 V			6	—		
			1.8 V ≤ VCC < 2.4 V			8	—		
			1.6 V ≤ VCC <1.8 V			2	—		
	Input clock pulse width				t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time				t_{SCKr}	—	20	ns	
	Input clock fall time				t_{SCKf}	—	20	ns	
	Output clock cycle time	Asynchronous			t_{Scyc}	6	—	t_{PBcyc}	Figure 2.46
		Clock synchronous	4.5 V ≤ VCC ≤ 5.5 V	24 MHz < PCLKB ≤ 32 MHz		4	—		
				PCLKB ≤ 24 MHz		2	—		
			2.7 V ≤ VCC < 4.5 V			4	—		
			2.4 V ≤ VCC < 2.7 V			6	—		
			1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		8	—		
				PCLKB ≤ 24 MHz		6	—		
			1.6 V ≤ VCC <1.8 V			2	—		
	Output clock pulse width				t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			4.5 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	5	ns	
				1.8 V ≤ VCC < 4.5 V		—	20	ns	
				1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Output clock fall time			4.5 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	5	ns	
				1.8 V ≤ VCC < 4.5 V		—	20	ns	
				1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Transmit data delay time (master)		Clock synchronous	4.5 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	10	ns	
				1.8 V ≤ VCC < 4.5 V		—	40	ns	
				1.6 V ≤ VCC < 1.8 V		—	45	ns	
	Transmit data delay time (slave)		Clock synchronous	4.5 V ≤ VCC ≤ 5.5 V		—	30	ns	
				2.7 V ≤ VCC < 4.5 V		—	55	ns	
				2.4 V ≤ VCC < 2.7 V		—	60	ns	
				1.8 V ≤ VCC < 2.4 V		—	100	ns	
				1.6 V ≤ VCC < 1.8 V		—	125	ns	
	Receive data setup time (master)		Clock synchronous	4.5 V ≤ VCC ≤ 5.5 V	t_{RXS}	25	—	ns	
				2.7 V ≤ VCC < 4.5 V		45	—	ns	
				2.4 V ≤ VCC < 2.7 V		55	—	ns	
				1.8 V ≤ VCC < 2.4 V		90	—	ns	
				1.6 V ≤ VCC < 1.8 V		110	—	ns	
	Receive data setup time (slave)		Clock synchronous	4.5 V ≤ VCC ≤ 5.5 V		10	—	ns	
				1.8 V ≤ VCC < 4.5 V		40	—	ns	
				1.6 V ≤ VCC < 1.8 V		45	—	ns	
	Receive data hold time		Clock synchronous		t_{RXH}	10	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle

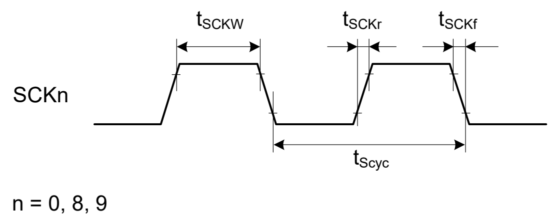


Figure 2.45 SCK Clock Input Timing

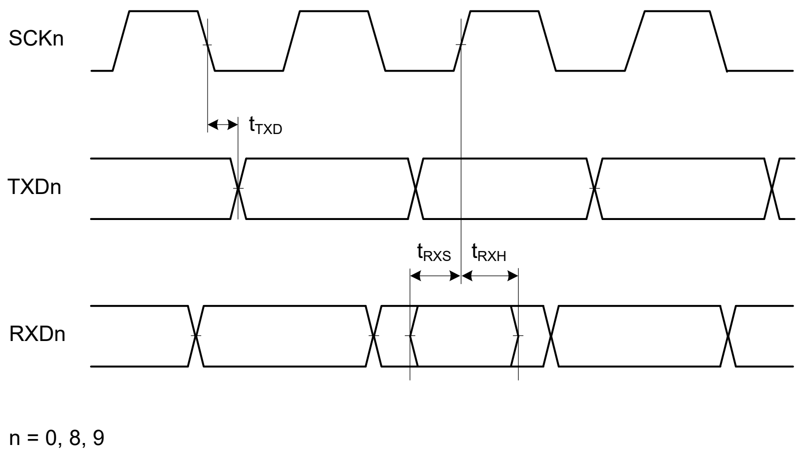


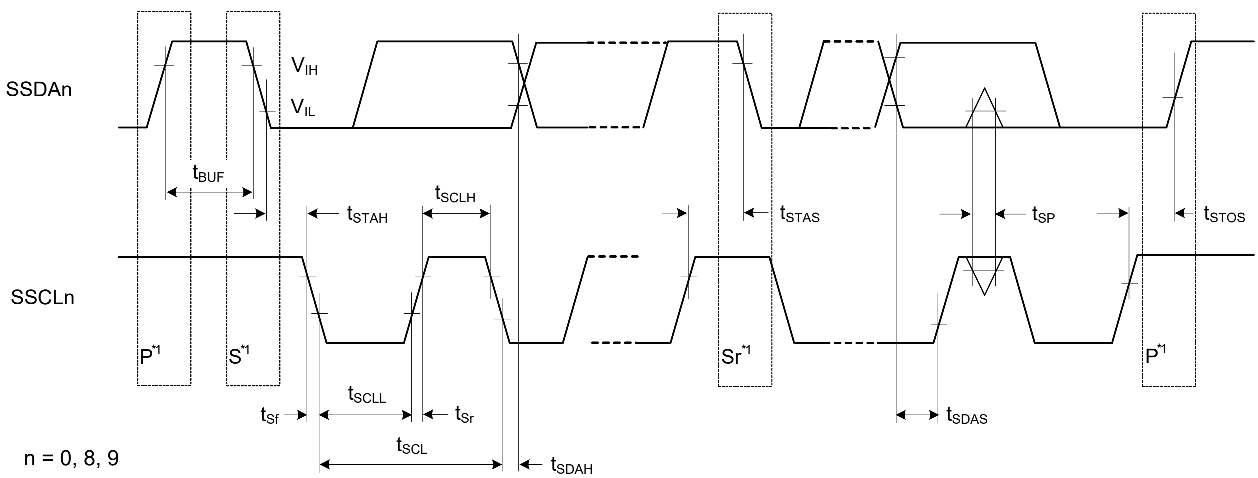
Figure 2.46 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.55 Simple I2C Timing

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I2C (standard mode)	SDA rise time	t_{Sr}	—	1000	ns	Figure 2.47
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple I2C (fast mode)	SDA rise time	t_{Sr}	—	300	ns	Figure 2.47
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc}: PCLKB cycle
Note 1. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.47 Output Timing and Simple I2C Bus Interface Input/Output Timing

Table 2.56 Simple SPI Timing (1/2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	4.5 V ≤ VCC ≤ 5.5 V	24 MHz < PCLKB ≤ 32 MHz	t_{SPcyc}	4	65536	t_{PBcyc}	Figure 2.48
			PCLKB ≤ 24 MHz		2	65536		
		2.7 V ≤ VCC < 4.5 V			4	65536		
		2.4 V ≤ VCC < 2.7 V			6	65536		
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		8	65536		
			PCLKB ≤ 24 MHz		6	65536		
		1.6 V ≤ VCC < 1.8 V			2	65536		
	SCK clock cycle input (slave)	4.5 V ≤ VCC ≤ 5.5 V	24 MHz < PCLKB ≤ 32 MHz	t_{SPcyc}	4	—	t_{PBcyc}	
			PCLKB ≤ 24 MHz		2	—		
		2.7 V ≤ VCC < 4.5 V			6	—		
		1.8 V ≤ VCC < 2.4 V			8	—		
		1.6 V ≤ VCC < 1.8 V			2	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		4.5 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	5	ns	
			1.8 V ≤ VCC < 4.5 V		—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
	Data input setup time (master)		4.5 V ≤ VCC ≤ 5.5 V	t_{SU}	25	—	ns	Figure 2.49, Figure 2.50
			2.7 V ≤ VCC < 4.5 V		45	—		
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Data input setup time (slave)		4.5 V ≤ VCC ≤ 5.5 V		10	—		
			1.8 V ≤ VCC < 4.5 V		40	—		
			1.6 V ≤ VCC < 1.8 V		45	—		
	Data input hold time			t_H	10	—	ns	
	SSL input setup time		t_{SPcyc} < 6 t_{PBcyc}	t_{LEAD}	2	—	t_{SPcyc}	
			t_{SPcyc} ≥ 6 t_{PBcyc}		1	—		
	SSL input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time (master)		4.5 V ≤ VCC ≤ 5.5 V	t_{OD}	—	10	ns	
			1.8 V ≤ VCC < 4.5 V		—	40		
			1.6 V ≤ VCC < 1.8 V		—	50		
	Data output delay time (slave)		4.5 V ≤ VCC ≤ 5.5 V		—	30		
			2.4 V ≤ VCC < 4.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	–10	—	ns	
			1.8 V ≤ VCC < 2.7 V		–20	—		
			1.6 V ≤ VCC < 1.8 V		–40	—		
	Data output hold time (slave)				–10	—		
	Data rise/fall time		4.5 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	5	ns	
			1.8 V ≤ VCC < 4.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 2.56 Simple SPI Timing (2/2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SSL input rise/fall time			t_{SSLr}, t_{SSLf}	—	20	ns	Figure 2.49, Figure 2.50
	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{PBcyc}	Figure 2.51, Figure 2.52
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		—	7		
			PCLKB ≤ 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{PBcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz < PCLKB ≤ 32 MHz		—	7		
			PCLKB ≤ 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

Note 1. t_{PBcyc}: PCLKB cycle

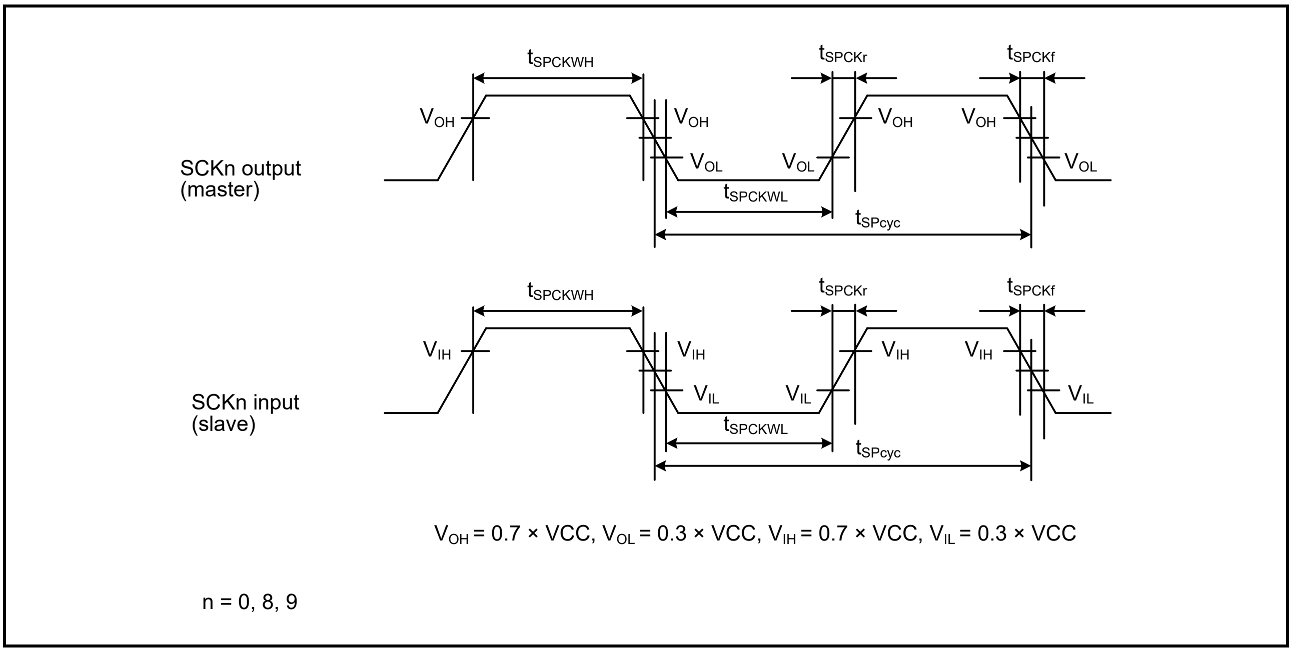


Figure 2.48 Simple SPI Clock Timing

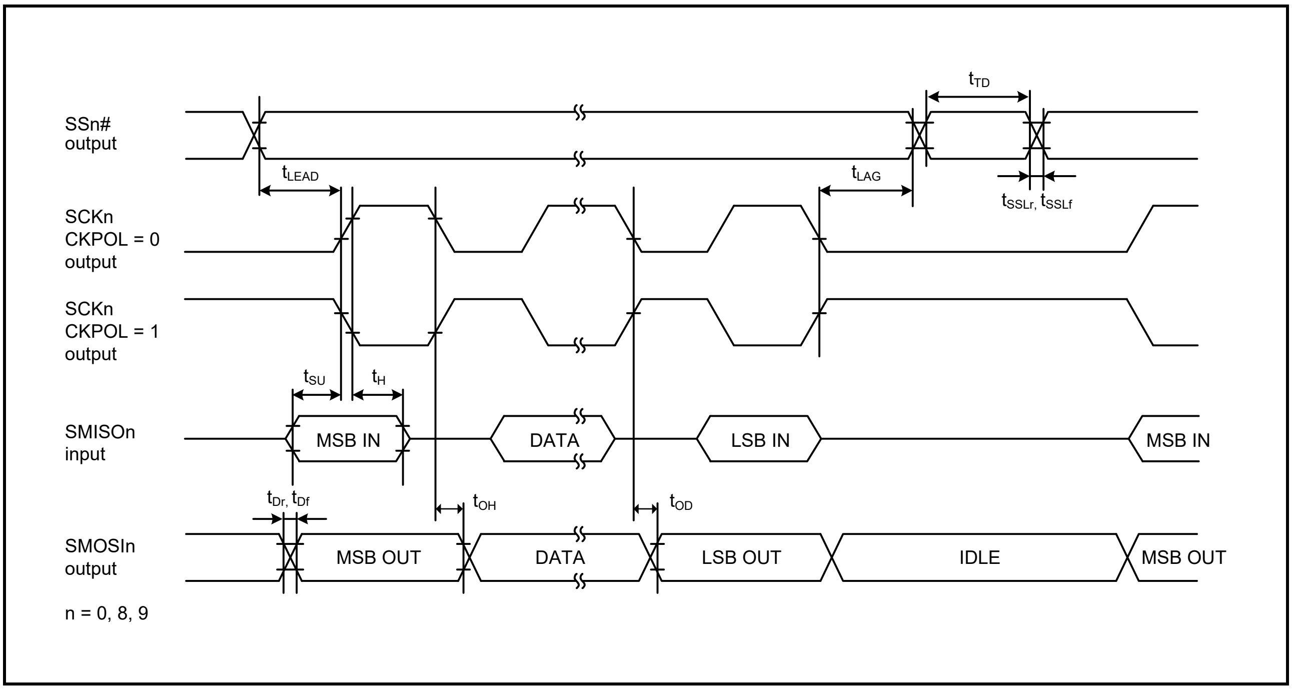


Figure 2.49 Simple SPI Clock Timing (Master, CPHA = 1)

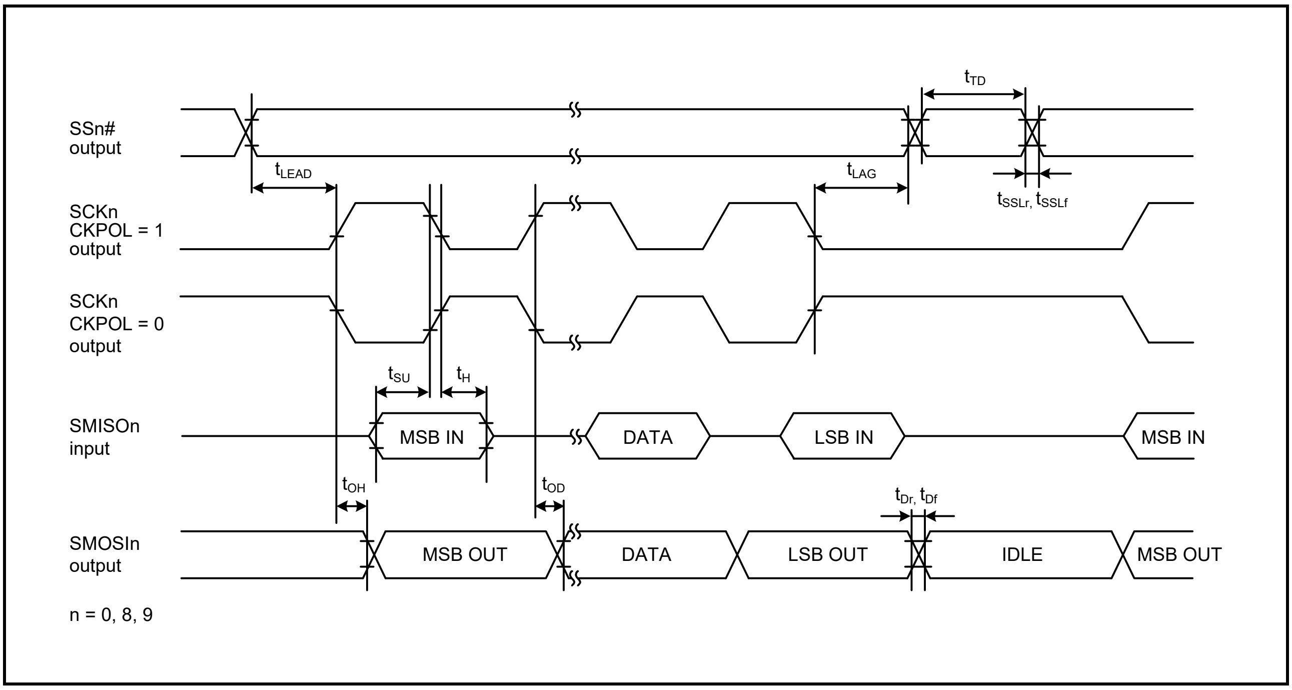


Figure 2.50 Simple SPI Clock Timing (Master, CPHA = 0)

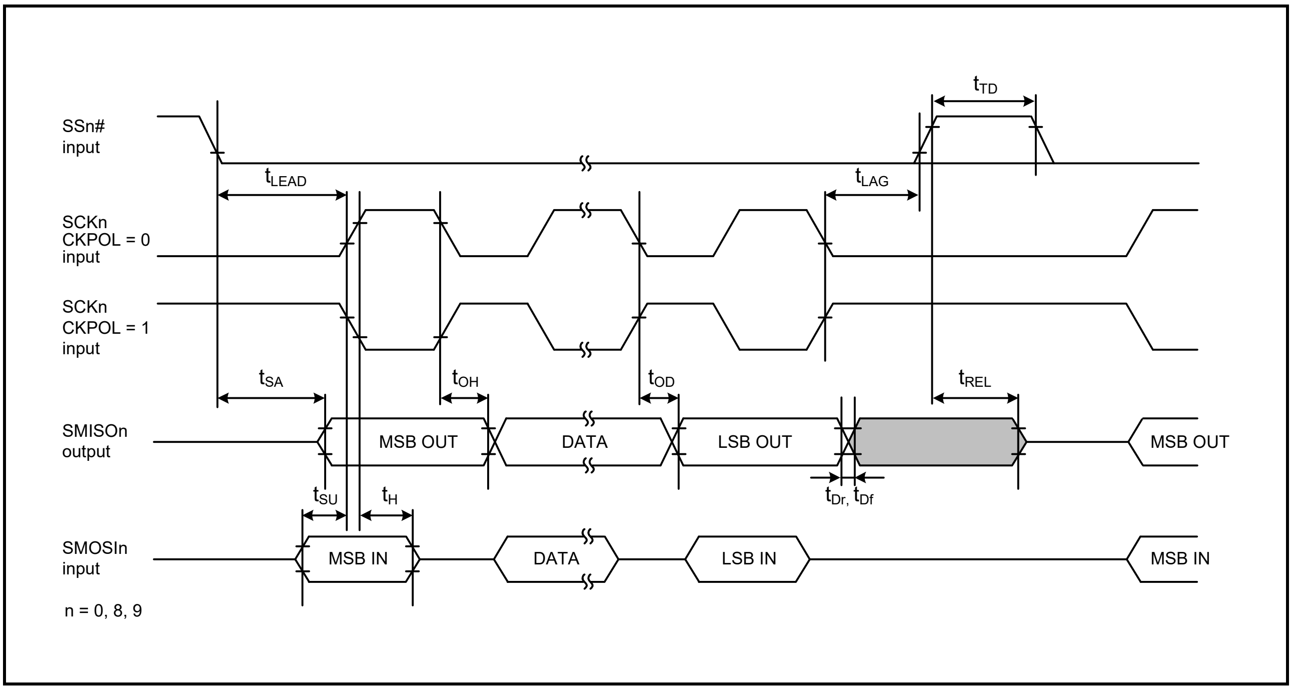


Figure 2.51 Simple SPI Clock Timing (Slave, CPHA = 1)

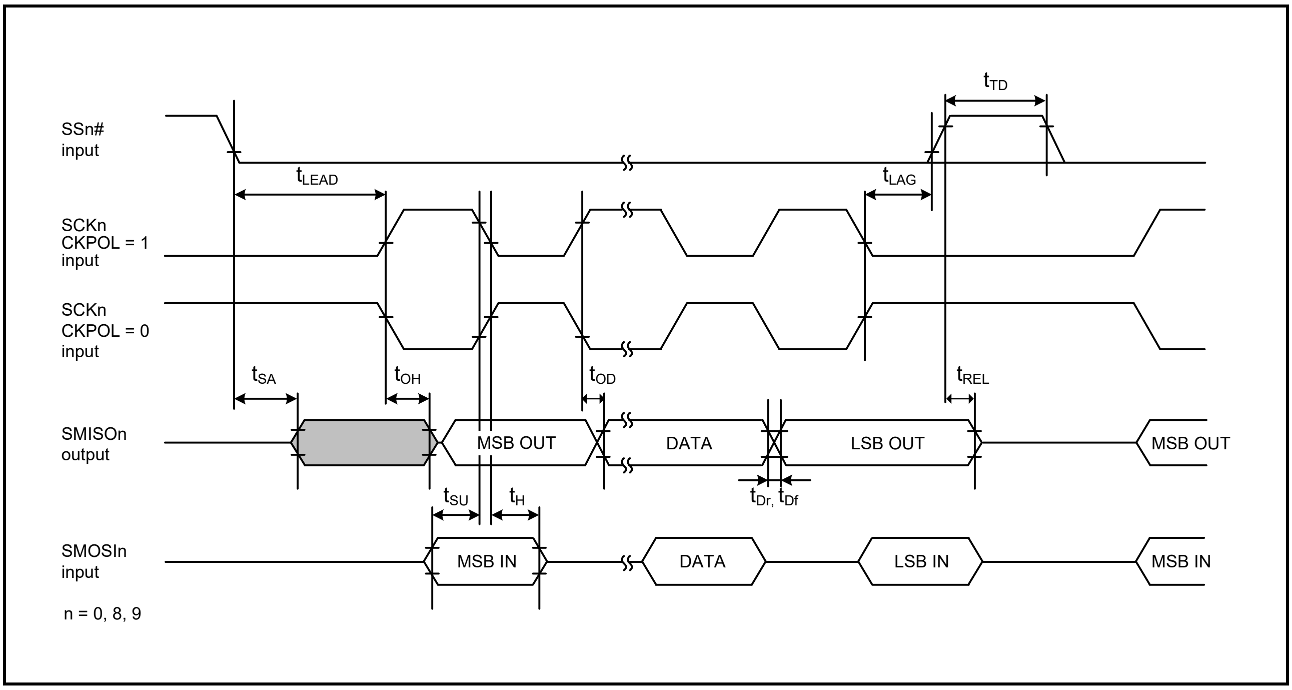


Figure 2.52 Simple SPI Clock Timing (Slave, CPHA = 0)

2.5.6.7 RIIC

Table 2.57 RIIC Timing

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.53
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.53
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle
Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.
Note 2. C_b is the total capacitance of the bus lines.

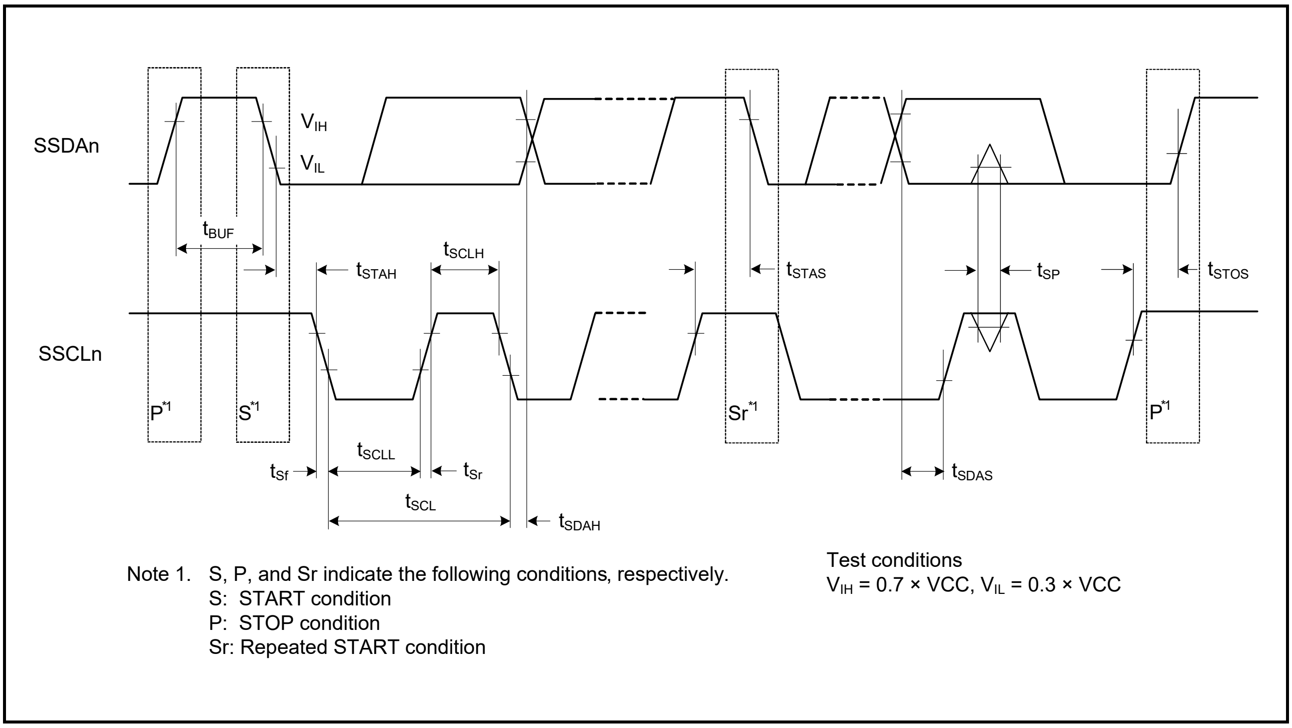


Figure 2.53 RIIC Bus Interface Input/Output Timing

2.5.6.8 RSPI

Table 2.58 RSPI Timing (1/2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	2	4096	t_{PBcyc} *1	Figure 2.54
			1.8 V ≤ VC C< 2.7 V		4	4096		
			1.6 V ≤ VCC < 1.8 V		2	4096		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		4	—		
			2.4 V ≤ VCC < 2.7 V		6	—		
			1.8 V ≤ VCC < 2.4 V		8	—		
			1.6 V ≤ VCC < 1.8 V		4	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock rise/ fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	0.1	μs/V	
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	10	—	ns	Figure 2.55 to Figure 2.60
			1.8 V ≤ VCC < 2.7 V		30	—		
			1.6 V ≤ VCC < 1.8 V		10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		10	—		
			1.8 V ≤ VCC < 2.4 V		15	—		
			1.6 V ≤ VCC < 1.8 V		20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{PBcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	20	—		
	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
			1.6 V ≤ VCC < 1.8 V		–50 + N*2 × t_{SPcyc}	—		
		Slave			6	—	t_{PBcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{PBcyc}	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V		—	20		
			1.8 V ≤ VCC < 2.4 V		—	25		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		—	50		
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	85		
			1.6 V ≤ VCC < 1.8 V		—	110		

Table 2.58 RSPI Timing (2/2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, C = 30 pF,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	Data output hold time	Master		t_{OH}	0	—	ns	Figure 2.55 to Figure 2.60
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{PBcyc}	8 × t_{SPcyc} + 2 × t_{PBcyc}	ns	
		Slave			6 × t_{PBcyc}	—		
	MOSI and MISO rise/ fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	μs	
	SSL rise/fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15	ns	
			1.8 V ≤ VCC < 2.4 V		—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30	ns	
		Input			—	1	μs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{PBcyc} + 100	ns	Figure 2.59, Figure 2.60
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{PBcyc} + 140	ns	
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{PBcyc} + 180	ns	
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{PBcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{PBcyc} + 140	ns	
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{PBcyc} + 180	ns	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

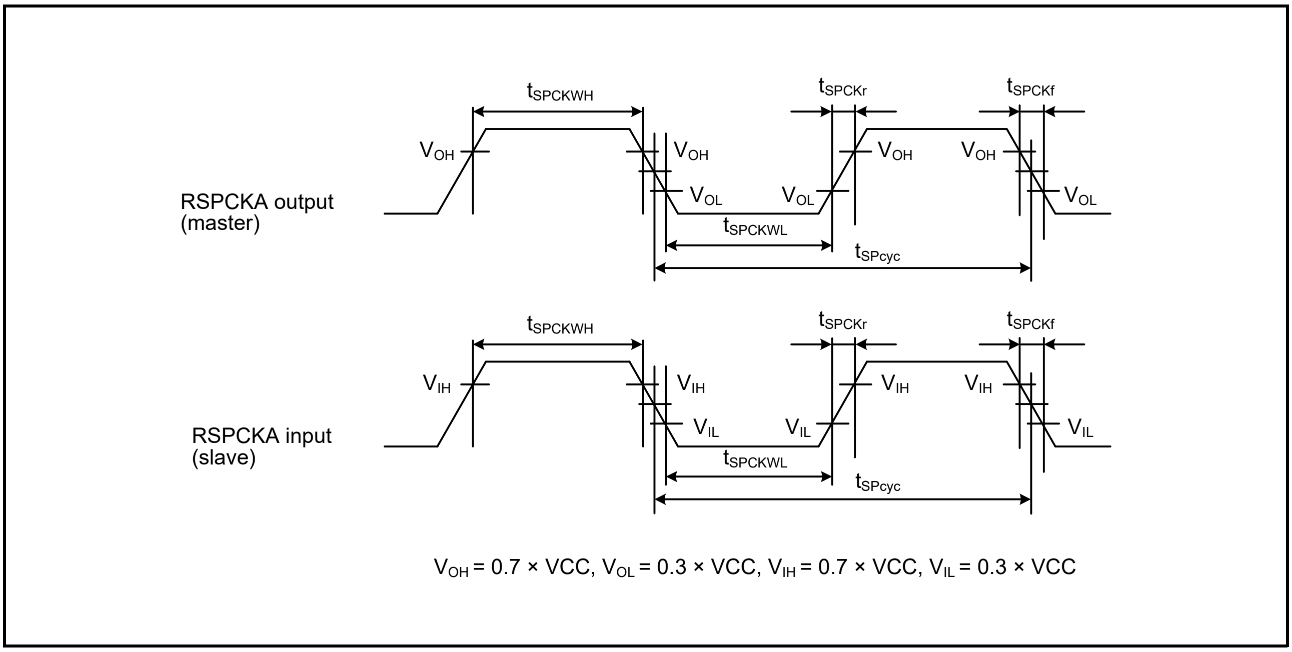


Figure 2.54 RSPI Clock Timing

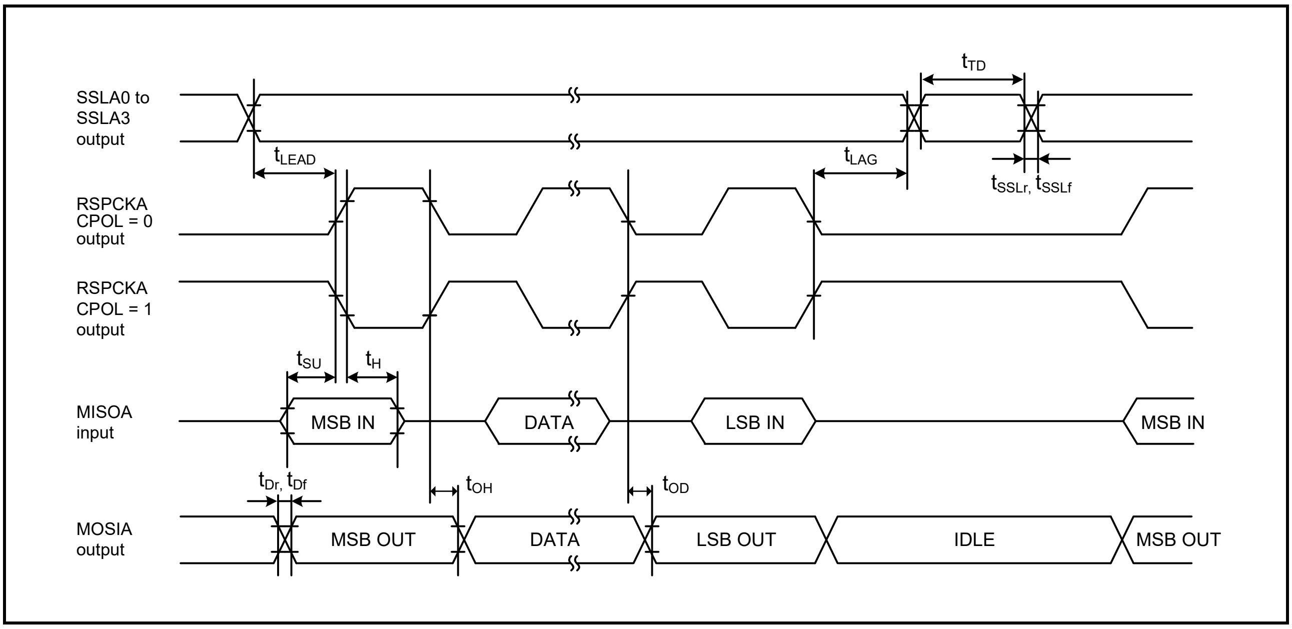


Figure 2.55 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

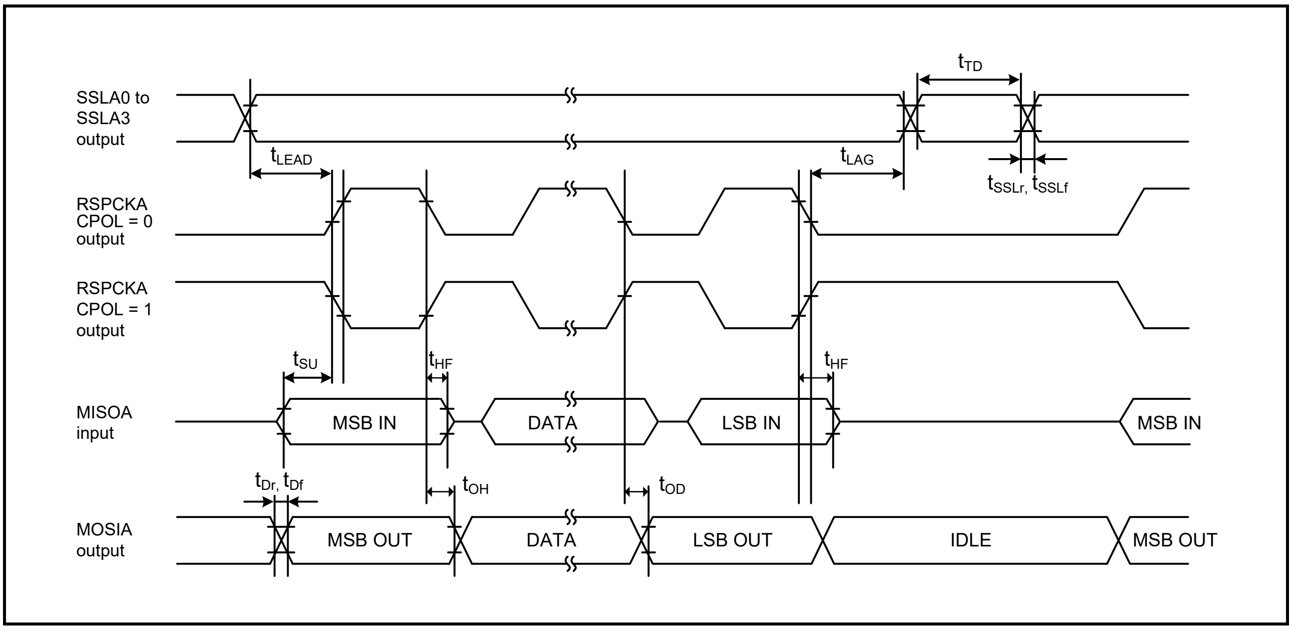


Figure 2.56 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

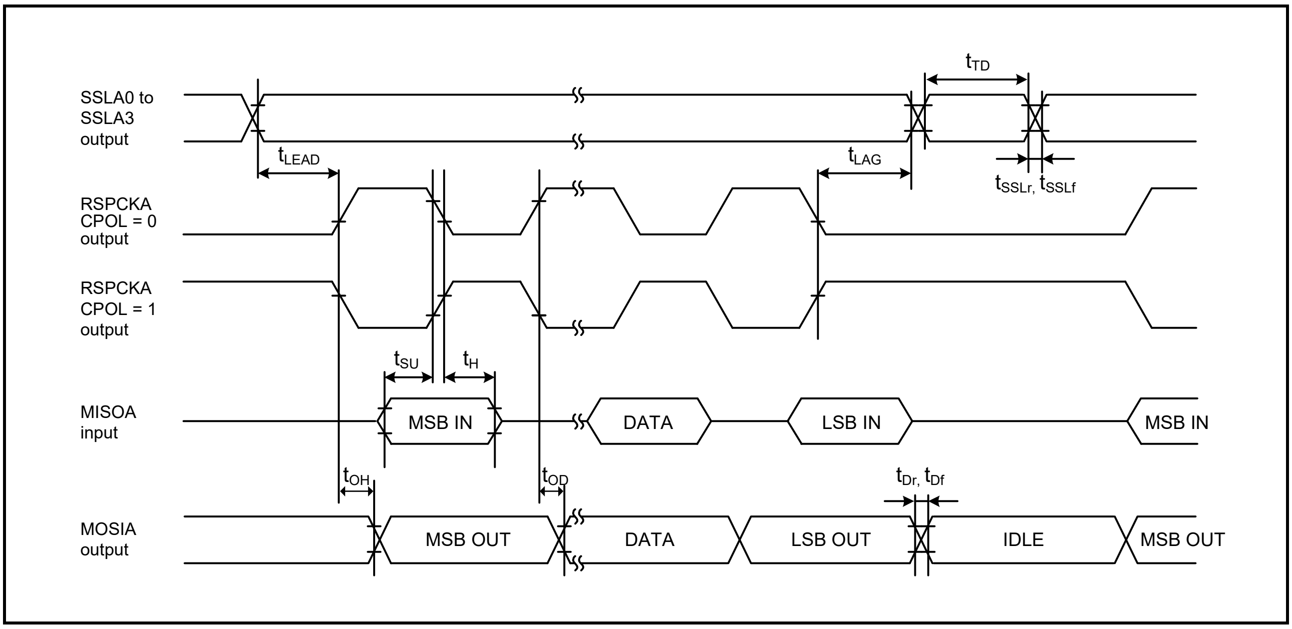


Figure 2.57 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

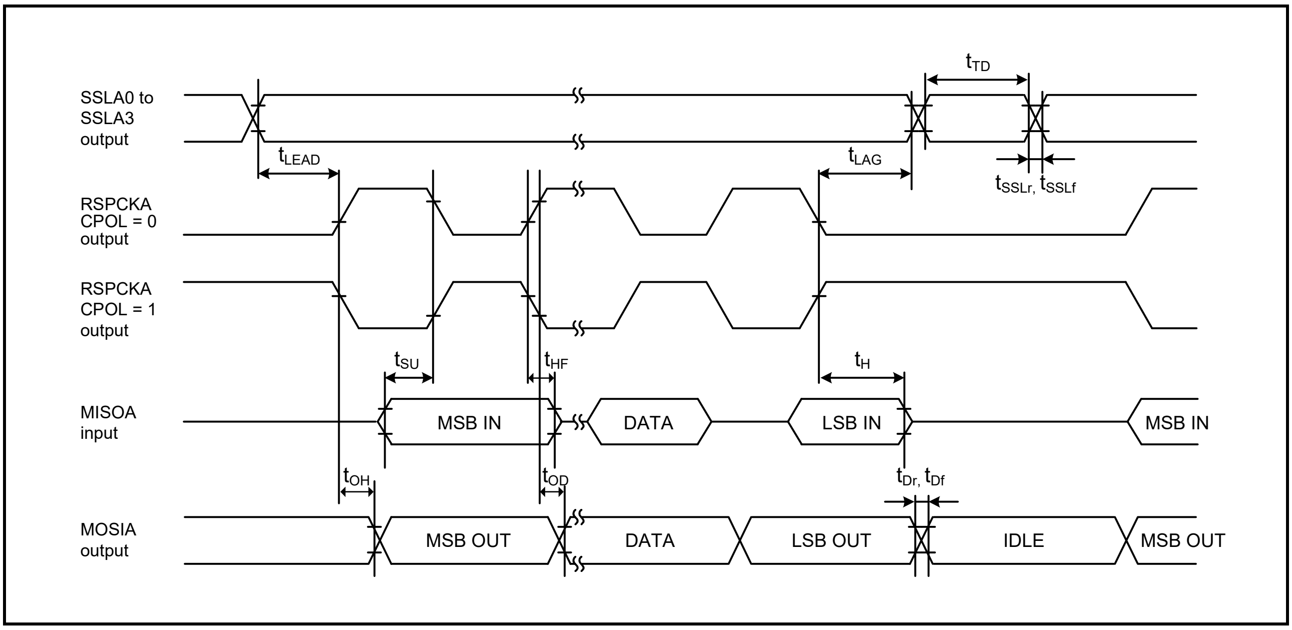


Figure 2.58 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

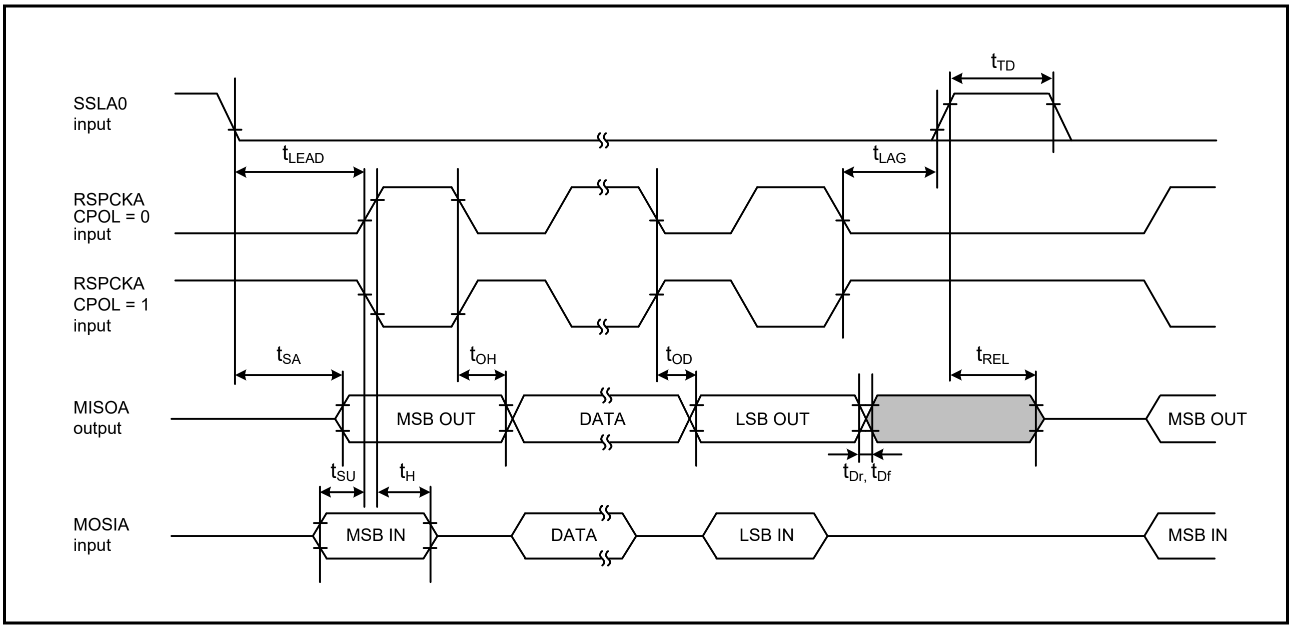


Figure 2.59 RSPI Timing (Slave, CPHA = 0)

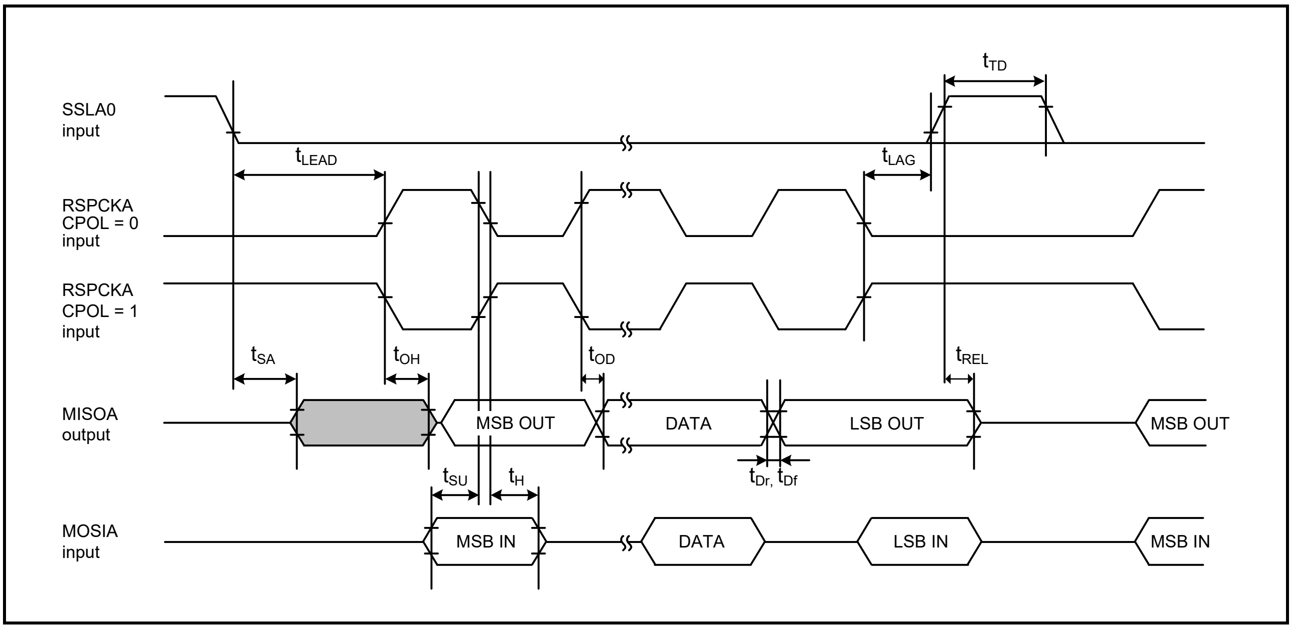


Figure 2.60 RSPI Timing (Slave, CPHA = 1)

2.5.6.9 CANFD

Table 2.59 CANFD Timing

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item		Symbol	Min.	Max.	Unit	Test Conditions
Internal delay time	2.4 V ≤ VCC ≤ 5.5 V	t_{NODE}	—	50	ns	Figure 2.61
	1.8 V ≤ VCC < 2.4 V		—	75		

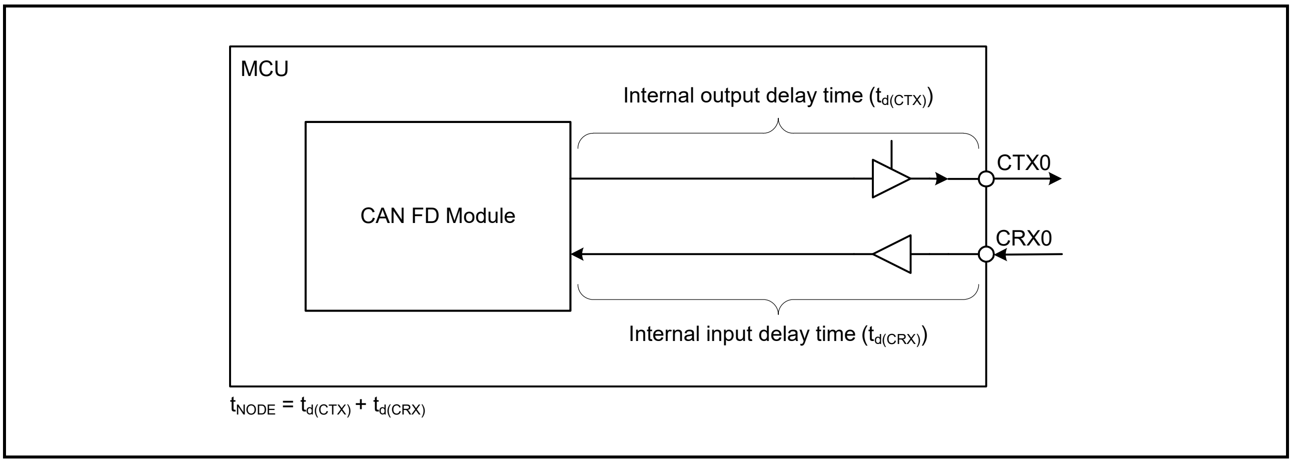


Figure 2.61 Definition of Internal Delay Time

2.5.6.10 A/D Converter Trigger

Table 2.60 A/D Converter Trigger Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.62

Note 1. t_{PBcyc}: PCLKB cycle

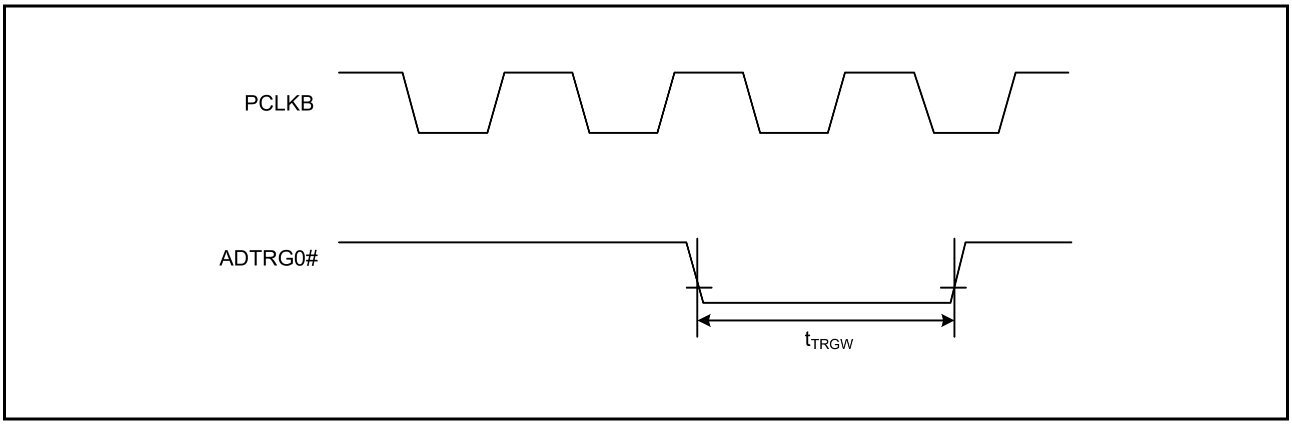


Figure 2.62 A/D Converter External Trigger Input Timing

2.5.6.11 CAC

Table 2.61 CAC Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$ *2	t_{CACREF}	$4.5\ t_{cac} + 3\ t_{PBcyc}$	—	ns	
		$t_{PBcyc} > t_{cac}$ *2		$5\ t_{cac} + 6.5\ t_{PBcyc}$			
	CACREF input rise/fall time		$t_{CACREFr}$, $t_{CACREFf}$	—	0.1	μs/V	

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

2.5.6.12 CLKOUT

Table 2.62 CLKOUT Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C,
Output load conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Item			Symbol	Min.	Max.	Unit	Test Conditions
CLKOUT	CLKOUT pin output cycle*2	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.63
		1.8 V ≤ VCC < 2.7 V		125			
		1.6 V ≤ VCC < 1.8 V		250			
	CLKOUT pin high pulse width*1	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30			
		1.6 V ≤ VCC < 1.8 V		80			
	CLKOUT pin low pulse width*1	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30			
		1.6 V ≤ VCC < 1.8 V		80			
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V			25		
		1.6 V ≤ VCC < 1.8 V			30		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V			25		
		1.6 V ≤ VCC < 1.8 V			30		

Note 1. When the LOCO is selected as the clock output source (CKOCR.CKOSEL[3:0] bits = 0000b), set the clock output division ratio selection to divided by 2 (CKOCR.CKODIV[2:0] bits = 001b).
Note 2. When the XTAL external clock input or an oscillator is used with divided by 1 (CKOCR.CKOSEL[3:0] bits = 010b and CKOCR.CKODIV[2:0] bits = 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

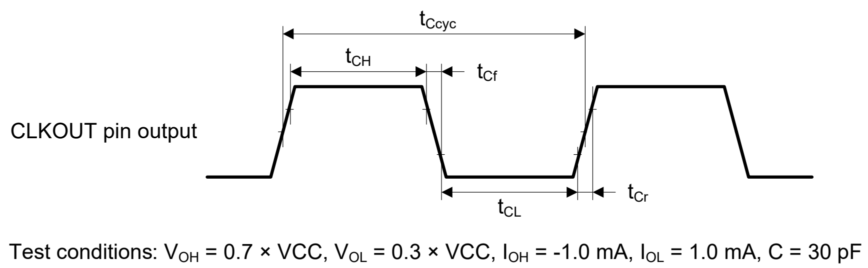


Figure 2.63 CLKOUT Output Timing

2.6 USB Characteristics

Table 2.63 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: 3.0 V ≤ VCC ≤ 3.6 V, 3.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V		
	Input low level voltage		V_{IL}	—	0.8	V		
	Differential input sensitivity		V_{DI}	0.2	—	V	| USB0_DP – USB0_DM |	
	Differential common mode range		V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC	V	I_{OH} = –200 μA	
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA	
	Cross-over voltage		V_{CRS}	1.3	2.0	V		Figure 2.64, Figure 2.65
	Rise time	FS	t_r	4	20	ns		
		LS		75	300			
	Fall time	FS	t_f	4	20	ns		
		LS		75	300			
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	t_r/t_f	
		LS		80	125			
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)	
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ		
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state	
			R_{PUA}	1.425	3.09	kΩ	During transmission and reception	

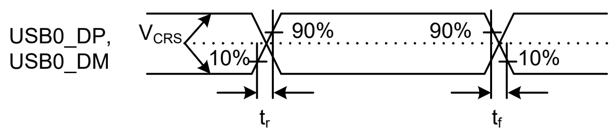


Figure 2.64 USB0_DP and USB0_DM Output Timing

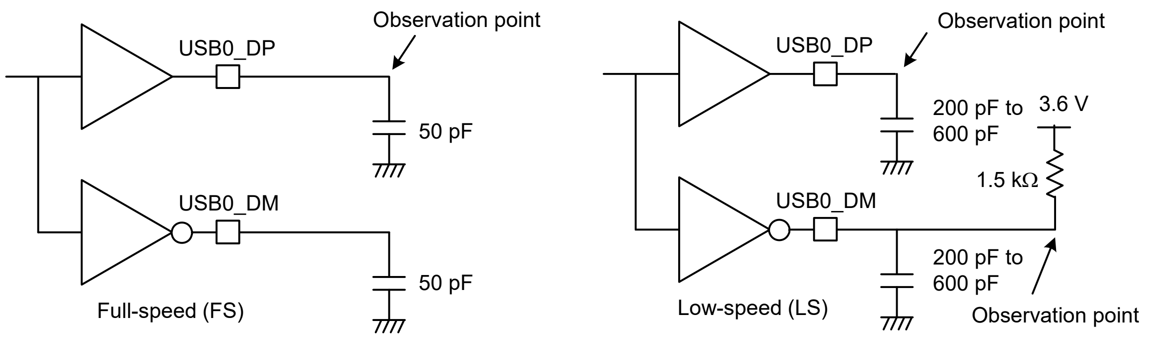


Figure 2.65 Test Circuit

2.7 A/D Conversion Characteristics

Table 2.64 A/D Conversion Characteristics (1)

Conditions: 4.5 V ≤ VCC ≤ 5.5 V, 4.5 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C,
signal source impedance = 0.5 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	64	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (operation at PCLKD = 64 MHz)		0.50 (0.156)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Ah ADCCR.CCS = 1
		0.97 (0.625)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	1.3*3	kΩ	High-precision channel
		—	—	5.0*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.65 A/D Conversion Characteristics (2)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C,
signal source impedance = 0.3 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	48	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (operation at PCLKD = 48 MHz)		0.67 (0.208)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Ah ADCCR.CCS = 1
		1.29 (0.833)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	± 0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.66 A/D Conversion Characteristics (3)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, signal source impedance = 1.3 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)		1.00 (0.313)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 0Ah ADCCR.CCS = 1
		1.94 (1.250)*2	—	—	μs	Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn = 28h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7.0*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.67 A/D Conversion Characteristics (4)

Conditions: 2.7 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C,
signal source impedance = 1.1 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	24	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (operation at PCLKD = 24 MHz)		1.58 (0.417)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		2.00 (0.833)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.68 A/D Conversion Characteristics (5)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, 2.4 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C, signal source impedance = 2.2 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (operation at PCLKD = 16 MHz)		2.38 (0.625)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		3.00 (1.250)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel
				±8.5	LSB	Other than above
DNL differential nonlinearity error		—	±1.0	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.69 A/D Conversion Characteristics (6)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C, signal source impedance = 5 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (operation at PCLKD = 8 MHz)		4.75 (1.250)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		6.00 (2.500)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	6*3	kΩ	High-precision channel
		—	—	14*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	High-precision channel
				±11.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.70 A/D Conversion Characteristics (7)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C,
signal source impedance = 9.9 kΩ
Reference voltage = VREFH0

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	4	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (operation at PCLKD = 4 MHz)		9.50 (2.500)*2	—	—	μs	High-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 0Ah ADCCR.CCS = 1
		12.00 (5.000)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 1 ADSSTRn = 14h ADCCR.CCS = 1
Analog input capacitance	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3		Normal-precision channel
Analog input resistance	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3		Normal-precision channel
Analog input effective range		0	—	VREFH0	V	
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	High-precision channel
				±11.0	LSB	Other than above
DNL differential nonlinearity error		—	±1.25	—	LSB	
INL integral nonlinearity error		—	±1.5	±3.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The values in ( ) show the sampling times.

Note 3. The values are reference values.

Table 2.71 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN031		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.6 to 5.5 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.6 to 5.5 V	
CTSU input channels	AN008	AVCC0 = 1.6 to 5.5V	

Table 2.72 A/D Internal Reference Voltage Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ VREFH0 = AVCC0 ≤ 5.5 V, VSS = AVSS0 = VREFL0 = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*1	1.42	1.48	1.54	V	

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

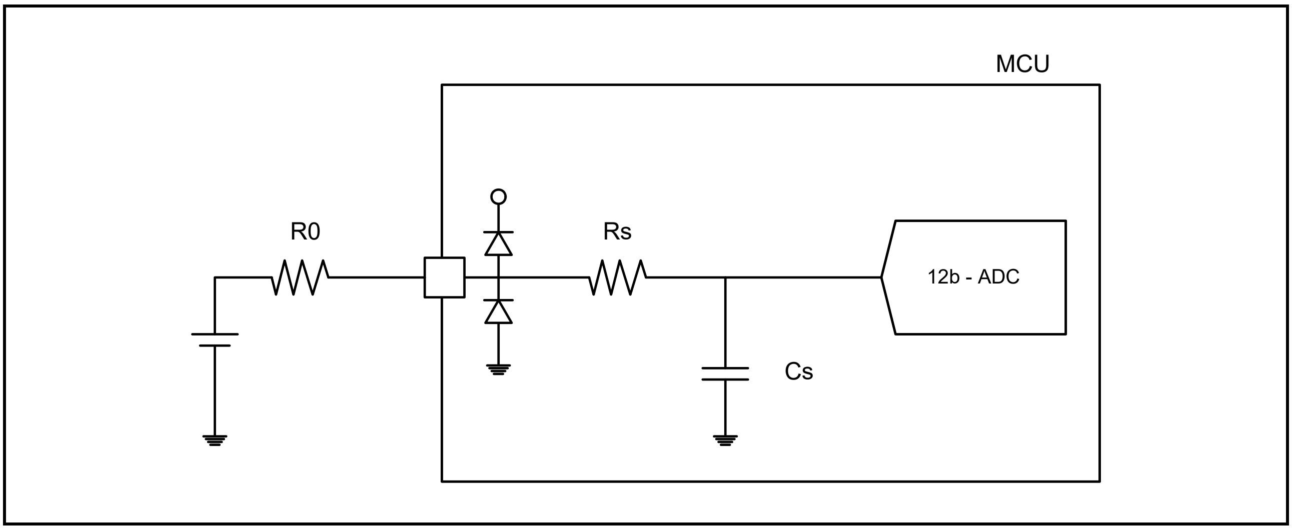


Figure 2.66 Equivalent Circuit

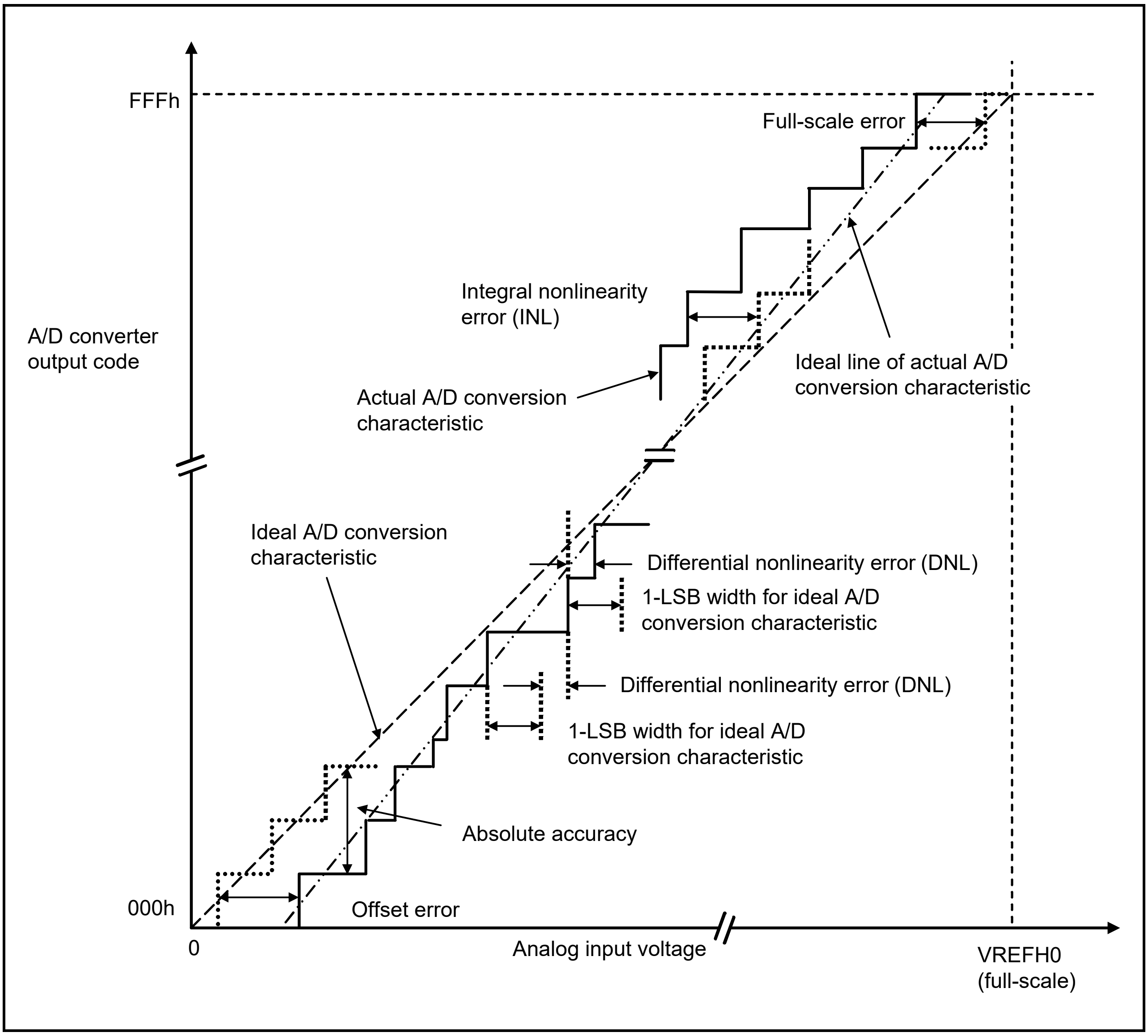


Figure 2.67 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, … are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

2.8 D/A Conversion Characteristics

Table 2.73 D/A Conversion Characteristics

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		—	—	—	8	Bit	
Conversion time	AVCC0 = 1.6 to 5.5 V	t_{DCONV}	—	—	3.0	μs	35-pF capacitive load
Absolute accuracy	AVCC0 = 2.4 to 5.5 V	—	—	—	±3.0	LSB	2-MΩ resistive load
	AVCC0 = 1.8 to 2.4 V	—	—	—	±3.5		
	AVCC0 = 1.6 to 1.8 V	—	—	—	±4.0		
	AVCC0 = 2.4 to 5.5 V	—	—	—	±2.0	LSB	4-MΩ resistive load
	AVCC0 = 1.8 to 2.4 V	—	—	—	±2.5		
	AVCC0 = 1.6 to 1.8 V	—	—	—	±3.0		
RO output resistance		—	—	9.0	—	kΩ	

2.9 Temperature Sensor Characteristics

Table 2.74 Temperature Sensor Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.3	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	μs	
Sampling time	—	5	—	—	μs	

2.10 Comparator Characteristics

Table 2.75 Comparator Characteristics

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 to CVREFB1 input reference voltage		VREF	0	—	VCC – 1.4	V	
CMPB0 to CMPB1 input voltage		VI	0	—	VCC	V	
Internal reference voltage*1		—	1.34	1.44	1.54	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	μs	VCC = 3 V, input slew rate ≥ 50 mV/μs
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	μs	
	Comparator low-speed mode	Td	—	—	9.0	μs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 × VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 × VCC	—	V	
Operation stabilization wait time (high-speed mode)	VCC = 1.6 V to 5.5 V	Tcmp	100	—	—	μs	
Operation stabilization wait time (low-speed mode)	VCC = 1.8 V to 5.5 V		100	—	—		
	VCC = 1.6 V to 1.8 V		1000	—	—		

Note 1. The internal reference voltage cannot be used when VCC < 1.8 V.

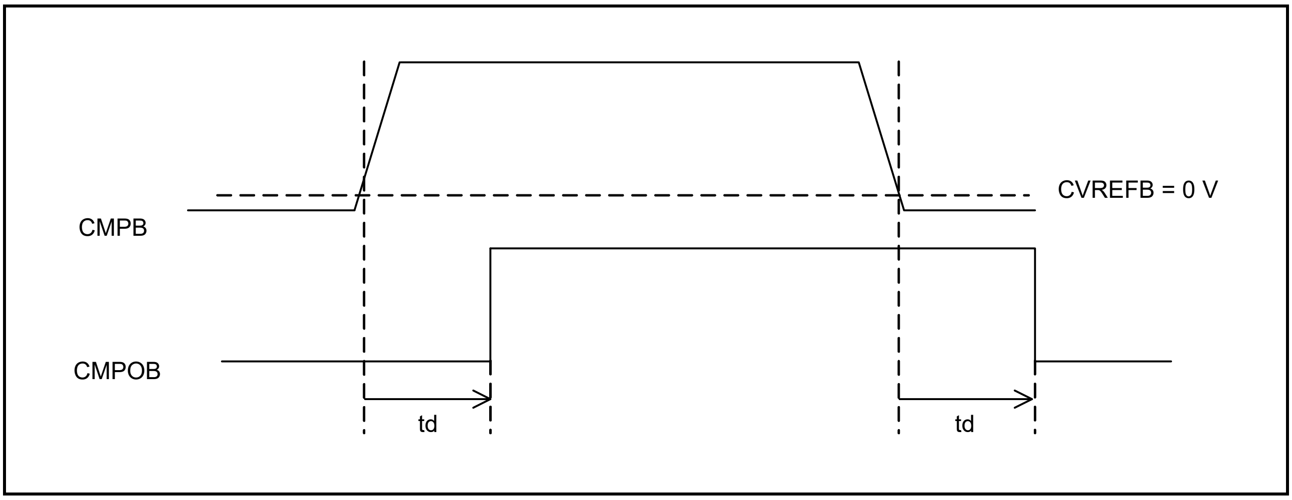


Figure 2.68 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

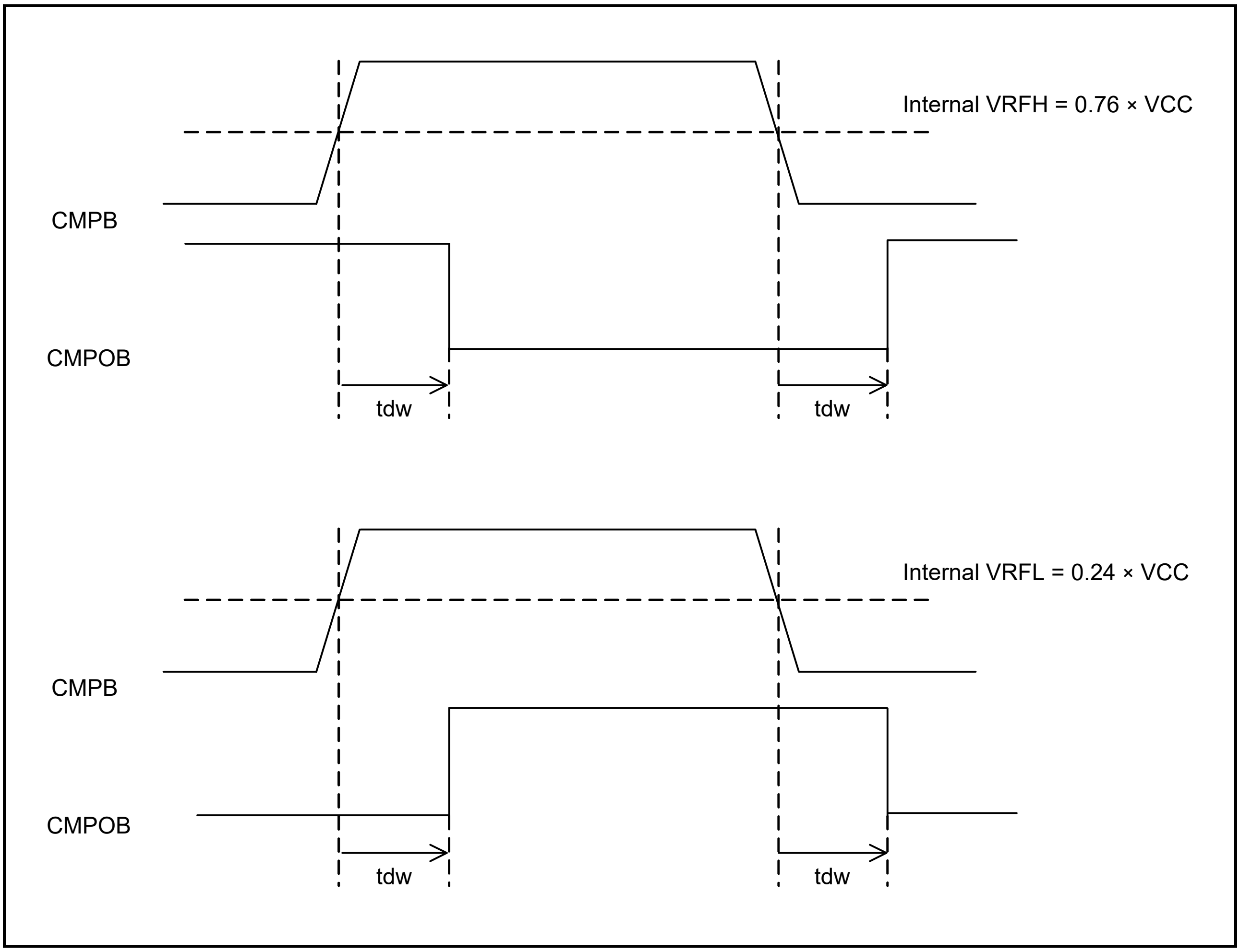


Figure 2.69 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

2.11 CTSU Characteristics

Table 2.76 CTSU Characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	

2.12 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.77 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.46	1.50	1.54	V	Figure 2.70, Figure 2.71
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.85	3.97	V	Figure 2.72 At falling edge VCC
		V_{det0_1}	2.70	2.85	3.00		
		V_{det0_2}	2.37	2.53	2.67		
		V_{det0_3}	1.80	1.90	1.99		
		V_{det0_4}	1.60	1.69	1.80		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 2.73 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.28		
		V_{det1_2}	3.86	4.03	4.16		
		V_{det1_3}	3.68	3.86	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.80	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.59	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		
		V_{det1_E}	1.69	1.75	1.81		
		V_{det1_F}	1.60	1.65	1.70		
Voltage detection level	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.32	4.48	V	Figure 2.74 At falling edge VCC
		V_{det2_1}	3.95	4.17	4.35		
		V_{det2_2}	3.82	4.03	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL2, VDSEL[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

Table 2.78 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	12.5	—	ms	Figure 2.71
	During fast startup time*2	t_{POR}	—	5.0	—		
Wait time after voltage monitoring 0 reset cancellation		t_{LVD0}	—	880	—	μs	Figure 2.72
Wait time after voltage monitoring 1 reset cancellation	LVD0 disabled*4	t_{LVD1}	—	180	—	μs	Figure 2.73
	LVD0 enabled*5		—	880	—	μs	
Wait time after voltage monitoring 2 reset cancellation	LVD0 disabled*4	t_{LVD2}	—	180	—	μs	Figure 2.74
	LVD0 enabled*5		—	880	—	μs	
PDR response delay time		t_{det}	—	—	500	μs	Figure 2.70
LVD0 response delay time			—	—	500	μs	Figure 2.70
LVD1 response delay time			—	—	360	μs	Figure 2.70
LVD2 response delay time			—	—	600	μs	Figure 2.70
POR/LVD0 minimum VCC down time*3		t_{VOFF}	500	—	—	μs	Figure 2.70, VCC = 1.0 V or above
LVD1 minimum VCC down time*3			300	—	—	μs	Figure 2.70, VCC = 1.0 V or above
LVD2 minimum VCC down time*3			600	—	—	μs	Figure 2.70, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 2.71, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	300	μs	Figure 2.73
LVD2 operation stabilization time (after LVD is enabled)		$t_{d(E-A)}$	—	—	1200	μs	Figure 2.74
Hysteresis width (power-on rest (POR))		V_{PORH}	—	10	—	mV	
Hysteresis width (LVD0, LVD1, and LVD2)		V_{LVH}	—	60	—	mV	Vdet0_0 to Vdet0_4 selected
			—	110	—		Vdet1_0 to Vdet1_2 selected
			—	70	—		Vdet1_3 to Vdet1_9 selected
			—	60	—		Vdet1_A to Vdet1_B selected
			—	50	—		Vdet1_C to Vdet1_F selected
			—	90	—		LVD2 selected

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

Note 4. When OFS1.LVDAS = 1b.

Note 5. When OFS1.LVDAS = 0b.

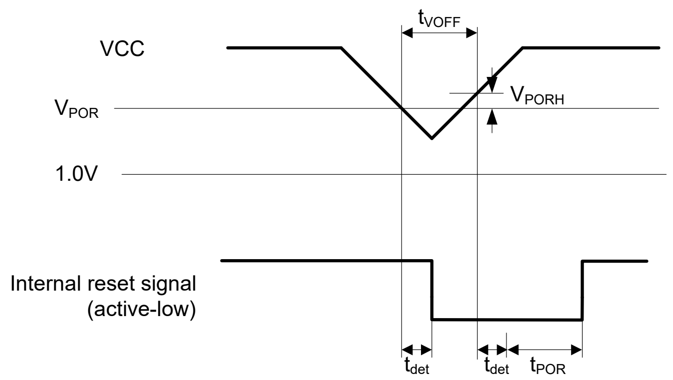
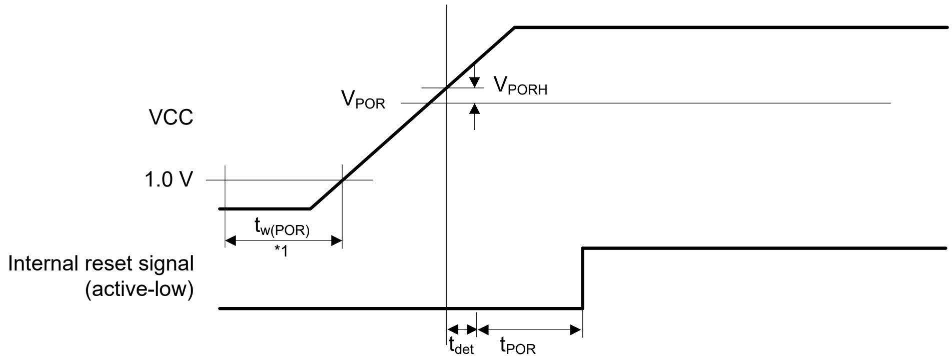


Figure 2.70 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.71 Power-On Reset Timing

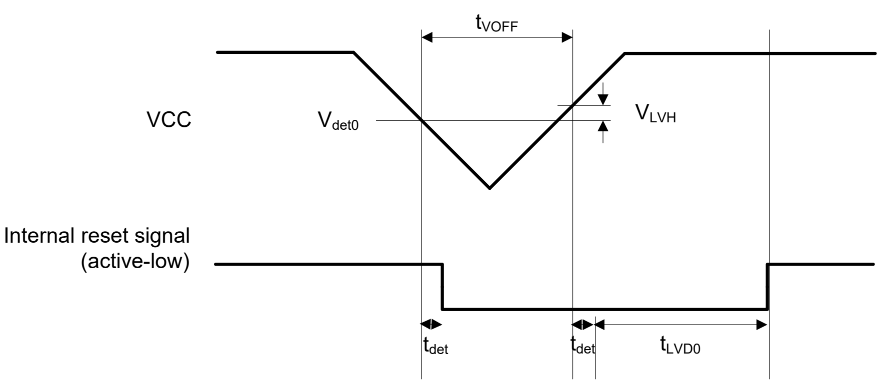


Figure 2.72 Voltage Detection Circuit Timing (V_{det0})

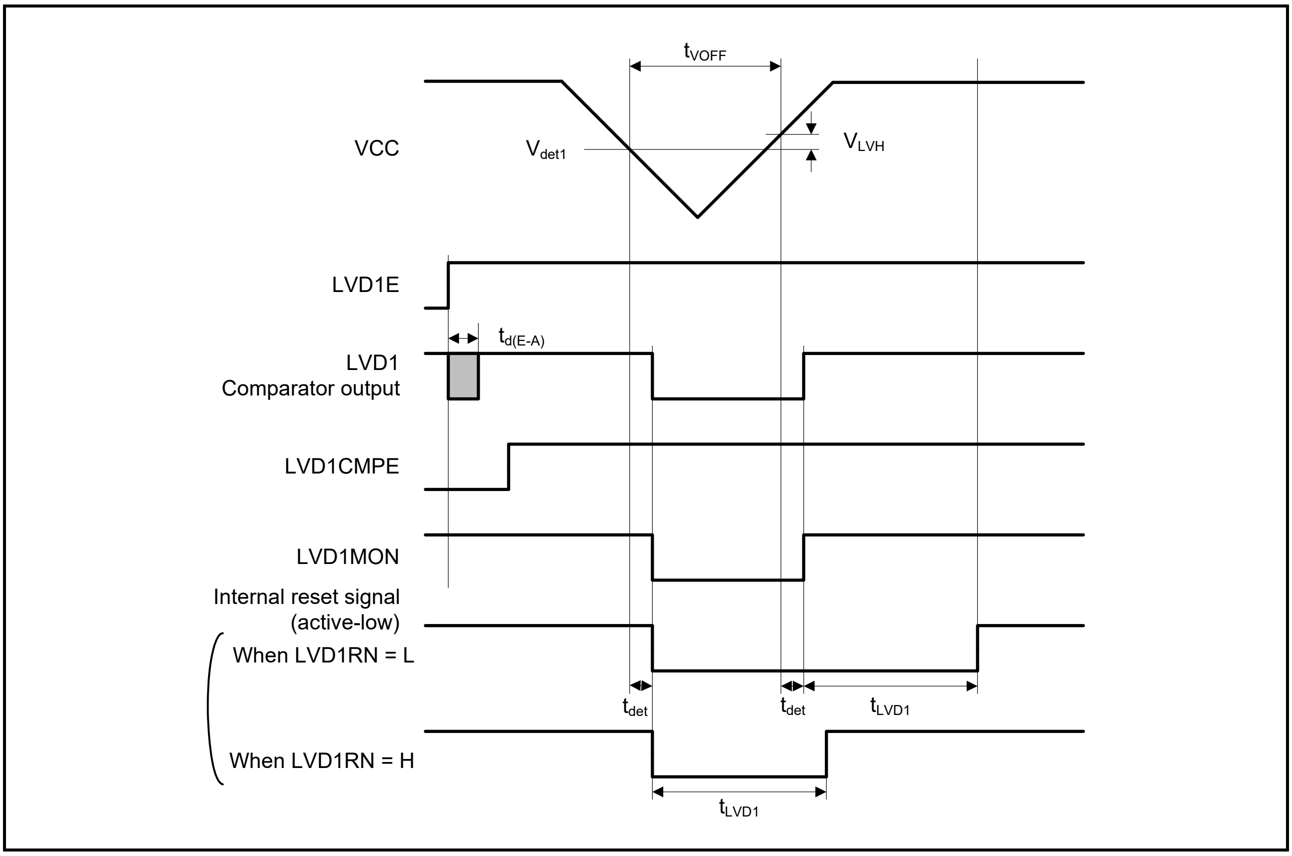


Figure 2.73 Voltage Detection Circuit Timing (V_{det1})

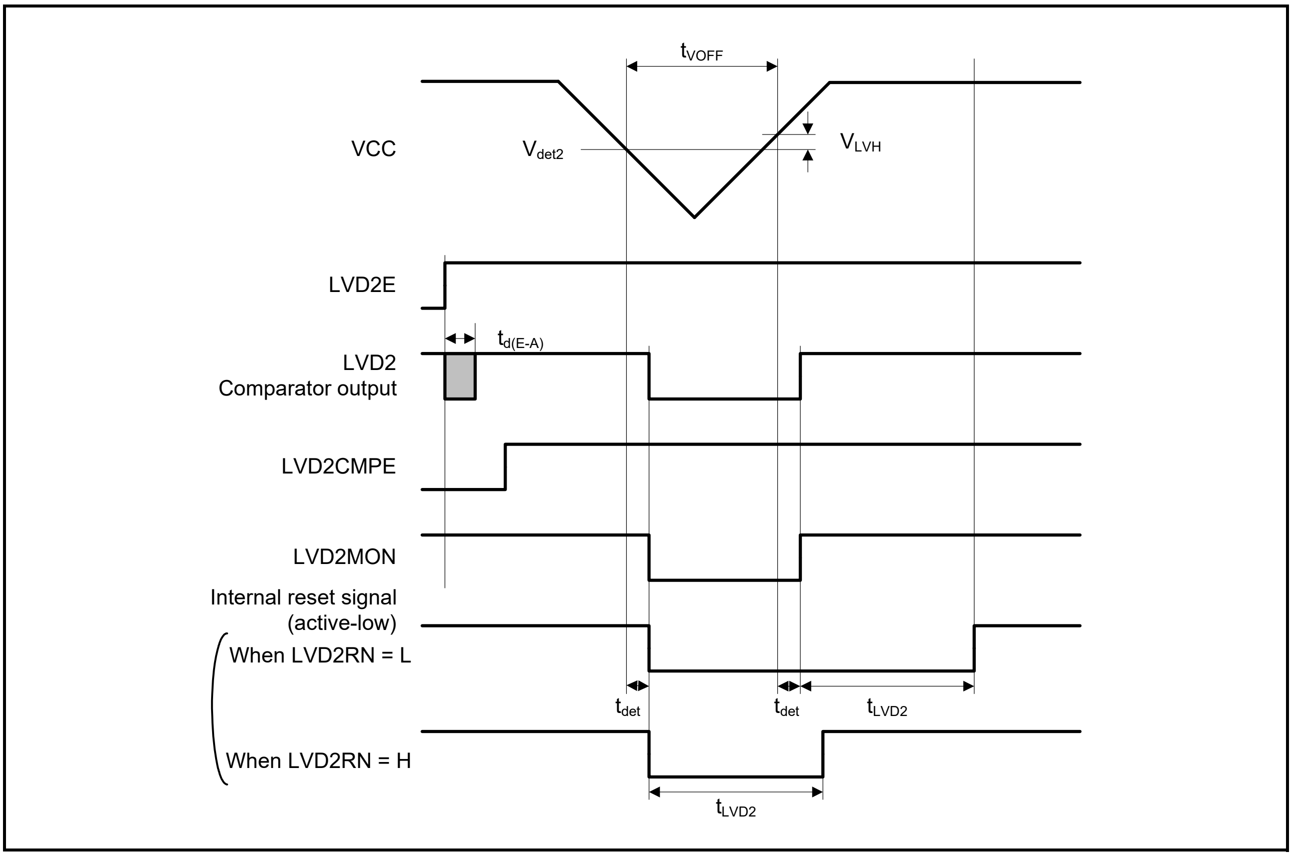


Figure 2.74 Voltage Detection Circuit Timing (V_{det2})

2.13 Oscillation Stop Detection Timing

Table 2.79 Oscillation Stop Detection Timing

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.75

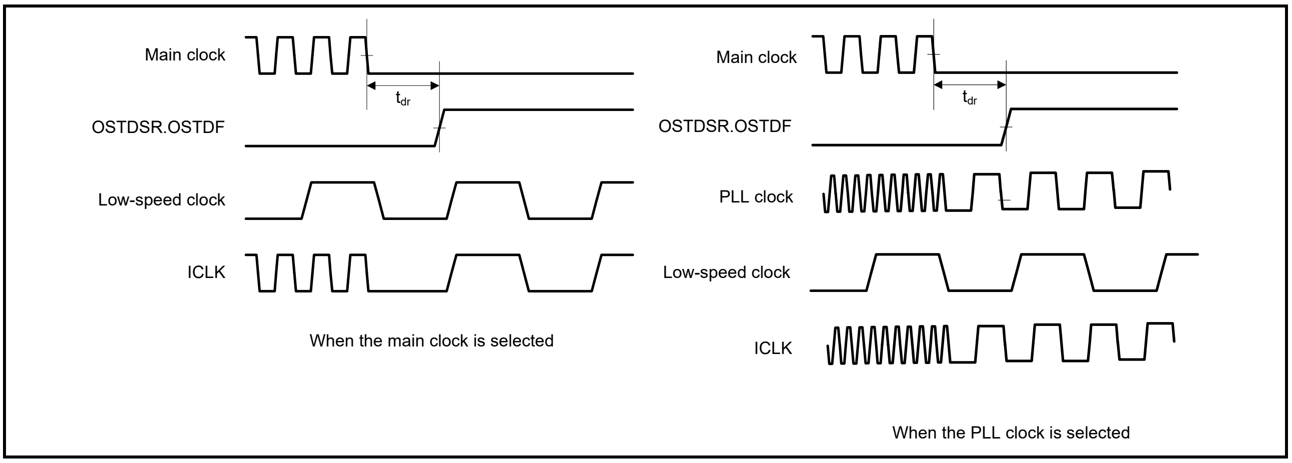


Figure 2.75 Oscillation Stop Detection Timing

2.14 ROM (Flash Memory for Code Storage) Characteristics

Table 2.80 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1K	—	—	Times	
Data retention*2, *3	After 1K times of N_{PEC}	t_{DRP}	20	—	—	Year	T_a = +105°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1K), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.81 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 48 MHz*1			FCLK = 64 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	—	45.1	446.0	—	45.0	445.0	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	—	5.4	220.1	—	5.4	220.4	ms
	512-Kbyte (block erase command)	t_{E512K}	—	807.1	17356.0	—	67.9	1651.9	—	70.6	1709.3	ms
	512-Kbyte (all-block erase command)	t_{EA512K}	—	801.9	17140.5	—	62.7	1436.9	—	65.4	1494.3	ms
Blank check time	8-byte	t_{BC8}	—	—	45.0	—	—	8.7	—	—	8.6	μs
	2-Kbyte	t_{BC2K}	—	—	1573	—	—	115	—	—	120	μs
Erase operation forcible stop time		t_{SED}	—	—	22.8	—	—	11.0	—	—	10.9	μs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	—	5.6	437.7	—	5.6	437.9	ms
Access window setting time		t_{AWS}	—	8.2	503.3	—	5.6	437.7	—	5.6	437.9	ms
ROM mode transition wait time		t_{MS}	15	—	—	15	—	—	15	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.
Note 1. 2.4 V ≤ VCC ≤ 5.5 V

Table 2.82 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 24 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	—	45.7	450.7	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	—	5.4	220.2	ms
	512-Kbyte (block erase command)	t_{E512K}	—	807.1	17356.0	—	67.9	1653.0	ms
	512-Kbyte (all-block erase command)	t_{EA512K}	—	801.9	17140.5	—	62.7	1438.1	ms
Blank check time	8-byte	t_{BC8}	—	—	45	—	—	9	μs
	2-Kbyte	t_{BC2K}	—	—	1573	—	—	115	μs
Erase operation forcible stop time		t_{SED}	—	—	22.8	—	—	11.2	μs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	—	5.6	437.7	ms
Access window setting time		t_{AWS}	—	8.2	503.3	—	5.6	437.7	ms
ROM mode transition wait time		t_{MS}	15	—	—	15	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.
Note 1. 2.4 V ≤ VCC ≤ 5.5 V

Table 2.83 ROM (Flash Memory for Code Storage) Characteristics (4) Middle-Speed Operating Mode 2

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			Unit
			Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	94.0	843.5	μs
Erasure time	2-Kbyte	t_{E2K}	—	8.3	282.0	ms
	512-Kbyte (block erase command)	t_{E512K}	—	807.1	17356.0	ms
	512-Kbyte (all-block erase command)	t_{EA512K}	—	801.9	17140.5	ms
Blank check time	8-byte	t_{BC8}	—	—	45	μs
	2-Kbyte	t_{BC2K}	—	—	1573	μs
Erase operation forcible stop time		t_{SED}	—	—	22.8	μs
Start-up area switching setting time		t_{SAS}	—	8.2	503.3	ms
Access window setting time		t_{AWS}	—	8.2	503.3	ms
ROM mode transition wait time		t_{MS}	15	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory.
Note: The frequency accuracy of FCLK should be ±3.5%.

2.15 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 2.84 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100K	1000K	—	Times	
Data retention	After 10K times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +105°C
	After 100K times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000K times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100K), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 256 times for different addresses in 256-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.85 E2 DataFlash Characteristics (2) High-speed operating mode

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, 1.8 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 48 MHz			FCLK = 64 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	—	34.8	338.8	—	34.6	337.7	μs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	—	5.4	220.1	—	5.4	220.4	ms
	8-Kbyte	t_{DE8K}	—	104.8	2331.4	—	12.4	368.0	—	12.7	375.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	—	—	8.7	—	—	8.6	μs
	256-byte	t_{DBC256}	—	—	1573	—	—	115	—	—	120	μs
Erase operation forcible stop time		t_{DSED}	—	—	22.8	—	—	11.0	—	—	10.9	μs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.
Note 1. 2.4 V ≤ VCC ≤ 5.5 V

Table 2.86 E2 DataFlash Characteristics (3) Middle-speed operating mode

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 24 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	—	35.3	343.2	μs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	—	5.4	220.2	ms
	8-Kbyte	t_{DE8K}	—	104.8	2331.4	—	12.4	368.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	—	—	9.0	μs
	256-byte	t_{DBC256}	—	—	1573	—	—	0.1	ms
Erase operation forcible stop time		t_{DSED}	—	—	22.8	—	—	11.2	μs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 2.87 E2 DataFlash Characteristics (4) Middle-speed operating mode 2

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, 1.6 V ≤ AVCC0 ≤ 5.5 V, VSS = AVSS0 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +105°C

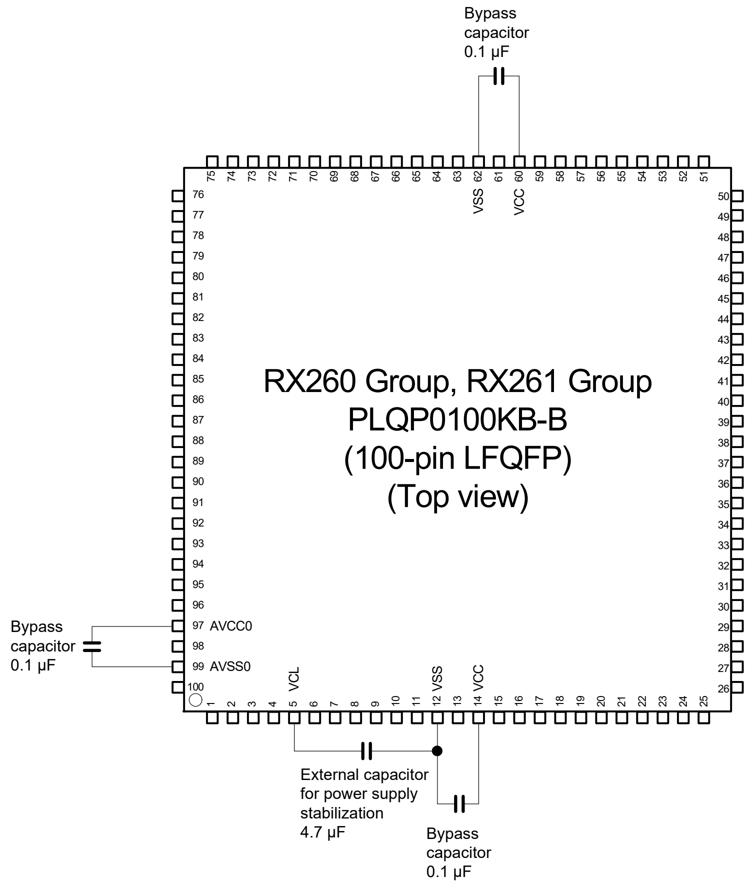
Item		Symbol	FCLK = 1 MHz			Unit
			Min.	Typ.	Max.	
Programming time	1-byte	t_{DP1}	—	83.0	729.5	μs
Erasure time	256-byte	t_{DE256}	—	8.3	282.0	ms
	8-Kbyte	t_{DE8K}	—	104.8	2331.4	ms
Blank check time	1-byte	t_{DBC1}	—	—	44.6	μs
	256-byte	t_{DBC256}	—	—	1573	ms
Erase operation forcible stop time		t_{DSED}	—	—	22.8	μs
DataFlash STOP recovery time		t_{DSTOP}	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory.
Note: The frequency accuracy of FCLK should be ±3.5%.

2.16 Usage Notes

2.16.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 2.77 to Figure 2.79 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User’s Manual: Hardware. For the capacitors related to analog modules, also see section 40, 12-Bit A/D Converter (S12ADE) in the User’s Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note “Hardware Design Guide” (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic capacitor for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.76 Connecting Capacitors (100 Pins)

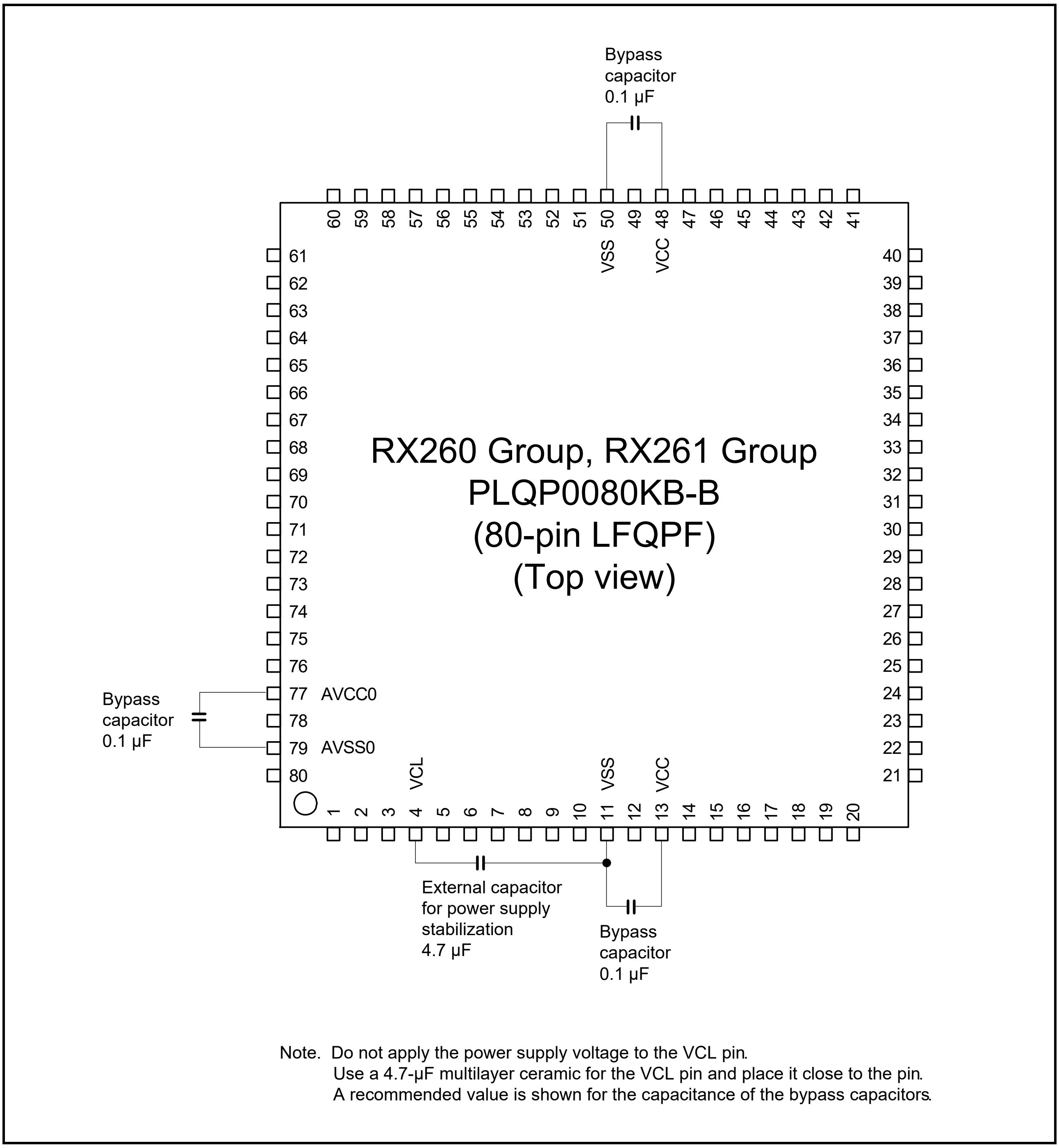
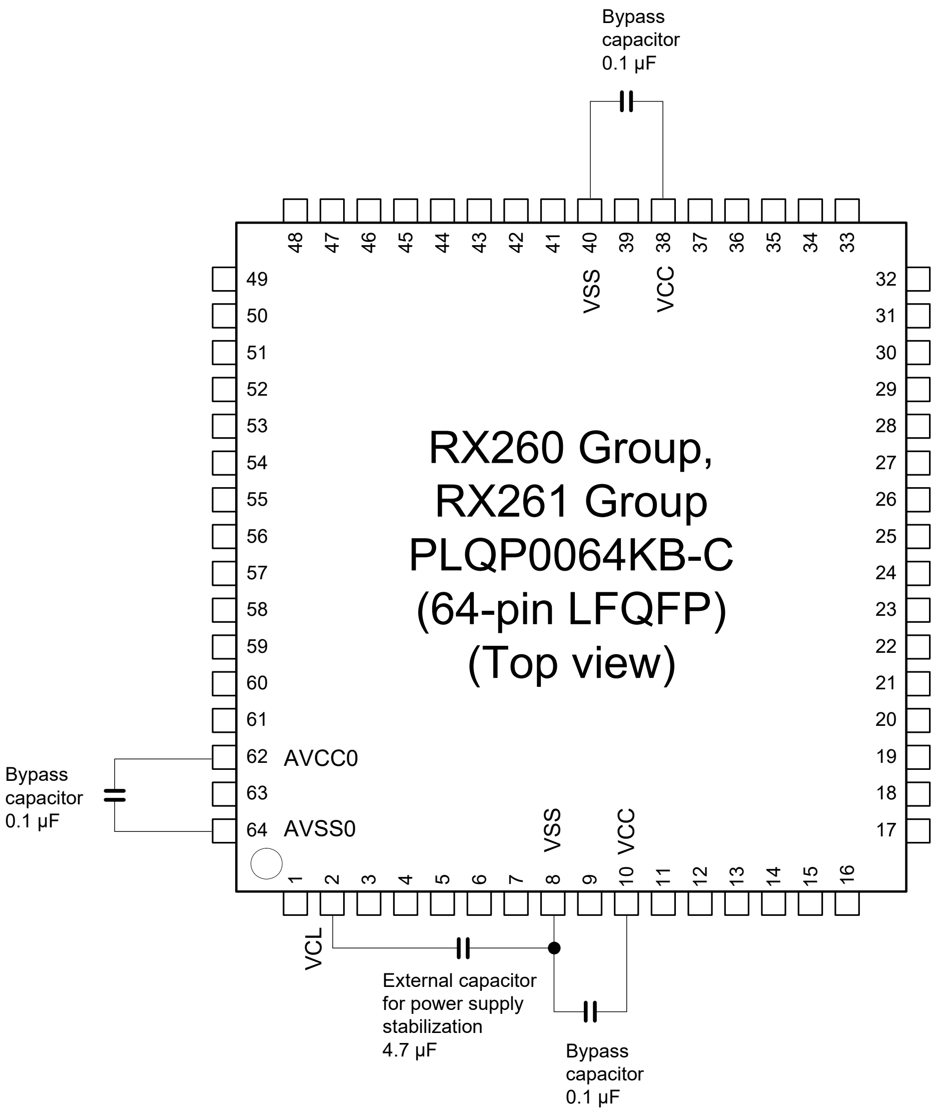
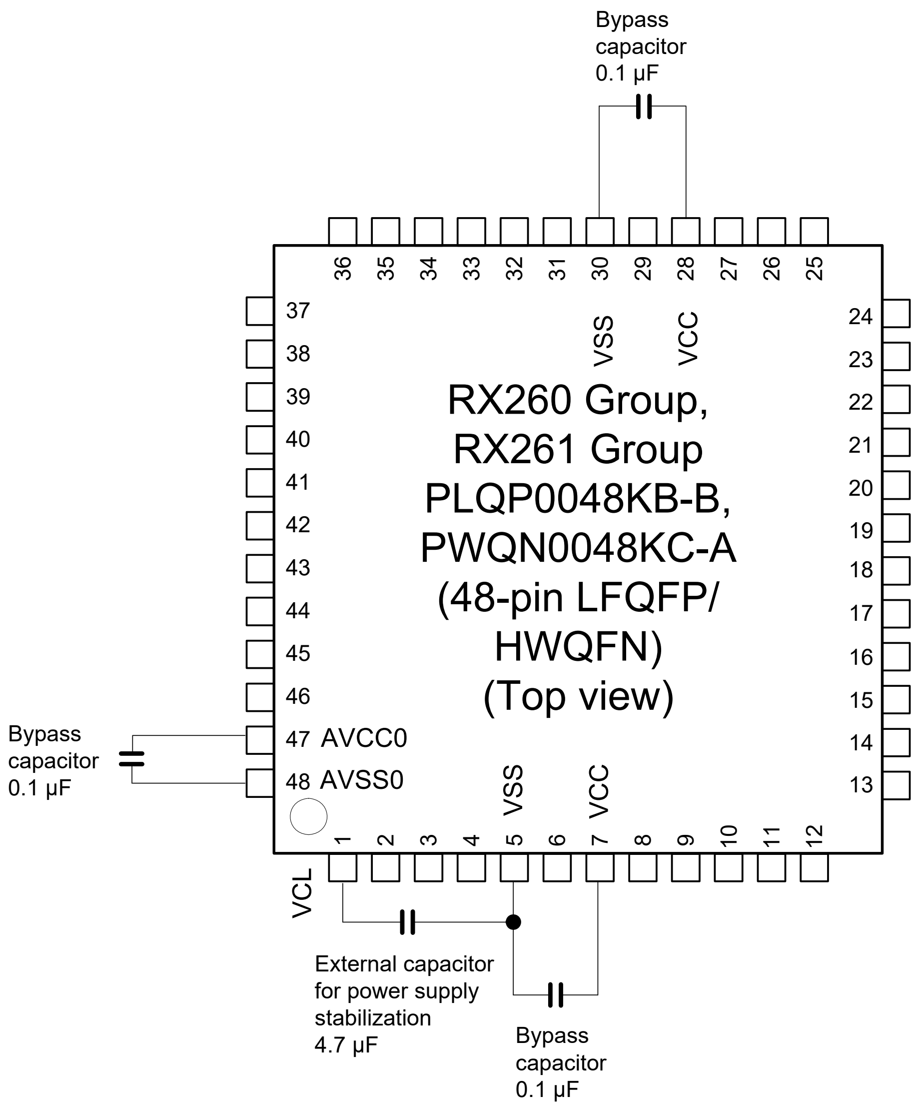


Figure 2.77 Connecting Capacitors (80 Pins)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 2.78 Connecting Capacitors (64 Pins)



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-μF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

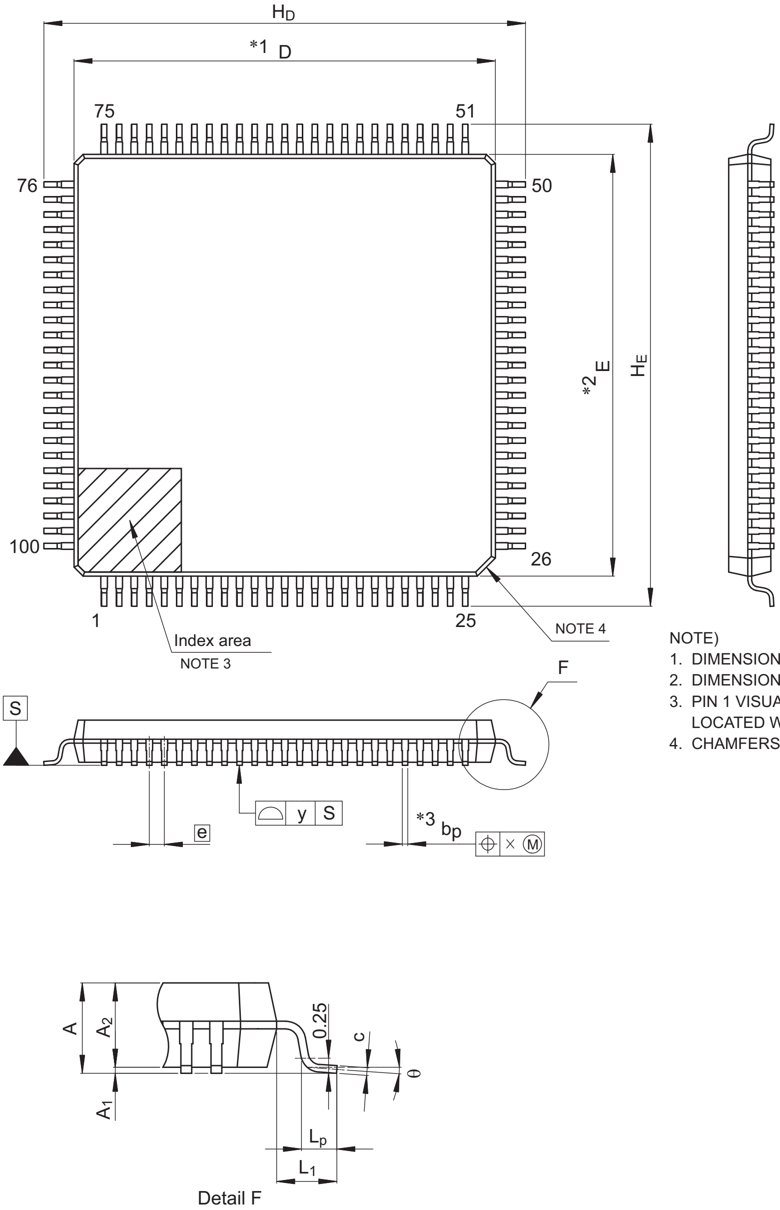
Figure 2.79 Connecting Capacitors (48 Pins)

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



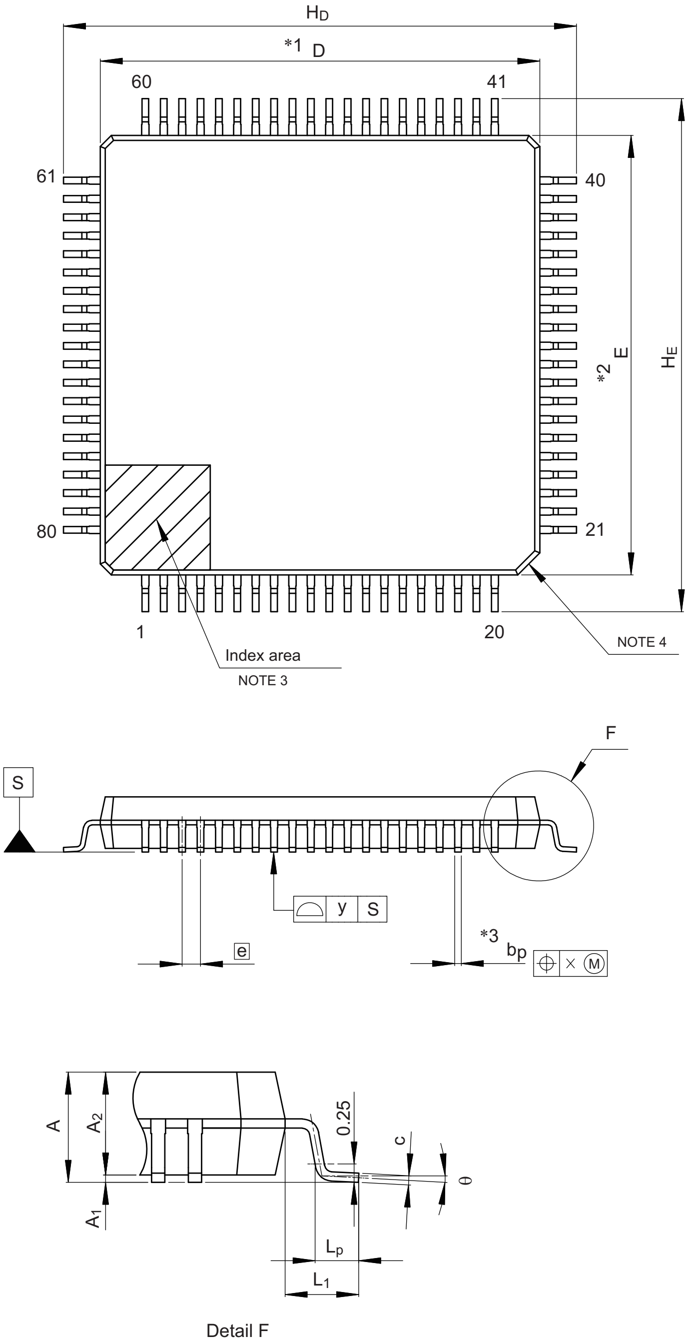
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



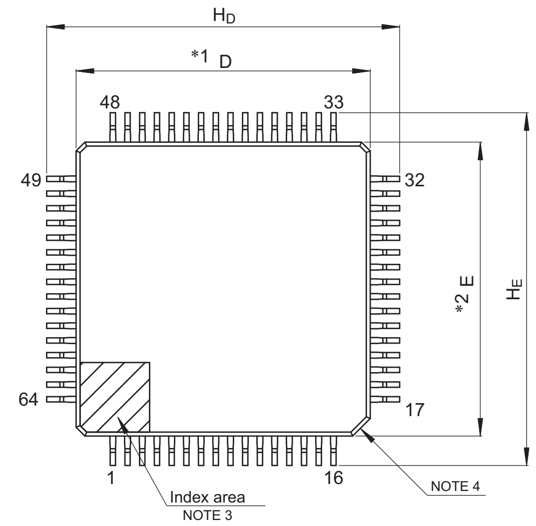
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

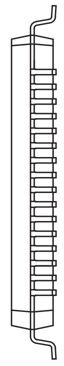
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

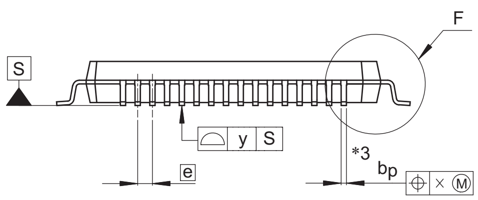
Figure B 80-Pin LFQFP (PLQP0080KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

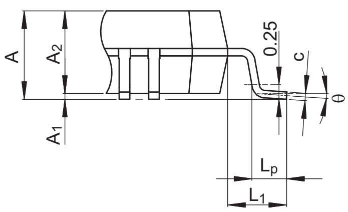
Unit: mm







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



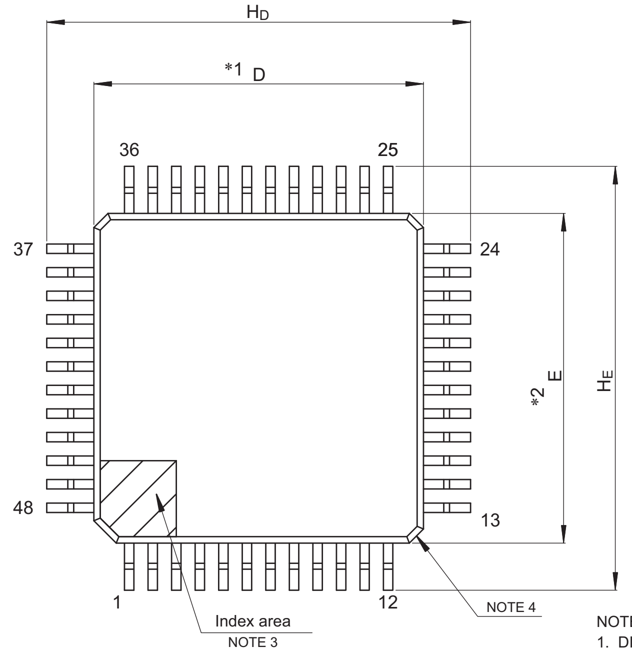
Detail F

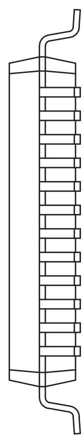
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

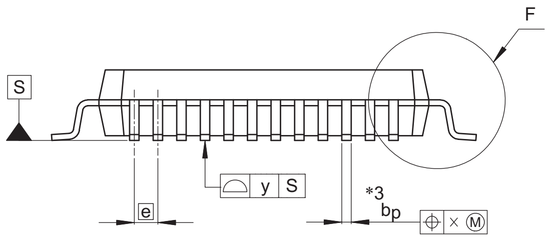
Figure C 64-Pin LFQFP (PLQP0064KB-C)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

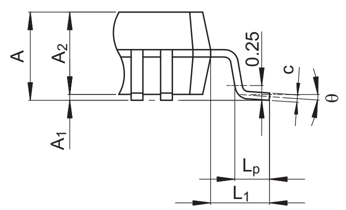
Unit: mm







NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

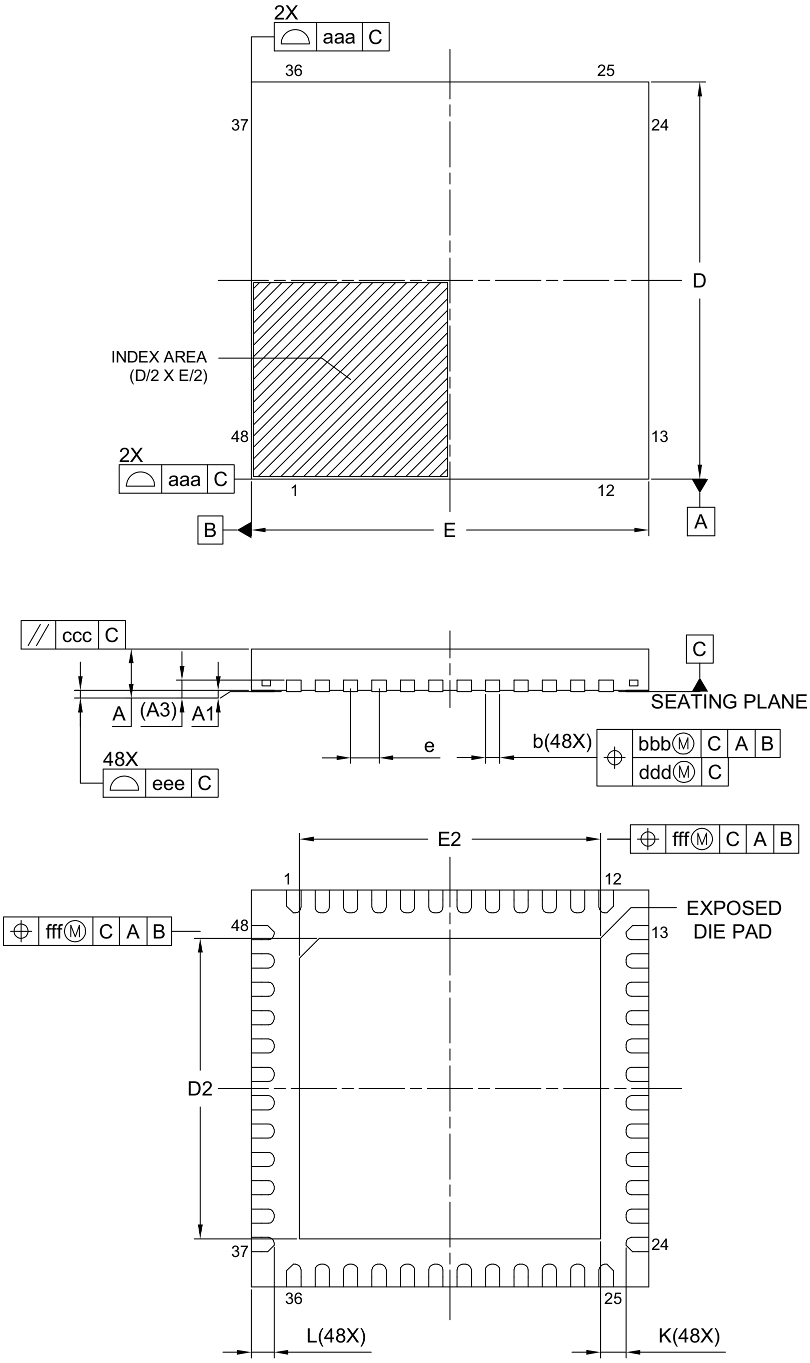


Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure D 48-Pin LFQFP (PLQP0048KB-B)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure E 48-Pin HWQFN (PWQN0048KC-A)

REVISION HISTORY	RX260 Group, RX261 Group Datasheet

Classifications
- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jul 31, 2024	—	First edition, issued	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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