

Section 1 Overview

1.1 Features

This LSI chip includes the AI dedicated accelerator (DRP-AI) and 4K-compatible image signal processor (ISP). This processor is vision-AI ASSP for real-time human and object recognition.

The AI dedicated hardware IP, DRP-AI, configured with the dynamic reconfigurable processor (DRP) and AI-MAC, combines both a high-speed AI inference and low power consumption and realizes 1TOPS/W class power performance. In addition, the image signal processor (ISP) is highly robust, producing a stable image independent of the environment, allowing for a high AI recognition accuracy. With these features, this LSI realizes low power consumption, which is a critical factor for embedded devices, making heat dissipation measures easier. The result is that it is ideal for vision AI applications in a wide range of embedded markets, including surveillance security, retail, office automation (OA), industrial automation, and robotics. In addition, this LSI also features abundant high-speed communication interfaces such as USB 3.1, PCI Express®, Gigabit Ethernet, and many CPU peripheral functions, so it can also be used in a variety of applications.

■ CPU and DDR Memory Interfaces

- Cortex®-A53 Dual (996 MHz maximum)
- 32-bit LPDDR4-3200

■ Vision and AI

- AI accelerator: DRP-AI (1.0 TOPS/W class)
- Image signal processor (ISP) with multi-stream capability
- Camera interface: 2× MIPI® CSI-2®
- Face and Human Detection Engine

■ Video and Graphics, Display

- H.265/H.264 Multi Codec
Encoding: H.265 up to 2160p30, H.264 up to 1080p60
Decoding: H.265 up to 2160p30, H.264 up to 1080p60
- 2D Graphics Engine: 200 MPixels/s
- Display: HDMI® 1.4a

■ High Speed Interfaces

- 1× Gigabit Ethernet
- 1× USB3.1 Gen1 Host/Peripheral
- 1× PCIe® Gen 2 (2 lanes)
- 2× SDIO 3.0
- 1× eMMC™ 4.5.1

■ Hardware Security Engine provided

■ Package

- FCBGA (15×15 mm, 0.5-mm pitch)

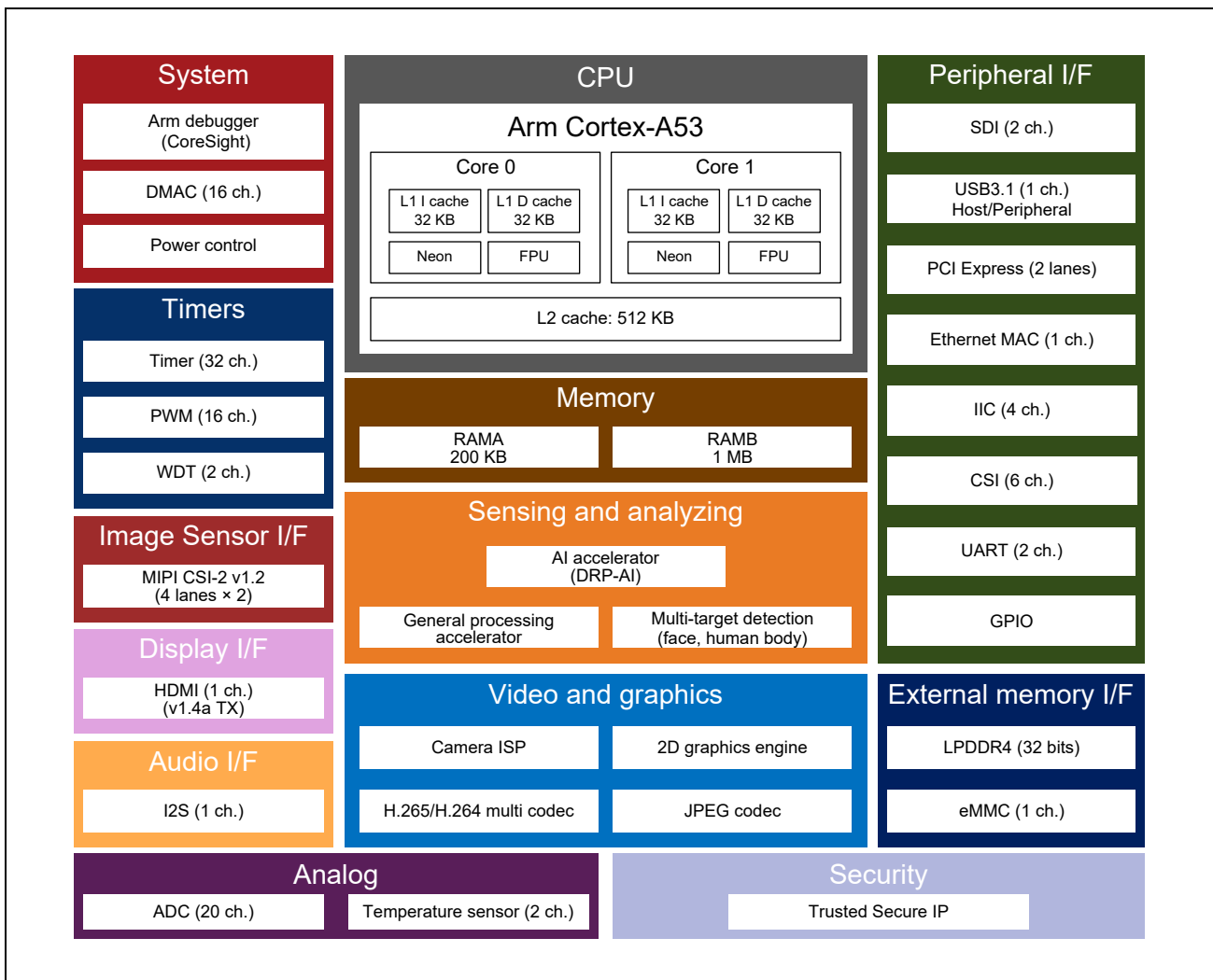


Figure 1.1-1 Diagram of Functional Overview

1.2 Product Lineup

The group currently consists of the following products.

Table 1.2-1 Product Lineup

Product Part Number	Part Number for Ordering	Package	Packing
R9A09G011GBG	R9A09G011GBG#ACC	PRBG0841KA-A	Individual tray
	R9A09G011GBG#BCC	PRBG0841KA-A	Full carton

1.3 Functions

Table 1.3-1 Overview of Functions (1/4)

Item	Function
CPU	<ul style="list-style-type: none"> • Arm® Cortex-A53 dual core (CA53): 996 MHz <ul style="list-style-type: none"> – L1 cache: 32 KB (for instructions) + 32 KB (for data) for each core – L2 cache: 512 KB – FPU, Neon™ extension – ECC supported • Debugger interface (JTAG/SWD) <ul style="list-style-type: none"> – CoreSight™ debugging components incorporated – ETF (64-Kbyte trace RAM), ETR, and STM incorporated – External trace output (16-bit width)
Memory	<ul style="list-style-type: none"> • RAM A (RAMA): 200 KB (with ECC) • RAM B (RAMB): 1 MB • ROM: 128 KB
Timers	<ul style="list-style-type: none"> • Watchdog timer (WDT): 2 channels (CA53 core 0, CA53 core 1) • Compare-match timer: 32 channels • Pulse-width modulation timer (PWM): 16 channels • Real-time clock (RTC)
DMA controller	DMA controller (16 channels)
CMOS image sensor interfaces	<ul style="list-style-type: none"> • MIPI CSI-2 Ver.1.2/ D-PHY Ver.1.2 4 lanes × 2, 2.5 Gbps per lane: Supports 2 sensor inputs • Formats: <ul style="list-style-type: none"> – RAW: 8/10/12 bits – YUV422: 8 bits*1 • Supports WDR extraction • Virtual channel
Audio interfaces	I2S interface for the external audio codec: 1 channel Audio sampling rate: 32 kHz, 44.1 kHz, 48 kHz
Sensing and analyzing	<ul style="list-style-type: none"> • AI accelerator (DRP-AI) • Multi-target detection (face, human body) • General-purpose accelerator

Note 1. The input of data in this format limits the available functions of the LSI chip. For details, contact a Renesas Electronics sales representative.

Table 1.3-1 Overview of Functions (2/4)

Item	Function
Video & graphics	<ul style="list-style-type: none"> • Camera ISP <ul style="list-style-type: none"> – 3840 × 2160 p × 30 fps / 1920 × 1080 p × 30 fps × 2 / 640 × 480 p × 800 fps supported – WDR processing – 3D noise reduction – Fisheye correction • H.265/H.264 multi codec <ul style="list-style-type: none"> – Supported functions <ul style="list-style-type: none"> H.265 encoding and H.265 decoding, or H.264 encoding and H.264 decoding – Support encoding/decoding standard <ul style="list-style-type: none"> H.265/HEVC main profile at level 5 H.264/AVC constrained baseline/main/high profile at level 4.2 – I/P-slice supported for H.264/H.265 encoding and decoding – H.265 encoding and decoding performance <ul style="list-style-type: none"> 3840 × 2160 p × 30 fps encoding, 3840 × 2160 p × 30 fps decoding 1920 × 1080 p × 60 fps encoding, 1920 × 1080 p × 60 fps decoding 640 × 480 p × 800 fps encoding – H.264 encoding and decoding performance <ul style="list-style-type: none"> 1920 × 1080 p × 60 fps encoding, 1920 × 1080 p × 60 fps decoding 640 × 480 p × 800 fps encoding • JPEG codec <ul style="list-style-type: none"> – JPEG extended DCT-based process/baseline-process compliant – Color format: YUV – Image data rate: Max. 16 samples/clock cycle • 2D graphics engine <ul style="list-style-type: none"> – 200 Mpixels per second fill rate (200-MHz clock, single pipeline) – 4096 × 4096 texture size
External memory interfaces	<ul style="list-style-type: none"> • LPDDR4 interface <ul style="list-style-type: none"> – 3200 Mbps – 32-bit data width – Up to 4 GB supported • eMMC interface conforming to eMMC version 4.51 <ul style="list-style-type: none"> – Supports HS200 (high-speed DDR and HS400 are not supported) – 1/4/8-bit data bus

Table 1.3-1 Overview of Functions (3/4)

Item	Function
Peripheral interfaces	<ul style="list-style-type: none"> • SD host interface (SDI): 2 channels (SD specification version 3.01 compliant) <ul style="list-style-type: none"> – SD memory / I/O card interface (1-bit/4-bit SD bus) – SD memory card access for SD, SDHC, and SDXC – Supports default, high-speed, UHS-I/SDR12, SDR25, SDR50, and SDR104 transfer modes (DDR50, not supported) – Supports card detection and write protection • USB interface: 1 channel <ul style="list-style-type: none"> – USB3.1 Gen1 standard compliant – Dual-role device function supported (static switching of the host controller function and the peripheral controller function) – Supports super-speed (5 Gbps), high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transfer (low-speed is only supported for the host controller) • PCI Express interface Gen2 (5GT/s): 2 lanes <ul style="list-style-type: none"> – PCI Express base specification revision 4.0 compliant – Supports root complex/endpoint • Ethernet MAC interface: 1 channel <ul style="list-style-type: none"> – Supports transfer at 1000 Mbps, and 100 Mbps in full-duplex mode – Supports IEEE802.3 PHY GMII, MII compliant interface • IIC bus interface: 4 channels • Clocked serial interface: 6 channels • UART: 2 channels • GPIO
Display interfaces	<ul style="list-style-type: none"> • Display control <ul style="list-style-type: none"> – Display control via HDMI – Resolution conversion, picture compositing, and image frame adjustment • HDMI Tx interface v1.4a: 1 channel <ul style="list-style-type: none"> – Supports DTV with 1280 × 720 p, 1920 × 1080 p resolution – YUV digital video output format, supported – HDCP™, CEC, and HEAC, not supported
Security engine	<ul style="list-style-type: none"> • AES and ARC4 encryption and decryption algorithms implemented • RSA2048 signature verification algorithm implemented • SHA-224/256 tamper proofing algorithms implemented • Hardware Random Number Generator
Analog	<ul style="list-style-type: none"> • A/D converter: 12 channels, A/D converter: 8 channels (12 bits, 600 ksamples /sec) • Temperature sensor: 2 channels
Power control	<ul style="list-style-type: none"> • External power supply sequence control • Internal power domain control

Table 1.3-1 Overview of Functions (4/4)

Item	Function
Power voltage	<ul style="list-style-type: none"> • 0.8-V power supply VDD08, RTVDD08, PWVDD08, LPVDD, PLDVDD08n (n = 1, 2, 3, 4, 6, 7), OTVDD08, TSnDVDD08A (n = 0, 1), LVRXAVDD, HDAVDD08, DSMSVDD0P8, PCVDD08, USDVDD, USVP, USVPTX • 1.1-V power supply LPVDDQ • 1.2-V power supply DSMVDD12 • 1.5-V power supply RTVDD • 1.8-V power supply PLVDDn (n = 1, 2, 3, 4, 6, 7), OTVDD18, TSnAVDD18 (n = 0, 1), ADnAVCCA (n = 0, 1), LVRXAVCC, LPVAA, HDAVDD18, DSMSVDD18, PCVDD18, USVDDH, PWVDD, VDD18, PAPREDVDD, PBPREDVDD, PCPREDVDD, IM0PREDVDD, IM1PREDVDD, NAPREDVDD, SD0PREDVDD, SD1FVDD, GEPREDVDD, PREDVDD33 • 3.3-V power supply USVD330, USVPH, VDD33 • 3.3-V/1.8-V switchable power supply PAMODVDD, PBMODVDD, PCMODVDD, IM0MODVDD, IM1MODVDD, NAMODVDD, SD0MODVDD, SD1FVDD, GEMODVDD
Operating temperature	Tj = 103°C (max.) Tj: Junction temperature

Table 2.1-1 Ball Numbers and External Pin Names (1/5)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
A1	LVRXAVSS	B17	GND	D4	LVRXD5P	E20	AD0AIN6
A2	LVRXD6M	B18	SD0WP	D5	LVRXAVCC	E21	AD0AIN2
A3	LVRXAVSS	B19	AD1AIN5	D6	LVRXD3P	E22	PWCTEST0
A4	LVRXD4M	B20	AD0AIN11	D7	LVRXAVSS	E23	PWEN4
A5	LVRXAVCC	B21	AD0AIN9	D8	LVRXD1P	E24	PWEN2
A6	LVRXD2M	B22	GND	D9	LVRXAVSS	E25	PWOUT1
A7	LVRXAVSS	B23	PWCTEST1	D10	PCREFCKM	E26	GND
A8	LVRXD0M	B24	PWSD0SEL	D11	GND	E27	GND
A9	LVRXAVCC	B25	GND	D12	PCRXD0P	E28	LPDQA10
A10	LVRXREXT	B26	PWOUT0	D13	GND	E29	LPDQSAC1
A11	PCTXD0M	B27	PWDETRSTN	D14	PCRXD1P	F1	IM1TXD
A12	GND	B28	RTRSTN	D15	GND	F2	IM1SIG0
A13	PCTXD1M	B29	RTXIN	D16	SD0DAT3	F3	IM0CLK
A14	GND	C1	LVRXAVSS	D17	SD0DAT2	F4	IM0SIG0
A15	PCREXT	C2	LVRXD7M	D18	SD0CLK	F5	LVRXAVSS
A16	SD1FVDD	C3	LVRXAVSS	D19	AD1AIN1	F6	LVRXCK1P
A17	SD1FMODVDD	C4	LVRXD5M	D20	AD0AIN4	F7	LVRXAVSS
A18	SD0MODVDD	C5	LVRXAVCC	D21	AD0AIN3	F8	LVRXCK0P
A19	AD1AIN7	C6	LVRXD3M	D22	PWMEMSWIENA	F9	LVRXAVSS
A20	AD0AIN8	C7	LVRXAVSS	D23	PWSD1SEL	F10	LVRXAVSS
A21	AD0AIN10	C8	LVRXD1M	D24	PWEN5	F11	LVRXAVSS
A22	PWVDD	C9	LVRXAVSS	D25	PWEN3	F12	GND
A23	PWVDD08	C10	PCREFCKP	D26	PWKY3N	F13	PCVDD18
A24	RTVDD08	C11	GND	D27	PWRSTN	F14	PCVDD18
A25	RTVDD	C12	PCRXD0M	D28	GND	F15	SD1FWP
A26	PWKY1N	C13	GND	D29	LPDQSAT1	F16	SD1FDAT0
A27	PWEN1	C14	PCRXD1M	E1	IM0SCLK	F17	SD0CD
A28	RTXOUT	C15	GND	E2	GND	F18	AD1AIN2
A29	GND	C16	SD1FDAT1	E3	IM0RXD	F19	AD1AVSSA
B1	LVRXAVSS	C17	SD1FCLK	E4	LVRXAVSS	F20	AD0AVSSA
B2	LVRXD6P	C18	SD0DAT1	E5	LVRXAVSS	F21	AD0AIN1
B3	LVRXAVSS	C19	AD1AIN4	E6	LVRXCK1M	F22	GND
B4	LVRXD4P	C20	AD0AIN7	E7	LVRXAVSS	F23	PWKY4N
B5	LVRXAVCC	C21	AD0AIN5	E8	LVRXCK0M	F24	PWEN0
B6	LVRXD2P	C22	PWTEST	E9	LVRXAVSS	F25	GND
B7	LVRXAVSS	C23	PWPWM	E10	LVRXAVSS	F26	LPDQA9
B8	LVRXD0P	C24	PWKY2N	E11	GND	F27	LPDMDBIA1
B9	LVRXAVCC	C25	PWVBAT	E12	GND	F28	LPDQA11
B10	GND	C26	PWKY0N	E13	GND	F29	LPDQA14
B11	PCTXD0P	C27	PWISO	E14	GND	G1	IM0VS
B12	GND	C28	RTISO	E15	SD1FDAT3	G2	IM1CS
B13	PCTXD1P	C29	GND	E16	SD1FCMD	G3	IM1RXD
B14	GND	D1	LVRXAVSS	E17	SD0CMD	G4	CSTXD5
B15	GND	D2	LVRXD7P	E18	AD1AIN6	G5	CSRXD4
B16	SD1FCD	D3	LVRXAVSS	E19	AD1AIN3	G6	GND

Table 2.1-1 Ball Numbers and External Pin Names (2/5)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
G7	CSSCLK4	H23	GND	K10	TS0DVDD08A	L26	LPDQSAC0
G8	GND	H24	GND	K11	GND	L27	LPDQA7
G9	LVRXAVSS	H25	GND	K12	GND	L28	GND
G10	LVRXAVSS	H26	LPVDDQ	K13	VDD08	L29	LPDQA4
G11	LVRXAVSS	H27	LPVDDQ	K14	VDD08	M1	PBPREDVDD
G12	LVRXAVSS	H28	LPVDDQ	K15	GND	M2	IM1SCLK
G13	PCVDD18	H29	LPVDDQ	K16	GND	M3	IMSTSIG1
G14	PCVDD18	J1	OTVDD18	K17	VDD08	M4	IMSTSIG0
G15	SD1FDAT2	J2	TS0AVDD18	K18	VDD08	M5	IM0SIG1
G16	GND	J3	GND	K19	GND	M6	IM0CS
G17	SD0DAT0	J4	AUMCLK	K20	GND	M7	PM9
G18	AD1AIN0	J5	GND	K21	GND	M8	MD8
G19	AD1AVCCA	J6	AUPLLCLK	K22	GND	M9	VDD08
G20	AD0AVCCA	J7	PM13	K23	GND	M10	VDD08
G21	AD0AIN0	J8	PM11	K24	LPDQA0	M11	GND
G22	GND	J9	GND	K25	GND	M12	GND
G23	PWSYSRSTN	J10	GND	K26	LPDQSAT0	M13	VDD08
G24	GND	J11	VDD08	K27	LPDQA3	M14	VDD08
G25	LPDQA8	J12	VDD08	K28	LPDQA5	M15	GND
G26	LPDQA13	J13	GND	K29	GND	M16	GND
G27	LPDQA15	J14	GND	L1	IM1HS	M17	VDD08
G28	GND	J15	VDD08	L2	IM1VS	M18	VDD08
G29	LPDQA12	J16	VDD08	L3	IM1SIG1	M19	GND
H1	IM1CLK	J17	GND	L4	IM0SIG2	M20	GND
H2	IM1SIG2	J18	GND	L5	IM0TXD	M21	LPVDD
H3	CSRXD5	J19	VDD08	L6	PM15	M22	GND
H4	CSCS5	J20	VDD08	L7	PM8	M23	GND
H5	CSSCLK5	J21	GND	L8	PM10	M24	GND
H6	CSCS4	J22	GND	L9	GND	M25	GND
H7	CSTXD4	J23	GND	L10	GND	M26	LPVDDQ
H8	GND	J24	GND	L11	VDD08	M27	LPVDDQ
H9	LVRXAVDD	J25	LPDQA2	L12	VDD08	M28	LPVDDQ
H10	LVRXAVDD	J26	LPDQA1	L13	GND	M29	LPVDDQ
H11	LVRXAVDD	J27	LPDMDBIA0	L14	GND	N1	PBMODVDD
H12	LVRXAVDD	J28	GND	L15	VDD08	N2	PBMODVDD
H13	PCVDD08	J29	LPDQA6	L16	VDD08	N3	GND
H14	PCVDD08	K1	IM0HS	L17	GND	N4	IMSHUT1
H15	GND	K2	AUDI	L18	GND	N5	IMSHUT0
H16	GND	K3	AUDO	L19	VDD08	N6	RETEST0
H17	SD0PREDVDD	K4	AULRCK	L20	VDD08	N7	MTRXD0
H18	GND	K5	AUBICK	L21	LPVDD	N8	MTDCPLS1
H19	GND	K6	GND	L22	GND	N9	GND
H20	GND	K7	PM14	L23	GND	N10	GND
H21	GND	K8	PM12	L24	LPCAA3	N11	VDD08
H22	GND	K9	OTVDD08	L25	LPCAA4	N12	VDD08

Table 2.1-1 Ball Numbers and External Pin Names (3/5)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
N13	GND	P29	GND	T16	PLVDD1	V3	GND
N14	GND	R1	MTDRV6	T17	VDD08	V4	DETDI
N15	VDD08	R2	USPWEN	T18	VDD08	V5	DETKC
N16	VDD08	R3	MTDRV3	T19	PLVSS3	V6	USOVC
N17	GND	R4	MTCS1	T20	PLVDD3	V7	PCRSTOUTB
N18	GND	R5	MTCS0	T21	LPVDD	V8	MD0
N19	VDD08	R6	MTDCPLS0	T22	GND	V9	VDD08
N20	VDD08	R7	MTDCPLS3	T23	GND	V10	VDD08
N21	LPVDD	R8	MTDRV0	T24	GND	V11	GND
N22	GND	R9	GND	T25	GND	V12	GND
N23	GND	R10	GND	T26	LPVDDQ	V13	VDD08
N24	LPCAA2	R11	VDD08	T27	LPVDDQ	V14	VDD08
N25	LPCAA5	R12	VDD08	T28	LPVDDQ	V15	GND
N26	LPCAA0	R13	PLVSS6	T29	LPVDDQ	V16	GND
N27	LPCKEA0	R14	PLVSS4	U1	IM0MODVDD	V17	VDD08
N28	GND	R15	PLVSS2	U2	IM1MODVDD	V18	VDD08
N29	LPCSA0	R16	PLVSS1	U3	DESRSTN	V19	GND
P1	MTSCLK0	R17	GND	U4	DETMS	V20	GND
P2	MTSCLK1	R18	GND	U5	GND	V21	LPVDD
P3	DETRSTN	R19	PLDVDD083	U6	MTTXD1	V22	GND
P4	MTDRV7	R20	GND	U7	MTTXD0	V23	GND
P5	GND	R21	LPVDD	U8	MTDRV2	V24	GND
P6	MTDRV1	R22	GND	U9	GND	V25	LPCSB0
P7	MTDCPLS2	R23	LPATEST	U10	GND	V26	LPCSB1
P8	RETEST1	R24	LPCLKAC	U11	VDD08	V27	LPCAB1
P9	VDD08	R25	LPCAB4	U12	VDD08	V28	GND
P10	VDD08	R26	LPCAB5	U13	GND	V29	LPZN
P11	GND	R27	LPCAB2	U14	GND	W1	INEXINT6
P12	GND	R28	GND	U15	VDD08	W2	INEXINT2
P13	PLDVDD086	R29	LPMRESETL	U16	VDD08	W3	INEXINT0
P14	PLDVDD084	T1	IM0PREDVDD	U17	GND	W4	INEXINT1
P15	PLDVDD082	T2	IM1PREDVDD	U18	GND	W5	DETDO
P16	PLDVDD081	T3	PREDVDD33	U19	TS1DVDD08A	W6	INEXINT5
P17	VDD08	T4	GND	U20	TS1AVDD18	W7	MD2
P18	VDD08	T5	MTRXD1	U21	LPVDD	W8	MD1
P19	GND	T6	MTDRV4	U22	GND	W9	GND
P20	GND	T7	MTDRV5	U23	LPDTEST	W10	GND
P21	LPVDD	T8	GND	U24	LPCAB3	W11	VDD08
P22	GND	T9	VDD08	U25	LPCLKBC	W12	VDD08
P23	GND	T10	VDD08	U26	LPCLKBT	W13	GND
P24	LPCLKAT	T11	GND	U27	GND	W14	GND
P25	GND	T12	GND	U28	LPVAA	W15	VDD08
P26	LPCSA1	T13	PLVDD6	U29	LPVAA	W16	VDD08
P27	LPCKEA1	T14	PLVDD4	V1	VDD33	W17	PLVDD7
P28	LPCAA1	T15	PLVDD2	V2	VDD33	W18	GND

Table 2.1-1 Ball Numbers and External Pin Names (4/5)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
W19	VDD08	AA6	INEXINT4	AB22	GND	AD9	PM2
W20	VDD08	AA7	MD6	AB23	GND	AD10	PM6
W21	LPVDD	AA8	MD5	AB24	LPDQB0	AD11	GERXD2
W22	GND	AA9	GND	AB25	LPDQB2	AD12	GERXD6
W23	GND	AA10	GND	AB26	LPDQB1	AD13	GND
W24	LPDQB4	AA11	VDD08	AB27	LPDQB6	AD14	USTX0P
W25	GND	AA12	VDD08	AB28	GND	AD15	GND
W26	LPCAB0	AA13	GND	AB29	LPDMDBIB0	AD16	GND
W27	LPCKEB1	AA14	GND	AC1	PCPREDVDD	AD17	HDTX0P
W28	LPCKEB0	AA15	USDVDD	AC2	P0605	AD18	HDTX1P
W29	GND	AA16	USDVDD	AC3	P0607	AD19	GND
Y1	VDD18	AA17	PLDVDD087	AC4	P0603	AD20	DSMDPDATA2
Y2	VDD18	AA18	HDAVDD08	AC5	P0611	AD21	DSMDPDATA1
Y3	GND	AA19	DSMSVDD0P8	AC6	P0604	AD22	GND
Y4	INEXINT7	AA20	DSMSVDD0P8	AC7	P0601	AD23	NADAT1
Y5	INEXINT3	AA21	GND	AC8	P0602	AD24	GND
Y6	MD3	AA22	GND	AC9	GND	AD25	LPDQB8
Y7	MD7	AA23	GND	AC10	PM3	AD26	LPDQB9
Y8	MD4	AA24	LPDQSBT0	AC11	GND	AD27	LPDQB13
Y9	VDD08	AA25	LPDQSBC0	AC12	GERXD4	AD28	GND
Y10	VDD08	AA26	LPDQB3	AC13	GND	AD29	LPDQB12
Y11	GND	AA27	LPDQB5	AC14	USTX0M	AE1	CSRXD1
Y12	GND	AA28	LPDQB7	AC15	GND	AE2	CSSCLK1
Y13	VDD08	AA29	GND	AC16	GND	AE3	CSTXD1
Y14	VDD08	AB1	PCMODVDD	AC17	HDTX0M	AE4	CSCS1
Y15	GND	AB2	GND	AC18	HDTX1M	AE5	CSSCLK2
Y16	GND	AB3	P0609	AC19	GND	AE6	CSRXD2
Y17	PLVSS7	AB4	GND	AC20	DSSDPCLK	AE7	PM5
Y18	HDAVDD08	AB5	P0606	AC21	DSSDPDATA0	AE8	PM7
Y19	GND	AB6	P0610	AC22	GND	AE9	GND
Y20	GND	AB7	P0608	AC23	GND	AE10	GERXER
Y21	DSMSVDD18	AB8	P0600	AC24	GND	AE11	GERXD1
Y22	DSMSVDD18	AB9	GND	AC25	GND	AE12	GND
Y23	GND	AB10	GND	AC26	LPVDDQ	AE13	USDM
Y24	GND	AB11	GND	AC27	LPVDDQ	AE14	GND
Y25	GND	AB12	GND	AC28	LPVDDQ	AE15	USRX0M
Y26	LPVDDQ	AB13	RSTN	AC29	LPVDDQ	AE16	GND
Y27	LPVDDQ	AB14	GND	AD1	CSSCLK0	AE17	GND
Y28	LPVDDQ	AB15	USVPTX	AD2	CSCS0	AE18	GND
Y29	LPVDDQ	AB16	USVP	AD3	CSTXD0	AE19	GND
AA1	I2SDA1	AB17	GND	AD4	CSRXD0	AE20	DSMDNDATA2
AA2	I2SDA0	AB18	GND	AD5	CSTXD2	AE21	DSMDNDATA1
AA3	I2SCL1	AB19	VDD18	AD6	CSCS2	AE22	GND
AA4	I2SCL0	AB20	DSSDNCLK	AD7	PM0	AE23	NADAT7
AA5	GND	AB21	DSSDNDATA0	AD8	PM1	AE24	NAWEN

Table 2.1-1 Ball Numbers and External Pin Names (5/5)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
AE25	GND	AF27	GND	AG29	LPDQSBT1	AJ2	GERXD3
AE26	LPDQB10	AF28	LPDQB11	AH1	GETXEN	AJ3	GERXD7
AE27	LPDMDBIB1	AF29	LPDQSBC1	AH2	GECLK	AJ4	GEMDC
AE28	LPDQB14	AG1	GETXD0	AH3	GERXD0	AJ5	GEPSS
AE29	LPDQB15	AG2	GETXC	AH4	GETXD1	AJ6	GECOL
AF1	CSRXD3	AG3	GETXD7	AH5	GETXD2	AJ7	PAMODVDD
AF2	GND	AG4	GETXD5	AH6	GEMDIO	AJ8	PAPREDVDD
AF3	CSTXD3	AG5	GETXD6	AH7	PAMODVDD	AJ9	GEPREDVDD
AF4	CSCS3	AG6	GEGTXCLK	AH8	GND	AJ10	GEMODVDD
AF5	GND	AG7	GND	AH9	GETXER	AJ11	XIN
AF6	CSSCLK3	AG8	GETXD4	AH10	GEMODVDD	AJ12	XOUT
AF7	PM4	AG9	GELINK	AH11	GND	AJ13	USRESREF
AF8	GETXD3	AG10	GND	AH12	GND	AJ14	USVD330
AF9	GEINT	AG11	GERXC	AH13	USVBUS	AJ15	USVDDH
AF10	GERXDV	AG12	GERXD5	AH14	USVPH	AJ16	HDREXT
AF11	GECRS	AG13	GND	AH15	GND	AJ17	HDHPD
AF12	GND	AG14	USOTGID	AH16	HDSCL	AJ18	HSDSA
AF13	USDP	AG15	GND	AH17	GND	AJ19	HDAVDD18
AF14	GND	AG16	GND	AH18	GND	AJ20	DSMVREG0P4V
AF15	USRX0P	AG17	HDTXCP	AH19	HDAVDD18	AJ21	GND
AF16	GND	AG18	HDTX2P	AH20	GND	AJ22	DSMDNDATA0
AF17	HDTXCM	AG19	GND	AH21	GND	AJ23	DSMVDD12
AF18	HDTX2M	AG20	DSMDNDATA3	AH22	DSMDPDATA0	AJ24	NADAT4
AF19	GND	AG21	DSMDPCLK	AH23	DSMVDD12	AJ25	NAMODVDD
AF20	DSMDPDATA3	AG22	GND	AH24	NADAT6	AJ26	NAPREDVDD
AF21	DSMDNCLK	AG23	GND	AH25	NAMODVDD	AJ27	NADAT5
AF22	GND	AG24	NADAT0	AH26	GND	AJ28	NAWPN
AF23	NADAT2	AG25	GND	AH27	NAREN	AJ29	GND
AF24	NADAT3	AG26	NACLE	AH28	NARBN	—	—
AF25	NACEN	AG27	NAALE	AH29	GND	—	—
AF26	GND	AG28	GND	AJ1	GND	—	—

2.2 External Pins

2.2.1 List of External Pins

Table 2.2-1 List of External Pins (1/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
RTXIN	I	1.5	1.5-V OSC	CLOCK	Pull down	—	—	—	—	—
RTXOUT	O	1.5	1.5-V OSC	CLOCK	Open	—	—	—	—	—
RTRSTN	I	1.5	RTC I/O	Don't care	Pull down	●	—	—	—	—
RTISO	I	1.5	RTC I/O	Hi-Z	Pull up	●	—	—	—	—
RTVDD	—	1.5	RTC I/O, 1.5-V OSC power supply	—	—	—	—	—	—	—
RTVDD08	—	0.8	RTC core power supply	—	—	—	—	—	—	—
PWRSTN	I	1.8	PWC I/O	Don't care	Pull down	●	—	—	—	—
PWTEST	I	1.8	PWC I/O	Don't care	Pull down	●	—	—	—	—
PWVBAT	I	1.8	PWC I/O	Don't care	Pull up*4	●	—	—	—	—
PWKY0N	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWKY1N	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWKY2N	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWKY3N	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWKY4N	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWDETRSTN	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWEN0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN1	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN2	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN3	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN4	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN5	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSYSRSTN	O	1.8	PWC I/O	L	Open	—	—	●	Fixed*2	—
PWOUT0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWOUT1	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWPWM	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSD0SEL	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSD1SEL	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWCTEST0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWCTEST1	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWMEMSWIENA	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWISO	O	1.8	PWC I/O	Hi-Z	Open	—	—	●	Fixed*2	—
PWVDD08	—	0.8	PWC core power supply	—	—	—	—	—	—	—
PWVDD	—	1.8	PWC I/O power supply	—	—	—	—	—	—	—
NADAT0	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NADAT1	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NADAT2	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)

Table 2.2-1 List of External Pins (2/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
NADAT3	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NADAT4	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NADAT5	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NADAT6	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NADAT7	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NACEN	IO	3.3/1.8	PORT00 I/O	PU	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NAREN	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NAWEN	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NACLE	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NAALE	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NARBN	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-3)
NAWPN	O	3.3/1.8	PORT00 I/O	L	Open	—	—	—	Selectable*2	—
NAMODVDD	—	3.3/1.8	PORT00 I/O power supply	—	—	—	—	—	—	—
NAPREDVDD	—	1.8	PORT00 pre-driver power supply	—	—	—	—	—	—	—
PM0*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM1*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM2*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM3*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)

Table 2.2-1 List of External Pins (3/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
PM4*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM5*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM6*3	IO	3.3/1.8	PORT01(A) I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM7*3	IO	3.3/1.8	PORT01(A) I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PAMODVDD	—	3.3/1.8	PORT01(A), PORT03 I/O power supply	—	—	—	—	—	—	—
PAPREDVDD	—	1.8	PORT01(A), PORT03 pre-driver power supply	—	—	—	—	—	—	—
PM8	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM9	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM10	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM11	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM12	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM13	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM14	IO	3.3/1.8	PORT01(B) I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PM15*3	IO	3.3/1.8	PORT01(B) I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-4)
PBMODVDD	—	3.3/1.8	PORT01(B), PORT04, PORT07, PORT21 I/O power supply	—	—	—	—	—	—	—
PBPREDVDD	—	1.8	PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	—	—	—	—	—	—	—
INEXINT0*1,*3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)

Table 2.2-1 List of External Pins (4/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
INEXINT1*1,*3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
INEXINT2*1,*3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
INEXINT3*1,*3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
INEXINT4*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
INEXINT5*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
INEXINT6*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
INEXINT7*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-5)
CSTXD0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSRXD0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSSCLK0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSCS0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSTXD1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSRXD1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSSCLK1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSCS1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSTXD2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSRXD2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)

Table 2.2-1 List of External Pins (5/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
CSSCLK2*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSCS2*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSTXD3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSRXD3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSSCLK3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSCS3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-6)
CSTXD4	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSRXD4	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSSCLK4	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSCS4	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSTXD5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSRXD5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSSCLK5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
CSCS5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-7)
I2SDA0*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-8)
I2SCL0*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-8)
I2SDA1*1,*3	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-8)

Table 2.2-1 List of External Pins (6/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
I2SCL1*1,*3	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-8)
P0600*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0601*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0602*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0603*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0604*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0605*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0606*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0607*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0608	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0609	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0610	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
P0611	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-9)
PCMODVDD	—	3.3/1.8	PORT06 I/O power supply	—	—	—	—	—	—	—
PCPREDVDD	—	1.8	PORT06 pre-driver power supply	—	—	—	—	—	—	—
AULRCK*3	IO	3.3/1.8	PORT07 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-10)
AUBICK*3	IO	3.3/1.8	PORT07 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-10)
AUDI*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-10)

Table 2.2-1 List of External Pins (7/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
AUDO*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-10)
AUMCLK*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-10)
AUPLLCLK*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-10)
SD0CMD	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0CLK	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0DAT0	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0DAT1	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0DAT2	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0DAT3	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0WP	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0CD	IO	3.3/1.8	PORT08 I/O	PU	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-11)
SD0MODVDD	—	3.3/1.8	PORT08 I/O power supply	—	—	—	—	—	—	—
SD0PREDVDD	—	1.8	PORT08 pre-driver power supply	—	—	—	—	—	—	—
SD1FCMD	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FCLK	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FDAT0	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FDAT1	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FDAT2	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)

Table 2.2-1 List of External Pins (8/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
SD1FDAT3	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FWP	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FCD	IO	3.3/1.8	PORT09 I/O	PU	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-12)
SD1FMODVDD	—	3.3/1.8	PORT09 I/O power supply	—	—	—	—	—	—	—
SD1FVDD	—	1.8	PORT09 pre-driver power supply	—	—	—	—	—	—	—
IM0VS*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0HS*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0CLK*3	O	3.3/1.8	PORT10 I/O	L	Open	—	PU/PD/OFF changeable	—	Selectable*2	—
IM0CS*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0TXD*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0RXD*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0SCLK*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0SIG0*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0SIG1*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0SIG2*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-13)
IM0MODVDD	—	3.3/1.8	PORT10 I/O power supply	—	—	—	—	—	—	—
IM0PREDVDD	—	1.8	PORT10 pre-driver power supply	—	—	—	—	—	—	—
IM1VS*3	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1HS*3	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1CLK*3	O	3.3/1.8	PORT11 I/O	L	Open	—	—	—	Selectable*2	—

Table 2.2-1 List of External Pins (9/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
IM1CS* ³	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1TXD* ³	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1RXD* ³	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1SCLK* ³	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1SIG0* ³	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1SIG1* ³	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1SIG2* ³	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-14)
IM1MODVDD	—	3.3/1.8	PORT11 I/O power supply	—	—	—	—	—	—	—
IM1PREDVDD	—	1.8	PORT11 pre-driver power supply	—	—	—	—	—	—	—
IMSHUT0* ³	IO	3.3	PORT12 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-15)
IMSHUT1* ³	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-15)
IMSTSIG0* ³	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-15)
IMSTSIG1* ³	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-15)
MTDRV0* ³	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDRV1* ³	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDRV2* ³	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDRV3* ³	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDRV4* ³	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable* ²	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)

Table 2.2-1 List of External Pins (10/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
MTDRV5*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDRV6*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDRV7*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDCPLS0*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDCPLS1*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDCPLS2*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTDCPLS3*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-16)
MTCS0*3	IO	3.3	PORT14 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTTXD0*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTRXD0*3	IO	3.3	PORT14 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTSCLK0*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTCS1*3	IO	3.3	PORT14 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTTXD1*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTRXD1*3	IO	3.3	PORT14 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
MTSCLK1*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-17)
GETXC	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXEN	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)

Table 2.2-1 List of External Pins (11/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
GETXER	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD0	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD1	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD2	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD3	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD4	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD5	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD6	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GETXD7	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GERXC	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GERXDV	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GERXER	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GERXD0	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GERXD1	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-18)
GERXD2	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GERXD3	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GERXD4	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)

Table 2.2-1 List of External Pins (12/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
GERXD5	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GERXD6	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GERXD7	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GE CRS	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GE COL	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GEMDC	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GEMDIO	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GEGTXCLK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GELINK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GEINT	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GECLK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-19)
GEPPS	IO	3.3/1.8	PORT17 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-20)
GEMODVDD	—	3.3/1.8	PORT15, PORT16, PORT17 I/O power supply	—	—	—	—	—	—	—
GEPREDVDD	—	1.8	PORT15, PORT16, PORT17 pre-driver power supply	—	—	—	—	—	—	—
DETCK	I	1.8	Debugger I/O	PD	Open	—	PD	—	—	—
DETDI	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
DETDO	O	1.8	Debugger I/O	Hi-Z	Open	—	—	—	Selectable*2	—
DETRMS	IO	1.8	Debugger I/O	PU	Open	—	PU	—	Selectable*2	—
DETRSTN	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
DESRSTN	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
RETEST0	I	3.3	LSI test I/O	PD	Pull down	●	PD	—	—	—
RETEST1	I	3.3	LSI test I/O	PD	Pull down	●	PD	—	—	—
LPATEST	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (13/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
LPCAA2	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA3	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA4	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA5	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB2	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB3	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB4	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB5	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCKEA0	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEA1	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEB0	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEB1	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCLKAC	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKAT	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKBC	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKBT	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSA0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSA1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSB0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSB1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIA0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIA1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIB0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIB1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA2	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA3	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA4	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA5	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA6	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA7	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA8	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA9	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA10	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA11	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA12	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA13	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA14	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA15	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB2	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB3	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB4	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB5	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB6	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB7	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (14/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
LPDQB8	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB9	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB10	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB11	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB12	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB13	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB14	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB15	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAC0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAC1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAT0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAT1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBC0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBC1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBT0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBT1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPMRESETL	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPZN	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPVAA	—	1.8	LPDDR4 PLL 1.8-V power supply	—	—	—	—	—	—	—
LPVDD	—	0.8	LPDDR4 core 0.8-V power supply	—	—	—	—	—	—	—
LPVDDQ	—	1.1	LPDDR4 PHY 1.1-V power supply	—	—	—	—	—	—	—
LPDTEST	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LVRXD0P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD0P
LVRXD0M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD0M
LVRXD1P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD1P
LVRXD1M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD1M
LVRXD2P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD2P
LVRXD2M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD2M
LVRXD3P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD3P
LVRXD3M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD3M
LVRXCK0P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK0P
LVRXCK0M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK0M
LVRXD4P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD4P
LVRXD4M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD4M
LVRXD5P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD5P
LVRXD5M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD5M
LVRXD6P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD6P
LVRXD6M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD6M
LVRXD7P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD7P
LVRXD7M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD7M
LVRXCK1P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK1P
LVRXCK1M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK1M
LVRREXT	I	1.8	CIF PHY	Hi-Z	Pull down (10 kΩ)	—	—	—	—	—
LVRXAVCC	—	1.8	CIF PHY 1.8-V power supply	—	—	—	—	—	—	—
LVRXAVDD	—	0.8	CIF PHY 0.8-V power supply	—	—	—	—	—	—	—
LVRXAVSS	—	0	CIF PHY GND	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (15/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
DSMDPDATA0	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDNDATA0	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDPDATA1	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDNDATA1	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDPDATA2	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDNDATA2	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDPDATA3	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDNDATA3	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDPCLK	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMDNCLK	IO	1.8	Reserved	L	Open	—	—	—	—	—
DSMVREG0P4V	IO	1.8	Reserved	L	Open (external capacitor not required)	—	—	—	—	—
DSSDPDATA0	IO	1.8	Reserved	Hi-Z	Pull down	—	—	—	—	—
DSSDNDATA0	IO	1.8	Reserved	Hi-Z	Pull down	—	—	—	—	—
DSSDPCLK	IO	1.8	Reserved	Hi-Z	Pull down	—	—	—	—	—
DSSDNCLK	IO	1.8	Reserved	Hi-Z	Pull down	—	—	—	—	—
DSMSVDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—
DSMVDD12*8	—	1.2	1.2-V power supply	—	—	—	—	—	—	—
DSMSVDD0P8	—	0.8	0.8-V power supply	—	—	—	—	—	—	—
PCRXD0P	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD0M	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCTXD0P	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCTXD0M	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCREFCKP	I	1.8	PCIe PHY	CLOCK	Open	—	—	—	—	—
PCREFCKM	I	1.8	PCIe PHY	CLOCK	Open	—	—	—	—	—
PCREXT	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD1P	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD1M	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCTXD1P	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCTXD1M	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCVDD08	—	0.8	PCIe PHY 0.8-V power supply	—	—	—	—	—	—	—
PCVDD18	—	1.8	PCIe PHY 1.8-V power supply	—	—	—	—	—	—	—
PCRSTOUTB	O	3.3	PCIe I/O	H	Open	—	—	—	Selectable*2	—
USDP	IO	3.3	USB PHY	L	Open	—	—	—	—	—
USDM	IO	3.3	USB PHY	L	Open	—	—	—	—	—
USRESREF	I	0.25	USB RESREF	—	Open	—	—	—	—	—
USVD330	—	3.3	USB PHY HS section 3.3-V power supply	—	—	—	—	—	—	—
USVDDH	—	1.8	USB PHY HS section 1.8-V power supply	—	—	—	—	—	—	—
USDVDD*5	—	0.8	USB PHY HS section 0.8-V power supply	—	—	—	—	—	—	—
USVBUS	I	3.3*6	USB PHY	Hi-Z	Open	—	—	—	—	—
USRX0M	I	0.8	USB PHY	—	Open	—	—	—	—	—
USRX0P	I	0.8	USB PHY	—	Open	—	—	—	—	—
USTX0M	O	0.8	USB PHY	—	Open	—	—	—	—	—
USTX0P	O	0.8	USB PHY	—	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (16/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
USOTGID	I	1.8	USB PHY	—	Open	—	—	—	—	—
USVP	—	0.8	USB PHY SS section 0.8-V power supply	—	—	—	—	—	—	—
USVPH	—	3.3	USB PHY SS section 3.3-V power supply	—	—	—	—	—	—	—
USVPTX	—	0.8	USB PHY SS section transmitter power supply	—	—	—	—	—	—	—
USPWEN	O	3.3	USB I/O	L	Open	—	OFF	—	Selectable*2	—
USOVC	I	3.3	USB I/O	Hi-Z	Pull up	—	OFF	—	—	—
HDTXCP	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTXCM	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX0P	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX0M	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX1P	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX1M	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX2P	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX2M	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDREXT	IO	1.8	HDMI PHY	—	Open	—	—	—	—	—
HDAVDD18	—	1.8	HDMI PHY 1.8-V power supply	—	—	—	—	—	—	—
HDAVDD08	—	0.8	HDMI PHY 0.8-V power supply	—	—	—	—	—	—	—
HSCL*3	IO	1.8	PORT20 I/O	Hi-Z	Open	●	OFF	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-21)
HSDA*3	IO	1.8	PORT20 I/O	Hi-Z	Open	●	OFF	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-21)
HDHPD*3	IO	1.8	PORT20 I/O	Hi-Z	Open	●	OFF	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-21)
AD0AIN0	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN1	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN2	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN3	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN4	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN5	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN6	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN7	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN8	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN9	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN10	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN11	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AVCCA	—	1.8	ADCA 1.8-V power supply	—	—	—	—	—	—	—
AD0AVSSA	—	0	ADCA GND	—	—	—	—	—	—	—
AD1AIN0	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN1	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN2	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN3	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN4	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN5	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—

Table 2.2-1 List of External Pins (17/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
AD1AIN6	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN7	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AVCCA	—	1.8	ADCA 1.8-V power supply	—	—	—	—	—	—	—
AD1AVSSA	—	0	ADCA GND	—	—	—	—	—	—	—
MD0	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD1	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD2	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD3	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD4	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD5	I	1.8	MD7-0 I/O	PD	Always in use	—	PD	—	—	—
MD6	I	1.8	MD7-0 I/O	PD	Always in use	—	PD	—	—	—
MD7	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD8*7	IO	3.3/1.8	PORT21 I/O	Hi-Z	Always in use	—	—	—	Selectable*2	Multiplexed pin (see Table 2.2-2 and Table 2.2-22)
OTVDD18	—	1.8	1.8-V power supply for test	—	—	—	—	—	—	—
OTVDD08	—	0.8	0.8-V power supply for test	—	—	—	—	—	—	—
TS0AVDD18	—	1.8	TSU ch. 0 1.8-V power supply	—	—	—	—	—	—	—
TS0DVDD08A	—	0.8	TSU ch. 0 0.8-V power supply	—	—	—	—	—	—	—
TS1AVDD18	—	1.8	TSU ch. 1 1.8-V power supply	—	—	—	—	—	—	—
TS1DVDD08A	—	0.8	TSU ch. 1 0.8-V power supply	—	—	—	—	—	—	—
XIN	I	1.8	1.8-V OSC	CLOCK	Always in use	—	—	—	—	—
XOUT	O	1.8	1.8-V OSC	CLOCK	Always in use	—	—	—	—	—
RSTN	I	1.8	RSTN I/O	PU	Always in use	●	PU	—	—	—
PLVDD1	—	1.8	PLL ch. 1 1.8-V power supply	—	—	—	—	—	—	—
PLVSS1	—	0	PLL ch. 1 GND	—	—	—	—	—	—	—
PLVDD2	—	1.8	PLL ch. 2 1.8-V power supply	—	—	—	—	—	—	—
PLVSS2	—	0	PLL ch. 2 GND	—	—	—	—	—	—	—
PLVDD3	—	1.8	PLL ch. 3 1.8-V power supply	—	—	—	—	—	—	—
PLVSS3	—	0	PLL ch. 3 GND	—	—	—	—	—	—	—
PLVDD4	—	1.8	PLL ch. 4 1.8-V power supply	—	—	—	—	—	—	—
PLVSS4	—	0	PLL ch. 4 GND	—	—	—	—	—	—	—
PLVDD6	—	1.8	PLL ch. 6 1.8-V power supply	—	—	—	—	—	—	—
PLVSS6	—	0	PLL ch. 6 GND	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (18/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
PLVDD7	—	1.8	PLL ch. 7 1.8-V power supply	—	—	—	—	—	—	—
PLVSS7	—	0	PLL ch. 7 GND	—	—	—	—	—	—	—
PLDVDD081	—	0.8	PLL ch. 1 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD082	—	0.8	PLL ch. 2 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD083	—	0.8	PLL ch. 3 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD084	—	0.8	PLL ch. 4 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD086	—	0.8	PLL ch. 6 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD087	—	0.8	PLL ch. 7 0.8-V power supply	—	—	—	—	—	—	—
VDD08	—	0.8	VDD08 0.8-V power supply	—	—	—	—	—	—	—
VDD18	—	1.8	VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	—	—	—	—	—	—	—
VDD33	—	3.3	VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	—	—	—	—	—	—	—
PREDVDD33	—	1.8	VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	—	—	—	—	—	—	—
GND	—	0	GND	—	—	—	—	—	—	—

Note 1. For 3.3-V input tolerant

Note 2. For the drive strength, see **Section 3.4.2, Standard I/O Characteristics**.

Note 3. These multiplexed pins are for use with the ISP support package, so do not change the multiplexed functional blocks. For details, refer to *RZ/V2M Default Pin Function List*.

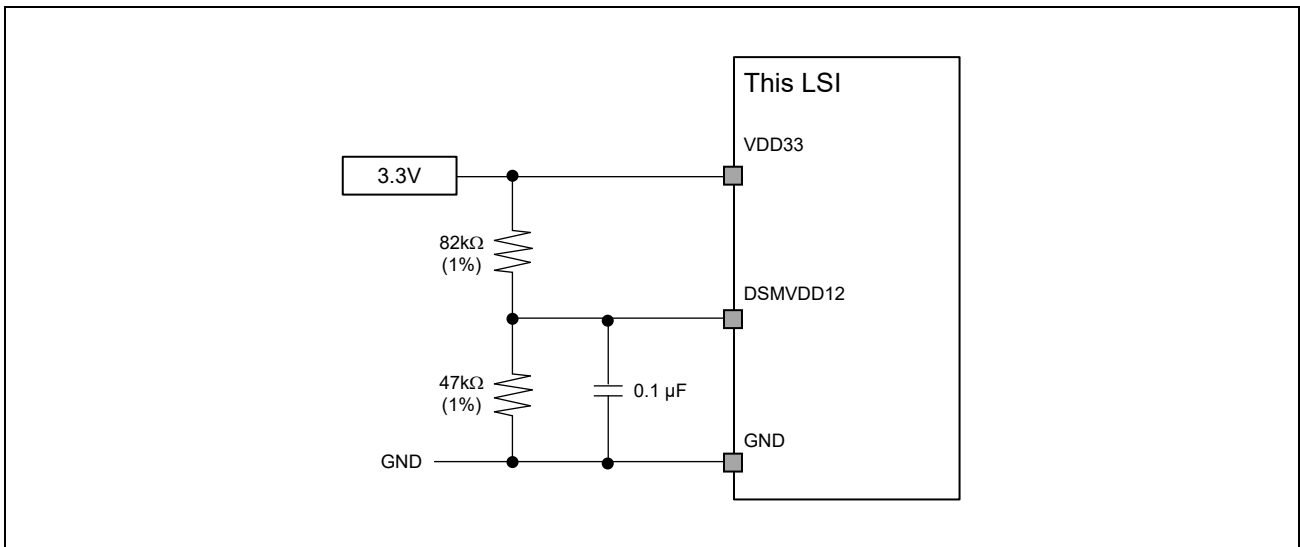
Note 4. If PWVBAT is not used, pulled up by PWVDD.

Note 5. Connect an external resistor (1.1kΩ). For details, refer to *the RZ/V2M High-Speed Interface PCB Design Guidelines*.

Note 6. See **Section 2.3, Pin Functions of Functional Blocks** for how to connect the USVBUS.

Note 7. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

Note 8. DSMVDD12 can be supplied with 1.2 V by the resistance voltage divider of VDD33. The schematic diagram is shown below.



<Usage Note>

In this LSI, supply power to all power pins.

It is necessary to supply power even if the power pin is an unused function and to connect the ground pin to the ground.

2.2.2 List of Multiplexed Functional Blocks

Table 2.2-2 List of Multiplexed Functional Blocks

I/O Group	Share Group 0	Share Group 1	Share Group 2	Share Group 3	Share Group 4	Share Group 5	Share Group 6	Share Group 7
PORT00	GPIO	—	eMMC	—	—	—	—	—
PORT01*1	GPIO	PWM	Ex. interrupt	CLK out	—	—	—	—
PORT02*1	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT03*1	GPIO	CSI0 CSI1 CSI2 CSI3	UART0 UART1 IIC2 IIC3 CSI3	CSI0 CSI1 CSI2	TRACE	—	—	—
PORT04*1	GPIO	CSI4 CSI5	CSI4 CSI5	—	TRACE	—	—	—
PORT05*1	GPIO	—	IIC0 IIC1	—	—	—	—	—
PORT06*1	GPIO	—	—	—	—	—	—	—
PORT07*1	GPIO	I2S	—	—	—	—	—	—
PORT08	GPIO	SDI0	—	—	—	—	—	—
PORT09	GPIO	SDI1	Ex. interrupt	—	—	—	—	—
PORT10*1	GPIO	STG0	Ex. interrupt	—	—	—	—	—
PORT11*1	GPIO	STG1	Ex. interrupt	—	—	—	—	—
PORT12*1	GPIO	Flash control	Ex. interrupt	—	—	—	—	—
PORT13*1	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT14*1	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT15	GPIO	ETHER	—	—	TRACE	—	—	—
PORT16	GPIO	ETHER	—	—	TRACE	—	—	—
PORT17	GPIO	ETHER	—	—	—	—	—	—
PORT20*1	GPIO	HDMI	—	—	—	—	—	—
PORT21	GPIO	—	—	—	—	—	—	—

Note 1. Some or all pins in the same I/O group are used by the ISP support package. Therefore, do not change the function of those pins. For details, refer to the following pages.

Table 2.2-3 I/O Group PORT00 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	eMMC	—	—	—	—	—
NADAT0	P00_00	—	MMDAT0	—	—	—	—	—
NADAT1	P00_01	—	MMDAT1	—	—	—	—	—
NADAT2	P00_02	—	MMDAT2	—	—	—	—	—
NADAT3	P00_03	—	MMDAT3	—	—	—	—	—
NADAT4	P00_04	—	MMDAT4	—	—	—	—	—
NADAT5	P00_05	—	MMDAT5	—	—	—	—	—
NADAT6	P00_06	—	MMDAT6	—	—	—	—	—
NADAT7	P00_07	—	MMDAT7	—	—	—	—	—
NACEN	P00_08	—	—	—	—	—	—	—
NAREN	P00_09	—	—	—	—	—	—	—
NAWEN	P00_10	—	MMCMD	—	—	—	—	—
NACLE	P00_11	—	MMCLK	—	—	—	—	—
NAALE	P00_12	—	—	—	—	—	—	—
NARBN	P00_13	—	—	—	—	—	—	—

Table 2.2-4 I/O Group PORT01 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	PWM	Ex. interrupt	CLK out	—	—	—	—
PM0*1	P01_00	PM0	INEXINT8	—	—	—	—	—
PM1*1	P01_01	PM1	INEXINT9	—	—	—	—	—
PM2*1	P01_02	PM2	INEXINT10	—	—	—	—	—
PM3*1	P01_03	PM3	INEXINT11	—	—	—	—	—
PM4*1	P01_04	PM4	INEXINT12	—	—	—	—	—
PM5*1	P01_05	PM5	INEXINT13	—	—	—	—	—
PM6*1	P01_06	PM6	INEXINT14	GMCLK0	—	—	—	—
PM7*1	P01_07	PM7	INEXINT15	GMCLK1	—	—	—	—
PM8	P01_08	PM8	INEXINT16	—	—	—	—	—
PM9	P01_09	PM9	INEXINT17	—	—	—	—	—
PM10	P01_10	PM10	INEXINT18	—	—	—	—	—
PM11	P01_11	PM11	INEXINT19	—	—	—	—	—
PM12	P01_12	PM12	INEXINT20	—	—	—	—	—
PM13	P01_13	PM13	INEXINT21	—	—	—	—	—
PM14	P01_14	PM14	INEXINT22	GMCLK0	—	—	—	—
PM15*1	P01_15	PM15	INEXINT23	GMCLK1	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-5 I/O Group PORT02 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
INEXINT0*1	P02_00	—	INEXINT0	—	—	—	—	—
INEXINT1*1	P02_01	—	INEXINT1	—	—	—	—	—
INEXINT2*1	P02_02	—	INEXINT2	—	—	—	—	—
INEXINT3*1	P02_03	—	INEXINT3	—	—	—	—	—
INEXINT4	P02_04	—	INEXINT4	—	—	—	—	—
INEXINT5	P02_05	—	INEXINT5	—	—	—	—	—
INEXINT6	P02_06	—	INEXINT6	—	—	—	—	—
INEXINT7	P02_07	—	INEXINT7	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-6 I/O Group PORT03 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	CSI0, CSI1, CSI2, CSI3	UART0, UART1, IIC2, IIC3, CSI3	CSI0, CSI1, CSI2	TRACE	—	—	—
CSTXD0	P03_00	CSTXD0	UATX0	CSRXD0	—	—	—	—
CSRXD0	P03_01	CSRXD0	UARX0	—	—	—	—	—
CSSCLK0	P03_02	CSSCLK0	UACTS0N	—	—	—	—	—
CSCS0	P03_03	CSCS0	UARTS0N	—	—	—	—	—
CSTXD1*1	P03_04	CSTXD1	UATX1	CSRXD1	—	—	—	—
CSRXD1*1	P03_05	CSRXD1	UARX1	—	—	—	—	—
CSSCLK1*1	P03_06	CSSCLK1	UACTS1N	—	TRDAT15	—	—	—
CSCS1*1	P03_07	CSCS1	UARTS1N	—	TRDAT14	—	—	—
CSTXD2	P03_08	CSTXD2	I2SDA2	CSRXD2	TRDAT13	—	—	—
CSRXD2	P03_09	CSRXD2	I2SCL2	—	TRDAT12	—	—	—
CSSCLK2*1	P03_10	CSSCLK2	I2SDA3	—	TRDAT11	—	—	—
CSCS2*1	P03_11	CSCS2	I2SCL3	—	TRDAT10	—	—	—
CSTXD3*1	P03_12	CSTXD3	CSRXD3	—	TRDAT9	—	—	—
CSRXD3*1	P03_13	CSRXD3	—	—	TRDAT8	—	—	—
CSSCLK3*1	P03_14	CSSCLK3	—	—	TRDAT7	—	—	—
CSCS3*1	P03_15	CSCS3	—	—	TRDAT6	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-7 I/O Group PORT04 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	CSI4, CSI5	CSI4, CSI5	—	TRACE	—	—	—
CSTXD4	P04_00	CSTXD4	CSRXD4	—	TRDAT5	—	—	—
CSRXD4	P04_01	CSRXD4	—	—	TRDAT4	—	—	—
CSSCLK4	P04_02	CSSCLK4	—	—	TRDAT3	—	—	—
CSCS4	P04_03	CSCS4	—	—	TRDAT2	—	—	—
CSTXD5*1	P04_04	CSTXD5	CSRXD5	—	TRDAT1	—	—	—
CSRXD5*1	P04_05	CSRXD5	—	—	TRDAT0	—	—	—
CSSCLK5*1	P04_06	CSSCLK5	—	—	TRCLK	—	—	—
CSCS5*1	P04_07	CSCS5	—	—	TRCTL	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-8 I/O Group PORT05 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	IIC0, IIC1	—	—	—	—	—
I2SDA0	P05_00	—	I2SDA0	—	—	—	—	—
I2SCL0	P05_01	—	I2SCL0	—	—	—	—	—
I2SDA1*1	P05_02	—	I2SDA1	—	—	—	—	—
I2SCL1*1	P05_03	—	I2SCL1	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-9 I/O Group PORT06 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
P0600*1	P06_00	—	—	—	—	—	—	—
P0601*1	P06_01	—	—	—	—	—	—	—
P0602*1	P06_02	—	—	—	—	—	—	—
P0603*1	P06_03	—	—	—	—	—	—	—
P0604*1	P06_04	—	—	—	—	—	—	—
P0605*1	P06_05	—	—	—	—	—	—	—
P0606*1	P06_06	—	—	—	—	—	—	—
P0607*1	P06_07	—	—	—	—	—	—	—
P0608	P06_08	—	—	—	—	—	—	—
P0609	P06_09	—	—	—	—	—	—	—
P0610	P06_10	—	—	—	—	—	—	—
P0611	P06_11	—	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-10 I/O Group PORT07 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	AUI	—	—	—	—	—	—
AULRCK*1	P07_00	AULRCK	—	—	—	—	—	—
AUBICK*1	P07_01	AUBICK	—	—	—	—	—	—
AUDI*1	P07_02	AUDI	—	—	—	—	—	—
AUDO*1	P07_03	AUDO	—	—	—	—	—	—
AUMCLK*1	P07_04	AUMCLK	—	—	—	—	—	—
AUPLLCLK*1	P07_05	AUPLLCLK	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-11 I/O Group PORT08 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	SDI0	—	—	—	—	—	—
SD0CMD	P08_00	SD0CMD	—	—	—	—	—	—
SD0CLK	P08_01	SD0CLK	—	—	—	—	—	—
SD0DAT0	P08_02	SD0DAT0	—	—	—	—	—	—
SD0DAT1	P08_03	SD0DAT1	—	—	—	—	—	—
SD0DAT2	P08_04	SD0DAT2	—	—	—	—	—	—
SD0DAT3	P08_05	SD0DAT3	—	—	—	—	—	—
SD0WP	P08_06	SD0WP	—	—	—	—	—	—
SD0CD	P08_07	SD0CD	—	—	—	—	—	—

Table 2.2-12 I/O Group PORT09 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	SDI1	Ex. interrupt	—	—	—	—	—
SD1FCMD	P09_00	SD1FCMD	—	—	—	—	—	—
SD1FCLK	P09_01	SD1FCLK	—	—	—	—	—	—
SD1FDAT0	P09_02	SD1FDAT0	—	—	—	—	—	—
SD1FDAT1	P09_03	SD1FDAT1	—	—	—	—	—	—
SD1FDAT2	P09_04	SD1FDAT2	—	—	—	—	—	—
SD1FDAT3	P09_05	SD1FDAT3	—	—	—	—	—	—
SD1FWP	P09_06	SD1FWP	INEXINT24	—	—	—	—	—
SD1FCD	P09_07	SD1FCD	INEXINT25	—	—	—	—	—

Table 2.2-13 I/O Group PORT10 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	STG0	Ex. interrupt	—	—	—	—	—
IM0VS*1	P10_00	IM0VS	—	—	—	—	—	—
IM0HS*1	P10_01	IM0HS	—	—	—	—	—	—
IM0CS*1	P10_02	IM0CS	—	—	—	—	—	—
IM0TXD*1	P10_03	IM0TXD	—	—	—	—	—	—
IM0RXD*1	P10_04	IM0RXD	—	—	—	—	—	—
IM0SCLK*1	P10_05	IM0SCLK	—	—	—	—	—	—
IM0SIG0*1	P10_06	IM0SIG0	INEXINT26	—	—	—	—	—
IM0SIG1*1	P10_07	IM0SIG1	INEXINT27	—	—	—	—	—
IM0SIG2*1	P10_08	IM0SIG2	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-14 I/O Group PORT11 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	STG1	Ex. interrupt	—	—	—	—	—
IM1VS*1	P11_00	IM1VS	—	—	—	—	—	—
IM1HS*1	P11_01	IM1HS	—	—	—	—	—	—
IM1CS*1	P11_02	IM1CS	—	—	—	—	—	—
IM1TXD*1	P11_03	IM1TXD	—	—	—	—	—	—
IM1RXD*1	P11_04	IM1RXD	—	—	—	—	—	—
IM1SCLK*1	P11_05	IM1SCLK	—	—	—	—	—	—
IM1SIG0*1	P11_06	IM1SIG0	INEXINT28	—	—	—	—	—
IM1SIG1*1	P11_07	IM1SIG1	INEXINT29	—	—	—	—	—
IM1SIG2*1	P11_08	IM1SIG2	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-15 I/O Group PORT12 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
IMSHUT0*1	P12_00	—	INEXINT30	—	—	—	—	—
IMSHUT1*1	P12_01	—	INEXINT31	—	—	—	—	—
IMSTSIG0*1	P12_02	IMSTSIG0	INEXINT32	—	—	—	—	—
IMSTSIG1*1	P12_03	IMSTSIG1	INEXINT33	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-16 I/O Group PORT13 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
MTDRV0*1	P13_00	—	—	—	—	—	—	—
MTDRV1*1	P13_01	—	—	—	—	—	—	—
MTDRV2*1	P13_02	—	—	—	—	—	—	—
MTDRV3*1	P13_03	—	—	—	—	—	—	—
MTDRV4*1	P13_04	—	—	—	—	—	—	—
MTDRV5*1	P13_05	—	—	—	—	—	—	—
MTDRV6*1	P13_06	—	—	—	—	—	—	—
MTDRV7*1	P13_07	—	—	—	—	—	—	—
MTDCPLS0*1	P13_08	—	—	—	—	—	—	—
MTDCPLS1*1	P13_09	—	INEXINT34	—	—	—	—	—
MTDCPLS2*1	P13_10	—	INEXINT35	—	—	—	—	—
MTDCPLS3*1	P13_11	—	INEXINT36	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-17 I/O Group PORT14 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
MTCS0*1	P14_00	—	—	—	—	—	—	—
MTTXD0*1	P14_01	—	—	—	—	—	—	—
MTRXD0*1	P14_02	—	INEXINT37	—	—	—	—	—
MTSCLK0*1	P14_03	—	—	—	—	—	—	—
MTCS1*1	P14_04	—	—	—	—	—	—	—
MTTXD1*1	P14_05	—	—	—	—	—	—	—
MTRXD1*1	P14_06	—	INEXINT38	—	—	—	—	—
MTSCLK1*1	P14_07	—	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-18 I/O Group PORT15 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	—	TRACE	—	—	—
GETXC	P15_00	GETXC	—	—	TRCLK	—	—	—
GETXEN	P15_01	GETXEN	—	—	TRCTL	—	—	—
GETXER	P15_02	GETXER	—	—	—	—	—	—
GETXD0	P15_03	GETXD0	—	—	—	—	—	—
GETXD1	P15_04	GETXD1	—	—	—	—	—	—
GETXD2	P15_05	GETXD2	—	—	—	—	—	—
GETXD3	P15_06	GETXD3	—	—	—	—	—	—
GETXD4	P15_07	GETXD4	—	—	—	—	—	—
GETXD5	P15_08	GETXD5	—	—	TRDAT0	—	—	—
GETXD6	P15_09	GETXD6	—	—	TRDAT1	—	—	—
GETXD7	P15_10	GETXD7	—	—	TRDAT2	—	—	—
GERXC	P15_11	GERXC	—	—	TRDAT3	—	—	—
GERXDV	P15_12	GERXDV	—	—	TRDAT4	—	—	—
GERXER	P15_13	GERXER	—	—	TRDAT5	—	—	—
GERXD0	P15_14	GERXD0	—	—	TRDAT6	—	—	—
GERXD1	P15_15	GERXD1	—	—	TRDAT7	—	—	—

Table 2.2-19 I/O Group PORT16 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	—	TRACE	—	—	—
GERXD2	P16_00	GERXD2	—	—	TRDAT8	—	—	—
GERXD3	P16_01	GERXD3	—	—	TRDAT9	—	—	—
GERXD4	P16_02	GERXD4	—	—	TRDAT10	—	—	—
GERXD5	P16_03	GERXD5	—	—	TRDAT11	—	—	—
GERXD6	P16_04	GERXD6	—	—	TRDAT12	—	—	—
GERXD7	P16_05	GERXD7	—	—	TRDAT13	—	—	—
GECRS	P16_06	GECRS	—	—	TRDAT14	—	—	—
GECOL	P16_07	GECOL	—	—	TRDAT15	—	—	—
GEMDC	P16_08	GEMDC	—	—	—	—	—	—
GEMDIO	P16_09	GEMDIO	—	—	—	—	—	—
GEGTXCLK	P16_10	GEGTXCLK	—	—	—	—	—	—
GELINK	P16_11	GELINK	—	—	—	—	—	—
GEINT	P16_12	GEINT	—	—	—	—	—	—
GECLK	P16_13	GECLK	—	—	—	—	—	—

Table 2.2-20 I/O Group PORT17 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
GEPPS	P17_00	—	—	—	—	—	—	—

Table 2.2-21 I/O Group PORT20 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	HDMI	—	—	—	—	—	—
HDSCL*1	P20_00	HDSCL	—	—	—	—	—	—
HSDA*1	P20_01	HSDA	—	—	—	—	—	—
HDHPD*1	P20_02	HDHPD	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-22 I/O Group PORT21 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
MD8*1	P21_00	—	—	—	—	—	—	—

Note 1. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

2.3 Pin Functions of Functional Blocks

Table 2.3-1 List of Pin Functions (1/7)

Classification	Pin Name	I/O	Function
Real time clock (RTC)	RTXIN	I	To connect a 32.768-kHz crystal resonator
	RTXOUT	O	To connect a 32.768-kHz crystal resonator
	RTRSTN	I	RTC reset input (active low)
	RTISO	I	RTC isolation input pin
Power control (PWC)	PWRSTN	I	PWC reset input (active low)
	PWTEST	I	LSI test pin, fixed to the low level
	PWVBAT	I	Battery voltage detection
	PWKY2N to PWKY0N	I	Reserved, pulled up by a 1.8-V power supply
	PWKY4N, PWKY3N	I	Reserved, pulled up by a 1.8-V power supply
	PWDETRSTN	I	Reserved, pulled up by a 1.8-V power supply
	PWEN5 to PWEN0	O	Power enable 5 to 0 (active high)
	PWSYSRSTN	O	System reset output. Connected to the RSTN pin to use the power control function of PWC.
	PWOUT1, PWOUT0	O	Reserved, leave these pins open-circuit.
	PWPWM	O	Reserved, leave this pin open-circuit.
	PWSD0SEL	O	PWC SDI0 interface power supply selection
	PWSD1SEL	O	PWC SDI1 interface power supply selection
	PWCTEST0	O	LSI test pin: leave this pin open-circuit.
	PWCTEST1	I	LSI test pin: fixed to the high level.(pulled up by the PWVDD)
	PWMEMSWIENA	O	Enable signal output pin for controlling the LPVDD power supply on/off
	PWISO	O	RTC separation output pin. Open drain output. Connected to the RTISO pin and pulled up (with 10kΩ to 100kΩ) to a 1.5-V power supply.*1
eMMC interface (eMMC)	MMDAT7 to MMDAT0	I/O	eMMC data [7:0]
	MMCMD	I/O	eMMC command
	MMCLK	O	eMMC clock
Pulse-width modulation timer (PWM)	PM15 to PM0	O	PWM output
External interrupt	INEXINT38 to INEXINT0	I	External interrupt

Table 2.3-1 List of Pin Functions (2/7)

Classification	Pin Name	I/O	Function
CSI ch. 0 (CSI0)	CSTXD0	O	CSI0 serial data output
	CSRXD0	I	CSI0 serial data input
	CSSCLK0	I/O	CSI0 serial clock
	CSCS0	I	CSI0 serial chip select
CSI ch. 1 (CSI1)	CSTXD1	O	CSI1 serial data output
	CSRXD1	I	CSI1 serial data input
	CSSCLK1	I/O	CSI1 serial clock
	CSCS1	I	CSI1 serial chip select
CSI ch. 2 (CSI2)	CSTXD2	O	CSI2 serial data output
	CSRXD2	I	CSI2 serial data input
	CSSCLK2	I/O	CSI2 serial clock
	CSCS2	I	CSI2 serial chip select
CSI ch. 3 (CSI3)	CSTXD3	O	CSI3 serial data output
	CSRXD3	I	CSI3 serial data input
	CSSCLK3	I/O	CSI3 serial clock
	CSCS3	I	CSI3 serial chip select
CSI ch. 4 (CSI4)	CSTXD4	O	CSI4 serial data output
	CSRXD4	I	CSI4 serial data input
	CSSCLK4	I/O	CSI4 serial clock
	CSCS4	I	CSI4 serial chip select
CSI ch. 5 (CSI5)	CSTXD5	O	CSI5 serial data output
	CSRXD5	I	CSI5 serial data input
	CSSCLK5	I/O	CSI5 serial clock
	CSCS5	I	CSI5 serial chip select
IIC ch. 0 (IIC0)	I2SDA0	I/O	IIC0 serial data
	I2SCL0	I/O	IIC0 serial clock
IIC ch. 1 (IIC1)	I2SDA1	I/O	IIC1 serial data
	I2SCL1	I/O	IIC1 serial clock
IIC ch. 2 (IIC2)	I2SDA2	I/O	IIC2 serial data
	I2SCL2	I/O	IIC2 serial clock
IIC ch. 3 (IIC3)	I2SDA3	I/O	IIC3 serial data
	I2SCL3	I/O	IIC3 serial clock
UART ch. 0 (UART0)	UATX0	O	UART0 transmission data
	UARX0	I	UART0 reception data
	UACTS0N	I	UART0 transmission enable signal (active low)
	UARTS0N	O	UART0 reception enable signal (active low)
UART ch. 1 (UART1)	UATX1	O	UART1 transmission data
	UARX1	I	UART1 reception data
	UACTS1N	I	UART1 transmission enable signal (active low)
	UARTS1N	O	UART1 reception enable signal (active low)

Table 2.3-1 List of Pin Functions (3/7)

Classification	Pin Name	I/O	Function
Audio interface (AUI)	AULRCK	I	Audio channel clock
	AUBICK	I	Audio serial clock
	AUDI	I	Audio serial data input
	AUDO	O	Audio serial data output
	AUMCLK	O	Audio master clock output
	AUPLLCLK	I	Audio master clock input
SD host interface ch. 0 (SDI0)	SD0CMD	I/O	SDI0 command/response signal
	SD0CLK	O	SDI0 clock
	SD0DAT3 to SD0DAT0	I/O	SDI0 data line bits [3:0]
	SD0WP	I	SDI0 write protect signal
	SD0CD	I	SDI0 card detection signal
SD host interface ch. 1 (SDI1)	SD1FCMD	I/O	SDI1 command/response signal
	SD1FCLK	O	SDI1 clock
	SD1FDAT3 to SD1FDAT0	I/O	SDI1 data line bits [3:0]
	SD1FWP	I	SDI1 write protect signal
	SD1FCD	I	SDI1 card detection signal
Image sensor timing generator ch. 0 (STG0)	IM0VS	I/O	Image sensor 0 vertical synchronization signal
	IM0HS	I/O	Image sensor 0 horizontal synchronization signal
	IM0CLK	O	Image sensor 0 clock supply port
	IM0CS	I/O	Image sensor 0 dedicated serial chip select output (or dedicated IIC clock)
	IM0TXD	O	Image sensor 0 dedicated serial transmission data output
	IM0RXD	I/O	Image sensor 0 dedicated serial reception data input (or dedicated IIC data)
	IM0SCLK	O	Image sensor 0 dedicated serial clock output
	IM0SIG2 to IM0SIG0	O	Image sensor 0 control pulse output
Image sensor timing generator ch. 1 (STG1)	IM1VS	I/O	Image sensor 1 vertical synchronization signal
	IM1HS	I/O	Image sensor 1 horizontal synchronization signal
	IM1CLK	O	Image sensor 1 clock supply port
	IM1CS	I/O	Image sensor 1 dedicated serial chip select output (or dedicated IIC clock)
	IM1TXD	O	Image sensor 1 dedicated serial transmission data output
	IM1RXD	I/O	Image sensor 1 dedicated serial reception data input (or dedicated IIC data)
	IM1SCLK	O	Image sensor 1 dedicated serial clock output
	IM1SIG2 to IM1SIG0	O	Image sensor 1 control pulse output
Flash control	IMSTSIG0	O	External flash control pin 0
	IMSTSIG1	O	External flash control pin 1

Table 2.3-1 List of Pin Functions (4/7)

Classification	Pin Name	I/O	Function
Gigabit Ethernet MAC interface (ETHER)	GETXC	I	Transmission clock for Ethernet 100-Mbps mode
	GETXEN	O	Transmission enable signal (active high)
	GETXER	O	Transmission error signal (active high)
	GETXD7 to GETXD0	O	Transmission data [7:0]
	GERXC	I	Ethernet reception clock
	GERXDV	I	Reception data valid signal (active high)
	GERXER	I	Reception error signal (active high)
	GERXD7 to GERXD0	I	Receive data [7:0]
	GECRS	I	Carrier detection signal (active high)
	GECOL	I	Transmission collision signal (active high)
	GEMDC	O	PHY management clock
	GEMDIO	I/O	PHY management I/O data
	GEGTXCLK	O	GMI transmission clock
	GELINK	I	PHY LINK signal
	GEINT	I	PHY interrupt signal
GECLK*2	I	Clock input	
Debugger interface	DETC	I	JTAG TCK
	DETDI	I	JTAG TDI
	DETD0	O	JTAG TDO
	DETM	I/O	JTAG TMS
	DETRSTN	I	JTAG TRST (active low)
	DESRSTN	I	System reset from debugger (active low)
For LSI test	RETEST0	I	LSI test enable, fixed to the low level
	RETEST1	I	LSI test enable, fixed to the low level

Table 2.3-1 List of Pin Functions (5/7)

Classification	Pin Name	I/O	Function
LPDDR4 interface	LPATEST	O	LSI test pin, leave this pin open-circuit.
	LPCAA5 to LPCAA0	O	DRAM address and command bits: Ch-A command/address input
	LPCAB5 to LPCAB0	O	DRAM address and command bits: Ch-B command/address input
	LPCKEA1, LPCKEA0	O	DRAM address and command bits: Ch-A clock enable
	LPCKEB1, LPCKEB0	O	DRAM address and command bits: Ch-B clock enable
	LPCLKAC	O	DRAM address and command bits: Ch-A clock (negative)
	LPCLKAT	O	DRAM address and command bits: Ch-A clock (positive)
	LPCLKBC	O	DRAM address and command bits: Ch-B clock (negative)
	LPCLKBT	O	DRAM address and command bits: Ch-B clock (positive)
	LPCSA1, LPCSA0	O	DRAM address and command bits: Ch-A chip select
	LPCSB1, LPCSB0	O	DRAM address and command bits: Ch-B chip select
	LPDMDBIA1, LPDMDBIA0	I/O	DRAM data bits and strobes: Ch-A data mask inversion
	LPDMDBIB1, LPDMDBIB0	I/O	DRAM data bits and strobes: Ch-B data mask inversion
	LPDQA15 to LPDQA0	I/O	DRAM data bits and strobes: Ch-A data input/output
	LPDQB15 to LPDQB0	I/O	DRAM data bits and strobes: Ch-B data input/output
	LPDQSAC1, LPDQSAC0	I/O	DRAM data bits and strobes: Ch-A data strobe (negative)
	LPDQSAT1, LPDQSAT0	I/O	DRAM data bits and strobes: Ch-A data strobe (positive)
	LPDQSBC1, LPDQSBC0	I/O	DRAM data bits and strobes: Ch-B data strobe (negative)
	LPDQSBT1, LPDQSBT0	I/O	DRAM data bits and strobes: Ch-B data strobe (positive)
	LPMRESETL	O	DRAM reset. Note that this requires no external resistor.
LPZN	O	External reference resistor connection pin for use in calibration. * To connect a pull-down resistor. Resistance: 240Ω±1%	
	LPDTEST	O	LSI test pin, leave this pin open-circuit.
MIPI CSI-2	LVRXREXT	I	External reference resistor connection pin * Resistance: 10kΩ ±1%
MIPI CSI-2 interface	MPRXD7P to MPRXD0P	I	MIPI CSI-2 differential data 7 to 0 (positive)
	MPRXD7M to MPRXD0M	I	MIPI CSI-2 differential data 7 to 0 (negative)
	MPRXCK1P, MPRXCK0P	I	MIPI CSI-2 differential clocks 1, 0 (positive)
	MPRXCK1M, MPRXCK0M	I	MIPI CSI-2 differential clocks 1, 0 (negative)
Reserved pins	DSMDPDATA3 to DSMDPDATA0	I/O	Reserved pins, leave these pins open-circuit
	DSMDNDATA3 to DSMDNDATA0	I/O	Reserved pins, leave these pins open-circuit
	DSMDPCLK	I/O	Reserved pin, leave this pin open-circuit
	DSMDNCLK	I/O	Reserved pin, leave this pin open-circuit
	DSMVREG0P4V	I/O	External capacitor connection pin * Connect the pin to GND via the capacitance. Recommended capacitance: 2.2 nF
	DSSDPCLK	I/O	LSI test pin, fixed to the low level
	DSSDNCLK	I/O	LSI test pin, fixed to the low level
	DSSDPDATA0	I/O	LSI test pin, fixed to the low level
	DSSDNDATA0	I/O	LSI test pin, fixed to the low level

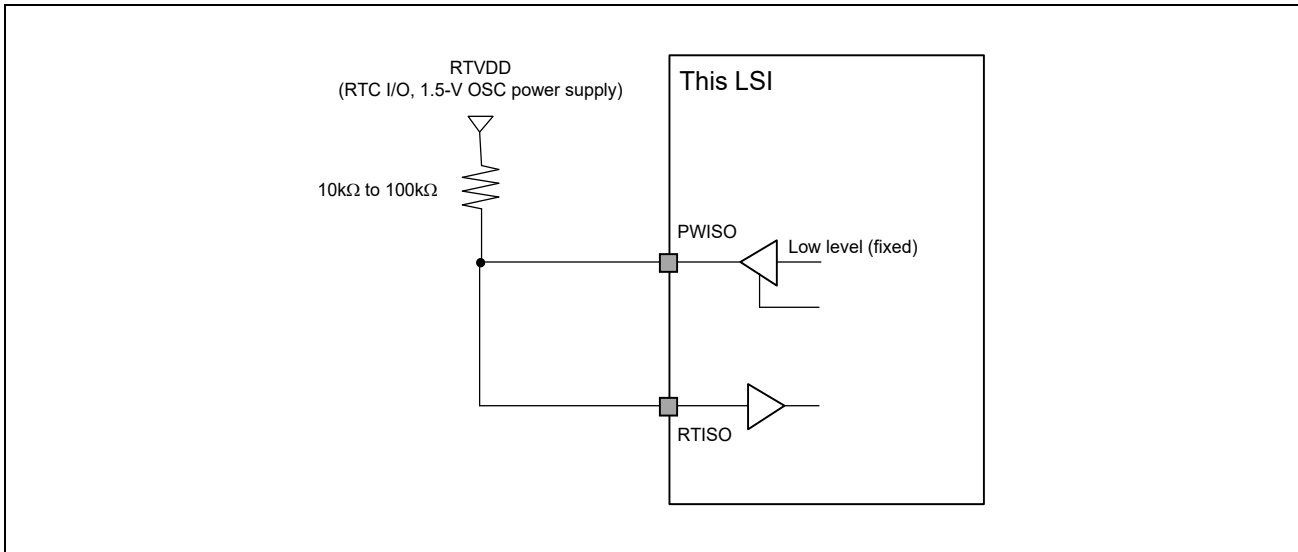
Table 2.3-1 List of Pin Functions (6/7)

Classification	Pin Name	I/O	Function
PCI Express interface	PCRXD1P, PCRXD0P	I	Rx serial data inputs 1, 0 (positive)
	PCRXD1M, PCRXD0M	I	Rx serial data inputs 1, 0 (negative)
	PCTXD1P, PCTXD0P	O	Tx serial data outputs 1, 0 (positive)
	PCTXD1M, PCTXD0M	O	Tx serial data outputs 1, 0 (negative)
	PCREFCKP	I	Differential reference clock (positive)
	PCREFCKM	I	Differential reference clock (negative)
	PCREXT	I	Reference resistor connection pin for band-gap reference (BGR) and bias generator * To connect a pull-down resistor. Resistance: 8.2kΩ ±1%
	PCRSTOUTB	O	Reset output (for other-party PCIe devices) (active low)
USB interface	USDP	I/O	USB2.0 USB D+ signal (positive)
	USDM	I/O	USB2.0 USB D- signal (negative)
	USRESREF	I	Reference resistor connection pin * To connect a pull-down resistor. Resistance: 200Ω ±1%
	USVBUS	I	USB VBUS signal detection pin* ³ * Resistance partial pressure outside the chip
	USRX0M	I	USB3.1 super-speed differential reception pair (negative)
	USRX0P	I	USB3.1 super-speed differential reception pair (positive)
	USTX0M	O	USB3.1 super-speed differential transmission pair (negative)
	USTX0P	O	USB3.1 super-speed differential transmission pair (positive)
	USOTGID	I	ID detection (OTG ID input, 0: Host, 1: Peripheral) In the initial state, an internal pull-up resistor is enabled.* ⁴
	USPWEN	O	VBUS control signal (active high)* ⁵
	USOVC	I	Overcurrent detection (active low)* ⁵
	HDMI Tx interface (HDMI)	HDTXCP	O
HDTXCM		O	TXPHY clock output (negative)* ⁵
HDTX0P		O	Data channel 0 TXPHY output (positive)* ⁵
HDTX0M		O	Data channel 0 TXPHY output (negative)* ⁵
HDTX1P		O	Data channel 1 TXPHY output (positive)* ⁵
HDTX1M		O	Data channel 1 TXPHY output (negative)* ⁵
HDTX2P		O	Data channel 2 TXPHY output (positive)* ⁵
HDTX2M		O	Data channel 2 TXPHY output (negative)* ⁵
HDREXT		I/O	External reference resistor connection pin * To connect a pull-down resistor. Resistance: 8.2kΩ ±1%
HDSCS		I/O	DDC IIC master SCL
HDSDA		I/O	DDC IIC master SDA
HDHPD	I/O	Hot plug detection (active high)	
ADC unit A (ADCA)	AD0AIN11 to AD0AIN0	I	Analog input signal
ADC unit B (ADCB)	AD1AIN7 to AD1AIN0	I	Analog input signal

Table 2.3-1 List of Pin Functions (7/7)

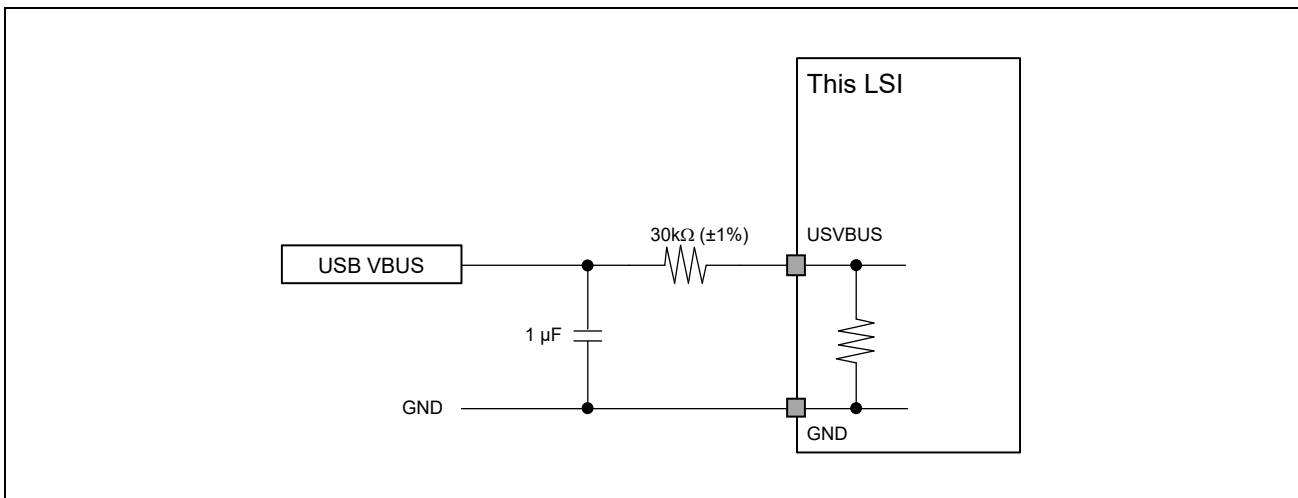
Classification	Pin Name	I/O	Function
Boot	MD2 to MD0	I	Boot device select [2:0]
	MD3	I	Boot device write interface select When not using security, fix the input level to low. When using security, prepare a circuit that is capable of switching the input level externally to low or high (pull up with VDD18).
	MD4, MD5	I	Boot mode select [1:0] (reserved) Fix the pin to the low level.
	MD6	I	Boot mode select [2]
	MD7	I	Boot mode select [3] (reserved) Fix the pin to the low level.
	MD8	I/O	Boot GPIO (LED control when booted)*6
	Clock/reset	XIN	I
XOUT		O	To connect a 48-MHz crystal resonator
RSTN		I	System reset (active low)
Clock output	GMCLK0	O	Clock output 0
	GMCLK1	O	Clock output 1
Trace interface (TRACE)	TRDAT15 to TRDAT0	O	Trace data [15:0]
	TRCLK	O	Trace clock
	TRCTL	O	Trace control
General-purpose input/output ports (GPIO)	P00_13 to P00_00	I/O	GPIO port 00 [13:0]
	P01_15 to P01_00	I/O	GPIO port 01 [15:0]
	P02_07 to P02_00	I/O	GPIO port 02 [7:0]
	P03_15 to P03_00	I/O	GPIO port 03 [15:0]
	P04_07 to P04_00	I/O	GPIO port 04 [7:0]
	P05_03 to P05_00	I/O	GPIO port 05 [3:0]
	P06_11 to P06_00	I/O	GPIO port 06 [11:0]
	P07_05 to P07_00	I/O	GPIO port 07[5:0]
	P08_07 to P08_00	I/O	GPIO port 08[7:0]
	P09_07 to P09_00	I/O	GPIO port 09[7:0]
	P10_08 to P10_00	I/O	GPIO port 10[8:0]
	P11_08 to P11_00	I/O	GPIO port 11[8:0]
	P12_03 to P12_00	I/O	GPIO port 12[3:0]
	P13_11 to P13_00	I/O	GPIO port 13[11:0]
	P14_07 to P14_00	I/O	GPIO port 14[7:0]
	P15_15 to P15_00	I/O	GPIO port 15[15:0]
	P16_13 to P16_00	I/O	GPIO port 16[13:0]
	P17_00	I/O	GPIO port 17[0]
	P20_02 to P20_00	I/O	GPIO port 20[2:0]
	P21_00	I/O	GPIO port 21[0]*6

- Note 1. The PWISO and RTISO pins are connected to this LSI, and these nodes should be pulled up with a 10kΩ to 100kΩ resistor. The schematic diagram is shown below.

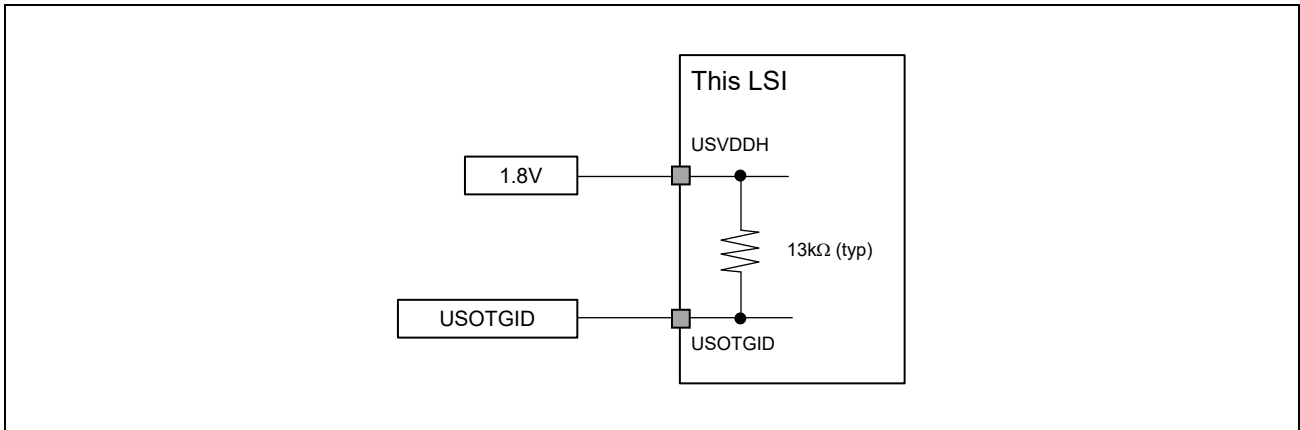


- Note 2. GECLK is the input clock for GEGTXCLK.

- Note 3. Since this LSI has a resistor mounted between the USVBUS pin and GND, connect the pin to the USVBUS pin via a 30-kΩ ($\pm 1\%$) resistor. The schematic diagram is shown below. In addition, design so that the voltage is applied to the USVBUS pin after supplying USDVDD, USVP and USVPTX.



Note 4. USOTGID has the internal pull-up resistor.



Note 5. When the power of this LSI is turned off, applying the 3.3-V pull-up voltage in the opposite direction to these pins does not cause any problem.

Note 6. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

Section 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 3.1-1 Absolute Maximum Ratings (1/3)

Item	Symbol	Min.	Max.	Unit
VDD08 core power supply	V _{DD08}	-0.4	1.2	V
RTC core power supply	RTV _{DD08}	-0.4	1.2	V
RTC I/O, 1.5-V OSC power supply	RTV _{DD}	-0.4	2.5	V
PWC core power supply	PWV _{DD08}	-0.4	1.2	V
PWC I/O power supply	PWV _{DD}	-0.4	2.5	V
PORT01(A), PORT03 pre-driver power supply	PAPREDV _{DD}	-0.4	2.5	V
PORT01(A), PORT03 I/O power supply	PAMODV _{DD}	-0.4	3.8	V
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	PBPREDV _{DD}	-0.4	2.5	V
PORT01(B), PORT04, PORT07, PORT21 I/O power supply	PBMODV _{DD}	-0.4	3.8	V
PORT06 pre-driver power supply	PCPREDV _{DD}	-0.4	2.5	V
PORT06 I/O power supply	PCMODV _{DD}	-0.4	3.8	V
PORT10 pre-driver power supply	IM0PREDV _{DD}	-0.4	2.5	V
PORT10 I/O power supply	IM0MODV _{DD}	-0.4	3.8	V
PORT11 pre-driver power supply	IM1PREDV _{DD}	-0.4	2.5	V
PORT11 I/O power supply	IM1MODV _{DD}	-0.4	3.8	V
PORT00 pre-driver power supply	NAPREDV _{DD}	-0.4	2.5	V
PORT00 I/O power supply	NAMODV _{DD}	-0.4	3.8	V
PORT08 pre-driver power supply	SD0PREDV _{DD}	-0.4	2.5	V
PORT08 I/O power supply	SD0MODV _{DD}	-0.4	3.8	V
PORT09 pre-driver power supply	SD1FV _{DD}	-0.4	2.5	V
PORT09 I/O power supply	SD1FMODV _{DD}	-0.4	3.8	V
PORT15, PORT16, PORT17 pre-driver power supply	GEPREDV _{DD}	-0.4	2.5	V
PORT15, PORT16, PORT17 I/O power supply	GEMODV _{DD}	-0.4	3.8	V

Table 3.1-1 Absolute Maximum Ratings (2/3)

Item	Symbol	Min.	Max.	Unit
VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	V _{DD18}	-0.4	2.5	V
VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	PREDV _{DD33}	-0.4	2.5	V
VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	V _{DD33}	-0.4	3.8	V
PLL ch. 1, 2, 3, 4, 6, 7 0.8-V power supply	PLDV _{DD08n} (n = 1, 2, 3, 4, 6, 7)	-0.4	1.2	V
PLL ch. 1, 2, 3, 4, 6, 7 1.8-V power supply	PLV _{DDn} (n = 1, 2, 3, 4, 6, 7)	-0.4	2.5	V
0.8-V power supply for test	OTV _{DD08}	-0.4	1.2	V
1.8-V power supply for test	OTV _{DD18}	-0.4	2.5	V
TSU ch. 0 0.8-V power supply	TS0DV _{DD08A}	-0.4	1.2	V
TSU ch. 1 0.8-V power supply	TS1DV _{DD08A}	-0.4	1.2	V
TSU ch. 0 1.8-V power supply	TS0AV _{DD18}	-0.4	2.5	V
TSU ch. 1 1.8-V power supply	TS1AV _{DD18}	-0.4	2.5	V
ADC unit A 1.8-V power supply	AD0AV _{CCA}	-0.4	2.5	V
ADC unit B 1.8-V power supply	AD1AV _{CCA}	-0.4	2.5	V
CIF PHY 0.8-V power supply	LVRXAV _{DD}	-0.4	1.2	V
CIF PHY 1.8-V power supply	LVRXAV _{CC}	-0.4	2.5	V
LPDDR4 core 0.8-V power supply	LPV _{DD}	-0.4	1.2	V
LPDDR4 PLL 1.8-V power supply	LPV _{AA}	-0.4	2.5	V
LPDDR4 I/O 1.1-V power supply	LPV _{DDQ}	-0.4	1.5	V
HDMI PHY 1.8-V power supply	HDAV _{DD18}	-0.4	2.5	V
HDMI PHY 0.8-V power supply	HDAV _{DD08}	-0.4	1.2	V
1.8-V power supply	DSMSV _{DD18}	-0.4	2.5	V
1.2-V power supply	DSMV _{DD12}	-0.4	2.5	V
0.8-V power supply	DSMSV _{DD0P8}	-0.4	1.2	V
PCIe PHY 0.8-V power supply	PCV _{DD08}	-0.4	1.2	V
PCIe PHY 1.8-V power supply	PCV _{DD18}	-0.4	2.5	V
USB PHY HS section 3.3-V power supply	USV _{D330}	-0.4	3.8	V
USB PHY HS section 1.8-V power supply	USV _{DDH}	-0.4	2.5	V
USB PHY HS section 0.8-V power supply	USDV _{DD}	-0.4	1.2	V

Table 3.1-1 Absolute Maximum Ratings (3/3)

Item	Symbol	Min.	Max.	Unit
USB PHY SS section 0.8-V power supply	USV _P	-0.4	1.2	V
USB PHY SS section 3.3-V power supply	USV _{PH}	-0.4	3.8	V
USB3.0 transmitter power supply	USV _{PTX}	-0.4	1.2	V
Input voltage (1.1-V I/O)	V _{in11}	-0.4	LPV _{DDQ} +0.3* ³	V
Input voltage (1.5-V I/O)	V _{in15}	-0.4	RTV _{DD} + 0.3* ⁴	V
Input voltage (1.8-V I/O)* ¹	V _{in18}	-0.4	V ₁₈ + 0.3* ⁵	V
Input voltage (1.8-V I/O (3.3-V tolerant))* ²	V _{in18_tol}	-0.4	3.6	V
Input voltage (3.3-V I/O)	V _{in33}	-0.4	V ₃₃ + 0.3* ⁶	V
Analog input voltage (ADC unit A AIN)	V _{ain18_0}	0	AD0AV _{CCA}	V
Analog input voltage (ADC unit B AIN)	V _{ain18_1}	0	AD1AV _{CCA}	V
Junction temperature	T _j	-40	125	°C
Storage temperature	T _{stg}	-40	150	°C

Note 1. 1.8-V I/O (except for PORT02 I/O and PORT05 I/O)

Note 2. 1.8-V I/O (PORT02 I/O and PORT05 I/O)

Note 3. The voltage to be applied must be within the absolute maximum rating (1.5 V).

Note 4. The voltage to be applied must be within the absolute maximum rating (2.5 V).

Note 5. The voltage to be applied must be within the absolute maximum rating (2.5 V). V18 indicates the power supply voltage for 1.8-V I/O pins.

Note 6. The voltage to be applied must be within the absolute maximum rating (3.8 V). V33 indicates the power supply voltage for 3.3-V I/O pins.

3.2 Recommended Operating Range

Table 3.2-1 Recommended Operating Range (1/2)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
VDD08 core power supply	V_{DD08}	0.76	0.8	0.84	V	
RTC core power supply	RTV_{DD08}	0.76	0.8	0.84	V	
RTC I/O, 1.5-V OSC power supply	RTV_{DD}	1.425	1.5	1.575	V	
PWC core power supply	PWV_{DD08}	0.76	0.8	0.84	V	
PWC I/O power supply	PWV_{DD}	1.71	1.8	1.89	V	
PORT01(A), PORT03 pre-driver power supply	$PAPREDV_{DD}$	1.71	1.8	1.89	V	
PORT01(A), PORT03 I/O power supply	$PAMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	$PBPREDV_{DD}$	1.71	1.8	1.89	V	
PORT01(B), PORT04, PORT07, PORT21 I/O power supply	$PBMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT06 pre-driver power supply	$PCPREDV_{DD}$	1.71	1.8	1.89	V	
PORT06 I/O power supply	$PCMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT10 pre-driver power supply	$IM0PREDV_{DD}$	1.71	1.8	1.89	V	
PORT10 I/O power supply	$IM0MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT11 pre-driver power supply	$IM1PREDV_{DD}$	1.71	1.8	1.89	V	
PORT11 I/O power supply	$IM1MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT00 pre-driver power supply	$NAPREDV_{DD}$	1.71	1.8	1.89	V	
PORT00 I/O power supply	$NAMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT08 pre-driver power supply	$SD0PREDV_{DD}$	1.71	1.8	1.89	V	
PORT08 I/O power supply	$SD0MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT09 pre-driver power supply	$SD1FV_{DD}$	1.71	1.8	1.89	V	
PORT09 I/O power supply	$SD1FMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT15, PORT16, PORT17 pre-driver power supply	$GEPREDV_{DD}$	1.71	1.8	1.89	V	
PORT15, PORT16, PORT17 I/O power supply	$GEMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	V_{DD18}	1.71	1.8	1.89	V	
VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$PREDV_{DD33}$	1.71	1.8	1.89	V	

Table 3.2-1 Recommended Operating Range (2/2)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	V _{DD33}	3.135	3.3	3.465	V	
PLL ch. 1, 2, 3, 4, 6, 7 0.8-V power supply	PLDV _{DD08n} , (n = 1, 2, 3, 4, 6, 7)	0.76	0.8	0.84	V	
PLL ch. 1, 2, 3, 4, 6, 7 1.8-V power supply	PLVDDn (n = 1, 2, 3, 4, 6, 7)	1.71	1.8	1.89	V	
0.8-V power supply for test	OTV _{DD08}	0.76	0.8	0.84	V	
1.8-V power supply for test	OTV _{DD18}	1.71	1.8	1.89	V	
TSU ch. 0 0.8-V power supply	TS0DV _{DD08A}	0.76	0.8	0.84	V	
TSU ch. 1 0.8-V power supply	TS1DV _{DD08A}	0.76	0.8	0.84	V	
TSU ch. 0 1.8-V power supply	TS0AV _{DD18}	1.71	1.8	1.89	V	
TSU ch. 1 1.8-V power supply	TS1AV _{DD18}	1.71	1.8	1.89	V	
ADC unit A 1.8-V power supply	AD0AV _{CCA}	1.71	1.8	1.89	V	
ADC unit B 1.8-V power supply	AD1AV _{CCA}	1.71	1.8	1.89	V	
CIF PHY 0.8-V power supply	LVRXAV _{DD}	0.76	0.8	0.84	V	
CIF PHY 1.8-V power supply	LVRXAV _{CC}	1.71	1.8	1.89	V	
LPDDR4 core 0.8-V power supply	LPV _{DD}	0.76	0.8	0.84	V	
LPDDR4 PLL 1.8-V power supply	LPV _{AA}	1.71	1.8	1.89	V	
LPDDR4 PHY 1.1-V power supply	LPV _{DDQ}	1.06	1.1	1.17	V	
HDMI PHY 0.8-V power supply	HDAV _{DD08}	0.76	0.8	0.84	V	
HDMI PHY 1.8-V power supply	HDAV _{DD18}	1.71	1.8	1.89	V	
0.8-V power supply	DSMSV _{DD0P8}	0.76	0.8	0.84	V	
1.8-V power supply	DSMSV _{DD18}	1.71	1.8	1.89	V	
1.2-V power supply	DSMV _{DD12}	1.14	1.2	1.26	V	
PCIe PHY 0.8-V power supply	PCV _{DD08}	0.76	0.8	0.84	V	
PCIe PHY 1.8-V power supply	PCV _{DD18}	1.71	1.8	1.89	V	
USB PHY SS section 0.8-V power supply	USV _P	0.76	0.8	0.84	V	
USB PHY HS section 1.8-V power supply	USV _{DDH}	1.71	1.8	1.89	V	
USB PHY HS section 3.3-V power supply	USV _{D330}	3.135	3.3	3.465	V	
USB PHY HS section 0.8-V power supply	USDV _{DD}	0.76	0.8	0.84	V	
USB PHY SS section transmitter power supply	USV _{PTX}	0.76	0.8	0.84	V	
USB PHY SS section 3.3-V power supply	USV _{PH}	3.135	3.3	3.465	V	
Junction temperature	T _J	—	—	103	°C	

3.3 Power-On/Off Procedures

3.3.1 Power-On Sequence (RTC/PWC)

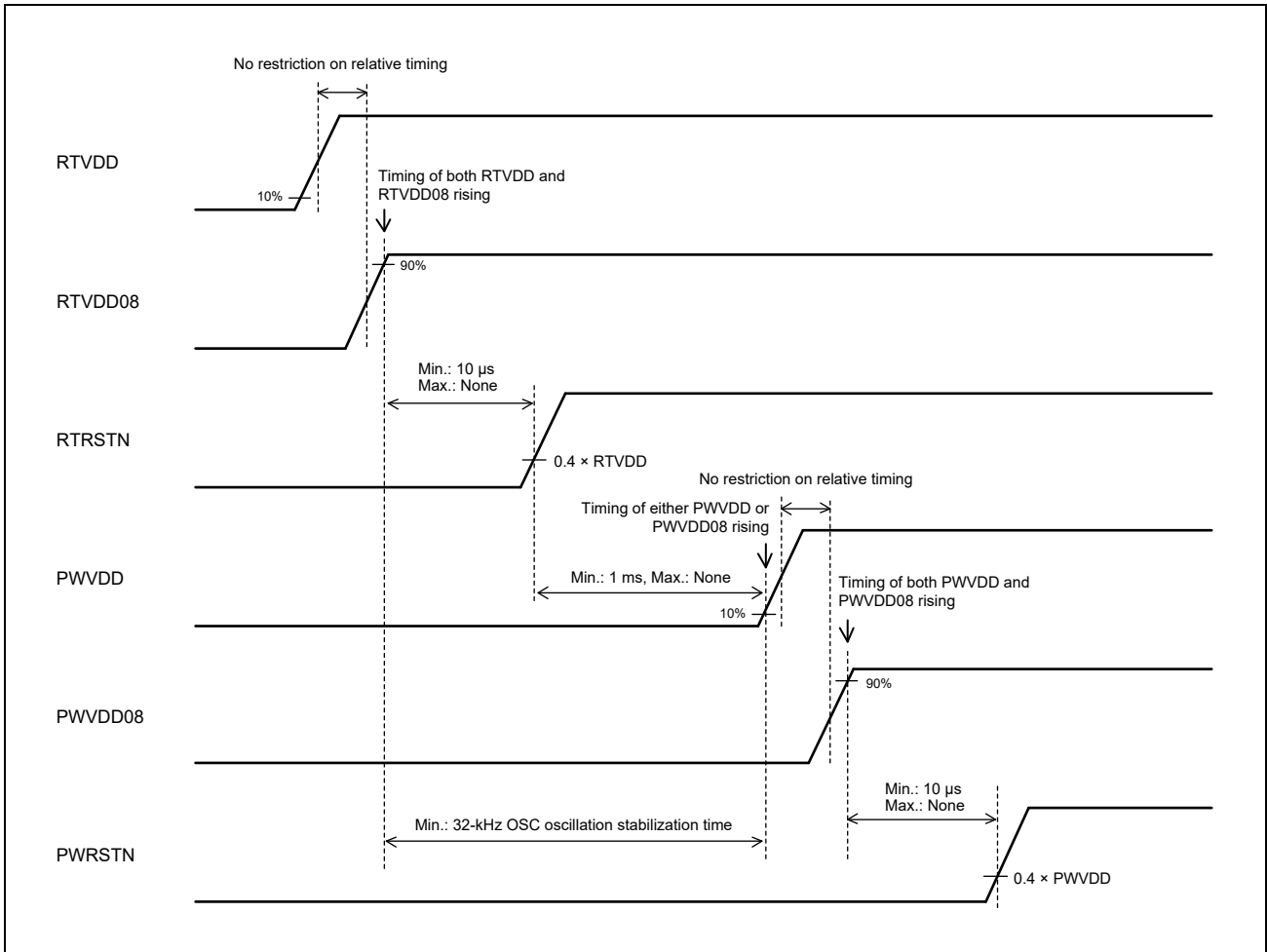


Figure 3.3-1 Power-On Sequence (RTC/PWC)

3.3.2 Power-On/Off Sequence (other than for RTC/PWC)

3.3.2.1 Power-On Sequence (other than for RTC/PWC)

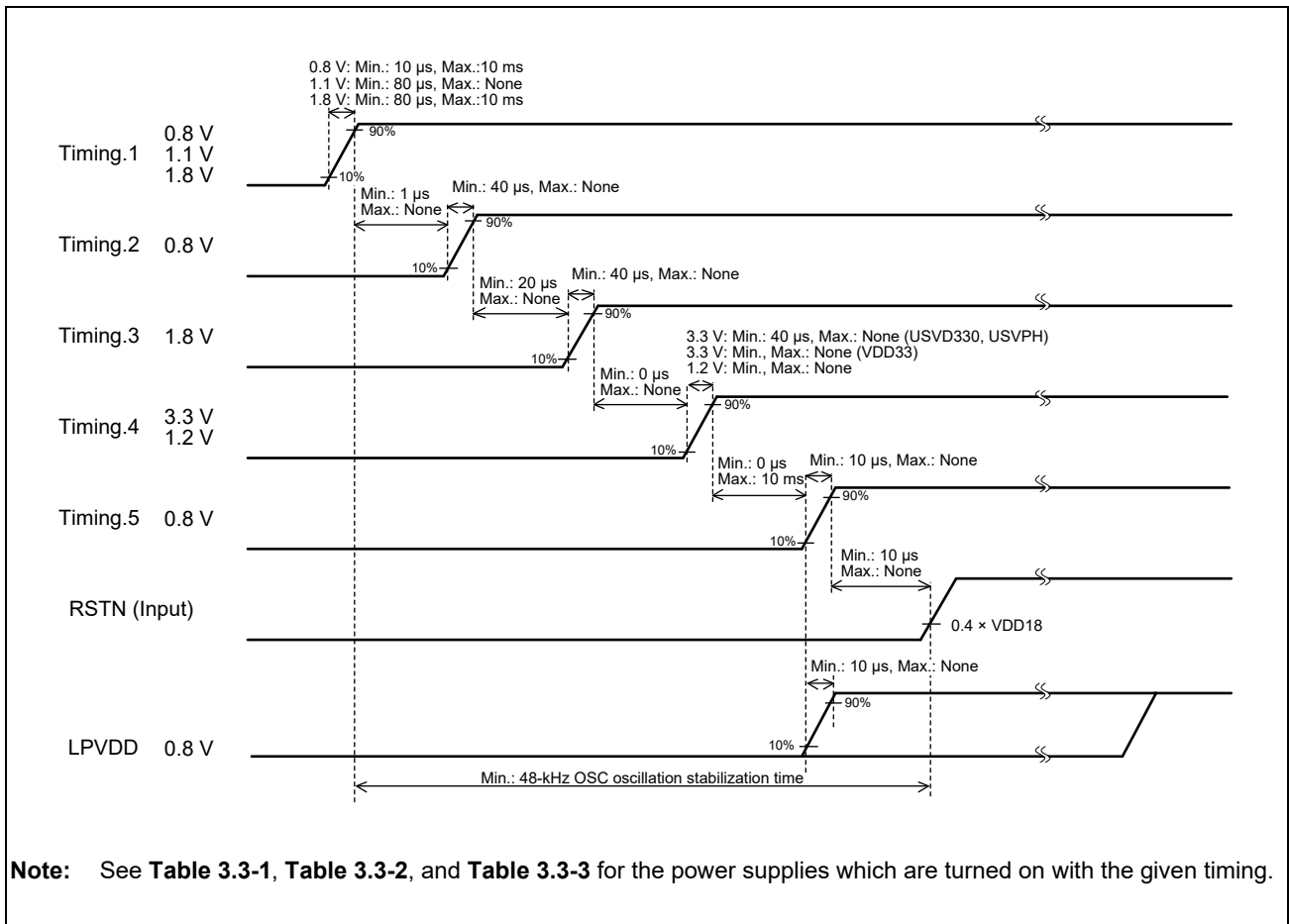


Figure 3.3-2 Power-On Sequence (other than for RTC/PWC)

Table 3.3-1, Table 3.3-2, and Table 3.3-3 show the correspondence between the power supplies and the power-on (off) timings.

Table 3.3-1 Various Power Supplies and Power On/Off Timings

Power Voltage	Power Supply Name	Timing
0.8 V	VDD08	Timing.1
1.1 V	LPVDDQ	
1.8 V	VDD18, LPVAA	
0.8 V	DSMSVDD0P8, PCVDD08, HDAVDD08, OTVDD08, LVRXAVDD	Timing.2
1.8 V	DSMSVDD18, PCVDD18, HDAVDD18, OTVDD18, LVRXAVCC, USVDDH	Timing.3
3.3 V	VDD33, USVD330, USVPH	Timing.4
1.2 V	DSMVDD12	Timing.5
0.8 V	USDVDD, USVP, USVPTX, LPVDD*1	

Note 1. When not controlled by the System FW, the power is on (off) at Timing.5.
 When controlled by the System FW, connect the 0.8-V power supply to the LPVDD pin of this LSI via the power switch. In addition, connect the PWMEMSWIENA pin of this LSI to an enable pin of this power switch.

Table 3.3-2 Various Power Supplies and Power On/Off Timings (PLL, TSU, ADC, etc.)

Power Voltage	Power Supply Name	Timing
0.8 V	PLDVDD08n (n = 1, 2, 3, 4, 6, 7), TSnDVDD08A (n = 0, 1)	Timing.1 or Timing.2
1.8 V	PLVDDn (n = 1, 2, 3, 4, 6, 7), TSnAVDD18 (n = 0, 1), ADnAVCCA (n = 0, 1), PREDVDD33	Timing.1 or Timing.3

Table 3.3-3 Various Power Supplies and Power On/Off Timings (1.8-V/3.3-V Switching I/O)

I/O Voltage	Power Supply Name	Case	Timing
Used as the 1.8-V I/O	Pre-driver power supply*1	1	Timing.1
	I/O power supply*2		
	Pre-driver power supply*1	2	Timing.1
	I/O power supply*2		Timing.3
	Pre-driver power supply*1	3	Timing.3
	I/O power supply*2		
Used as the 3.3-V IO	Pre-driver power supply*1	4	Timing.1
	I/O power supply*2		Timing.4
	Pre-driver power supply*1	5	Timing.3
	I/O power supply*2		Timing.4

Note 1. NAPREDVDD, PAPREDVDD, PBPREDVDD, PCPREDVDD, SD0PREDVDD, SD1FVDD, IM0PREDVDD, IM1PREDVDD, GEPREDVDD

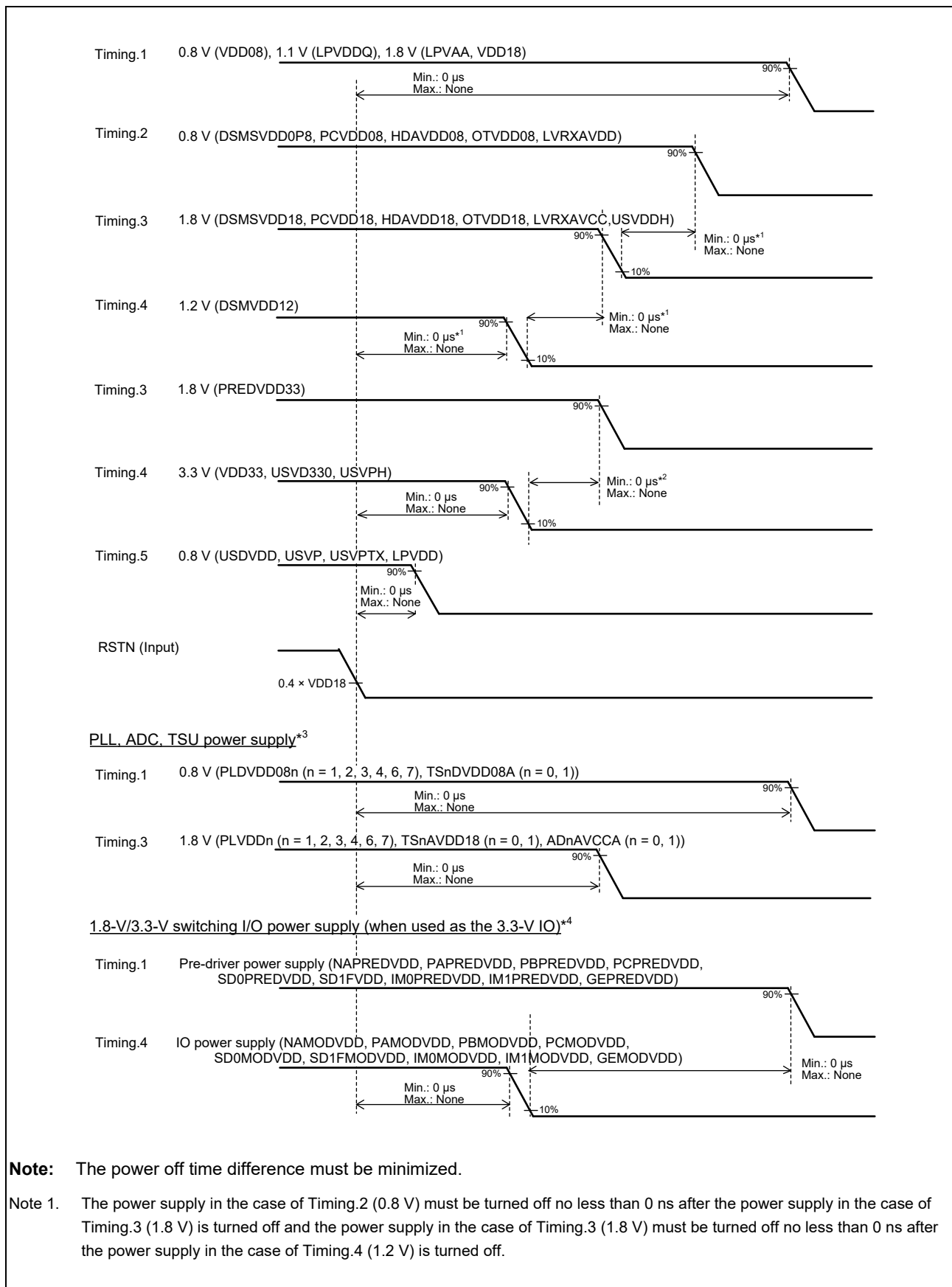
Note 2. NAMODVDD, PAMODVDD, PBMODVDD, PCMODVDD, SD0MODVDD, SD1FMODVDD, IM0MODVDD, IM1MODVDD, GEMODVDD

The following restrictions apply to the order of turning on the pre-driver power supply and the I/O power supply for the power supply of the 1.8-V/3.3-V switching I/O.

- When used as the 1.8-V I/O, “the pre-driver power supply and the I/O power supply are turned on at the same time” or “the pre-driver power supply is turned on first and then the I/O power supply”.
- When used as the 3.3-V I/O, “the pre-driver power supply is turned on first and then the I/O power supply”.

When used as the 1.8-V I/O, the pre-driver power supply and the I/O power supply must be turned on or off in case 1, 2, or 3. When used as the 3.3-V I/O, they must be turned on or off in case 4 or 5.

3.3.2.2 Power-Off Sequence (other than for RTC/PWC)



(Continuation of the previous page)

- Note 2. The power supply in the case of Timing.3 (1.8 V) must be turned off no less than 0 ns after the power supply in the case of Timing.4 (3.3 V) is turned off.
- Note 3. The 0.8-V power supply and the 1.8-V power supply are indicated in the case of Timing.1 and Timing.3, respectively. No restrictions apply to the order of turning off the 0.8-V power supply and the 1.8-V power supply.
- Note 4. This is used as the 3.3-V I/O, and the pre-driver power supply and the I/O power supply are indicated in the case of Timing.1 and Timing.4, respectively.
The pre-driver power supply must be turned off no less than 0 ns after the I/O power supply is turned off.
When used as the 1.8-V I/O, no restrictions apply to the order of turning on the pre-driver power supply and the I/O power supply.

Figure 3.3-3 Power-Off Sequence (other than for RTC/PWC)

3.3.3 Timing Limitations when Power is being Turned On

Control the input signals according to the timing limitations for power being turned on.

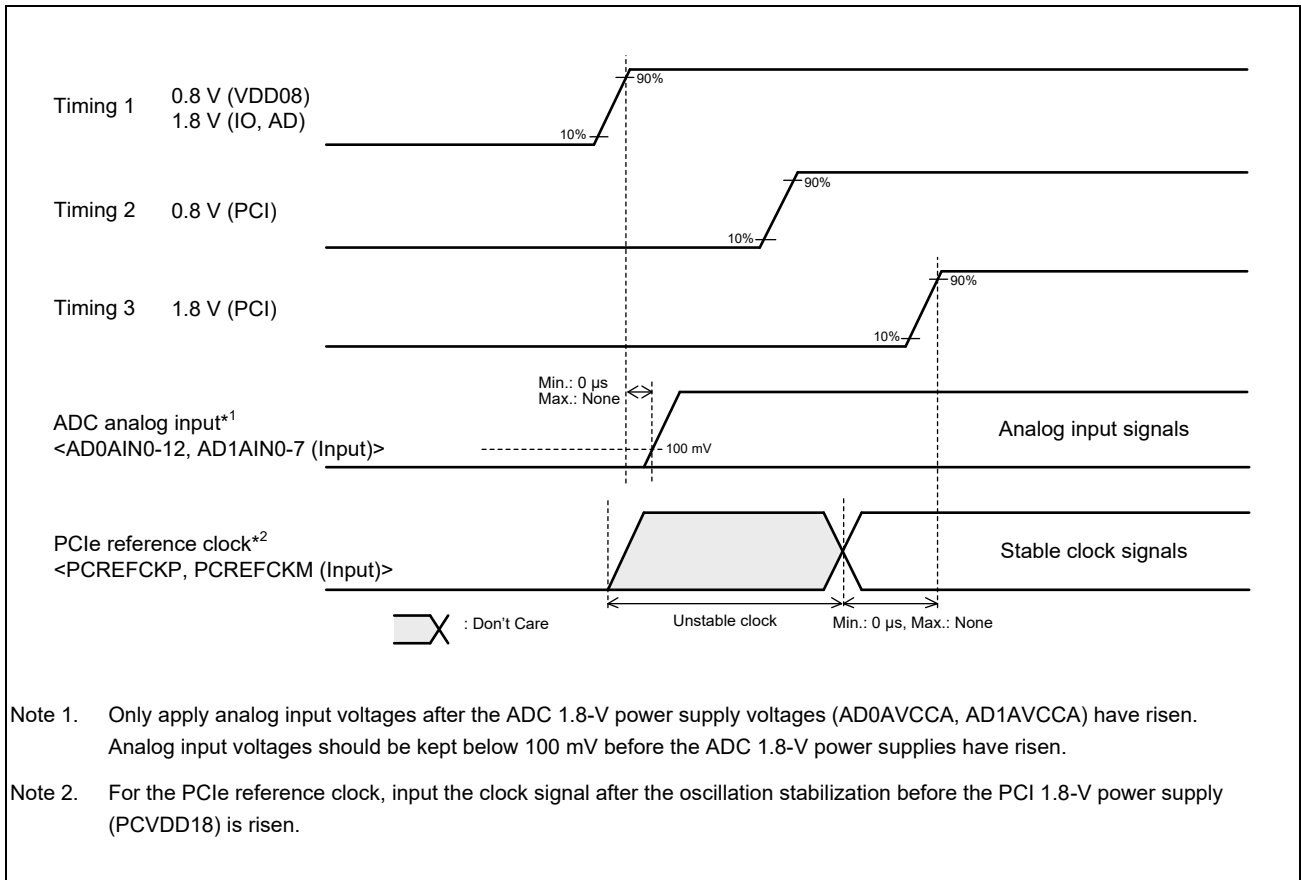


Figure 3.3-4 ADC Analog Inputs at Power-On/PCI Reference Clock Input Timing

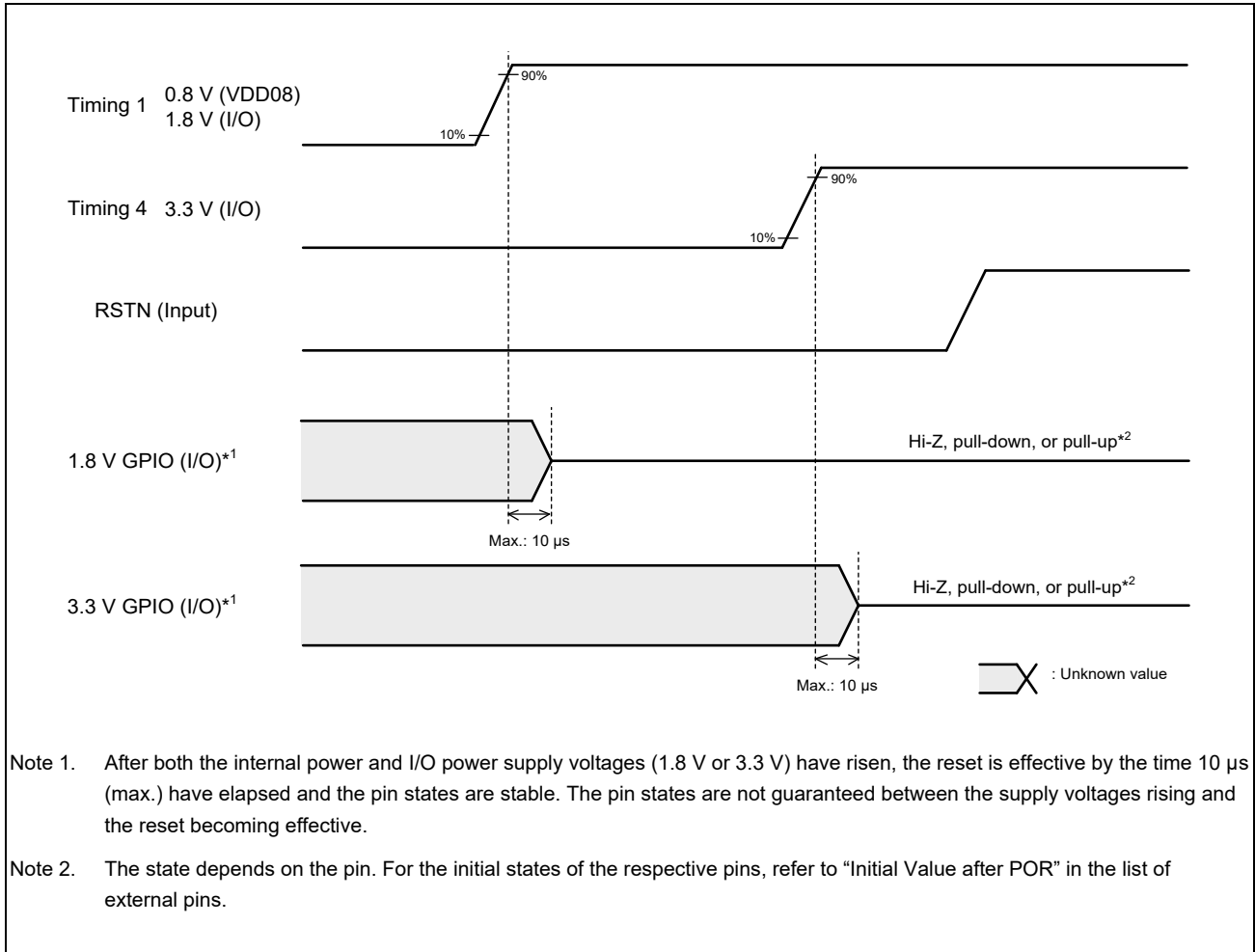


Figure 3.3-5 GPIO Timing at Power-On

3.4 DC Characteristics

3.4.1 Supply Current

3.4.1.1 Maximum Supply Current

Conditions for the supply current: Power supply voltage = Max. value, $T_j = -40$ to 125°C

Table 3.4-1 Max. Supply Currents during Operation (1/2)

Item	Symbol	Max.	Unit	Note
VDD08 core power supply current	I_{DD08}	4770	mA	The current must be within the maximum supply current.
RTC core power supply current	$I_{DDRTVDD08}$	700	μA	RTV_{DD08}^{*1}
RTC I/O, 1.5-V OSC power supply current	$I_{DDRTVDD}$	300^{*3}	μA	RTV_{DD}^{*2}
PWC core power supply current	$I_{DDPWVDD08}$	1	mA	PWV_{DD08}
PWC I/O power supply current	$I_{DDPWVDD}$	3	mA	PWV_{DD}
PORT01(A), PORT03 pre-driver power supply current	$I_{DDPAPRE}$	2	mA	$PAPREDV_{DD}$: PWM0 - 7, CSI0, TRDAT6 - 15
PORT01(A), PORT03 I/O power supply current	$I_{DDPAMOD}$	23	mA	$PAMODV_{DD}$: PWM0 - 7, CSI0, TRDAT6 - 15
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply current	$I_{DDBPBRE}$	1	mA	$PBPREDV_{DD}$: PWM8 - 15, TRACE0 - 6, AUI
PORT01(B), PORT04, PORT07, PORT21 I/O power supply current	$I_{DDPBMOD}$	16	mA	$PBMODV_{DD}$: PWM8 - 15, TRACE0 - 6, AUI
PORT06 pre-driver power supply current	$I_{DDPCPRE}$	1	mA	$PCPREDV_{DD}$: P0600 - 11
PORT06 I/O power supply current	$I_{DDPCMOD}$	11	mA	$PCMODV_{DD}$: P0600 - 11
PORT10 pre-driver power supply current	$I_{DDIM0PRE}$	1	mA	$IM0PREDV_{DD}$
PORT10 I/O power supply current	$I_{DDIM0MOD}$	4	mA	$IM0MODV_{DD}$
PORT11 pre-driver power supply current	$I_{DDIM1PRE}$	1	mA	$IM1PREDV_{DD}$
PORT11 I/O power supply current	$I_{DDIM1MOD}$	4	mA	$IM1MODV_{DD}$
PORT00 pre-driver power supply current	$I_{DDNAPRE}$	2	mA	$NAPREDV_{DD}$: eMMC HS200
PORT00 I/O power supply current	$I_{DDNAMOD}$	10	mA	$NAMODV_{DD}$: eMMC HS200
PORT08 pre-driver power supply current	$I_{DDSD0PRE}$	1	mA	$SD0PREDV_{DD}$: SDIO SDR104
PORT08 I/O power supply current	$I_{DDSD0MOD}$	16	mA	$SD0MODV_{DD}$: SDIO SDR104
PORT09 pre-driver power supply current	I_{DDSD1F}	1	mA	$SD1FV_{DD}$: SDIO SDR104
PORT09 I/O power supply current	$I_{DDSD1MOD}$	16	mA	$SD1FMODV_{DD}$: SDIO SDR104
PORT15, PORT16, PORT17 pre-driver power supply current	$I_{DDGEPRE}$	1	mA	$GEPREDV_{DD}$
PORT15, PORT16, PORT17 I/O power supply current	$I_{DDGEMOD}$	17	mA	$GEMODV_{DD}$
VDD18 group I/O power supply current (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	I_{DD18}	3	mA	V_{DD18} : IIC0 - 1, DEBUG

Table 3.4-1 Max. Supply Currents during Operation (2/2)

Item	Symbol	Max.	Unit	Note
VDD33 group pre-driver power supply current (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$I_{DDPRE33}$	2	mA	PREDV _{DD33}
VDD33 group I/O power supply current (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	I_{DD33}	20	mA	V _{DD33}
PLL ch. 1, 2, 3, 4, 6, 7 0.8-V power supply current	I_{DDPL08}	16	mA	Total of PLDV _{DD081} , PLDV _{DD082} , PLDV _{DD083} , PLDV _{DD084} , PLDV _{DD086} , PLDV _{DD087}
PLL ch. 1, 2, 3, 4, 6, 7 1.8-V power supply current	I_{DDPL18}	14	mA	Total of PLV _{DD1} , PLV _{DD2} , PLV _{DD3} , PLV _{DD4} , PLV _{DD6} , PLV _{DD7}
OTP 0.8-V power supply current	I_{DDOT08}	9	mA	OTV _{DD08}
OTP 1.8-V power supply current	I_{DDOT18}	60	mA	OTV _{DD18}
TSU ch. 0 0.8-V power supply current	I_{DDTS08}	1	mA	TS0DV _{DD08A}
TSU ch. 1 0.8-V power supply current	I_{DDTS08}	1	mA	TS1DV _{DD08A}
TSU ch. 0 1.8-V power supply current	I_{DDTS18}	4	mA	TS0AV _{DD18}
TSU ch. 1 1.8-V power supply current	I_{DDTS18}	4	mA	TS1AV _{DD18}
ADC unit A 1.8-V power supply current	I_{DDAD0}	1	mA	AD0AV _{CCA}
ADC unit B 1.8-V power supply current	I_{DDAD1}	1	mA	AD1AV _{CCA}
CIF PHY 0.8-V power supply current	$I_{DDLVD08}$	127	mA	LVRXAV _{DD}
CIF PHY 1.8-V power supply current	$I_{DDLVD18}$	81	mA	LVRXAV _{CC}
LPDDR4 core 0.8-V power supply current	$I_{DDLVP08}$	800	mA	LPV _{DD} : 3200 Mbps
LPDDR4 PLL 1.8-V power supply current	$I_{DDLVP18}$	6	mA	LPV _{AA} : 3200 Mbps
LPDDR4 PHY 1.1-V power supply current	$I_{DDLVP11}$	314	mA	LPV _{DDQ} : 3200 Mbps
HDMI PHY 0.8-V power supply current	I_{DDHD08}	24	mA	HDAV _{DD08}
HDMI PHY 1.8-V power supply current	I_{DDHD18}	10	mA	HDAV _{DD18}
0.8-V power supply current	$I_{DDDSM08}$	2	mA	DSMSV _{DD08P8}
1.8-V power supply current	$I_{DDDSM18}$	30	mA	DSMSV _{DD18}
1.2-V power supply current	$I_{DDDSM12}$	8	mA	DSMV _{DD12}
PCIe PHY 0.8-V power supply current	I_{DDPC08}	188	mA	PCV _{DD08}
PCIe PHY 1.8-V power supply current	I_{DDPC18}	132	mA	PCV _{DD18}
USB PHY 0.8-V power supply current	I_{DDUS08}	88	mA	Total of USDV _{DD} , USV _P , USV _{PTX}
USB PHY 1.8-V power supply current	I_{DDUS18}	21	mA	USV _{DDH}
USB PHY 3.3-V power supply current	I_{DDUS33}	57	mA	Total of USV _{D330} , USV _{PH}

Note 1. Reference value for the RTC core power supply current (at normal temperature at 0.8 V): 35 μ A

Note 2. Reference value for the RTC I/O, 1.5-V OSC power supply current (at normal temperature at 1.5 V): 10 μ A

Note 3. In normal operation (when the power supplies other than for the RTC power domain are turned on), current flows to the PWISO pin via a pull-up resistor, so this amount of current must be taken into account when the current drawn is estimated.
[Example] When the pull-up resistance is 10k Ω , 1.5 V/10k Ω = 150 μ A

3.4.2 Standard I/O Characteristics

For the I/O groups, refer to the multiplexed pin group numbers in the list of external pins.

Table 3.4-2 DC Characteristics

$V_{DD} = 1.35\text{ V to }1.65\text{ V}$ (1.5-V I/O group), $V_{DD} = 1.65\text{ V to }1.95\text{ V}$ (1.8-V I/O groups 1, 2, 3, and 4), $V_{DD} = 1.65\text{ V to }3.60\text{ V}$ (3.3/1.8-V switching I/O groups 1 and 2), $V_{DD} = 3.00\text{ V to }3.60\text{ V}$ (3.3-V I/O group)

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
External voltage tolerance	1.8-V I/O group 3*4	V_{TOL}	—	—	3.6	V	V_{DD} power-off & on
High-level input voltage	—	V_{IH}	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	—
Low-level input voltage	—	V_{IL}	-0.3	—	$0.3 \times V_{DD}$	V	—
Hysteresis voltage	1.5-V I/O group*1	ΔV	$0.1 \times V_{DD}$	—	—	V	—
	1.8-V I/O group 1*2	ΔV	$0.1 \times V_{DD}$	—	—	V	—
	1.8-V I/O group 2*3						
	1.8-V I/O group 3*4	ΔV	$0.08 \times V_{DD}$	—	—	V	—
	3.3/1.8-V switching I/O group 1*6	ΔV	$0.08 \times V_{DD}$	—	—	V	—
	3.3/1.8-V switching I/O group 2*7	ΔV	0.1	—	—	V	—
High-level input current (Non-tolerant input buffer)	3.3-V I/O group*8	ΔV	$0.08 \times V_{DD}$	—	—	V	—
	1.5V I/O group*1	I_{IH}	—	—	12	μA	$V_{in15} = V_{DD} \text{ max \& } V_{DD} \text{ power-on}$
	1.8-V I/O group 1*2 1.8-V I/O group 2*3 1.8-V I/O group 4*5	I_{IH}	—	—	12	μA	$V_{in18} = V_{DD} \text{ max \& } V_{DD} \text{ power-on}$
	3.3/1.8-V switching I/O group 1*6 3.3/1.8-V switching I/O group 2*7	I_{IH}	—	—	12	μA	$V_{in33} = V_{DD} \text{ max \& } V_{DD} \text{ power-on}$
High-level input current (Tolerant input buffer)	3.3-V I/O group*8	I_{IH}	—	—	12	μA	—
	1.8-V I/O group 3*4	I_{IH}	—	—	12	μA	$V_{in18_tol} = V_{DD} \text{ max \& } V_{DD} \text{ power-on}$
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	I_{IH}	—	—	200	μA	$V_{in18} = V_{DD} \text{ max}$
	3.3/1.8-V switching I/O group 1*6 3.3/1.8-V switching I/O group 2*7 3.3-V I/O group*8	I_{IH}	—	—	200	μA	$V_{in33} = V_{DD} \text{ max}$
Low-level input current (Non-tolerant input buffer)	1.5-V I/O group*1	I_{IL}	-12	—	—	μA	$V_{in15} = V_{SS}$
	1.8-V I/O group 1*2 1.8-V I/O group 2*3	I_{IL}	-12	—	—	μA	$V_{in18} = V_{SS}$
	1.8-V I/O group 4*5	I_{IL}	-12	—	—	μA	—
	3.3/1.8-V switching I/O group 1*6	I_{IL}	-12	—	—	μA	$V_{in33} = V_{SS}$
	3.3/1.8-V switching I/O group 2*7	I_{IL}	-12	—	—	μA	—
	3.3-V I/O group*8	I_{IL}	-12	—	—	μA	—
Low-level input current (Tolerant input buffer)	1.8-V I/O group 3*4	I_{IL}	-12	—	—	μA	$V_{in18_tol} = V_{SS}$
Low-level input current (Input buffer with pull-down resistor)	1.8-V I/O group 2*3	I_{IL}	-180	—	—	μA	$V_{in18} = V_{SS}$
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	I_{IL}	-200	—	—	μA	—
	3.3/1.8-V switching I/O group 1*6	I_{IL}	-200	—	—	μA	$V_{in33} = V_{SS}$
	3.3/1.8-V switching I/O group 2*7	I_{IL}	-190	—	—	μA	—
	3.3-V I/O group*8	I_{IL}	-200	—	—	μA	—

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	
High-level output voltage	1.5-V I/O group* ¹	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -1.8$ mA-
	1.8-V I/O group 1* ²	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -3.8$ mA
	1.8-V I/O group 2* ³	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -1.8/-3.8/-7.8/-11$ mA (drive strength X1/X2/X4/X6)
	1.8-V I/O group 3* ⁴ 1.8-V I/O group 4* ⁵	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -1.6/-3.2/-6.4/-9.6$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (1.8 V)* ⁶	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -1.6/-3.2/-6.4/-9.6$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (3.3 V)* ⁶	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -2/-4/-8/-12$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (1.8 V)* ⁷	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -5/-6/-7/-10$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (3.3 V)* ⁷	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -9/-11/-13/-18$ mA (drive strength X1/X2/X4/X6)
	3.3-V I/O group* ⁸	V_{OH}	$0.8 \times V_{DD}$	—	V_{DD}	V	$I_{OH} = -2/-4/-8/-12$ mA (drive strength X1/X2/X4/X6)
Low-level output voltage	1.5-V I/O group* ¹	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1.8$ mA
	1.8-V I/O group 1* ²	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 3.8$ mA
	1.8-V I/O group 2* ³	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1.8/3.8/7.8/11$ mA (drive strength X1/X2/X4/X6)
	1.8-V I/O group 3* ⁴ 1.8-V I/O group 4* ⁵	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1.6/3.2/6.4/9.6$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (1.8 V)* ⁶	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 1.6/3.2/6.4/9.6$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (3.3 V)* ⁶	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (1.8 V)* ⁷	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 5/6/7/10$ mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (3.3 V)* ⁷	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 9/11/13/18$ mA (drive strength X1/X2/X4/X6)
	3.3-V I/O group* ⁸	V_{OL}	0	—	$0.2 \times V_{DD}$	V	$I_{OL} = 2/4/8/12$ mA (drive strength X1/X2/X4/X6)
Pull-up resistance	1.8-V I/O group 2* ³	R_{PU}	11	—	47	k Ω	—
	1.8-V I/O group 3* ⁴ 1.8-V I/O group 4* ⁵	R_{PU}	11	—	49	k Ω	—
	3.3/1.8-V switching I/O group 1 (1.8 V)* ⁶	R_{PU}	11	—	49	k Ω	—
	3.3/1.8-V switching I/O group 1 (3.3 V)* ⁶	R_{PU}	15	—	83	k Ω	—
	3.3/1.8-V switching I/O group 2 (1.8 V)* ⁷	R_{PU}	12	—	92	k Ω	—
	3.3/1.8-V switching I/O group 2 (3.3 V)* ⁷	R_{PU}	18	—	72	k Ω	—
	3.3-V I/O group* ⁸	R_{PU}	15	—	83	k Ω	—

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Pull-down resistance	1.8-V I/O group 3*4 1.8V I/O group 4*5	R _{PD}	12	—	45	kΩ	—
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	R _{PD}	12	—	45	kΩ	—
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	R _{PD}	20	—	75	kΩ	—
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	R _{PD}	13	—	92	kΩ	—
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	R _{PD}	24	—	87	kΩ	—
	3.3-V I/O group*8	R _{PD}	20	—	75	kΩ	—
	Input capacitance	—	C _{in}	—	—	10	pF

Note 1. Target I/O group: 1.5-V OSC, RTC I/O

Note 2. Target I/O group: PWC I/O

Note 3. Target I/O group: PORT20 I/O, RSTN I/O, 1.8-V OSC

Note 4. Target I/O group: PORT02 I/O, PORT05 I/O

Note 5. Target I/O group: MD0-7 I/O, debugger I/O

Note 6. Target I/O group:
PORT01(A) I/O, PORT03 I/O, PORT01(B) I/O, PORT04 I/O, PORT07 I/O, PORT21 I/O, PORT06 I/O, PORT10 I/O,
PORT11 I/O

Note 7. Target I/O group:
PORT00 I/O, PORT08 I/O, PORT09 I/O, PORT15 I/O, PORT16 I/O, PORT17 I/O

Note 8. Target I/O group:
PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O

3.5 AC Characteristics

AC characteristics measurement conditions

- I/O signal reference levels:
 $V_{DD18}/2$, $V_{DD33}/2$, $NAMODV_{DD}/2$, $PAMODC_{DD}/2$, $PBMODV_{DD}/2$, $PCMODV_{DD}/2$, $SD0MODV_{DD}/2$,
 $SD1FMODV_{DD}/2$, $IM0MODV_{DD}/2$, $GEMODV_{DD}/2$, $IM1MODV_{DD}/2$, V_{IH} , V_{OH} (min.), V_{IL} , V_{OL} (max.)
(Refer to the corresponding timing charts.)
- Output load: $C_L = 20$ pF if not otherwise stated

3.5.1 IIC Bus Interface

Table 3.5-1 IIC Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
I2SCLn cycle time	t_{cyc}	2500	—	—	ns	
I2SCLn low level width	t_{LOW}	1300	—	—	ns	
I2SCLn high level width	t_{HIGH}	600	—	—	ns	
Bus free time (time from start to stop condition)	t_{BUF}	1300	—	—	ns	
Start condition hold time	t_{HSTA}	600	—	—	ns	
Restart condition setup time	t_{SSTA}	600	—	—	ns	
Stop condition setup time	t_{SSTO}	600	—	—	ns	
I2SDAn setup time	t_{SDAT}	100	—	—	ns	
I2SDAn hold time	t_{HDAT}	0	—	900	ns	

Note: n = 0 to 3

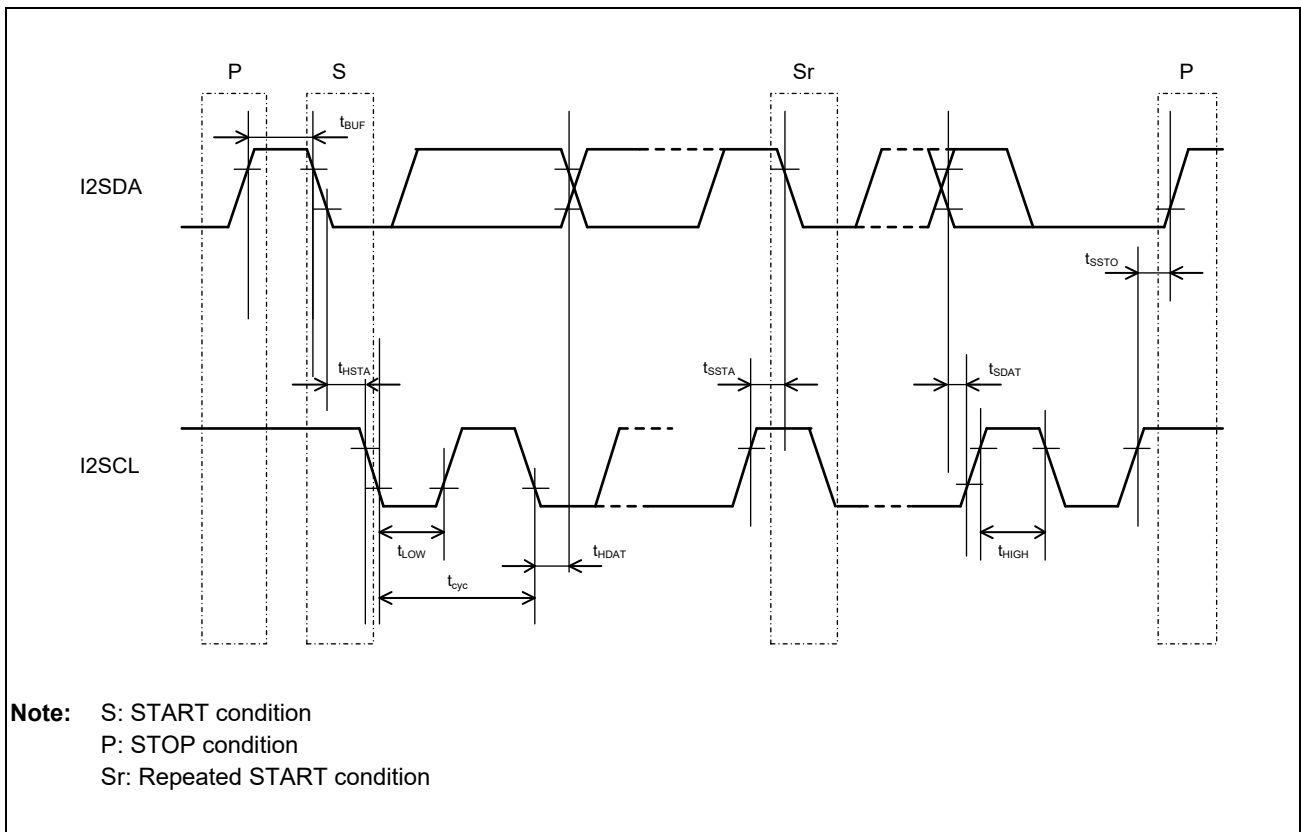


Figure 3.5-1 IIC Timing

3.5.2 Clocked Serial Interface (CSI)

3.5.2.1 Master Mode

Table 3.5-2 Master Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
CSSCLKn cycle time	t_{cyc}	41.66	—	—	ns	
CSSCLKn output low level width	t_{LOW}	18	—	—	ns	Falling edge mode*1
CSSCLKn output high level width	t_{HIGH}	18	—	—	ns	Rising edge mode*1
CSRxDn setup time (CSSCLKn rising and falling edges)	t_{SRXD}	$t_{LOW} - 9$	—	—	ns	
CSRxDn hold time (CSSCLKn rising and falling edges)	t_{HRXD}	5.0	—	—	ns	
CSTxDn output delay time (CSSCLKn rising and falling edges)	t_{DTXD}	-5.0	—	7.5	ns	*1

Note: n = 0 to 5

Note 1. The 3-wire serial interface (CSI) should be used with a driving ability of at least X2.
 Select one of the driving abilities listed below according to the load capacitance.
 X2@C_L = 15 pF, X4@C_L = 20 pF

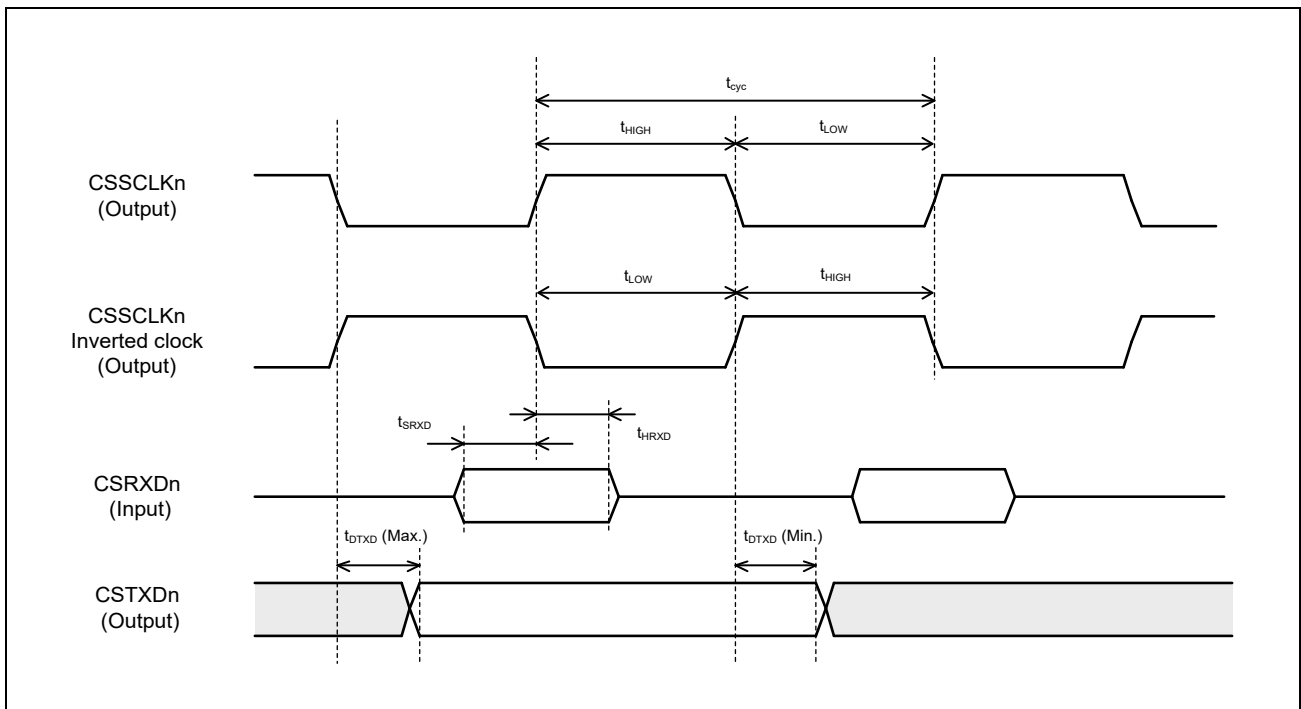


Figure 3.5-2 Master Mode Timing

3.5.2.2 Slave Mode

Table 3.5-3 Slave Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
CSSCLKn cycle time	t_{cyc}	41.66	—	—	ns	
CSSCLKn input low level width	t_{LOW}	18	—	—	ns	Falling edge mode
CSSCLKn input high level width	t_{HIGH}	18	—	—	ns	Rising edge mode
CSRXDn setup time (CSSCLKn rising and falling edges)	t_{SRXD}	7.5	—	—	ns	
CSRXDn hold time (CSSCLKn rising and falling edges)	t_{HRXD}	5.0	—	—	ns	
CSCSn setup time (CSSCLKn rising and falling edges)	t_{SCS}	84	—	—	ns	
CSCSn hold time (CSSCLKn rising and falling edges)	t_{HCS}	21	—	—	ns	
CSTXDn output delay time (CSSCLKn rising and falling edges)	t_{DTXD}	-5.0	—	10.5	ns	*1

Note: n=0 to 5

Note 1. The 3-wire serial interface (CSI) should be used with a driving ability of at least X2.
 Select one of the driving abilities listed below according to the load capacitance.
 X2@C_L = 15 pF, X4@C_L = 20 pF

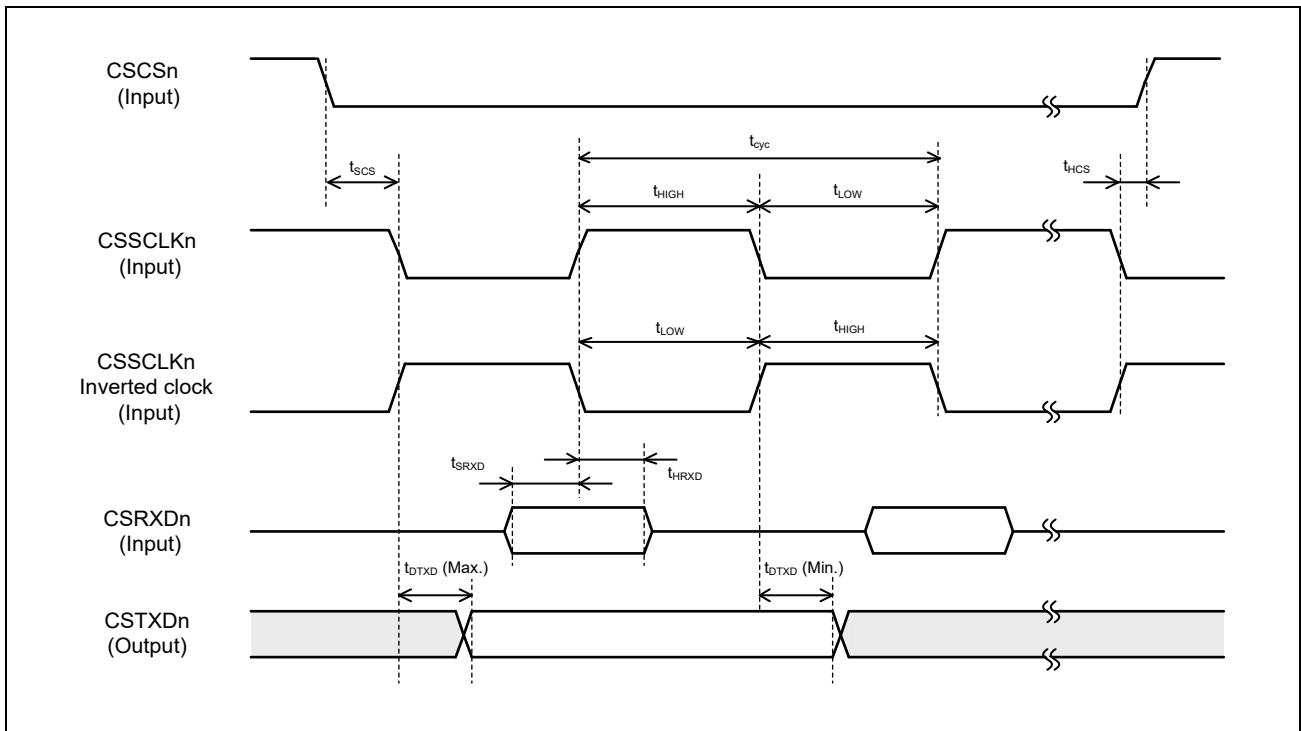


Figure 3.5-3 Slave Mode Timing

3.5.3 Ethernet MAC interface (ETHER)

3.5.3.1 100-Mbps Ethernet Mode

Table 3.5-4 100-Mbps Ethernet Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
GETXC cycle time	t_{Tcyc}	39.5	40	40.5	ns	
GETXEN output delay time	t_{DTXE}	0	—	25	ns	
GETXD output delay time	t_{DTXD}	0	—	25	ns	
GERXC cycle time	t_{Rcyc}	39.5	40	40.5	ns	
GERXDV setup time	t_{SRXV}	10	—	—	ns	
GERXDV hold time	t_{HRXV}	10	—	—	ns	
GERXD setup time	t_{SRXD}	10	—	—	ns	
GERXD hold time	t_{HRXD}	10	—	—	ns	
GERXER setup time	t_{SRER}	10	—	—	ns	
GERXER hold time	t_{HRER}	10	—	—	ns	

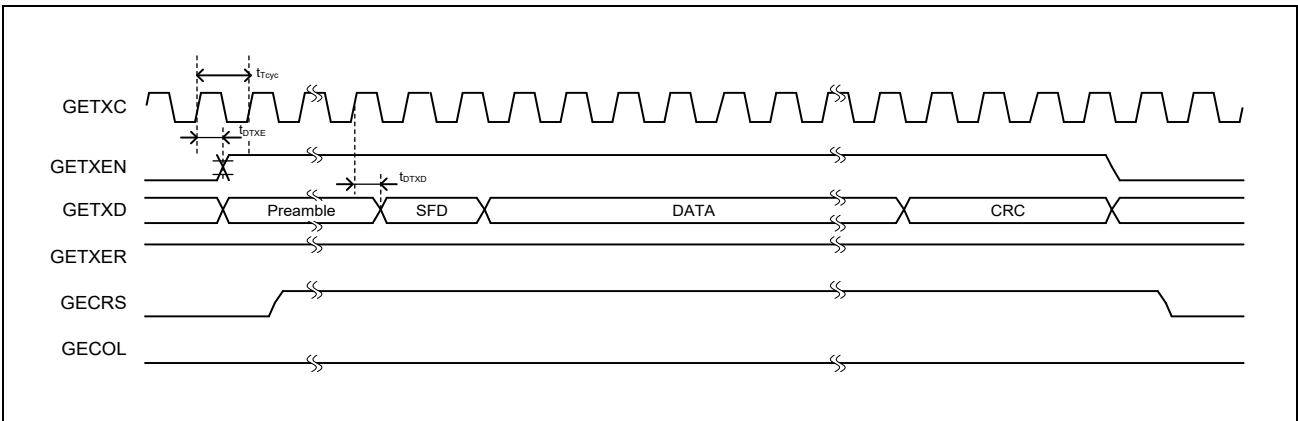


Figure 3.5-4 Transmission Timing

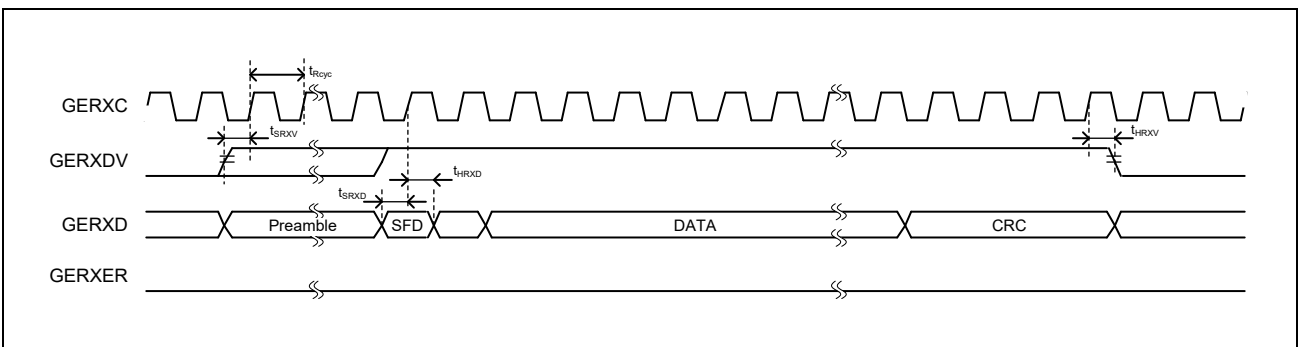


Figure 3.5-5 Reception Timing (Normal)

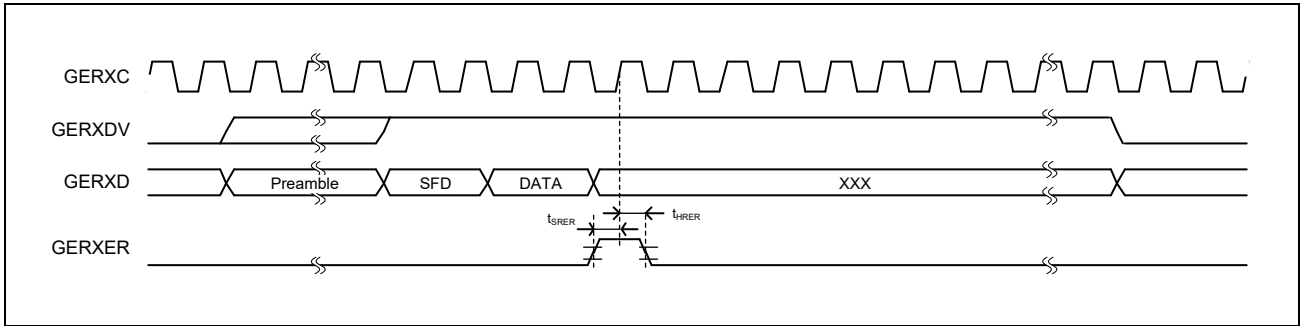


Figure 3.5-6 Reception Timing (in Cases of Error)

3.5.3.2 1-Gbps Ethernet Mode

Table 3.5-5 1-Gbps Ethernet Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
GECLK input frequency	$f_{REF125CK}$	125 - 100 ppm	—	125 + 100 ppm	MHz	
GECLK input duty ratio	I_{DUTY}	45	50	55	%	
GEGTXCLK cycle time	t_{GTcyc}	7.5	8	8.5	ns	
GETXEN output delay time	t_{dGTXE}	0.5	—	5.5	ns	
GETXD output delay time	t_{dGTXD}	0.5	—	5.5	ns	
GERXC cycle time	t_{GRcyc}	7.5	8	8.5	ns	
GERXDV setup time	t_{sGRXV}	2.5	—	—	ns	
GERCDV hold time	t_{HGRXV}	0.5	—	—	ns	
GERXD setup time	t_{sGRXD}	2.5	—	—	ns	
GERXD hold time	t_{HGRXD}	0.5	—	—	ns	
GERXER setup time	t_{sGRER}	2.5	—	—	ns	
GERXER hold time	t_{HGRER}	0.5	—	—	ns	

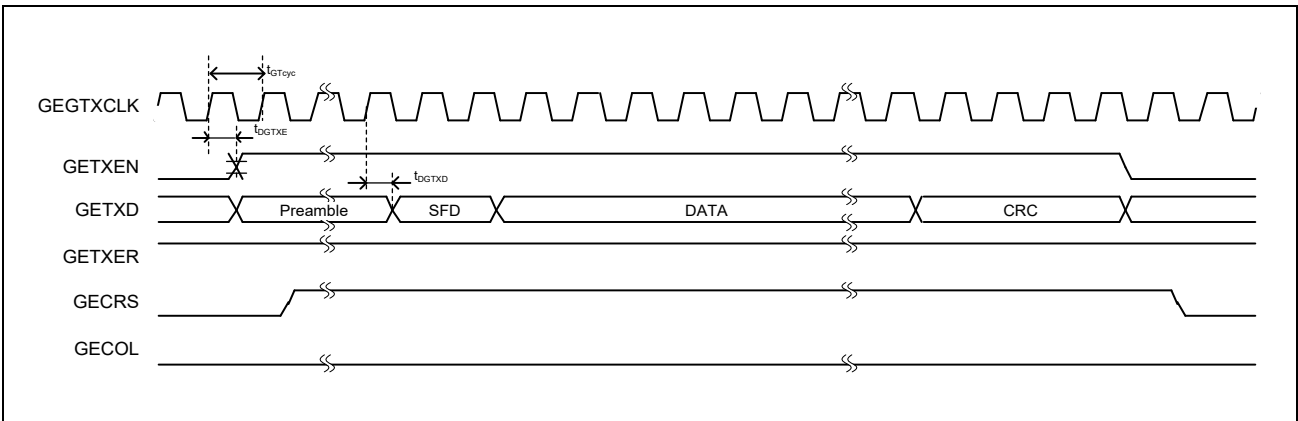


Figure 3.5-7 Transmission Timing

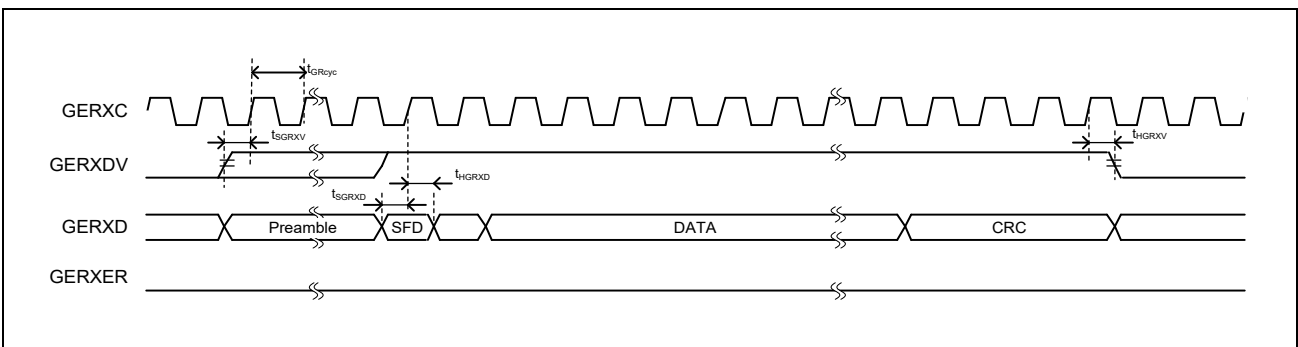


Figure 3.5-8 Reception Timing (Normal)

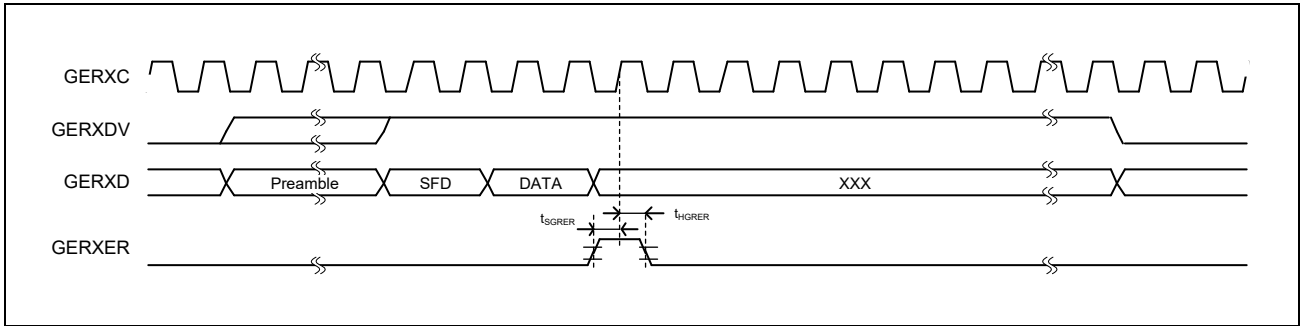


Figure 3.5-9 Reception Timing (in Cases of Error)

3.5.4 SD Host Interface (SDI)

This LSI includes *the SD host interfaces that are compliant with the SD specification version 3.01.*

3.5.5 eMMC Interface (eMMC)

The eMMC interface should be used with a driving ability of at least X2.

Table 3.5-6 HS200 Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	5	—	10	ns	$C_L = 15 \text{ pF}$
MMCLK output low level width	t_{LOW}	1.5	—	—	ns	$V_{OH} = 0.65 \times V_{DD}(\text{NAMODV}_{DD})$
MMCLK output high level width	t_{HIGH}	1.5	—	—	ns	$V_{OL} = 0.35 \times V_{DD}(\text{NAMODV}_{DD})$
MMCLK rise time	t_r	—	—	1	ns	$V_{DD}(\text{NAMODV}_{DD})$
MMCLK fall time	t_f	—	—	1	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	-1.5	—	0.9	ns	
MMCMD/ MMDAT setup time*1	t_{SDAT}	—	—	—	ns	
MMCMD/ MMDAT hold time*1	t_{HDAT}	—	—	—	ns	
MMCMD/ MMDAT data width*1	t_{WDAT}	2.88	—	—	ns	

Note 1. In HS200 mode, the sampling clock controller (SCC) must be used for tuning.

Table 3.5-7 High Speed Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	20	—	—	ns	$C_L = 30 \text{ pF}$
MMCLK output low level width	t_{LOW}	6.5	—	—	ns	1.8-V operation: $V_{OH} = 0.65 \times V_{DD}(\text{NAMODV}_{DD})$
MMCLK output high level width	t_{HIGH}	6.5	—	—	ns	$V_{OL} = 0.35 \times V_{DD}(\text{NAMODV}_{DD})$
MMCLK rise time	t_r	—	—	3	ns	3.3-V operation: $V_{OH} = 0.625 \times V_{DD}(\text{NAMODV}_{DD})$
MMCLK fall time	t_f	—	—	3	ns	$V_{OL} = 0.25 \times V_{DD}(\text{NAMODV}_{DD})$
MMCMD/ MMDAT output delay time	t_{DDAT}	-6.5	—	2.5	ns	$V_{OL} = 0.25 \times V_{DD}(\text{NAMODV}_{DD})$
MMCMD/ MMDAT setup time	t_{SDAT}	4.0	—	—	ns	
MMCMD/ MMDAT hold time	t_{HDAT}	2.0	—	—	ns	

Table 3.5-8 Backward Compatible Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	40	—	—	ns	$C_L = 30$ pF
MMCLK output low level width	t_{LOW}	10	—	—	ns	1.8-V operation: $V_{OH} = 0.65 \times V_{DD}(NAMODV_{DD})$
MMCLK output high level width	t_{HIGH}	10	—	—	ns	$V_{OL} = 0.35 \times V_{DD}(NAMODV_{DD})$
MMCLK rise time	t_r	—	—	10	ns	3.3-V operation: $V_{OH} = 0.625 \times V_{DD}(NAMODV_{DD})$
MMCLK fall time	t_f	—	—	10	ns	$V_{OH} = 0.625 \times V_{DD}(NAMODV_{DD})$
MMCMD/ MMDAT output delay time	t_{DDAT}	-7.5	—	2.5	ns	$V_{OL} = 0.25 \times V_{DD}(NAMODV_{DD})$
MMCMD/ MMDAT setup time	t_{SDAT}	4.0	—	—	ns	
MMCMD/ MMDAT hold time	t_{HDAT}	2.0	—	—	ns	

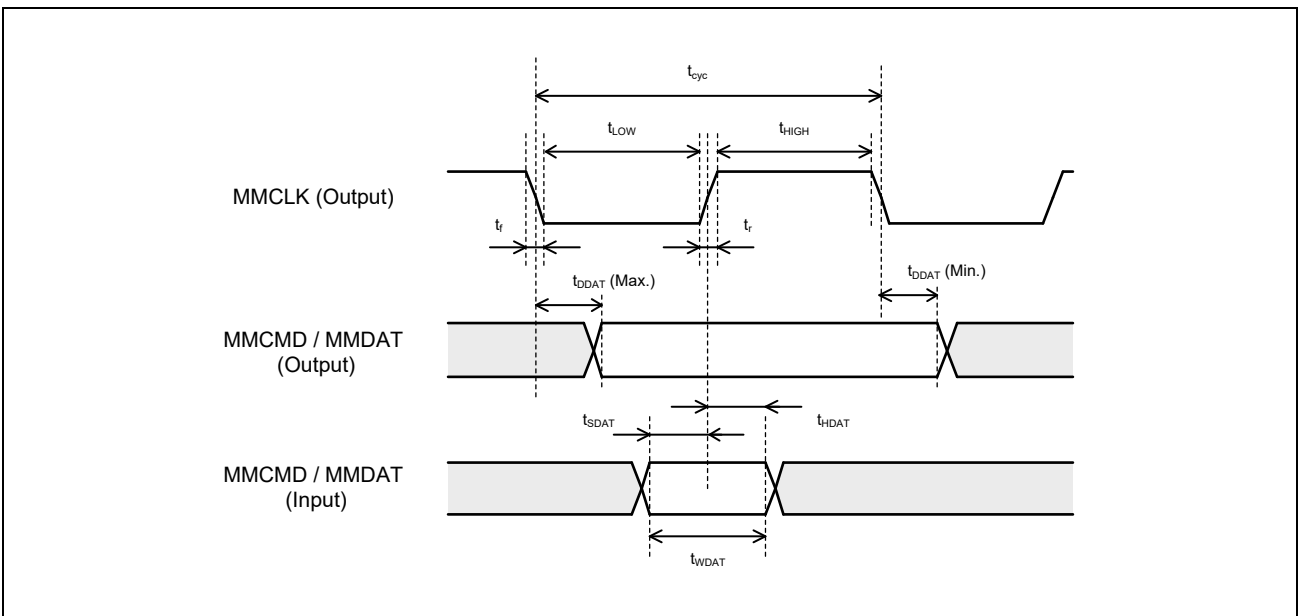


Figure 3.5-10 eMMC Timing

3.5.6 Image Sensor Timing Generator (STG)

3.5.6.1 Clock Synchronous Serial Interface

Table 3.5-9 Clock Synchronous Serial Data I/O Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
IMnSCLK cycle time	t_{cyc}	26.9	—	—	ns	
IMnSCLK output low level time	t_{LOW}	$t_{cyc} \times 0.45$	—	$t_{cyc} \times 0.55$	ns	
IMnSCLK output high level time	t_{HIGH}	$t_{cyc} \times 0.45$	—	$t_{cyc} \times 0.55$	ns	
IMnTXD output delay time	t_{DTXD}	-3	—	3	ns	$C_L = 15 \text{ pF}$
IMnRXD setup time	t_{SRXD}	$t_{cyc} - 12$	—	—	ns	
IMnRXD hold time	t_{HRXD}	0	—	—	ns	

Note: n = 0, 1

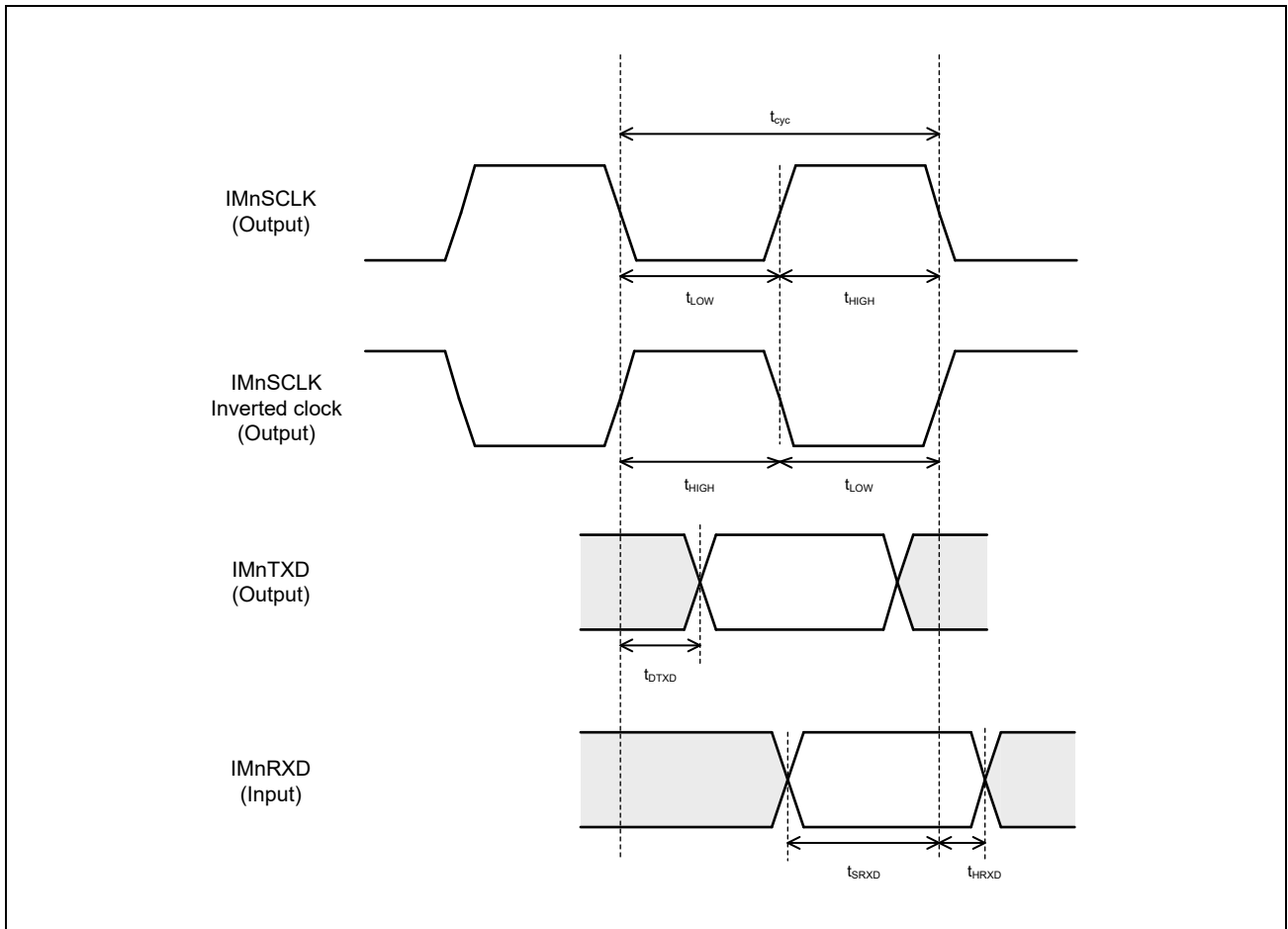


Figure 3.5-11 Clock Synchronous Serial Data I/O Timing

Table 3.5-10 Clock Synchronous HS/VS/SIG0 Signal Output Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
IMnSCLK cycle time	t_{cyc}	13.4	—	—	ns	
IMnSCLK output low level time	t_{LOW}	$t_{cyc} \times 0.45$	—	$t_{cyc} \times 0.55$	ns	
IMnSCLK output high level time	t_{HIGH}	$t_{cyc} \times 0.45$	—	$t_{cyc} \times 0.55$	ns	
IMnHS/ IMnVS/ IMnSIG0 output delay time	t_{DSIG}	-3	—	3	ns	$C_L = 15 \text{ pF}$

Note: n = 0, 1

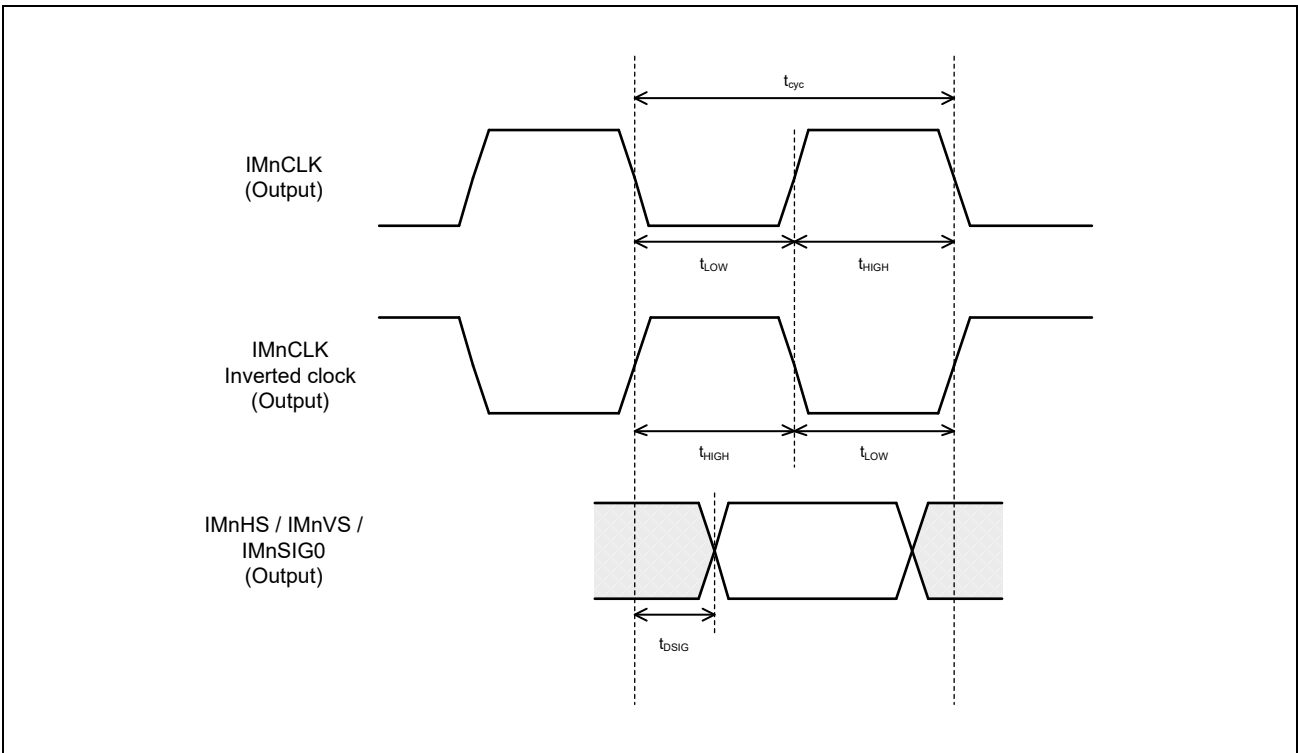


Figure 3.5-12 Clock Synchronous HS/VS/SIG0 Signal Output Timing

3.5.6.2 IIC Interface

Table 3.5-11 IIC Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
IMnSCL cycle time	t_{cyc}	2500	—	—	ns	
IMnSCL low level width	t_{LOW}	1300	—	—	ns	
IMnSCL high level width	t_{HIGH}	600	—	—	ns	
Bus free time (time from start to stop condition)	t_{BUF}	1300	—	—	ns	
Start condition hold time	t_{HSTA}	600	—	—	ns	
Restart condition setup time	t_{SSTA}	600	—	—	ns	
Stop condition setup time	t_{SSTO}	600	—	—	ns	
IMnSDA setup time	t_{SDAT}	100	—	—	ns	
IMnSDA hold time	t_{HDAT}	0	—	900	ns	

Note: n = 0, 1

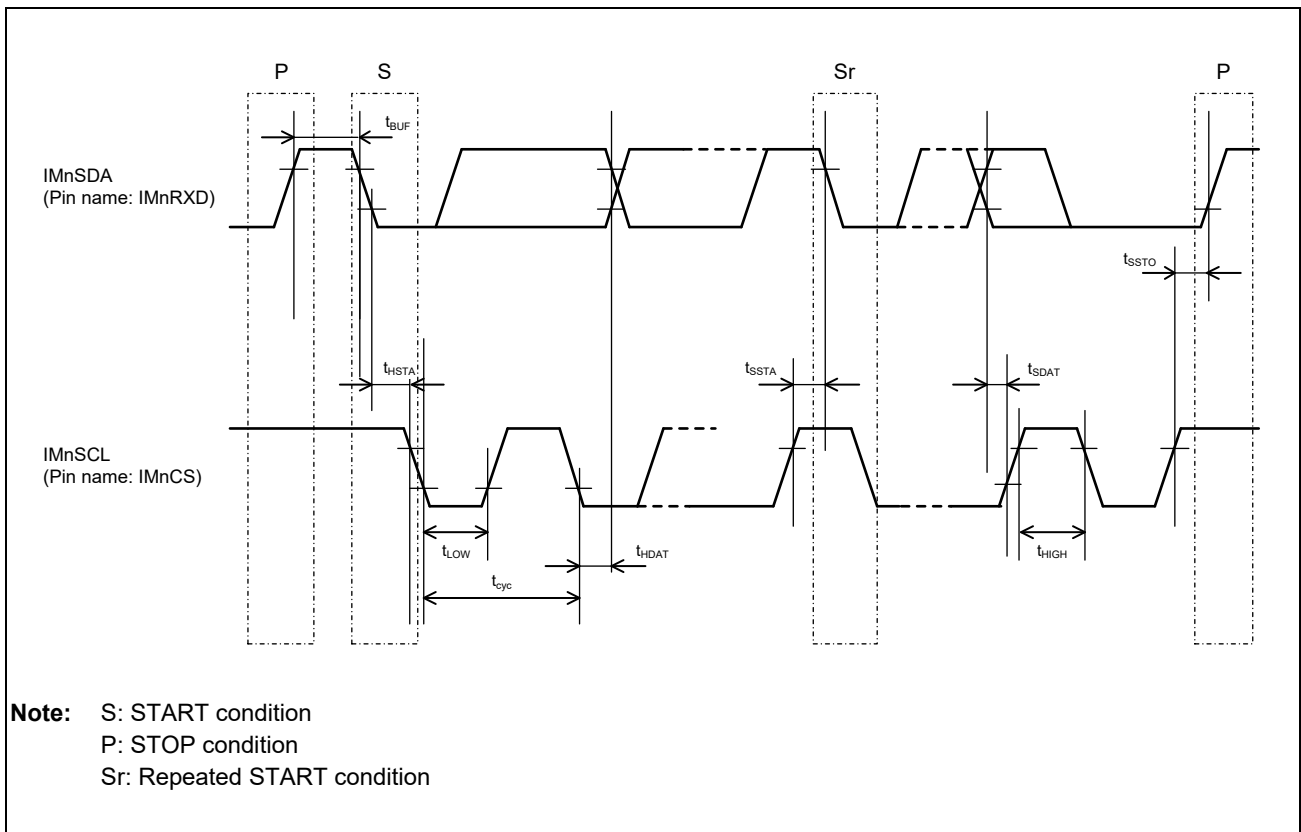


Figure 3.5-13 IIC Timing

3.5.7 Audio Interface (AUI)

Table 3.5-12 Audio Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
AUBICK cycle time	t_{cyc}	325.5	—	—	ns	
AUBICK low level time	t_{LOW}	$t_{cyc} \times 0.45$	—	$t_{cyc} \times 0.55$	ns	
AUBICK high level time	t_{HIGH}	$t_{cyc} \times 0.45$	—	$t_{cyc} \times 0.55$	ns	
AUDO output delay time	t_{DAU}	41.6	—	79.5	ns	$C_L = 15 \text{ pF}$
AUDI/ AULRCK setup time	t_{SAU}	26.9	—	—	ns	
AUDI/ AULRCK hold time	t_{HAU}	26.9	—	—	ns	

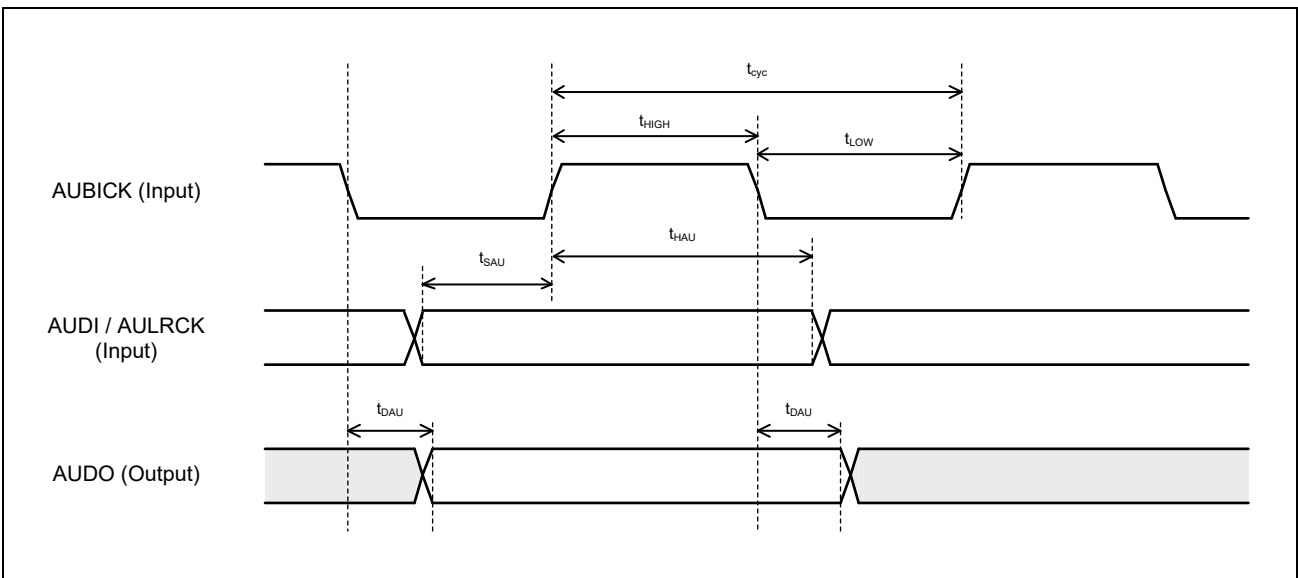


Figure 3.5-14 Audio Interface Timing

3.5.8 TRACE Interface (TRACE)

Table 3.5-13 TRACE Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
TRCLK cycle time	t_{cyc}	20	—	—	ns	
TRCLK output low level width	t_{LOW}	9	—	—	ns	
TRCLK output high level width	t_{HIGH}	9	—	—	ns	
TRCTL/ TRDATA output delay time (TRCLK rising edge)	t_{DRDAT}	2	—	7	ns	
TRCTL/ TRDATA output delay time (TRCLK falling edge)	t_{DFDAT}	2	—	7	ns	

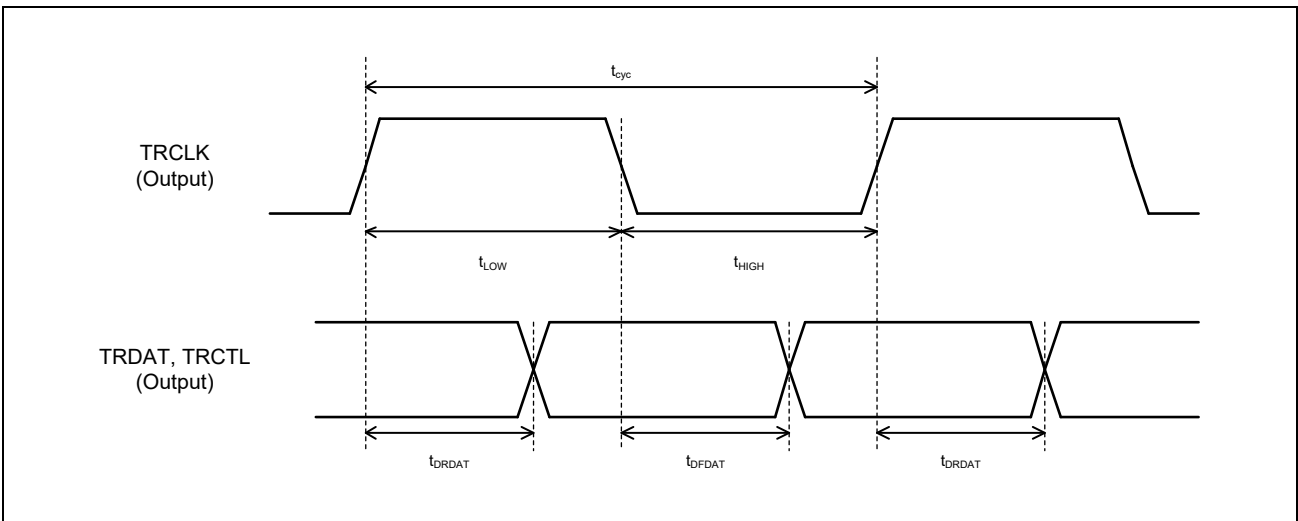


Figure 3.5-15 TRACE Interface Timing

3.6 Various Analog Characteristics

3.6.1 MIPI CSI-2 PHY Characteristics

The MIPI CSI-2 Rx D-PHY of this LSI is equivalent to the MIPI CSI-2 Ver.1.2/D-PHY Ver.1.2. For details, refer to the MIPI specification.

3.6.2 HDMI Tx PHY Characteristics

The HDMI Tx PHY of this LSI is compliant with the following HDMI 1.4a standard:

Version 1.4a of *the High-Definition Multimedia Interface Specification*, released on March 4, 2010

3.6.3 LPDDR4 PHY Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4A standard.

3.6.4 USB PHY Characteristics

The USB PHY of this LSI is compliant with the following USB 3.1 GEN1 standard:

Universal Serial Bus 3.1 Specification

3.6.5 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of *the PCI Express® Base Specification* for Gen1/Gen 2

3.6.6 ADC Characteristics

Table 3.6-1 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Resolution	—	—	12	—	Bit	
Differential non-linearity	DNL	—	±1.0	±3.0	LSB	F _{AIN} = 100 kHz, Ramp wave
Integral non-linearity	INL	—	±2.0	±6.0	LSB	
Top offset voltage	EOT	—	±10	±20	LSB	
Bottom offset voltage	EOB	—	±10	±20	LSB	

Table 3.6-2 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Main clock duty ratio	—	45	50	55	%	
Analog input frequency (AD0AIN11-AD0AIN0, AD1AIN7-AD1AIN0)	F _{AIN}	DC	—	100k	Hz	

Table 3.6-3 Recommended External Input Resistance

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
External input resistance*1 (AD0AIN11-AD0AIN0, AD1AIN7-AD1AIN0)	R _{ext}	—	—	2	kΩ	FCLK = 10 MHz

Note 1. Output resistance of signal generator + Series parasitic resistance between signal source and ADC input

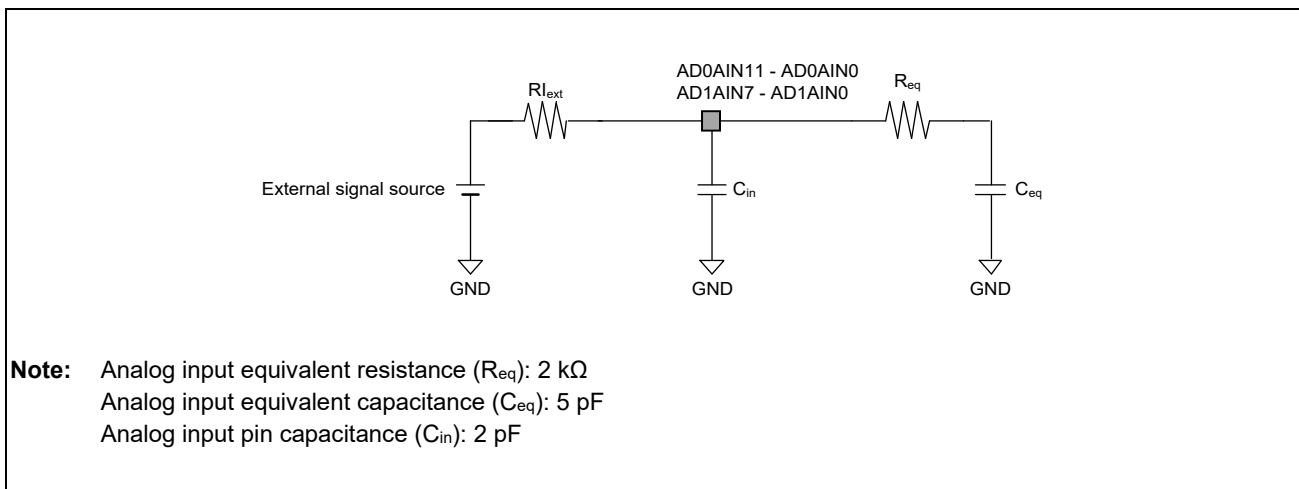


Figure 3.6-1 ADC Input Equivalent Circuit

3.6.7 Temperature Sensor Characteristics

Table 3.6-4 Temperature Sensor Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Accuracy from 70°C to 125°C	Acc70_125	—	±2.0	±3.0	°C	
Accuracy from -40°C to 70°C	Accm40_70	—	±3.0	±5.0	°C	

3.7 Oscillation Circuits for Connecting Crystal Resonators (OSC)

This LSI chip includes two oscillation circuits (OSC) for connection to crystal resonators, specifically a 48-MHz crystal resonator for the system clock and a 32.768-kHz crystal resonator for the real-time clock. **Table 3.7-1** lists the pins for connecting the crystal resonators and the clock frequencies. **Figure 3.7-1** shows an example of the connections with crystal resonators.

Table 3.7-1 Pins for Connecting Crystal Resonators and Clock Frequency

External Pin Name	I/O	Clock Frequency
For the system clock		
XIN	Input	48 MHz (frequency deviation: ±50 ppm, frequency temperature characteristic: ±30 ppm)
XOUT	Output	48 MHz
For the real-time clock		
RTXIN	Input	32.768 kHz (frequency deviation: ±20 ppm)
RTXOUT	Output	32.768 kHz

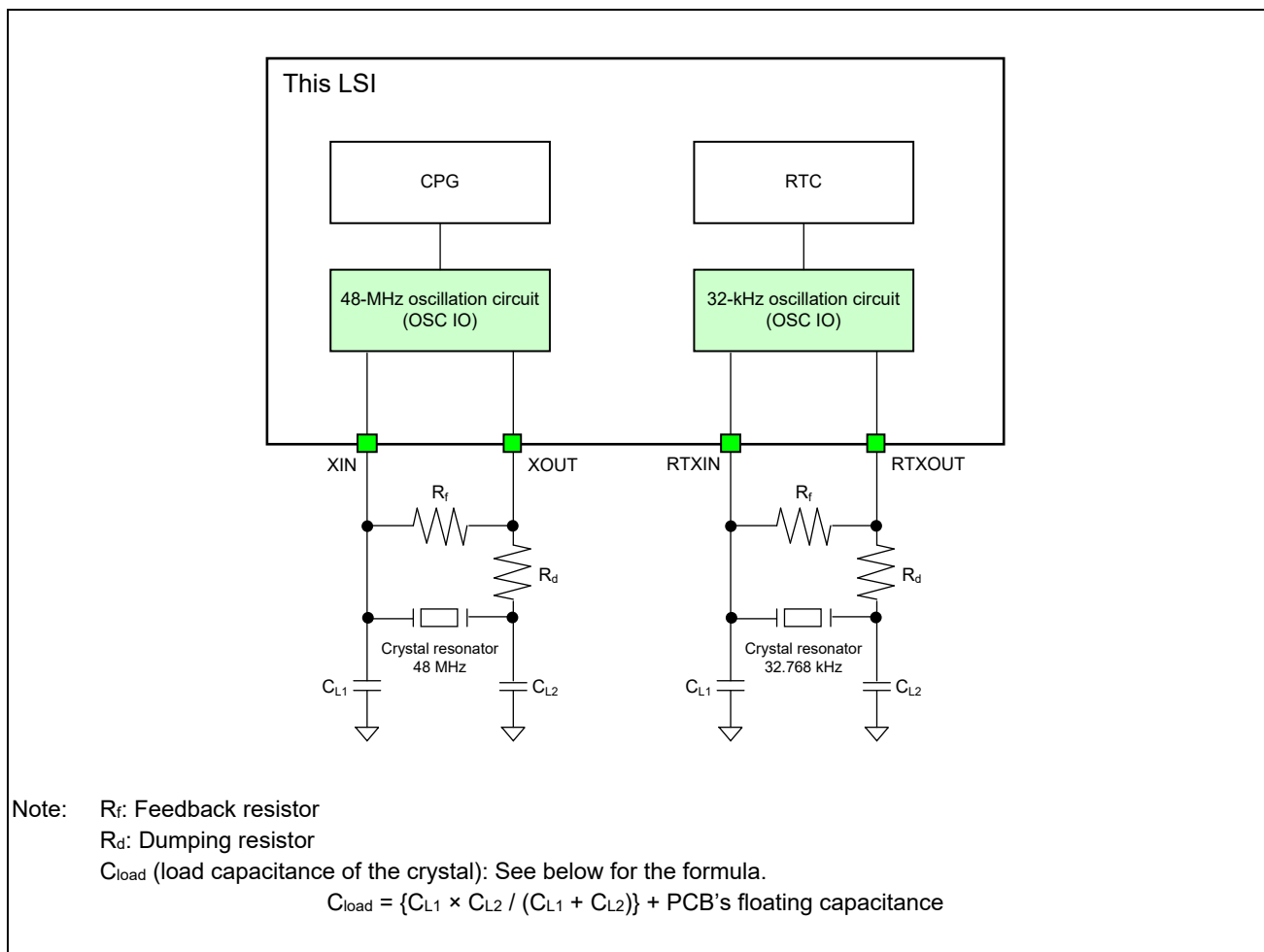


Figure 3.7-1 Example of Connections with Crystal Resonators

Place the crystal resonators and the capacitors C_{L1} and C_{L2} as close as possible to the pins to connect crystal resonators. To avoid interference and to ensure correct oscillation, the grounding points of the capacitors appended to the crystal resonators should be shared, and no wiring patterns should be placed near these components.

The characteristics of the crystal resonators are closely related to the design of the user board. Therefore, the user should sufficiently evaluate them with reference to the example of connection of crystal resonators in **Figure 3.7-1**.

The circuit rating of a crystal resonator depends on the crystal resonator and the stray capacitance of the mounting circuit. Therefore, contact the manufacturer of the crystal resonator before deciding upon the circuit rating. The user should thoroughly evaluate and then set the parameters (resistor and capacitor values).

Table 3.7-2 is a list of recommended values for the crystal resonators.

Table 3.7-2 Recommended Model Values for the Crystal Resonators

Clock Frequency	Model Values for the Crystal Resonators			
	Max. ESR* ¹	Max. C_L * ²	Max. C_0 * ³	Max. Drive Level
32.768 kHz	70 k Ω	12.5 pF	1.4 pF	1 μ W
48 MHz	50 Ω	10 pF	7 pF	100 μ W

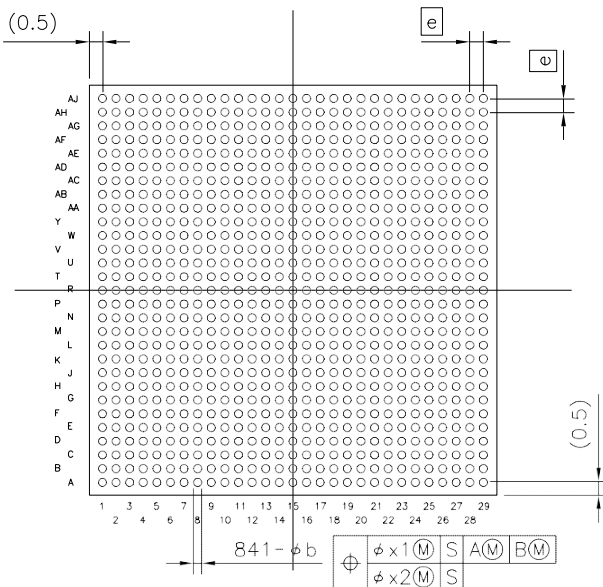
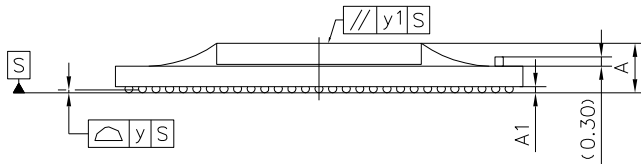
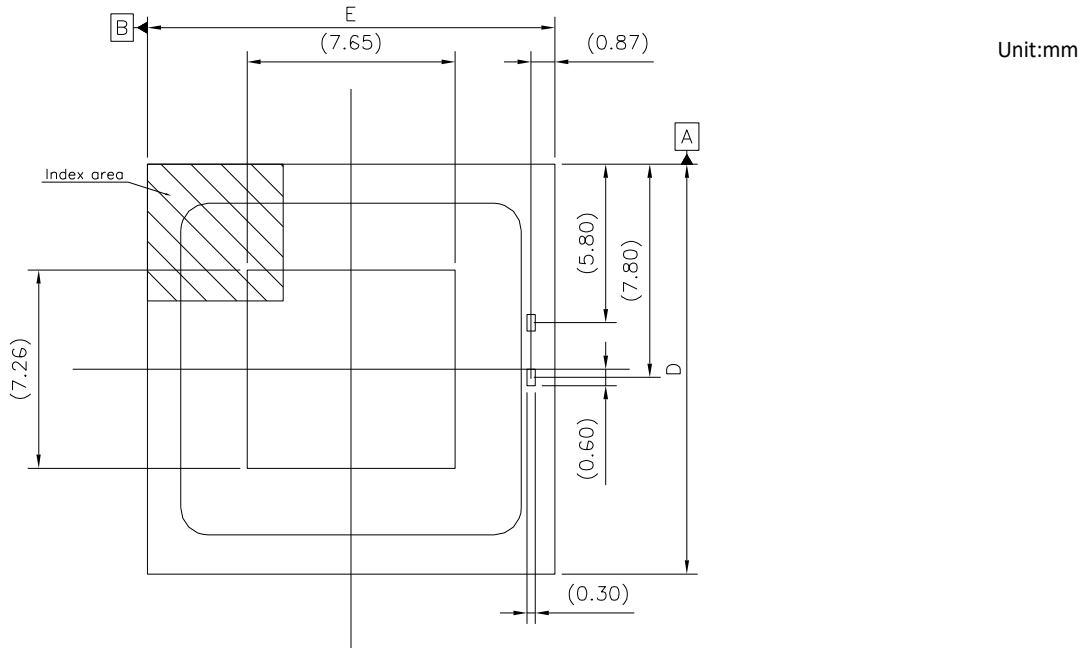
Note 1. ESR means the equivalent series resistor of the crystal resonator.

Note 2. C_L is the load capacitance of the crystal resonator.

Note 3. C_0 is the parallel capacitance of the crystal resonator.

Section 4 Package Dimensions

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA841-15x15-0.50	PRBG0841KA-A	-	0.71



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.85	15.00	15.15
E	14.85	15.00	15.15
e	-	0.50	-
A	(1.70)	(1.90)	2.10
A1	0.15	(0.25)	-
b	0.25	0.30	0.35
x1	-	-	0.20
x2	-	-	0.05
y	-	-	0.12
y1	-	-	0.20

Figure 4.1 Package Dimensions

REVISION HISTORY	RZ/V Series, VisionAI_ASSP RZ/V2M Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Apr 28, 2021	—	First edition issued
1.10	Jul 23, 2021	Section 1 Overview	
		4	Table 1.3-1 Overview of Functions (2/4): Video & graphics: JPEC → JPEG
		6	Table 1.3-1 Overview of Functions (4/4): Operating temperature: T _j , modified
		Section 2 Pins	
		30	2.2.1 List of External Pins: Usage Note, added
		43	Table 2.3-1 List of Pin Functions (5/7): The functional description of the LVRXREXT pin, modified
		43	Table 2.3-1 List of Pin Functions (5/7): The functional description of the DSMVREG0P4V pin, modified
		45	Table 2.3-1 List of Pin Functions (7/7): The functional description of the MD3 pin, modified
		Section 3 Functional Specifications	
		48	3.2 Memory: RAM (RMAB) → RAM (RAMB)
		63	3.11.2 USB Interface: low-speed (1.5 MHz) → low-speed (1.5 Mbps)
		Section 4 Electrical Characteristics	
		81	Table 4.1-1 Absolute Maximum Ratings (3/3): Case temperature (T _c), deleted
		83	Table 4.2-1 Recommended Operating Range (2/2): Junction temperature (T _j), added
		93	Table 4.4-1 Max. Supply Currents during Operation (2/2): I _{DDLVPDD} : The max. value, modified
		116	4.6.1 MIPI CSI-2 PHY Characteristics: The description, modified
		116	4.6.2 MIPI DSI Tx D-PHY Characteristics: The description, modified
		116	4.6.3 HDMI Tx PHY Characteristics: The description, modified: this LSI chip → this LSI
		116	4.6.4 LPDDR4 PHY Characteristics: The description, modified: this LSI chip → this LSI
		116	4.6.5 USB PHY Characteristics: The description, modified: this LSI chip → this LSI
116	4.6.6 PCI Express PHY Characteristics: The description, modified		
2.00	Jul 19, 2024	Section 1 Overview	
		1	1.1 Features The functional description of "Vision and AI", "Video and Graphics, Display", and "High Speed Interfaces", modified
		2	Figure 1.1-1 Diagram of Functional Overview Note 1, deleted
		3	Table 1.3-1 Overview of Functions (1/4) Note 1, modified
		4	Table 1.3-1 Overview of Functions (2/4) The "Function" column of "Video & graphics" and "External memory interfaces", modified
		5	Table 1.3-1 Overview of Functions (3/4) The "Function" column of "Peripheral interfaces", "Display interfaces", and "Security engine", modified
		Section 2 Pins	
		13 to 31	Table 2.2-1 List of External Pins, modified
		32	Table 2.2-2 List of Multiplexed Functional Blocks, modified
		33	Table 2.2-3 I/O Group PORT00 in the Multiplexed Mode, modified
		33	Table 2.2-4 I/O Group PORT01 in the Multiplexed Mode, modified
		34	Table 2.2-5 I/O Group PORT02 in the Multiplexed Mode Note 1, added
		34	Table 2.2-6 I/O Group PORT03 in the Multiplexed Mode, modified

Rev.	Date	Description	
		Page	Summary
2.00	Jul 19, 2024	35	Table 2.2-7 I/O Group PORT04 in the Multiplexed Mode Note 1, added
		35	Table 2.2-8 I/O Group PORT05 in the Multiplexed Mode Note 1, added
		35	Table 2.2-9 I/O Group PORT06 in the Multiplexed Mode Note 1, added
		36	Table 2.2-10 I/O Group PORT07 in the Multiplexed Mode Note 1, added
		37	Table 2.2-13 I/O Group PORT10 in the Multiplexed Mode Note 1, added
		37	Table 2.2-14 I/O Group PORT11 in the Multiplexed Mode Note 1, added
		37	Table 2.2-15 I/O Group PORT12 in the Multiplexed Mode, modified
		38	Table 2.2-16 I/O Group PORT13 in the Multiplexed Mode, modified
		38	Table 2.2-17 I/O Group PORT14 in the Multiplexed Mode, modified
		39	Table 2.2-19 I/O Group PORT16 in the Multiplexed Mode, modified
		39	Table 2.2-20 I/O Group PORT17 in the Multiplexed Mode, modified
		40	Table 2.2-21 I/O Group PORT20 in the Multiplexed Mode Note 1, added
		40	Table 2.2-22 I/O Group PORT21 in the Multiplexed Mode Note 1, added
		41	Table 2.3-1 List of Pin Functions (1/7) Pin Name: The "Function" column of "PWKY2N to PWKY0N" and "PWKY4N, PWKY3N", modified Classification: NAND flash interface, deleted
		43	Table 2.3-1 List of Pin Functions (3/7) Classification: Flash control, modified Pin Name: IMSHUT0 and IMSHUT1, deleted
		44	Table 2.3-1 List of Pin Functions (4/7) Classification: Motor controller, deleted Pin Name: GEPPS, deleted
		45	Table 2.3-1 List of Pin Functions (5/7) Classification: Reserved pins, modified Pin Name: The "Function" column of "DSMDPDATA3 to DSMDPDATA0", "DSMDNDATA3 to DSMDNDATA0", "DSMDPCLK", "DSMDNCLK", and "DSMVREG0P4V", modified
		46	Table 2.3-1 List of Pin Functions (6/7) Pin Name: The "Function" column of "USVBUS" and "USOTGID", modified Classification: Environment sensor interface, deleted
		47	Table 2.3-1 List of Pin Functions (7/7) Classification: The "Pin Name" and "Function" columns of "Boot", modified Classification: Clock output, modified Pin Name: GFPLS0 and GFPLS1, deleted
		48	Table 2.3-1 List of Pin Functions Notes 2 and 3, modified Notes 4, 5, and 6, added
			Section 3 Functional Specifications, deleted
			Section 3 Electrical Characteristics
		51	Table 3.1-1 Absolute Maximum Ratings (2/3), modified
		54	Table 3.2-1 Recommended Operating Range (2/2), modified
		55	3.3.1 Power-On Sequence (RTC/PWC): The section title, modified

Rev.	Date	Description	
		Page	Summary
2.00	Jul 19, 2024	—	Figure 4.3-2 Power-Off Sequence (RTC/PWC), deleted
		63	Table 3.4-1 Max. Supply Currents during Operation (2/2), modified
		64, 65	Table 3.4-2 DC Characteristics, modified
		—	4.5.7 Motor Controller (MTR), deleted
		—	4.5.8 Environment Sensor Interface (ESI), deleted
		—	4.5.10 Debugger Interface, deleted
		—	4.6.2 MIPI DSI Tx D-PHY Characteristics, deleted

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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