SLG46127

GreenPAK Programmable Mixed-signal Matrix with Dual 44 mΩ / 2 A P-FET

General Description

The SLG46127 GreenPAK combines the functionality and versatility of a GreenPAK Programmable Mixed-signal Matrix with the capabilities of Renesas' CuFET technology. Capable of integrating a number common discrete ICs and passive components into a single device, the GreenPAK family's SLG46127M enables high power switching with dual 2 A P-Ch MOSFETs.

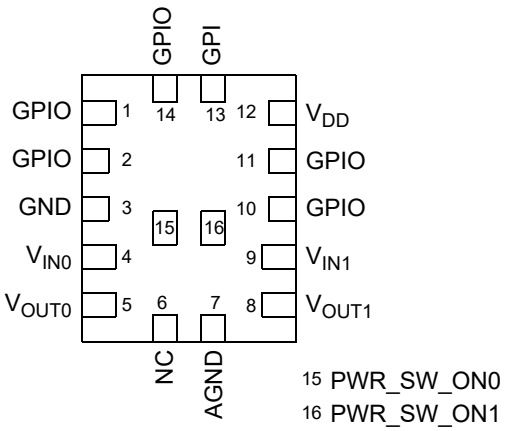
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5 %) to 5 V (±10 %) Supply
- Operating Temperature Range -40 °C to 85 °C
- Dual 44 mΩ, 2 A P-Channel MOSFETs
- Package
  - 1.6 x 2.0 x 0.55 mm MSTQFN 16L package
  - Pb-Free / Halogen-Free / RoHS compliant

Applications

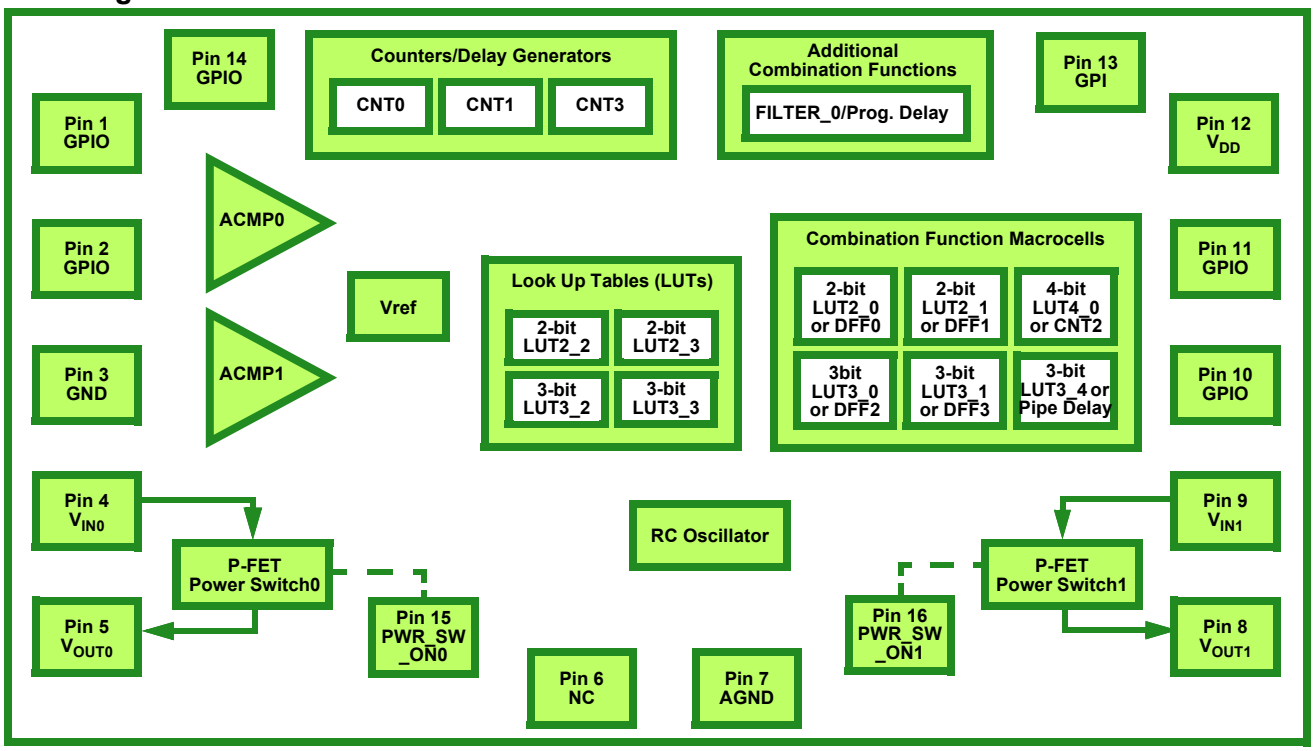
- Power Sequencing with Complex Analog Control
- Power Plane Component Size Reduction Project
- LED Driver
- Haptic Motor Driver
- System RESET with Power Switch

Pin Configuration



16pin MSTQFN
(Top View)

Block Diagram



1.0 Overview

The SLG46127 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46127. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The SLG46127 includes the following:

- Two Analog Comparators (ACMP)
- Voltage References (Vref)
- Four Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Seven Combination Function Macrocell
  - Two Selectable DFF/Latch or 2-bit LUTs
  - Two Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output
  - One Selectable Counter/Delay or 4-bit LUT
  - One Programmable Delay/ Deglitch Filter
- Three Counter / Delay Generators (CNT/DLY)
  - Three 8-bit counter/delays with external clock/reset
- RC Oscillator (RC OSC)
- Power On Reset (POR)
- P-FET Power Switch
  - Power Switch IDS: 2 A
  - V_{IN}: 1.71 V to 5.5 V
  - Low RDSON
    - 44 mΩ @ 5.5 V
    - 58 mΩ @ 3.3 V
    - 110 mΩ @ 1.71 V

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	GPIO	General Purpose I/O or Analog Comparator 0 (-)
2	GPIO	General Purpose I/O or Analog Comparator 1 (+) with OE
3	GND	Ground
4	V_{IN0}	P-FET Power Switch Input
5	V_{OUT0}	P-FET Power Switch Output
6	NC	No Connect
7	AGND	P-FET Power Switch Ground
8	V_{OUT1}	P-FET Power Switch Output
9	V_{IN1}	P-FET Power Switch Input
10	GPIO	General Purpose I/O with OE and Vref output
11	GPIO	General Purpose I/O or External Clock Input
12	V_{DD}	Power Supply
13	GPI	General Purpose Input
14	GPIO	General Purpose I/O or Analog Comparator 0 (+)
15	PWR_SW_ON0	P-FET Power Switch On
16	PWR_SW_ON1	P-FET Power Switch On

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46127's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Renesas's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Renesas to integrate into the production process.

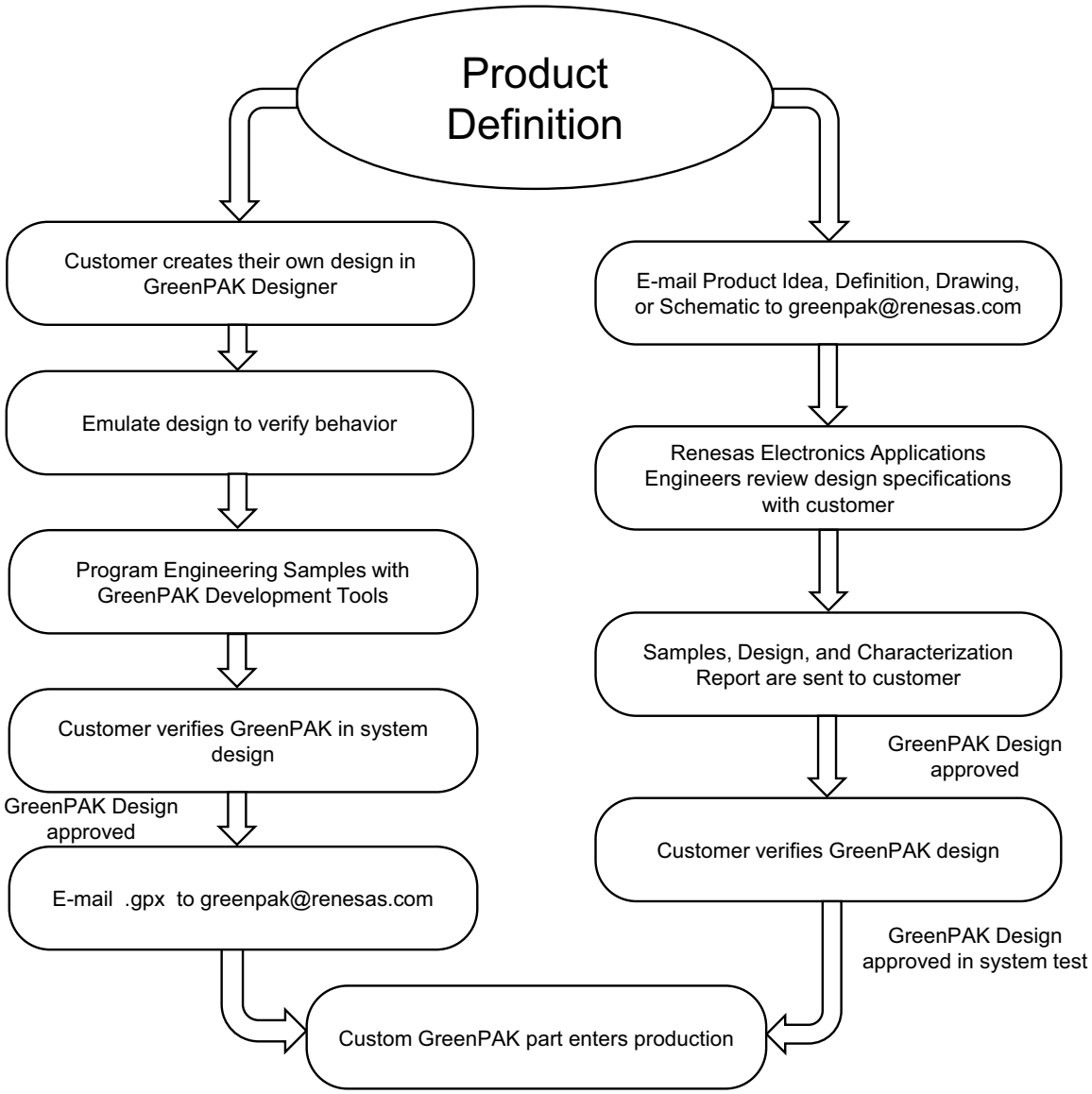


Figure 1. Steps to create a custom Renesas GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46127M	MSTQFN 16L
SLG46127MTR	MSTQFN 16L - Tape and Reel (3k units)

Note 1: Use SLG46127M to order. Shipments are automatically in Tape and Reel.

Note 2: "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter	Condition/Description	Min.	Max.	Unit
Supply Voltage on V_{DD} relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5	V_{DD} + 0.5	V
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		
V_{IN}	P-FET	0.3	V_{DD}	V
Θ_{JA}	Thermal Resistance*	--	99	°C/W
P_D	Maximum Power Dissipation, T_A = +25 °C	--	1.25	W
$T_{J,MAX}$	Maximum Junction Temperature		150	°C
P-FET Power Switch IDS_{CONT}	Total, T_J < 150 °C	--	2	A
P-FET Power Switch IDS_{PK}	For no more than 1 ms with 1 % duty cycle	--	2.5	A
Note: Mounted on 27.4 mm x 30.1 mm PCB (1.6 mm thick, 1 oz copper, FR-4 material).*				

5.2 Electrical Characteristics (1.8 V ±5 % V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.5	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{AIR}	Analog Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.702	1.800	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.010	0.010	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.040	1.400	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.150	2.710	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.130	--	mA
I_{VDD}	Maximum Average or DC Current Through V_{DD} Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	73	mA
		T_J = 110 °C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	92	mA
		T_J = 110 °C	--	--	44	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.27	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.110	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: $V_{IN} = V_{DD}$	--	1	--	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: $V_{IN} = V_{DD}$	--	100	--	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: $V_{IN} = V_{DD}$	--	10	--	kΩ
C_{VDD}	Decoupling Capacitor	Capacitor Value at V_{DD}	--	0.1	--	µF

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 1, 2, 13 and 14 are connected to one side, pins 10, 11, 15 and 16 to another.

5.3 Electrical Characteristics (3.3 V ±10 % V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.75	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{AIR}	Analog Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.710	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.870	3.190	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.180	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.050	0.070	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.830	10.180	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.264	19.660	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.060	6.440	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	16.260	22.900	--	mA
I_{VDD}	Maximum Average or DC Current Through V_{DD} Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	73	mA
		T_J = 110 °C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	92	mA
		T_J = 110 °C	--	--	44	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.27	-	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.110	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{VDD}	Decoupling Capacitor	Capacitor Value at V_{DD}	--	0.1	--	µF

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 1, 2, 13 and 14 are connected to one side, pins 10, 11, 15 and 16 to another.

5.4 Electrical Characteristics (5 V ±10 % V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	1.0	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{AIR}	Analog Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.160	--	V_{DD}	V
		Low-Level Logic Input	1.230	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.150	4.730	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.300	4.860	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.230	0.330	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.070	0.090	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	21.808	29.100	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	40.598	56.080	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.010	9.730	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	11.590	19.460	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	11.760	19.460	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	19.120	35.621	--	mA
I_{VDD}	Maximum Average or DC Current Through V_{DD} Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	73	mA
		T_J = 110 °C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	92	mA
		T_J = 110 °C	--	--	44	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.27	-	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.110	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{VDD}	Decoupling Capacitor	Capacitor Value at V_{DD}	--	0.1	--	µF

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 1, 2, 13 and 14 are connected to one side, pins 10, 11, 15 and 16 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	µA
		Vref	56.9	56.9	63.3	µA
		Vref Buffer (each)	2.7	13.0	13.7	µA
		OSC 25 kHz, predivide = 1	3.1	4.8	6.4	µA
		OSC 25 kHz, predivide = 8	3.0	4.5	6.0	µA
		OSC 2 MHz, predivide = 1	27.4	45.4	67.4	µA
		OSC 2 MHz, predivide = 8	17.5	23.7	29.5	µA
		1st ACMP used (includes Vref)	60.6	62.0	68.4	µA
		Each additional ACMP add	3.7	4.9	5.1	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger - Push Pull	35.3	34.4	14.5	14.3	10.3	10.5	ns
tpd	Delay	Digital Input with Schmitt Trigger - Push Pull	34.8	32.9	14.2	13.8	10.0	10.1	ns
tpd	Delay	Low Voltage Digital input - Push Pull	37.8	450.0	15.0	208.2	10.5	142.3	ns
tpd	Delay	Digital Input without Schmitt Trigger -- NMOS	—	73.5	—	26.0	—	16.3	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	44.6	—	17.9	—	12.4	—	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	—	43.0	—	17.6	—	12.5	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	29.6	24.8	11.5	10.1	8.2	6.9	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	29.2	31.5	11.8	12.5	8.4	8.4	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	33.0	27.4	12.8	11.1	9.1	7.5	ns
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	29.9	32.4	12.1	13.0	8.7	8.7	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	29.2	27.2	11.2	10.8	8.0	7.3	ns
tpd	Delay	2-bit LUT	19.4	18.8	7.2	7.4	5.1	5.0	ns
tpd	Delay	3-bit LUT	22.3	22.7	8.3	8.9	6.0	5.9	ns
tpd	Delay	CNT/DLY	38.4	36.0	15.2	15.1	10.8	10.4	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	41.0	36.2	16.3	15.6	11.5	10.9	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	39.7	—	15.7	—	11.1	—	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	—	41.5	—	16.9	—	11.6	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	39.7	41.5	15.7	16.9	11.1	11.6	ns
tpd	Delay	Filter	183.1	186.2	73.5	75.7	47.9	50.2	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
offset	25kHz	auto	19	14	12	µs
offset	2MHz	auto	7	4	4	µs
frequency settling time	25kHz	auto	19	14	12	µs
frequency settling time	2MHz	auto	14	14	14	µs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical).

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time1	Width, 1 cell	PDLY mode:(any)edge detect, edge detect output	272.4	128.8	97.5	ns
time1	Width, 2 cell	PDLY mode:(any)edge detect, edge detect output	582.7	272.6	205.1	ns
time1	Width, 3 cell	PDLY mode:(any)edge detect, edge detect output	893.4	416.6	312.9	ns
time1	Width, 4 cell	PDLY mode:(any)edge detect, edge detect output	1203.4	560.6	420.9	ns
time2	Delay, 1 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time2	Delay, 2 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time2	Delay, 3 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time2	Delay, 4 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time1	Delay, 1 cell	PDLY mode: both edge delay (shared macrocell inputs)	354	161.5	120.1	ns
time1	Delay, 2 cell	PDLY mode: both edge delay (shared macrocell inputs)	664.2	305.2	227.8	ns
time1	Delay, 3 cell	PDLY mode: both edge delay (shared macrocell inputs)	974.9	449.1	335.7	ns
time1	Delay, 4 cell	PDLY mode: both edge delay (shared macrocell inputs)	1284.8	593.1	443.6	ns
time1	Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	63.6	32.4	22.9	ns
time1	Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	61.3	31.1	22.5	ns
time1	Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	62.2	31.6	22.7	ns

5.9 Typical Deglitch Filter Pulse Width Performance

Table 5. Typical Deglitch Filter Pulse Width Performance at T = 25 °C.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

5.10 Power Switch Electrical Characteristics (each P-FET)

Table 6. Power Switch Electrical Characteristics, T_A = -40 °C to +85 °C (with typical values at T_A = +25 °C), V_{DD} = 5.5 V, unless otherwise specified

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	T_A = +25 °C, V_{GS} = -5.5 V, I_D = -100 mA (see Note 1)	--	44	50	mΩ
		T_A = +25 °C, V_{GS} = -3.3 V, I_D = -100 mA (see Note 1)	--	58	65	
		T_A = +25 °C, V_{GS} = -1.71 V, I_D = -100 mA (see Note 1)	--	110	119	
		T_A = +85 °C, V_{GS} = -5.5 V, I_D = -100 mA (see Note 1)	--	51	58	
		T_A = +85 °C, V_{GS} = -3.3 V, I_D = -100 mA (see Note 1)	--	69	77	
		T_A = +85 °C, V_{GS} = -1.71 V, I_D = -100 mA (see Note 1)	--	129	138	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -1 mA	-0.48	-0.61	-0.72	V
I_{DSS}	Zero Gate Voltage Drain Current	T_A = +25 °C, V_{DS} = -4.0 V, V_{GS} = 0 V (see Note 2)	--	--	0.4	µA
		T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = 0 V	--	--	1.0	
		T_A = +85 °C, V_{DS} = -5.5 V, V_{GS} = 0 V	--	--	3.4	
I_{GSS}	Gate-Body Leakage	T_A = +25 °C, V_{GS} = ±5.5 V	--	±5	±100	nA
		T_A = +85 °C, V_{GS} = ±5.5 V	--	±400	±2000	
G_m	Forward Transconductance	V_{DS} = -5.5 V, V_{GS} = -1.8 V, I_D = -2 A (see Note 1)	4.5	5.4	--	S
Dynamic						
R_G	Internal Gate Resistance		--	200	--	Ω
C_{iss}	Input Capacitance	T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = 0 V, f = 1.0 MHz (see Note 3)	--	207	--	pF
C_{oss}	Output Capacitance		--	122	--	
C_{rss}	Reverse Transfer Capacitance		--	57	--	
Q_g	Total Gate Charge	T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = -5.5 V, I_D = -2 A (see Note 1)	--	1.45	1.55	nC
Q_{gs}	Gate-to-Source Charge		--	0.24	--	
Q_{gd}	Gate-to-Drain Charge		--	0.24	--	
t_{on}	Turn-On Time	T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = 0 to -5.5 V, ID = -1 A, Internal Drive	--	63	--	ns
t_{off}	Turn-Off Delay Time		--	287	--	ns
Drain-Source Body Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current	T_A = +25 °C, single channel operation	--	--	-2	A
V_{DSF}	Diode Forward Voltage	V_{GS} = 0 V, I_S = 100 mA (see Note 1)	0.63	0.75	0.87	V

Note 1: Pulse test: ƒ = 100 Hz, Duty cycle < 2 %.
Note 2: Measured to be less than 0.4 µA during production test.
Note 3: R_G influence has been excluded.

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external Pin 10

6.5 Combinational Logic Look Up Tables (LUTs – 4 total)

- Two 2-bit Lookup Tables
- Two 3-bit Lookup Tables

6.6 Combination Function Macrocells (7 total)

- Two Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Programmable Delay/ Deglitch Filter
  - 125 ns/250 ns/375 ns/500 ns @ 3.3 V
  - Includes Edge Detection function

6.7 Delays/Counters (3 total)

- Three 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1-8 stage selectable outputs.

6.9 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider (8): selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.10 Power On Reset (POR)

6.11 Dual P-FET Power Switch

- Power Switch IDS: 2.0 A
- V_{IN}: 1.71 V to 5.5 V
- Low RDSON
  - 44 mΩ @ 5.5 V
  - 58 mΩ @ 3.3 V
  - 110 mΩ @ 1.71 V

7.0 I/O Pins

The SLG46127 has a total of 6 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference). Refer to Section *2.0 Pin Description* for pin definitions.

Normal Mode pin definitions are as follows and Programming Mode pin definitions are as follows according to section *2.1 Functional Pin Description*.

Each of the six user defined I/O pins on the SLG46127 can serve as both digital input and digital output. But Pin 13 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input. Pins 1, 2 and 14 can also be configured to serve as analog inputs to the on-chip comparators and Vref output. PIN10 can be used as Vref output.

7.2 Output Modes

Pins 1, 2, 10, 11 and 14 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 13, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.5 PIN 1 Register Settings

Table 7. PIN 1 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 1 Mode Control	reg <392:390>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 1 Pull Up/Down Resistor Value Selection	reg <394:393>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 1 Pull Up/Down Resistor Selection	reg <395>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 1 Driver Strength Selection	reg <396>	0: 1X 1: 2X

7.5.1 PIN 2 Register Settings

Table 8. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control (sig_PIN2_oe=0)	reg <398:397>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input
PIN 2 Mode Control (sig_PIN2_oe =1)	reg <400:399>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 2 Pull Up/Down Resistor Value Selection	reg <402:401>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 2 Pull Up/Down Resistor Selection	reg <403>	0: Pull Down Resistor 1: Pull Up Resistor

7.5.2 PIN 10 Register Settings

Table 9. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control (sig_PIN10_oe =0)	reg <419:418>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog Input / Output
PIN 10 Mode Control (sig_PIN10_oe =1)	reg <421:420>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 10 Pull Up/Down Resistor Value Selection	reg <423:422>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <424>	0: Pull Down Resistor 1: Pull Up Resistor

7.5.3 PIN 11 Register Settings

Table 10. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Mode Control	reg <427:425>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 11 Pull Up/Down Resistor Value Selection	reg <429:428>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 11 Pull Up/Down Resistor Selection	reg <430>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Driver Strength Selection	reg <431>	0: 1X 1: 2X

7.5.4 PIN 13 Register Settings

Table 11. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Mode Control	reg <380:379>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 13 Pull Down Resistor Value Selection	reg <382:381>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.5.5 PIN 14 Register Settings

Table 12. PIN 14 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 14 Mode Control	reg <385:383>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 14 Pull Up/Down Resistor Value Selection	reg <387:386>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 14 Pull Up/Down Resistor Selection	reg <388>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 14 Driver Strength Selection	reg <389>	0: 1X 1: 2X

7.6 GPI IO Structure

7.6.1 GPI IO Structure (for Pin 13)

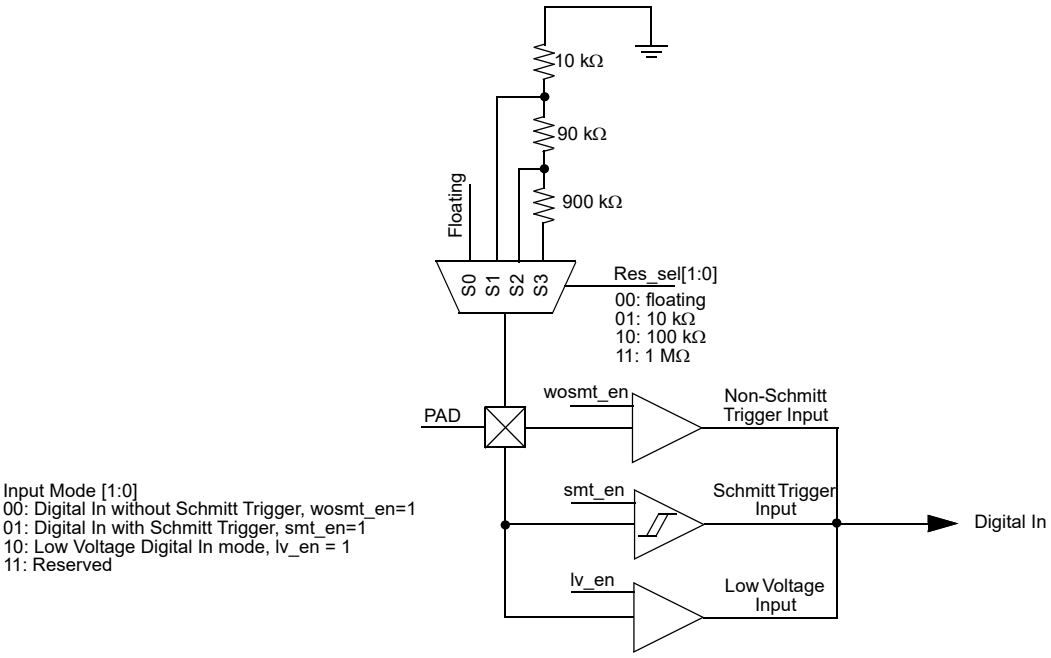


Figure 2. PIN 13 GPI IO Structure Diagram

7.7 Matrix OE IO Structure

7.7.1 Matrix OE IO Structure (for Pin 2, 10)

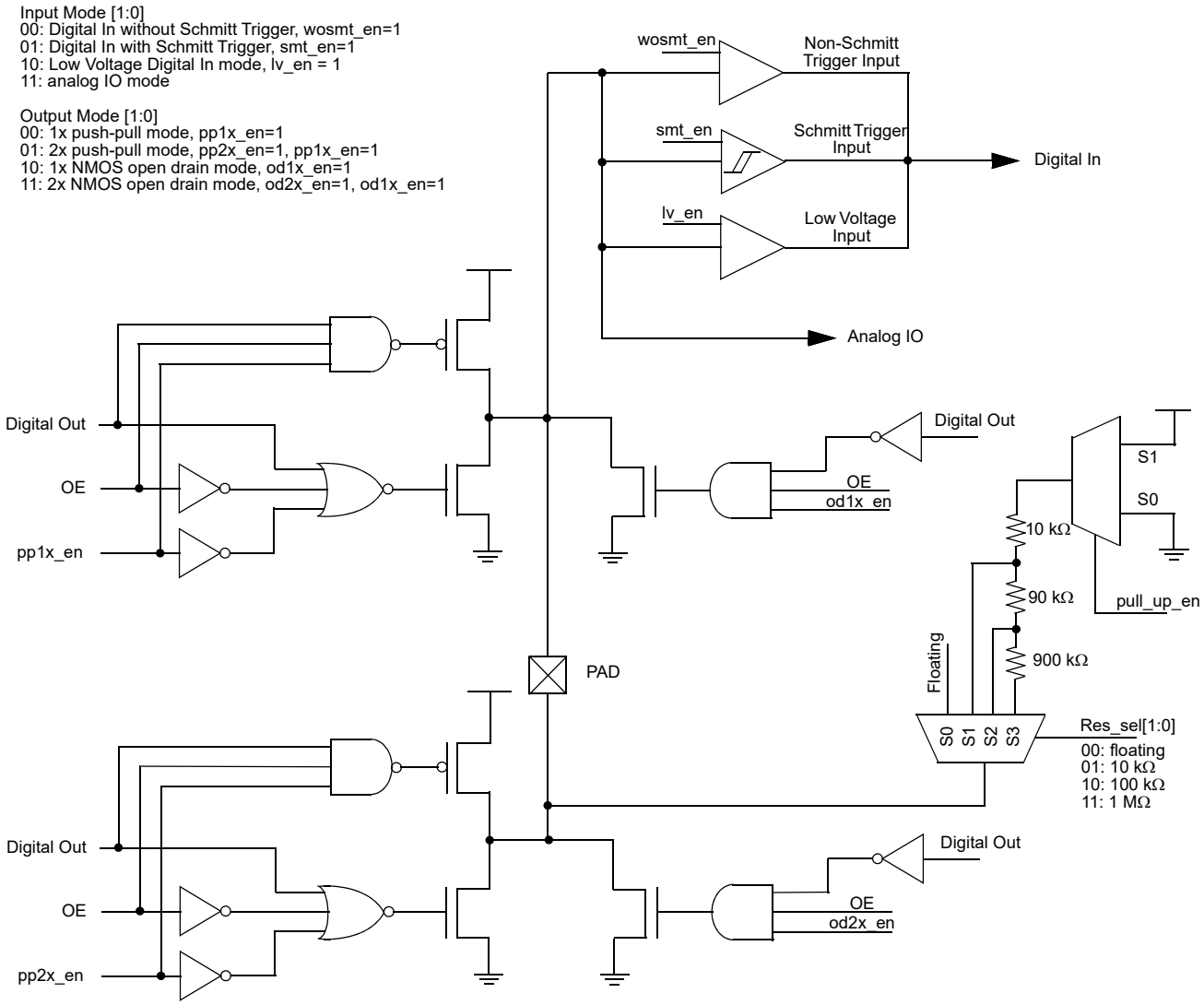


Figure 3. Matrix OE IO Structure Diagram

7.8 Register OE IO Structure

7.8.1 Register OE IO Structure (for Pins 1, 11, 14)

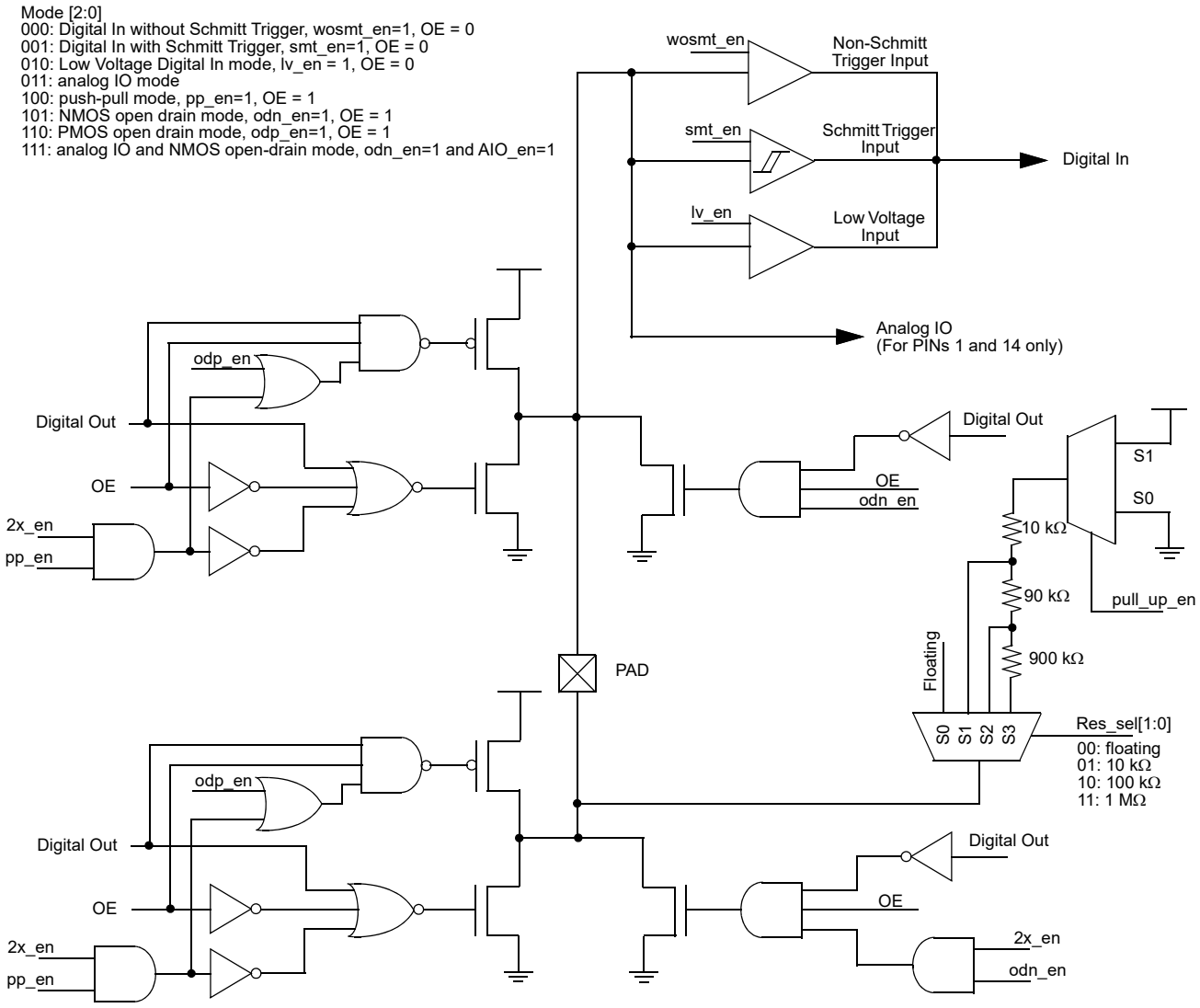


Figure 4. Register OE IO Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46127 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46127 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 512 register bits within the SLG46127 are programmed a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 44 outputs. Each of the 32 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, analog comparators, other digital resources and V_{DD} and V_{SS}. The input to a digital macrocell uses a 5-bit register to select one of these 32 input lines.

For a complete list of the SLG46127’s register table, see Section *18.0 Appendix A - SLG46127 Register Definition*.

Matrix Input Signal Functions	N
VSS	0
Pin 13 Digital In	1
Pin 14 Digital In	2
Pin 1 Digital In	3
⋮	⋮
PIN11 Digital In	30
V_{DD}	31

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	43
Registers	reg <4:0>	reg <9:5>	reg <14:10>	⋯	reg <219:215>
Function	PIN14 Digital Output Source	PIN1Digital Output Source	PIN2 Digital Output Source	⋯	PIN11 Digital Output Source

Figure 5. Connection Matrix

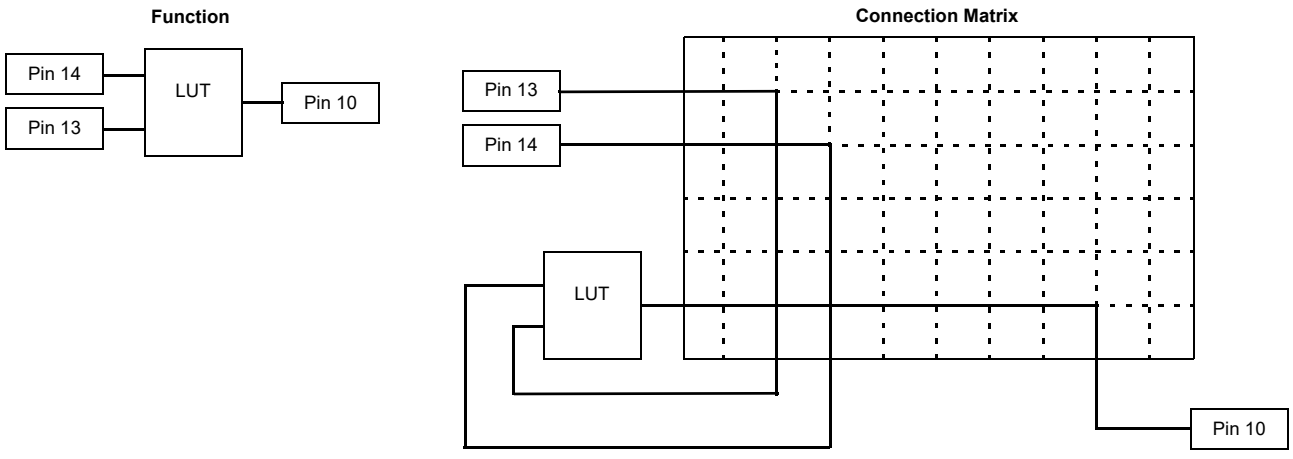


Figure 6. Connection Matrix Example

8.1 Matrix Input Table

Table 13. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
0	GND	0	0	0	0	0
1	pin13 digital Input	0	0	0	0	1
2	pin14 digital Input	0	0	0	1	0
3	pin1 digital Input	0	0	0	1	1
4	pin2 digital Input	0	0	1	0	0
5	LUT2_0 output (DFF/LATCH_0 output)	0	0	1	0	1
6	LUT2_1 output (DFF/LATCH_1 output)	0	0	1	1	0
7	LUT2_2 output	0	0	1	1	1
8	LUT2_3 output	0	1	0	0	0
9	LUT3_0 output (DFF/LATCH_2 output with nRST or nSET)	0	1	0	0	1
10	LUT3_1 output (DFF/LATCH_3 output with nRST or nSET)	0	1	0	1	0
11	LUT3_2 output	0	1	0	1	1
12	LUT3_3 output	0	1	1	0	0
13	LUT3_4 output (pipe delay ouput0)	0	1	1	0	1
14	pipe delay ouput1	0	1	1	1	0
15	LUT4_0 output (CNT_DLY2 output (8 bit w/ ext CK, reset))	0	1	1	1	1
16	CNT_DLY0 output (8 bit w/ ext CK (shared bottom delay/CNT), reset)	1	0	0	0	0
17	CNT_DLY1 output (8 bit w/ ext CK (from dedicated matrix output), reset)	1	0	0	0	1
18	CNT_DLY3 (8 bit) output	1	0	0	1	0
19	ACMP_0 output	1	0	0	1	1
20	ACMP_1 output	1	0	1	0	0
21	Edge detect output	1	0	1	0	1
22	Programmable delay with edge detector output (Deglitch filter output)	1	0	1	1	0
23	Internal oscillator output1 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	1	1
24	Internal oscillator output2 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	1	0	0	0
25	Bandgap OK signal	1	1	0	0	1
26	POR output to matrix	1	1	0	1	0
27	Power Switch ON0, pin15 digital Input	1	1	0	1	1
28	Power Switch ON1, pin16 digital Input	1	1	1	0	0
29	pin10 digital Input	1	1	1	0	1
30	pin11 digital Input	1	1	1	1	0
31	V_{DD}	1	1	1	1	1

8.2 Matrix Output Table

Table 14. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <4:0>	Pin 14 digital out source	0
reg <9:5>	Pin 1 digital out source	1
reg <14:10>	Pin 2 digital out source	2
reg <19:15>	Pin 2 output enable	3
reg <24:20>	in0 of LUT2_0 (Clock Input of DFF0)	4
reg <29:25>	in1 of LUT2_0 (Data Input of DFF0)	5
reg <34:30>	in0 of LUT2_1 (Clock Input of DFF1)	6
reg <39:35>	in1 of LUT2_1 (Data Input of DFF1)	7
reg <44:40>	in0 of LUT2_2	8
reg <49:45>	in1 of LUT2_2	9
reg <54:50>	in0 of LUT2_3	10
reg <59:55>	in1 of LUT2_3	11
reg <64:60>	in0 of LUT3_0 (Clock Input of DFF2 with nRST/nSET)	12
reg <69:65>	in1 of LUT3_0 (Data input of DFF2 with nRST/nSET)	13
reg <74:70>	in2 of LUT3_0 (nRST or nSET of DFF2 with nRST/nSET)	14
reg <79:75>	in0 of LUT3_1 (Clock Input of DFF3 with nRST/nSET)	15
reg <84:80>	in1 of LUT3_1 (Data input of DFF3 with nRST/nSET)	16
reg <89:85>	in2 of LUT3_1 (nRST or nSET of DFF3 with nRST/nSET)	17
reg <94:90>	in0 of LUT3_2	18
reg <99:95>	in1 of LUT3_2	19
reg <104:100>	in2 of LUT3_2	20
reg <109:105>	in0 of LUT3_3	21
reg <114:110>	in1 of LUT3_3	22
reg <119:115>	in2 of LUT3_3	23
reg <124:120>	in0 of LUT3_4 (Input of pipe delay)	24
reg <129:125>	in1 of LUT3_4 (nRST of pipe delay)	25
reg <134:130>	in2 of LUT3_4 (Clock of pipe delay)	26
reg <139:135>	in0 of LUT4_0 (Input for Delay2 ext. clock or Counter2 external Clock)	27
reg <144:140>	in1 of LUT4_0 (Input for Delay2 or Counter2 reset input)	28
reg <149:145>	in2 of LUT4_0	29
reg <154:150>	in3 of LUT4_0	30
reg <159:155>	Input for Delay0 or Counter0 reset input	31
reg <164:160>	Input for Delay1 or Counter1 reset input	32
reg <169:165>	Input for Delay0/1 ext. clock or Counter1 external Clock	33
reg <174:170>	Input for Delay3 or Counter3 reset input	34
reg <179:175>	pdb for ACMP0	35
reg <184:180>	pdb for ACMP1	36
reg <189:185>	Input for programmable delay (deglitch filter input)	37

Table 14. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <194:190>	Power down for osc. (higher priority) (high = power down).	38
reg <199:195>	Pin15 digital out source and Input of Power Switch ON0	39
reg <204:200>	Pin16 digital out source and Input of Power Switch ON1	40
reg <209:205>	Pin 10 digital out source	41
reg <214:210>	Pin 10 output enable	42
reg <219:215>	Pin 11 digital out source	43

9.0 Combinatorial Logic

Combinatorial logic is supported via four Lookup Tables (LUTs) within the SLG46127. There are two 2-bit LUTs and two 3-bit LUTs. The device also includes six Combination Function Macrocells that can be used as LUTs. For more details, please see Section *10.0 Combination Function Macrocells*.

Inputs/Outputs for the four LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT

The two 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

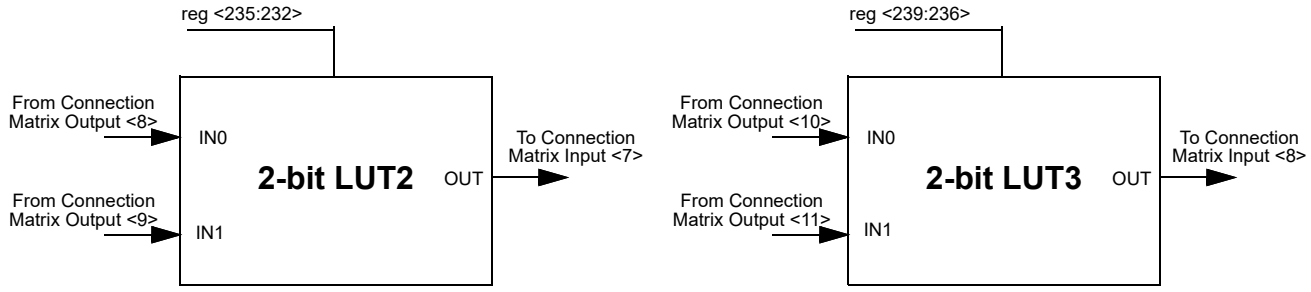


Figure 7. 2-bit LUTs

Table 15. 2-bit LUT2 Truth Table.

IN1	IN0	OUT
0	0	reg <232>
0	1	reg <233>
1	0	reg <234>
1	1	reg <235>

Table 16. 2-bit LUT3 Truth Table.

IN1	IN0	OUT
0	0	reg <236>
0	1	reg <237>
1	0	reg <238>
1	1	reg <239>

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT2 is defined by reg <235:232>

2-Bit LUT3 is defined by reg <239:236>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 17. 2-bit LUT2/LUT3 Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-Bit LUT

The two 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

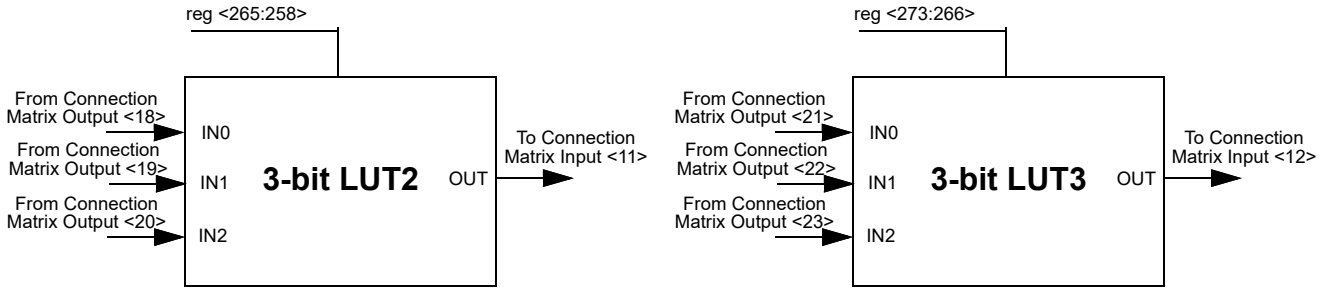


Figure 8. 3-bit LUTs

Table 18. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <258>
0	0	1	reg <259>
0	1	0	reg <260>
0	1	1	reg <261>
1	0	0	reg <262>
1	0	1	reg <263>
1	1	0	reg <264>
1	1	1	reg <265>

Table 19. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <266>
0	0	1	reg <267>
0	1	0	reg <268>
0	1	1	reg <269>
1	0	0	reg <270>
1	0	1	reg <271>
1	1	0	reg <272>
1	1	1	reg <273>

Each 3-bit LUT uses a 8-bit register signal to define their output functions;

3-Bit LUT2 is defined by reg <265:258>

3-Bit LUT3 is defined by reg <273:266>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 3-bit LUT logic cells.

Table 20. 3-bit LUT2/LUT3 Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.0 Combination Function Macrocells

The SLG46127 has six combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells;

- Two macrocells that can serve as either 2-bit LUTs or as D Flip-Flops.
- Two macrocells that can serve as either 3-bit LUTs or as D Flip-Flops.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- One macrocells that can serve as either 4-bit LUTs or as 8-Bit Counter / Delays

Inputs/Outputs for the six combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

When used as a D Flip-Flop / Latch, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state, and all have the option to connect both the Q and Q Bar outputs to the connection matrix. The macrocells DFF2, DFF3 have an additional input from the matrix that can serve as a nSET or nRST function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 0, then Q = D

10.1 2-Bit LUT or D Flip-Flop Macrocells

There are two macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

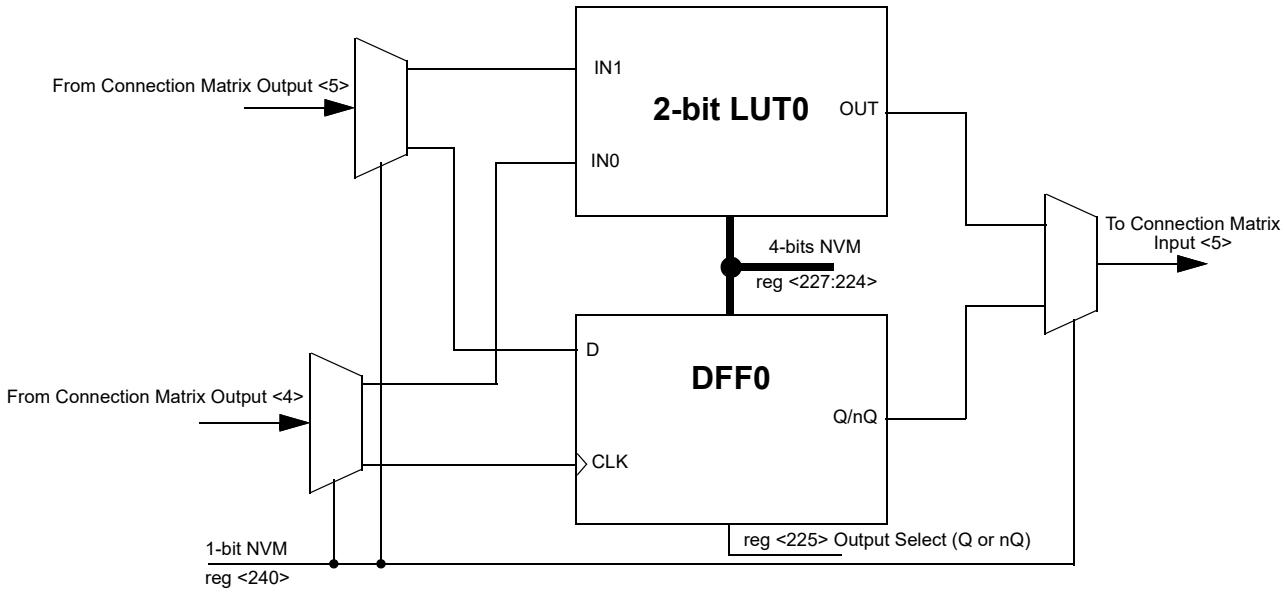


Figure 9. 2-bit LUT0 or DFF0

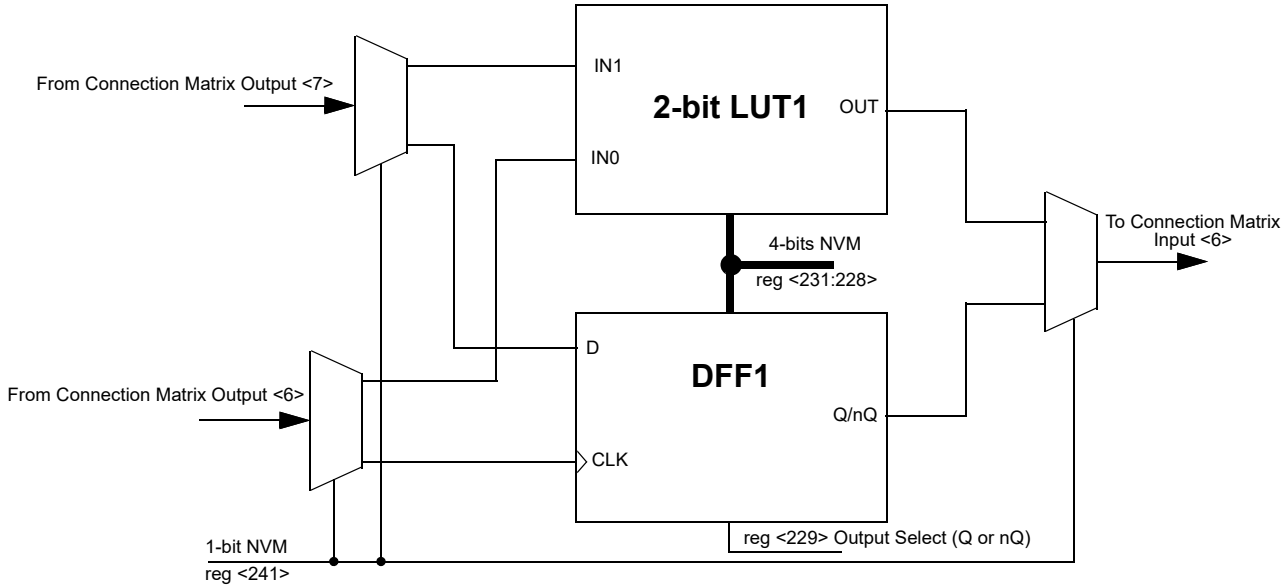


Figure 10. 2-bit LUT1 or DFF1

10.1.1 2-Bit LUT or D Flip-Flop Macrocells Used as 2-Bit LUTs

Table 21. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <224>
0	1	reg <225>
1	0	reg <226>
1	1	reg <227>

Table 22. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <228>
0	1	reg <229>
1	0	reg <230>
1	1	reg <231>

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg <227:224>

2-Bit LUT1 is defined by reg <231:228>

10.1.2 2-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 23. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or Latch select	reg <224>	0: DFF function 1: Latch function
DFF0 output select	reg <225>	0: Q output 1: nQ output
DFF0 initial polarity select	reg <226>	0: Low 1: High
LUT2_0 data	reg <235:232>	LUT2_0 data
LUT2_0 or DFF0 select	reg <240>	0: LUT2_0 1: DFF0

Table 24. DFF1Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or Latch select	reg <228>	0: DFF function 1: Latch function
DFF1 output select	reg <229>	0: Q output 1: nQ output
DFF1 initial polarity select	reg <230>	0: Low 1: High
LUT2_1 data	reg <239:236>	LUT2_1 data
LUT2_1 or DFF1 select	reg <241>	0: LUT2_1 1: DFF1

10.2 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

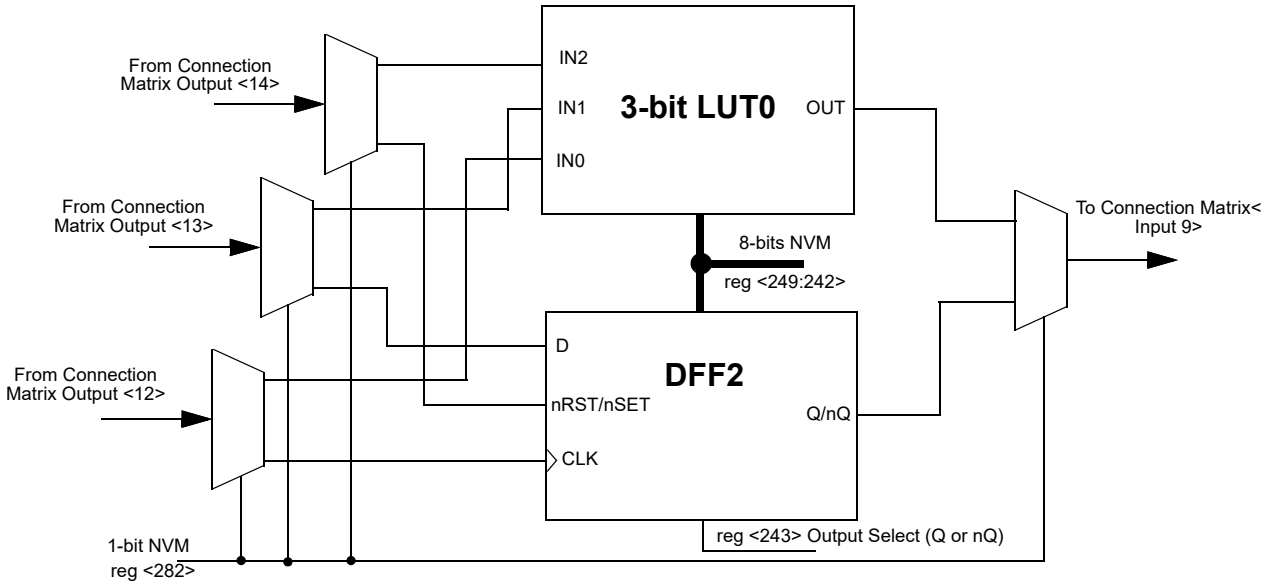


Figure 11. 3-bit LUT0 or DFF2

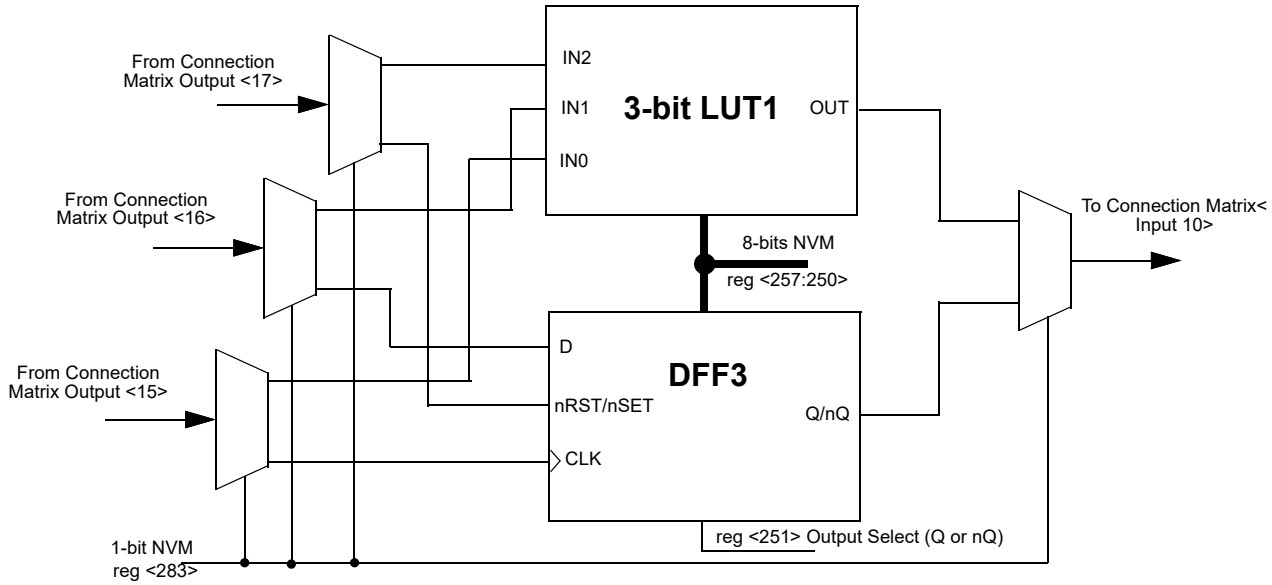


Figure 12. 3-bit LUT1 or DFF3

10.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 25. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <242>
0	0	1	reg <243>
0	1	0	reg <244>
0	1	1	reg <245>
1	0	0	reg <246>
1	0	1	reg <247>
1	1	0	reg <248>
1	1	1	reg <249>

Table 26. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <250>
0	0	1	reg <251>
0	1	0	reg <252>
0	1	1	reg <253>
1	0	0	reg <254>
1	0	1	reg <255>
1	1	0	reg <256>
1	1	1	reg <257>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT2 is defined by reg <249:242>

3-Bit LUT3 is defined by reg <257:250>

10.2.2 3-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 27. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or Latch select	reg <242>	0: DFF function 1: Latch function
DFF2 output select	reg <243>	0: Q output 1: nQ output
DFF2 initial polarity select	reg <244>	0: Low 1: High
DFF2 nRST/nSET Select	reg <245>	1: nSET from matrix out 0: nRST from matrix out
LUT3_0 data	reg <265:258>	LUT3_0 data
LUT3_0 or DFF2 select	reg <282>	0: LUT3_0 1: DFF2

Table 28. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or Latch Select	reg <250>	0: DFF function 1: Latch function
DFF3 Output Select	reg <251>	0: Q output 1: nQ output
DFF3 nRST/nSET Select	reg <252>	1: nSETfrom matrix out 0: nRST from matrix out
DFF3 initial polarity select	reg <253>	0: Low 1: High
LUT3_1 data	reg <273:266>	LUT3_1 data
LUT3_1 or DFF3 select	reg <283>	0: LUT3_1 1: DFF3

10.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as an 8-stage pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (nRST). The pipe delay cell is built from D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (OUT2) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 to 8 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 3-input mux that is controlled by reg <666:663> for OUT0 and reg <670:667> for OUT1. The 3-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46127 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46127). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

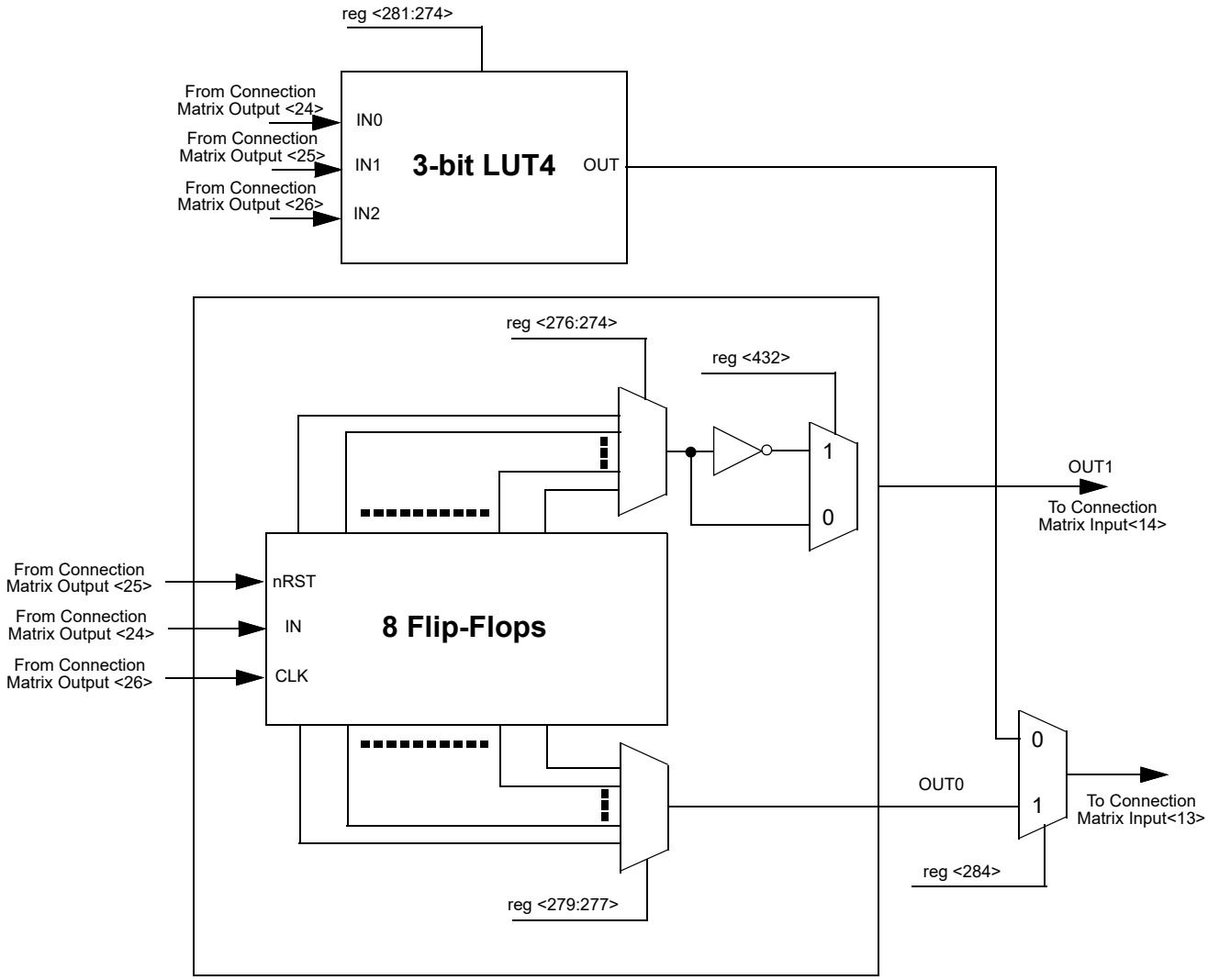


Figure 13. 3-bit LUT4 or Pipe Delay

10.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 29. 3-bit LUT4 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <274>
0	0	1	reg <275>
0	1	0	reg <276>
0	1	1	reg <277>
1	0	0	reg <278>
1	0	1	reg <279>
1	1	0	reg <280>
1	1	1	reg <281>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT4 is defined by reg <281:274>

10.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 30. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	reg <276:274>	data (pipe number)
OUT1 select	reg <279:277>	data (pipe number)
LUT3_4 or pipe delay output select	reg <284>	0: LUT3_4 1: pipe delay

10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells

There is one macrocell that can serve as either a 4-bit LUT or as a Counter / Delay. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_in/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

Note: Counters initialize with counter data=0 after POR.

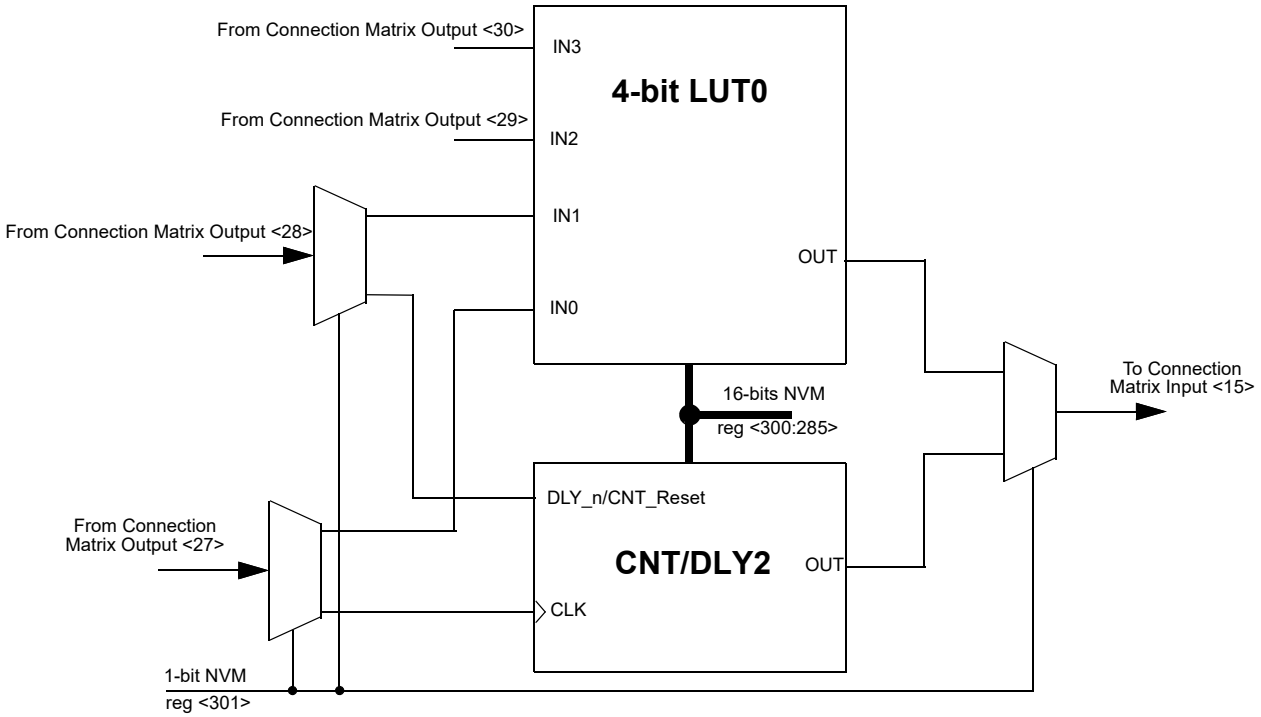


Figure 14. 4-bit LUT0 or CNT/DLY2

10.4.1 4-Bit LUT or 8-Bit Counter / Delay Macrocell Used as 4-Bit LUTs

Table 31. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <285>
0	0	0	1	reg <286>
0	0	1	0	reg <287>
0	0	1	1	reg <288>
0	1	0	0	reg <289>
0	1	0	1	reg <290>
0	1	1	0	reg <291>
0	1	1	1	reg <292>
1	0	0	0	reg <293>
1	0	0	1	reg <294>
1	0	1	0	reg <295>
1	0	1	1	reg <296>
1	1	0	0	reg <297>
1	1	0	1	reg <298>
1	1	1	0	reg <299>
1	1	1	1	reg <300>

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg <300:285>

10.4.2 4-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

Table 32. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay2 Mode Selection	reg <285>	0: Delay Mode 1: Counter Mode
Counter/delay2 Clock Source Select	reg <288:286>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter1 Overflow
Counter/delay2 Control Data	reg <296:289>	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay2 Mode Select or asynchronous counter reset	reg <298:297>	00: Delay on both falling and rising edgeless delay & counter reset) 01: Delay on falling edge only (for delay & counter reset Delay) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode
LUT4_0 or Counter2 select	reg <301>	0: LUT4_0 1: Counter2

11.0 Analog Comparators (ACMP)

There are two Analog Comparator (ACMP) macrocells in the SLG46127. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0_pdb and ACMP1_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by way of the external sources.

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low bandwidth signals are input into the analog comparator. And if input frequency > 200 kHz, the output will retain its previous value. Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV.

During powerup, the ACMP output will remain low, and then become valid 110 µs (max) after POR signal goes high, see *Figure 15.* .

Note: Regulator and Charge Pump set to automatic ON/OFF.

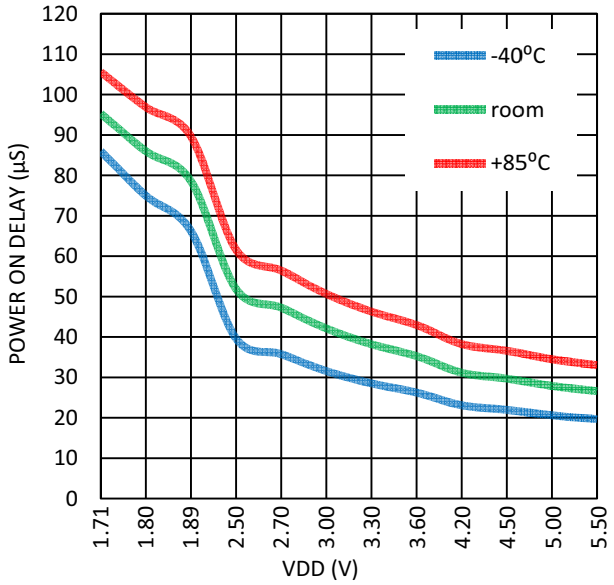


Figure 15. Maximum Power On Delay vs. V_{DD}.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 KΩ (typ.) resistors, see *Table 33*. For gain divider accuracy refer to *Table 34*. IN- voltage range: 0 - 1.2 V. Can use Vref selection V_{DD}/4 and V_{DD}/3 to maintain this input range.

Table 33. Gain Divider Input Resistance (typ).

Gain	1X	0.5X	0.33X	0.25X
Input Resistance	100M	1M	0.75M	1M

Table 34. Gain Divider Accuracy.

Gain	0.5X	0.33X	0.25X
Accuracy	±0.6 %	±0.9 %	±2.8 %

Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by the external reference/source. Internal Vref accuracy is optimized near 1000 mV selection.

Note: Power supply control options have influence on the ACMP operation.

Note: Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on Vref (even when the Force BandGap option is set as Disabled).

Analog comparators have the following configurable options:

- Hysteresis: Input signal hysteresis options are Disable, 25 mV, 50 mV, 200 mV.
- Low Bandwidth: Enable, Disable;
- IN+ Gain: 1X, 0.5X, 0.33X, 0.25X;
- IN+ source:
  - ACMP0 IN+ options are PIN 14, V_{DD};
  - ACMP1 IN+ options are PIN 2, ACMP0 IN+;
- IN- source:
  - ACMP0 IN- options are 24 internal reference sources (50 mV – 1200 mV) and $V_{DD}/3$, $V_{DD}/4$, PIN 1;
  - PWR UP=0 – ACMP is powered down; PWR UP=1 – ACMP is powered up.
  - All ACMPs can have a common negative input. This can be achieved by configuring ACMP0 PIN 1 analog I/O connection.

11.1 ACMP0 Block Diagram

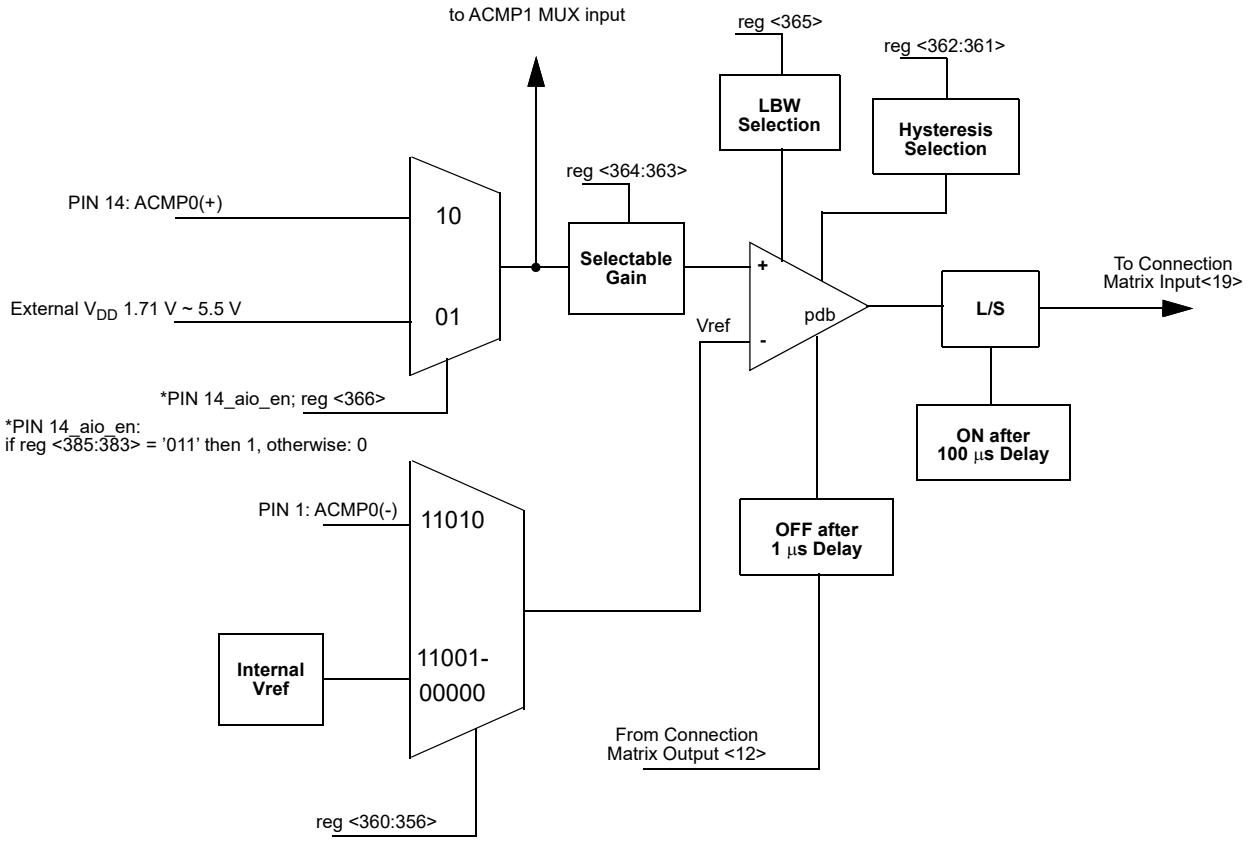


Figure 16. ACMP0 Block Diagram

11.2 ACMP0 Register Settings

Table 35. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 In Voltage Select	reg <360:356>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: EXT_VREF (PIN1)
ACMP0 Hysteresis Enable	reg <362:361>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 Positive Input Divider	reg <364:363>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg <365>	0: Off 1: On
ACMP0 positive input source select PIN 14 and V_{DD}	reg <366>	0: PIN 14 1: V_{DD}

11.3 ACMP1 Block Diagram

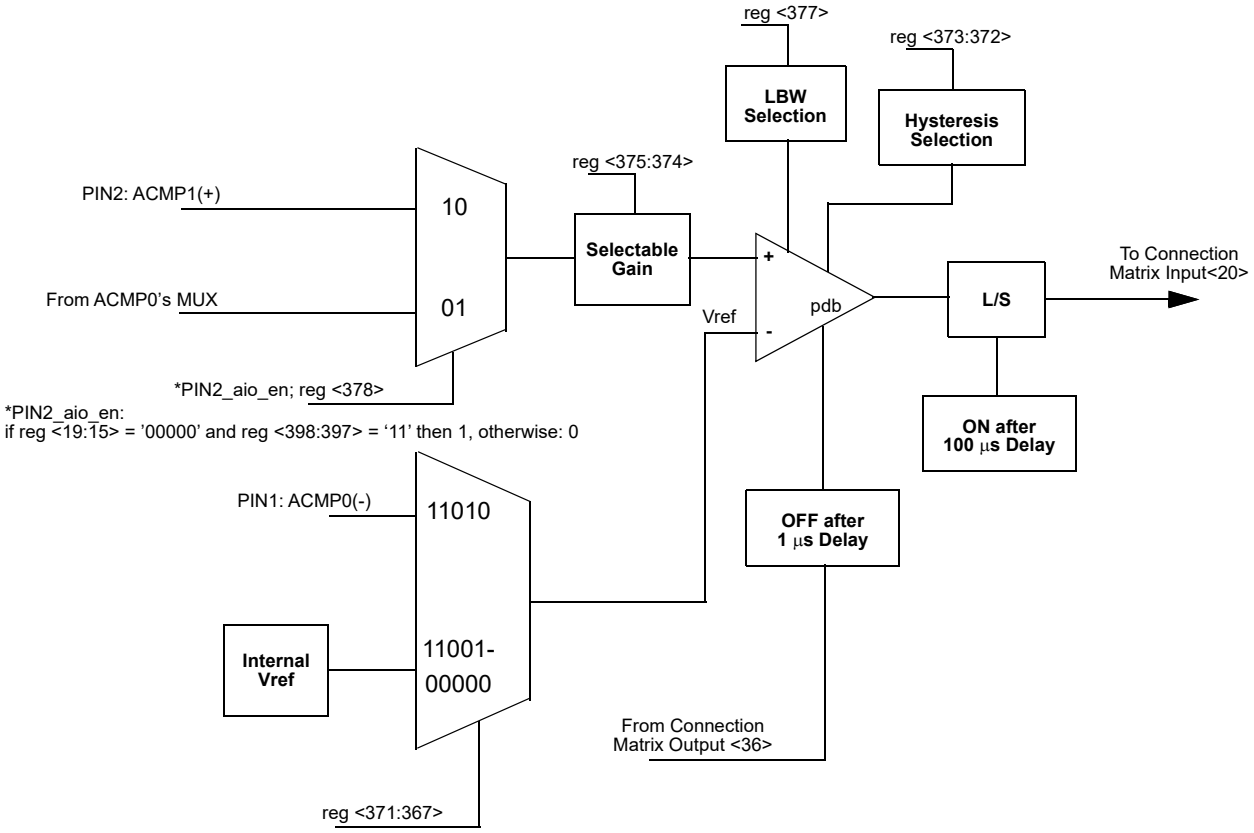


Figure 17. ACMP1 Block Diagram

11.4 ACMP1 Register Settings

Table 36. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 In Voltage Select	reg <371:367>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: EXT_VREF (PIN1)
ACMP1 Hysteresis Enable	reg <373:372>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 Positive Input Divider	reg <375:374>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg <377>	1: On 0: Off
ACMP1 positive input source select PIN14 and Pin2	reg <378>	0: Pin2 1: Pin14

11.5 Typical Performance Characteristics

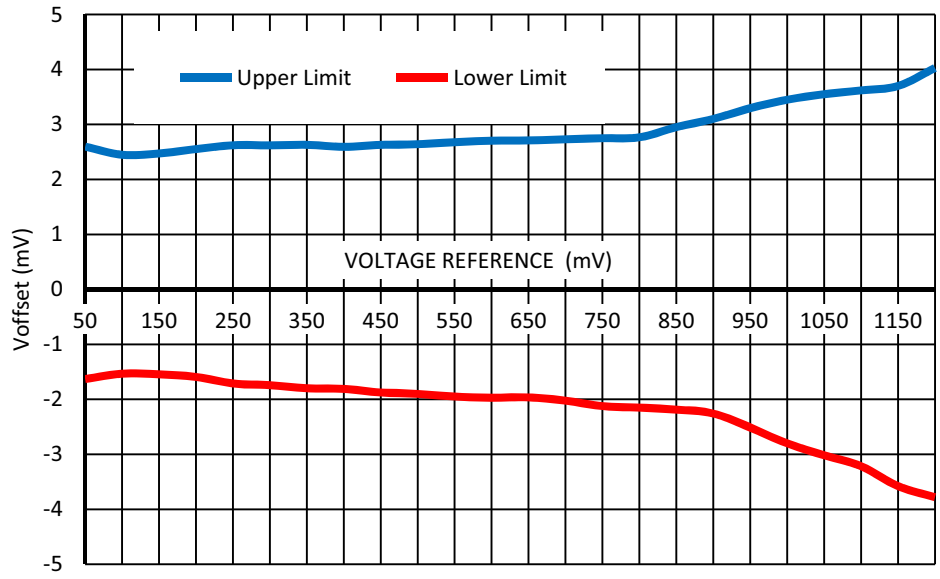


Figure 18. Typical Input Voltage Offset vs. Voltage Reference at room temperature, LBW Mode – Disable, Vhys=0 mV, V_{DD}=(1.7 – 5.5) V.

Note: when V_{DD} < 1.8 V voltage reference should not exceed 1100 mV.

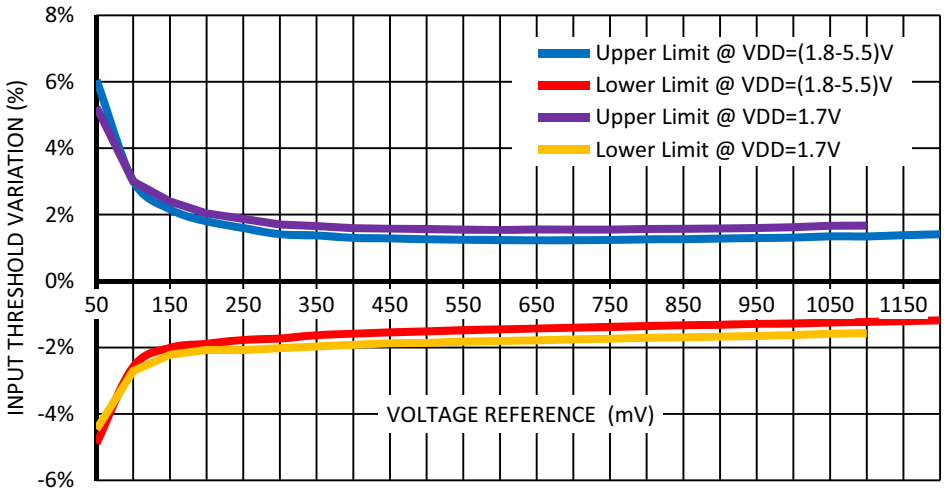


Figure 19. Typical Input Threshold Variation (including Vref variation, ACMP offset) vs. Voltage reference at room temperature, LBW Mode – Disable, Vhys=0 mV.

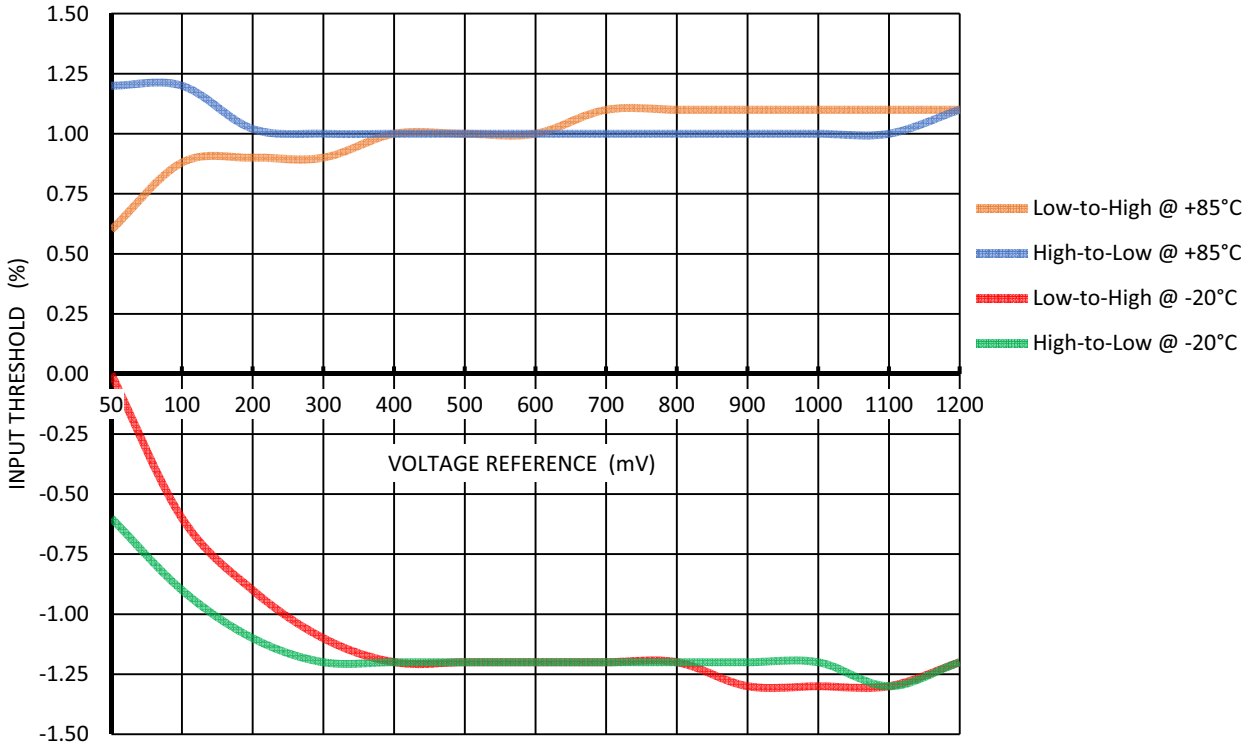


Figure 20. Input Threshold Ratio vs. Voltage Reference at V_{DD} = (1.71 - 5.5) V, Vhys = 0, Gain = 1

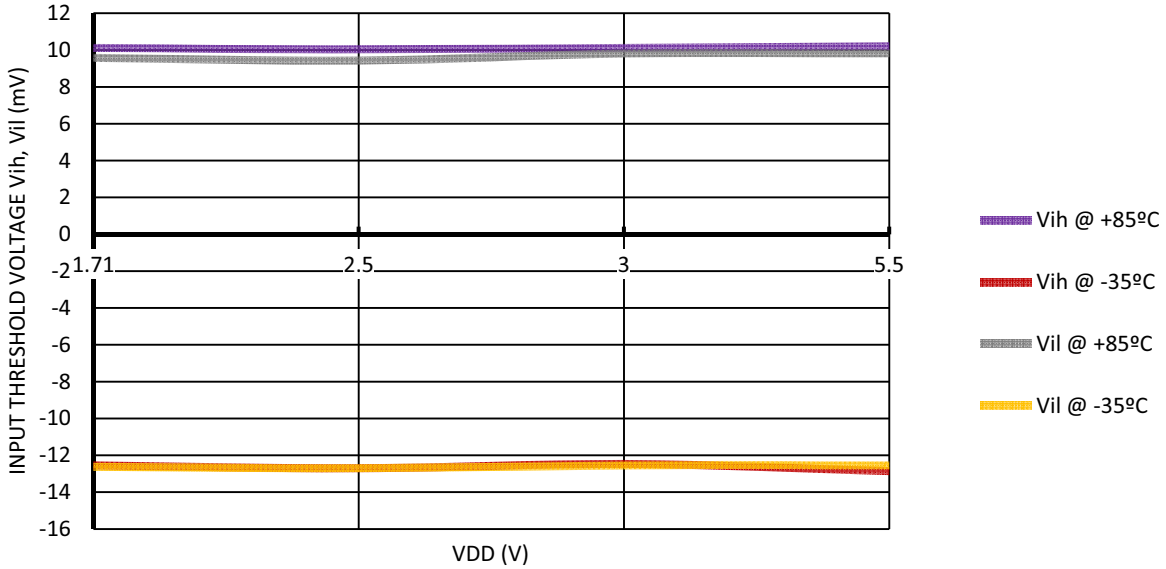


Figure 21. Input Threshold Voltage Vih, Vil vs. V_{DD} at Vref = 1000 mV, Gain = 1

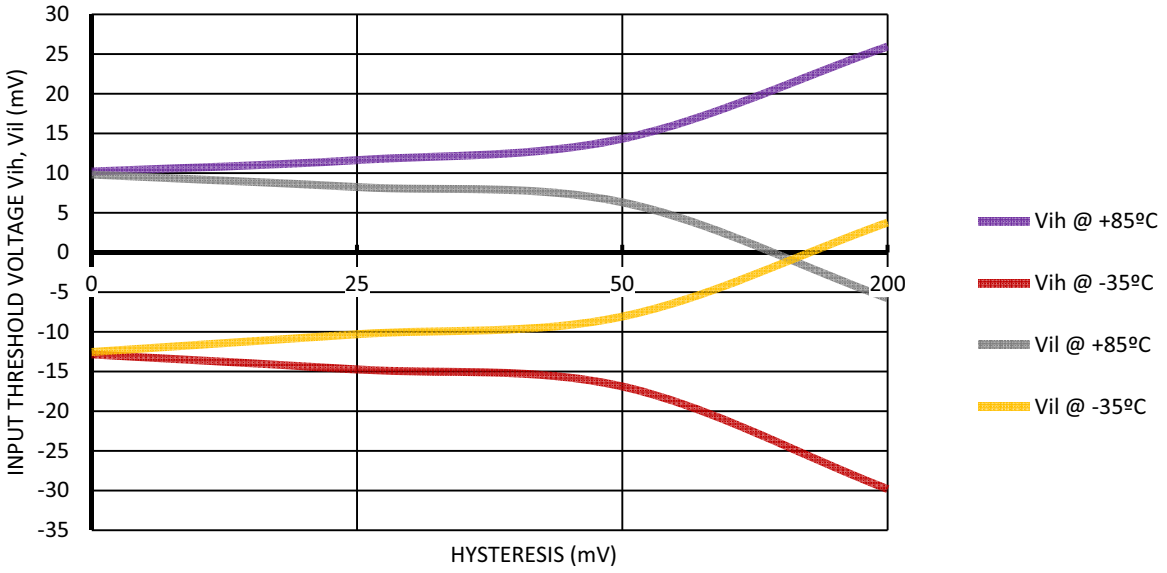


Figure 22. Input Threshold Voltage Vih, Vil vs. Hysteresis at V_{DD} = 5.5 V, Vref = 1000 mV. Gain = 1

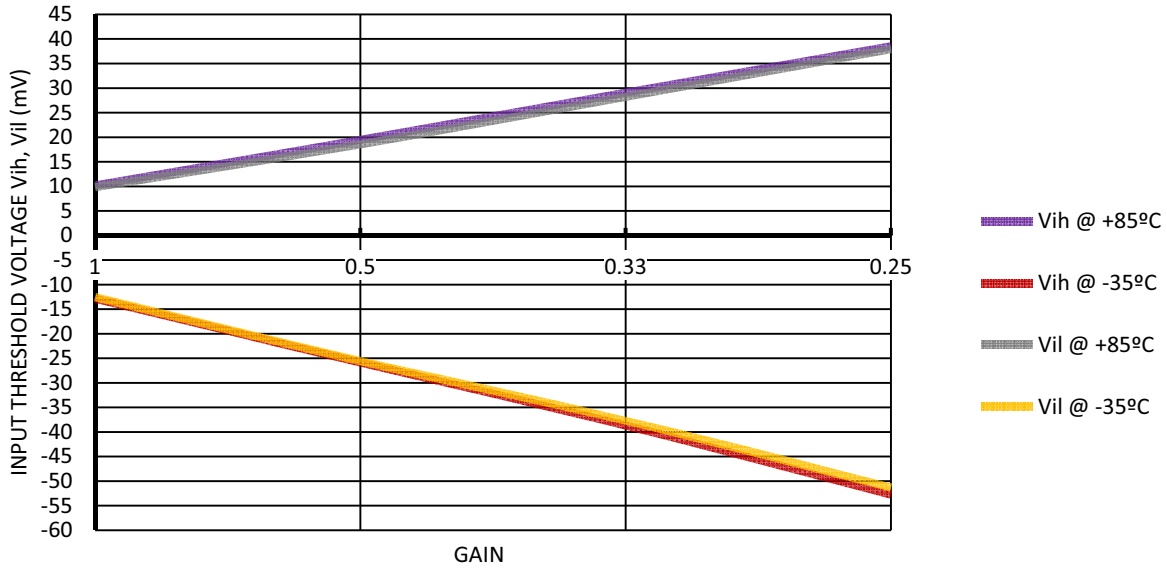


Figure 23. Input Threshold Voltage Vih, Vil vs. Gain at Hysteresis = 0, V_{DD} = 5.5 V, Vref = 1000 mV

Table 37. Built-in Hysteresis Tolerance.

Vhys (mV)	V_{DD}=(1.7-1.8) V						V_{DD}=(1.89-5.5) V					
	Vref = (50-500) mV		Vref = (550-1000) mV		Vref = (1050-1200) mV		Vref = (50-500) mV		Vref = (550-1000) mV		Vref = (1050-1200) mV	
	min	max	min	max	min	max	min	max	min	max	min	max
25	18.9	26.4	17.3	26.1	13.0	24.6	18.8	26.5	17.8	26.1	15.6	25.5
50	40.3	50.4	37.9	50.1	28.9	47.7	40.3	50.5	39.5	50.1	34.5	49.5
200	180.5	208.4	172.9	210.7	153.5	217.2	180.6	207.7	180.2	210.8	166.5	211.9

11.6 Timing Characteristics

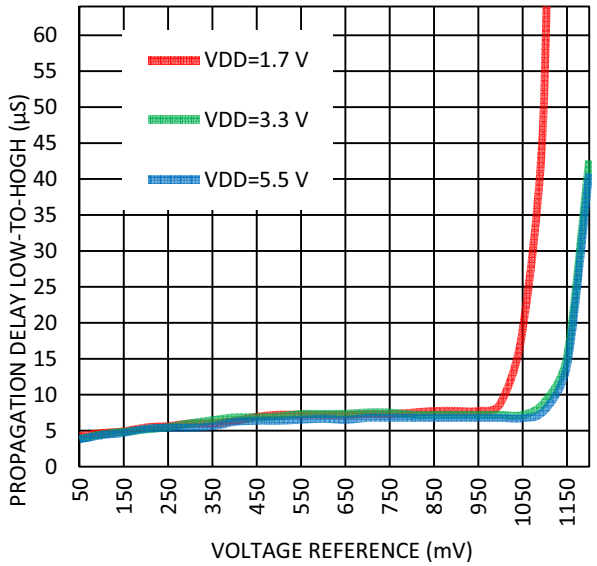


Figure 24. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, Vod = 2 mV.

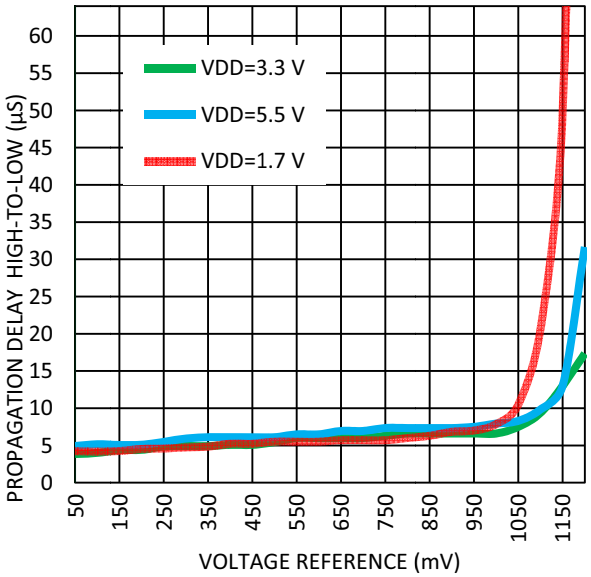


Figure 26. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, Vod = 2 mV.

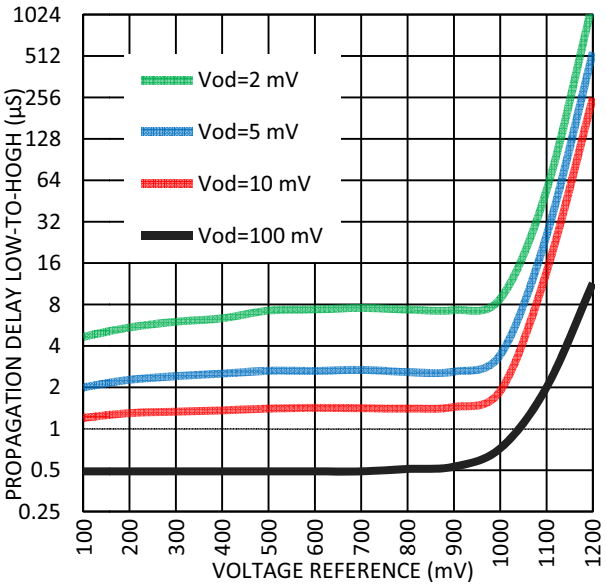


Figure 25. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, V_{DD}=(1.71 – 1.89) V.

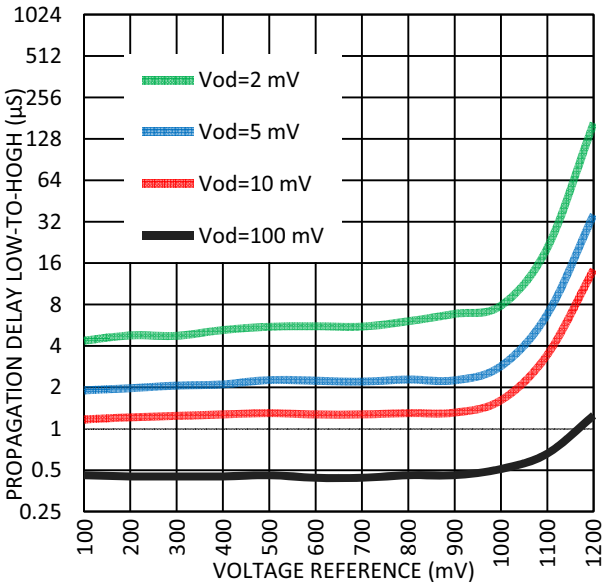


Figure 27. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, V_{DD}=(1.71 – 1.89) V.

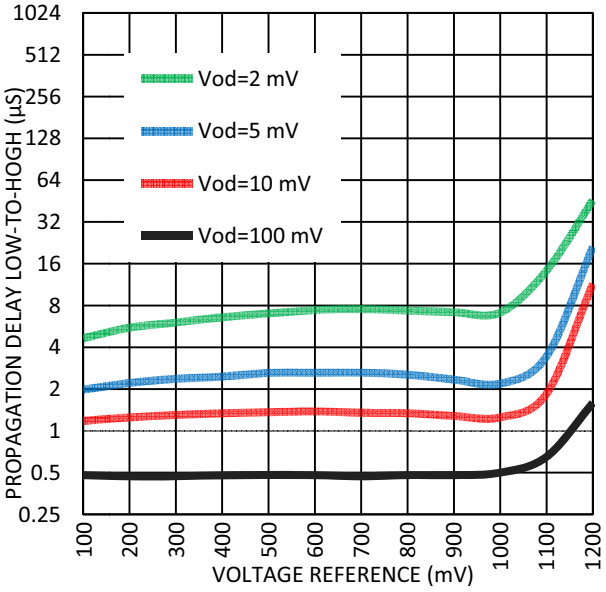


Figure 28. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, V_{DD} = (1.89 – 3.6) V.

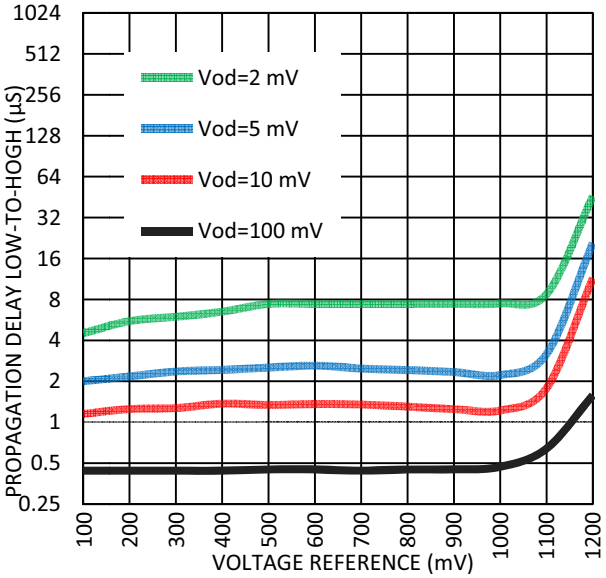


Figure 29. Maximum Propagation Delay Low-to-High vs. Voltage Reference at Room Temperature, V_{DD} = (3.6 – 5.5) V.

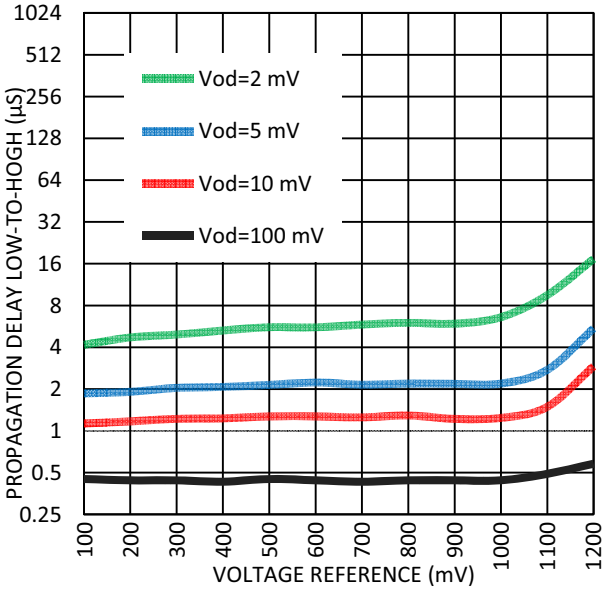


Figure 30. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, V_{DD} = (1.89 – 3.6) V.

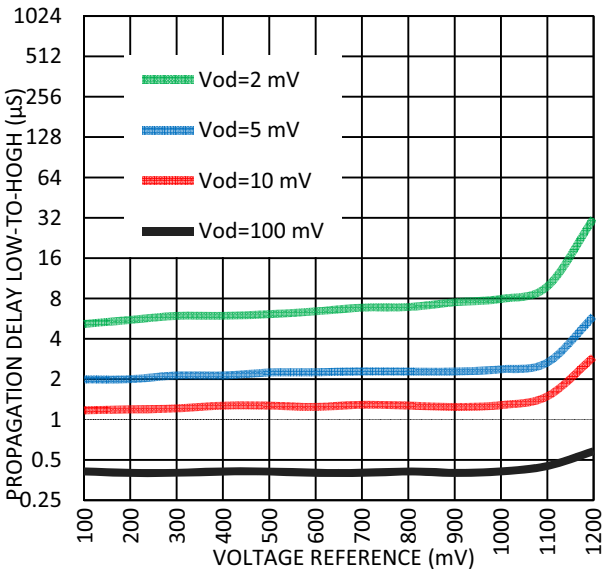


Figure 31. Maximum Propagation Delay High-to-Low vs. Voltage Reference at Room Temperature, V_{DD} = (3.6 – 5.5) V.

12.0 Counters/Delay Generators (CNT/DLY)

There are three configurable counters/delay generators in the SLG46127. The three counters/delay generators (CNT/DLY 0, 1, 3) are 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

Two of the counter/delay generator macrocells (CNT/DLY0 and CNT/DLY1) have two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. One of the counter/delay generator macrocells (CNT/DLY3) has one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

Note that there is also one Combination Function Macrocells that can implement either 4-bit LUTs or 8-bit counter / delays, For more information please see Section *10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells*.

Note: Counters initialize with counter data=0 after POR.

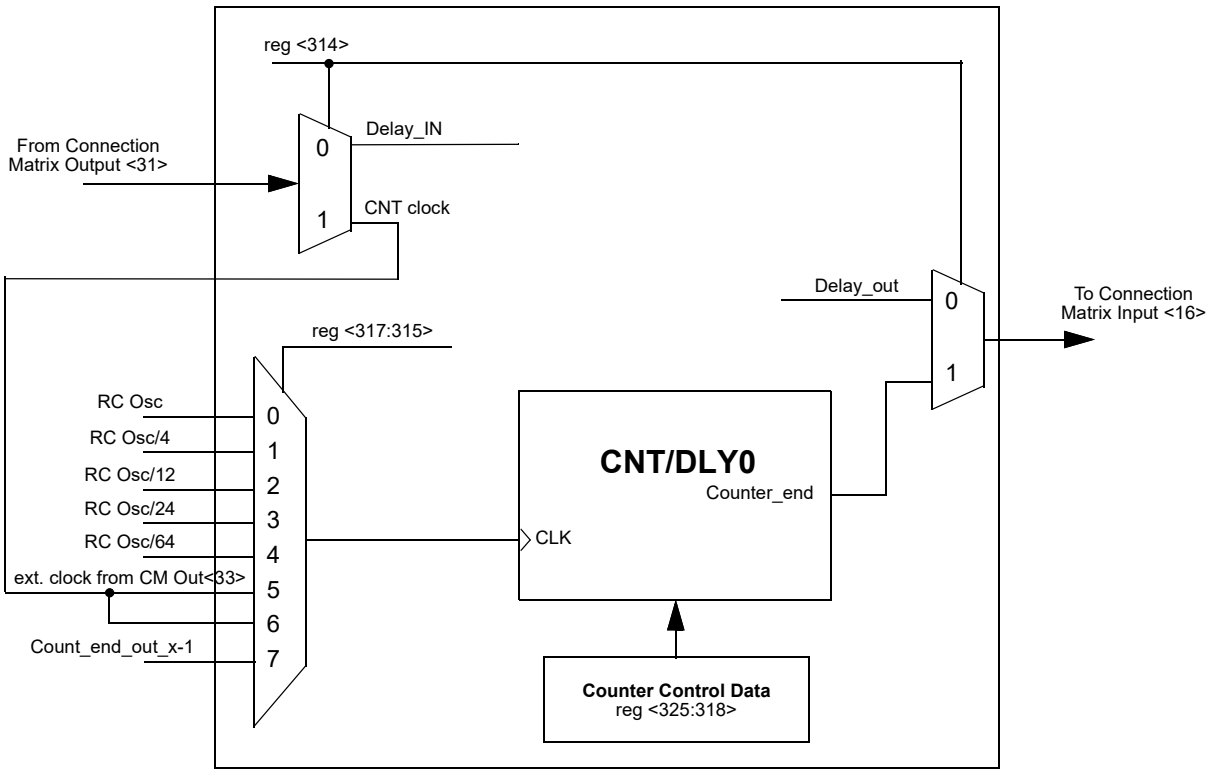


Figure 32. CNT/DLY0

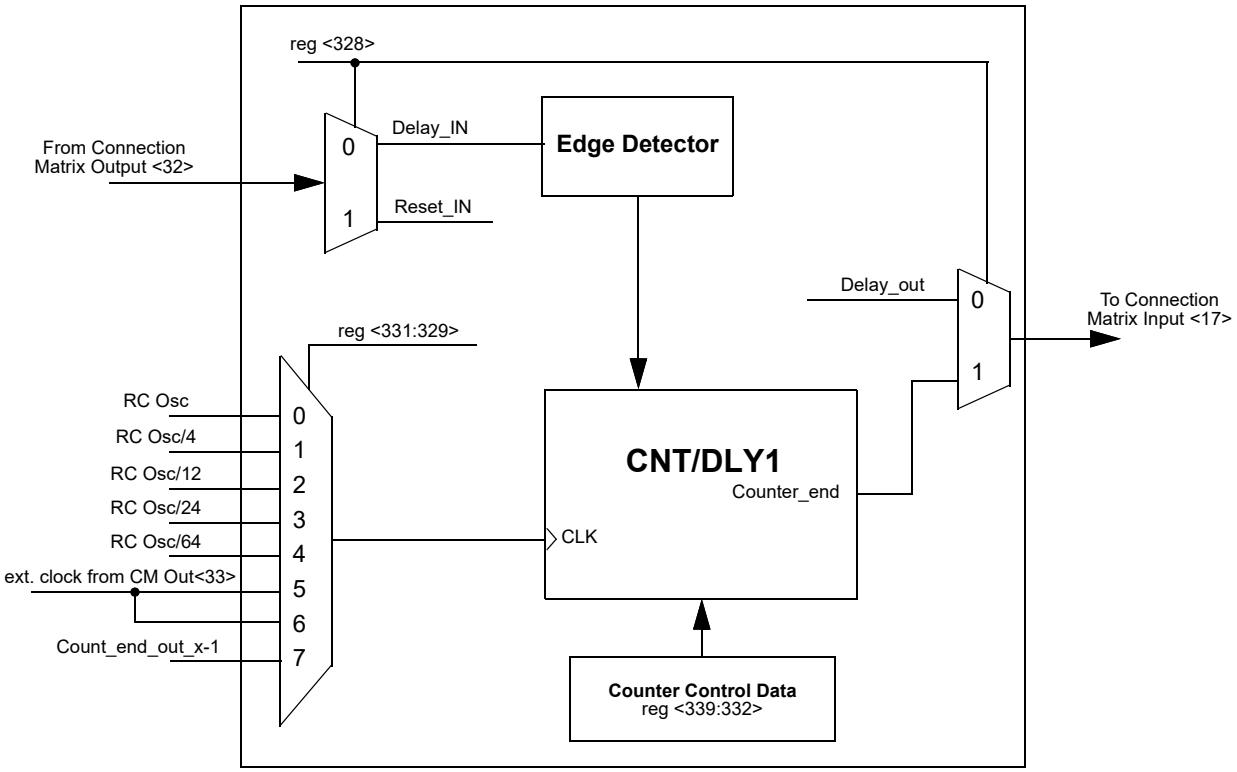


Figure 33. CNT/DLY1

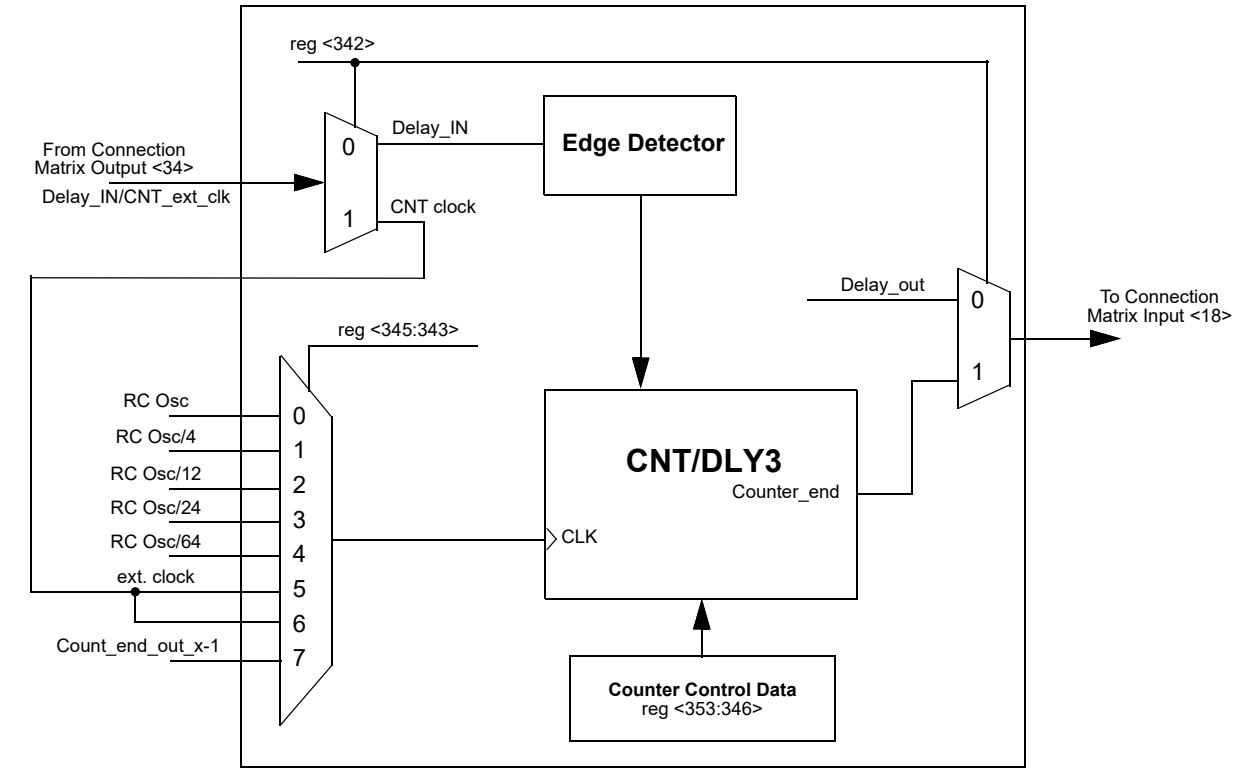


Figure 34. CNT/DLY3

12.1 CNT/DLY0 Register Settings

Table 38. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg <314>	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select (external clock is only for counter mode)	reg <317:315>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter3 Overflow
Counter0 Control Data/Delay0 Time Control	reg <325:318>	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay0 Mode Select or asynchronous counter reset	reg <327:326>	00: Delay on both falling and rising edgeless delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.2 CNT/DLY1 Register Settings

Table 39. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg <328>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source Select (external clock is only for counter mode)	reg <331:329>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
Counter1 Control Data/Delay1 Time Control	reg <339:332>	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay1 Mode Select or asynchronous counter reset	reg <341:340>	00: Delay on both falling and rising edgeless delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

12.3 CNT/DLY3 Register Settings

Table 40. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay3 Mode Select	reg <342>	0: Delay Mode 1: Counter Mode
Counter/Delay3 Clock Source Select (external clock is only for counter mode)	reg <345:343>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter2 Overflow
Counter3 Control Data/Delay3 Time Control	reg <353:346>	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay3 Mode Select	reg <355:354>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

13.0 Programmable Delay / Edge Detector or Deglitch Filter (Part of Combination Macrocells)

13.1 Programmable Delay / Edge Detector

The SLG46127 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

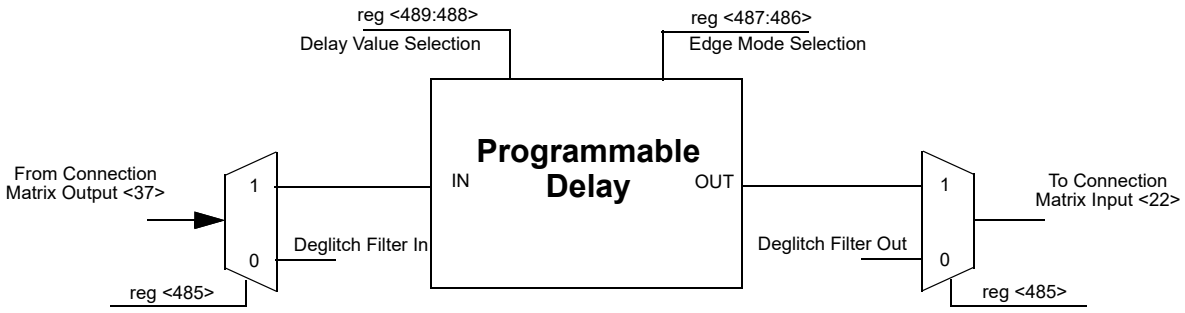


Figure 35. Programmable Delay

13.1.1 Programmable Delay Timing Diagram - Edge Detector Output

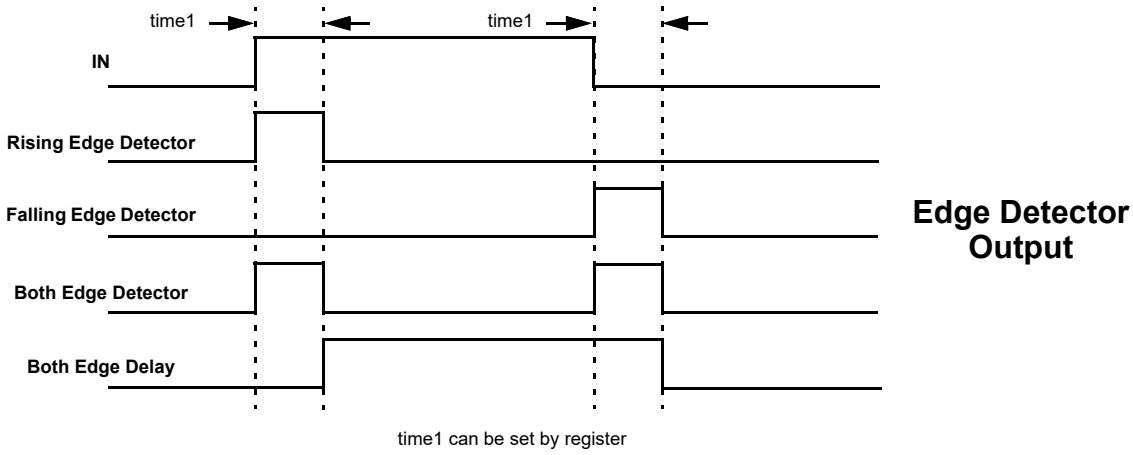


Figure 36. Edge Detector Output

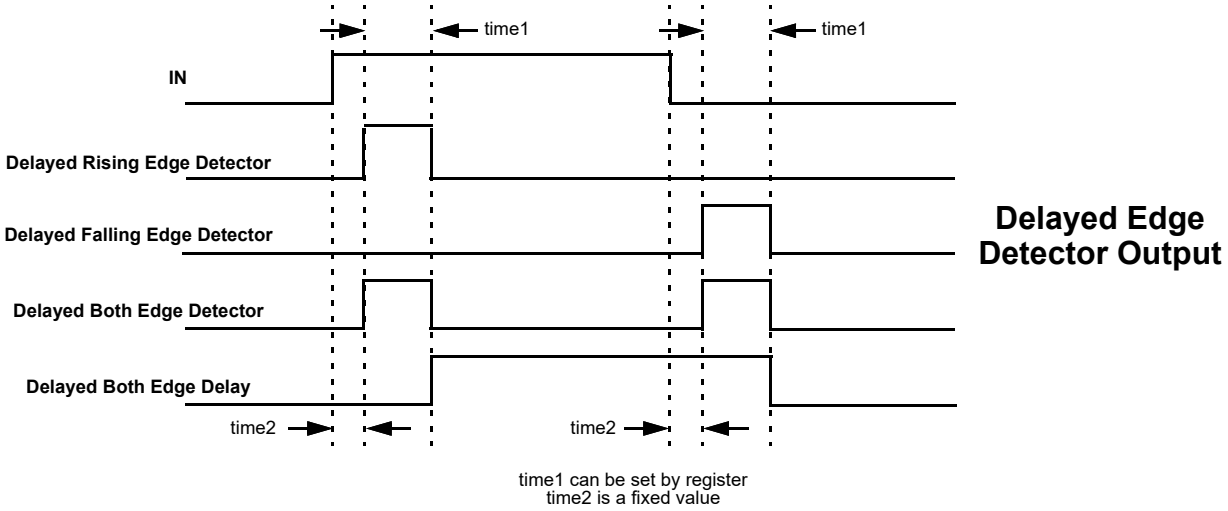


Figure 37. Delayed Edge Detector Output

Note: For delays and widths refer to Table 4.

13.1.2 Programmable Delay Register Settings

Table 41. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable delay or filter output select	reg <485>	0: programmable delay output 1: filter output
Select the edge mode of programmable delay & edge detector	reg <487:486>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	reg <489:488>	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns

13.2 Deglitch Filter

The SLG46127 has an additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one deglitch filter.

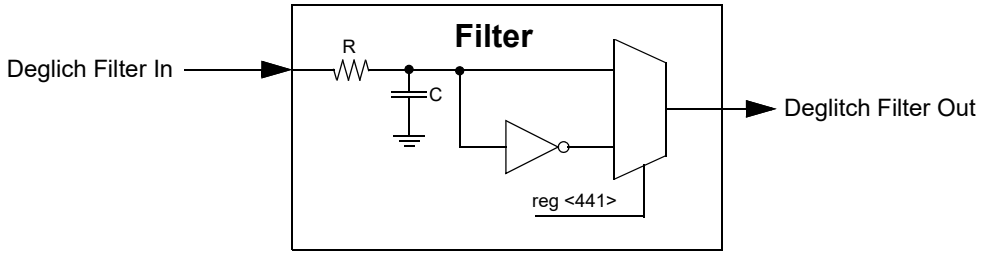


Figure 38. Deglitch Filter

14.0 Voltage Reference (VREF)

14.1 Voltage Reference Overview

The SLG46127 has a Voltage Reference Macrocell to provide references to the two analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from PIN1. The macrocell also has the option to output reference voltages on PIN10. See table below for the available selections for each analog comparator. Also see *Figure 39.* below, which shows the reference output structure.

14.2 VREF Selection Table

Table 42. VREF Selection Table.

SEL<4:0>	ACMP0_VREF	ACMP1_VREF
11010	ext. Vref (PIN1)	ext. Vref (PIN1)
11001	V_{DD} / 4	V_{DD} / 4
11000	V_{DD} / 3	V_{DD} / 3
10111	1.20 V	1.20 V
10110	1.15 V	1.15 V
10101	1.10 V	1.10 V
10100	1.05 V	1.05 V
10011	1.00 V	1.00 V
10010	0.95 V	0.95 V
10001	0.90 V	0.90 V
10000	0.85 V	0.85 V
01111	0.80 V	0.80 V
01110	0.75 V	0.75 V
01101	0.70 V	0.70 V
01100	0.65 V	0.65 V
01011	0.60 V	0.60 V
01010	0.55 V	0.55 V
01001	0.50 V	0.50 V
01000	0.45 V	0.45 V
00111	0.40 V	0.40 V
00110	0.35 V	0.35 V
00101	0.30 V	0.30 V
00100	0.25 V	0.25 V
00011	0.20 V	0.20 V
00010	0.15 V	0.15 V
00001	0.10 V	0.10 V
00000	0.05 V	0.05 V

V_{DD}	Practical VREF Range	Note
2.0 V - 5.5 V	50 mV ~1.2 V	
1.7 V - 2.0 V	50 mV ~1.1 V	Do not operate above 1.1 V

14.3 VREF Block Diagram

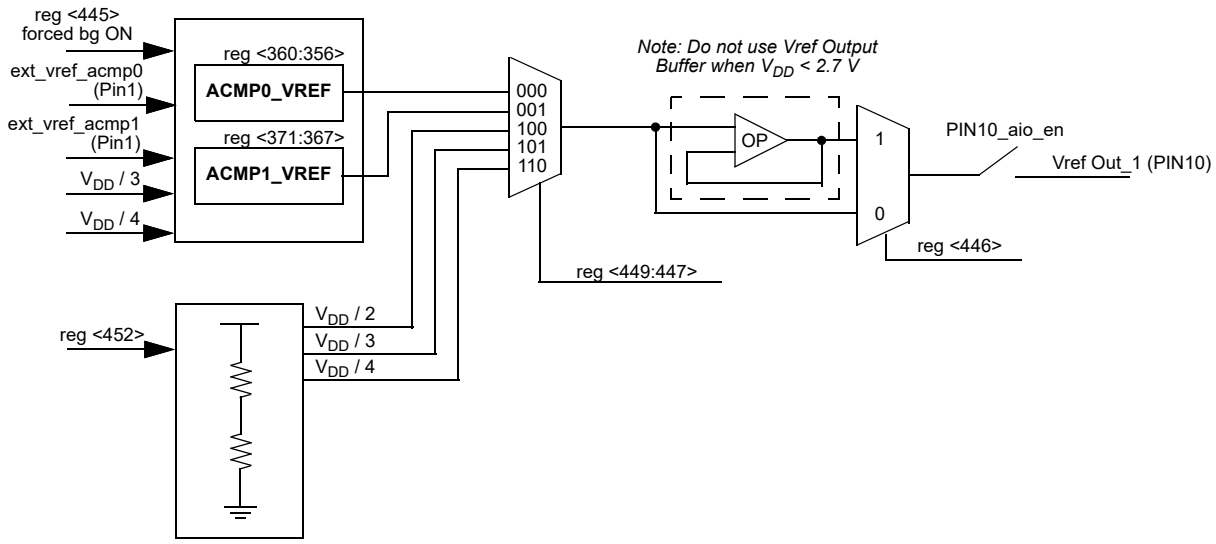


Figure 39. Voltage Reference Block Diagram

15.0 RC Oscillator (RC Osc)

15.1 RC Oscillator Overview

The SLG46127 has two internal RC oscillators, one that runs at 25 kHz and one that runs at 2 MHz. When using the chip internal RC OSC, a choice is available to “Force Power On”, meaning that the RC OSC will always run, or “Auto Power On”, meaning that the RC OSC will have an associated startup and settling time associated with it (offset). *Figure 40.* and *Figure 41.* show maximum power on delay vs. V_{DD}.

Note: RC OSC power setting: "Auto Power On”.

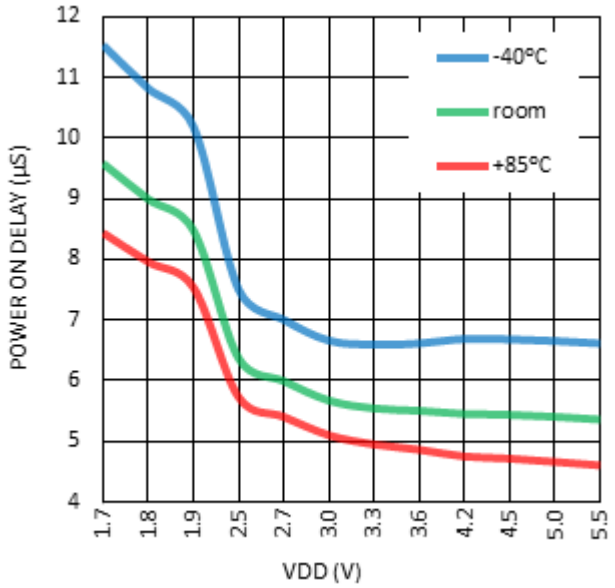


Figure 40. Maximum Power On Delay vs. V_{DD}, RC OSC = 2 MHz.

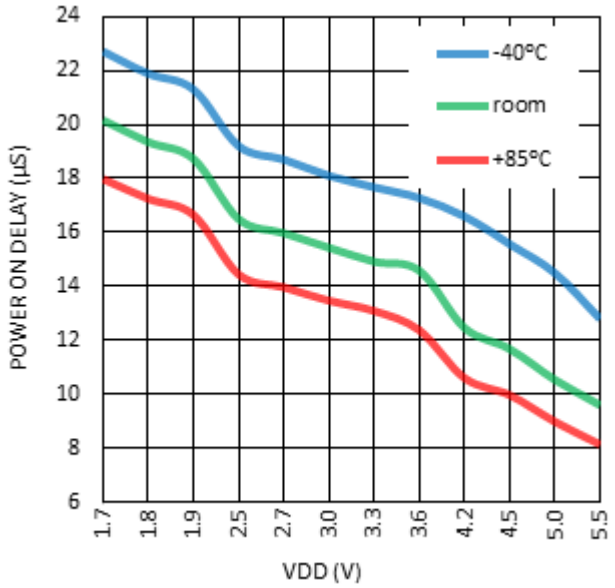


Figure 41. Maximum Power On Delay vs. V_{DD}, RC OSC = 25 kHz.

The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (PIN11). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider (also known as the clock pre-divider) allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. There are two second stage divider controls (OUT0 and OUT1). Each has its own input of one frequency from the first stage divider, and outputs five different frequencies on Connection Matrix Input lines <23>, and <24>. See *Figure 42.* below for details of the frequencies for each of these five Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

15.2 RC OSC Block Diagram

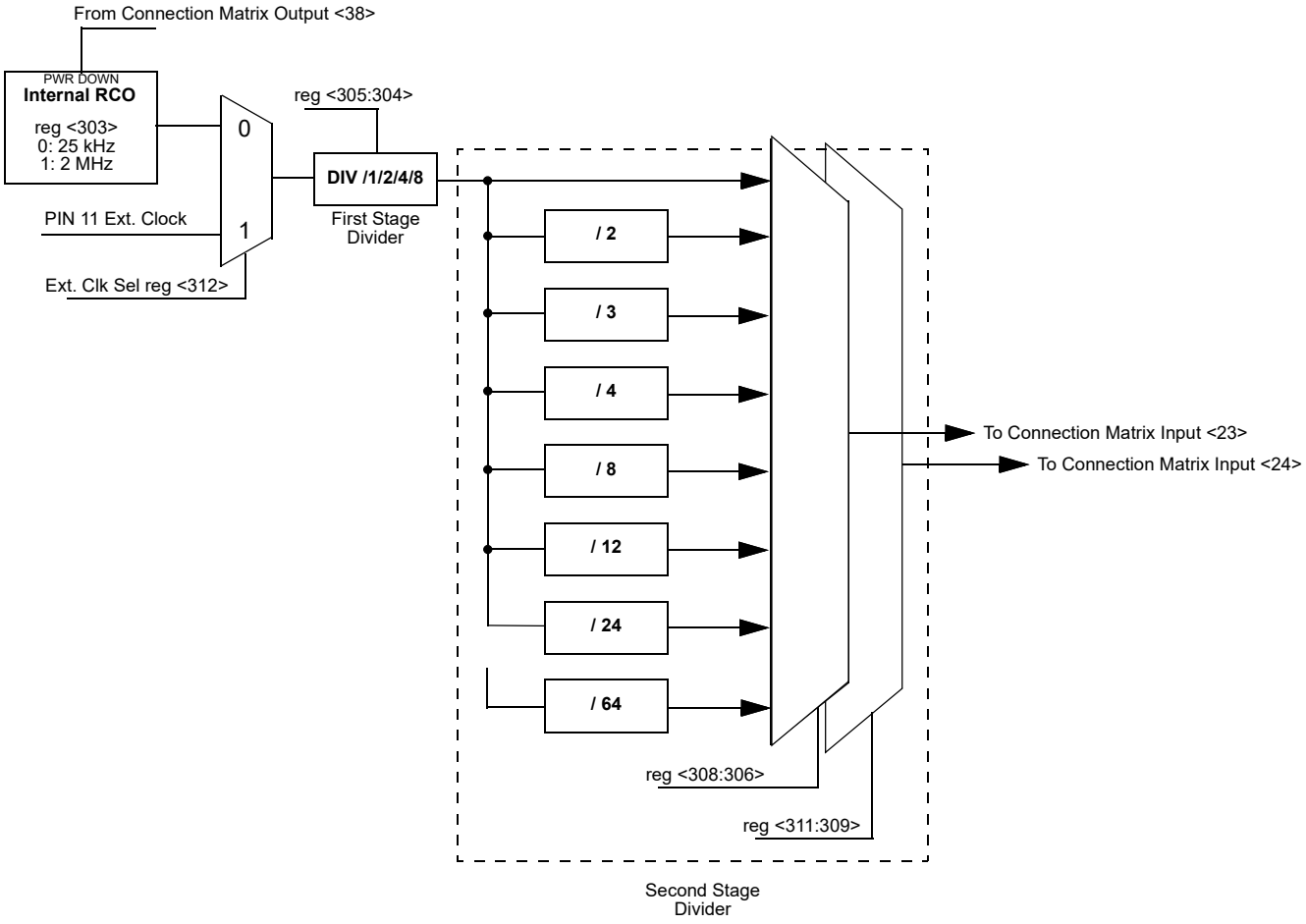


Figure 42. RC OSC Block Diagram

16.0 Power On Reset (POR)

The SLG46127 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins.

16.1 General Operation

The SLG46127 is guaranteed to be powered down and nonoperational when the V_{DD} voltage (on PIN12) is less than 0.6 V, but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1. There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46127, the voltage applied on the V_{DD} should be higher than the Power_ON threshold (see Note 2). The full operational V_{DD} range for the SLG46127 is 1.71 V – 5.5 V (1.8 V ±5 % - 5 V±10 %). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46127 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note 2. The Power_ON threshold can vary by PVT, but typically it is 1.6 V.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than 0.6 V.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can’t be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

16.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 43.* .

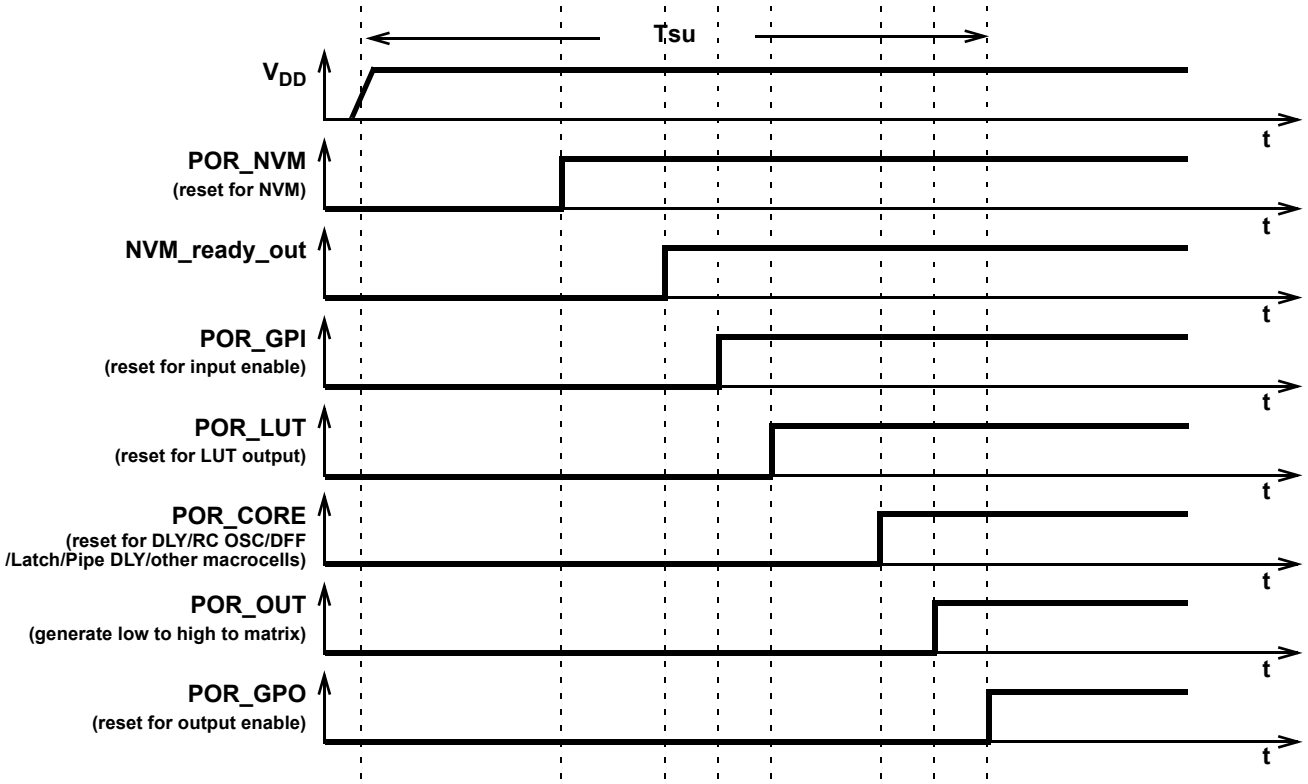


Figure 43. POR sequence

As can be seen from *Figure 43.* after the V_{DD} has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input PINs, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature and even will vary from chip to chip (process influence).

16.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46127 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (*Figure 44.* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

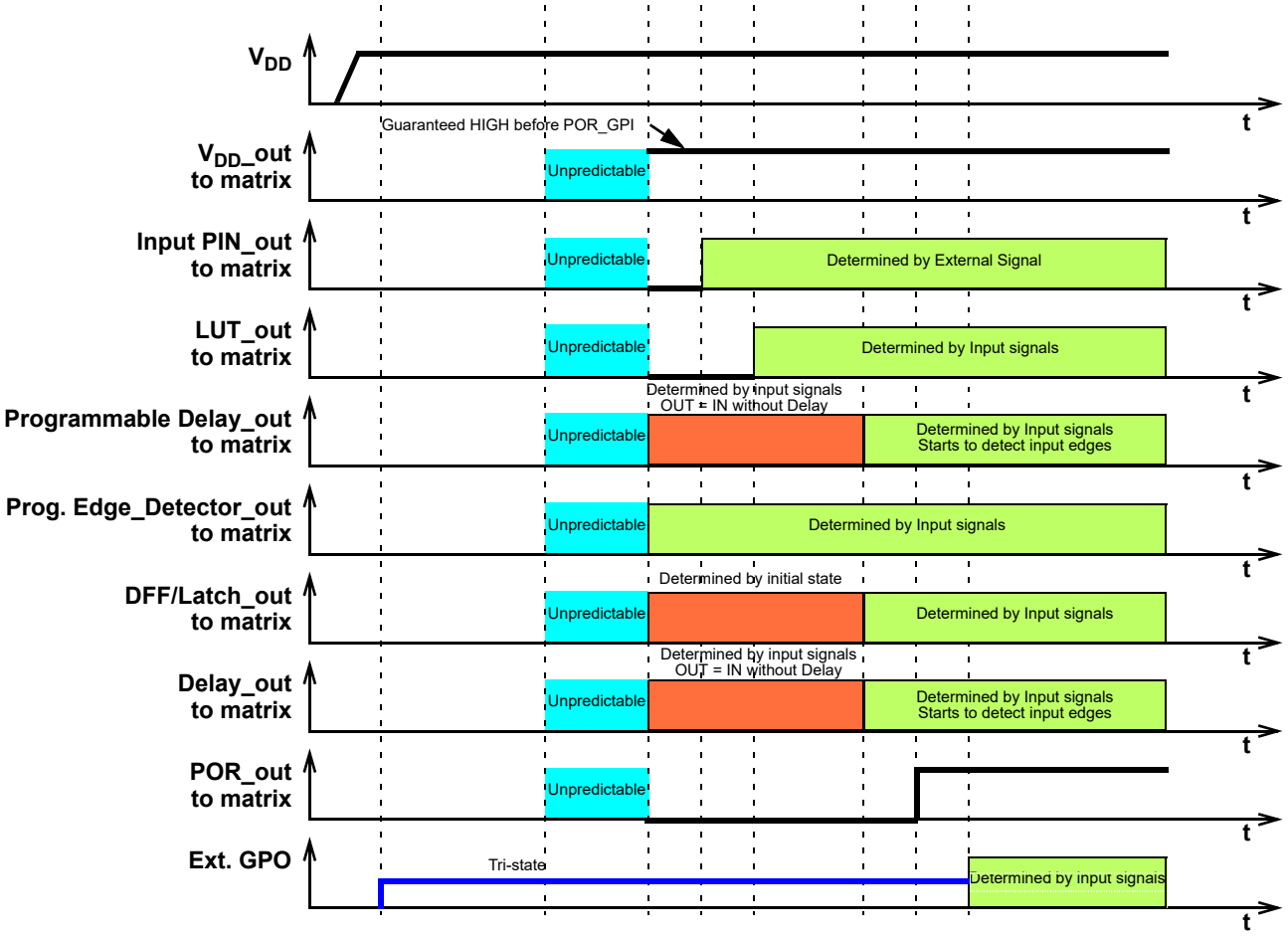


Figure 44. Internal Macrocell States during POR sequence

17.0 Dual, 2A P-FET Power Switches

17.1 Power Switches Overview

The SLG46127 has a dual-channel, 44 mΩ PMOS power switch designed to switch 1.71 to 5.5 V power rails up to 2 A per channel.

Each P-FET Power Switch can be controlled internally via the ONx digital input of the P-FET Power Switch component in GreenPAK Designer, allowing the user to generate integrated mixed-signal control circuits, or externally via PWR_SW_ONx.

Whether controlled externally or internally, a low signal on either ONx or PWR_SW_ONx will close the P-FET Power Switch.

Each P-FET Power Switch need not be used in the same voltage domain as V_{DD}. However, when V_{IN} is not tied to V_{DD}, using a large pull-up resistor on PWR_SW_ON0 and PWR_SW_ON1 is recommended to prevent current from flowing through the P-FET Power Switch while the device is not powered.

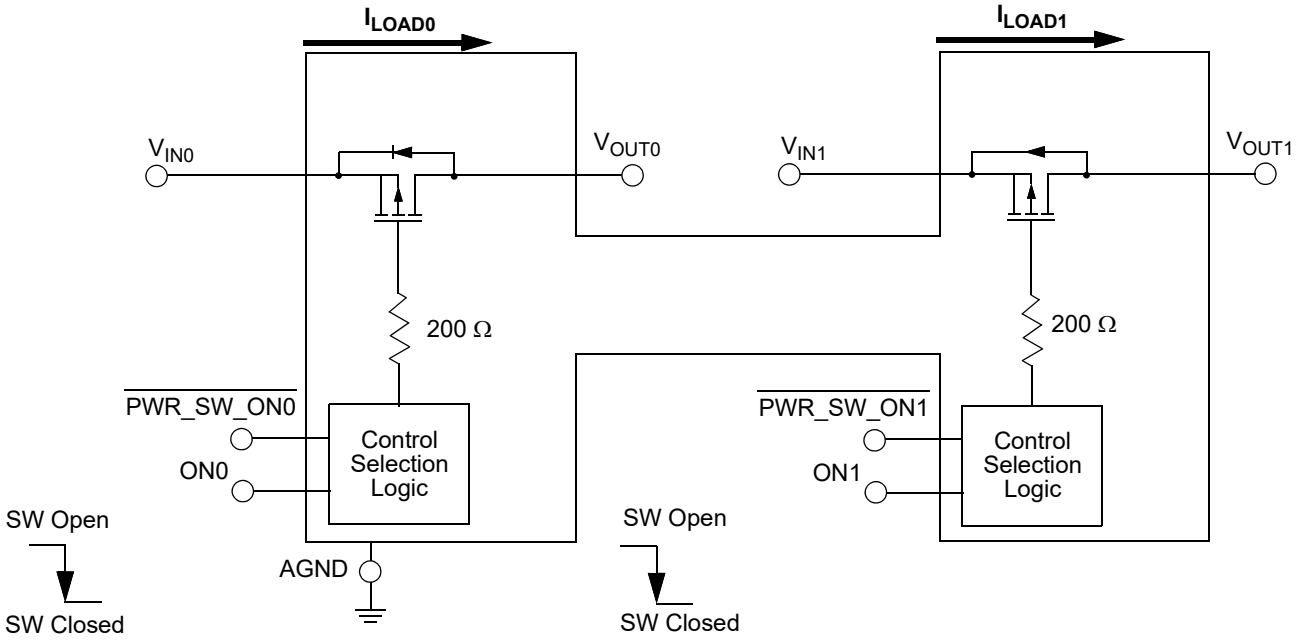


Figure 45. Dual P-FET Power Switch

17.2 Driving the P-FET Switch

Gate of P-FET power switch can be driven by either internally generated signal or directly by external source connected to corresponding PWR_SW_ONx pin. Simplified circuit topologies are illustrated on *Figure 46.*

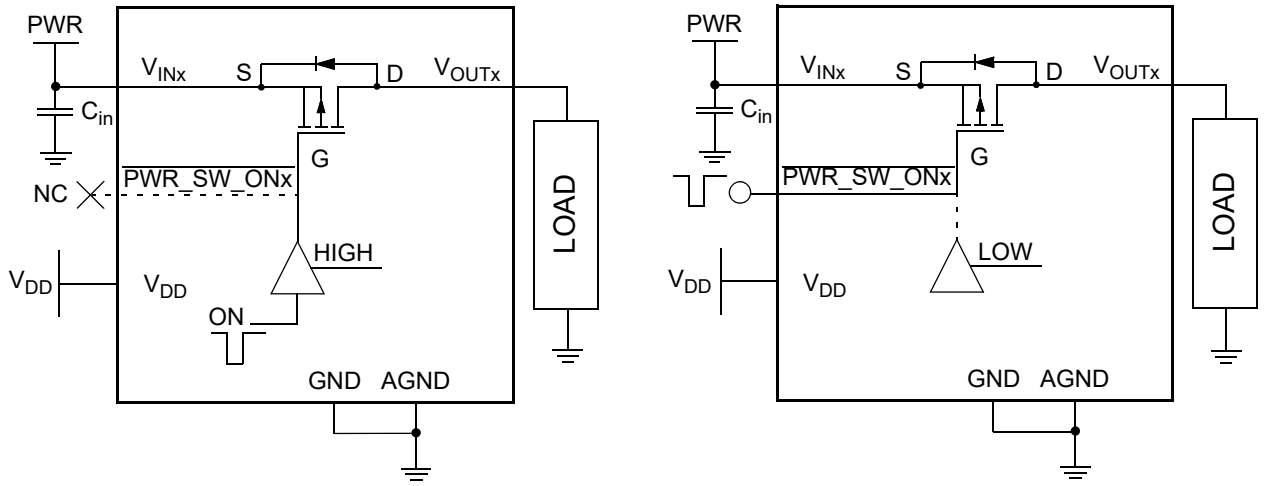


Figure 46. Typical Circuit Topology for Internal (left) and External (right) drive modes

Datasheet values for switching times are given for driving the resistive loads. The definitions of rise (t_r), fall (t_f) and delay times ($t_{d(on)}$ and $t_{d(off)}$) are given on *Figure 47*. To achieve highest switching performance circuit should be laid off using high speed PCB layout techniques.

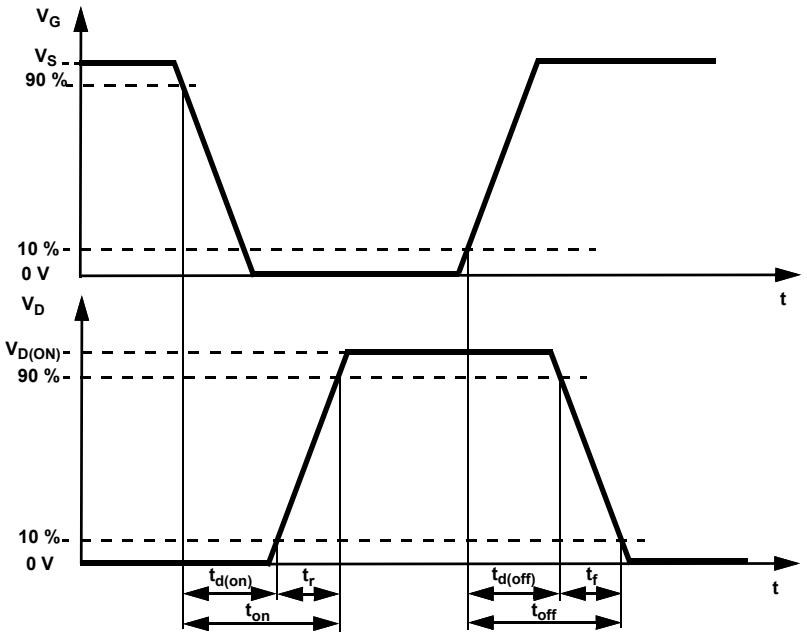


Figure 47. Definitions for Rise, Fall and Switching Delay Times

Typical resistive switching waveforms are given on *Figure 49.* and *Figure 50.* Note that fall time is dependent on load current (see section *17.4 Power Switch Typical Performance*). At low loads turn off process can be delayed, therefore discharge circuit should be provided to reduce load turn off time in that case.

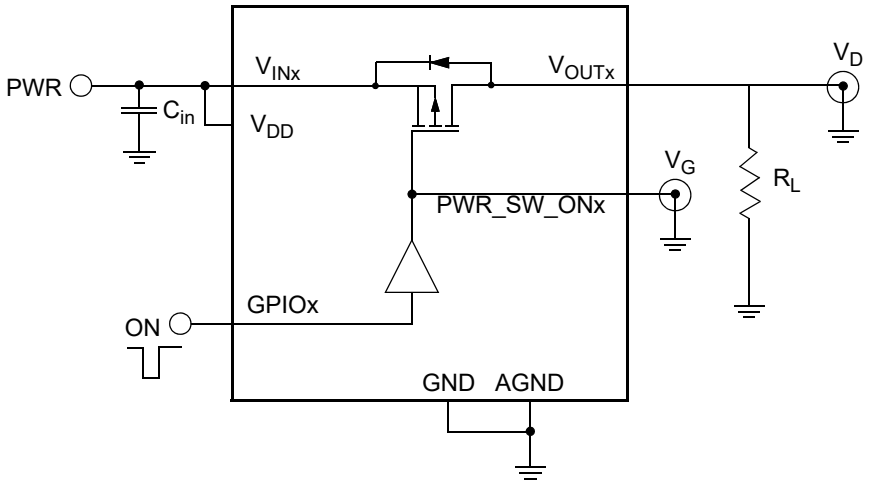


Figure 48. Test Circuit for Typical Switching Waveforms

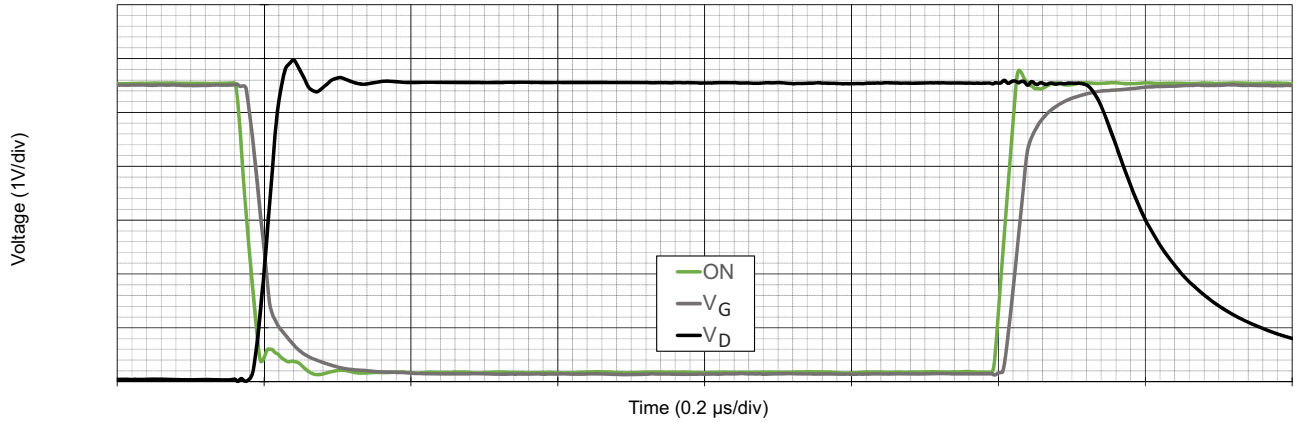


Figure 49. Typical Switching Waveforms (Internal Drive, Resistive Load, R_L = 100 Ω, V_{DD} = V_{IN} = 5.5 V)

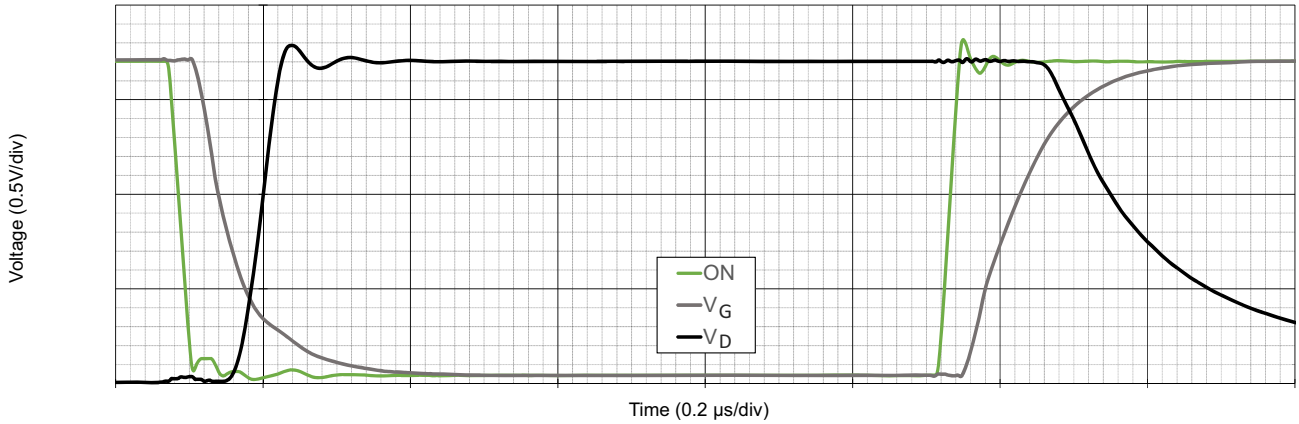


Figure 50. Typical Switching Waveforms (Internal Drive, Resistive Load, R_L = 100 Ω, V_{DD} = V_{IN} = 1.71 V)

17.3 Power Dissipation

The junction temperature of the Power Switch depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the Power Switch is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON0} \times I_{OUT0}^2) + (RDS_{ON1} \times I_{OUT1}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON} = Channel 0 and Channel 1 Power MOSFET ON resistance, in Ohms (Ω), respectively

I_{OUT} = Channel 0 and Channel 1 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \Theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

Θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the Power Switch power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{INx}-V_{OUTx}) and the magnitude of that channel's output current (I_{OUTx}):

$$PD_{TOTAL} = [(V_{IN0}-V_{OUT0}) \times I_{OUT0}] + [(V_{IN1}-V_{OUT1}) \times I_{OUT1}] \text{ or}$$

$$PD_{TOTAL} = [(V_{IN0} - (R_{LOAD0} \times I_{OUT0})) \times I_{OUT0}] + [(V_{IN1} - (R_{LOAD1} \times I_{OU1})) \times I_{OUT1}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

V_{IN} = Channel 0 and Channel 1 Input Voltage, in Volts (V), respectively

R_{LOAD} = Channel 0 and Channel 1 Output Load Resistance, in Ohms (Ω), respectively

I_{OUT} = Channel 0 and Channel 1 output current, in Amps (A), respectively

V_{OUT} = Channel 0 and Channel 1 output voltage, or $R_{LOAD} \times I_{OUT}$, respectively

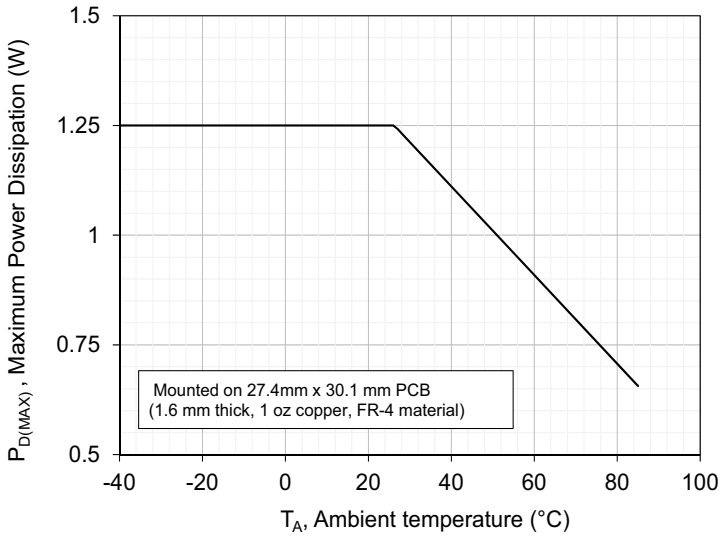


Figure 51. Power Dissipation Derating Curve

17.4 Power Switch Typical Performance

T_A = 25 °C, V_{DD} = 5.5 V, unless otherwise noted.

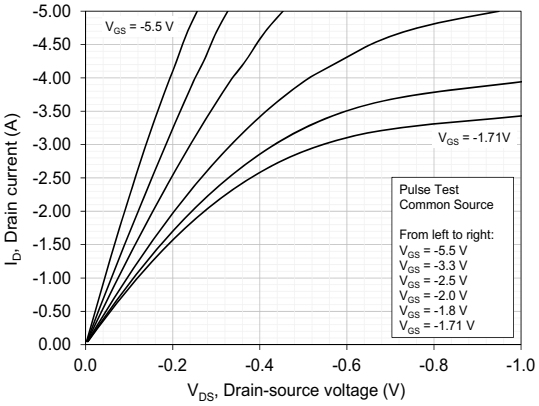


Figure 52. Typical Output Characteristics

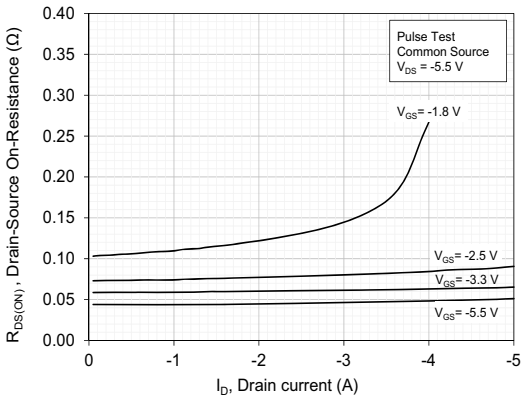


Figure 53. Drain-Source On-Resistance vs. Drain Current

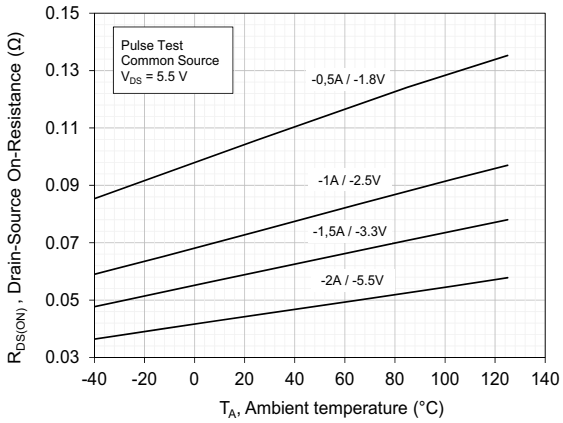


Figure 54. Typical Drain-Source On-Resistance vs. Ambient Temperature

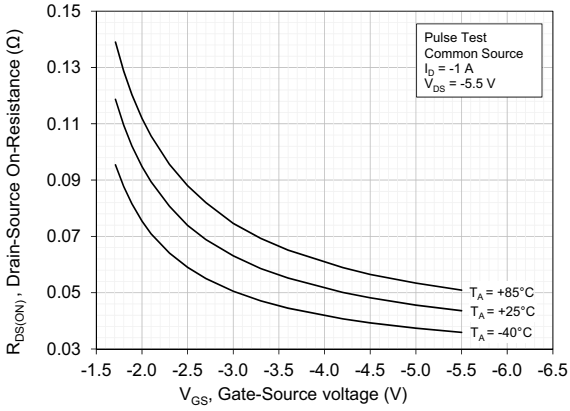


Figure 55. Gate-Source On-Resistance Gate-Source Voltage

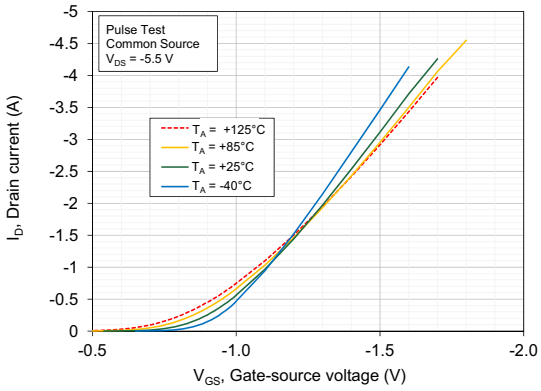


Figure 56. Drain Current vs. Gate-Source Voltage

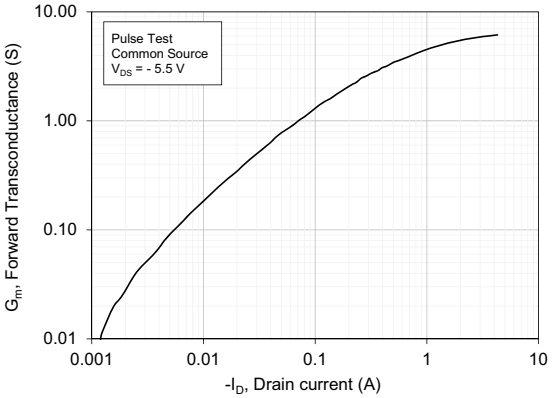


Figure 57. Typical Forward Transconductance

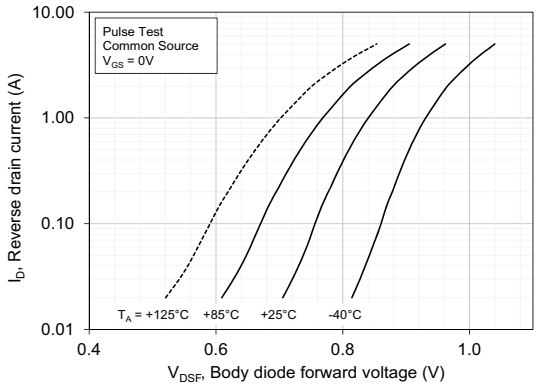


Figure 58. Typical Drain-Source Diode Forward Voltage

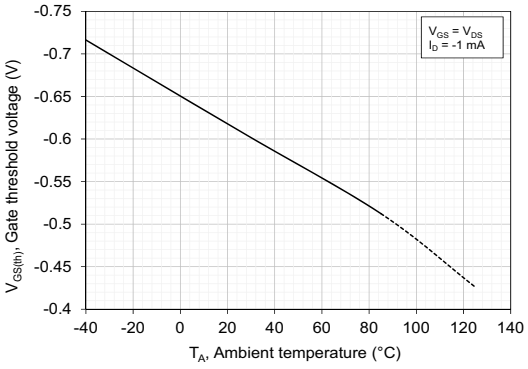


Figure 59. Gate Threshold Voltage vs Ambient Temperature

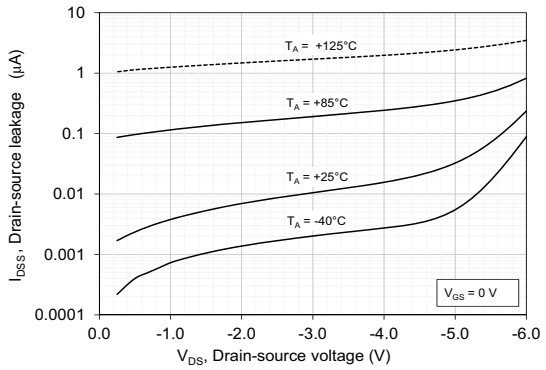


Figure 60. Zero Gate Voltage Drain Current

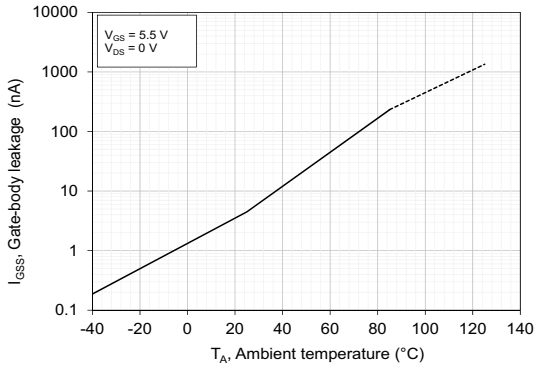


Figure 61. Gate-Body Leakage vs. Ambient Temperature

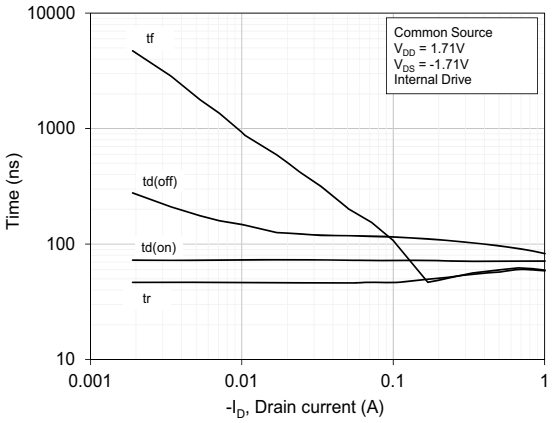


Figure 62. Typical Switching Time (Internal Gate Drive) at V_{DS} = 1.71 V

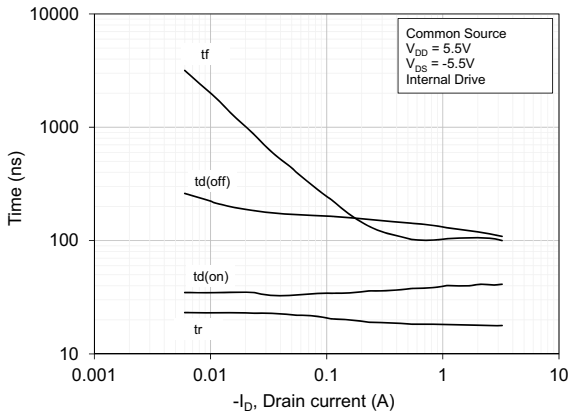


Figure 63. Typical Switching Time (Internal Gate Drive) at V_{DS} = 5.5 V

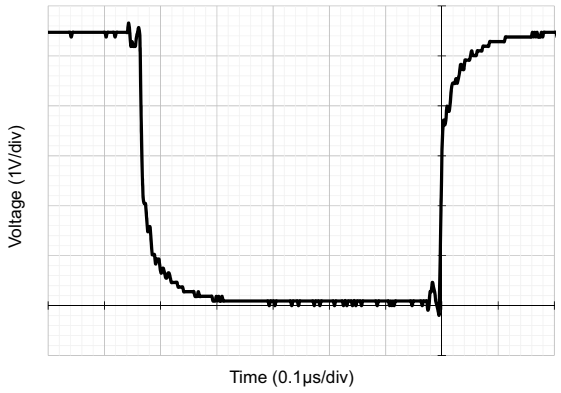


Figure 64. Typical Gate Input Waveform, Internal Gate Drive Source (Switching Time Test)

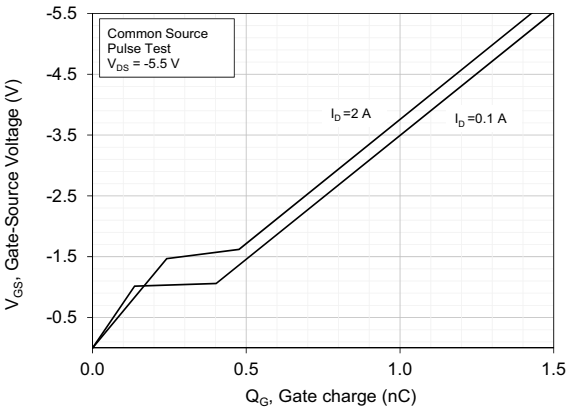


Figure 65. Typical Gate Charge vs. Gate-Source Voltage

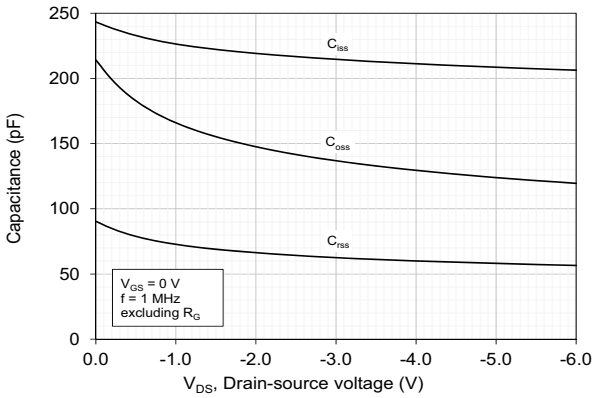


Figure 66. Typical Capacitance vs. Drain-Source Voltage

18.0 Appendix A - SLG46127 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg <4:0>	Matrix Out: PIN14 Digital Output Source	
reg <9:5>	Matrix Out: PIN1 Digital Output Source	
reg <14:10>	Matrix Out: PIN2 Digital Output Source	
reg <19:15>	Matrix Out: Output Enable of PIN2	
reg <24:20>	Matrix Out: In0 of LUT2_0 or Clock Input of DFF0	
reg <29:25>	Matrix Out: In1 of LUT2_0 or Data Input of DFF0	
reg <34:30>	Matrix Out: In0 of LUT2_1 or Clock Input of DFF1	
reg <39:35>	Matrix Out: In1 of LUT2_1 or Data Input of DFF1	
reg <44:40>	Matrix Out: In0 of LUT2_2	
reg <49:45>	Matrix Out: In1 of LUT2_2	
reg <54:50>	Matrix Out: In0 of LUT2_3	
reg <59:55>	Matrix Out: In1 of LUT2_3	
reg <64:60>	Matrix Out: In0 of LUT3_0 or Clock Input of DFF2	
reg <69:65>	Matrix Out: In1 of LUT3_0 or Data Input of DFF2	
reg <74:70>	Matrix Out: In2 of LUT3_0 or nRST Input of DFF2	
reg <79:75>	Matrix Out: In0 of LUT3_1 or Clock Input of DFF3	
reg <84:80>	Matrix Out: In1 of LUT3_1 or Data Input of DFF3	
reg <89:85>	Matrix Out: In2 of LUT3_1 or nRST (nSET) of DFF3	
reg <94:90>	Matrix Out: In0 of LUT3_2	
reg <99:95>	Matrix Out: In1 of LUT3_2	
reg <104:100>	Matrix Out: In2 of LUT3_2	
reg <109:105>	Matrix Out: In0 of LUT3_3	
reg <114:110>	Matrix Out: In1 of LUT3_3	
reg <119:115>	Matrix Out: In2 of LUT3_3	
reg <124:120>	Matrix Out: In0 of LUT3_4 or Input of Pipe Delay	
reg <129:125>	Matrix Out: In1 of LUT3_4 or nRST of Pipe Delay	
reg <134:130>	Matrix Out: In2 of LUT3_4 or Clock of Pipe Delay	
reg <139:135>	Matrix Out: In0 of LUT4_0 or Input for Delay2 (Counter2) external clock	
reg <144:140>	Matrix Out: In1 of LUT4_0 or Input for Delay2 data (Counter2 reset)	
reg <149:145>	Matrix Out: In2 of LUT4_0	
reg <154:150>	Matrix Out: In3 of LUT4_0	
reg <159:155>	Matrix Out: Input for Delay0 data (Counter0 reset)	
reg <164:160>	Matrix Out: Input for Delay1 data (Counter1 reset)	
reg <169:165>	Matrix Out: Input for Delay0/1 (Counter0/1) external clock	
reg <174:170>	Matrix Out: Input for Delay3 (Counter3) external clock	
reg <179:175>	Matrix Out: pdb (power down) for ACMP0	
reg <184:180>	Matrix Out: pdb (power down) for ACMP1	
reg <189:185>	Matrix Out: Input for programmable Delay (deglitch filter input)	

Register Bit Address	Signal Function	Register Bit Definition
reg <194:190>	Matrix Out: Power down for OSC	
reg <199:195>	Pin15 Digital Output Source and Power Switch ON0 Source	
reg <204:200>	Pin16 Digital Output Source and Power Switch ON1 Source	
reg <209:205>	Matrix Out: PIN10 Digital Output Source	
reg <214:210>	Matrix Out: Output Enable of PIN10	
reg <219:215>	Matrix Out: PIN11 Digital Output Source	
reg <223:220>	Reserved	Reserved
DFF0/Latch		
reg <227:224>	reg <224> DFF0 or Latch select	0: DFF function 1: Latch function
	reg <225> DFF0 output select	0: Q output 1: nQ output
	reg <226> DFF0 initial polarity select	0: Low 1: High
	reg <227> Unused if DFF/Latch selected	Unused
DFF1/Latch		
reg <231:228>	reg <228> DFF1 or Latch select	0: DFF function 1:Latch function
	reg <229> DFF1 output select	0: Q output 1: nQ output
	reg <230> DFF1 initial polarity select	0: Low 1:High
	reg <231> Unused if DFF/Latch selected	Unused
LUT2_2 data		
reg <235:232>	LUT2_2 data	LUT2_2 data
LUT2_1 data		
reg <239:236>	LUT2_1 data	LUT2_1 data
LUT2_0/DFF0		
reg <240>	LUT2_0 or DFF0 select	0: LUT2_0 1: DFF0
LUT2_1/DFF1		
reg <241>	LUT2_1 or DFF1 select	0: LUT2_1 1: DFF1
LUT3_0 or DFF2/Latch		
reg <249:242>	reg <242> DFF2 or Latch select	0: DFF function 1: Latch function
	reg <243> DFF2 output select	0: Q output 1: nQ output
	reg <244> DFF2 nRST/nSET select	0: nRST from matrix output 1: nSET from matrix output
	reg <245> DFF2 initial polarity select	0: Low 1: High
	reg <249:246> Unused if DFF/Latch selected	Unused

Register Bit Address	Signal Function	Register Bit Definition
LUT3_1 or DFF3/Latch		
reg <257:250>	reg <250> DFF3 or Latch select	0: DFF function 1: Latch function
	reg <251> DFF3 output select	0: Q output 1: nQ output
	reg <252> DFF3 nRST/nSET select	0: nRST from matrix output 1: nSET from matrix output
	reg <253> DFF3 initial polarity select	0: Low 1: High
	reg <257:254> Unused if DFF/Latch selected	Unused
LUT3_2 data		
reg <265:258>	LUT3_2 data	LUT3_2 data
LUT3_3 data		
reg <273:266>	LUT3_3 data	LUT3_3 data
LUT3_4 or pipe number select		
reg <281:274>	reg <276:274>: OUT0 select	data (pipe number)
	reg <279:277>: OUT1 select	data (pipe number)
	reg <281:280>: Unused if Pipe Delay selected	Unused
LUT3/DFF Select		
reg <282>	LUT3_0 or DFF2 select	0: LUT3_0 1: DFF2
reg <283>	LUT3_1 or DFF3 select	0: LUT3_1 1: DFF3
reg <284>	LUT3_4 or Pipe Delay output select	0: LUT3_4 1: Pipe Delay
LUT4_0 or Counter/Delay2 mode selection		
reg <300:285>	reg <285> Counter/Delay2 mode selection	0: Delay Mode 1: Counter Mode
	reg <288:286> Counter/Delay2 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter1 Overflow
	reg <296:289> Counter/Delay2 Control Data	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
	reg <298:297> Delay2 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for Delay & counter reset) 01: Delay on falling edge only (for Delay & counter reset Delay) 10: on rising edge only (for Delay & counter reset) 11: No Delay on either falling or rising edges / high level reset for counter mode
	reg <300:299> Unused is Counter/Delay2 selected	Unused
reg <301>	LUT4_0 or Counter2 select 0: LUT4_0, 1: Counter2	0: LUT4_0 1: Counter2

Register Bit Address	Signal Function	Register Bit Definition
reg <302>	Force RC oscillator on	0: Auto Power on 1: Force Power on
reg <303>	RC Oscillator frequency control	0: 25k 1: 2M
reg <305:304>	Osc clock pre-divider	00: div1 01: div2 10: div4 11: div8
reg <308:306>	Internal Oscillator frequency divider control 0 for Matrix Input	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg <311:309>	Internal Oscillator frequency divider control 1 for Matrix Input	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
reg <312>	External Clock Source Select	0: Internal Oscillator 1: External Clock from PIN11
reg <313>	Reserved Reserved	Reserved
Counter/Delay 0		
reg <327:314>	reg <314>Counter/Delay0 mode selection	0: Delay Mode 1: Counter Mode
	reg <317:315> Counter/Delay0 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter3 Overflow
	reg <325:318> Counter0 Control Data/Delay0 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
	reg <327:326> Delay0 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for Delay & counter reset) 01: Delay on falling edge only (for Delay & counter reset) 10: Delay on rising edge only (for Delay & counter reset) 11: No Delay on either falling or rising edges / high level reset for counter mode

Register Bit Address	Signal Function	Register Bit Definition
Counter/Delay 1		
reg <341:328>	reg <328> Counter/Delay1 mode selection	0: Delay Mode 1: Counter Mode
	reg <331:329> Counter/Delay1 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
	reg <339:332> Counter1 Control Data/Delay1 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
	reg <341:340> Delay1 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for Delay & counter reset) 01: Delay on falling edge only (for Delay & counter reset) 10: Delay on rising edge only (for Delay & counter reset) 11: No Delay on either falling or rising edges / high level reset for counter mode
Counter/Delay 3		
reg <355:342>	reg <342> Counter/Delay3 mode selection	0: Delay Mode 1: Counter Mode
	reg <345:343> Counter/Delay3 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter2 Overflow
	reg <353:346> Counter3 Control Data/Delay4 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
	reg <355:354> Delay3 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No Delay on either falling or rising edges

Register Bit Address	Signal Function	Register Bit Definition
ACMP0		
reg <366:356>	reg <360:356> ACMP0 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: EXT_VREF(PIN1)
	reg <362:361> ACMP0 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
	reg <364:363> ACMP0 positive Input divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x
	reg <365> ACMP0 low bandwidth (typ: Max.1 MHz) enable	0: off 1: on
	reg <366> ACMP0 positive input source select PIN14 and V_{DD}	0: PIN14 1: V_{DD}

Register Bit Address	Signal Function	Register Bit Definition
ACMP1		
reg <378:367>	reg <371:367> ACMP1 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: EXT_VREF(PIN1)
	reg <373:372> ACMP1 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
	reg <375:374> ACMP1 positive Input divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x
	reg <376> ACMP1 100uA current source option	0: disable 1: enable
	reg <377> ACMP1 low bandwidth (typ: Max.1 MHz) enable	0: off 1: on
	reg <378> ACMP1 positive input source select PIN2 and PIN14	0: PIN2 1: PIN14
PIN 1		
reg <396:390>	reg <392:390> PIN1 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <394:393> PIN1 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <395> PIN1 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <396> PIN1 driver strength selection	0: 1X 1: 2X

Register Bit Address	Signal Function	Register Bit Definition
PIN2		
reg <403:397>	reg <398:397> PIN2 mode control (sig_PIN2_oe =0)	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input / Output
	reg <400:399> PIN2 mode control (sig_PIN2_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
	reg <402:401> PIN2 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <403> PIN2 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
PIN10		
reg <424:418>	reg <419:418> PIN10 mode control (sig_PIN10_oe =0)	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input / Output
	reg <421:420> PIN10 mode control (sig_PIN10_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
	reg <423:422> PIN10 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <424> PIN10 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
PIN11		
reg <431:425>	reg <427:425> PIN11 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
	reg <429:428> PIN11 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <430> PIN11 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <431> PIN11 driver strength selection	0: 1X 1: 2X

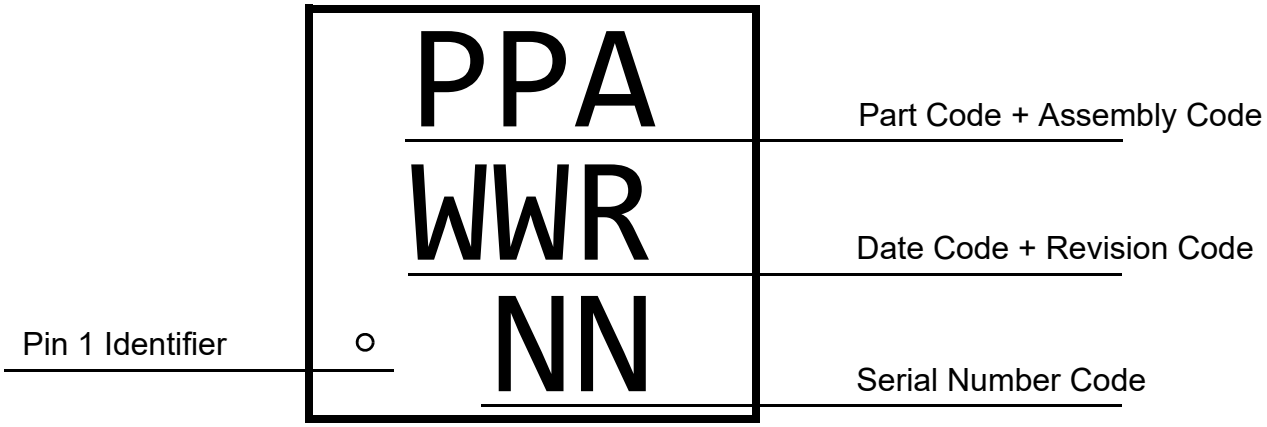
Register Bit Address	Signal Function	Register Bit Definition
PIN 13		
reg <382:379>	reg <380:379> PIN13 mode control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
	reg <382:381> PIN13 pull down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
PIN 14		
reg <389:383>	reg <385:383> PIN14 mode control	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
	reg <387:386> PIN14 pull up/down resistor value selection	00: floating 01: 10K 10: 100K 11: 1M
	reg <388> PIN14 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
	reg <389> PIN14 driver strength selection	0: 1X 1: 2X
PIN15		
reg <410:404>	reg <406:404> PIN15 mode control	000: Digital Input without Schmitt trigger 001: Reserved 010: Reserved 011: Reserved 100: Push Pull 101: Reserved 110: Reserved 111: Reserved
	reg <408:407> PIN15 pull up/down resistor value selection	00: Reserved 01: Reserved 10: Reserved 11: Reserved
	reg <409> PIN15 pull up/down resistor select	0: Reserved 1: Reserved
	reg <410> PIN15 driver strength selection	0: Reserved 1: 2X

Register Bit Address	Signal Function	Register Bit Definition
PIN16		
reg <417:411>	reg <413:411> PIN16 mode control	000: Digital Input without Schmitt trigger 001: Reserved 010: Reserved 011: Reserved 100: Push Pull 101: Reserved 110: Reserved 111: Reserved
	reg <415:414> PIN16 pull down resistor value selection	00: Reserved 01: Reserved 10: Reserved 11: Reserved
	reg <416> PIN16 pull up/down resistor select	0: Reserved 1: Reserved
	reg <417> PIN16 driver strength selection	0: Reserved 1: 2X
reg <432>	Pipe Delay OUT1 polarity select bit	0: non-inverting 1: inverting
reg <440:433>	8-bit pattern id	8-bit pattern id
reg <441>	filter0 output polarity select	0: non-inverting 1: inverting
reg <443:442>	Reserved Reserved	
reg <444>	GPIO quick charge enable	0: Disable 1: Enable
reg <445>	Force bandgap on	0: Auto-mode 1: Enable
reg <446>	VREF Output Active Buffer Control	0: Disabled 1: Enabled
reg <449:447>	VREF Output Source Select	000: ACMP0 reference voltage 001: ACMP1 reference voltage 100: $V_{DD}/2$ 101: $V_{DD}/3$ 110: $V_{DD}/4$ 011: Reserved 010: Reserved 111: Reserved
reg <450>	NVM data read disable	0: Disable (read enable) 1: Enable (read disable)
reg <451>	NVM power down (or NVM data programming disable)	0: None (or programming enable) 1: Power Down (or programming disable)
reg <452>	Power Divider Power	0: Power down 1: Power On
reg <453>	POR Auto Power detect	0: Enable 1: Disable
reg <454>	Charge pump for analog macrocell enable (when V_{DD} <= 2.7 V turn on)	0: Disable (automatic on/off control) 1: Enable (always on)
reg <455>	V_{DD} bypass enable	0: Regulator auto on 1: Regulator off (V_{DD} bypass)
reg <471:456>	Reserved	Reserved
reg <479:472>	Reserved	Reserved

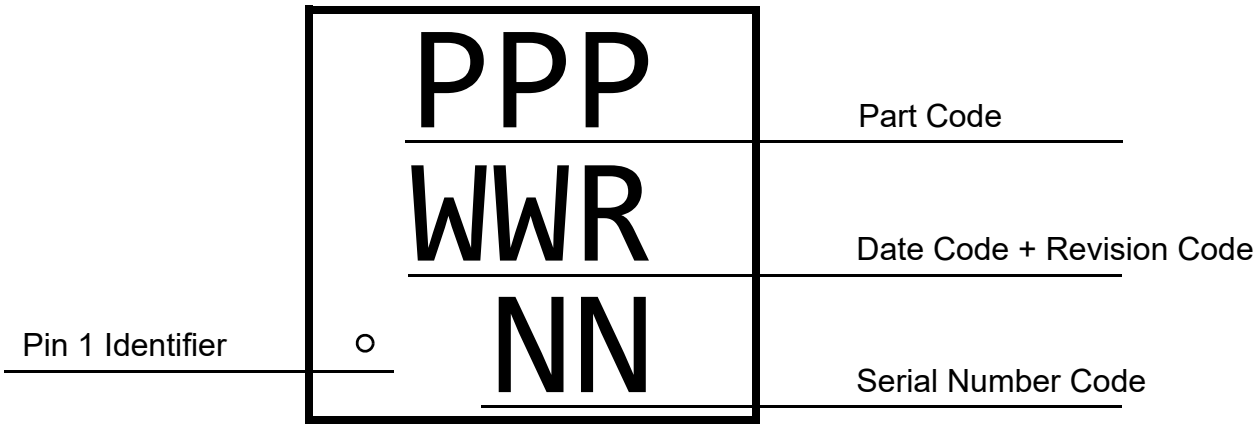
Register Bit Address	Signal Function	Register Bit Definition
reg <481:480>	Reserved	Reserved
reg <482>	PIN13 edge detect mode	0: rising edge 1: falling edge
reg <483>	Bypass the PIN13	0: PIN13 edge active 1: PIN13 high active
reg <484>	PIN13 reset enable	0: Disable 1: Enable
reg <485>	programmable Delay or filter output select	0: programmable Delay output 1: filter output
reg <487:486>	Select the edge mode of programmable Delay & edge detector	00: rising edge detector 01: falling edge detector 10: both edge detector 11: both edge Delay
reg <489:488>	Delay value select for programmable Delay & edge detector (V_{DD} = 3.3 V, typical condition)	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
reg <490>	Reserved	Reserved
reg <495:491>	Reserved	Reserved
reg <501:496>	Reserved	Reserved
reg <502>	Reserved	
reg <503>	Reserved	Reserved
reg <511:504>	Reserved	Reserved

19.0 Package Top Marking System Definition

19.1 Before February 1, 2021



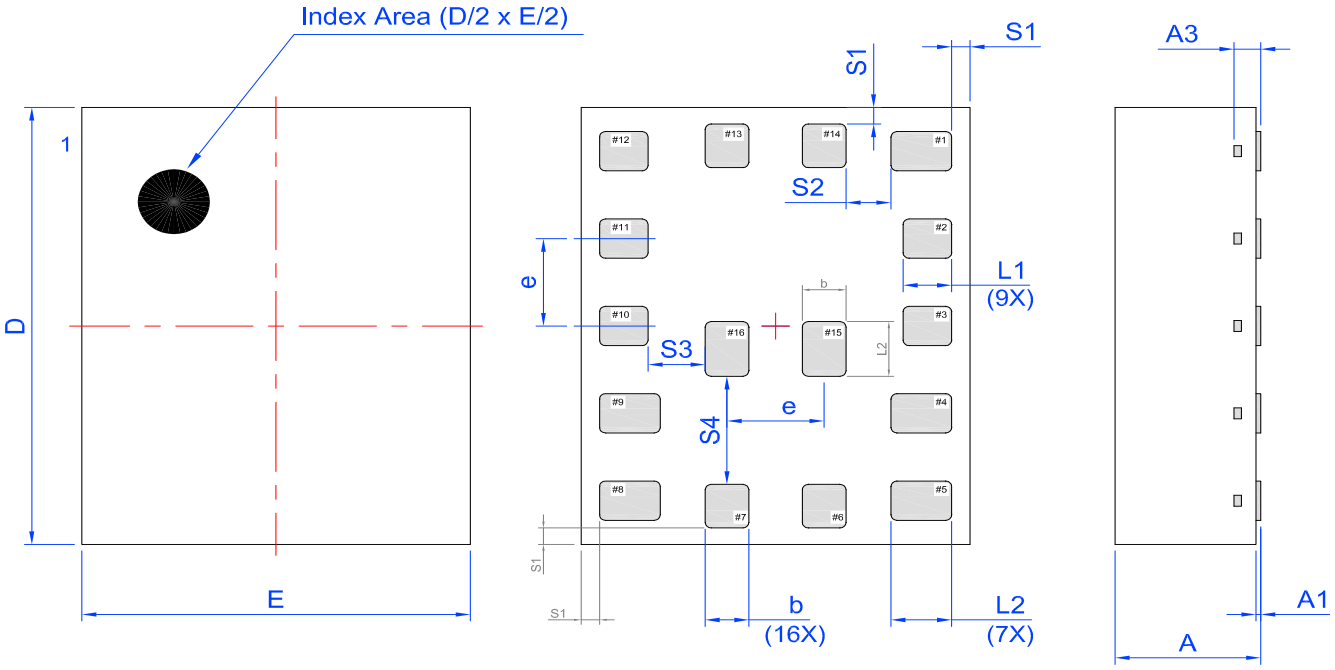
19.2 After February 1, 2021



20.0 Package Drawing and Dimensions

16 Lead MSTQFN Package 1.6 x 2 mm
JEDEC MO-252
IC Net Weight: 0.059 g

MSTQFN 16L 1.6x2mm 0.4P FC Green PKG



Marking View **BTM View** **SIDE View**

Unit: mm

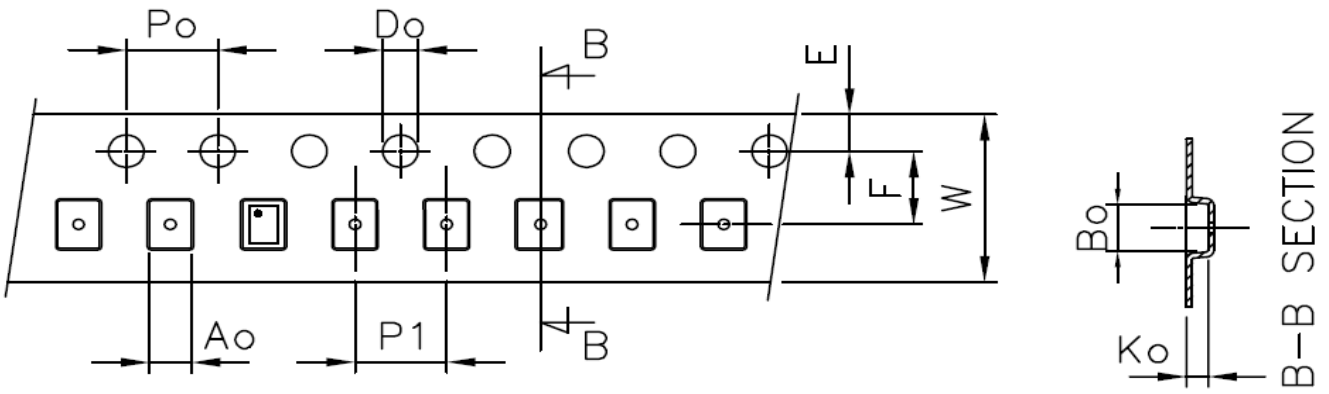
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	1.950	2.000	2.050
A1	0.00	-	0.010	E	1.550	1.600	1.650
A3	0.11 REF			L1	0.150	0.200	0.250
b	0.130	0.180	0.230	L2	0.200	0.250	0.300
e	0.400 BSC			S3	0.235 REF		
S1	0.075 REF			S4	0.495 REF		
S2	0.185 REF						

21.0 Tape and Reel Specifications

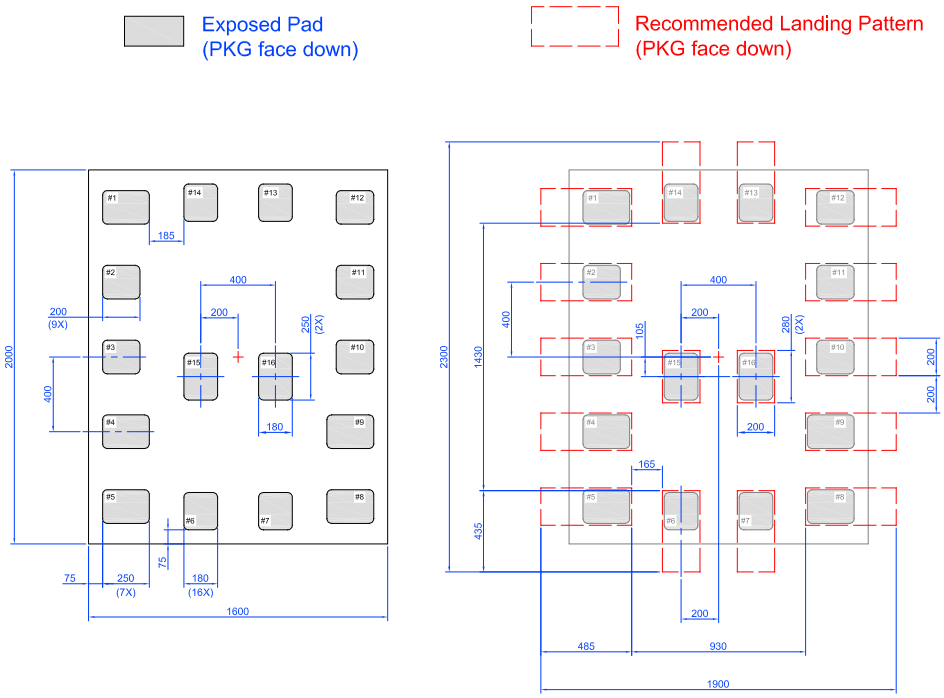
Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
MSTQFN 16L 1.6x2.0 mm FC 0.4P Green	16	1.6x2x0.55	3000	3000	178/60	100	400	100	400	8	4

22.0 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
MSTQFN 16L 1.6x2.0 mm FC 0.4P Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



23.0 Recommended Landing Pattern



Marking View

Unit:um

24.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

25.0 Revision History

Date	Version	Change
8/14/2023	1.11	Updated tables Electrical Characteristics Fixed typos
3/10/2023	1.10	Added notes to section Ordering Information
3/4/2022	1.09	Updated Pull Up/Down Resistance in Electrical Characteristics Renesas rebranding Updated tables CNT/DLY Register Settings Corrected registers [296:289], [325:318], [339:332], [353:346] in Appendix A - SLG46127 Register Definition
2/2/2021	1.08	Updated section Package Top Marking System Definition Added note for CNTs Corrected registers [353:343], [339:329], [325:315], [296:286]
10/29/2019	1.07	Updated last page with disclaimer and contacts Added pre front page
7/2/2019	1.06	Updated I_{DSS} in Table 6 Fixed typos
12/20/2017	1.05	Corrected subsection Driving the P-FET Switch
12/11/2017	1.04	Updated Dual, 2A P-FET Power Switches
12/4/2017	1.03	Fixed typos
10/10/2017	1.02	Updated Electrical Spec Changed Programmable Delay/ Deglitch Filter Section Structure Fixed typos
9/28/2017	1.01	Updated Power On Pins Settings Fixed typos Updated Power Switch Electrical Characteristics (each P-FET) Updated Absolute Maximum Conditions Updated Dual, 2A P-FET Power Switches
9/15/2017	1.00	Production Release Updated Power Switch Electrical Characteristics (each P-FET)

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