SLG46535-EV

GreenPAK Programmable Mixed-Signal Matrix
with Asynchronous State Machine, Dual Supply, and Extended Temperature Range

The SLG46535-EV provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the IO pins, and the macrocells of the SLG46535-EV. This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

The additional power supply (V_{DD2}) on the SLG46535-EV provides the ability to interface two independent voltage domains within the same design. Users can configure pins, dedicated to each power supply, as inputs, outputs, or both (controlled dynamically by internal logic) to both V_{DD} and V_{DD2} voltage domains. Using the available macrocells, designers can implement Mixed-Signal functions bridging both domains or simply pass through level-translation in both High to Low and Low to High directions.

Features

- Three Analog Comparators (ACMP)
- Nineteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Continuous DFF/LATCH or 3-bit LUT
  - Four Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Function Generator or 2-bit LUT
  - Five 8-bit Delays/Counters or 3-bit LUTs
  - Two 16-bit Delays/Counters or 4-bit LUTs
  - Two Deglitch Filters with Edge Detectors
- Asynchronous State Machine
  - Eight States
  - Flexible Input Logic from State Transitions
- Serial Communications
  - I^2C Protocol Compliant
- Pipe Delay – 16 Stage/3 Output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Function
  - One Inverter
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 25 MHz Oscillator
- Power-On-Reset (POR)
- Eight Byte RAM + OTP User Memory
  - RAM Memory Space that is Readable and Writable via I^2C
  - User Defined Initial Values Transferred from OTP
- Logic and Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5 %) to 5.0 V (±10 %) V_{DD}
- 1.8 V (±5 %) to 5.0 V (±10 %) V_{DD2} ($V_{DD2} \leq V_{DD}$)
- Ambient Operating Temperature Range: -40 °C to +105 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - 14-pin STQFN: 2.0 mm x 2.2 mm x 0.55 mm, 0.4 mm Pitch

Applications

- Outdoors Electronics
- Factory Automation
- Servers and Networking Equipment
- Chargers

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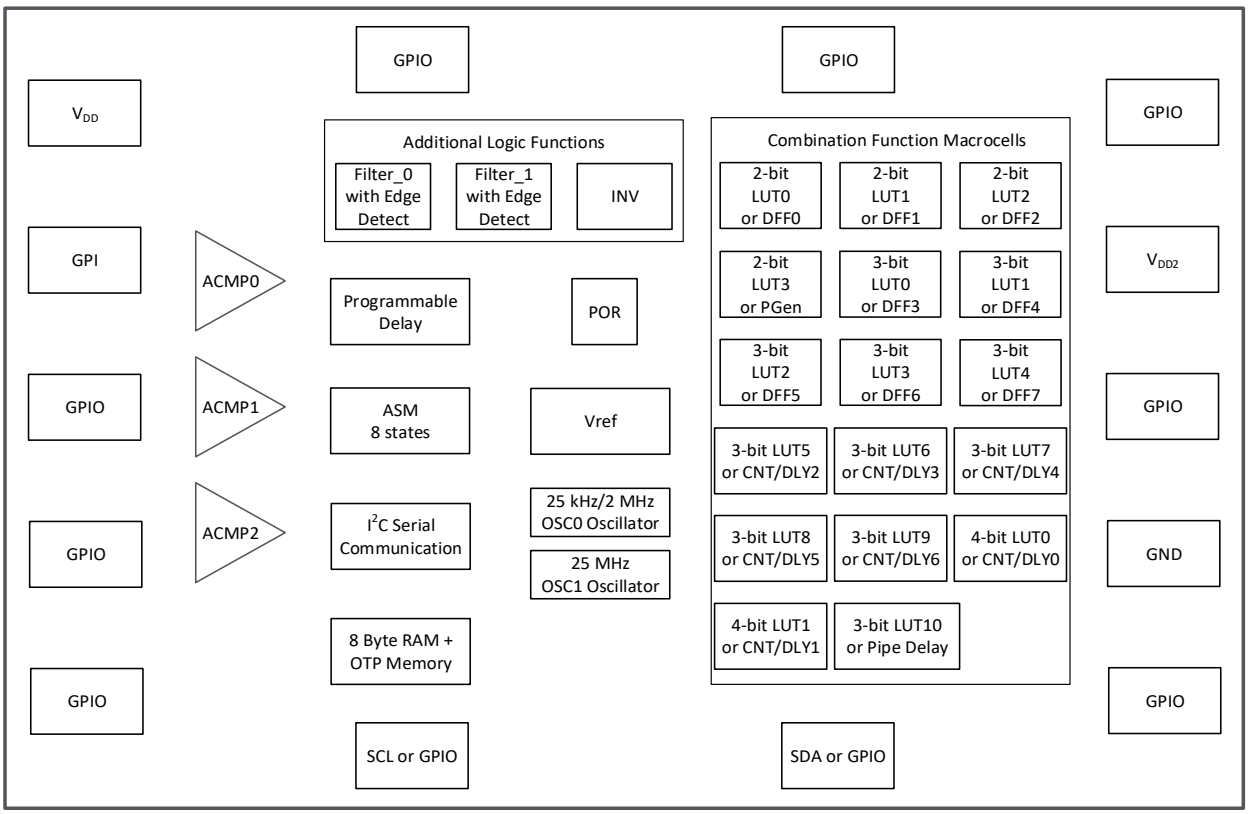


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

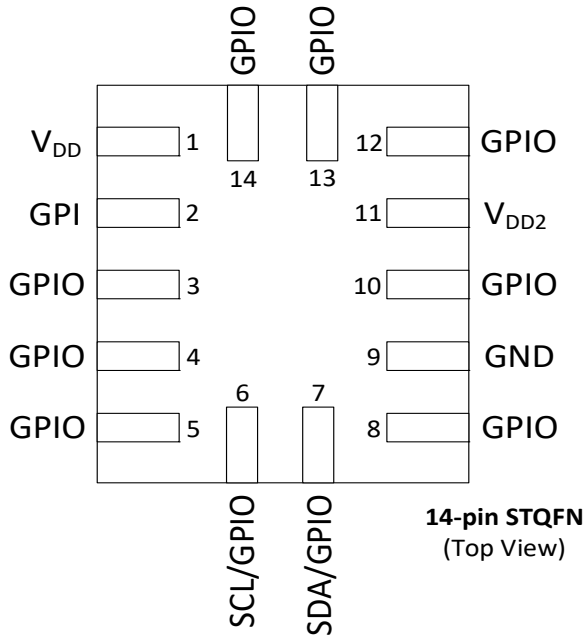


Figure 2. Pin Assignments - STQFN-14 (Top View)

2.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Description
1	V_{DD}	Power Supply 1
2	GPI	General Purpose Input
3	GPIO	General Purpose IO
4	GPIO	General Purpose IO or Analog Comparator 0 (+)
5	GPIO	General Purpose IO with OE or Analog Comparator 0 (-)
6	SCL/GPIO	General Purpose IO SCL or GPIOD (NMOS Open-Drain Only)
7	SDA/GPIO	General Purpose IO SDA or GPIOD (NMOS Open-Drain Only)
8	GPIO	General Purpose IO with OE or Analog Comparator 1 (+)
9	GND	Ground
10	GPIO	General Purpose IO or Analog Comparator 1 (-)
11	V_{DD2}	Power Supply 2
12	GPIO	General Purpose IO with OE
13	GPIO	General Purpose IO
14	GPIO	General Purpose IO or External Clock Input

Table 2. Pin Type Definitions

Pin Type	Definition
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GND	General Ground
SCL	I^2C Clock Input
SDA	I^2C Data Input
V_{DD}	Power Supply
V_{DD2}	Power Supply 2

Table 3. Functional Pin Description

STQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DD}	V_{DD}	Power Supply	--	--
2	GPI	GPI	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
3	GPIO	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
4	GPIO	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
5	GPIO	GPIO	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		EXT_V_{REF}	Analog Comparator 0 Negative Input	Analog	--

Table 3. Functional Pin Description (Cont.)

STQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
6	SCL/GPIO	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
7	SDA/GPIO	SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
8	GPIO	GPIO	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
				Low Voltage Digital Input	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
9	GND	GND	Ground	--	--
10	GPIO	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		EXT_V_{REF}	Analog Comparator 1 Negative Input	Analog	--
11	V_{DD2}	V_{DD2}	Power Supply 2	--	--

Table 3. Functional Pin Description (Cont.)

STQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
12	GPIO	GPIO	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
13	GPIO	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
14	GPIO	GPIO	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)

[1] General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Parameter		Min	Max	Unit
Supply voltage on V_{DD} relative to GND		-0.5	7.0	V
Supply voltage on V_{DD2} relative to GND		-0.5	V_{DD} + 0.5	V
DC Input voltage	Pins 2, 6, 7	GND - 0.5	7.0	V
	Pins 3, 4, 5, 8		V_{DD} + 0.5, up to 7.0	
	Pins 10, 12, 13, 14		V_{DD2} + 0.5, up to 7.0	
V_{DD} DC Current	T_J = +85 °C	--	45	mA
	T_J = +110 °C	--	22	mA
V_{DD2} DC Current	T_J = +85 °C	--	45	mA
	T_J = +110 °C	--	22	mA
GND DC Current	T_J = +85 °C	--	86	mA
	T_J = +110 °C	--	41	mA
GPIO DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	+150	°C
Junction Temperature		--	+150	°C
Moisture Sensitivity Level		1		

3.2 Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	500	--	V

3.3 Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		1.71	5.5	V
Supply Voltage 2 (V_{DD2})	$V_{DD2} \leq V_{DD}$	1.71	V_{DD}	V
Operating Ambient Temperature Range		-40	+105	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 Electrical Specifications

3.4.1 Logic IO Specifications

T_A = -40 °C to +105 °C, V_{DD} = 1.71 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ACMP Input Voltage Range	V_{ACMP}	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
HIGH-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8	V_{IH}	Logic Input [1]	0.7 x V_{DD} [2]	--	V_{DD}+ 0.3 [2]	V
		Logic Input with Schmitt Trigger	0.8 x V_{DD} [2]	--	V_{DD}+ 0.3 [2]	V
		Low-Level Logic Input [1]	1.25	--	V_{DD}+ 0.3 [2]	V
LOW-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8	V_{IL}	Logic Input [1]	GND - 0.3	--	0.3 x V_{DD} [2]	V
		Logic Input with Schmitt Trigger	GND - 0.3	--	0.2 x V_{DD} [2]	V
		Low-Level Logic Input [1]	GND - 0.3	--	0.5	V
Schmitt Trigger Hysteresis Voltage PINs 2, 3, 4, 5, 6, 7, 8	V_{HYS}	Logic Input with Schmitt Trigger, V_{DD} = 1.8 V ± 5 %	0.19 x V_{DD}	0.26 x V_{DD}	0.31 x V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD} = 3.3 V ± 10 %	0.16 x V_{DD}	0.21 x V_{DD}	0.26 x V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD} = 5.0 V ± 10 %	0.15 x V_{DD}	0.18 x V_{DD}	0.22 x V_{DD}	V
Input leakage (Absolute Value)	I_{LKG}		--	--	1000	nA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8	V_{OH}	Push-Pull, I_{OH} = 100 µA, 1x Drive, V_{DD} = 1.8 V ± 5 %	0.992 x V_{DD}	0.994 x V_{DD}	--	V
		Push-Pull, I_{OH} = 3 mA, 1x Drive, V_{DD} = 3.3 V ± 10 %	0.931 x V_{DD}	0.948 x V_{DD}	--	V
		Push-Pull, I_{OH} = 5 mA, 1x Drive, V_{DD} = 5.0 V ± 10 %	0.945 x V_{DD}	0.958 x V_{DD}	--	V
		PMOS OD, I_{OH} = 100 µA, 1x Drive, V_{DD} = 1.8 V ± 5 %	0.992 x V_{DD}	0.99 x V_{DD}	--	V
		PMOS OD, I_{OH} = 3 mA, 1x Drive, V_{DD} = 3.3 V ± 10 %	0.931 x V_{DD}	0.95 x V_{DD}	--	V
		PMOS OD, I_{OH} = 5 mA, 1x Drive, V_{DD} = 5.0 V ± 10 %	0.945 x V_{DD}	0.96 x V_{DD}	--	V
		Push-Pull, I_{OH} = 100 µA, 2x Drive, V_{DD} = 1.8 V ± 5 %	0.996 x V_{DD}	0.997 x V_{DD}	--	V
		Push-Pull, I_{OH} = 3 mA, 2x Drive, V_{DD} = 3.3 V ± 10 %	0.966 x V_{DD}	0.974 x V_{DD}	--	V
		Push-Pull, I_{OH} = 5 mA, 2x Drive, V_{DD} = 5.0 V ± 10 %	0.972 x V_{DD}	0.979 x V_{DD}	--	V
		PMOS OD, I_{OH} = 100 µA, 2x Drive, V_{DD} = 1.8 V ± 5 %	0.996 x V_{DD}	0.997 x V_{DD}	--	V
		PMOS OD, I_{OH} = 3 mA, 2x Drive, V_{DD} = 3.3 V ± 10 %	0.966 x V_{DD}	0.974 x V_{DD}	--	V
		PMOS OD, I_{OH} = 5 mA, 2x Drive, V_{DD} = 5.0 V ± 10 %	0.972 x V_{DD}	0.979 x V_{DD}	--	V
LOW-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8	V_{OL}	Push-Pull, I_{OL}= 100 µA, 1x Drive, V_{DD} = 1.8 V ± 5 %	--	0.004 x V_{DD}	0.006 x V_{DD}	V
		Push-Pull, I_{OL}= 3 mA, 1x Drive, V_{DD} = 3.3 V ± 10 %	--	0.038 x V_{DD}	0.054 x V_{DD}	V
		Push-Pull, I_{OL}= 5 mA, 1x Drive, V_{DD} = 5.0 V ± 10 %	--	0.033 x V_{DD}	0.046 x V_{DD}	V
		Push-Pull, I_{OL} = 100 µA, 2x Drive, V_{DD} = 1.8 V ± 5 %	--	0.002 x V_{DD}	0.003 x V_{DD}	V
		Push-Pull, I_{OL} = 3 mA, 2x Drive, V_{DD} = 3.3 V ± 10 %	--	0.019 x V_{DD}	0.026 x V_{DD}	V
		Push-Pull, I_{OL} =5 mA, 2x Drive, V_{DD} = 5.0 V ± 10 %	--	0.017 x V_{DD}	0.023 x V_{DD}	V
		NMOS Open-Drain, I_{OL} = 100 µA, 1x Drive, V_{DD} = 1.8 V ± 5 %	--	0.003 x V_{DD}	0.004 x V_{DD}	V
		NMOS Open-Drain, I_{OL} = 3 mA, 1x Drive, V_{DD} = 3.3 V ± 10 %	--	0.025 x V_{DD}	0.035 x V_{DD}	V
		NMOS Open-Drain, I_{OL} = 5 mA, 1x Drive, V_{DD} = 5.0 V ± 10 %	--	0.022 x V_{DD}	0.03 x V_{DD}	V
		NMOS Open-Drain, I_{OL} = 100 µA, 2x Drive, V_{DD} = 1.8 V ± 5 %	--	0.002 x V_{DD}	0.002 x V_{DD}	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LOW-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8	V_{OL}	NMOS Open-Drain, I_{OL} = 3 mA, 2x Drive, V_{DD} = 3.3 V ± 10 %	--	0.013 x V_{DD}	0.018 x V_{DD}	V
		NMOS Open-Drain, I_{OL} = 5 mA, 2x Drive, V_{DD} = 5.0 V ± 10 %	--	0.011 x V_{DD}	0.015 x V_{DD}	V
		Open-Drain NMOS 4x, PIN 8, I_{OL} = 100 µA, V_{DD} = 1.8 V ± 5 %	--	0.001 x V_{DD}	0.001 x V_{DD}	V
		Open-Drain NMOS 4x, PIN 8, I_{OL} = 3 mA, V_{DD} = 3.3 V ± 10 %	--	0.007 x V_{DD}	0.009 x V_{DD}	V
		Open-Drain NMOS 4x, PIN 8, I_{OL} = 5 mA, V_{DD} = 5.0 V ± 10 %	--	0.006 x V_{DD}	0.008 x V_{DD}	V
HIGH-Level Output Pulse Current [3] PINs 2, 3, 4, 5, 6, 7, 8	I_{OH}	Push-Pull, V_{OH} = V_{DD} - 0.2, 1x Drive, V_{DD} = 1.8 V ± 5 %	0.963	1.331	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1x Drive, V_{DD} = 3.3 V ± 10 %	5.219	12.234	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1x Drive, V_{DD} = 5.0 V ± 10 %	19.403	32.766	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1x Drive, V_{DD} = 1.8 V ± 5 %	0.973	1.331	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1x Drive, V_{DD} = 3.3 V ± 10 %	5.243	12.234	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1x Drive, V_{DD} = 5.0 V ± 10 %	19.478	32.771	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2x Drive, V_{DD} = 1.8 V ± 5 %	1.902	2.642	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2x Drive, V_{DD} = 3.3 V ± 10 %	10.29	24.137	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 5.0 V ± 10 %	37.967	64.23	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2x Drive, V_{DD} = 1.8 V ± 5 %	1.926	3.643	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2x Drive, V_{DD} = 3.3 V ± 10 %	10.389	24.148	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2x Drive, V_{DD} = 5.0 V ± 10 %	38.275	64.275	--	mA
LOW-Level Output Pulse Current [3] PINs 2, 3, 4, 5, 6, 7, 8	I_{OL}	Push-Pull, V_{OL} = 0.15 V, 1x Drive, V_{DD} = 1.8 V ± 5 %	0.92	1.562	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1x Drive, V_{DD} = 3.3 V ± 10 %	4.769	7.847	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1x Drive, V_{DD} = 5.0 V ± 10 %	6.364	10.359	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2x Drive, V_{DD} = 1.8 V ± 5 %	1.83	3.114	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2x Drive, V_{DD} = 3.3 V ± 10 %	9.537	15.515	--	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LOW-Level Output Pulse Current [3] PINs 2, 3, 4, 5, 6, 7, 8	I_{OL}	Push-Pull, V_{OL} = 0.4 V, 2x Drive, V_{DD} = 5.0 V ± 10 %	12.669	20.367	--	mA
		NMOS Open-Drain, V_{OL} = 0.15 V, 1x Drive, V_{DD} = 1.8 V ± 5 %	1.38	2.37	--	mA
		NMOS Open-Drain, V_{OL} = 0.4 V, 1x Drive, V_{DD} = 3.3 V ± 10 %	7.31	11.873	--	mA
		NMOS Open-Drain, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5.0 V ± 10 %	9.825	15.654	--	mA
		NMOS Open-Drain, V_{OL} = 0.15 V, 2x Drive, V_{DD} = 1.8 V ± 5 %	2.75	4.644	--	mA
		NMOS Open-Drain, V_{OL} = 0.4 V, 2x Drive, V_{DD} = 3.3 V ± 10 %	14.472	22.973	--	mA
		NMOS Open-Drain, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5.0 V ± 10 %	17.34	30.033	--	mA
		Open-Drain NMOS 4x, PIN 8, V_{OL} = 0.15 V, V_{DD} = 1.8 V ± 5 %	6.897	9.202	--	mA
		Open-Drain NMOS 4x, PIN 8, V_{OL} = 0.4 V, V_{DD} = 3.3 V ± 10 %	28.502	45.065	--	mA
		Open-Drain NMOS 4X, PIN 8, V_{OL} = 0.4 V, V_{DD} = 5.0 V ± 10 %	37.33	58.499	--	mA
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	0.61	1.311	1.913	ms
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip	0.852	1.553	1.715	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip	0.879	1.167	1.405	V
Pull-up or Pull-down Resistance	R_{PULL}	1 MΩ Pull-up: V_{IN} = GND, 1 MΩ Pull-down: V_{IN} = V_{DD}	--	1000	--	kΩ
		100 kΩ Pull-up: V_{IN} = GND, 100 kΩ Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 kΩ Pull-up: V_{IN} = GND, 10 kΩ Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
Input Capacitance	C_{IN}		--	4	--	pF

[1] No hysteresis.
[2] The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, and 8 are connected to one side, Pins 10, 12, 13, 14 to another.
[3] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

T_A = -40 °C to +105 °C, V_{DD} = 5.5 V, V_{DD2} = 1.71 V to 5.5 V unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ACMP Input Voltage Range	V_{ACMP}	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
HIGH-Level Input Voltage PINs 10, 12, 13, 14	V_{IH2}	Logic Input [1]	0.7 x V_{DD2} [2]	--	V_{DD2} + 0.3 [2]	V
		Logic Input with Schmitt Trigger	0.8 x V_{DD2} [2]	--	V_{DD2} + 0.3 [2]	V
		Low-Level Logic Input [1]	1.25	--	V_{DD2} + 0.3 [2]	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LOW-Level Input Voltage PINs 10, 12, 13, 14	V_{IL2}	Logic Input [1]	GND - 0.3	--	0.3 x V_{DD2} [2]	V
		Logic Input with Schmitt Trigger	GND - 0.3	--	0.2 x V_{DD2} [2]	V
		Low-Level Logic Input [1]	GND - 0.3	--	0.5	V
Schmitt Trigger Hysteresis Voltage PINs 10, 12, 13, 14	V_{HYS2}	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V ± 5 %	0.19 x V_{DD2}	0.256 x V_{DD2}	0.31 x V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V ± 10 %	0.16 x V_{DD2}	0.2 x V_{DD2}	0.24 x V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 5.0 V ± 10 %	0.15 x V_{DD2}	0.183 x V_{DD2}	0.21 x V_{DD2}	V
Input leakage (Absolute Value)	I_{LKG2}		--	--	1000	nA
HIGH-Level Output Voltage PINs 10, 12, 13, 14	V_{OH2}	Push-Pull, I_{OH2} = 100 µA, 1x Drive, V_{DD2} = 1.8 V ± 5 %	0.992 x V_{DD2}	0.994 x V_{DD2}	--	V
		Push-Pull, I_{OH2} = 3 mA, 1x Drive, V_{DD2} = 3.3 V ± 10 %	0.931 x V_{DD2}	0.949 x V_{DD2}	--	V
		Push-Pull, I_{OH2} = 3 mA, 1x Drive, V_{DD2} = 5.0 V ± 10 %	0.968 x V_{DD2}	0.975 x V_{DD2}	--	V
		PMOS OD, I_{OH2} = 100 µA, 1x Drive, V_{DD2} = 1.8 V ± 5 %	0.992 x V_{DD2}	0.994 x V_{DD2}	--	V
		PMOS OD, I_{OH2} = 3 mA, 1x Drive, V_{DD2} = 3.3 V ± 10 %	0.931 x V_{DD2}	0.949 x V_{DD2}	--	V
		PMOS OD, I_{OH2} = 3 mA, 1x Drive, V_{DD2} = 5.0 V ± 10 %	0.968 x V_{DD2}	0.975 x V_{DD2}	--	V
		Push-Pull, I_{OH2} = 100 µA, 2x Drive, V_{DD2} = 1.8 V ± 5 %	0.996 x V_{DD2}	0.997 x V_{DD2}	--	V
		Push-Pull, I_{OH2} = 3 mA, 2x Drive, V_{DD2} = 3.3 V ± 10 %	0.966 x V_{DD2}	0.974 x V_{DD2}	--	V
		Push-Pull, I_{OH2} = 3 mA, 2x Drive, V_{DD2} = 5.0 V ± 10 %	0.984 x V_{DD2}	0.987 x V_{DD2}	--	V
		PMOS OD, I_{OH2} = 100 µA, 2x Drive, V_{DD2} = 1.8 V ± 5 %	0.996 x V_{DD2}	0.997 x V_{DD2}	--	V
		PMOS OD, I_{OH2} = 3 mA, 2x Drive, V_{DD2} = 3.3 V ± 10 %	0.966 x V_{DD2}	0.974 x V_{DD2}	--	V
		PMOS OD, I_{OH2} = 3 mA, 2x Drive, V_{DD2} = 5.0 V ± 10 %	0.984 x V_{DD2}	0.987 x V_{DD2}	--	V
LOW-Level Output Voltage PINs 10, 12, 13, 14	V_{OL2}	Push-Pull, I_{OL2} = 100 µA, 1x Drive, V_{DD2} = 1.8 V ± 5 %	--	0.004 x V_{DD2}	0.005 x V_{DD2}	V
		Push-Pull, I_{OL2} = 3 mA, 1x Drive, V_{DD2} = 3.3 V ± 10 %	--	0.038 x V_{DD2}	0.053 x V_{DD2}	V
		Push-Pull, I_{OL2} = 3 mA, 1x Drive, V_{DD2} = 5.0 V ± 10 %	--	0.020 x V_{DD2}	0.027 x V_{DD2}	V
		Push-Pull, I_{OL2} = 100 µA, 2x Drive, V_{DD2} = 1.8 V ± 5 %	--	0.002 x V_{DD2}	0.003 x V_{DD2}	V
		Push-Pull, I_{OL2} = 3 mA, 2x Drive,V_{DD2} = 3.3 V ± 10 %	--	0.019 x V_{DD2}	0.026 x V_{DD2}	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LOW-Level Output Voltage PINs 10, 12, 13, 14	V_{OL2}	Push-Pull, I_{OL2} = 3 mA, 2x Drive, V_{DD2} = 5.0 V ± 10 %	--	0.01 x V_{DD2}	0.014 x V_{DD2}	V
		NMOS Open-Drain, I_{OL2} = 100 µA, 1x Drive, V_{DD2} = 1.8 V ± 5 %	--	0.003 x V_{DD2}	0.004 x V_{DD2}	V
		NMOS Open-Drain, I_{OL2} = 3 mA, 1x Drive, V_{DD2} = 3.3 V ± 10 %	--	0.025 x V_{DD2}	0.035 x V_{DD2}	V
		NMOS Open-Drain, I_{OL2} = 3 mA, 1x Drive, V_{DD2} = 5.0 V ± 10 %	--	0.013 x V_{DD2}	0.018 x V_{DD2}	V
		NMOS Open-Drain, I_{OL2} = 100 µA, 2x Drive, V_{DD2} = 1.8 V ± 5 %	--	0.002 x V_{DD2}	0.002 x V_{DD2}	V
		NMOS Open-Drain, I_{OL2} = 3 mA, 2x Drive, V_{DD2} = 3.3 V ± 10 %	--	0.013 x V_{DD2}	0.018 x V_{DD2}	V
		NMOS Open-Drain, I_{OL2} = 3 mA, 2x Drive, V_{DD2} = 5.0 V ± 10 %	--	0.006 x V_{DD2}	0.009 x V_{DD2}	V
		Open-Drain NMOS 4x, PIN 10, I_{OL2} = 100 µA, V_{DD2} = 1.8 V ±5 %	--	0.001 x V_{DD2}	0.001 x V_{DD2}	V
		Open-Drain NMOS 4x, PIN 10, I_{OL2} = 3 mA, V_{DD2} = 3.3 V ± 10 %	--	0.007 x V_{DD2}	0.009 x V_{DD2}	V
		Open-Drain NMOS 4x, PIN 10, I_{OL2} = 3 mA, V_{DD2} = 5.0 V ± 10 %	--	0.003 x V_{DD2}	0.005 x V_{DD2}	V
HIGH-Level Output Pulse Current [3] PINs 10, 12, 13, 14	I_{OH2}	Push-Pull, V_{OH2} = V_{DD2} - 0.2, 1x Drive, V_{DD2} = 1.8 V ± 5 %	0.96	1.33	--	mA
		Push-Pull, V_{OH2} = 2.4 V, 1x Drive, V_{DD2} = 3.3 V ± 10 %	5.21	12.31	--	mA
		Push-Pull, V_{OH2} = 2.4 V, 1x Drive, V_{DD2} = 5.0 V ± 10 %	19.41	32.95	--	mA
		PMOS OD, V_{OH2} = V_{DD2} - 0.2, 1x Drive, V_{DD2} = 1.8 V ± 5 %	0.97	1.34	--	mA
		PMOS OD, V_{OH2} = 2.4 V, 1x Drive, V_{DD2} = 3.3 V ± 10 %	5.21	12.32	--	mA
		PMOS OD, V_{OH2} = 2.4 V, 1x Drive, V_{DD2} = 5.0 V ± 10 %	19.42	32.97	--	mA
		Push-Pull, V_{OH2} = V_{DD2} - 0.2, 2x Drive, V_{DD2} = 1.8 V ± 5 %	1.92	2.65	--	mA
		Push-Pull, V_{OH2} = 2.4 V, 2x Drive, V_{DD2} = 3.3 V ± 10 %	10.32	24.34	--	mA
		Push-Pull, V_{OH2} = 2.4 V, 2x Drive, V_{DD2} = 5.0 V ± 10 %	38.31	64.76	--	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-Level Output Pulse Current [3] PINs 10, 12, 13, 14	I_{OH2}	PMOS OD, V_{OH2} = V_{DD2} - 0.2, 2x Drive, V_{DD2} = 1.8 V ± 5 %	1.93	2.65	--	mA
		PMOS OD, V_{OH2} = 2.4 V, 2x Drive, V_{DD2} = 3.3 V ± 10 %	10.35	24.35	--	mA
		PMOS OD, V_{OH2} = 2.4 V, 2x Drive, V_{DD2} = 5.0 V ± 10 %	38.39	64.78	--	mA
LOW-Level Output Pulse Current [3] PINs 10, 12, 13, 14	I_{OL2}	Push-Pull, V_{OL2} = 0.15 V, 1x Drive, V_{DD2} = 1.8 V ± 5 %	1.16	1.57	--	mA
		Push-Pull, V_{OL2} = 0.4 V, 1x Drive, V_{DD2} = 3.3 V ± 10 %	4.89	7.87	--	mA
		Push-Pull, V_{OL2} = 0.4 V, 1x Drive, V_{DD2} = 5.0 V ± 10 %	6.50	10.39	--	mA
		Push-Pull, V_{OL2} = 0.15 V, 2x Drive, V_{DD2} = 1.8 V ± 5 %	1.83	3.122	--	mA
		Push-Pull, V_{OL2} = 0.4 V, 2x Drive, V_{DD2} = 3.3 V ± 10 %	9.71	15.572	--	mA
		Push-Pull, V_{OL2} = 0.4 V, 2x Drive, V_{DD2} = 5.0 V ± 10 %	12.871	20.452	--	mA
		NMOS Open-Drain, V_{OL2} = 0.15 V, 1x Drive, V_{DD2} = 1.8 V ± 5 %	1.38	2.372	--	mA
		NMOS Open-Drain, V_{OL2} = 0.4 V, 1x Drive, V_{DD2} = 3.3 V ± 10 %	7.31	11.89	--	mA
		NMOS Open-Drain, V_{OL2} = 0.4 V, 1x Drive, V_{DD2} = 5.0 V ± 10 %	9.902	15.674	--	mA
		NMOS Open-Drain, V_{OL2} = 0.15 V, 2x Drive, V_{DD2} = 1.8 V ± 5 %	2.75	4.651	--	mA
		NMOS Open-Drain, V_{OL2} = 0.4 V, 2x Drive, V_{DD2} = 3.3 V ± 10 %	14.529	23.018	--	mA
		NMOS Open-Drain, V_{OL2} = 0.4 V, 2x Drive, V_{DD2} = 5.0 V ± 10 %	17.34	30.089	--	mA
		Open-Drain NMOS 4x, PIN 10, V_{OL2} = 0.15 V, V_{DD2} = 1.8 V ± 5 %	6.936	9.258	--	mA
		Open-Drain NMOS 4x, PIN 10, V_{OL2} = 0.4 V, V_{DD2} = 3.3 V ± 10 %	29.078	45.594	--	mA
		Open-Drain NMOS 4x, PIN 10, V_{OL2} = 0.4 V, V_{DD2} = 5.0 V ± 10 %	38.252	59.393	--	mA
Power-On Threshold of V_{DD2} Detector	PON_{THR2}	V_{DD2} Level Required to Start Up the Pins Powered from V_{DD2}	0.04	0.6	1.6	V
Power-Off Threshold of V_{DD2} Detector	$POFF_{THR2}$	V_{DD2} Level Required to Switch Off the Pins Powered from V_{DD2}	0.29	0.6	0.7	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pull-up or Pull-down Resistance	R_{PULL2}	1 MΩ Pull-up: V_{IN} = GND, 1 MΩ Pull-down: V_{IN} = V_{DD2}	--	1000	--	kΩ
		100 kΩ Pull-up: V_{IN} = GND, 100 kΩ Pull-down: V_{IN} = V_{DD2}	--	100	--	kΩ
		10 kΩ Pull-up: V_{IN} = GND, 10 kΩ Pull-down: V_{IN} = V_{DD2}	--	10	--	kΩ
Input Capacitance	C_{IN2}		--	4	--	pF

[1] No hysteresis.
[2] The GreenPAK's power rails are divided in two sides. PINs 2, 3, 4, 5, 6, 7, and 8 are connected to one side, PINs 10, 12, 13, and 14 to another.
[3] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.4.2 I²C Pins Electrical Specifications

T_A = -40 °C to +105 °C, V_{DD} = 1.71 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Condition	Fast-Mode		Unit
			Min	Max	
IO Stage					
LOW-level Input Voltage	V_{IL}		-0.5	0.3 x V_{DD}	V
HIGH-level Input Voltage	V_{IH}		0.7 x V_{DD}	V_{DD} + 0.5	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 x V_{DD}	--	V
LOW-Level Output Voltage 1	V_{OL1}	(Open-Drain) at 3 mA sink current, V_{DD} > 2 V	0	0.4	V
LOW-Level Output Voltage 2	V_{OL2}	(Open-Drain) at 2 mA sink current, V_{DD} ≤ 2 V	0	0.2 x V_{DD}	V
LOW-Level Output Current	I_{OL}	V_{OL} = 0.4 V	3	--	mA
		V_{OL} = 0.6 V	6	--	mA
Output Fall Time from V_{IHmin} to V_{ILmax} [1]	t_{of}		0.3	250	ns
Pulse Width of Spikes that must be suppressed by the Input Filter	t_{SP}	SDA line	0	50	ns
		SCL line	0	20 [1]	
Input Current Each IO Pin	I_i	0.1 x V_{DD} < V_I < 0.9 x V_{DDmax}	-10	+10	µA
Capacitance for Each IO Pin	C_i		--	10	pF
Timing (see Figure 116 for Diagram)					
Clock Frequency, SCL	F_{SCL}		--	400	kHz
Clock Pulse Width Low	t_{LOW}		1300	--	ns
Clock Pulse Width High	t_{HIGH}		600	--	ns
Data Valid Acknowledge Time	t_{VD_ACK}		--	900	ns
Data Valid Time	t_{VD_DAT}		--	900	ns
Bus Free Time between Stop and Start	t_{BUF}		1300	--	ns
Start Hold Time	t_{HD_STA}		600	--	ns
Start Set-up Time	t_{SU_STA}		600	--	ns

Parameter	Symbol	Condition	Fast-Mode		Unit
			Min	Max	
Data Hold Time	t_{HD_DAT}		0	--	ns
Data Set-up Time	t_{SU_DAT}		100	--	ns
Inputs Rise Time	t_R		--	300	ns
Inputs Fall Time	t_F		--	300	ns
Stop Set-up Time	t_{SU_STO}		600	--	ns
Data Out Hold Time	t_{DH}		50	--	ns
[1] Does not meet standard I^2C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min), t_{SP} = 50 ns (max).					

3.4.3 Asynchronous State Machine Specifications

T_A = -40 °C to +105 °C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Asynchronous State Machine Output Delay Time	$t_{st\_out\_delay}$	V_{DD} = 1.8 V ± 5 %	148	--	287	ns
		V_{DD} = 3.3 V ± 10 %	60	--	121	
		V_{DD} = 5.0 V ± 10 %	42	--	81	
Asynchronous State Machine Output Transition Time	t_{st_out}	V_{DD} = 1.8 V ± 5 %	--	--	190	ns
		V_{DD} = 3.3 V ± 10 %	--	--	78	
		V_{DD} = 5.0 V ± 10 %	--	--	50	
Asynchronous State Machine Input Pulse Acceptance Time	t_{st_pulse}	V_{DD} = 1.8 V ± 5 %	14	--	--	ns
		V_{DD} = 3.3 V ± 10 %	6	--	--	
		V_{DD} = 5.0 V ± 10 %	5	--	--	
Asynchronous State Machine Input Compete Time	t_{st_comp}	V_{DD} = 1.8 V ± 5 %	--	--	21	ns
		V_{DD} = 3.3 V ± 10 %	--	--	9	
		V_{DD} = 5.0 V ± 10 %	--	--	6	

3.4.4 Macrocells Current Consumption

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD}/V_{DD2} = 1.8 V	V_{DD}/V_{DD2} = 3.3 V	V_{DD}/V_{DD2} = 5.0 V	Unit
Current	I_{DD}	Chip Quiescent, I_{DD1}	0.28	0.52	0.81	µA
		Chip Quiescent, I_{DD2}	0.001	0.002	0.002	
		OSC 2 MHz, pre-divide = 1	32.73	50.92	76.79	
		OSC 2 MHz, pre-divide = 8	19.36	24.90	34.48	
		OSC 25 kHz, pre-divide = 1	5.39	6.11	7.34	
		OSC 25 kHz, pre-divide = 8	5.23	5.79	6.84	
		OSC 25 MHz, pre-divide = 1	76.84	204.45	375.54	
		OSC 25 MHz, pre-divide = 8	68.18	181.65	341.65	
		ACMP (each)	47.22	43.87	51.98	
		ACMP with buffer (each)	62.46	59.52	68.18	
		V_{REF} (each)	43.19	39.78	47.88	
		V_{REF} with buffer (each)	51.88	48.80	57.08	

3.4.5 Estimated Typical Delay of Each Macrocell

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD}/V_{DD2} = 1.8 V		V_{DD}/V_{DD2} = 3.3 V		V_{DD}/V_{DD2} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
GPI and GPIO Macrocell									
Propagation Delay	t_{PD}	Digital Input to PP 1x	46	48	20	20	14	15	ns
		Digital Input with Schmitt Trigger to PP 1x	45	47	19	20	14	14	
		Low Voltage Digital input to PP 1x	51	468	23	186	18	120	
		Digital input to PMOS output	41	-	18	-	13	-	
		Digital input to NMOS output	-	78	-	29	-	19	
		Output enable from pin, OE Hi-Z to 1	46	-	19	-	14	-	
		Output enable from pin, OE Hi-Z to 0	43	-	19	-	14	-	
Pulse Width	t_W	IO with 1x Push-Pull (min transmitted)	20	20	20	20	20	20	ns

Parameter	Symbol	Note	V_{DD}/V_{DD2} = 1.8 V		V_{DD}/V_{DD2} = 3.3 V		V_{DD}/V_{DD2} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Combination Function Macrocell									
Propagation Delay	t_{PD}	2-bit LUT (LATCH)	34	34	14	13	10	9	ns
		LATCH (2-bit LUT)	30	32	12	13	9	9	
		3-bit LUT(LATCH)	31	33	13	13	9	9	
		LATCH+nRESET(3-bit LUT)	37	36	15	14	11	10	
		4-bit LUT	29	35	12	13	9	9	
		2-bit LUT	30	32	12	13	9	9	
		3-bit LUT	31	33	13	13	9	9	
		CNT/DLY Logic	60	60	25	25	17	17	
Programmable Delay									
Propagation Delay	t_{PD}	P_DLY1C	377	369	167	164	123	121	ns
		P_DLY2C	689	682	309	305	229	226	
		P_DLY3C	1002	995	450	447	334	331	
		P_DLY4C	1311	1303	590	586	438	435	
Pipe Delay									
Propagation Delay	t_{PD}	Pipe Delay OUT0	48	42	20	18	14	13	ns
		Pipe Delay OUT1	45	39	19	16	13	12	
Filter/Edge Detector									
Propagation Delay	t_{PD}	Filter 0	225	205	86	80	56	52	ns
		Filter 1	175	156	66	61	43	40	
		Mode: Edge Detect 0, Any Edge Detect	59	63	23	24	16	16	
		Mode: Edge Detect 1, Any Edge Detect	58	62	23	23	16	16	
		Mode: Edge Detect 0, BothEdge Detect	378	366	167	162	123	120	
		Mode: Edge Detect 1, Both Edge Detect	377	364	166	162	122	119	
ACMP									
Propagation Delay	t_{PD}	ACMP (5 mV overdrive, IN- = 600 mV)	3000	3000	2000	2000	2000	2000	ns

3.4.6 Programmable Delay Typical Delays and Widths

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note		V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Pulse Width	t_W	Mode: (any) Edge Detect, Edge Detect Output	1-Cell	309	139	103	ns
			2-Cell	621	280	209	
			3-Cell	934	422	314	
			4-Cell	1243	562	418	
Delay Time	t_{DLY1}	Mode: (any) Edge Detect, Edge Detect Output	1-Cell	55	22	15	ns
			2-Cell	55	22	15	
			3-Cell	55	22	15	
			4-Cell	55	22	15	
	t_{DLY2}	Mode: Both Edge Delay, Edge Detect Output	1-Cell	373	165	122	ns
			2-Cell	685	307	227	
			3-Cell	998	448	332	
			4-Cell	1307	588	437	

3.4.7 Typical Filter Rejection Pulse Width

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width for Filter 0	< 143	< 58	< 37	ns
Filtered Pulse Width for Filter 1	< 97	< 40	< 26	ns

3.4.8 Counter/Delay Specifications

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	OSC Freq	OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On Delay Time	25 kHz	Auto	1.6	1.6	1.6	µs
Power-On Delay Time (Fast Start)	25 kHz	Auto	2.1	2.1	2.1	µs
Power-On Delay	2 MHz	Auto	0.4	0.2	0.2	µs
Power-On Delay Time (Fast Start)	2 MHz	Auto	0.7	0.5	0.4	µs
Power-On Delay) Time	25 MHz	Auto	0.01	0.05	0.04	µs
Frequency settling time	25 kHz	Auto	19	14	12	µs
	2 MHz	Auto	14	14	14	µs
Variable (CLK period)	25 kHz	Forced	0-40	0-40	0-40	µs
	2 MHz	Forced	0-0.5	0-0.5	0-0.5	µs
	25 MHz	Forced	0-0.04	0-0.04	0-0.04	µs
Propagation Delay (Non-Delayed Edge)	25 kHz/ 2 MHz	Either	35	14	10	ns

3.4.9 25 kHz OSC0 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5 %	24.317	25.726	23.576	26.116	23.576	27.219
3.3 V ±10 %	24.495	25.66	23.6	25.934	23.6	26.399
5.0 V ±10 %	24.443	25.698	23.517	25.978	23.517	26.567
2.5 V to 4.5 V	24.493	25.665	23.59	25.942	23.59	26.408
1.71 V to 5.5 V	24.224	25.698	23.484	26.257	23.484	27.225

3.4.10 25 kHz OSC0 Frequency Error

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-2.732	2.904	-10.7	6.92	-10.7	16.832
3.3 V ±10 %	-2.02	2.64	-10.432	4.772	-10.432	9.66
5.0 V ±10 %	-2.228	2.792	-11.064	4.996	-11.064	10.22
2.5 V to 4.5 V	-2.028	2.66	-10.588	4.844	-10.588	9.848
1.71 V to 5.5 V	-3.104	3.872	-11.536	6.904	-11.536	16.728

3.4.11 2 MHz OSC0 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5 %	1.903	2.098	1.856	2.104	1.856	2.115
3.3 V ±10 %	1.885	2.115	1.839	2.123	1.834	2.132
5.0 V ±10 %	1.858	2.220	1.821	2.230	1.803	2.252
2.5 V to 4.5 V	1.874	2.123	1.835	2.129	1.819	2.137
1.71 V to 5.5 V	1.811	2.249	1.779	2.260	1.623	2.283

3.4.12 2 MHz OSC0 Frequency Error

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-4.85	4.9	-9.15	5.7	-10.35	6.95
3.3 V ±10 %	-5.75	5.75	-9.0	7.05	-11.4	7.65
5.0 V ±10 %	-7.1	11.0	-10.85	12.8	-13.1	14.4
2.5 V to 4.5 V	-6.3	6.15	-9.6	8.0	-13.75	8.2
1.71 V to 5.5 V	-9.45	12.45	-15.45	14.25	-30.5	16.0

3.4.13 25 MHz OSC1 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±10 %	22.964	26.443	21.759	26.828	21.759	27.327
3.3 V ±10 %	24.056	25.824	22.655	26.081	22.655	26.350
5.0 V ±10 %	23.860	25.894	22.832	26.215	22.832	26.714
2.5 V to 4.5 V	22.232	25.824	21.386	26.081	21.386	26.350
1.71 V to 5.5 V	14.130	25.824	13.718	26.081	13.028	26.350

3.4.14 25 MHz OSC1 Frequency Error

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±10 %	-8.144	5.772	-17.804	8.74	-17.804	13.04
3.3 V ±10 %	-3.776	3.296	-14.96	5.904	-14.96	8.556
5.0 V ±10 %	-4.56	3.576	-13.408	6.596	-13.408	10.36
2.5 V to 4.5 V	-11.072	3.296	-20.152	5.904	-20.152	8.768
1.71 V to 5.5 V	-43.48	3.296	-51.088	8.892	-53.848	9.988

Note: 25 MHz OSC1 performance is not guaranteed at V_{DD} < 2.5 V.

3.4.15 OSCs Power-On Delay (Normal Mode)

Note: DLY/CNT Counter Data = 100, OSC Power Setting: "Auto Power-On", OSC Clock to Matrix Input: "Enable".

Typical values are at T_A = +25 °C, unless otherwise specified.

Power Supply Range (V_{DD}) V	OSC0 2 MHz		OSC0 25 kHz		OSC1	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns
1.71	372.7	407.3	0.40	0.57	71.2	87.3
1.80	349.2	379.5	0.38	0.41	65.0	78.7
1.89	330.3	358.0	0.35	0.41	59.7	71.3
2.30	277.2	298.1	0.29	0.31	43.0	54.0
2.50	262.0	281.9	0.28	0.30	39.6	48.1
2.70	250.2	269.8	0.26	0.30	36.7	43.5
3.00	236.6	256.7	0.25	0.44	33.2	39.8
3.30	226.7	247.4	0.23	0.47	30.4	36.8
3.60	219.0	239.9	0.22	0.46	28.2	34.3
4.20	207.4	229.2	0.37	0.50	25.8	30.6
4.50	202.8	224.5	1.63	1.92	25.0	29.2
5.00	196.3	218.7	1.67	2.05	24.3	27.5
5.50	190.8	213.3	1.69	1.99	23.7	26.8

3.4.16 OSCs Power-On Delay (Fast Start-Up Time Mode)

Typical values are at T_A = +25 °C, unless otherwise specified.

Power Supply Range (V_{DD}) V	OSC0 2 MHz		OSC0 25 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
1.71	327.9	360.0	0.68	0.76
1.80	309.9	338.3	0.64	0.64
1.89	295.5	323.1	0.61	0.70
2.30	254.9	278.1	0.53	21.93
2.50	243.1	266.1	3.23	21.88
2.70	234.1	257.1	16.68	21.94
3.00	223.7	246.8	19.25	21.90
3.30	215.7	239.1	19.22	21.77
3.60	209.4	232.9	19.21	21.74
4.20	199.5	223.4	19.17	21.78
4.50	195.5	219.8	19.15	21.69
5.00	189.8	214.6	19.12	21.71
5.50	184.9	209.8	19.05	21.75

3.4.17 ACMP Specifications

T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V, unless otherwise noted.

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
ACMP Input Voltage Range	V_{ACMP}	Positive Input	V_{DD} = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	V_{DD} = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	V_{DD} = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
ACMP Input Offset Voltage	V_{offset}	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, V_{REF} = 50 mV to 1200 mV, V_{DD} = 1.71 V to 5.5 V	T_A = +25 °C	-10.7	--	8.4	mV
			T_A = -40 °C to +105 °C	-10.6	--	7.0	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, V_{REF} = 50 mV to 1200 mV, V_{DD} = 1.71 V to 5.5 V	T_A = +25 °C	-10.2	--	9.1	mV
			T_A = -40 °C to +105 °C	-10.3	--	7.6	mV
ACMP Start Time	t_{start}	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T_A = +25 °C V_{DD} = 1.71 V to 5.5 V	--	672.6	909.0	µs
			BG = 550 µs, T_A = -40 °C to +105 °C V_{DD} = 1.71 V to 5.5 V	--	676.5	1033.8	µs
			BG = 100 µs, T_A = +25 °C V_{DD} = 2.7 V to 5.5 V	--	133.2	181.9	µs
			BG = 100 µs, T_A = -40 °C to +105 °C V_{DD} = 2.7 V to 5.5 V	--	134.7	207.0	µs
ACMP Start Time	t_{start}	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump always OFF	BG = 550 µs, T_A = +25 °C V_{DD} = 3.0 V to 5.5 V	--	673.1	909.0	µs
			BG = 550 µs, T_A = -40 °C to +105 °C V_{DD} = 3.0 V to 5.5 V	--	676.9	1033.8	µs
			BG = 100 µs, T_A = +25 °C V_{DD} = 3.0 V to 5.5 V	--	133.0	181.2	µs
			BG = 100 µs, T_A = -40 °C to +105 °C V_{DD} = 3.0 V to 5.5 V	--	134.4	207.0	µs

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Built-in Hysteresis	V_{HYS}	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T_A = +25 °C	7.32	--	35.5	mV
			LB - Disabled, T_A = +25 °C	10.0	--	38.5	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T_A = +25 °C	42.9	--	57.8	mV
			LB - Disabled, T_A = +25 °C	44.2	--	54.3	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T_A = +25 °C	192.7	--	208.7	mV
			LB - Disabled, T_A = +25 °C	193.3	--	204.8	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled T_A = -40 °C to +105 °C	23.745	--	44.435	mV
			LB - Disabled T_A = -40 °C to +105 °C	3.691	--	45.604	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled T_A = -40 °C to +105 °C	48.408	--	51.004	mV
			LB - Disabled T_A = -40 °C to +105 °C	40.130	--	54.622	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled T_A = -40 °C to +105 °C	198.131	--	201.066	mV
			LB - Disabled T_A = -40 °C to +105 °C	189.278	--	203.599	mV
Series Input Resistance	R_{sin}	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Propagation Delay, Response Time	PROP	Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	20.14	224.67	µs
			High to Low, T_A = -40 °C to +105 °C	--	21.40	228.61	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	7.11	86.83	µs
			High to Low, T_A = -40 °C to +105 °C	--	8.59	98.99	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	1.14	12.06	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.14	4.84	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	0.46	1.79	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.55	2.60	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	13.91	84.35	µs
			High to Low, T_A = -40 °C to +105 °C	--	15.36	90.15	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	4.97	31.60	µs
			High to Low, T_A = -40 °C to +105 °C	--	5.98	39.68	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	0.91	1.98	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.01	1.58	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 50 mV	Low to High, T_A = -40 °C to +105 °C	--	0.37	1.14	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.45	0.81	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	20.28	228.06	µs
			High to Low, T_A = -40 °C to +105 °C	--	21.67	232.39	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	7.19	89.05	µs
			High to Low, T_A = -40 °C to +105 °C	--	6.39	78.66	µs

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Propagation Delay, Response Time	PROP	Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	1.17	2.01	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.25	2.06	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	0.41	0.68	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.39	0.75	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	14.19	84.96	µs
			High to Low, T_A = -40 °C to +105 °C	--	15.66	91.88	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	5.03	32.06	µs
			High to Low, T_A = -40 °C to +105 °C	--	4.51	30.70	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	1.10	1.82	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.20	1.94	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 250 mV	Low to High, T_A = -40 °C to +105 °C	--	0.35	0.55	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.33	0.64	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	20.69	232.09	µs
			High to Low, T_A = -40 °C to +105 °C	--	22.19	241.46	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	7.28	90.29	µs
			High to Low, T_A = -40 °C to +105 °C	--	6.47	79.76	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	1.40	2.85	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.45	2.56	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	0.41	0.68	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.37	0.62	µs

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Propagation Delay, Response Time	PROP	Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	14.48	86.02	µs
			High to Low, T_A = -40 °C to +105 °C	--	16.01	93.69	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	5.09	32.43	µs
			High to Low, T_A = -40 °C to +105 °C	--	4.57	31.06	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	1.34	2.69	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.40	2.50	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 600 mV	Low to High, T_A = -40 °C to +105 °C	--	0.35	0.55	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.31	0.50	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	21.07	237.30	µs
			High to Low, T_A = -40 °C to +105 °C	--	22.66	244.72	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	7.38	91.95	µs
			High to Low, T_A = -40 °C to +105 °C	--	6.55	81.25	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	1.46	2.94	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.51	2.89	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	0.42	0.68	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.37	0.59	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	14.69	87.94	µs
			High to Low, T_A = -40 °C to +105 °C	--	16.31	95.65	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	5.14	32.91	µs
			High to Low, T_A = -40 °C to +105 °C	--	4.62	31.59	µs

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Propagation Delay, Response Time	PROP	Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	1.36	2.81	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.45	2.89	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 850 mV	Low to High, T_A = -40 °C to +105 °C	--	0.35	0.53	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.31	0.48	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	27.40	1193.10	µs
			High to Low, T_A = -40 °C to +105 °C	--	28.14	962.09	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	10.67	683.00	µs
			High to Low, T_A = -40 °C to +105 °C	--	6.98	108.00	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 10 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	8.14	1078.16	µs
			High to Low, T_A = -40 °C to +105 °C	--	5.00	748.66	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 100 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	4.07	648.33	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.61	27.15	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	15.28	99.83	µs
			High to Low, T_A = -40 °C to +105 °C	--	17.06	105.90	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	5.38	37.46	µs
			High to Low, T_A = -40 °C to +105 °C	--	4.73	32.64	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 10 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	1.82	11.85	µs
			High to Low, T_A = -40 °C to +105 °C	--	1.77	10.13	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 100 mV, V_{REF} = 1200 mV	Low to High, T_A = -40 °C to +105 °C	--	0.63	6.60	µs
			High to Low, T_A = -40 °C to +105 °C	--	0.34	0.78	µs

Parameter	Symbol	Note	Conditions	Min	Typ	Max	Unit
Gain error (including threshold and internal V_{REF} error), T_A = -40 °C to +105 °C	G	G = 1, V_{DD} = 1.71 V	V_{REF} = 50 mV to 1200 mV	--	1	--	
		G = 1, V_{DD} = 3.3 V		--	1	--	
		G = 1, V_{DD} = 5.5 V		--	1	--	
		G = 0.5, V_{DD} = 1.71 V		-6.323	--	9.895	%
		G = 0.5, V_{DD} = 3.3 V		-6.110	--	7.751	
		G = 0.5, V_{DD} = 5.5 V		-6.369	--	7.715	
		G = 0.33, V_{DD} = 1.71V		-5.028	--	11.334	
		G = 0.33, V_{DD} = 3.3 V		-3.677	--	6.273	
		G = 0.33, V_{DD} = 5.5 V		-5.201	--	7.370	
		G = 0.25, V_{DD} = 1.71V		-5.940	--	7.709	
		G = 0.25, V_{DD} = 3.3 V		-5.910	--	7.353	
		G = 0.25, V_{DD} = 5.5 V		-5.793	--	4.990	
Internal V_{REF} error, V_{REF} = 1200 mV	V_{REF}	V_{DD} = 1.8 V ± 5 %	T_A = +25 °C	-0.25	--	0.50	%
			T_A = -40 °C to +105 °C	-2.25	--	0.67	
		V_{DD} = 3.3 V ± 10 %	T_A = +25 °C	-0.33	--	0.42	
			T_A = -40 °C to +105 °C	-2.50	--	0.58	
		V_{DD} = 5.0 V ± 10 %	T_A = +25 °C	-0.50	--	0.33	
			T_A = -40 °C to +105 °C	-2.08	--	0.50	
Internal V_{REF} error, V_{REF} = 1000 mV		V_{DD} = 1.8 V ± 5 %	T_A = +25 °C	-0.10	--	0.70	
			T_A = -40 °C to +105 °C	-7.30	--	0.80	
		V_{DD} = 3.3 V ± 10 %	T_A = +25 °C	-0.20	--	0.60	
			T_A = -40 °C to +105 °C	-2.10	--	0.70	
		V_{DD} = 5.0 V ± 10 %	T_A = +25 °C	-0.40	--	0.50	
			T_A = -40 °C to +105 °C	-1.60	--	0.60	
Internal V_{REF} error, V_{REF} = 500 mV		V_{DD} = 1.8 V ± 5 %	T_A = +25 °C	-0.40	--	0.60	
			T_A = -40 °C to +105 °C	-3.00	--	0.80	
		V_{DD} = 3.3 V ± 10 %	T_A = +25 °C	-0.60	--	0.40	
			T_A = -40 °C to +105 °C	-2.60	--	0.60	
		V_{DD} = 5.0 V ± 10 %	T_A = +25 °C	-0.60	--	0.40	
			T_A = -40 °C to +105 °C	-2.20	--	0.60	

4. User Programmability

Non-volatile memory (NVM) is used to configure the SLG46535-EV's connection matrix routing and macrocells. The NVM is One Time Programmable (OTP). However, Renesas Electronics Corporation's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Renesas Electronics Corporation to integrate into the production process.

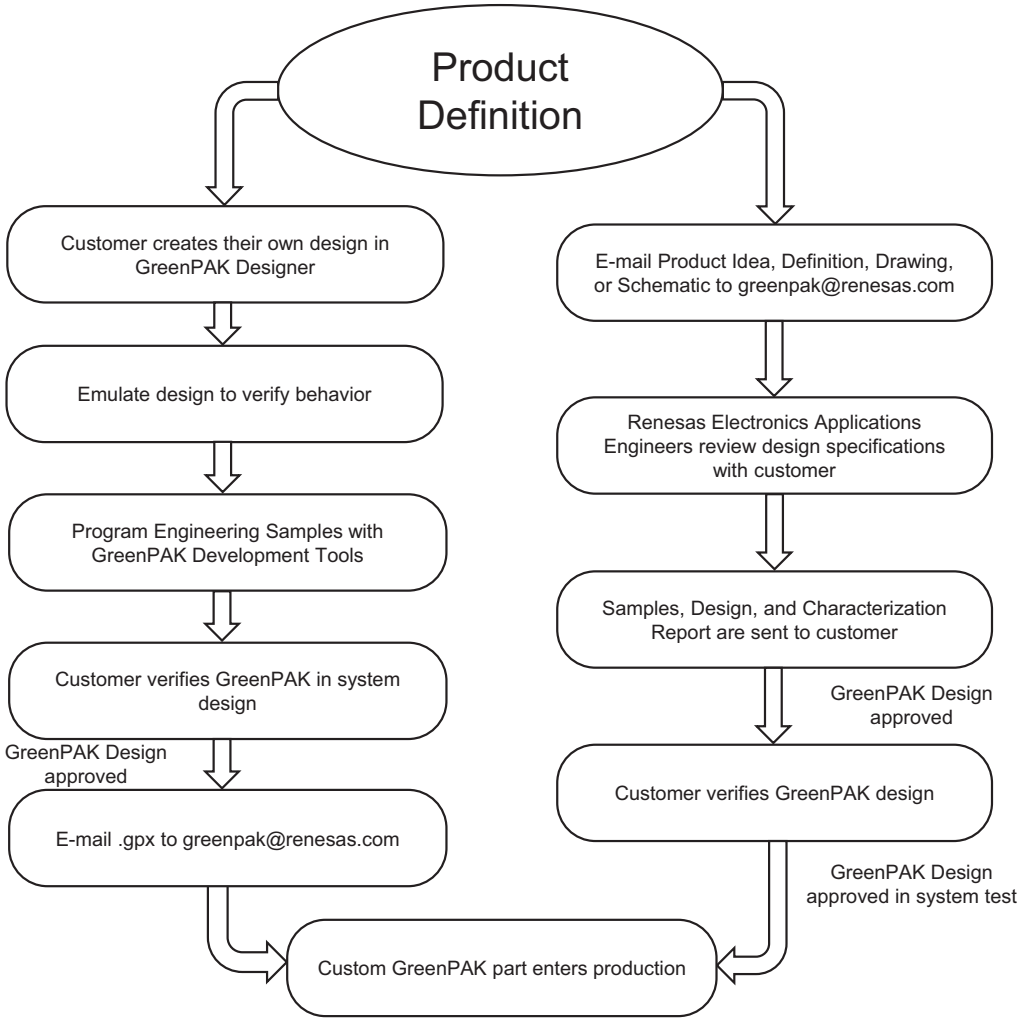


Figure 3. Steps to Create a Custom GreenPAK Device

5. Input/Output Pins

The SLG46535-EV has a total of 11 multi-function IO pins, which can function as either a user defined input or output, as well as serving as a special function, or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Refer to section 2. Pin Information for normal mode pin definitions.

Normal Mode pin definitions are as follows:

- Pin 1: V_{DD} power supply
- Pin 2: general purpose input
- Pin 3: general purpose input or output
- Pin 4: general purpose input or output, or analog comparator 0(+)
- Pin 5: general purpose input or output with OE, or analog comparator 0(-)
- Pin 6: general purpose input or OD output SCL
- Pin 7: general purpose input or OD output SDA
- Pin 8: general purpose input or output with OE, or analog comparator 1(+)
- Pin 9: ground
- Pin 10: general purpose input or analog comparator 0/1/2(-)
- Pin 11: V_{DD2} power supply
- Pin 12: general purpose input or output with OE
- Pin 13: general purpose input or output, or external clock input for OSC0 25 kHz/2 MHz
- Pin 14: general purpose input or output, or external clock input for OSC1 25 MHz.

Of the 12 user defined IO pins on the SLG46535-EV, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

The high side of the user selectable push-pull or open-drain pin output structures for each GPIO is connected to either V_{DD} or V_{DD2}. This allows for the appropriate voltage level output compatible with each voltage domain.

Pins 2, 3, 4, 5, 6, 7, and 8 are powered from V_{DD} and Pins 10, 12, 13 and 14 are powered from V_{DD2}. All internal macrocells are powered from V_{DD}. Voltage on V_{DD2} Pin must be less or equal voltage on V_{DD} Pin.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as input, ESD pin protection diodes must be considered when applying an input signal to the pin. This will cause a significant current leakage.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as output, the pin will behave as NMOS Open-Drain. It is not recommended to connect V_{DD2} to the GND.

5.1 Input Modes

Each IO pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 4, 5, 8, and 10 can also be configured to serve as analog inputs to the on-chip comparators.

5.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 10, 12, 13, and 14 can all be configured as digital output pins.

5.3 Pull-Up/Down Resistors

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either pull-ups or pull-downs.

5.4 GPI Structure

5.4.1 GPI Structure (for Pin 2)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user.
Note 2: OE is Matrix output, Digital In is Matrix input.

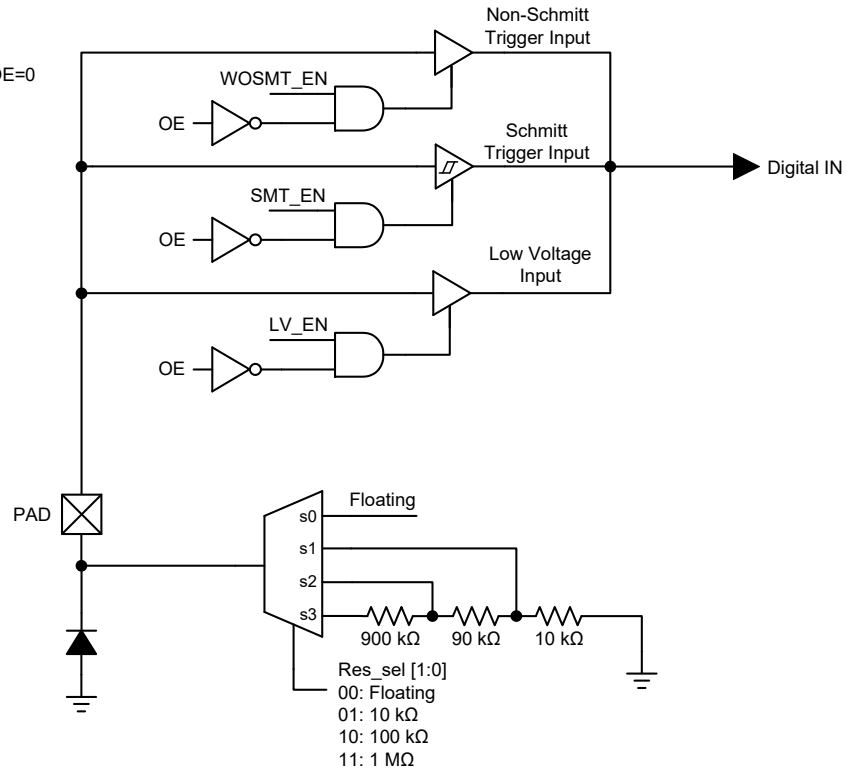


Figure 4. Pin 2 GPI Structure Diagram

5.5 Matrix OE IO Structure

5.5.1 Matrix OE IO Structure (for Pin 5)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en=1
01: Digital In with Schmitt Trigger, smt_en=1
10: Low Voltage Digital In mode, lv_en = 1
11: Analog IO mode
Output Mode [1:0]
00: 1x push-pull mode, pp1x_en=1
01: 2x push-pull mode, pp2x_en=1, pp1x_en=1
10: 1x NMOS open-drain mode, od1x_en=1
11: 2x NMOS open-drain mode, od2x_en=1, od1x_en=1

Note 1: Digital Out and OE are Matrix output, Digital In is Matrix Input.
Note 2: Can be varied over PVT, for reference only.

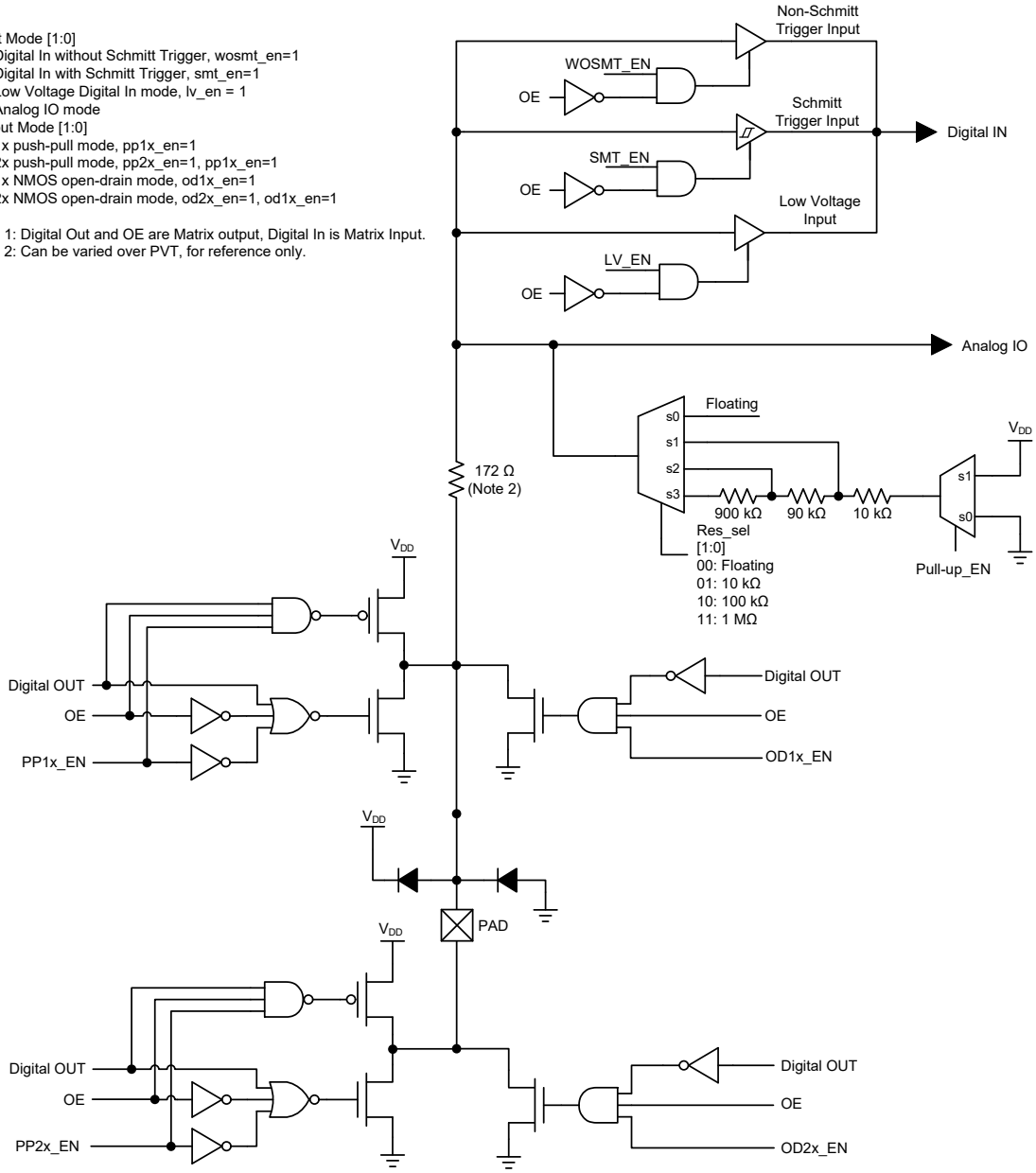


Figure 5. Matrix OE IO Structure Diagram

5.5.2 Matrix OE IO Structure (for Pin 12)

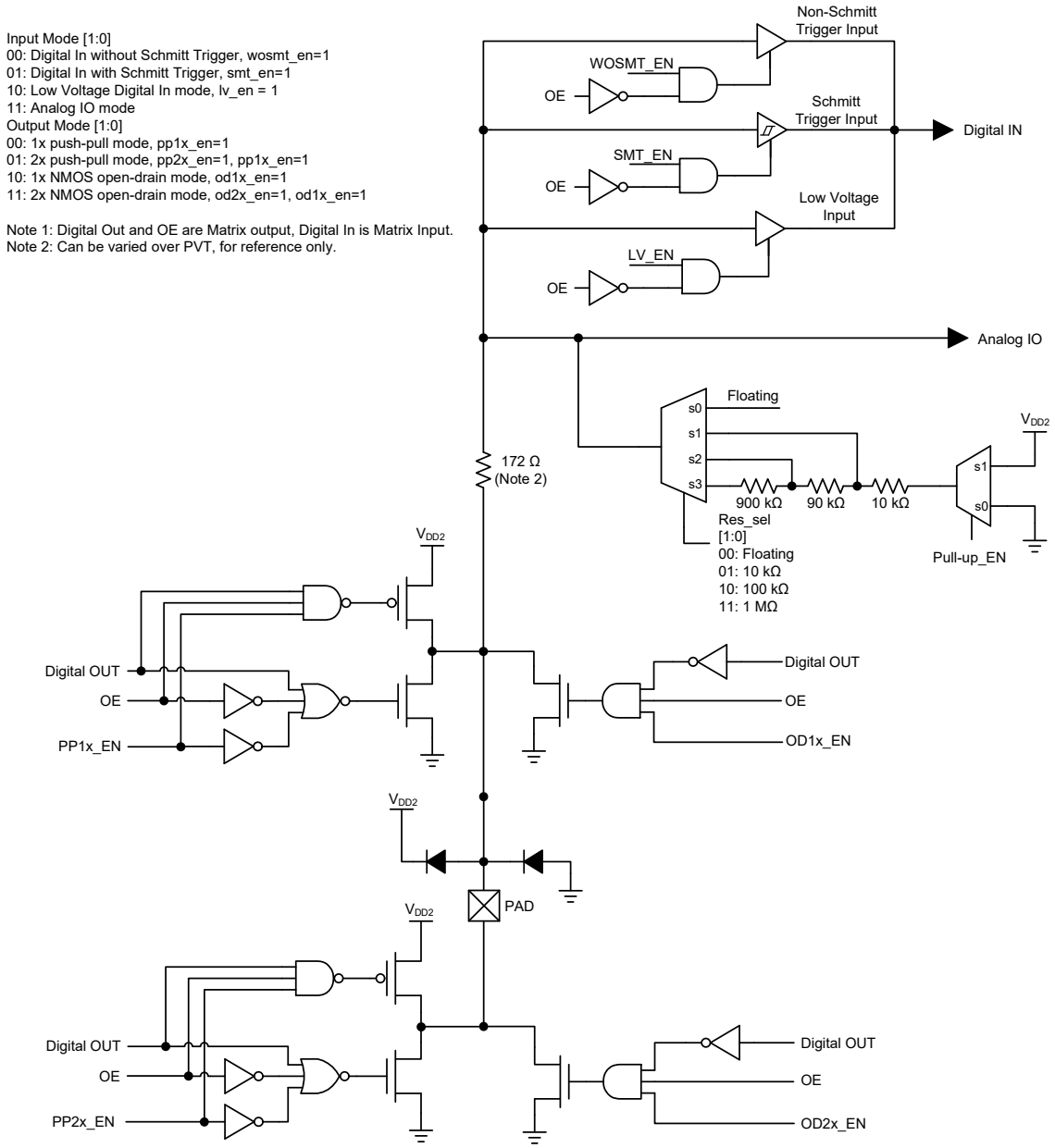


Figure 6. Matrix OE IO Structure Diagram

5.5.3 Matrix OE IO Structure (for Pins 6 and 7)

Pin 6, Pin 7 Mode [2:0]
000: Digital Input without Schmitt Trigger
001: Digital Input with Schmitt Trigger
010: Low Voltage Digital Input
011: Reserved
100: Reserved
101: Open Drain NMOS
110: Reserved
111: Reserved

Note: Digital Out and OE are Matrix output, Digital In is Matrix input.

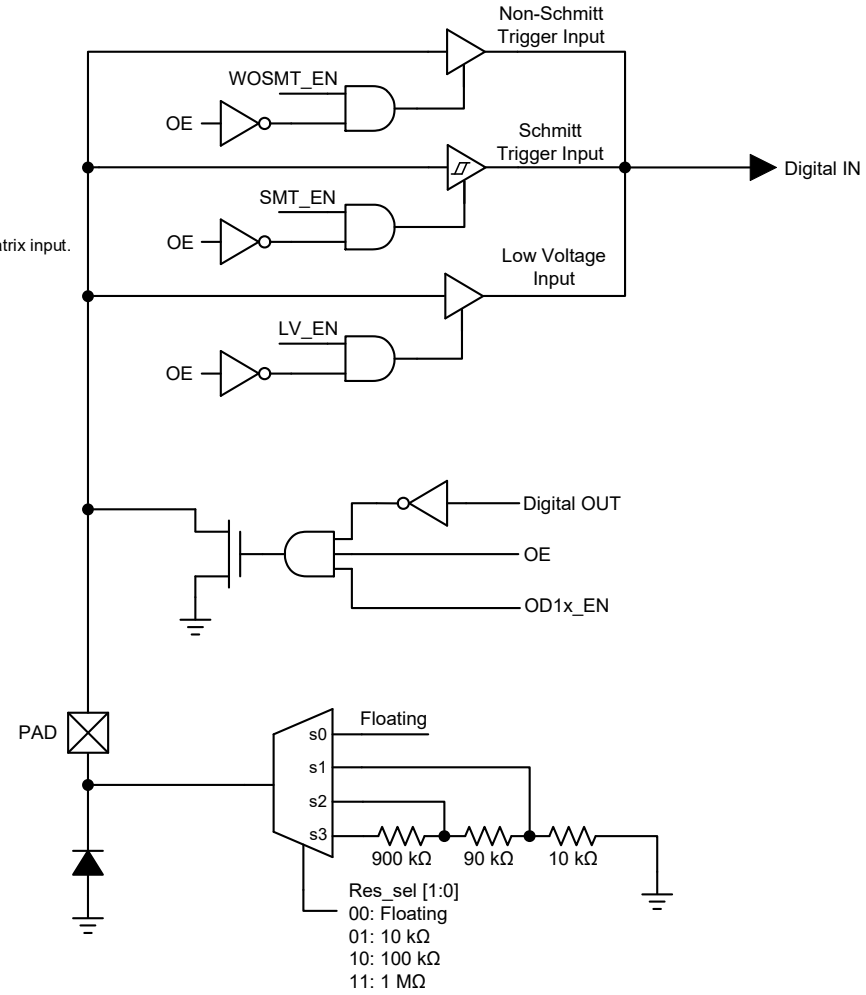


Figure 7. Matrix OE IO Structure Diagram

5.5.4 Matrix OE 4x Drive Structure (for Pin 8)

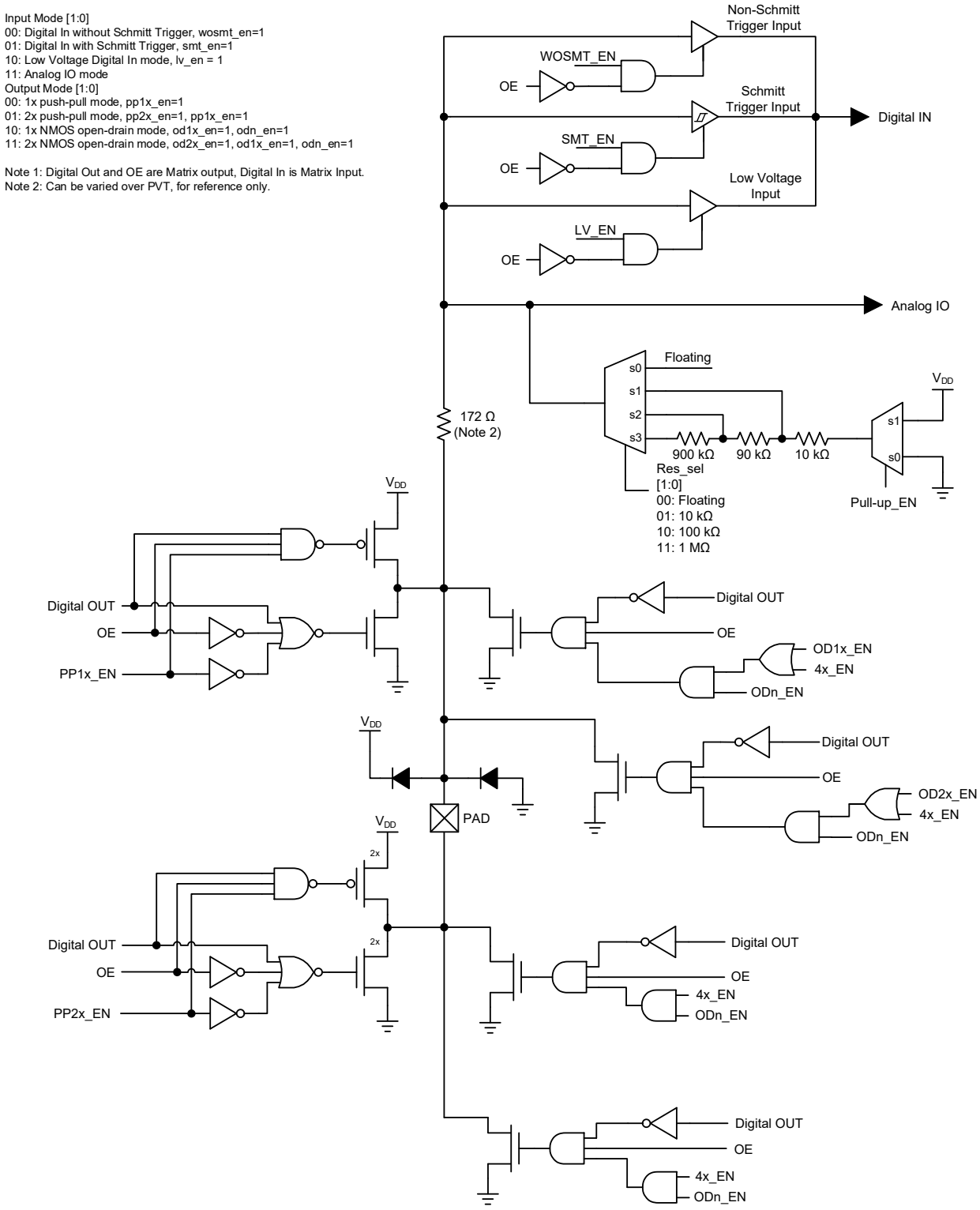


Figure 8. Matrix OE IO 4x Drive Structure Diagram

5.5.5 4x Drive Srtructure (for Pin 10)

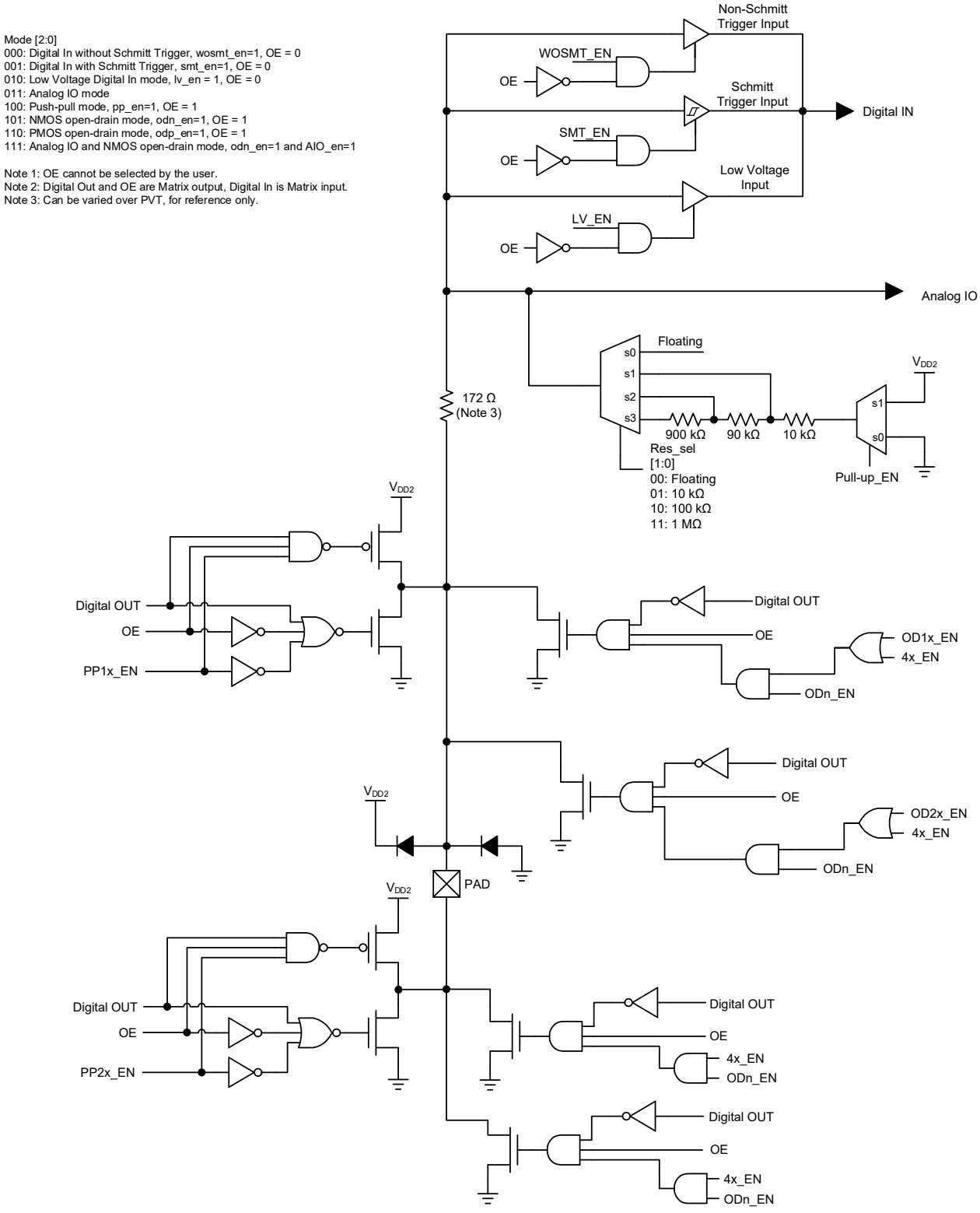


Figure 9. IO 4x Drive Structure Diagram

5.6 Register OE IO Structure

5.6.1 IO Structure (for Pins 3 and 4)

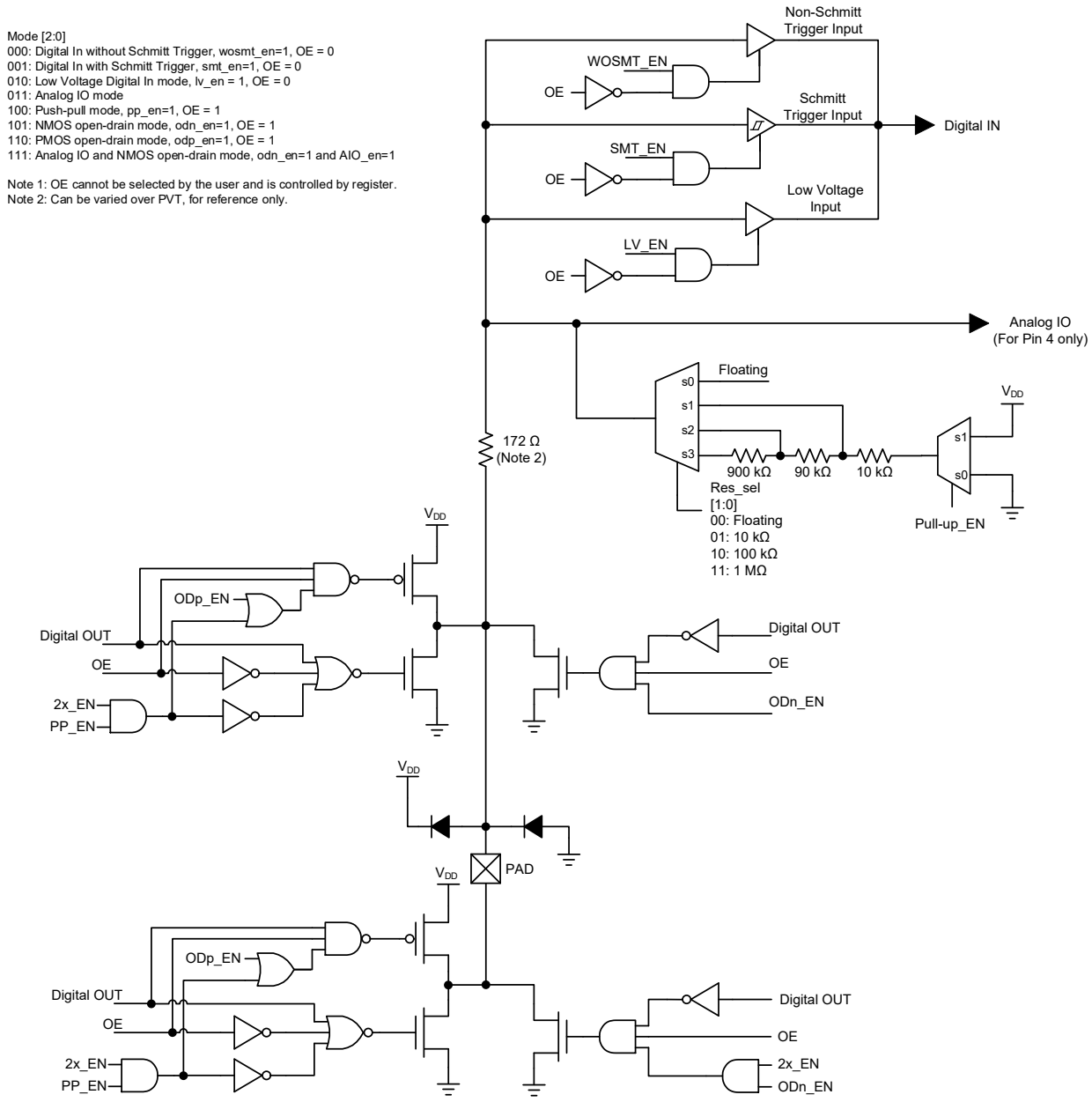


Figure 10. IO Structure Diagram

5.6.2 IO Structure (for Pins 13 and 14)

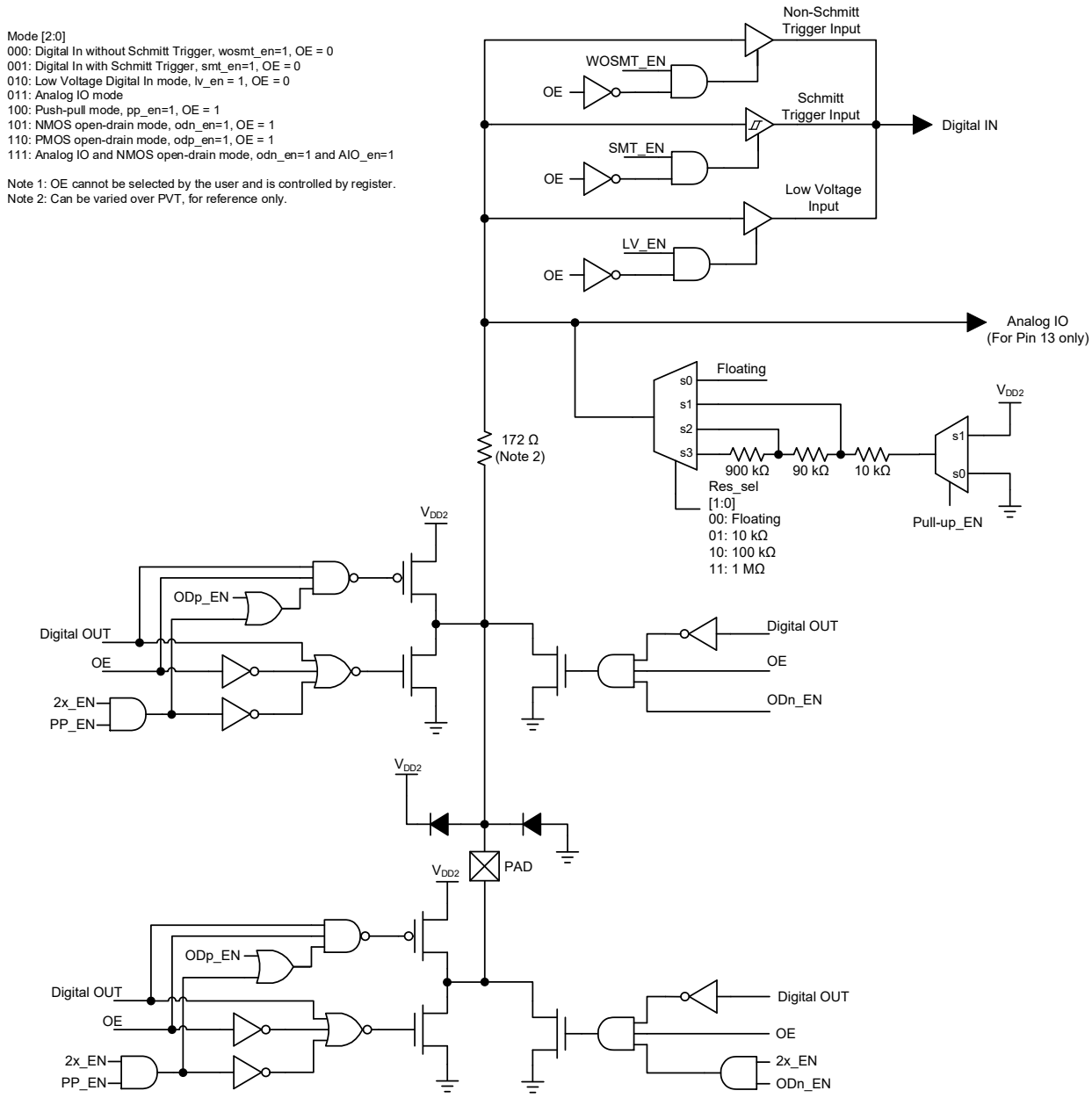


Figure 11. IO Structure Diagram

6. Connection Matrix

The Connection Matrix in the SLG46535-EV is used to create the internal routing for internal functional macrocells of the device as soon as it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46535-EV has a specific digital bit code assigned to it, that is either set to active High or inactive Low, based on the design that is created. Once the 2048 register bits within the SLG46535-EV are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 110 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46535-EV's register table, see section 17. Register Definitions.

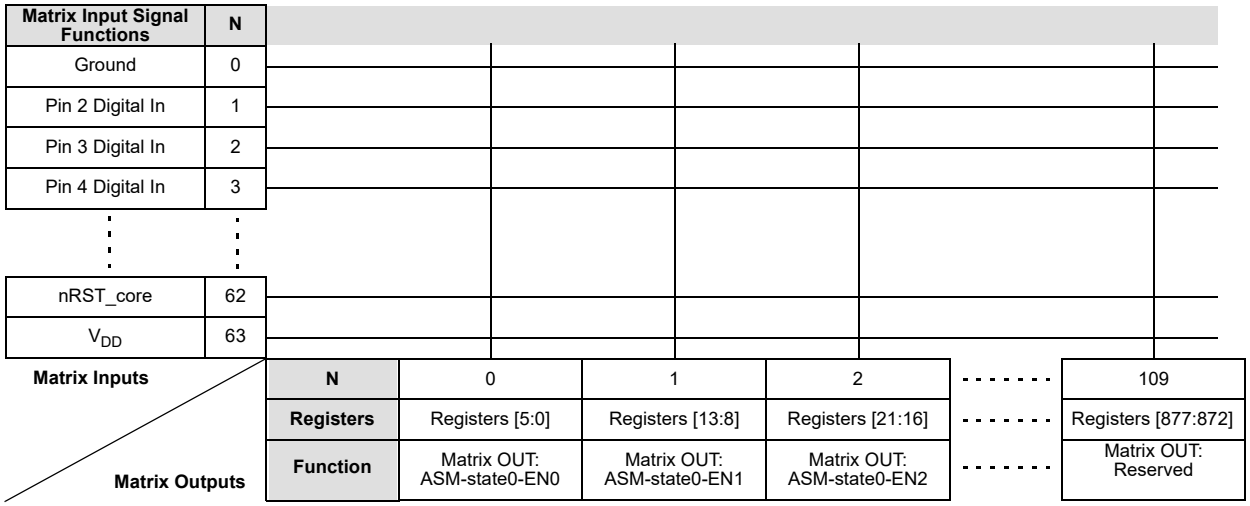


Figure 12. Connection Matrix

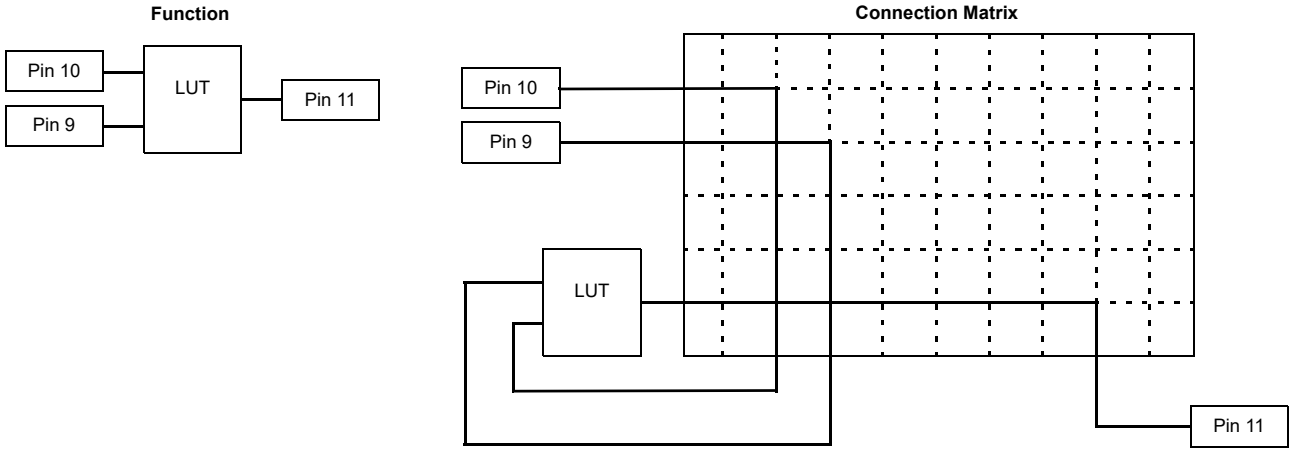


Figure 13. Connection Matrix Example

6.1 Matrix Input Table

Table 4. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	Ground	0	0	0	0	0	0
1	Pin 2 Digital Input	0	0	0	0	0	1
2	Reserved	0	0	0	0	1	0
3	Pin 3 Digital Input	0	0	0	0	1	1
4	Reserved	0	0	0	1	0	0
5	Pin 4 Digital Input	0	0	0	1	0	1
6	Pin 5 Digital Input	0	0	0	1	1	0
7	Pin 8 Digital Input	0	0	0	1	1	1
8	2-bit LUT0/DFF0 Output	0	0	1	0	0	0
9	2-bit LUT1/DFF1 Output	0	0	1	0	0	1
10	2-bit LUT2/DFF2 Output	0	0	1	0	1	0
11	2-bit LUT3/PGen Output	0	0	1	0	1	1
12	3-bit LUT0/DFF3 Output	0	0	1	1	0	0
13	3-bit LUT1/DFF4 Output	0	0	1	1	0	1
14	3-bit LUT2/DFF5 Output	0	0	1	1	1	0
15	3-bit LUT3/DFF6 Output	0	0	1	1	1	1
16	3-bit LUT4/DFF7 Output	0	1	0	0	0	0
17	3-bit LUT5/CNT_DLY2(8bit) Output	0	1	0	0	0	1
18	3-bit LUT6/CNT_DLY3(8bit) Output	0	1	0	0	1	0
19	3-bit LUT7/CNT_DLY4(8bit) Output	0	1	0	0	1	1
20	3-bit LUT8/CNT_DLY5(8bit) Output	0	1	0	1	0	0
21	3-bit LUT9/CNT_DLY6(8bit) Output	0	1	0	1	0	1
22	4-bit LUT0/CNT_DLY0(16bit) Output	0	1	0	1	1	0
23	4-bit LUT1/CNT_DLY1(16bit) Output	0	1	0	1	1	1
24	3-bit LUT10/Pipe Delay (1st stage) Output	0	1	1	0	0	0
25	Pipe Delay Output0	0	1	1	0	0	1
26	Pipe Delay Output1	0	1	1	0	1	0
27	Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output (25 kHz/2 MHz)	0	1	1	0	1	1
28	Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output (25 kHz/2 MHz)	0	1	1	1	0	0
29	Internal OSC Pre-Divided by 1/2/4/8 Output (25 MHz)	0	1	1	1	0	1
30	Filter0/Edge Detect0 Output	0	1	1	1	1	0
31	Filter1/Edge Detect1 Output	0	1	1	1	1	1
32	Pin 6 Digital or I2C_virtual_0 Input	1	0	0	0	0	0
33	Pin 7 Digital or I2C_virtual_1 Input	1	0	0	0	0	1

Table 4. Matrix Input Table (Cont.)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
34	I²C_virtual_2 Input	1	0	0	0	1	0
35	I²C_virtual_3 Input	1	0	0	0	1	1
36	I²C_virtual_4 Input	1	0	0	1	0	0
37	I²C_virtual_5 Input	1	0	0	1	0	1
38	I²C_virtual_6 Input	1	0	0	1	1	0
39	I²C_virtual_7 Input	1	0	0	1	1	1
40	ASM-stateX-dout0	1	0	1	0	0	0
41	ASM-stateX-dout1	1	0	1	0	0	1
42	ASM-stateX-dout2	1	0	1	0	1	0
43	ASM-stateX-dout3	1	0	1	0	1	1
44	ASM-stateX-dout4	1	0	1	1	0	0
45	ASM-stateX-dout5	1	0	1	1	0	1
46	ASM-stateX-dout6	1	0	1	1	1	0
47	ASM-stateX-dout7	1	0	1	1	1	1
48	Pin 10 Digital Input	1	1	0	0	0	0
49	Reserved	1	1	0	0	0	1
50	Reserved	1	1	0	0	1	0
51	Reserved	1	1	0	0	1	1
52	Pin 12 Digital Input	1	1	0	1	0	0
53	Pin 13 Digital Input	1	1	0	1	0	1
54	Reserved	1	1	0	1	1	0
55	Reserved	1	1	0	1	1	1
56	Pin 14 Digital Input	1	1	1	0	0	0
57	ACMP_0 Output	1	1	1	0	0	1
58	ACMP_1 Output	1	1	1	0	1	0
59	ACMP_2 Output	1	1	1	0	1	1
60	Reserved	1	1	1	1	0	0
61	Programmable Delay with Edge Detector Output	1	1	1	1	0	1
62	nRST_core (POR) as matrix input	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 Matrix Output Table

Table 5. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[7:0]	Matrix OUT: ASM-state0-EN0	0
[15:8]	Matrix OUT: ASM-state0-EN1	1
[23:16]	Matrix OUT: ASM-state0-EN2	2
[31:24]	Matrix OUT: ASM-state1-EN0	3
[39:32]	Matrix OUT: ASM-state1-EN1	4
[47:40]	Matrix OUT: ASM-state1-EN2	5
[55:48]	Matrix OUT: ASM-state2-EN0	6
[63:56]	Matrix OUT: ASM-state2-EN1	7
[71:64]	Matrix OUT: ASM-state2-EN2	8
[79:72]	Matrix OUT: ASM-state3-EN0	9
[87:80]	Matrix OUT: ASM-state3-EN1	10
[95:88]	Matrix OUT: ASM-state3-EN2	11
[103:96]	Matrix OUT: ASM-state4-EN0	12
[111:104]	Matrix OUT: ASM-state4-EN1	13
[119:112]	Matrix OUT: ASM-state4-EN2	14
[127:120]	Matrix OUT: ASM-state5-EN0	15
[135:128]	Matrix OUT: ASM-state5-EN1	16
[143:136]	Matrix OUT: ASM-state5-EN2	17
[151:144]	Matrix OUT: ASM-state6-EN0	18
[159:152]	Matrix OUT: ASM-state6-EN1	19
[167:160]	Matrix OUT: ASM-state6-EN2	20
[175:168]	Matrix OUT: ASM-state7-EN0	21
[183:176]	Matrix OUT: ASM-state7-EN1	22
[191:184]	Matrix OUT: ASM-state7-EN2	23
[199:192]	Matrix OUT: ASM-state-nRST	24
[207:200]	Reserved	25
[215:208]	Reserved	26
[223:216]	Matrix OUT: Pin 3 Digital Output Source	27
[231:224]	Reserved	28
[239:232]	Reserved	29
[247:240]	Matrix OUT: Pin 4 Digital Output Source	30
[255:248]	Matrix OUT: Pin 5 Digital Output Source	31
[263:256]	Matrix OUT: Pin 5 Output Enable	32
[271:264]	Matrix OUT: Pin 6 Digital Output Source (SCL with VI/Input and NMOS open-drain)	33
[279:272]	Matrix OUT: Pin 7 Digital Output Source (SDA with VI/Input and NMOS open-drain)	34

Table 5. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[287:280]	Matrix OUT: Pin 8 Digital Output Source	35
[295:288]	Matrix OUT: Pin 8 Output Enable	36
[303:296]	Matrix OUT: Pin 10 Digital Output Source	37
[311:304]	Reserved	38
[319:312]	Reserved	39
[327:320]	Matrix OUT: Inverter Input	40
[335:328]	Reserved	41
[343:336]	Reserved	42
[351:344]	Matrix OUT: Pin 12 Digital Output Source	43
[359:352]	Matrix OUT: Pin 12 Output Enable	44
[367:360]	Matrix OUT: Pin 13 Digital Output Source	45
[375:368]	Reserved	46
[383:376]	Reserved	47
[391:384]	Reserved	48
[399:392]	Reserved	49
[407:400]	Matrix OUT: Pin 14 Digital Output Source	50
[415:408]	Matrix OUT: ACMP0 nPD (Power-Down)	51
[423:416]	Matrix OUT: ACMP1 nPD (Power-Down)	52
[431:424]	Matrix OUT: ACMP2 nPD (Power-Down)	53
[439:432]	Reserved	54
[447:440]	Matrix OUT: Input of Filter_0 with fixed time edge detector	55
[455:448]	Matrix OUT: Input of Filter_1 with fixed time edge detector	56
[463:456]	Matrix OUT: Input of Programmable Delay and Edge Detector	57
[471:464]	Matrix OUT: OSC 25 kHz/2 MHz nPD (Power-Down)	58
[479:472]	Matrix OUT: OSC 25 MHz nPD (Power-Down)	59
[487:480]	Matrix OUT: IN0 of 2-bit LUT0 or Clock Input of DFF0	60
[495:488]	Matrix OUT: IN1 of 2-bit LUT0 or Data Input of DFF0	61
[503:496]	Matrix OUT: IN0 of 2-bit LUT1 or Clock Input of DFF1	62
[511:504]	Matrix OUT: IN1 of 2-bit LUT1 or Data Input of DFF1	63
[519:512]	Matrix OUT: IN0 of 2-bit LUT2 or Clock Input of DFF2	64
[527:520]	Matrix OUT: IN1 of 2-bit LUT2 or Data Input of DFF2	65
[535:528]	Matrix OUT: IN0 of 2-bit LUT3 or Clock Input of PGen	66
[543:536]	Matrix OUT: IN1 of 2-bit LUT3 or nRST of PGen	67
[551:544]	Matrix OUT: IN0 of 3-bit LUT0 or Clock Input of DFF3	68
[559:552]	Matrix OUT: IN1 of 3-bit LUT0 or Data Input of DFF3	69
[567:560]	Matrix OUT: IN2 of 3-bit LUT0 or nRST (nSET) of DFF3	70

Table 5. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[575:568]	Matrix OUT: IN0 of 3-bit LUT1 or Clock Input of DFF4	71
[583:576]	Matrix OUT: IN1 of 3-bit LUT1 or Data Input of DFF4	72
[591:584]	Matrix OUT: IN2 of 3-bit LUT1 or nRST (nSET) of DFF4	73
[599:592]	Matrix OUT: IN0 of 3-bit LUT2 or Clock Input of DFF5	74
[607:600]	Matrix OUT: IN1 of 3-bit LUT2 or Data Input of DFF5	75
[615:608]	Matrix OUT: IN2 of 3-bit LUT2 or nRST (nSET) of DFF5	76
[623:616]	Matrix OUT: IN0 of 3-bit LUT3 or Clock Input of DFF6	77
[631:624]	Matrix OUT: IN1 of 3-bit LUT3 or Data Input of DFF6	78
[639:632]	Matrix OUT: IN2 of 3-bit LUT3 or nRST (nSET) of DFF6	79
[647:640]	Matrix OUT: IN0 of 3-bit LUT4 or Clock Input of DFF7	80
[655:648]	Matrix OUT: IN1 of 3-bit LUT4 or Data Input of DFF7	81
[663:656]	Matrix OUT: IN2 of 3-bit LUT4 or nRST (nSET) of DFF7	82
[671:664]	Matrix OUT: IN0 of 3-bit LUT5 or Delay2 Input (or Counter2 RST Input)	83
[679:672]	Matrix OUT: IN1 of 3-bit LUT5 or External Clock Input of Delay2 (or Counter2)	84
[687:680]	Matrix OUT: IN2 of 3-bit LUT5	85
[695:688]	Matrix OUT: IN0 of 3-bit LUT6 or Delay3 Input (or Counter3 RST Input)	86
[703:696]	Matrix OUT: IN1 of 3-bit LUT6 or External Clock Input of Delay3 (or Counter3)	87
[711:704]	Matrix OUT: IN2 of 3-bit LUT6	88
[719:712]	Matrix OUT: IN0 of 3-bit LUT7 or Delay4 Input (or Counter4 RST Input)	89
[727:720]	Matrix OUT: IN1 of 3-bit LUT7 or External Clock Input of Delay4 (or Counter4)	90
[735:728]	Matrix OUT: IN2 of 3-bit LUT7	91
[743:736]	Matrix OUT: IN0 of 3-bit LUT8 or Delay5 Input (or Counter5 RST Input)	92
[751:744]	Matrix OUT: IN1 of 3-bit LUT8 or External Clock Input of Delay5 (or Counter5)	93
[759:752]	Matrix OUT: IN2 of 3-bit LUT8	94
[767:760]	Matrix OUT: IN0 of 3-bit LUT9 or Delay6 Input (or Counter6 RST Input)	95
[775:768]	Matrix OUT: IN1 of 3-bit LUT9 or External Clock Input of Delay6 (or Counter6)	96
[783:776]	Matrix OUT: IN2 of 3-bit LUT9	97
[791:784]	Matrix OUT: IN0 of 3-bit LUT10 or Input of Pipe Delay	98
[799:792]	Matrix OUT: IN1 of 3-bit LUT10 or nRST of Pipe Delay	99
[807:800]	Matrix OUT: IN2 of 3-bit LUT10 or Clock of Pipe Delay	100
[815:808]	Matrix OUT: IN0 of 4-bit LUT0 or Delay0 Input (or Counter0 RST/SET Input)	101
[823:816]	Matrix OUT: IN1 of 4-bit LUT0 or External Clock Input of Delay0 (or Counter0)	102
[831:824]	Matrix OUT: IN2 of 4-bit LUT0 or UP Input of FSM0	103
[839:832]	Matrix OUT: IN3 of 4-bit LUT0 or KEEP Input of FSM0	104
[847:840]	Matrix OUT: IN0 of 4-bit LUT1 or Delay1 Input (or Counter1 RST/SET Input)	105
[855:848]	Matrix OUT: IN1 of 4-bit LUT1 or External Clock Input of Delay1 (or Counter1)	106

Table 5. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[863:856]	Matrix OUT: IN2 of 4-bit LUT1 or UP Input of FSM1	107
[871:864]	Matrix OUT: IN3 of 4-bit LUT1 or KEEP Input of FSM1	108
[879:872]	Reserved	109
[1] For each Address, the two most significant bits are unused.		

6.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at byte 0244.

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs,(Pin 6 Digital or I^2C_virtual_0 Input) and (Pin 7 Digital or I^2C_virtual_1 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). Two register bits select whether the Connection Matrix input comes from the pin input or from the virtual register:

- register [1074] Select SCL and Virtual Input 0 or Pin 6
- register [1082] Select SDA and Virtual Input 1 or Pin 7.

See Table 6 for Connection Matrix Virtual Inputs.

Table 6. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[1952]
33	I^2C_virtual_1 Input	[1953]
34	I^2C_virtual_2 Input	[1954]
35	I^2C_virtual_3 Input	[1955]
36	I^2C_virtual_4 Input	[1956]
37	I^2C_virtual_5 Input	[1957]
38	I^2C_virtual_6 Input	[1958]
39	I^2C_virtual_7 Input	[1959]

6.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell

outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are at bytes 0240 to 0247. Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0244).

7. Combination Function Macrocells

The SLG46535-EV has seventeen combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops.
- Five macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay.
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen).
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter/Delays.
- Two macrocells that can serve as either 4-bit LUTs or as 16-Bit Counter/Delays.

Inputs/Outputs for the 17 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices - AND, NAND, OR, NOR, XOR, XNOR.

7.1 2-Bit LUT or D Flip-Flop Macrocells

There are three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (clk) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
- LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

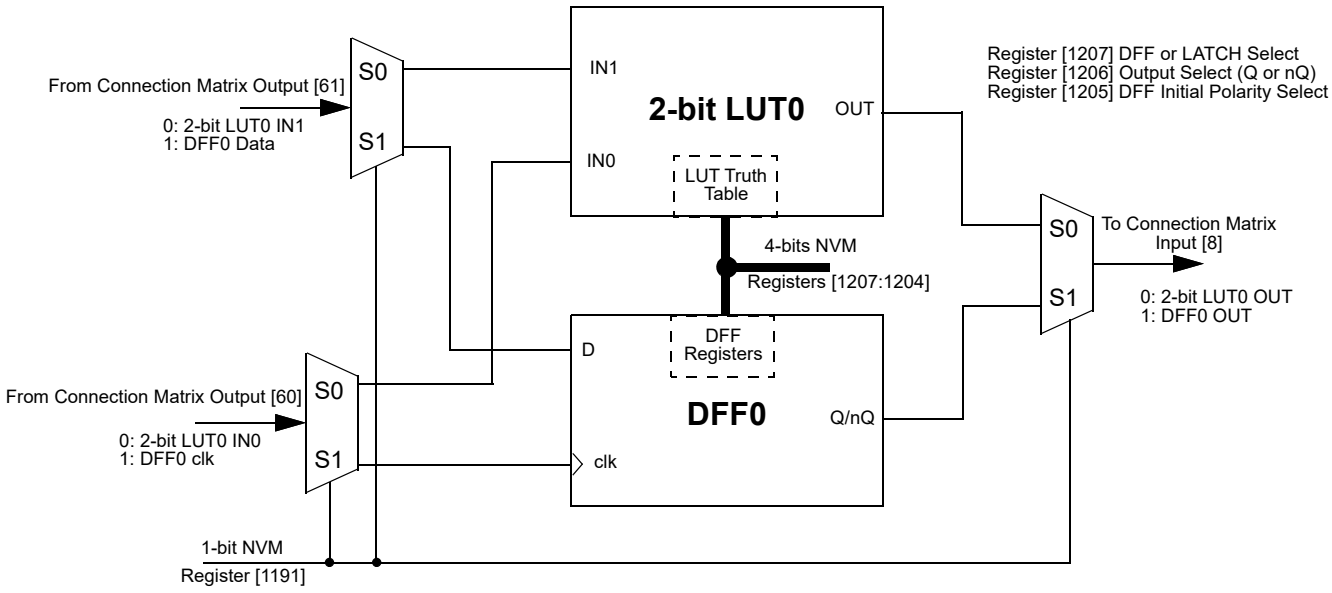


Figure 14. 2-bit LUT0 or DFF0

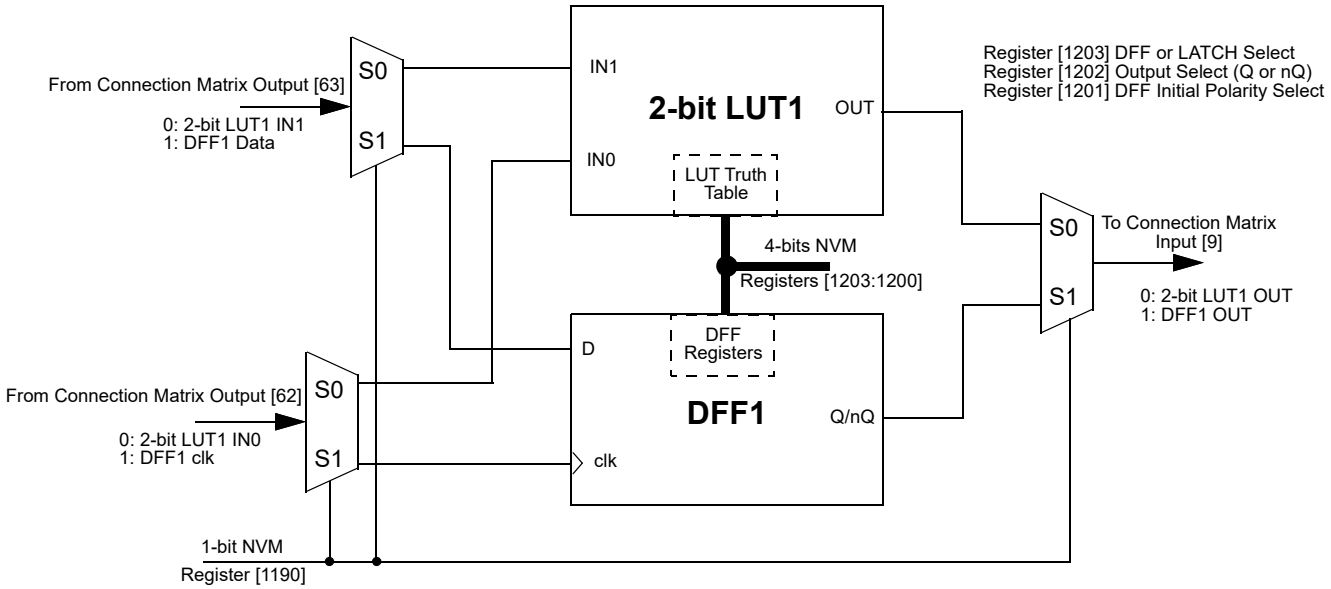


Figure 15. 2-bit LUT1 or DFF1

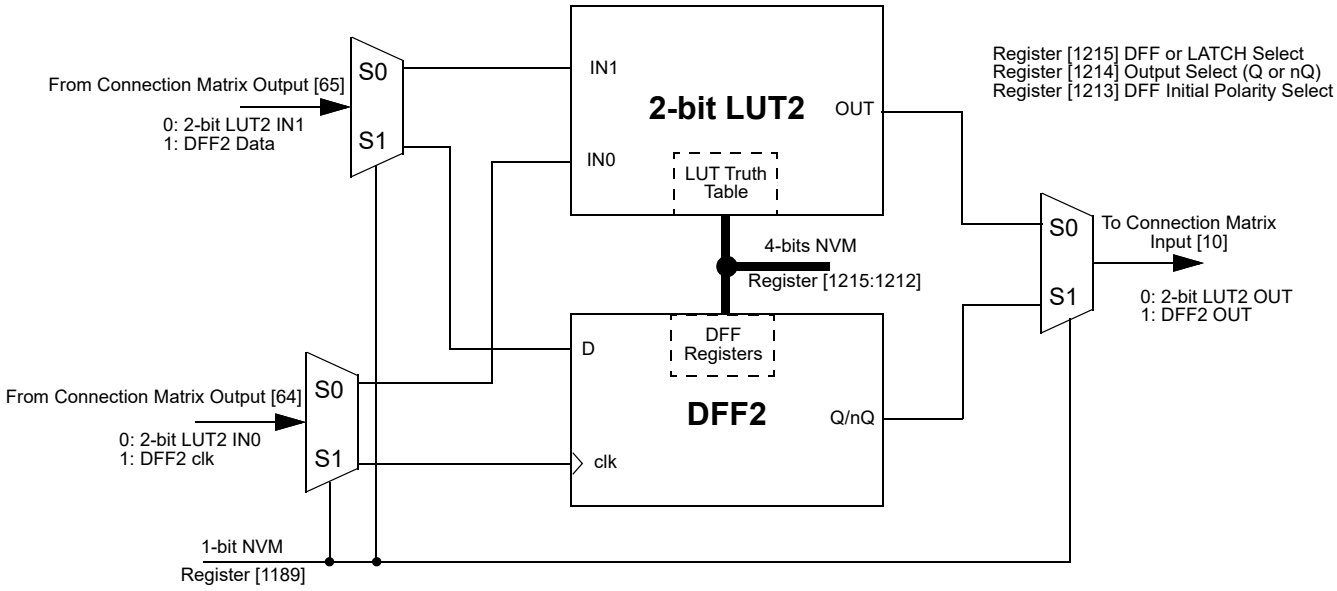


Figure 16. 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocells Used as 2-Bit LUTs

Table 7. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1204]	LSB
0	1	register [1205]	
1	0	register [1206]	
1	1	register [1207]	MSB

Table 8. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1200]	LSB
0	1	register [1201]	
1	0	register [1202]	
1	1	register [1203]	MSB

Table 9. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1212]	LSB
0	1	register [1213]	
1	0	register [1214]	
1	1	register [1215]	MSB

Each macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT0 is defined by registers [1207:1204]
- 2-bit LUT1 is defined by registers [1203:1200]
- 2-bit LUT2 is defined by registers [1215:1212].

Table 10 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR), that can be created within each of the two 2-bit LUT logic cells.

Table 10. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

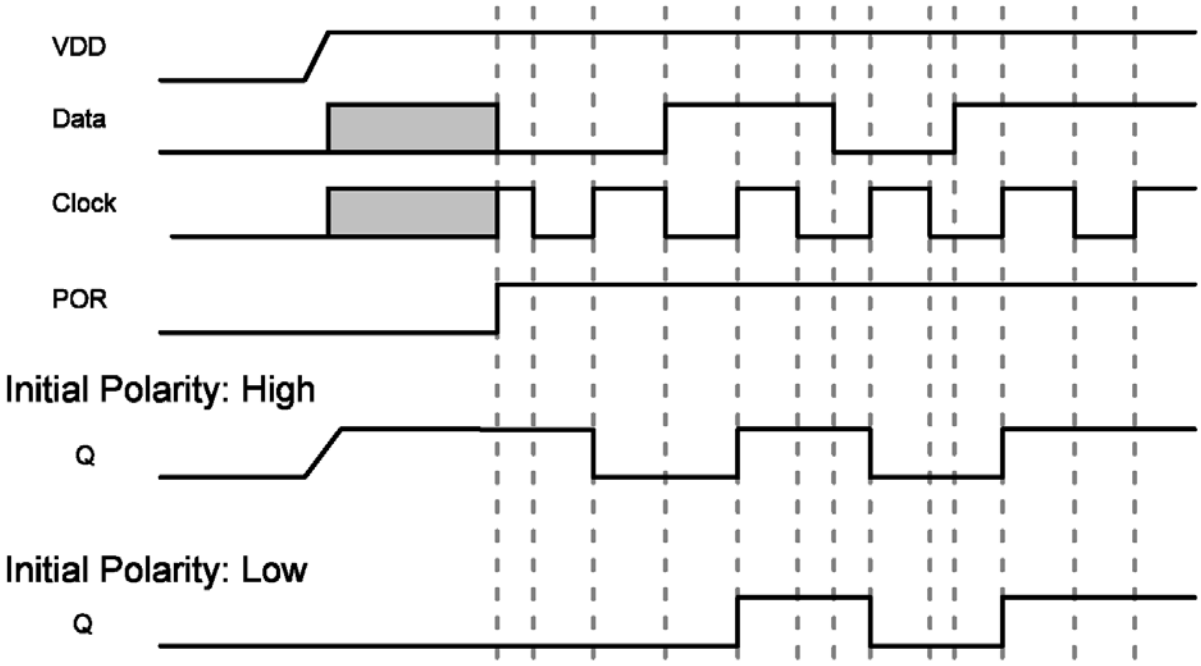


Figure 17. DFF Polarity Operations

7.2 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (clk) and Set/Reset (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

DFF3 has a user selectable option to allow the macrocell output to either come from the Q/nQ output of one D Flip-Flop, or two D Flip-Flops in series, with the first D Flip-Flop triggering on the rising clock edge, and the second D Flip-Flop triggering on the falling clock edge.

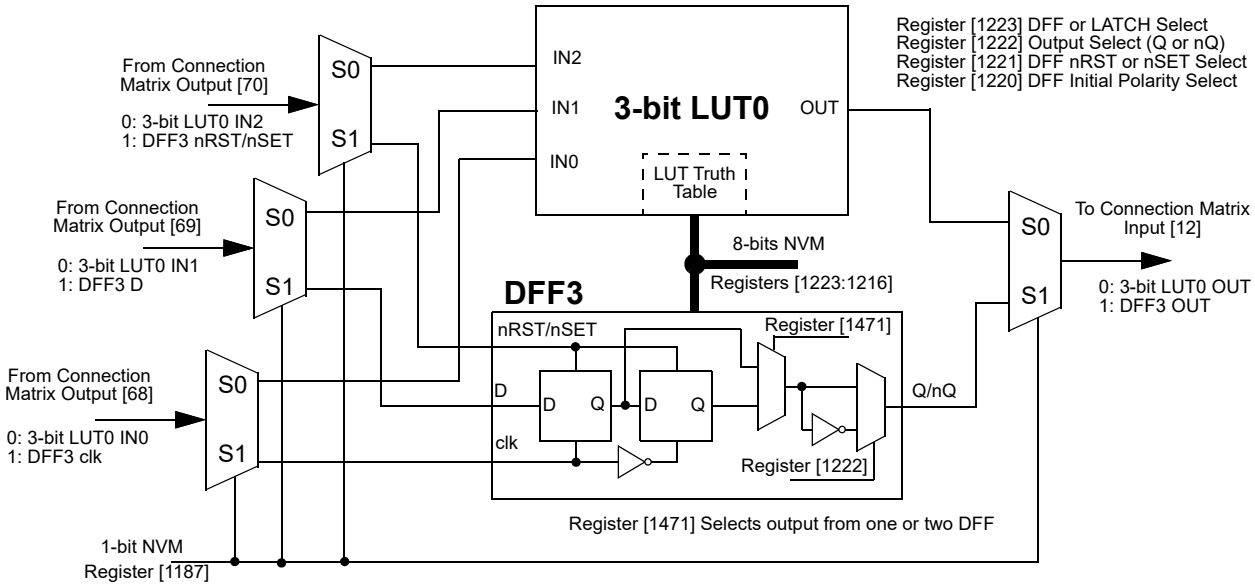


Figure 18. 3-bit LUT0 or DFF3 with RST/SET

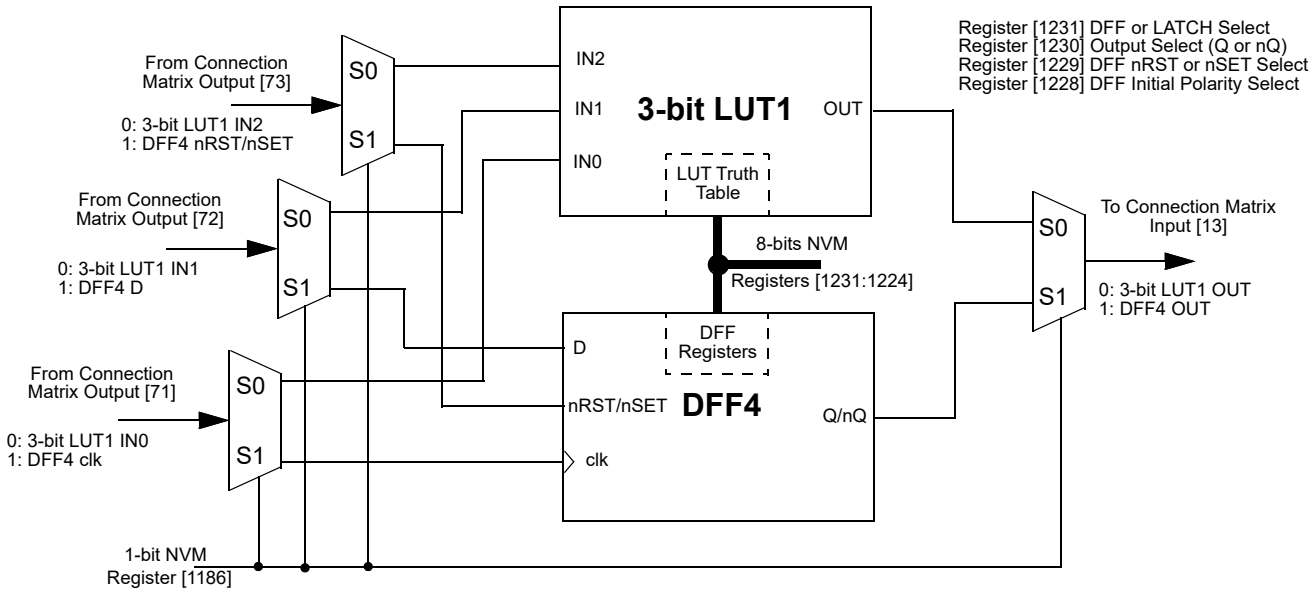


Figure 19. 3-bit LUT1 or DFF4 with RST/SET

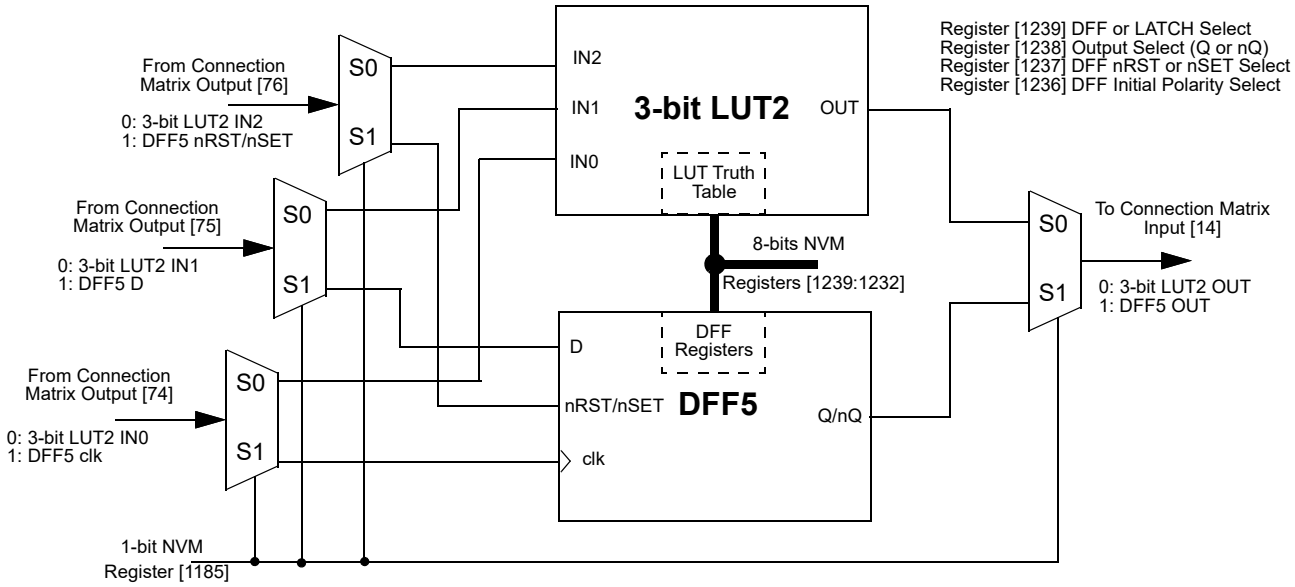


Figure 20. 3-bit LUT2 or DFF5 with RST/SET

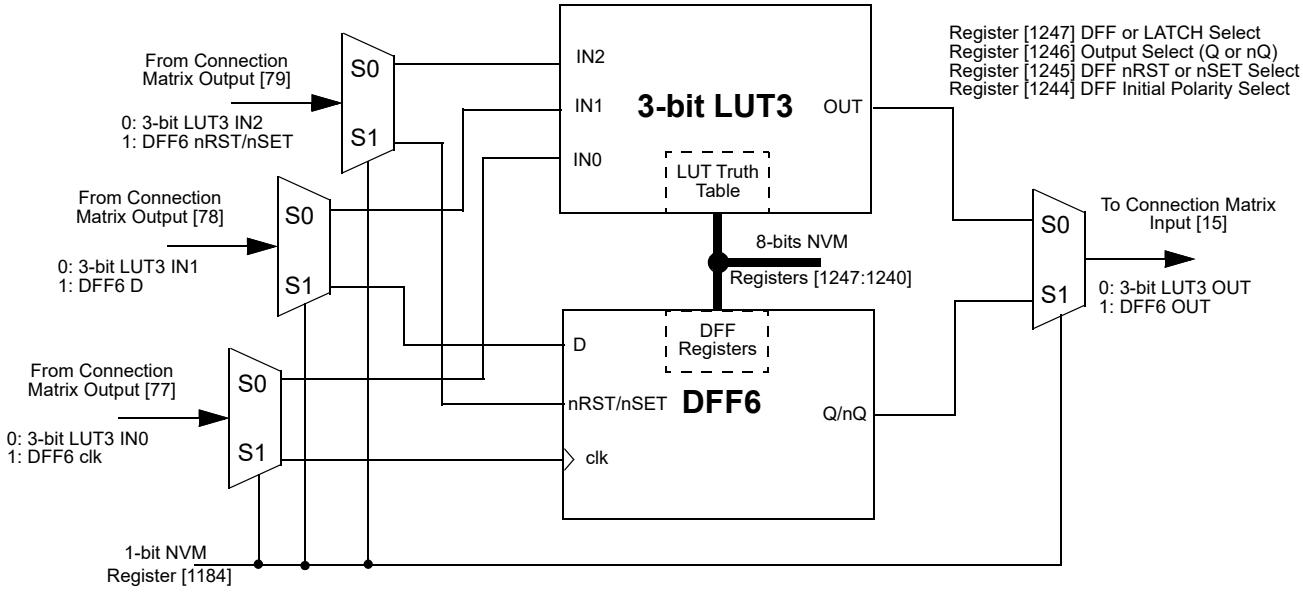


Figure 21. 3-bit LUT3 or DFF6 with RST/SET

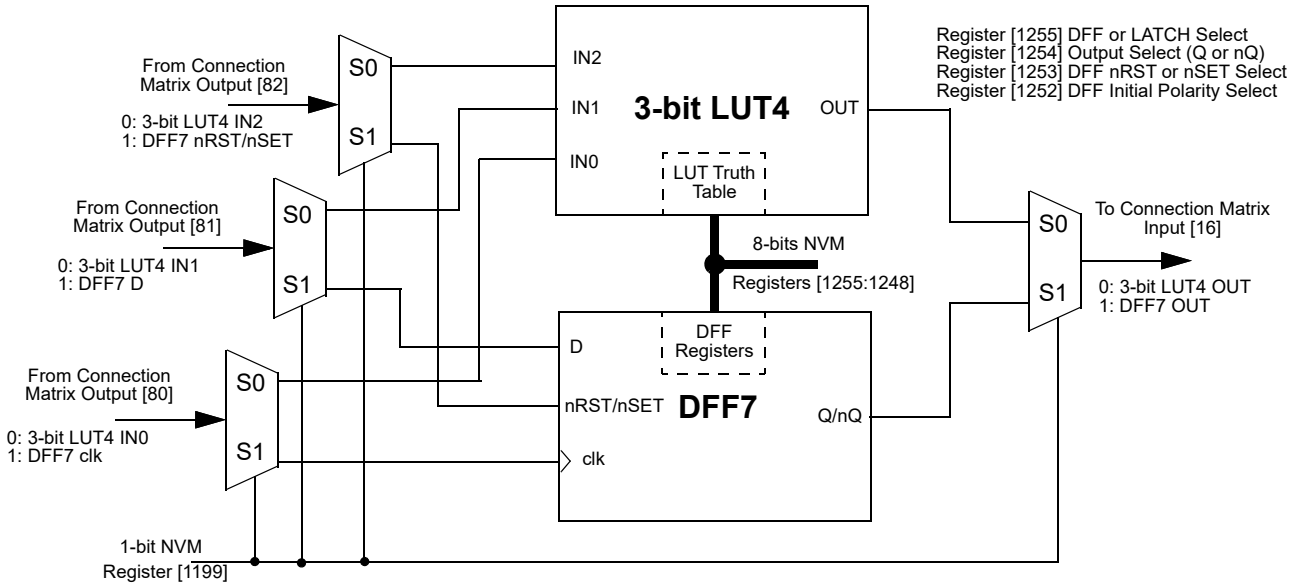


Figure 22. 3-bit LUT4 or DFF7 with RST/SET

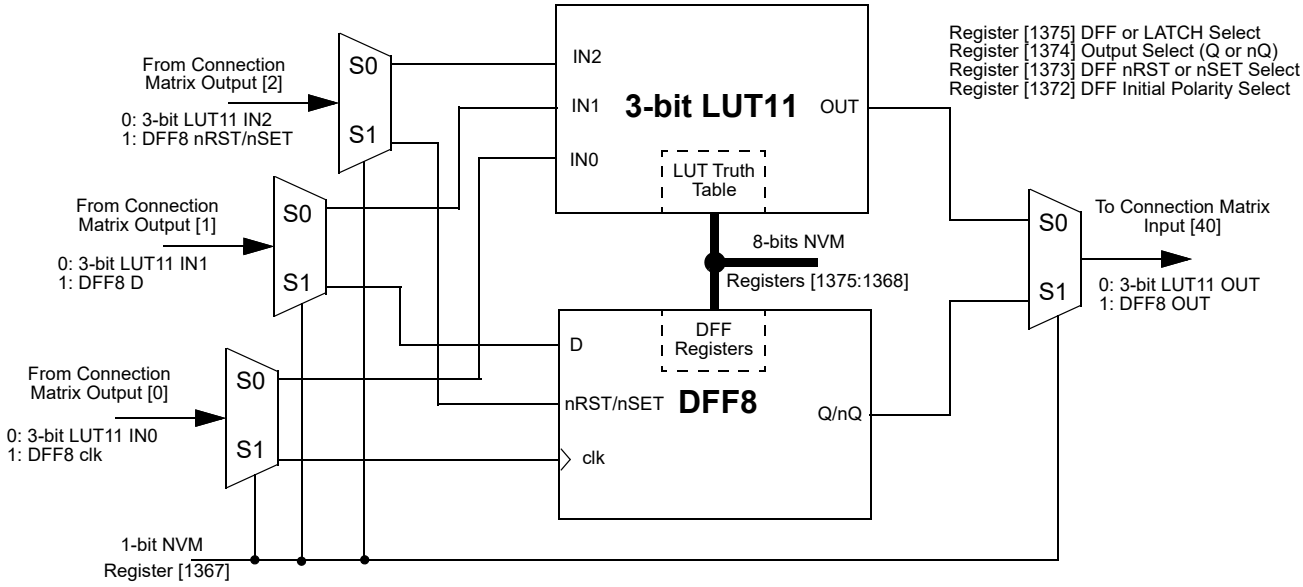


Figure 23. 3-bit LUT11 or DFF8 with RST/SET

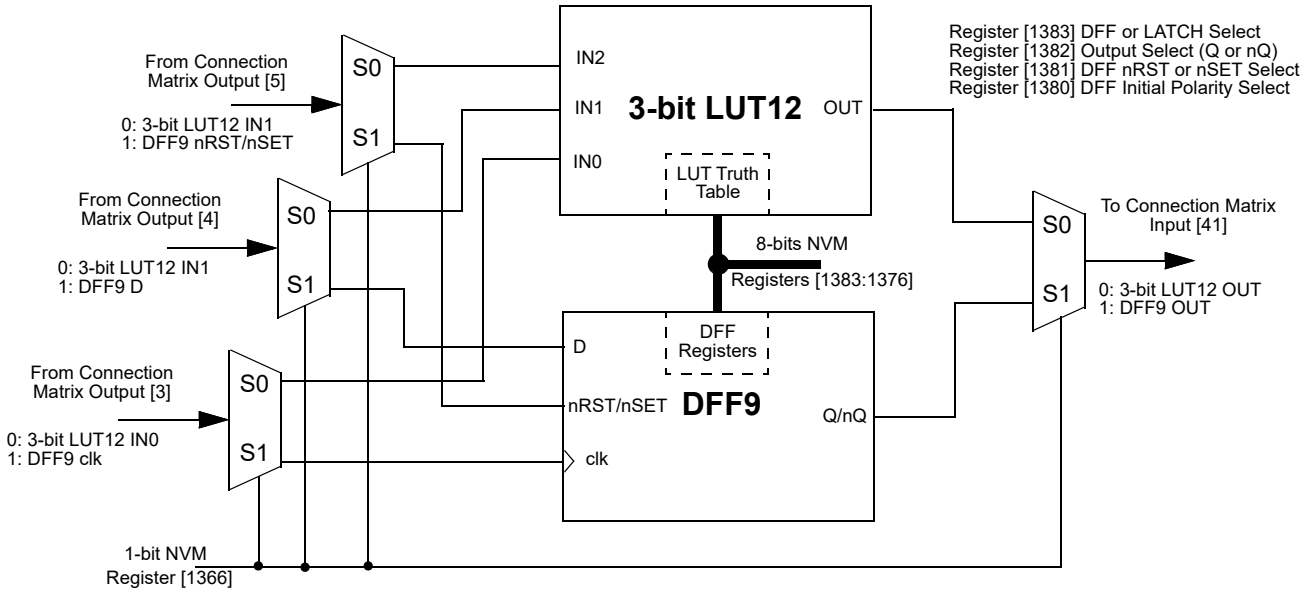


Figure 24. 3-bit LUT12 or DFF9 with RST/SET

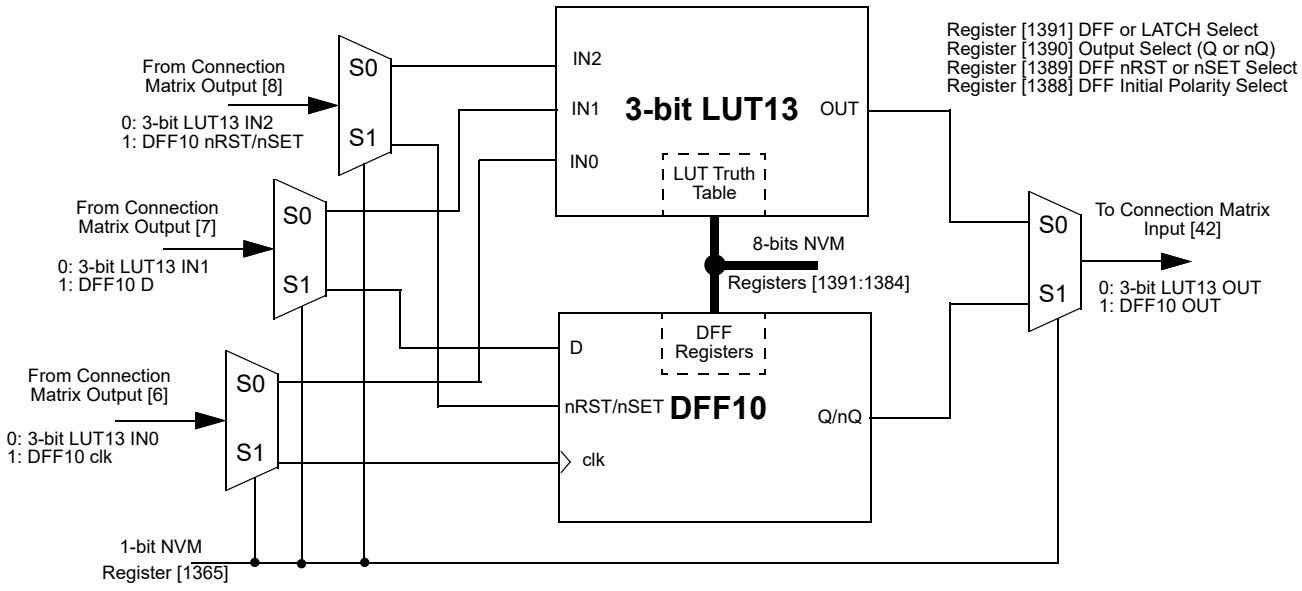


Figure 25. 3-bit LUT13 or DFF10 with RST/SET

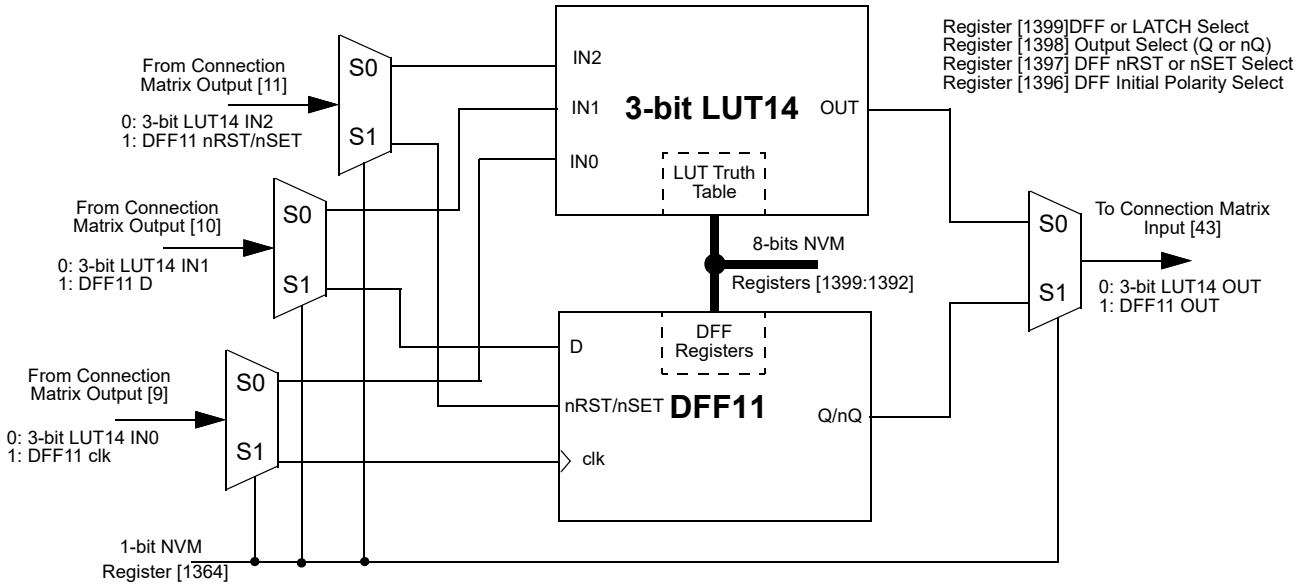


Figure 26. 3-bit LUT14 or DFF11 with RST/SET

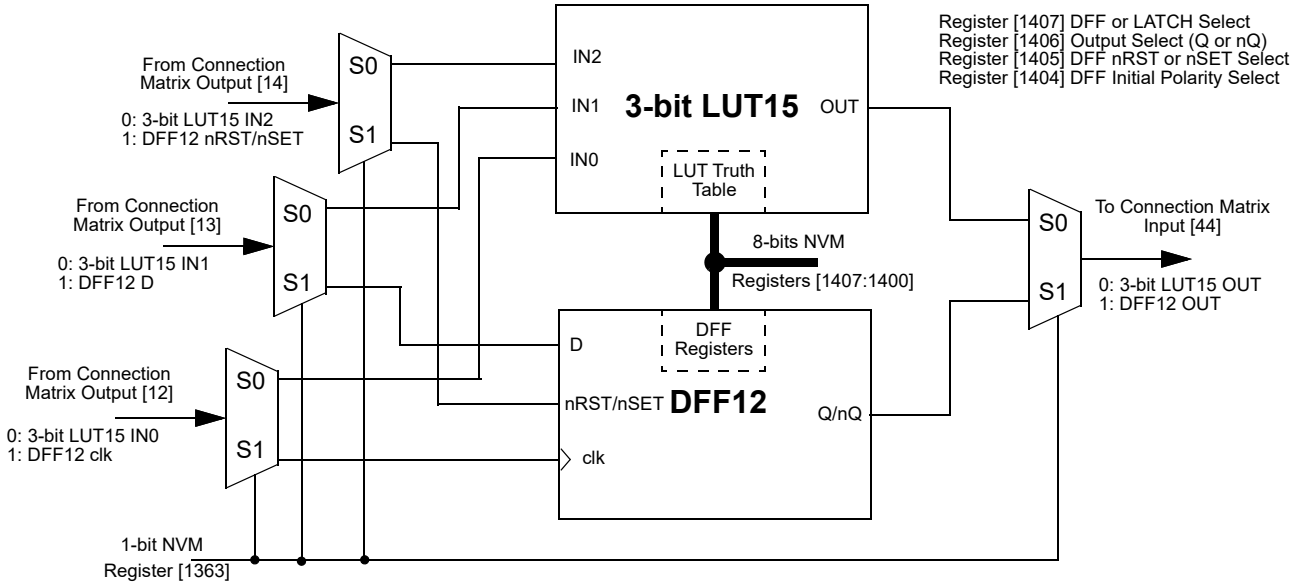


Figure 27. 3-bit LUT15 or DFF12 with RST/SET

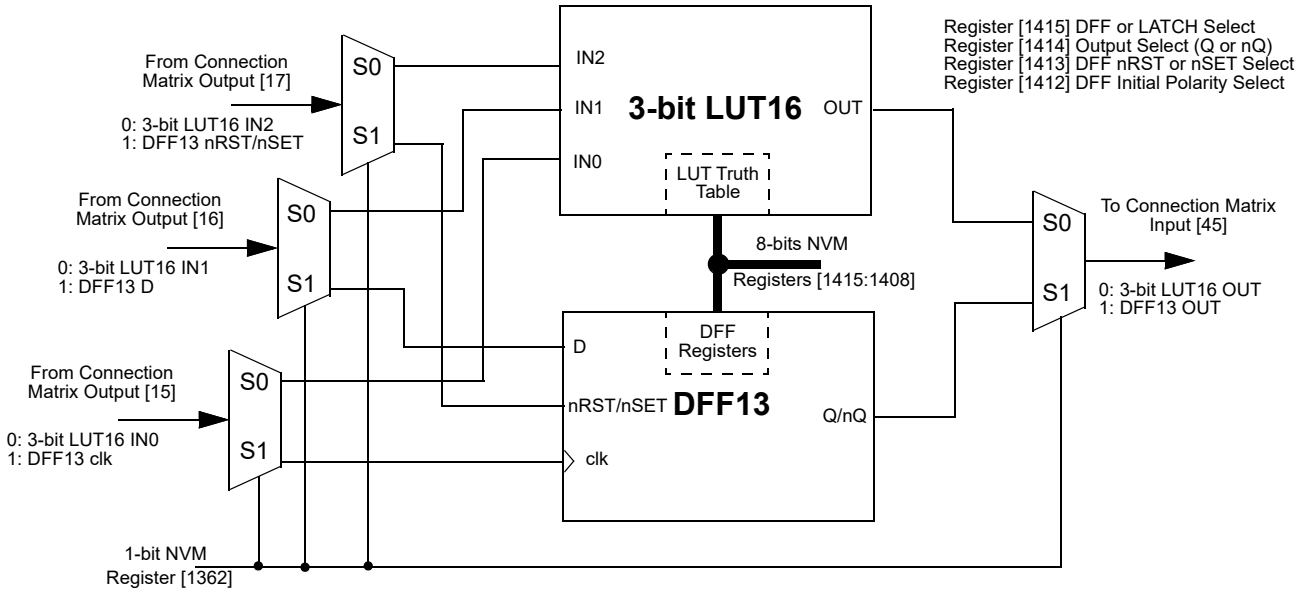


Figure 28. 3-bit LUT16 or DFF13 with RST/SET

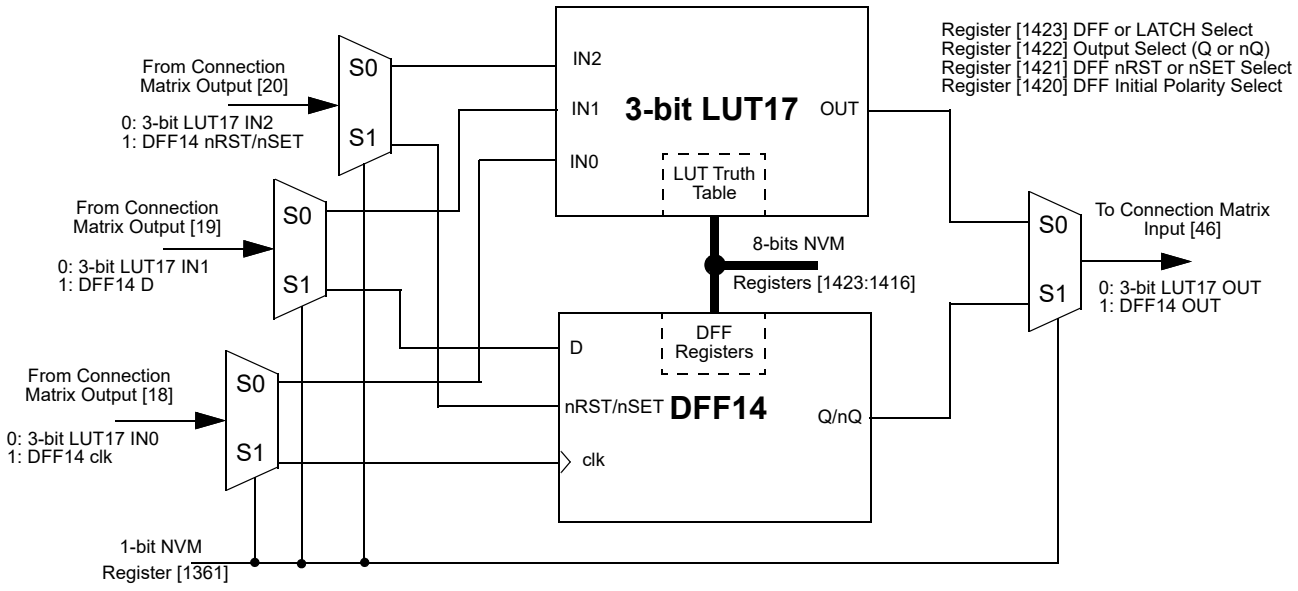


Figure 29. 3-bit LUT17 or DFF14 with RST/SET

7.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 11. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1216]	LSB
0	0	1	register [1217]	
0	1	0	register [1218]	
0	1	1	register [1219]	
1	0	0	register [1220]	
1	0	1	register [1221]	
1	1	0	register [1222]	
1	1	1	register [1223]	MSB

Table 12. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Table 13. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1232]	LSB
0	0	1	register [1233]	
0	1	0	register [1234]	
0	1	1	register [1235]	
1	0	0	register [1236]	
1	0	1	register [1237]	
1	1	0	register [1238]	
1	1	1	register [1239]	MSB

Table 14. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1240]	LSB
0	0	1	register [1241]	
0	1	0	register [1242]	
0	1	1	register [1243]	
1	0	0	register [1244]	
1	0	1	register [1245]	
1	1	0	register [1246]	
1	1	1	register [1247]	MSB

Table 15. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1248]	LSB
0	0	1	register [1249]	
0	1	0	register [1250]	
0	1	1	register [1251]	
1	0	0	register [1252]	
1	0	1	register [1253]	
1	1	0	register [1254]	
1	1	1	register [1255]	MSB

Table 16. 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1368]	LSB
0	0	1	register [1369]	
0	1	0	register [1370]	
0	1	1	register [1371]	
1	0	0	register [1372]	
1	0	1	register [1373]	
1	1	0	register [1374]	
1	1	1	register [1375]	MSB

Table 17. 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1376]	LSB
0	0	1	register [1377]	
0	1	0	register [1378]	
0	1	1	register [1379]	
1	0	0	register [1380]	
1	0	1	register [1381]	
1	1	0	register [1382]	
1	1	1	register [1383]	MSB

Table 18. 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1384]	LSB
0	0	1	register [1385]	
0	1	0	register [1386]	
0	1	1	register [1387]	
1	0	0	register [1388]	
1	0	1	register [1389]	
1	1	0	register [1390]	
1	1	1	register [1391]	MSB

Table 19. 3-bit LUT14 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1392]	LSB
0	0	1	register [1393]	
0	1	0	register [1394]	
0	1	1	register [1395]	
1	0	0	register [1396]	
1	0	1	register [1397]	
1	1	0	register [1398]	
1	1	1	register [1399]	MSB

Table 20. 3-bit LUT15 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1400]	LSB
0	0	1	register [1401]	
0	1	0	register [1402]	
0	1	1	register [1403]	
1	0	0	register [1404]	
1	0	1	register [1405]	
1	1	0	register [1406]	
1	1	1	register [1407]	MSB

Table 21. 3-bit LUT16 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1408]	LSB
0	0	1	register [1409]	
0	1	0	register [1410]	
0	1	1	register [1411]	
1	0	0	register [1412]	
1	0	1	register [1413]	
1	1	0	register [1414]	
1	1	1	register [1415]	MSB

Table 22. 3-bit LUT17 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1416]	LSB
0	0	1	register [1417]	
0	1	0	register [1418]	
0	1	1	register [1419]	
1	0	0	register [1420]	
1	0	1	register [1421]	
1	1	0	register [1422]	
1	1	1	register [1423]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT0 is defined by registers [1223:1216]
- 3-bit LUT1 is defined by registers [1231:1224]
- 3-bit LUT2 is defined by registers [1239:1232]
- 3-bit LUT3 is defined by registers [1247:1240]
- 3-bit LUT4 is defined by registers [1255:1248]
- 3-bit LUT11 is defined by registers [1375:1368]

- 3-bit LUT12 is defined by registers [1383:1376]
- 3-bit LUT13 is defined by registers [1391:1384]
- 3-bit LUT14 is defined by registers [1399:1392]
- 3-bit LUT15 is defined by registers [1407:1400]
- 3-bit LUT16 is defined by registers [1415:1408]
- 3-bit LUT17 is defined by registers [1423:1416].

Table 23 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR), that can be created within each of the six 3-bit LUT logic cells.

Table 23. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.2.2 Initial Polarity Operations

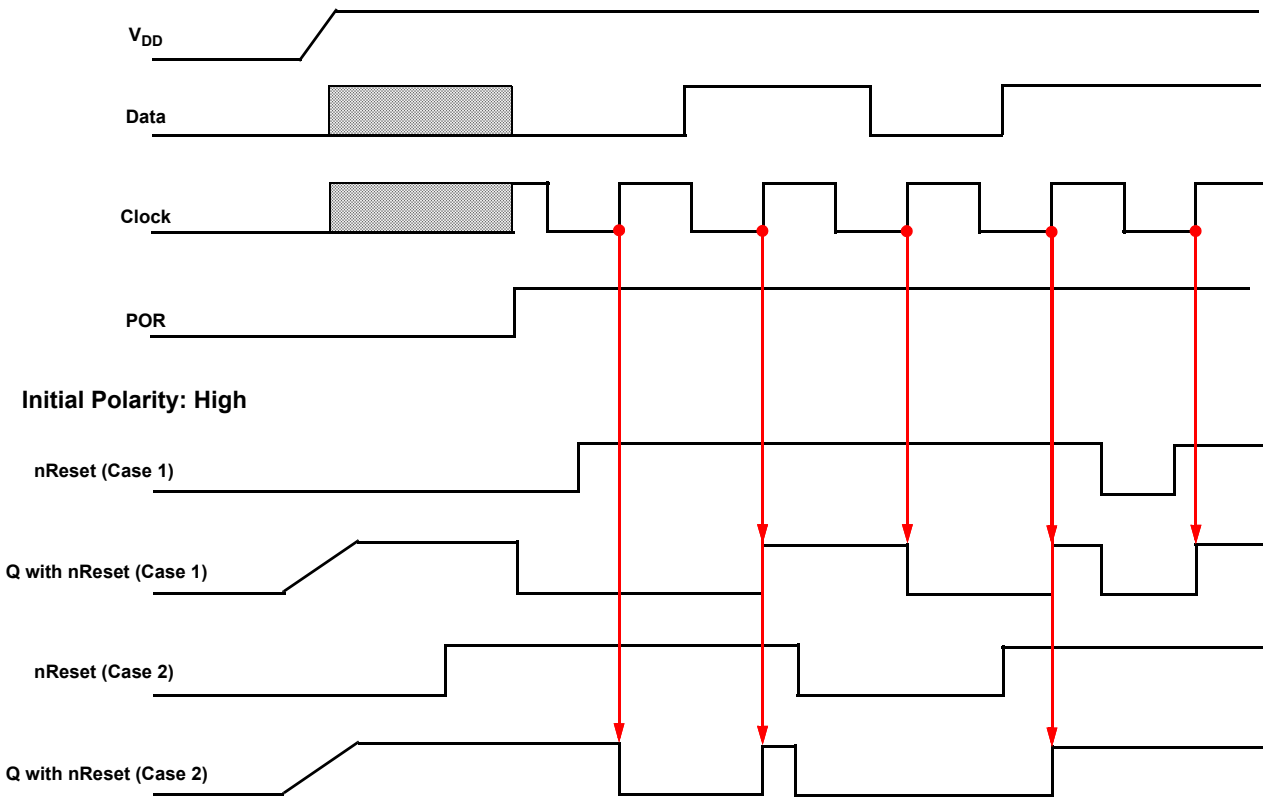


Figure 30. DFF Polarity Operations

7.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three output options, two of which are user selectable. The DFF cells are tied in series, where the output (Q) of each delay cell goes to the next DFF cell. The first delay option is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 16-input MUX that is controlled by registers [1259:1256] for OUT0 and registers [1263:1260] for OUT1. The 16-input MUX is used to select the amount of delay.

The overall time of the delay is based on the clock used in the SLG46535-EV design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the Oscillator within the SLG46535-EV). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

Note: CLK is rising edge triggered.

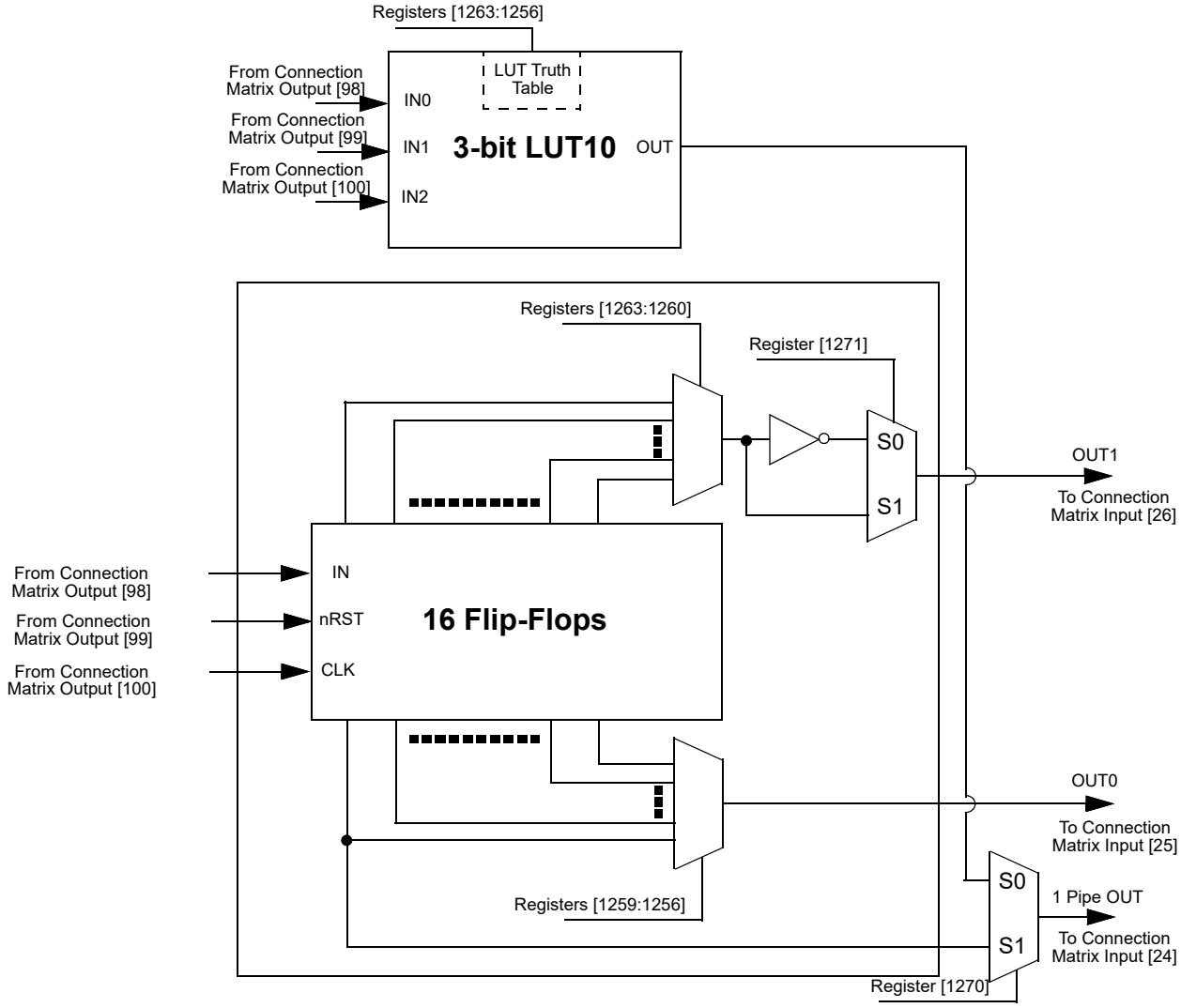


Figure 31. 3-bit LUT10 or Pipe Delay

7.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 24. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1256]	LSB
0	0	1	register [1257]	
0	1	0	register [1258]	
0	1	1	register [1259]	
1	0	0	register [1260]	
1	0	1	register [1261]	
1	1	0	register [1262]	
1	1	1	register [1263]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT10 is defined by registers [1263:1256].

7.4 3-Bit LUT or 8-Bit Counter/Delay Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as Counter/Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter/Delay function, two of the three input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_in/CNT_Reset) for the Counter/Delay, with the output going back to the connection matrix.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

For timing diagrams refer to section 7.6 CNT/DLY/FSM Timing Diagrams

Note: Counters initialize with counter data after POR.

Two of the five macrocells can have their active count value read via I^2C (CNT4 and CNT6). See section 16.6.1 Reading Counter Data via I2C for further details.

7.4.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

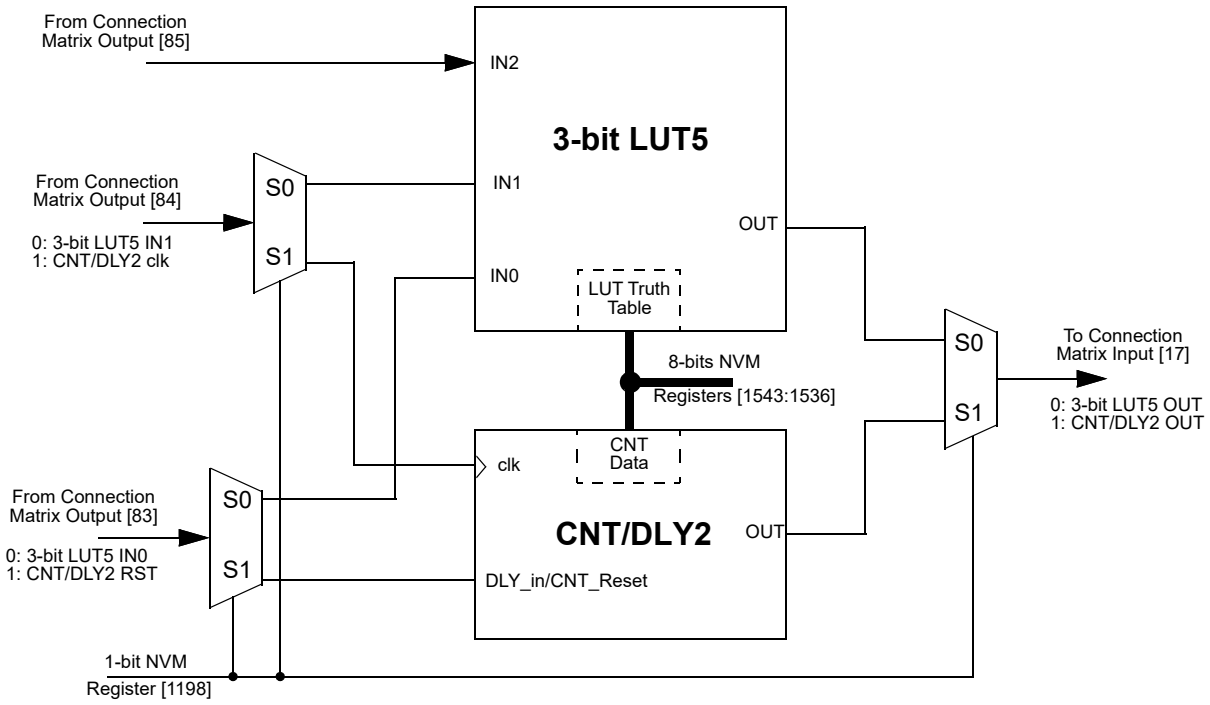


Figure 32. 3-bit LUT5 or CNT/DLY2

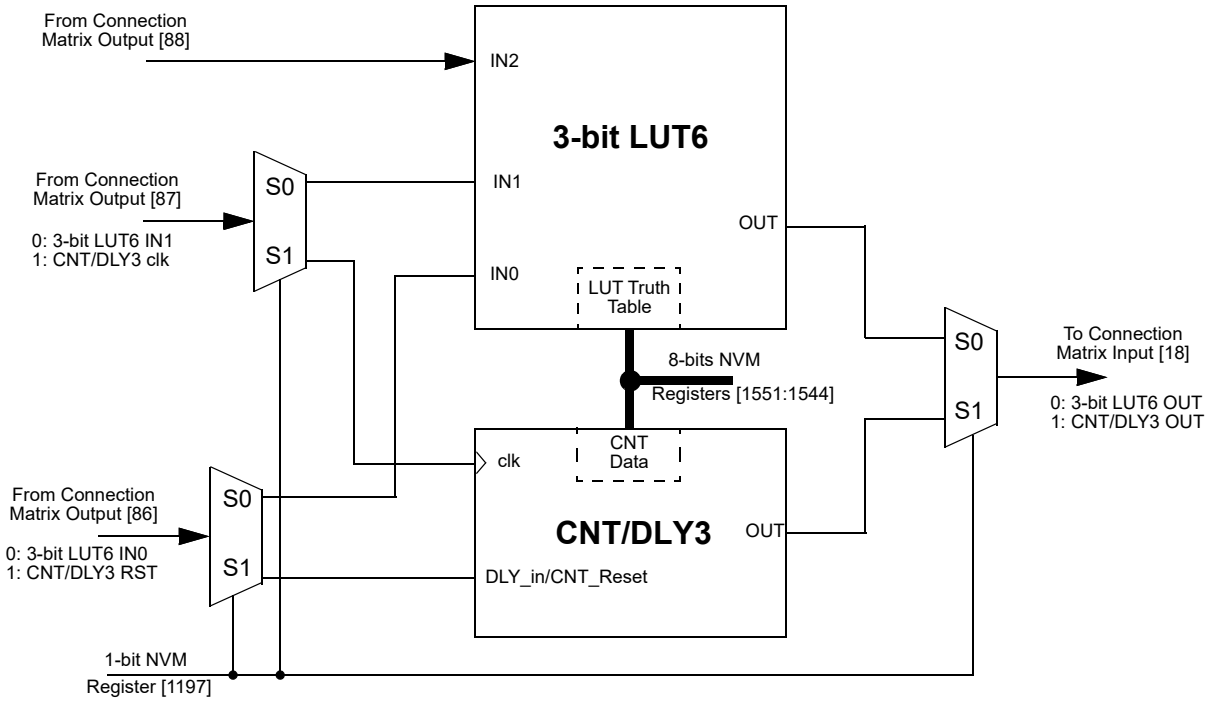


Figure 33. 3-bit LUT6 or CNT/DLY3

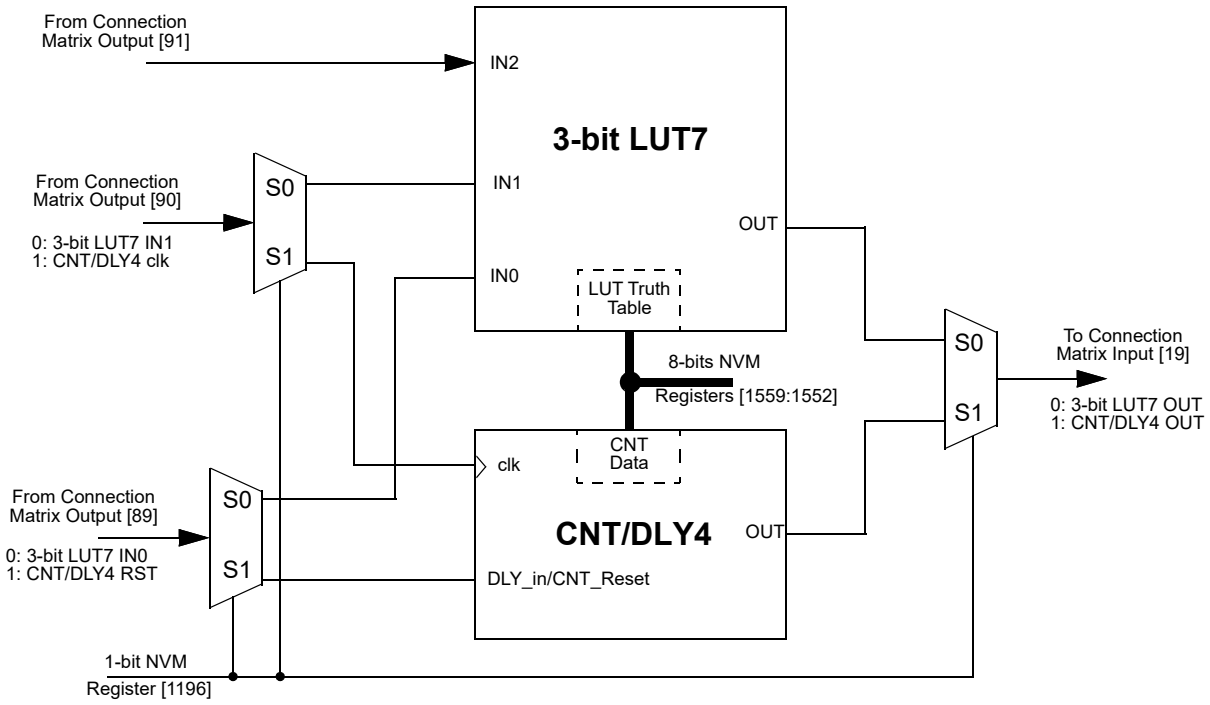


Figure 34. 3-bit LUT7 or CNT/DLY4

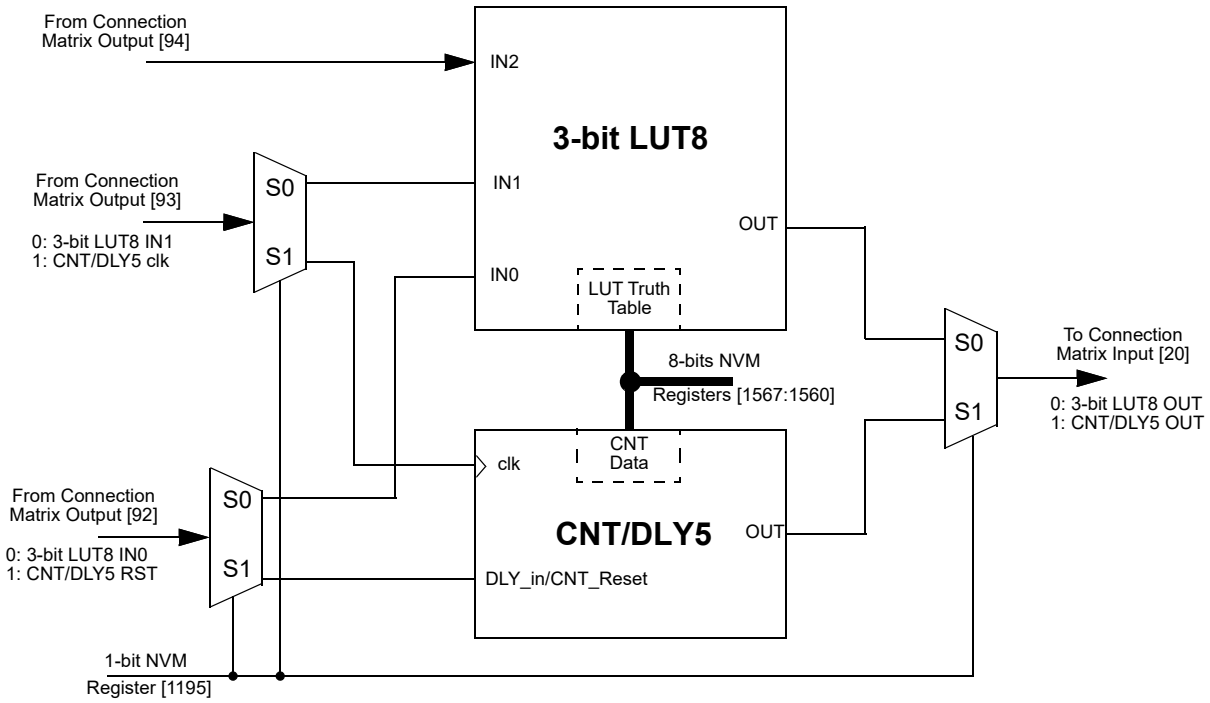


Figure 35. 3-bit LUT8 or CNT/DLY5

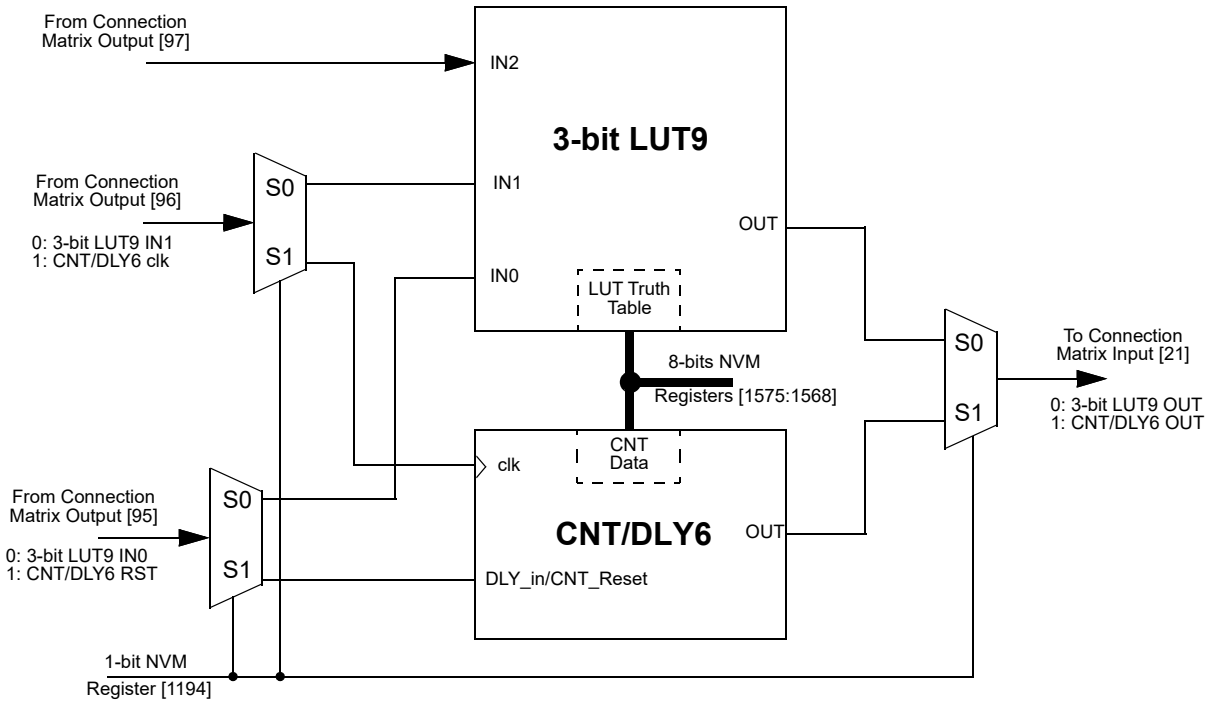


Figure 36. 3-bit LUT9 or CNT/DLY6

7.4.2 3-Bit LUT or Counter/Delay Macrocells Used as 3-Bit LUTs

Table 25. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1536]	LSB
0	0	1	register [1537]	
0	1	0	register [1538]	
0	1	1	register [1539]	
1	0	0	register [1540]	
1	0	1	register [1541]	
1	1	0	register [1542]	
1	1	1	register [1543]	MSB

Table 26. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1544]	LSB
0	0	1	register [1545]	
0	1	0	register [1546]	
0	1	1	register [1547]	
1	0	0	register [1548]	
1	0	1	register [1549]	
1	1	0	register [1550]	
1	1	1	register [1551]	MSB

Table 27. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1552]	LSB
0	0	1	register [1553]	
0	1	0	register [1554]	
0	1	1	register [1555]	
1	0	0	register [1556]	
1	0	1	register [1557]	
1	1	0	register [1558]	
1	1	1	register [1559]	MSB

Table 28. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1560]	LSB
0	0	1	register [1561]	
0	1	0	register [1562]	
0	1	1	register [1563]	
1	0	0	register [1564]	
1	0	1	register [1565]	
1	1	0	register [1566]	
1	1	1	register [1567]	MSB

Table 29. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1568]	LSB
0	0	1	register [1569]	
0	1	0	register [1570]	
0	1	1	register [1571]	
1	0	0	register [1572]	
1	0	1	register [1573]	
1	1	0	register [1574]	
1	1	1	register [1575]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT5 is defined by registers [1543:1536]
- 3-bit LUT6 is defined by registers [1551:1544]
- 3-bit LUT7 is defined by registers [1559:1552]
- 3-bit LUT8 is defined by registers [1567:1560]
- 3-bit LUT9 is defined by registers [1575:1568].

7.5 4-Bit LUT or 16-Bit Counter/Delay Macrocells

There are two macrocells that can serve as either 4-bit LUTs or as 16-bit Counter/Delays. When used to implement LUT function, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 16-Bit Counter/Delay function, four input signals from the connection matrix go to the external clock (EXT_CLK), reset (DLY_IN/CNT_Reset), Keep and Up for the Counter/Delay, with the output going back to the connection matrix.

These two macrocells have an optional Finite State Machine (FSM) function. There are two matrix inputs for Up and Keep to support FSM functionality. Any counter within GreenPAK is counting down by default. In FSM mode (CNT/DLY0 and CNT/DLY1), it is possible to reverse counting by applying High level to Up input. Also, there is a possibility to pause counting by applying High level to Keep input, after the level goes Low, the counter will proceed counting.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection.

Delay time and Output Period can be calculated using the following formulas:

- Delay time: [(Counter data + 2)/CLK input frequency – Offset*]
- Output Period: [(Counter data + 1)/CLK input frequency – Offset*].

One Shot pulse width can be calculated using formula:

- Pulse width = [(Counter Data + 2)/CLK input frequency – Offset*].

*Offset is the asynchronous time offset between the input signal and the first clock pulse.

Note: Counters initialize with counter data after POR.

For timing diagrams refer to section 7.6 CNT/DLY/FSM Timing Diagrams.

Both of these macrocells can have their active count value read via I^2C. See section 16.6.1 Reading Counter Data via I2C for further details.

7.5.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

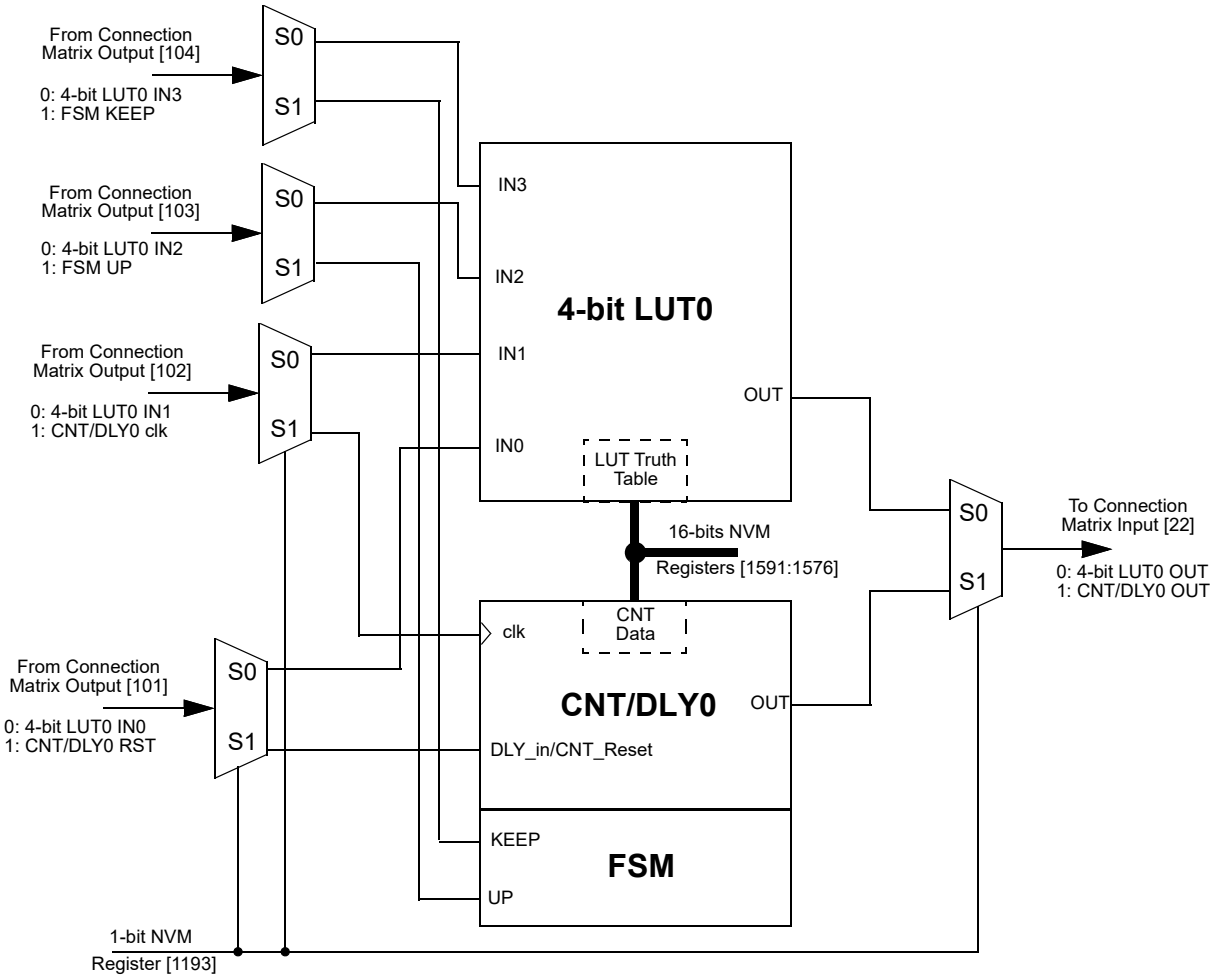


Figure 37. 4-bit LUT0 or CNT/DLY0

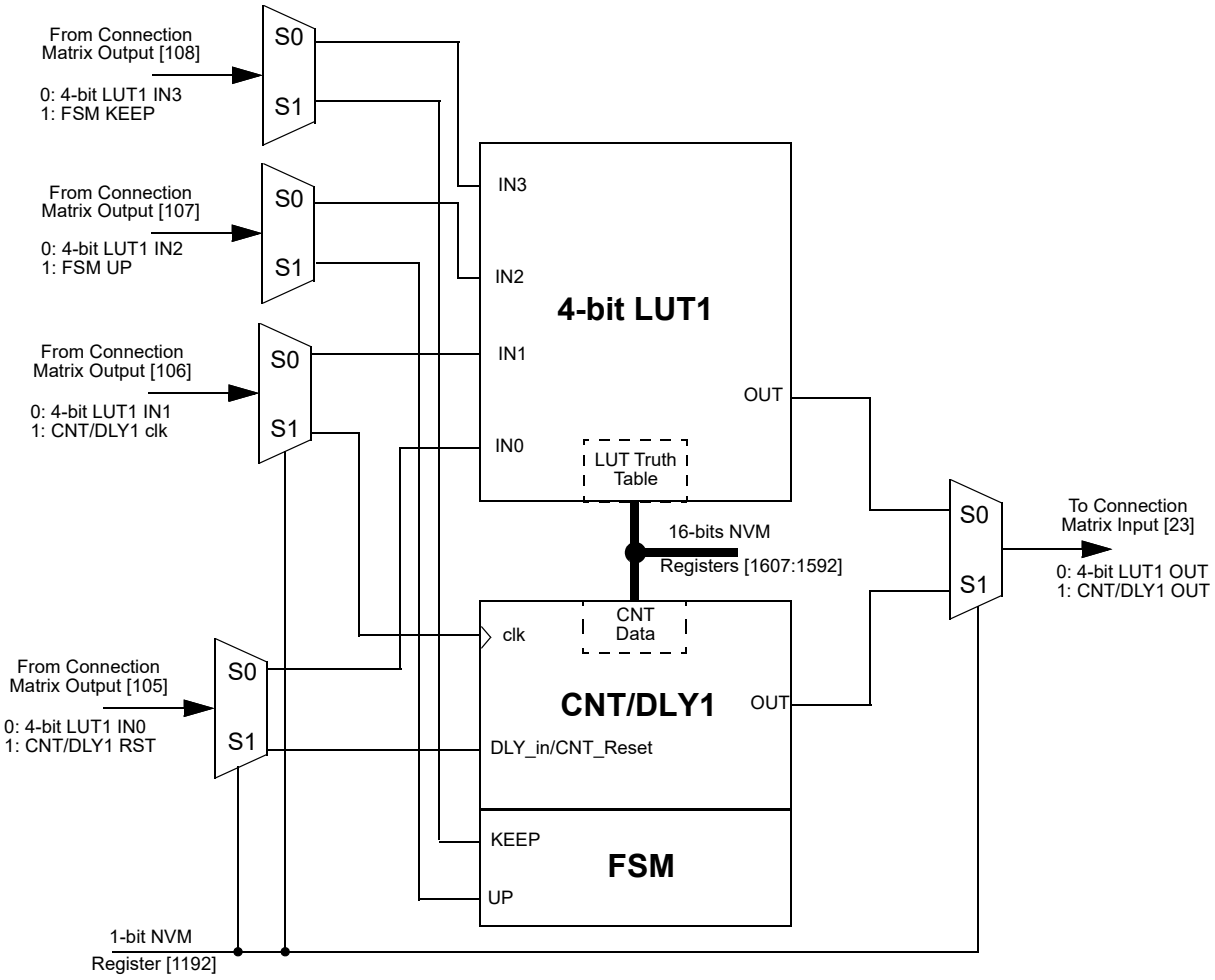


Figure 38. 4-bit LUT1 or CNT/DLY1

7.5.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 30. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1576]	LSB
0	0	0	1	register [1577]	
0	0	1	0	register [1578]	
0	0	1	1	register [1579]	
0	1	0	0	register [1580]	
0	1	0	1	register [1581]	
0	1	1	0	register [1582]	
0	1	1	1	register [1583]	
1	0	0	0	register [1584]	
1	0	0	1	register [1585]	
1	0	1	0	register [1586]	
1	0	1	1	register [1587]	
1	1	0	0	register [1588]	
1	1	0	1	register [1589]	
1	1	1	0	register [1590]	
1	1	1	1	register [1591]	MSB

Table 31. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1592]	LSB
0	0	0	1	register [1593]	
0	0	1	0	register [1594]	
0	0	1	1	register [1595]	
0	1	0	0	register [1596]	
0	1	0	1	register [1597]	
0	1	1	0	register [1598]	
0	1	1	1	register [1599]	
1	0	0	0	register [1600]	
1	0	0	1	register [1601]	
1	0	1	0	register [1602]	
1	0	1	1	register [1603]	
1	1	0	0	register [1604]	
1	1	0	1	register [1605]	
1	1	1	0	register [1606]	
1	1	1	1	register [1607]	MSB

Each macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-bit LUT0 is defined by registers [1591:1576]
- 4-bit LUT1 is defined by registers [1607:1592].

Table 32. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.6 CNT/DLY/FSM Timing Diagrams

7.6.1 Delay Mode (Edge Select: Both, Counter Data: 3) CNT/DLY2 to CNT/DLY6

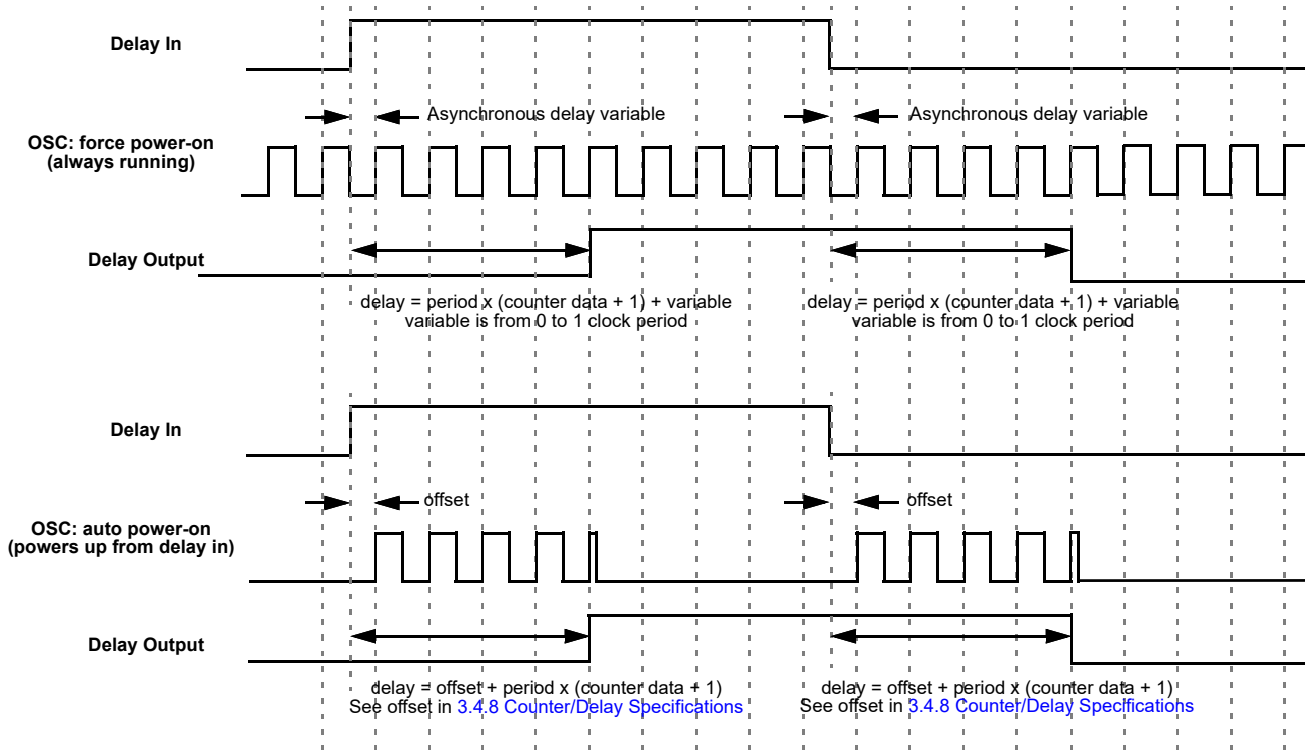


Figure 39. Delay Mode Timing Diagram

7.6.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY2 to CNT/DLY6

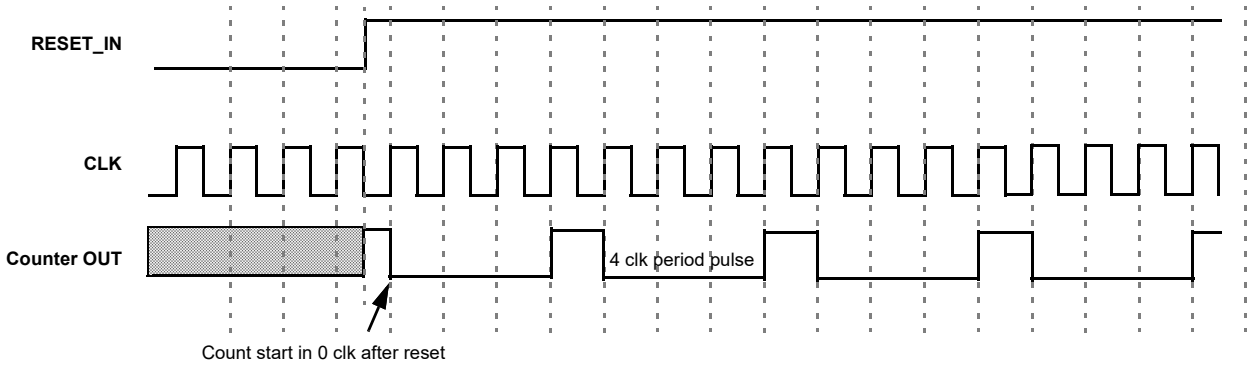


Figure 40. Counter Mode Timing Diagram

7.6.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. See Table 33. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

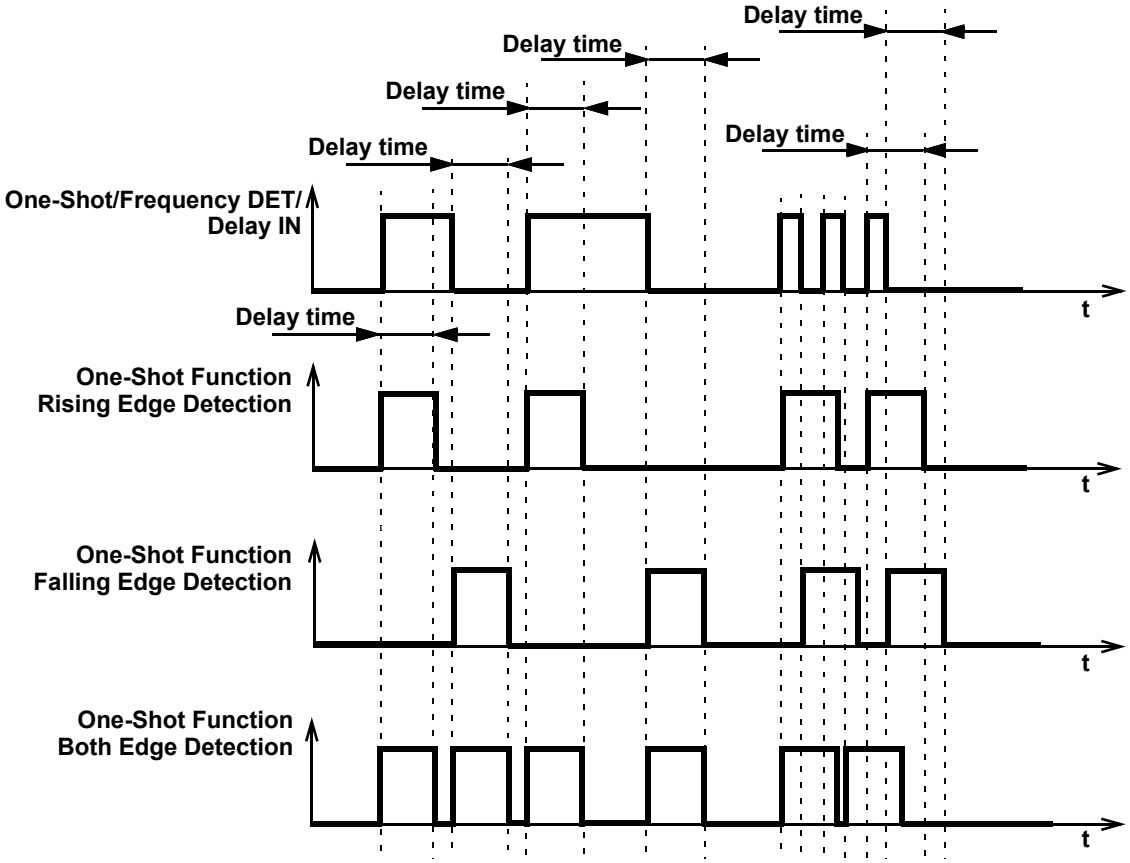


Figure 41. One-Shot Function Timing Diagram

Table 33. DLY/CNTx One-Shot/Frequency Detect Output Polarity

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A6	[1329]	Select the Polarity of DLY/CNT6's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1330]	Select the Polarity of DLY/CNT5's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1331]	Select the Polarity of DLY/CNT4's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1332]	Select the Polarity of DLY/CNT3's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1333]	Select the Polarity of DLY/CNT2's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1334]	Select the Polarity of DLY/CNT1's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1335]	Select the Polarity of DLY/CNT0's One-Shot/Frequency Detect Output	0: Default Output 1: Inverted Output	Valid	Valid

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

7.6.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: the output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: the output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: the output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

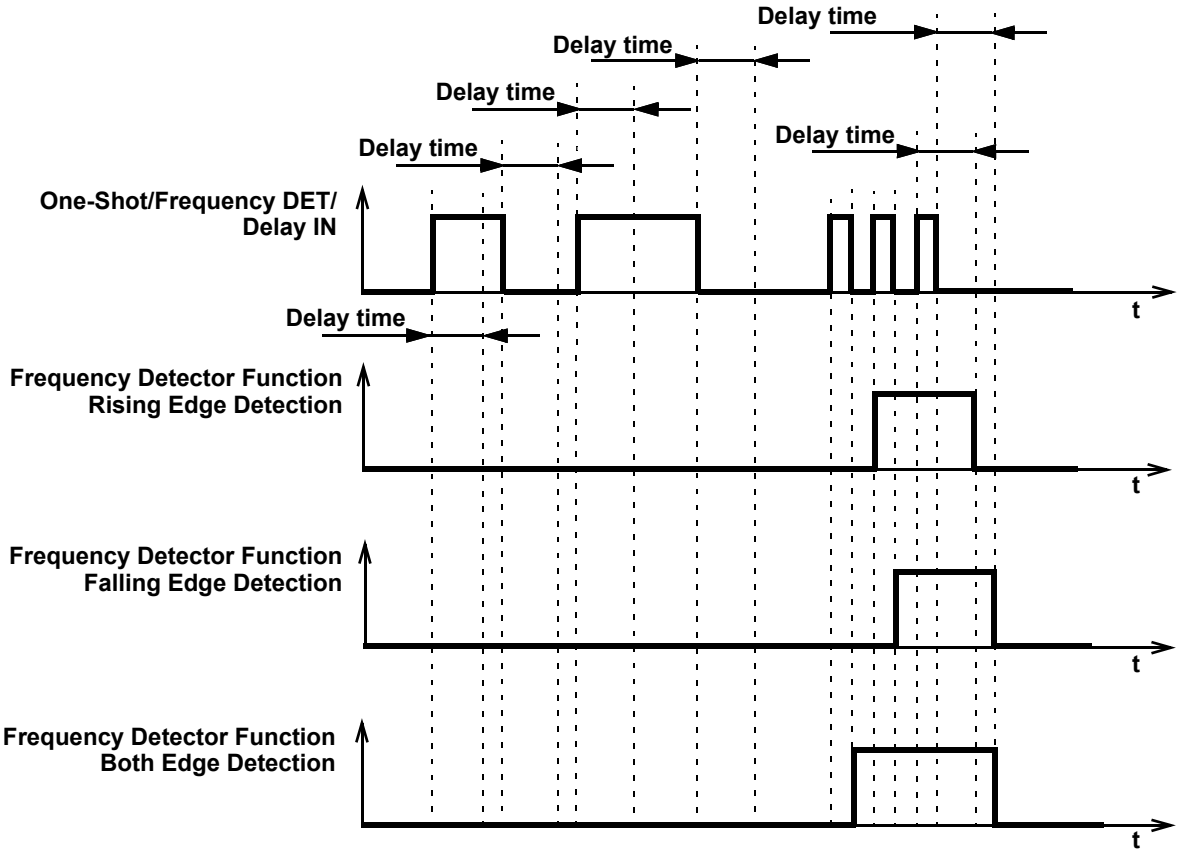


Figure 42. Frequency Detection Mode Timing Diagram

7.6.5 Edge Detection Mode CNT/DLY2 to CNT/DLY6

The macrocell generates high level short pulse when detecting the respective edge. See section 3.4.6 Programmable Delay Typical Delays and Widths.

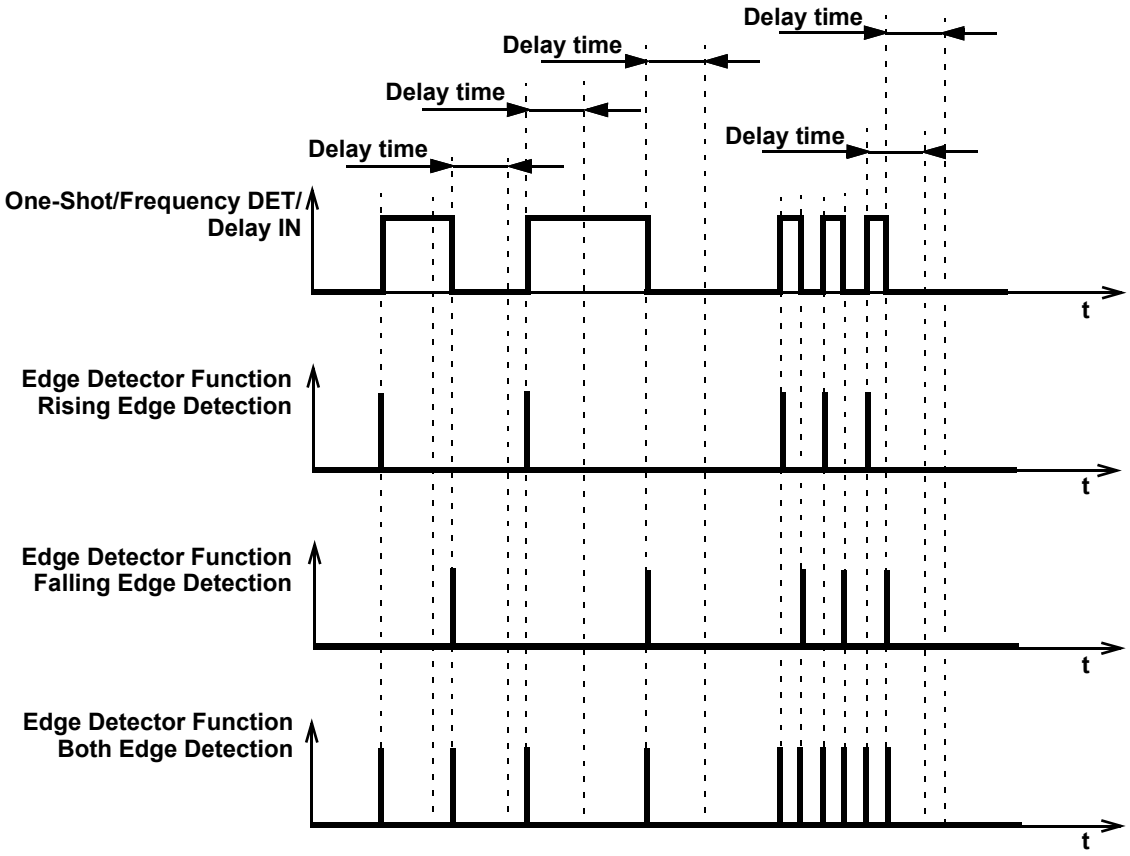


Figure 43. Edge Detection Mode Timing Diagram

7.6.6 Delay Mode CNT/DLY0 to CNT/DLY6

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

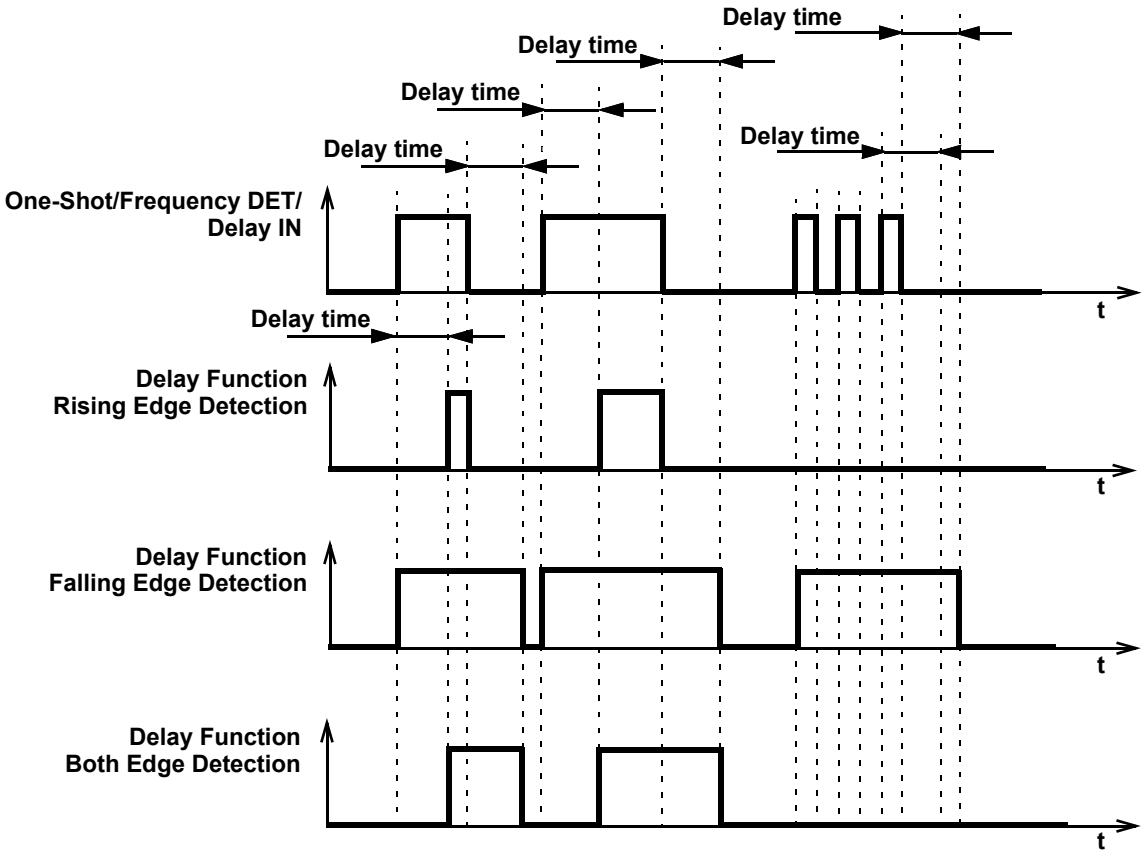


Figure 44. Delay Mode Timing Diagram

7.6.7 CNT/FSM Mode CNT/DLY0, CNT/DLY1

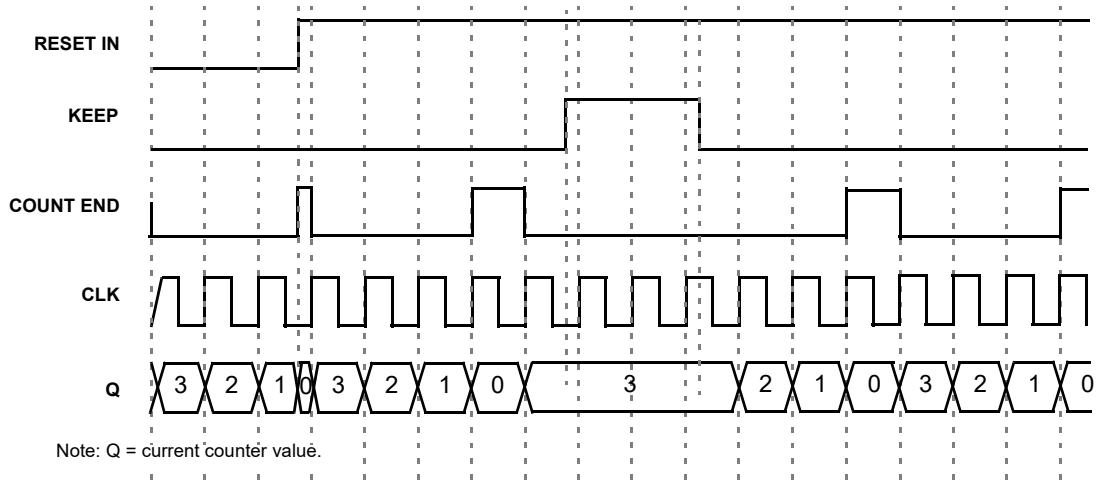


Figure 45. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

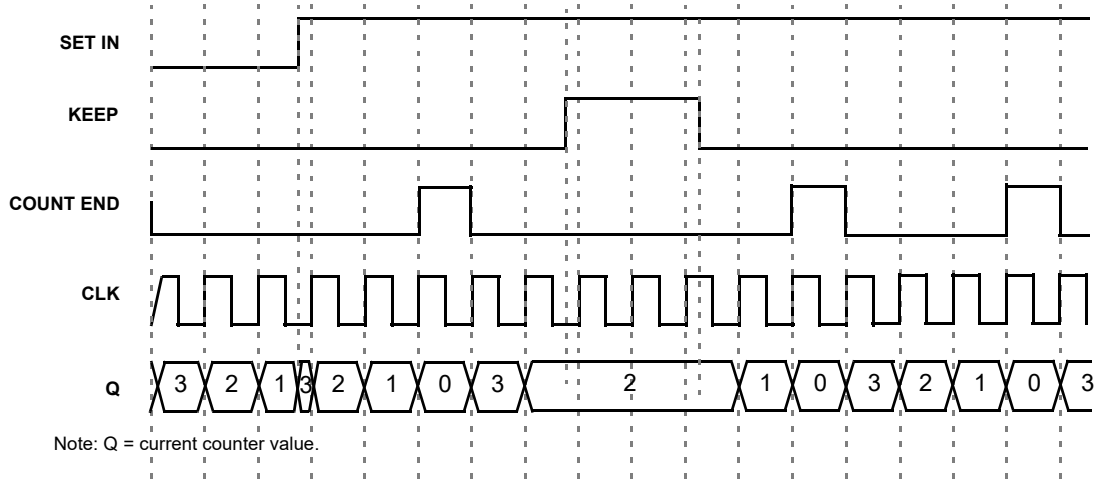


Figure 46. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

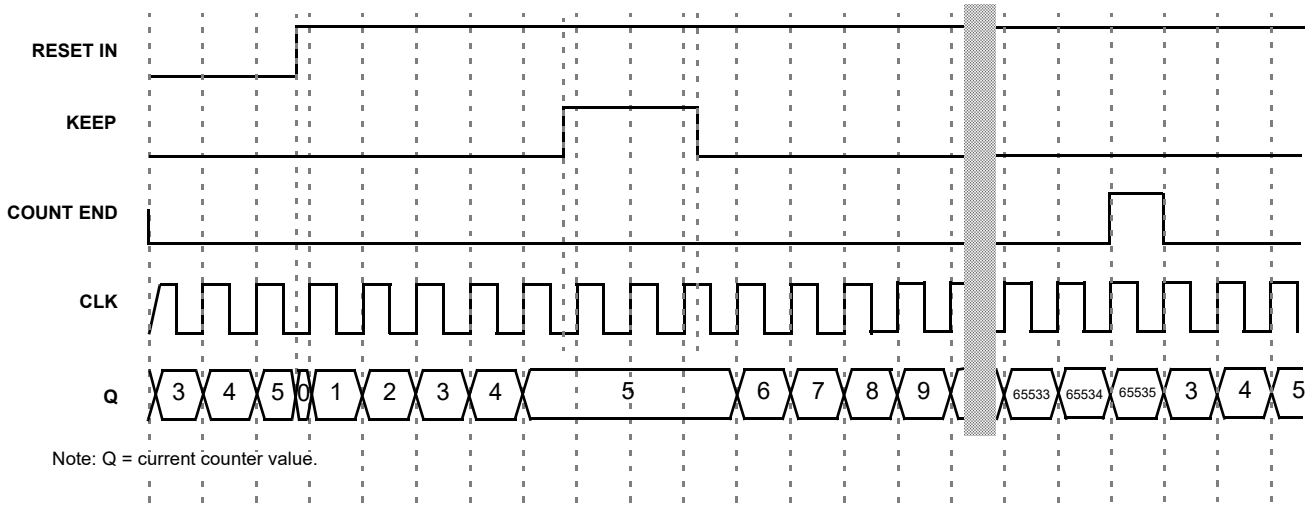


Figure 47. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

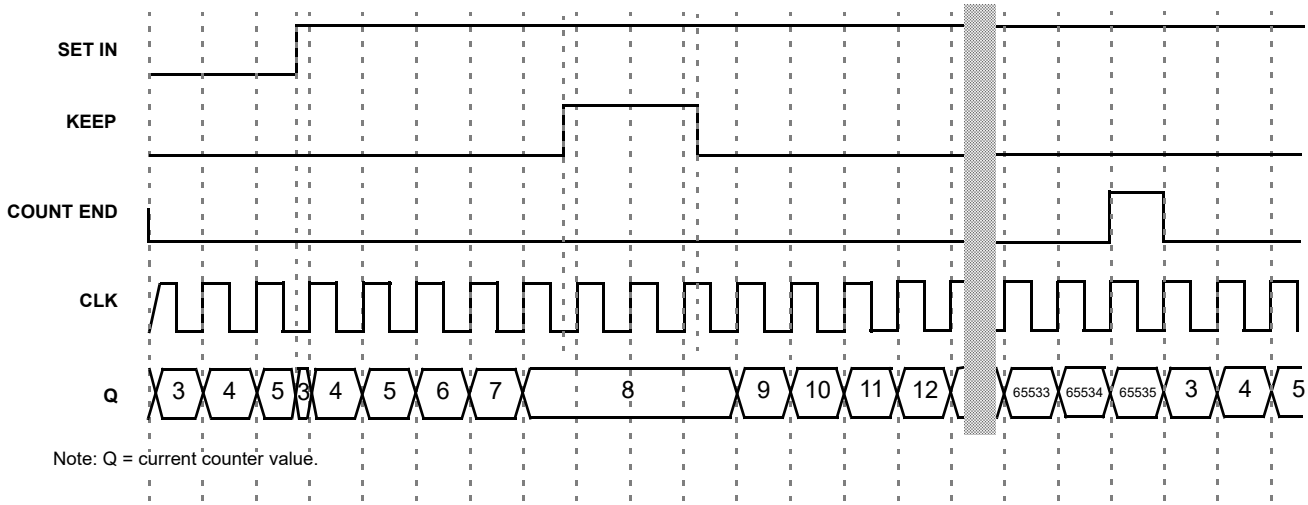


Figure 48. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

7.6.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 49.

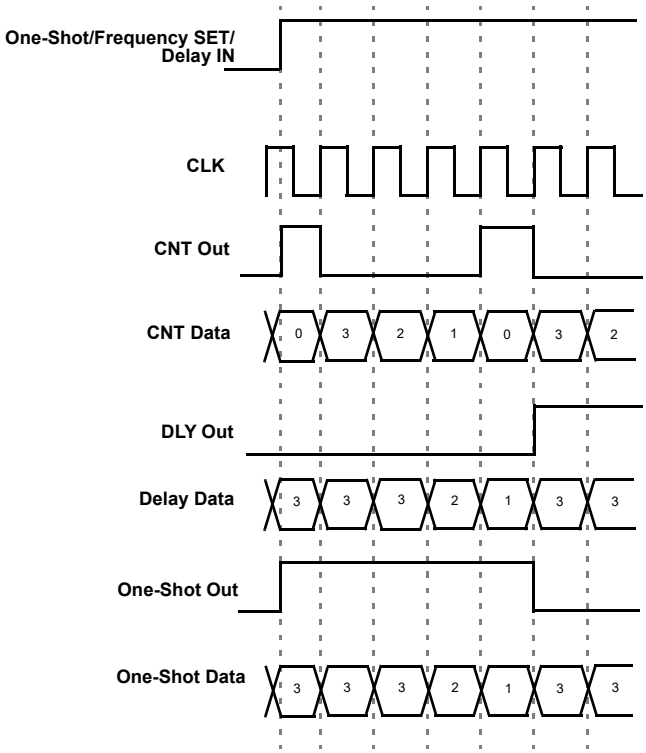


Figure 49. Counter Value, Counter Data = 3

7.7 2-bit LUT or Programmable Pattern Generator

The SLG46535-EV has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices - AND, NAND, OR, NOR, XOR, XNOR. The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats. See Figure 51.

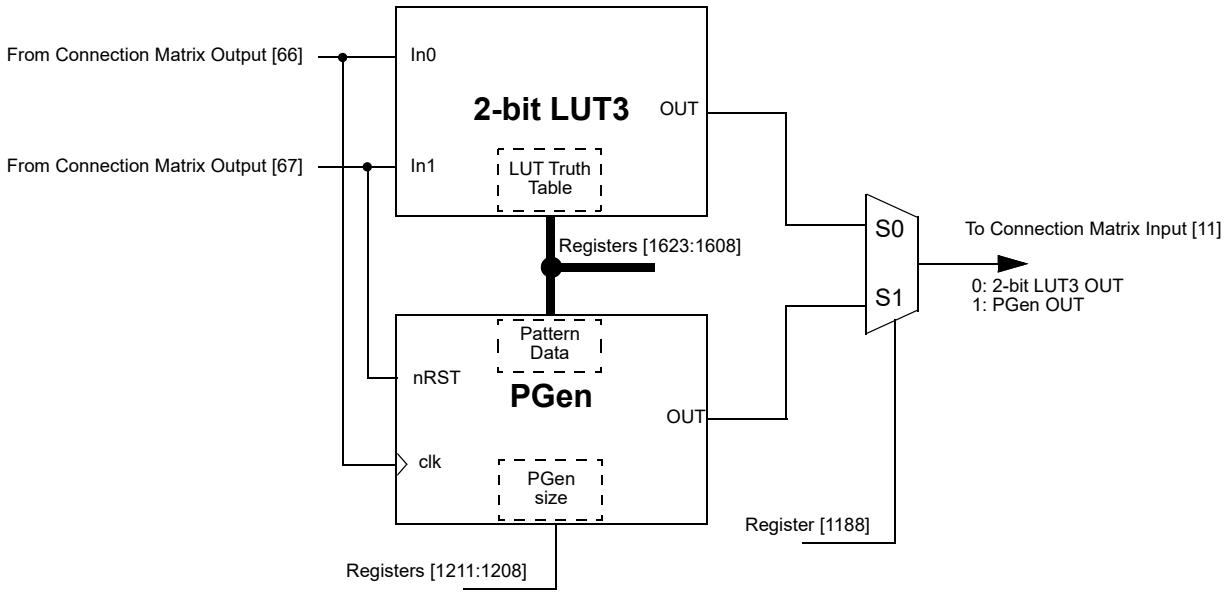


Figure 50. 2-bit LUT3 or PGen

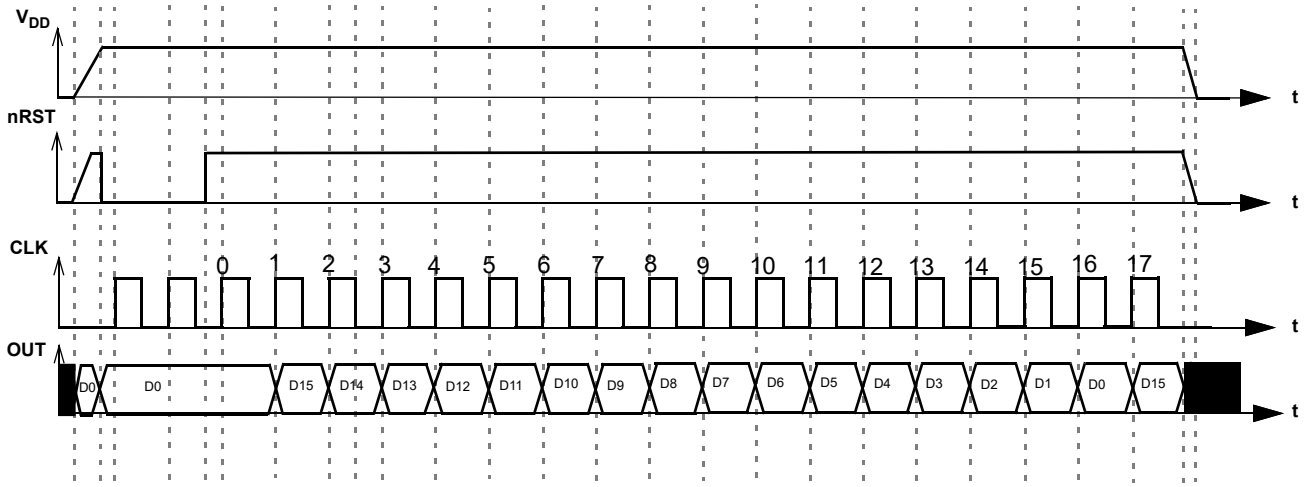


Figure 51. PGen Timing Diagram

7.8 Wake and Sleep Controller

The SLG46535-EV has a Wake and Sleep (WS) function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose, registers [1319:1318] = 11 and register [1495] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

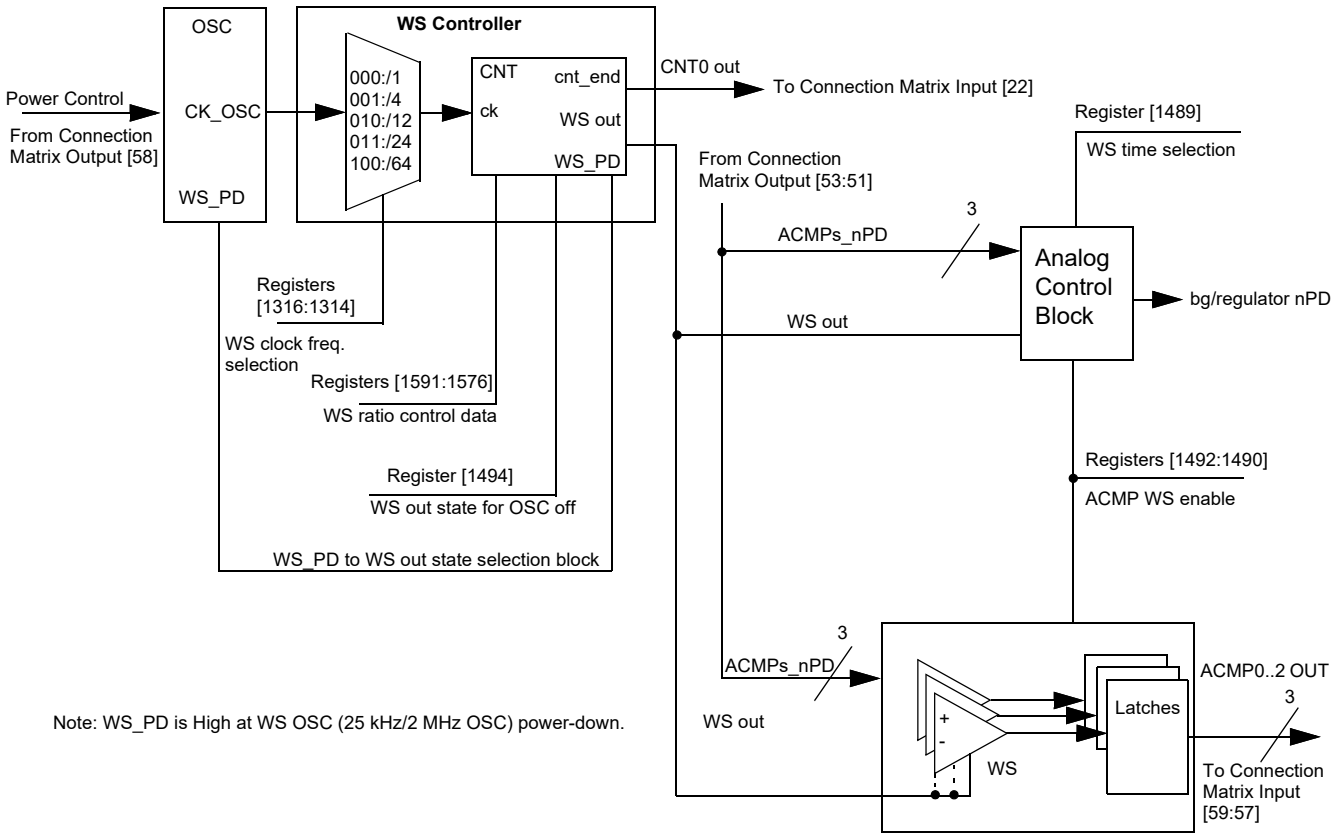


Figure 52. Wake/Sleep Controller

To use any ACMP under WS controller the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately)
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS => enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs)
- In case of using OSC1 (25 MHz), OSC0 must be set to Force Power-On.

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMPs are sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep, their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)

  If OSC is powered off (Power-Down option is selected; power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.

  If OSC is powered off (Power-Down option is selected; power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.

  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)

  The user can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears

  Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go Low and turn the ACMPs off until the counter counts up to the end.

  Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will go on counting and High level signal will turn the ACMPs on while counter is counting up to the end.

- Edge Select defines the edge for Q mode

  High level Set/Reset - switches mode Set/Reset when level is High.

  Note: Q mode operates only in case of High Level Set/Reset.

- Wake time selection - time required for wake signal to turn the ACMPs on

  Normal Wake Time - when WS signal is High, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

8. Analog Comparators

There are three Analog Comparator (ACMP) macrocells in the SLG46535-EV. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx_nPD) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. Also, all ACMPs have Wake and Sleep function (WS), see section 7.8 Wake and Sleep Controller. When ACMP is powered down, output is low.

PWR UP = 1 – ACMP is powered up.

PWR UP = 0 – ACMP is powered down.

During ACMP power up, its output will remain low, and then becomes valid 1 ms (max) after ACMP power up signal goes high, see Figure 56. The ACMP cells have an input "Low bandwidth" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the V_{DD} signal.

Note: Regulator and Charge Pump set to automatic ON/OFF.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 kΩ (typ) resistors. IN- voltage range: 0 V - 1.2 V. Can use V_{REF} selection $V_{DD}/4$ and $V_{DD}/3$ to maintain this input range.

Input bias current < 1 nA (typ).

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV, or 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be V_{REF} (high threshold) and V_{REF} - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within threshold window (between V_{REF} and V_{REF} - hysteresis). Please note: for the 25 mV hysteresis option threshold levels will be V_{REF} + hysteresis/2 (high threshold) and V_{REF} – hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on V_{REF} even when the Force BandGap option is set as Disabled.

For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer. However, this will add some offset, see Figure 57 and Figure 58. It is not recommended to use ACMP buffer when V_{DD} < 2.5 V.

8.1 ACMP0 Block Diagram

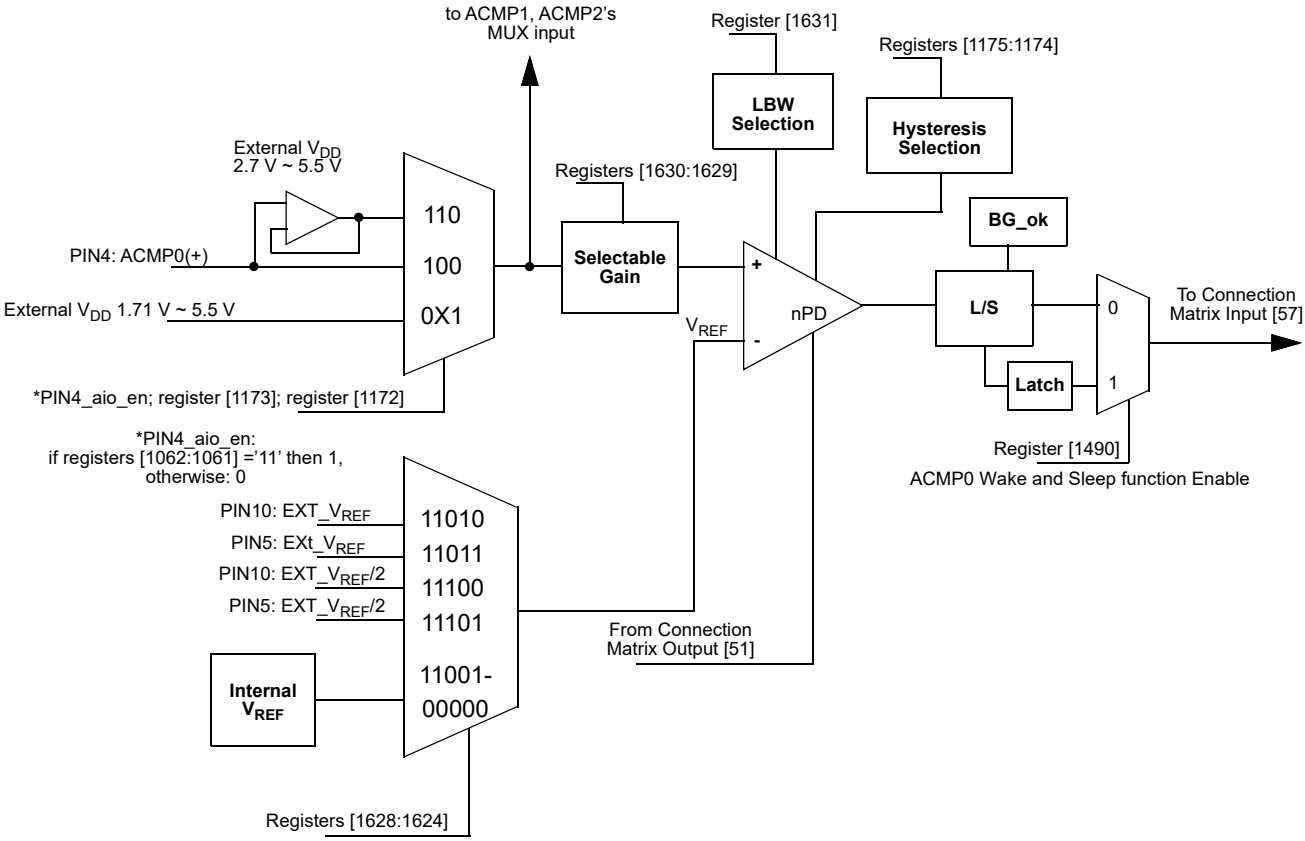
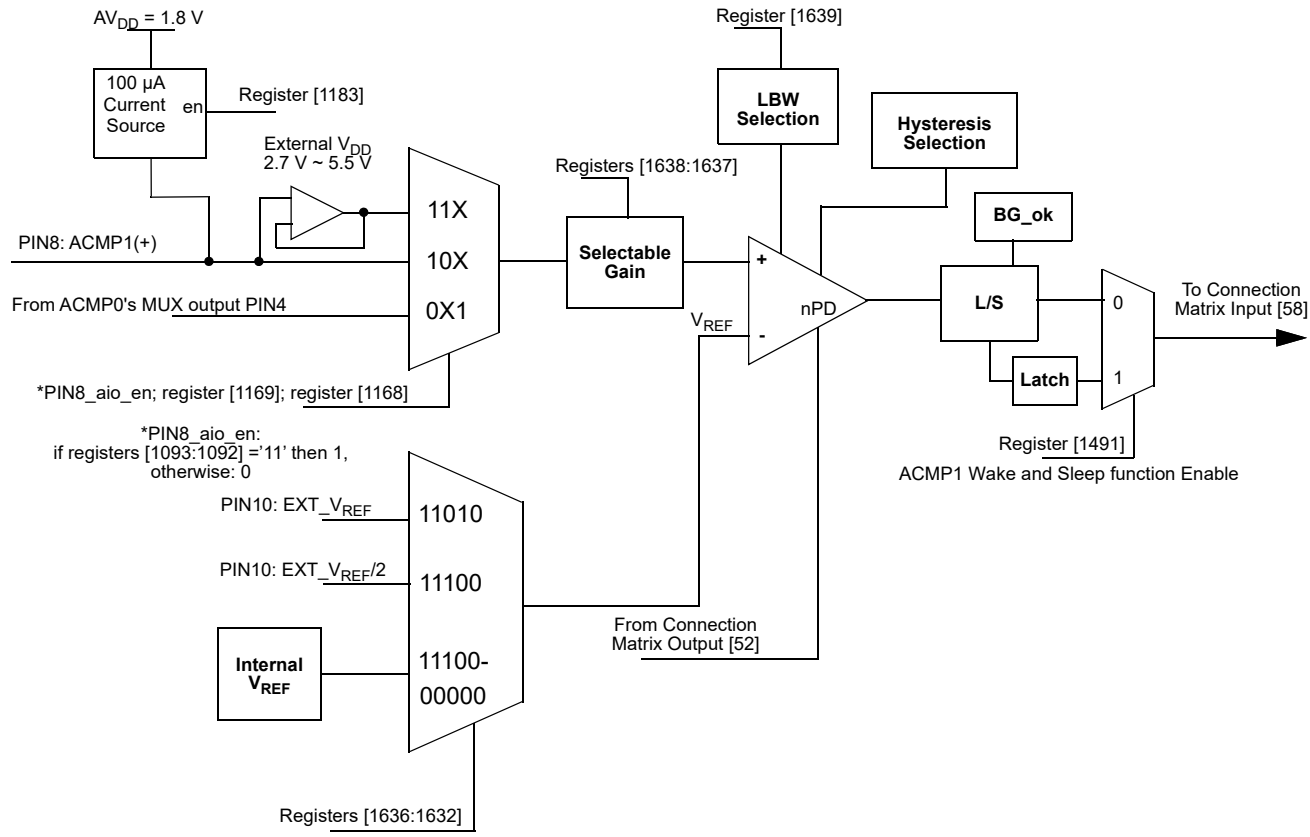


Figure 53. ACMP0 Block Diagram

8.2 ACMP1 Block Diagram



Note: when 100 µA Current Source is enabled, input voltage on Pin 8 should not exceed 1.8 V.

Figure 54. ACMP1 Block Diagram

8.3 ACMP2 Block Diagram

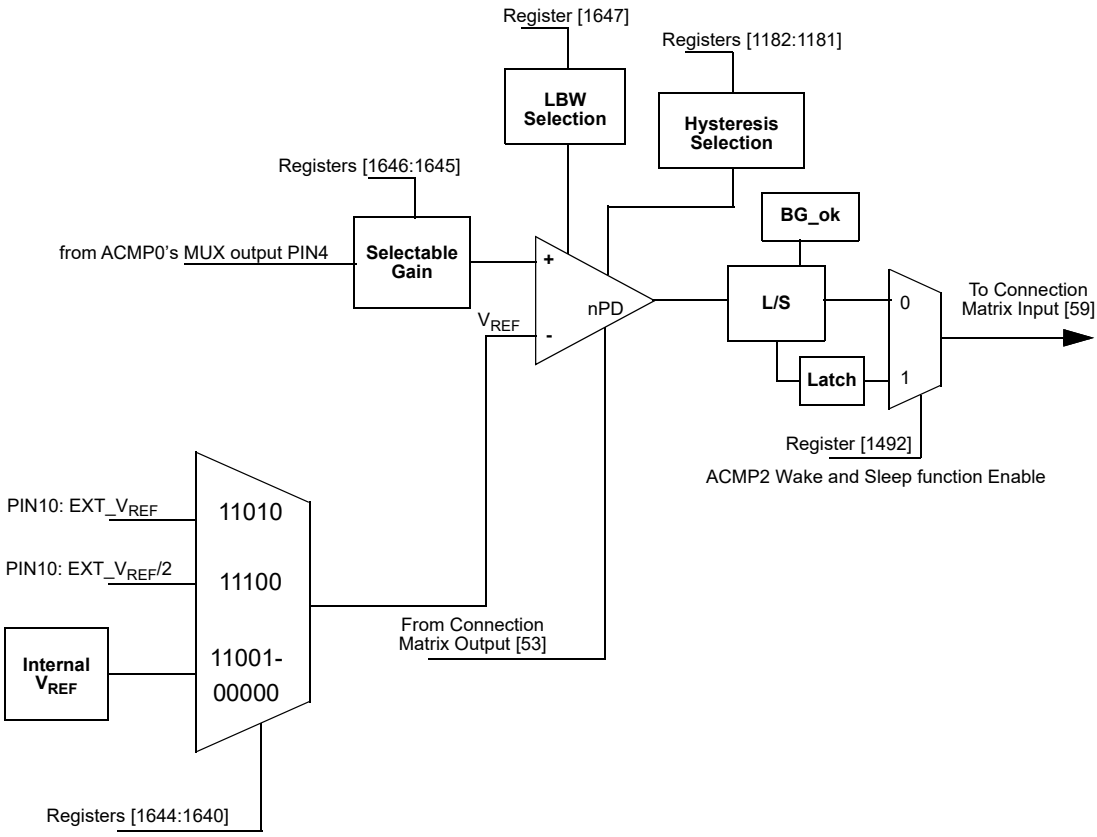


Figure 55. ACMP2 Block Diagram

8.4 ACMP Typical Performance

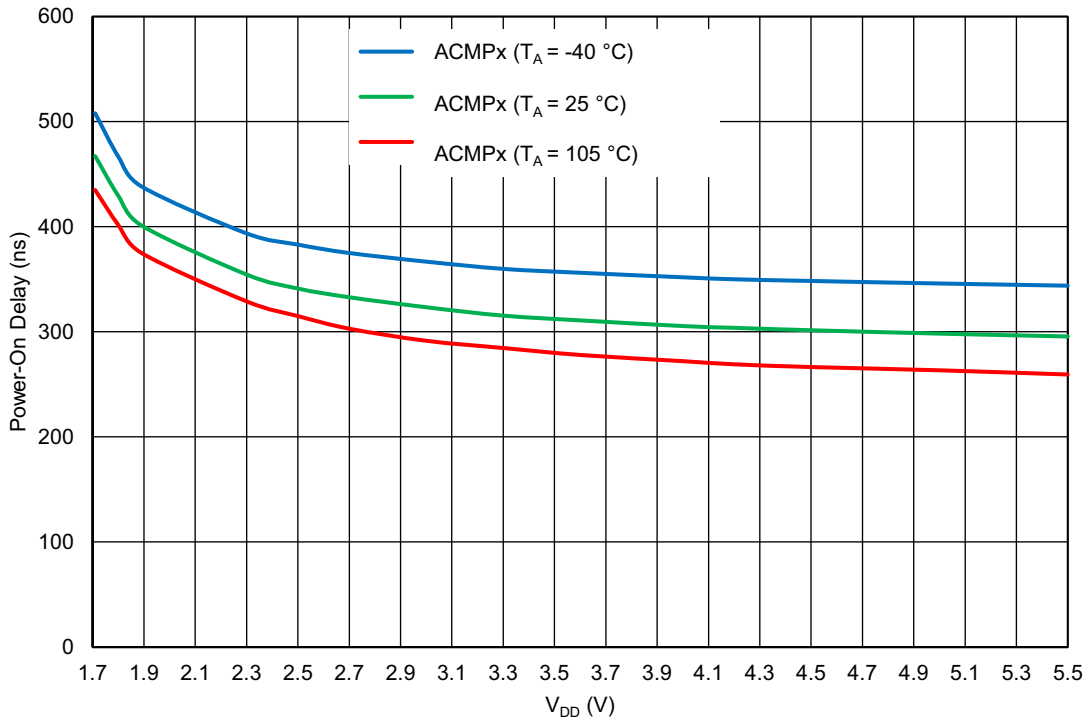


Figure 56. ACMPx Power-On Delay vs. V_{DD}, BG Delay – Any

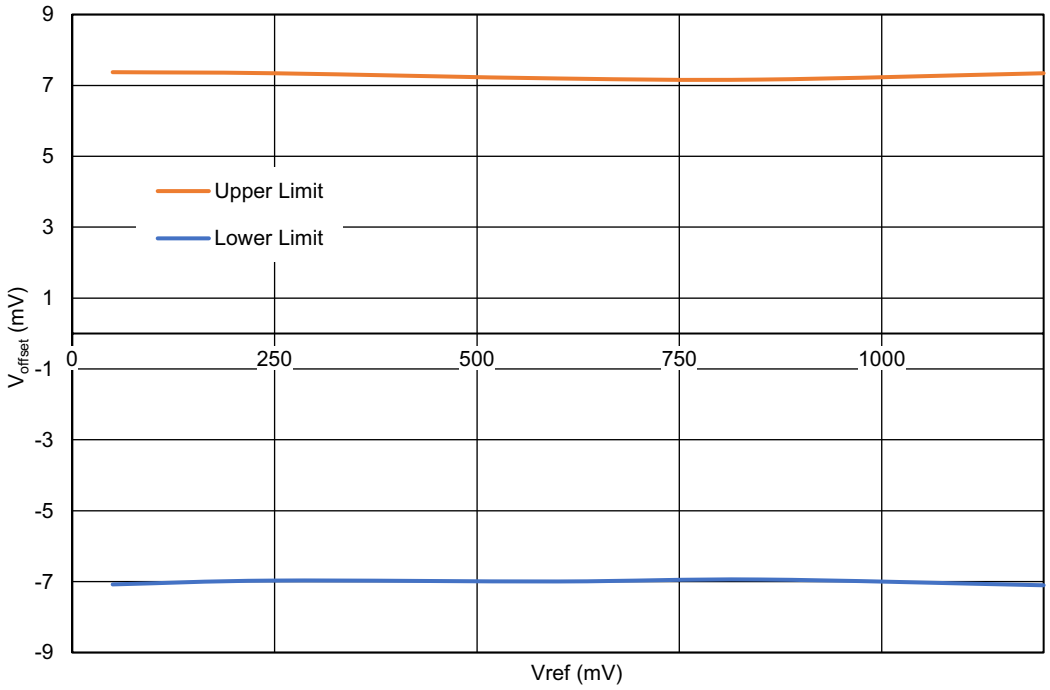


Figure 57. ACMPx Input Offset Voltage vs. V_{REF} at V_{DD} = 1.71 V to 5.5 V, T_A = -40 °C to +105°C

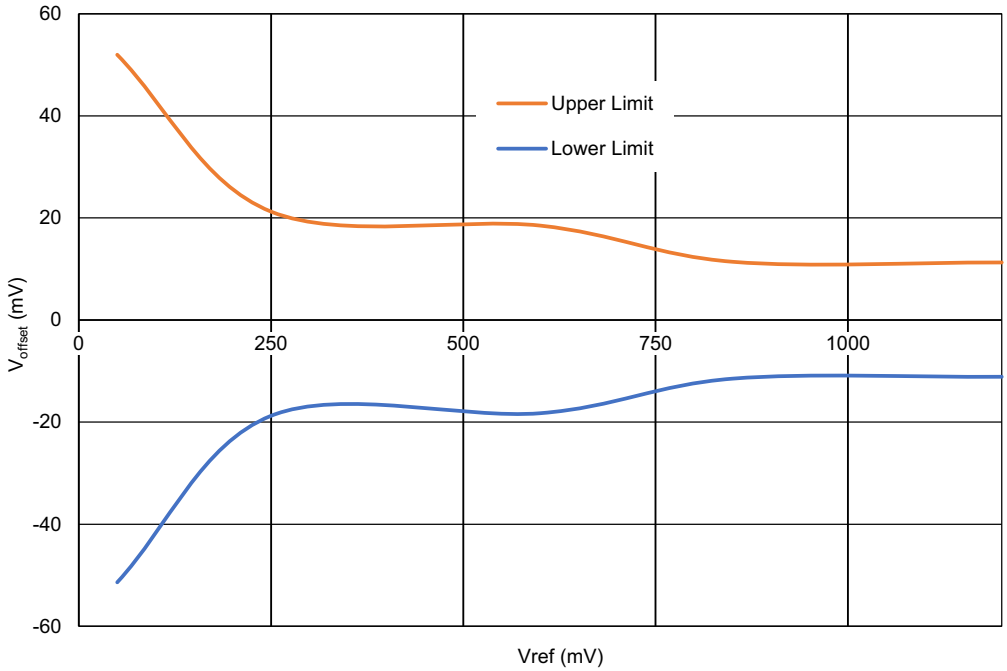


Figure 58. ACMPx Buffer Input Offset Voltage vs. V_{REF} at V_{DD} = 1.71 V to 5.5 V, T_A = -40 °C to +105°C

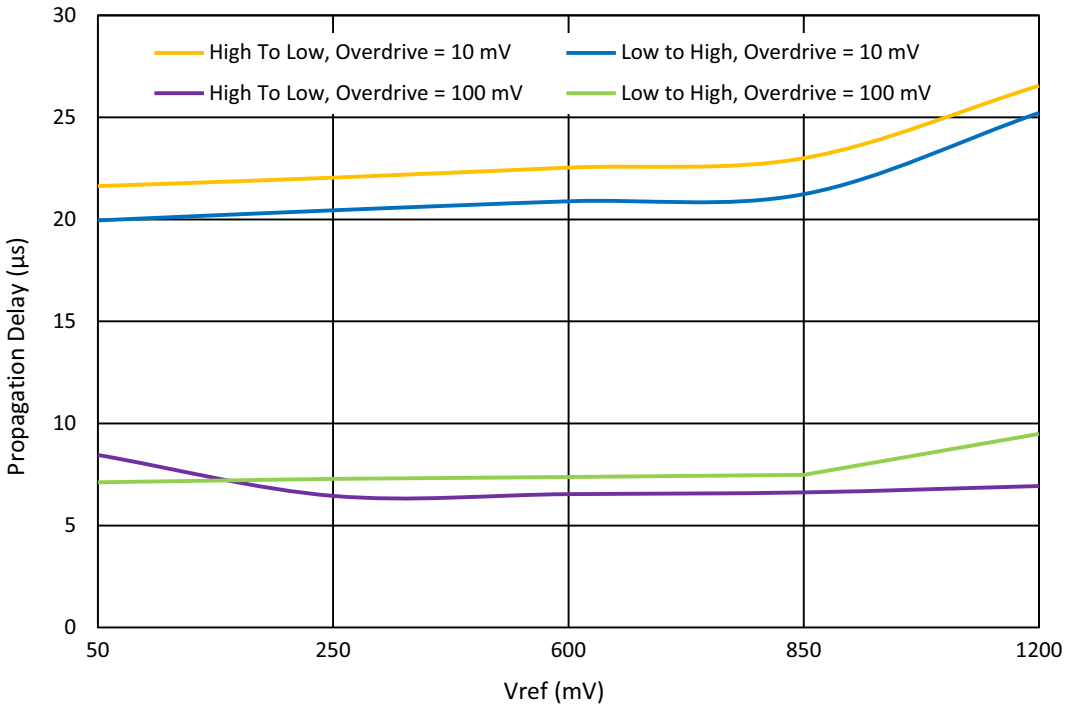


Figure 59. ACMPx Typical Propagation Delay at T_A = +25 °C, Gain = 1, Hysteresis = 0, V_{DD} = 1.71 V to 5.5 V, LPF-Enable

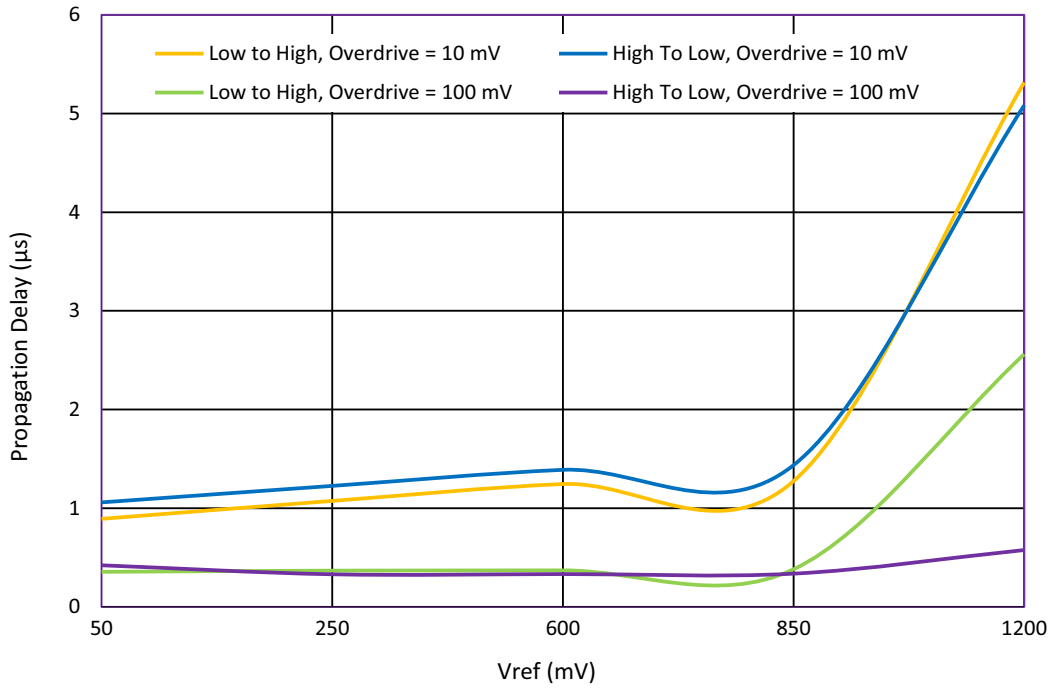


Figure 60. ACMPx Typical Propagation Delay at T_A = +25 °C, Gain = 1, Hysteresis = 0, V_{DD} = 1.71 V to 5.5 V, LPF-Disable

Note: When V_{DD} < 1.8 V voltage reference should not exceed 1100 mV.

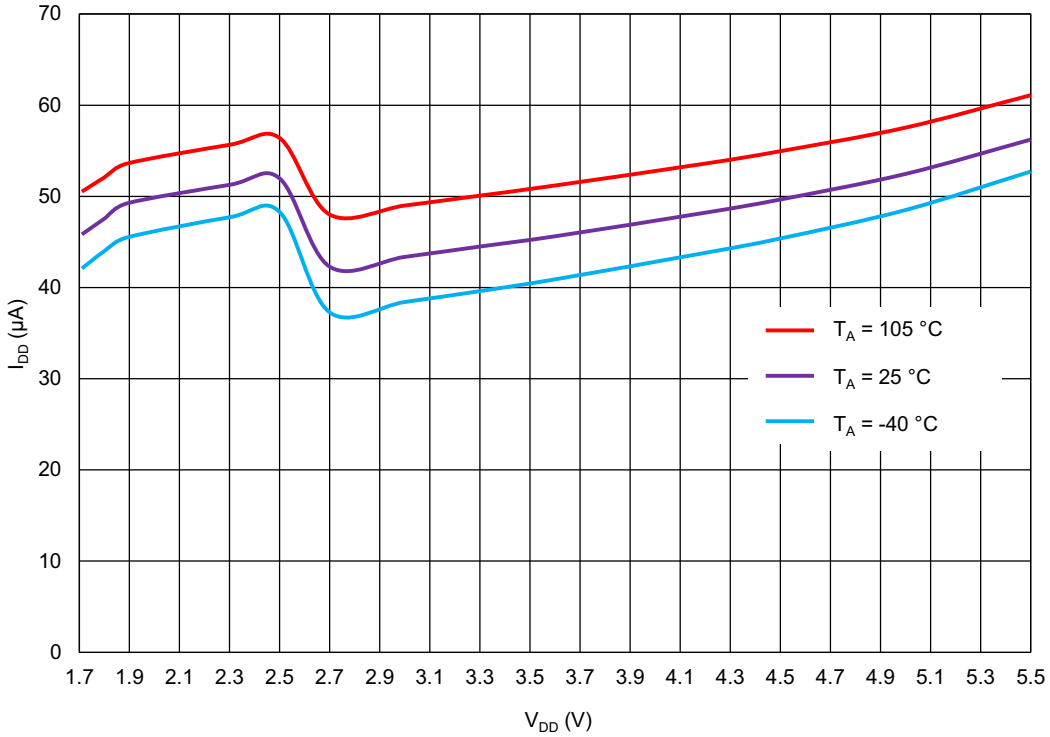


Figure 61. ACMPx Current Consumption vs. V_{DD} at V_{IN+} Connected to V_{DD}, Internal V_{REF} = 50 mV

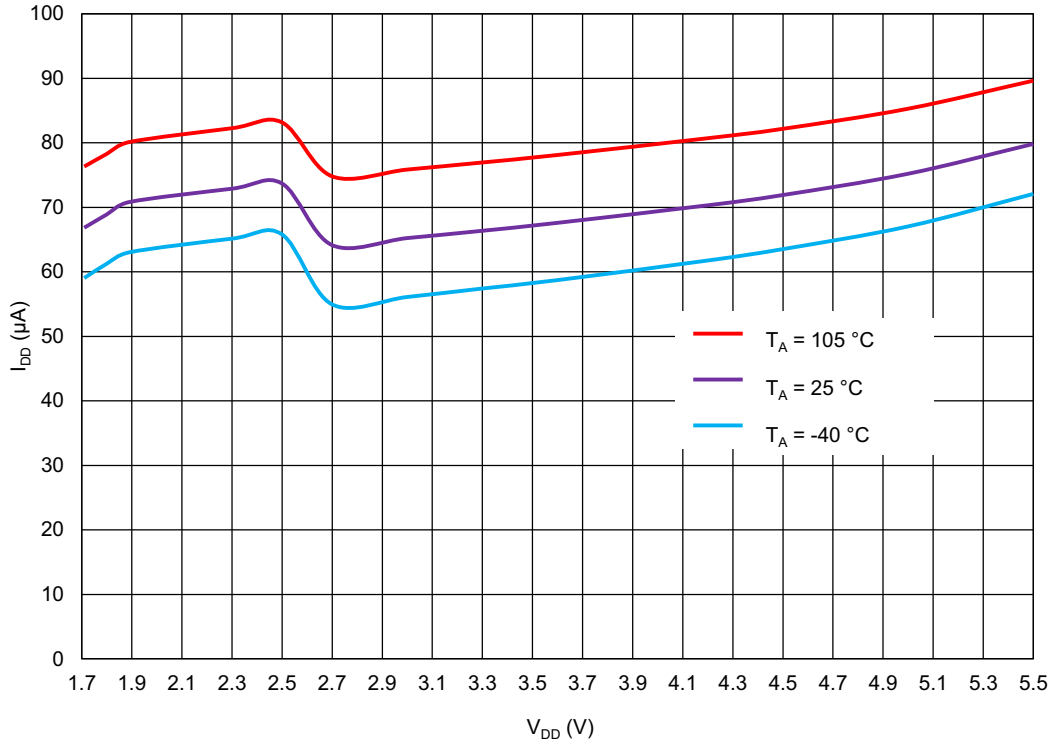


Figure 62. Buffered ACMPx Current Consumption vs. V_{DD} at V_{IN+} Connected to V_{DD}, Internal V_{REF} = 50 mV

9. Pipe Delay

The SLG46535-EV has a pipe delay logic cell that is shared with the 3-bit LUT10 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see section 7.3 3-Bit LUT or Pipe Delay Macrocell for the description of this Combination Function macrocell.

10. Programmable Delay/Edge Detector

The SLG46535-EV has a programmable time delay logic cell available, that can generate a delay, that is selectable from one of four timings configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. See Figure 63 and Figure 64 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

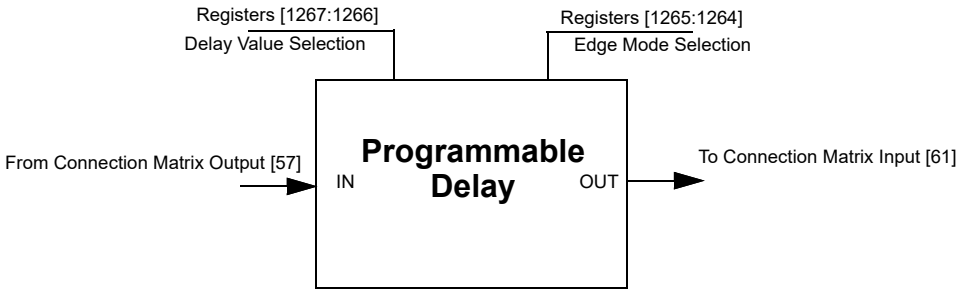


Figure 63. Programmable Delay

10.1 Programmable Delay Timing Diagram - Edge Detector Output

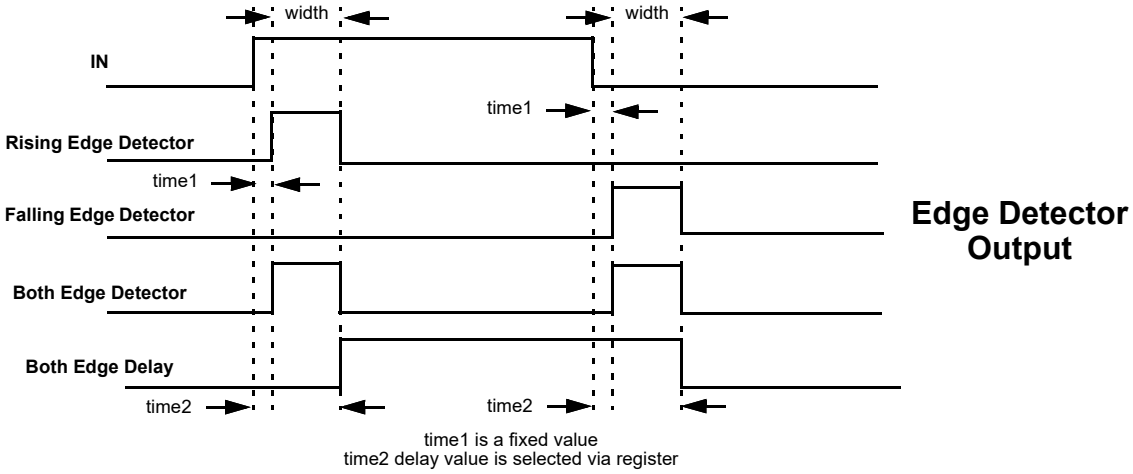


Figure 64. Edge Detector Output

Please refer to section 3.4.6 Programmable Delay Typical Delays and Widths.

11. Additional Logic Function. Deglitch Filter

The SLG46535-EV has three additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions and one inverter, which can switch the polarity of any Connection Matrix signal.

11.1 Deglitch Filter/Edge Detector

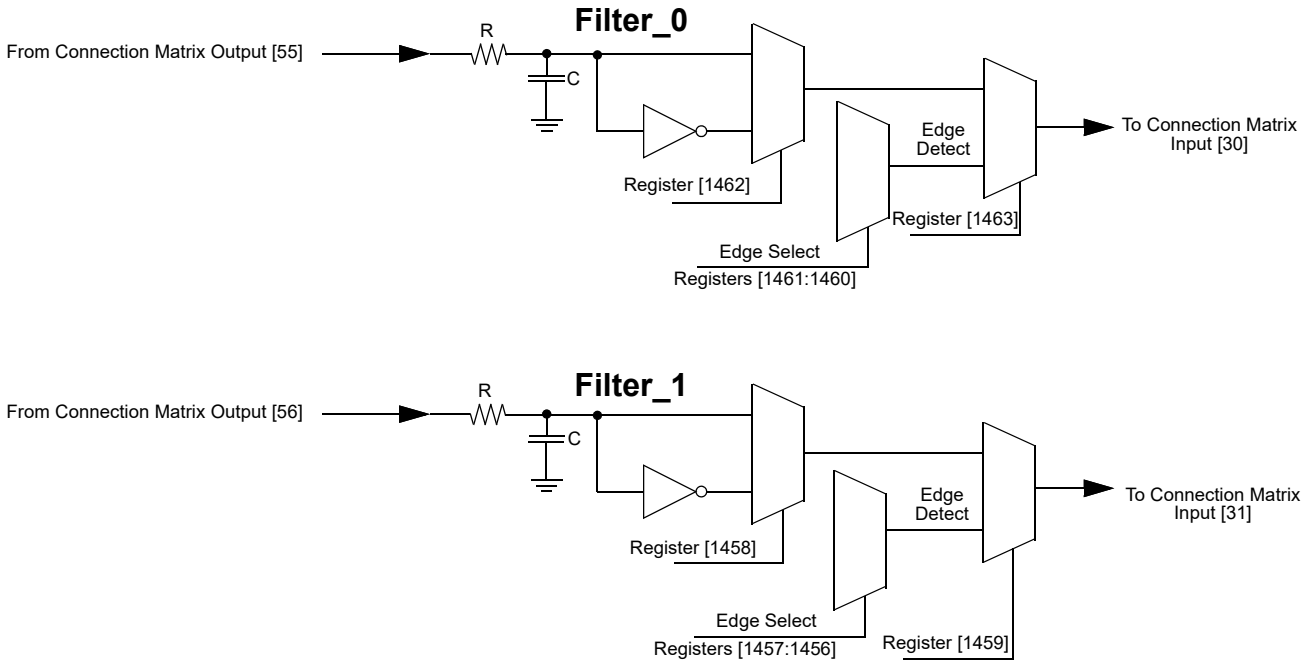


Figure 65. Deglitch Filter/Edge Detector

11.2 INV Gate

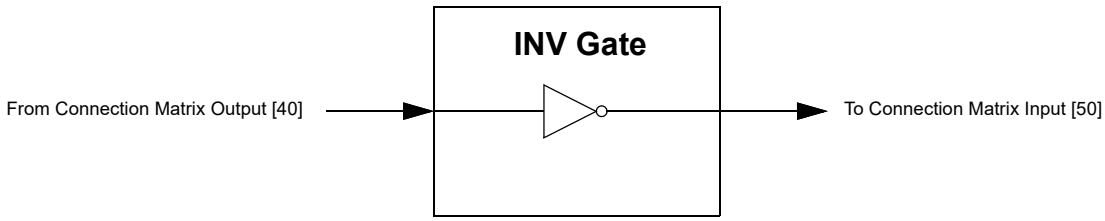


Figure 66. INV Gate

12. Voltage Reference

12.1 Voltage Reference Overview

The SLG46535-EV has a Voltage Reference Macrocell to provide references to the three analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from Pin 5. See Table 34 for the available selections for each analog comparator. Also, see Figure 67, which shows the reference output structure.

12.2 V_{REF} Selection Table

Table 34. V_{REF} Selection Table

SEL[4:0]	ACMP0_V_{REF}	ACMP1_V_{REF}	ACMP2_V_{REF}
11101	PIN 5: EXT_V_{REF}/2	Reserved	Reserved
11100	PIN 10: EXT_V_{REF}/2	PIN 10: EXT_V_{REF}/2	PIN 10: EXT_V_{REF}/2
11011	PIN 5: EXT_V_{REF}	Reserved	Reserved
11010	PIN 10: EXT_V_{REF}	PIN 10: EXT_V_{REF}	PIN 10: EXT_V_{REF}
11001	V_{DD}/4	V_{DD}/4	V_{DD}/4
11000	V_{DD}/3	V_{DD}/3	V_{DD}/3
10111	1.20	1.20	1.20
10110	1.15	1.15	1.15
10101	1.10	1.10	1.10
10100	1.05	1.05	1.05
10011	1.00	1.00	1.00
10010	0.95	0.95	0.95
10001	0.90	0.90	0.90
10000	0.85	0.85	0.85
01111	0.80	0.80	0.80
01110	0.75	0.75	0.75
01101	0.70	0.70	0.70
01100	0.65	0.65	0.65
01011	0.60	0.60	0.60
01010	0.55	0.55	0.55
01001	0.50	0.50	0.50
01000	0.45	0.45	0.45
00111	0.40	0.40	0.40
00110	0.35	0.35	0.35
00101	0.30	0.30	0.30
00100	0.25	0.25	0.25
00011	0.20	0.20	0.20
00010	0.15	0.15	0.15

Table 34. V_{REF} Selection Table (Cont.)

SEL[4:0]	ACMP0_V_{REF}	ACMP1_V_{REF}	ACMP2_V_{REF}
00001	0.10	0.10	0.10
00000	0.05	0.05	0.05

Table 35. Practical V_{REF} Range of Voltage Reference Macrocell

V_{DD}	Practical V_{REF} Range	Note
2.0 V - 5.5 V	50 mV ~ 1.2 V	
1.7 V - 2.0 V	50 mV ~ 1.0 V	Do not operate above 1.0 V

12.3 V_{REF} Block Diagram

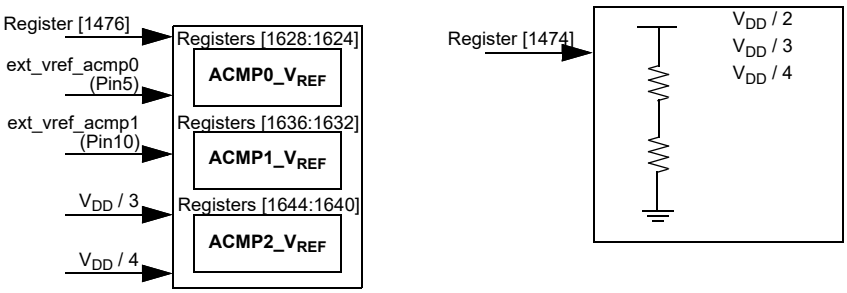


Figure 67. Voltage Reference Block Diagram

12.4 V_{REF} Load Regulation

Note 1: V_{REF} buffer performance is not guaranteed at V_{DD} < 2.7 V.

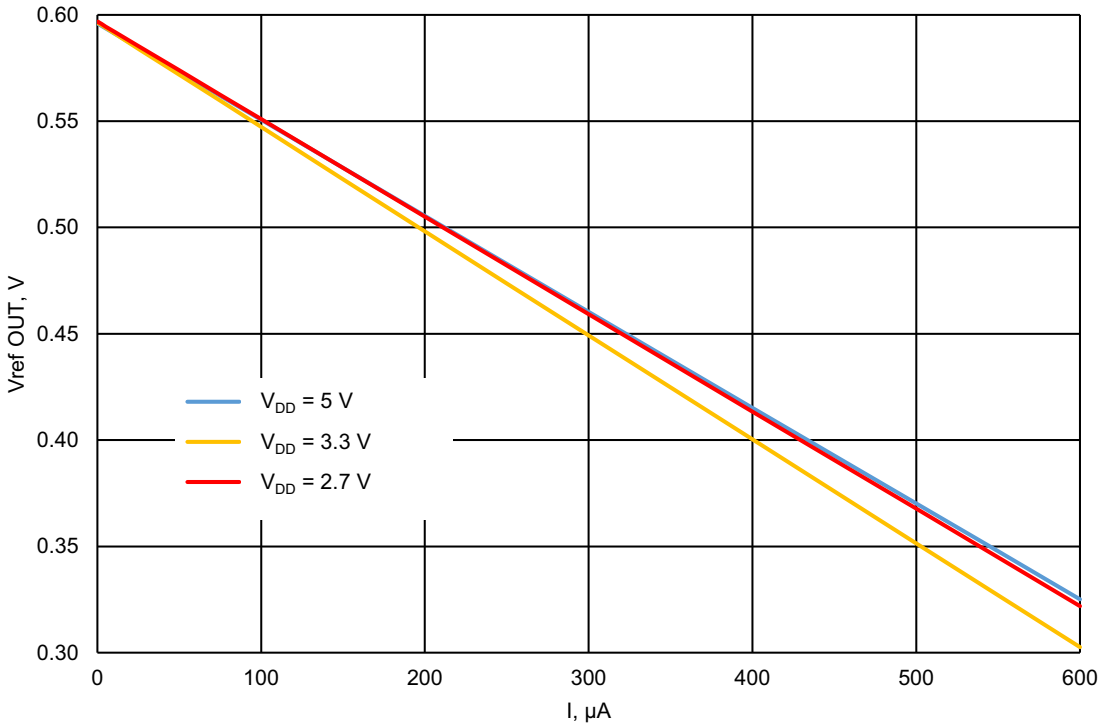


Figure 68. Typical Load Regulation, V_{REF} = 600 mV, T_A = -40 °C to +105 °C, Buffer - Enable

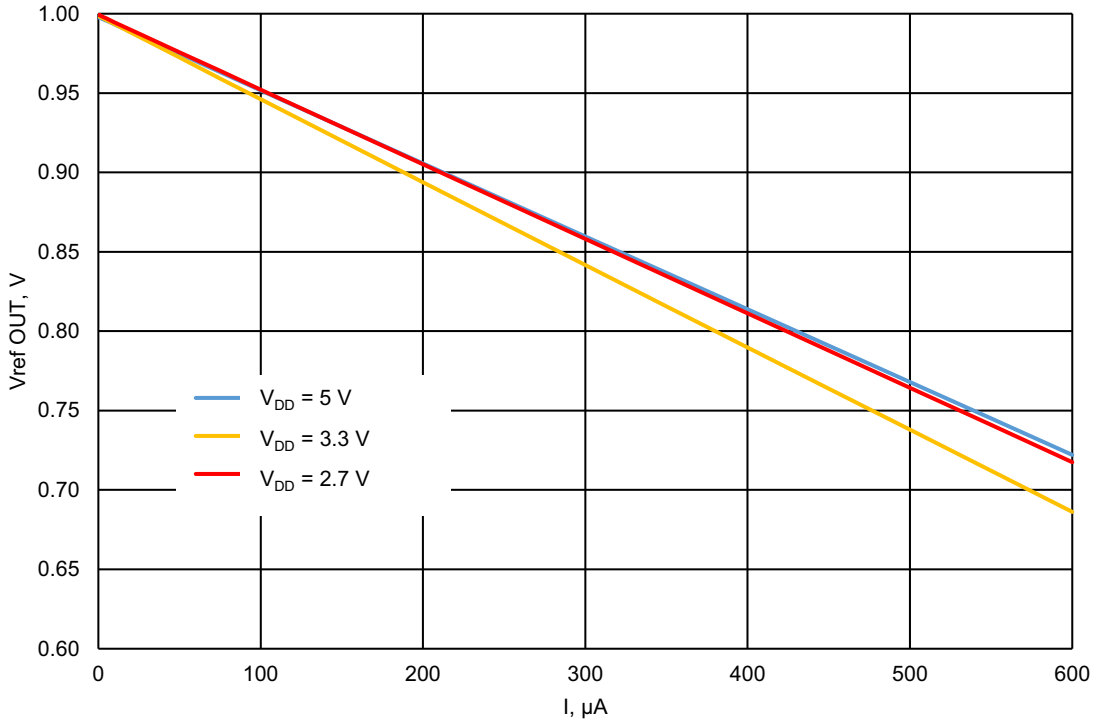


Figure 69. Typical Load Regulation, V_{REF} = 1000 mV, T_A = -40 °C to +105 °C, Buffer - Enable

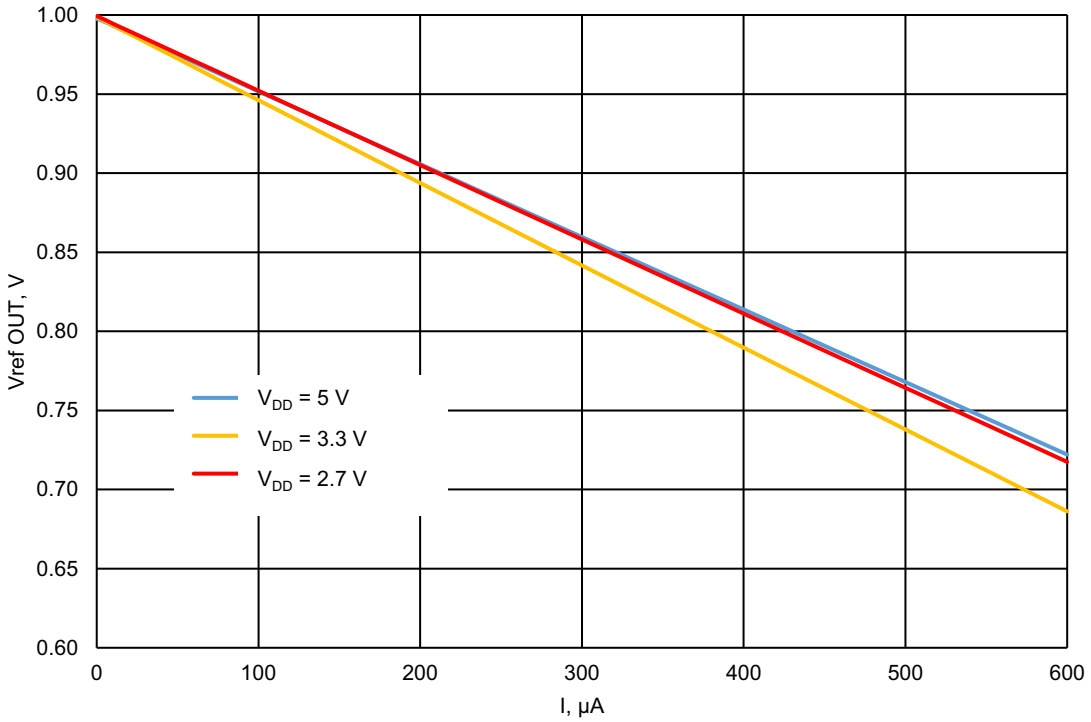


Figure 70. Typical Load Regulation, V_{REF} = 1200 mV, T_A = -40 °C to +105 °C, Buffer - Enable

13. Clocking

13.1 OSC General Description

The SLG46535-EV has two internal oscillators. Oscillator OSC 0 that runs at 25 kHz/2 MHz and Oscillator OSC1 that runs at 25 MHz. It is possible to use OSC0 and OSC1 simultaneously. The fundamental frequency can also come from clock input (Pin 14 for 25 kHz/2 MHz and Pin 13 for 25 MHz), see section 13.3 External Clocking.

13.2 25 kHz/2 MHz and 25 MHz Oscillators

There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The pre-divider allows the selection of /1, /2, /4, or /8 divide down frequency from the fundamental. The second stage divider (only for 25 kHz/2 MHz Oscillator) has an input of frequency from the pre-divider, and outputs one of seven different frequencies on Connection Matrix Input lines [27] (OUT0) and [28] (OUT1). See Figure 71 and Figure 72 for details.

There are two modes of the POWER CONTROL pin, (register [1658] for 25 kHz/2 MHz OSC and register [1657] for 25 MHz OSC):

- **POWER-DOWN [0]**. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned on. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned off and OSC divider will reset.
- **FORCE ON [1]**. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned on. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned off.

The PWR CONTROL signal has the highest priority.

The SLG46535-EV has a 25 kHz/2 MHz OSC FAST START-UP function register [1338] (1 – on, 0 – off). It allows the OSC to run immediately after power-up. Start-up time is less than one cycle. Note that when OSC FAST START-UP is on, the current consumption will rise.

The user can select two OSC POWER MODEs (register [1343] for 25 kHz/2 MHz OSC and register [1341] for 25 MHz OSC):

- If **AUTO POWER-ON [0]** is selected, the OSC will run when any macrocell that uses OSC is powered on.
- If **FORCE POWER-ON [1]** is selected, the OSC will run when the SLG46535-EV is powered on.

OSC can be turned on by:

- Register control (force Power-On)
- Delay mode, when delay requires OSC
- CNT/FSM.

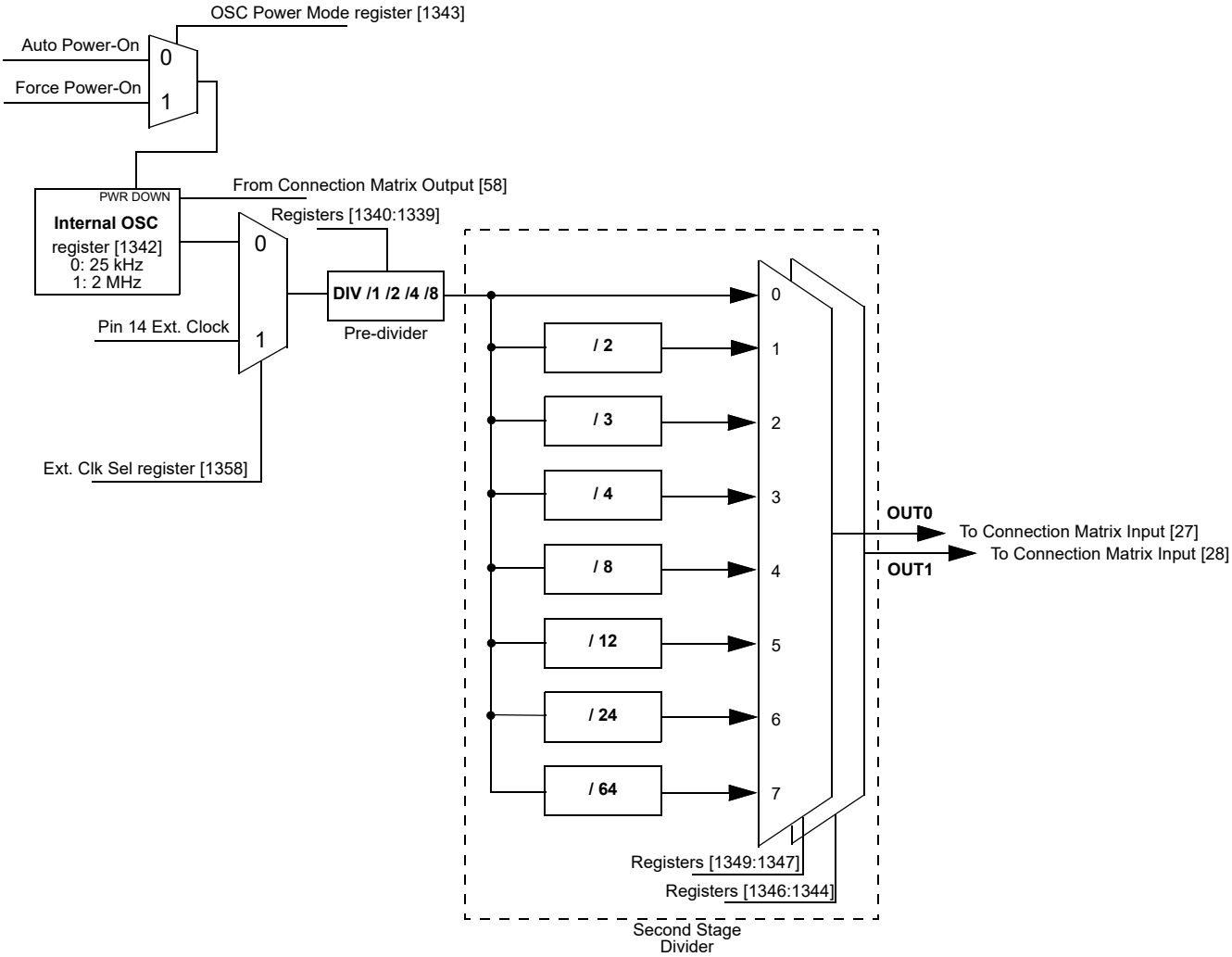


Figure 71. 25 kHz/2 MHz OSC0 Block Diagram

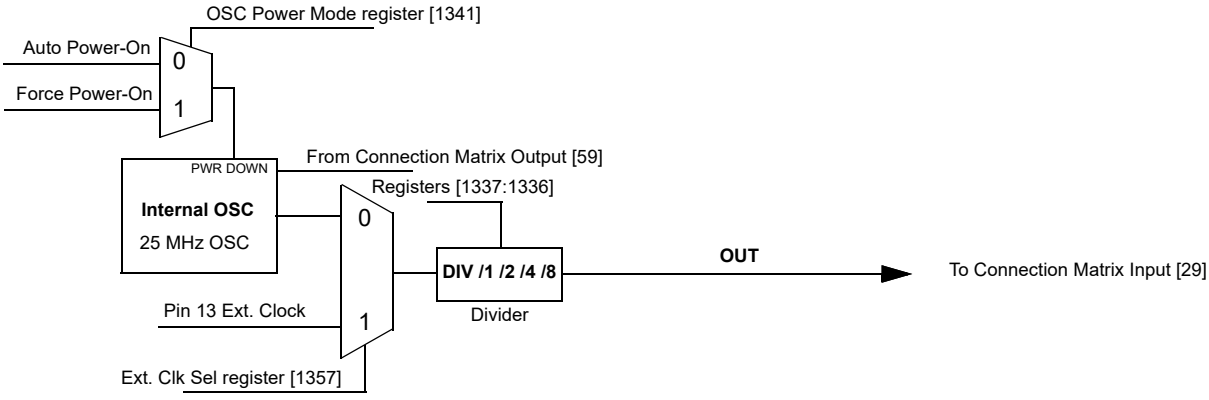


Figure 72. 25 MHz OSC1 Block Diagram

13.3 External Clocking

The SLG46535-EV supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.3.1 Pin 20 or Pin 18 Source for 25 kHz/2 MHz Clock

When register [1358] is set to 1, an external clocking signal on Pin 14 will be routed in place of the internal oscillator derived 25 kHz/2 MHz clock source. See Figure 71. The high and low limits for external frequency that can be selected are 0 MHz and 77 MHz.

13.3.2 Pin 17 Source for 25 MHz Clock

When register [1357] is set to 1, an external clocking signal on Pin 13 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 72. The high and low limits for external frequency that can be selected are 0 MHz and 84 MHz.

13.4 Oscillators Power-On Delay

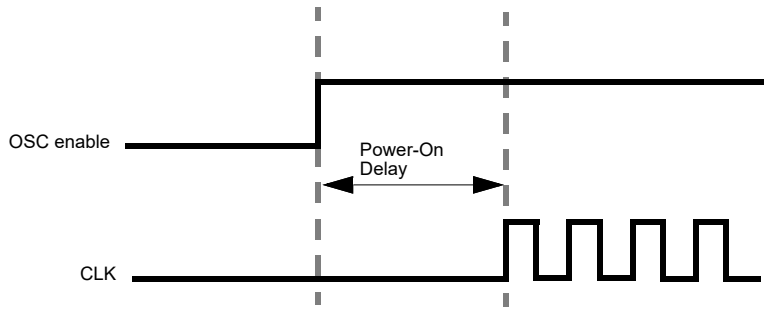


Figure 73. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.

Note 2: “OSC enable” signal appears when any macrocell that uses OSC is powered on.

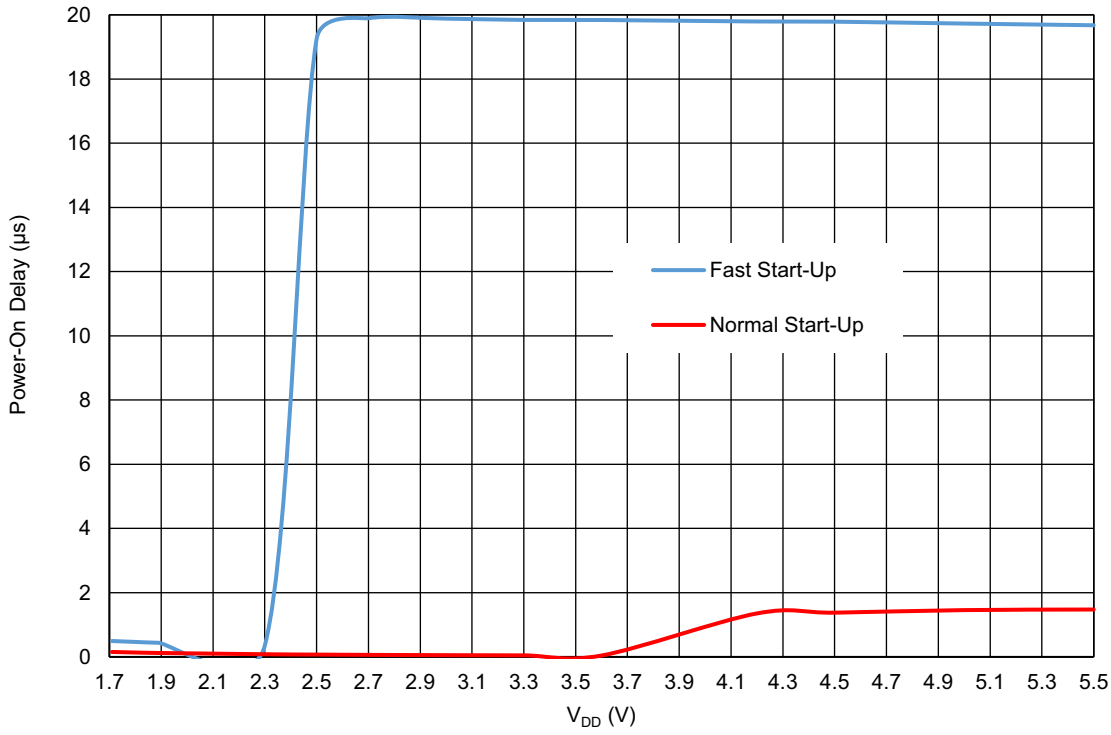


Figure 74. Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = +25 °C, OSC0 = 25 kHz

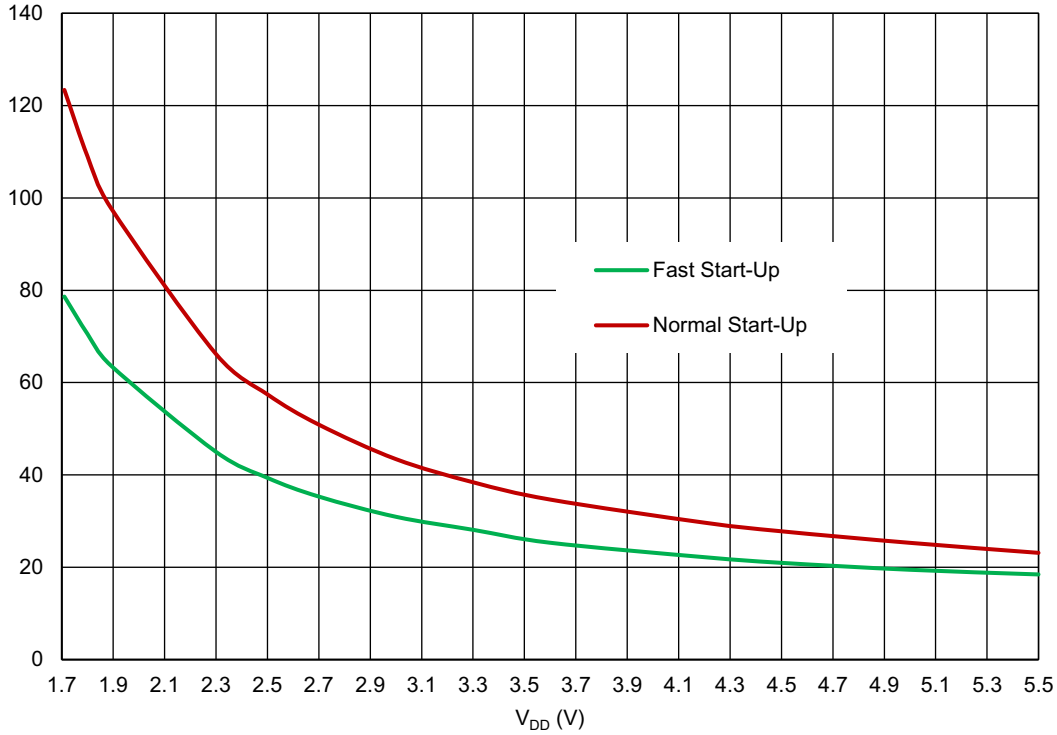


Figure 75. Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = +25 °C, OSC0 = 2 MHz

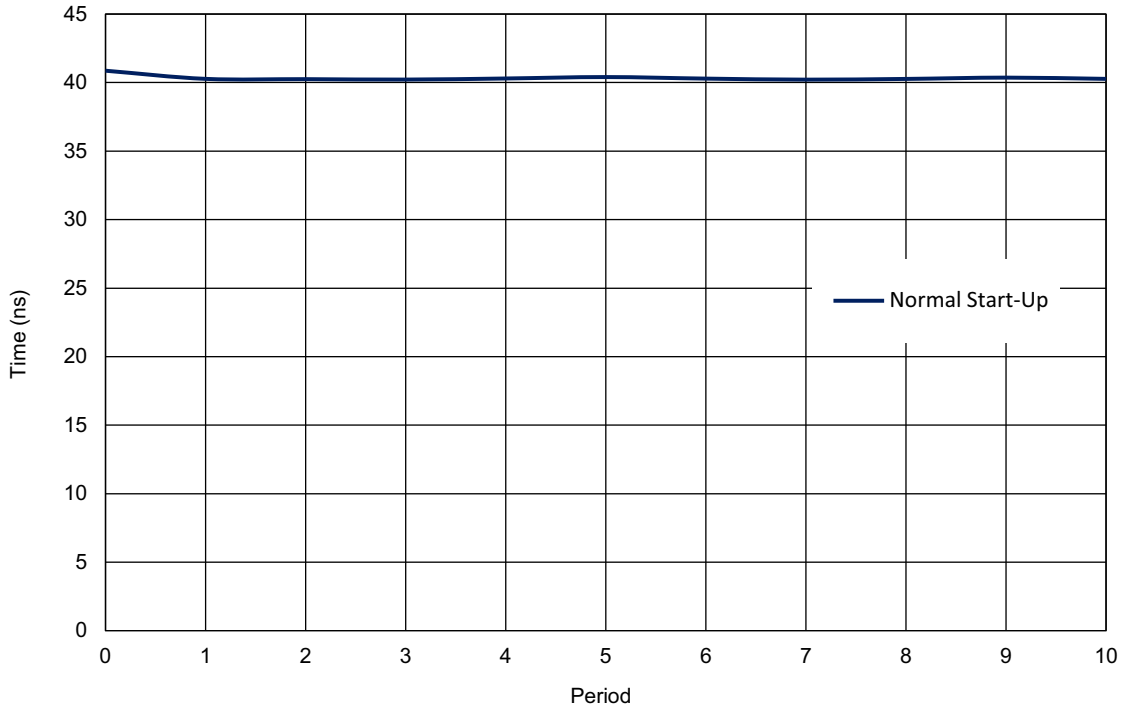


Figure 76. Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = +25 °C, OSC1 = 25 MHz

13.5 Oscillators Accuracy

Note 1: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

Note 2: For more information see sections 3.4.9 25 kHz OSC0 Frequency Limits, 3.4.11 2 MHz OSC0 Frequency Limits, 3.4.13 25 MHz OSC1 Frequency Limits.

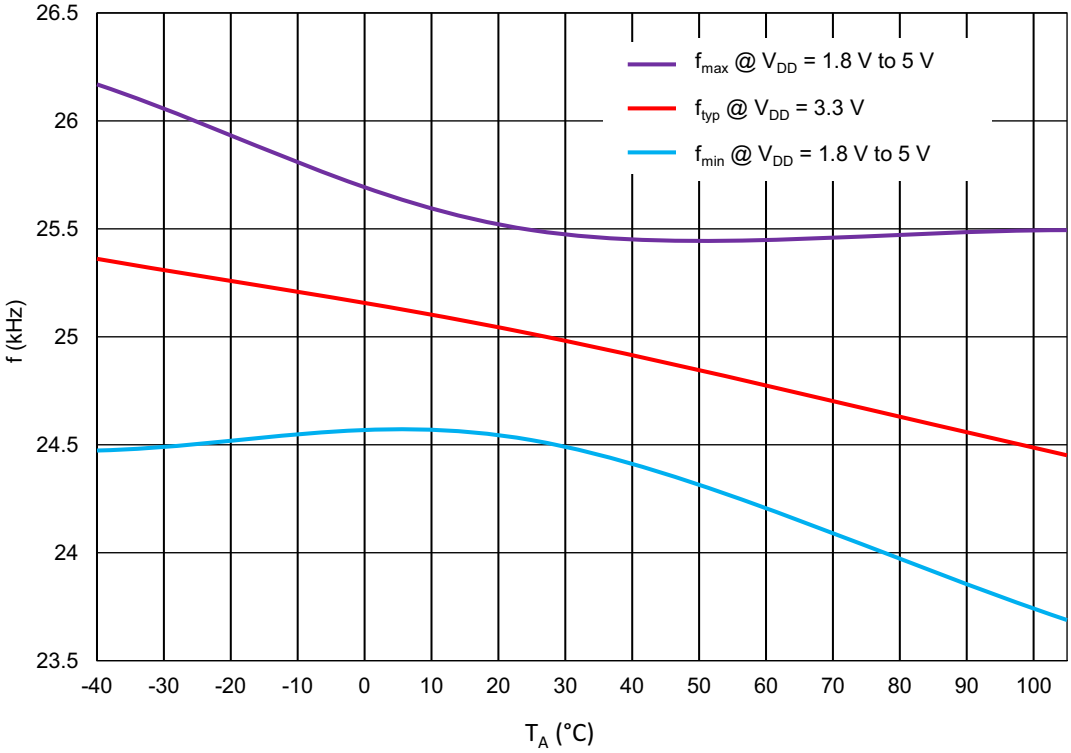


Figure 77. Oscillator Frequency vs. Ambient Temperature, OSC0 = 25 kHz

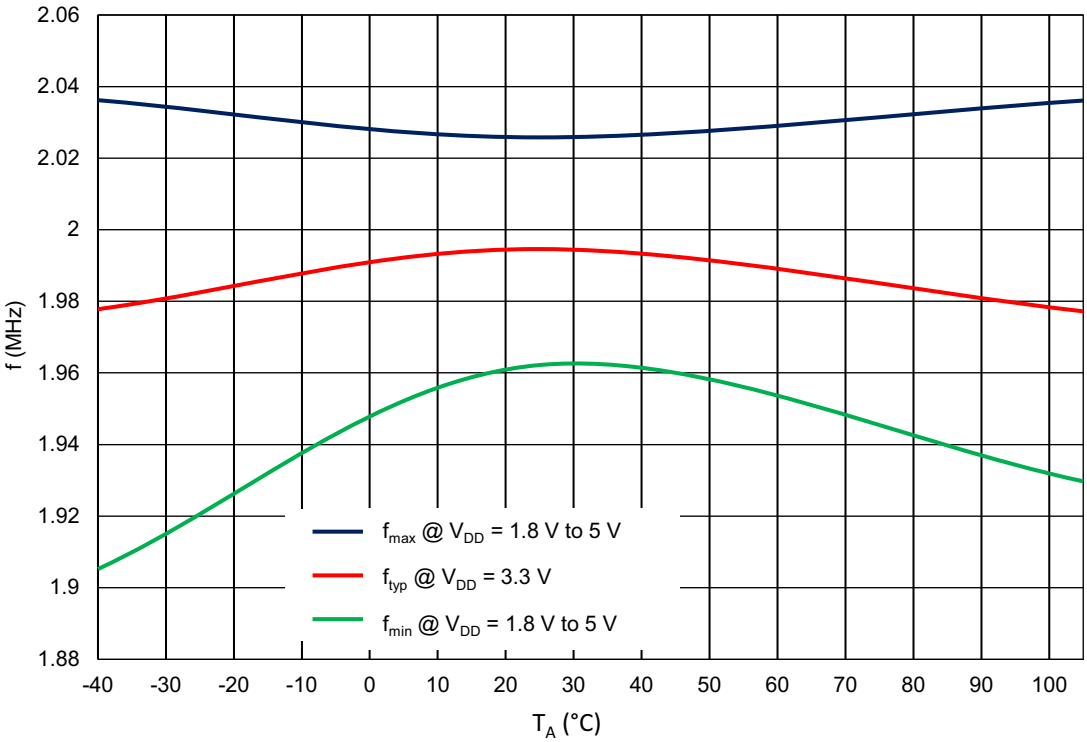


Figure 78. Oscillator Frequency vs. Ambient Temperature, OSC0 = 2 MHz

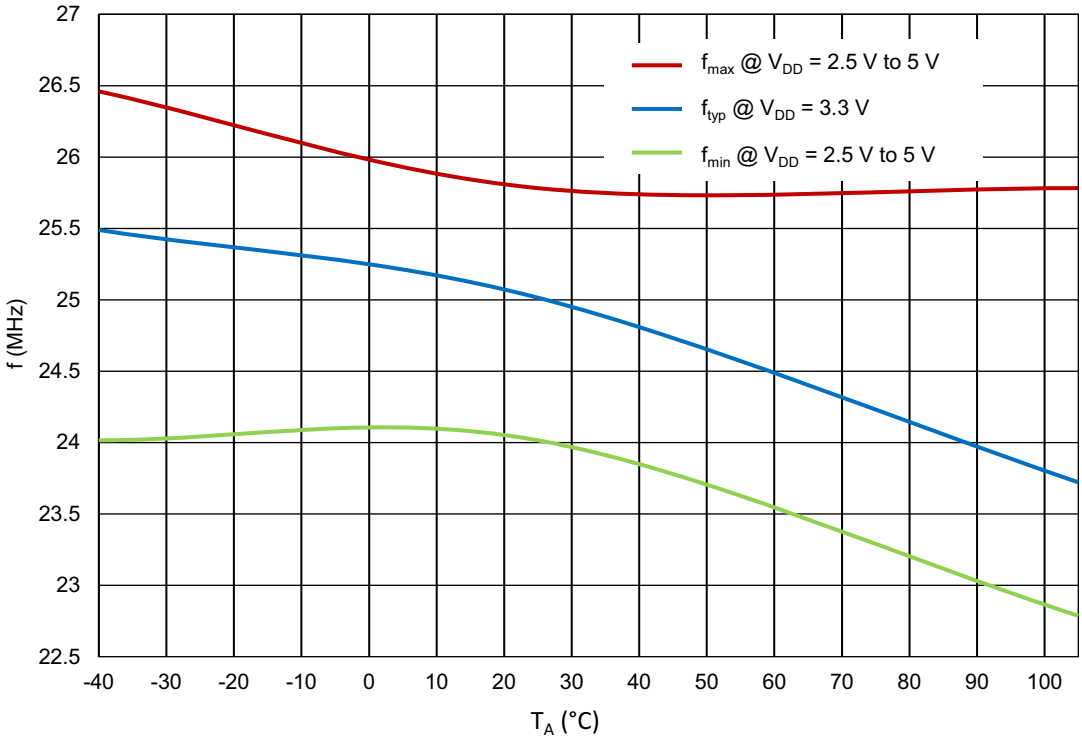


Figure 79. Oscillator Frequency vs. Ambient Temperature, OSC1 = 25 MHz

Note: 25 MHz OSC1 performance is not guaranteed at V_{DD} < 2.5 V.

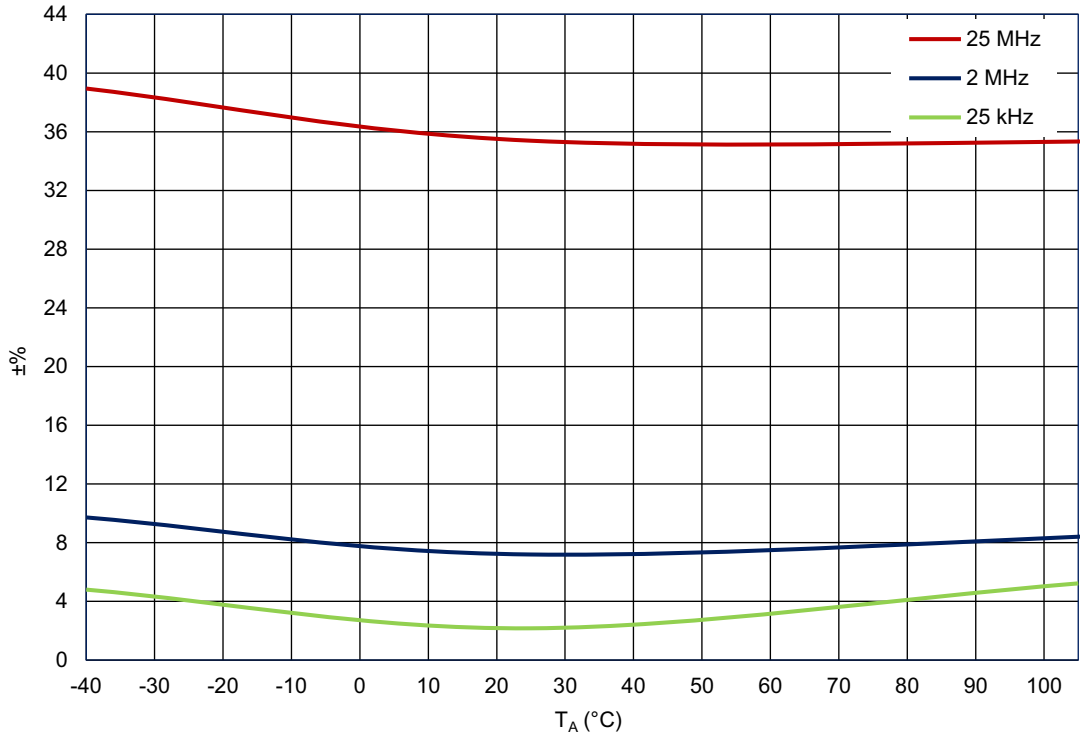


Figure 80. Oscillators Total Error vs. Ambient Temperature

13.6 Oscillators Settling Time

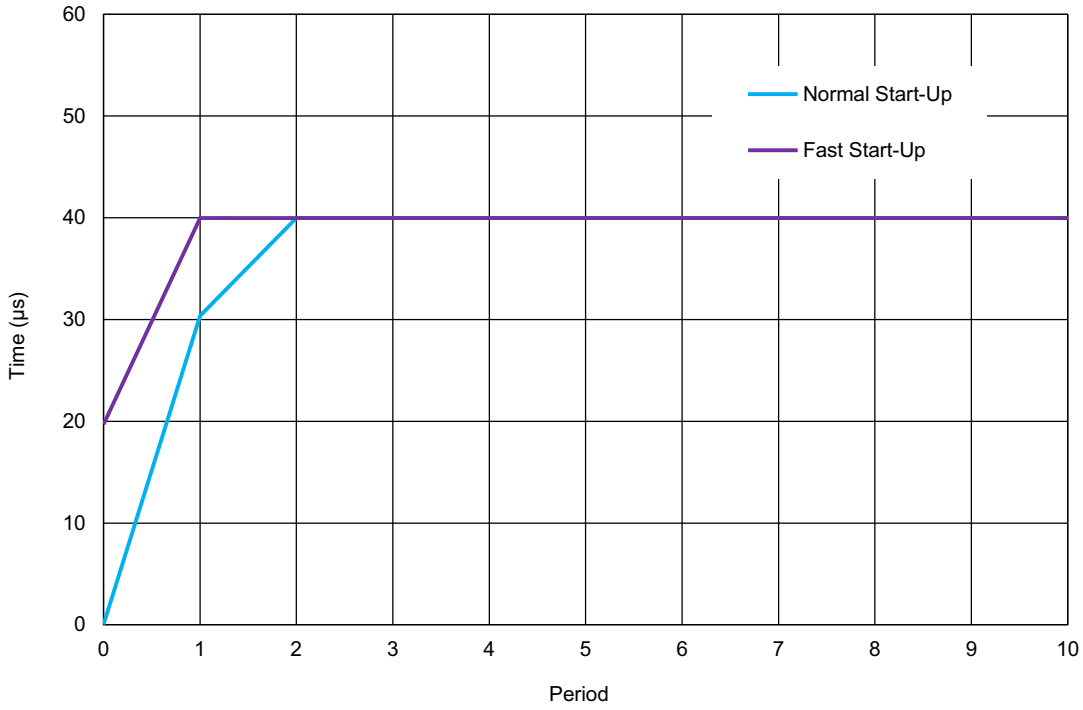


Figure 81. Oscillator0 Settling Time, V_{DD} = 3.3 V, T_A = +25 °C, OSC0 = 2 kHz

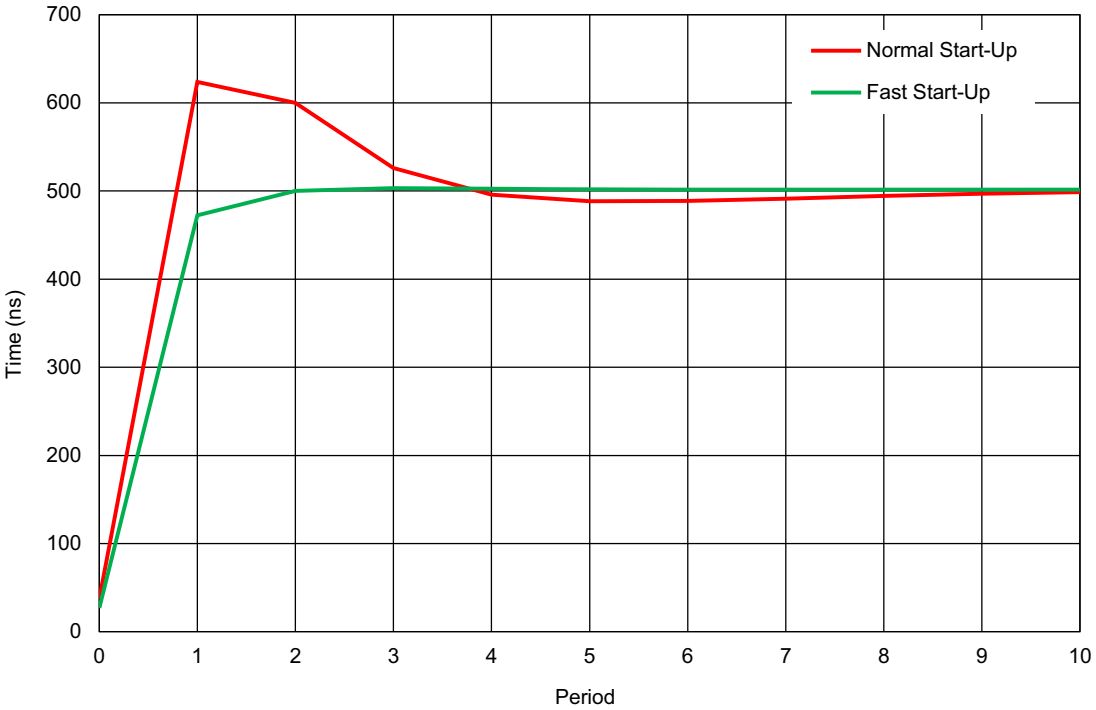


Figure 82. Oscillator0 Settling Time, V_{DD} = 3.3 V, T_A = +25 °C, OSC0 = 2 MHz

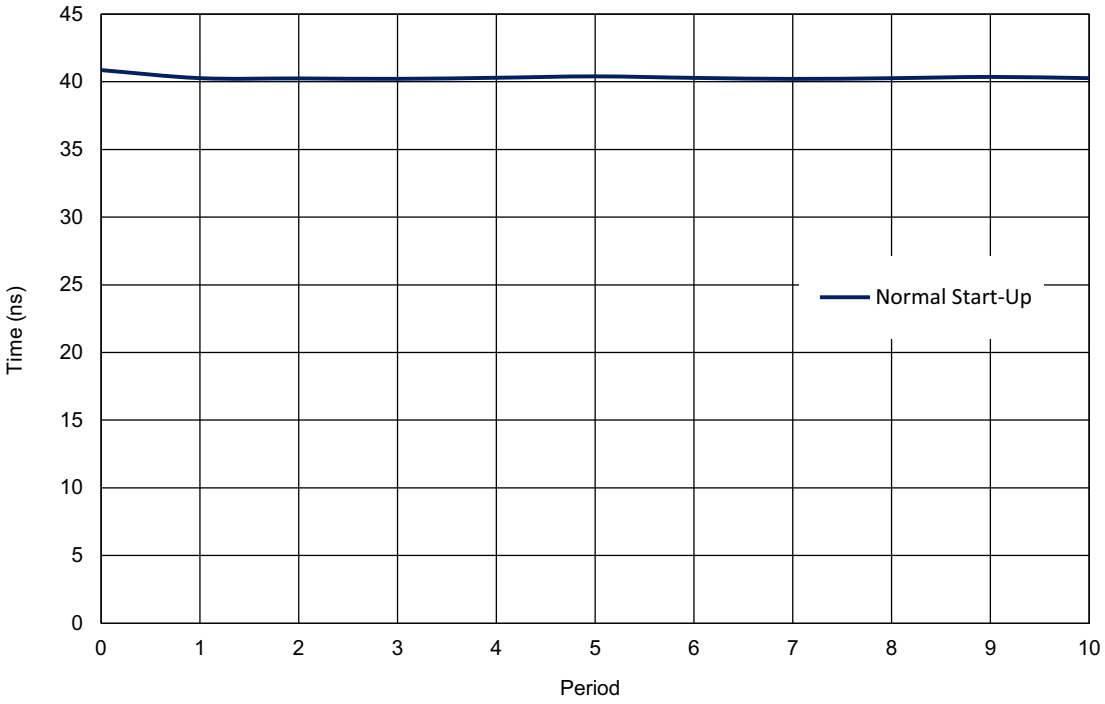


Figure 83. Oscillator1 Settling Time, V_{DD} = 3.3 V, T_A = +25 °C, OSC2 = 25 MHz

13.7 Oscillators Current Consumption

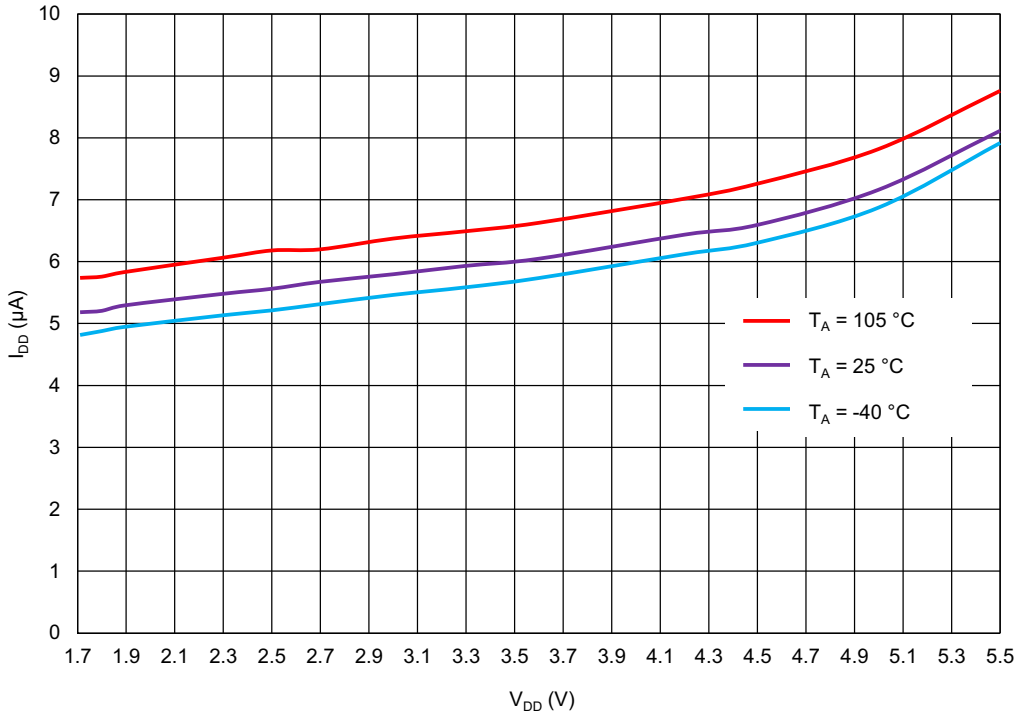


Figure 84. OSC0 (25 kHz) Current Consumption vs. V_{DD}, All Pre-Dividers

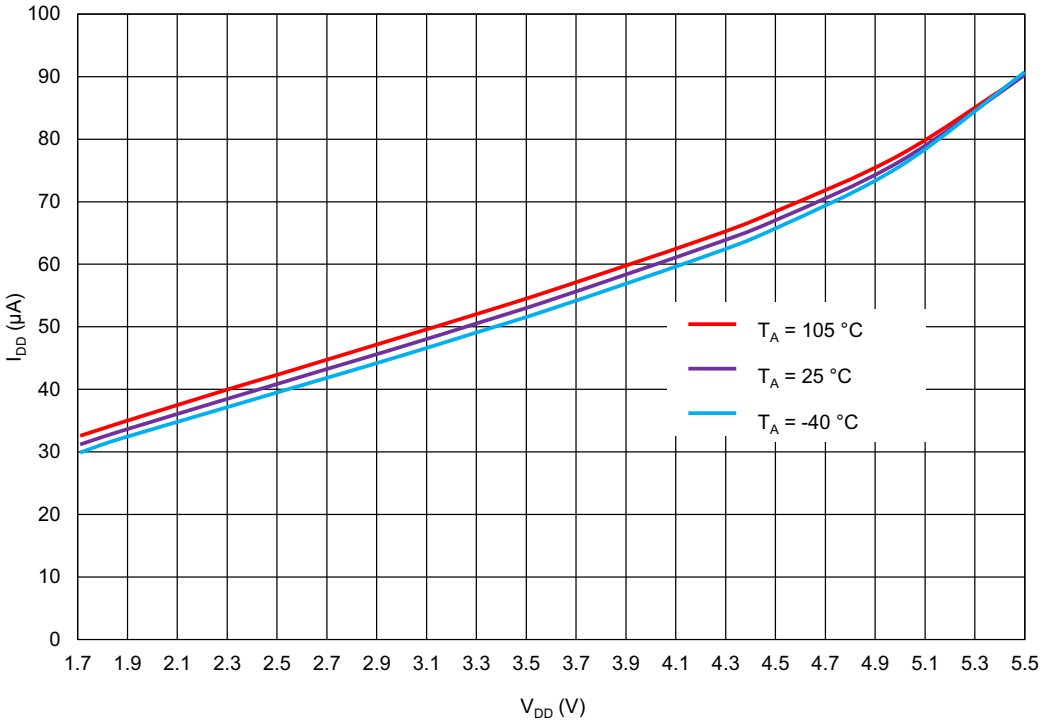


Figure 85. OSC0 (2 MHz) Current Consumption vs. V_{DD}, Pre-Divider = 1

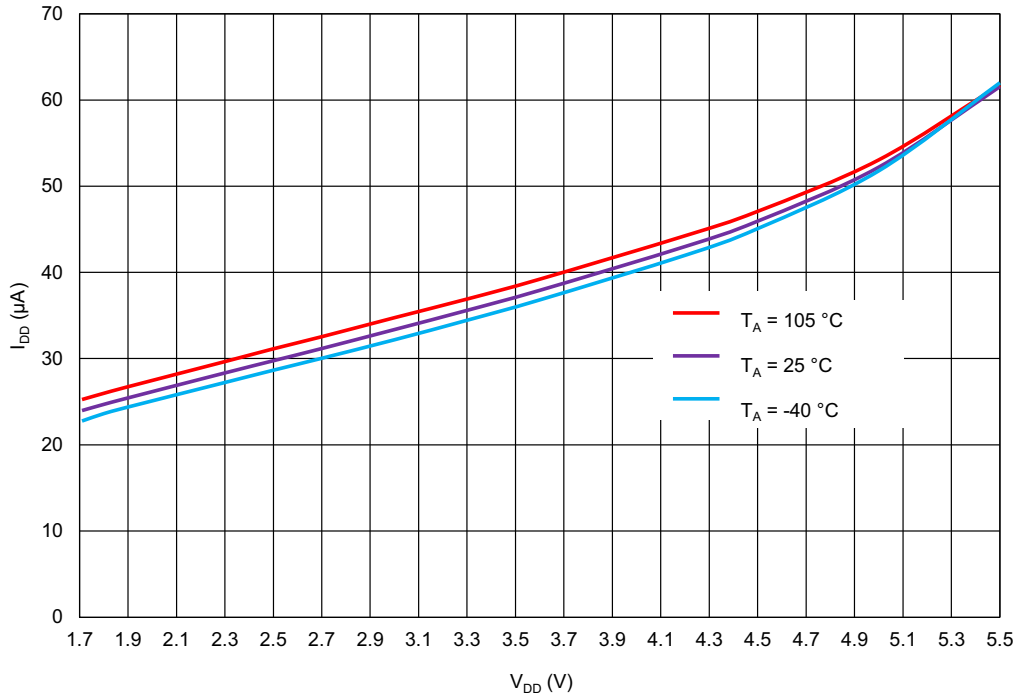


Figure 86. OSC0 (2 MHz) Current Consumption vs. $V_{DD,}$ Pre-Divider = 2

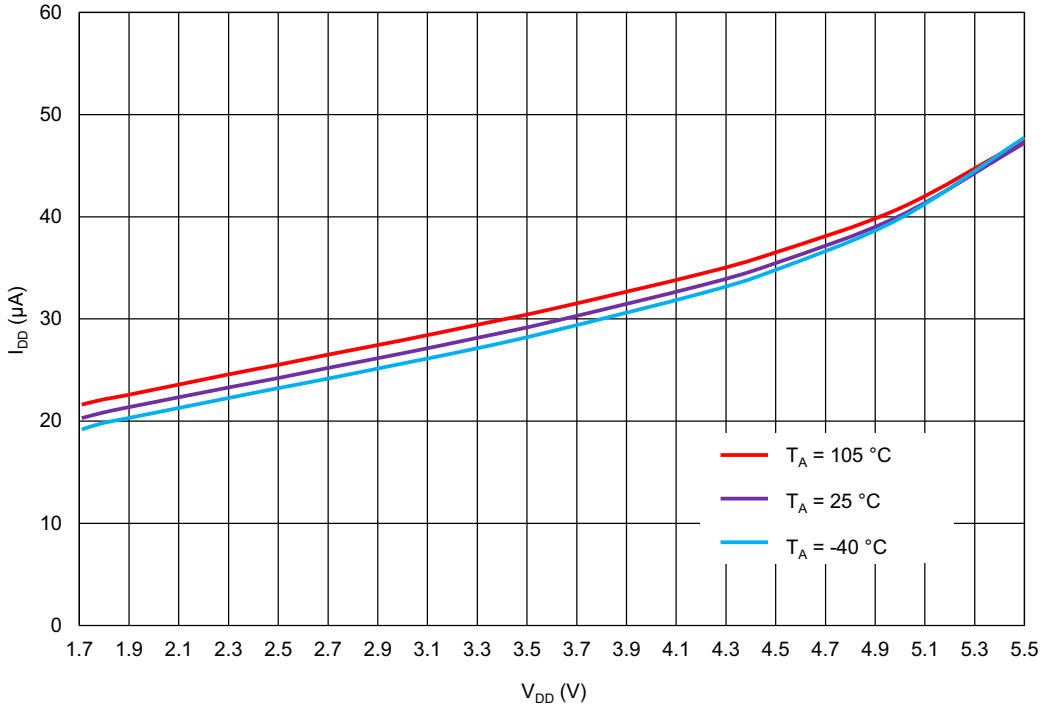


Figure 87. OSC0 (2 MHz) Current Consumption vs. $V_{DD,}$ Pre-Divider = 4

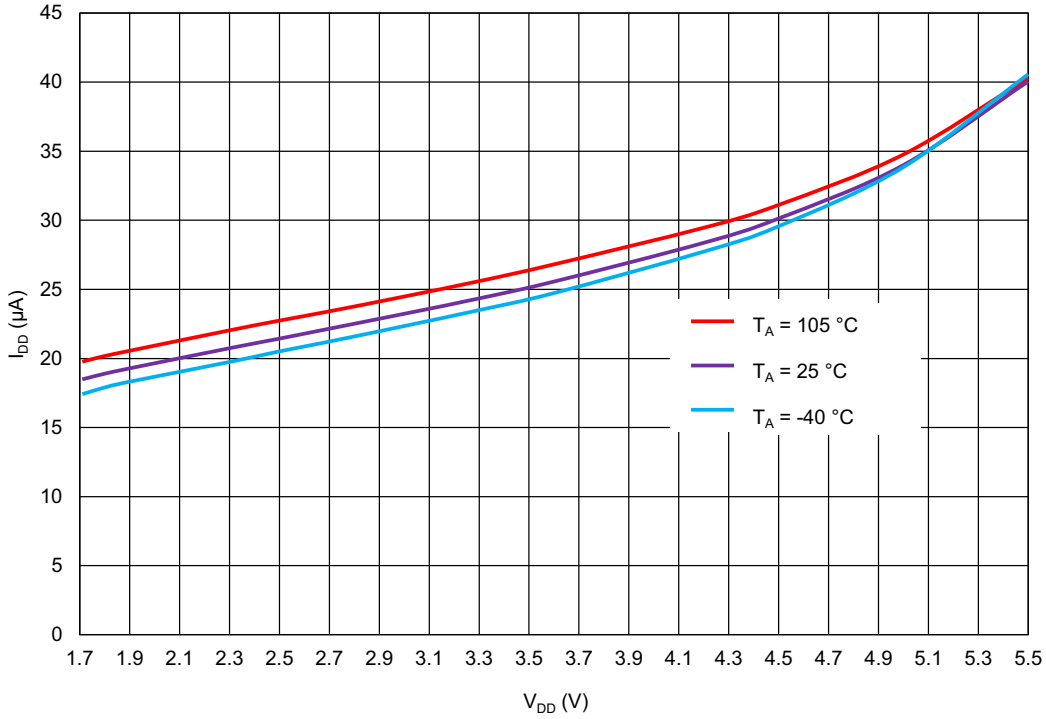


Figure 88. OSC0 (2 MHz) Current Consumption vs. $V_{DD,}$ Pre-Divider = 8

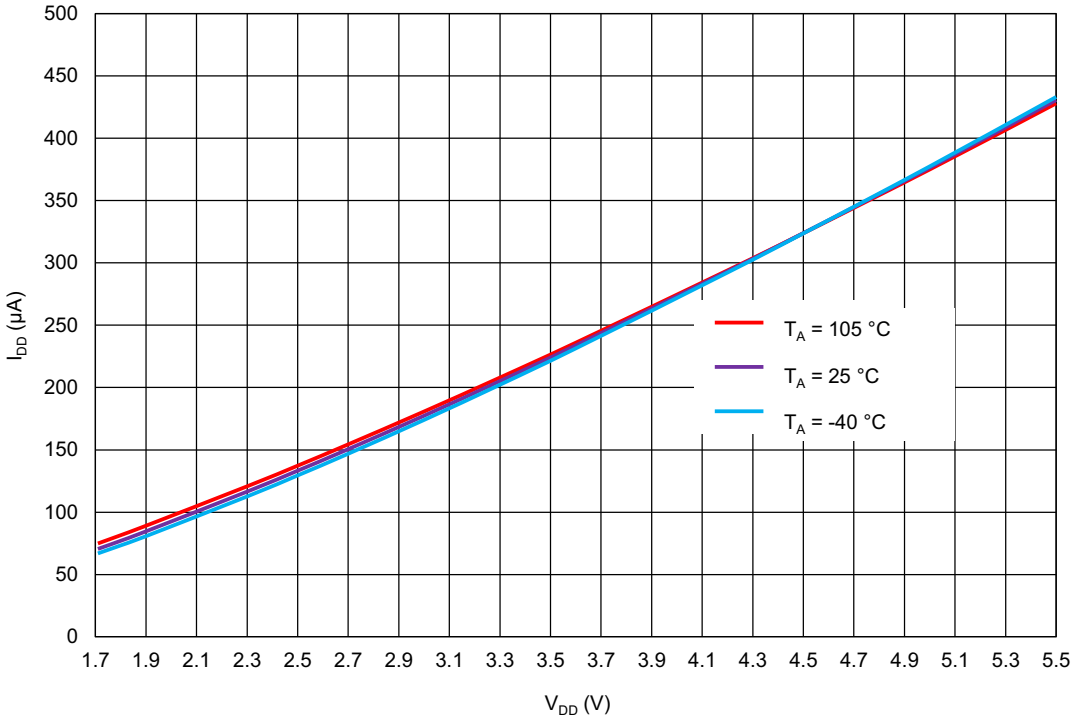


Figure 89. OSC1 (25 MHz) Current Consumption vs. $V_{DD,}$ Pre-Divider = 1

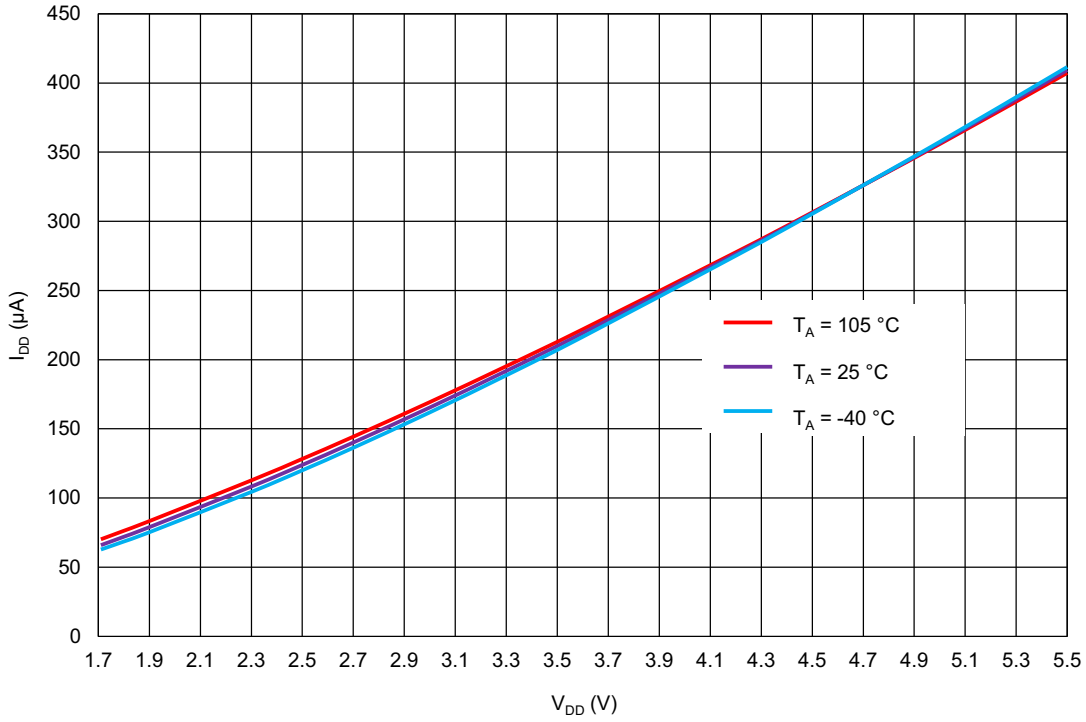


Figure 90. OSC1 (25 MHz) Current Consumption vs. V_{DD}, Pre-Divider = 2

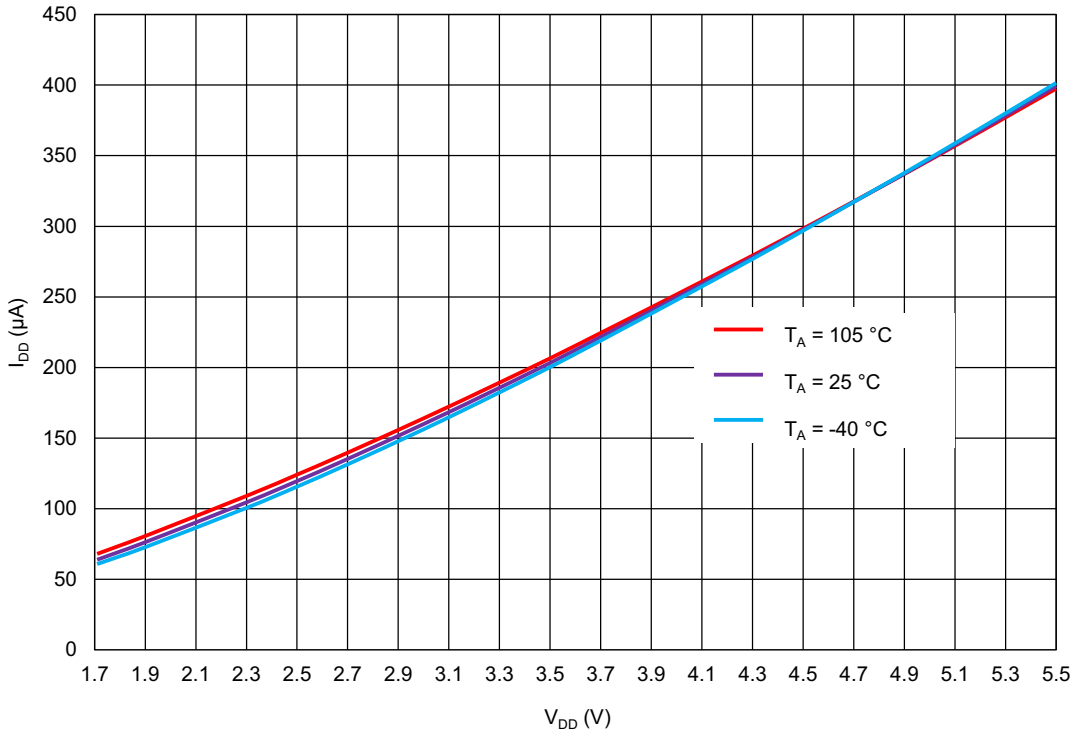


Figure 91. OSC1 (25 MHz) Current Consumption vs. V_{DD}, Pre-Divider = 4

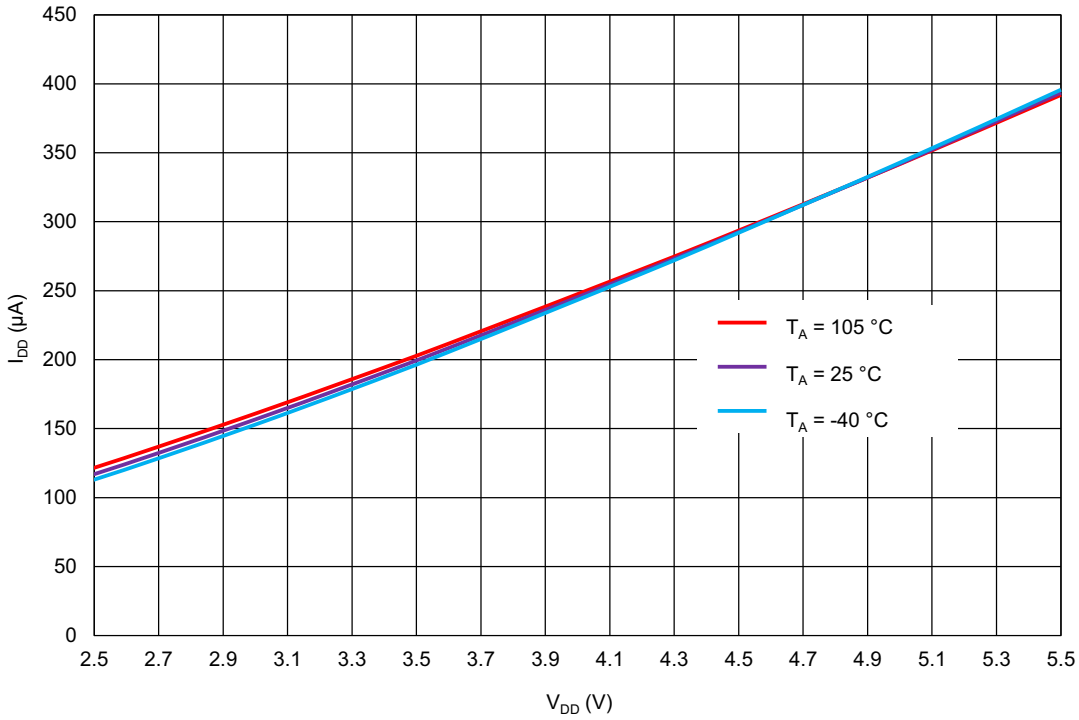


Figure 92. OSC1 (25 MHz) Current Consumption vs. V_{DD}, Pre-Divider = 8

14. Power-On Reset

The SLG46535-EV has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

14.1 General Operation

To start the POR sequence in the SLG46535-EV, the voltage applied on the V_{DD} should be higher than the Power-On Threshold **(Note 1)**. The full operational V_{DD} range for the SLG46535-EV is 1.71 V to 5.5 V (1.8 V ±5 % to 5.0 V ±10 %). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On Threshold. After the POR sequence has started, the SLG46535-EV will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

The SLG46535-EV is guaranteed to be powered down and nonoperational when the V_{DD} voltage (voltage on V_{DD}) is less than Power-Off Threshold (see section 3.4.1 Logic IO Specifications), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher than the V_{DD} voltage is applied to any other PIN **(Note 2)**. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1: The Power-On threshold is defined in section 3.4.1 Logic IO Specifications.

Note 2: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To power down the chip, the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on PINs cannot be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

Note that V_{DD2} has no influence on POR sequence, all internal macrocells are powered from V_{DD}. It means, V_{DD2} can be switched on/off while V_{DD} is on. If voltage on V_{DD2} appears after the POR sequence, pins 10, 12, 13, 14, become available when V_{DD2} reaches 0.6 V.

For proper power up sequence, make sure V_{DD2} will not exceed V_{DD} at any point during startup.

For normal operation V_{DD} should not be switched off while V_{DD2} is on, due to $V_{DD2} \leq V_{DD}$, see section 3. Specifications.

14.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 93.

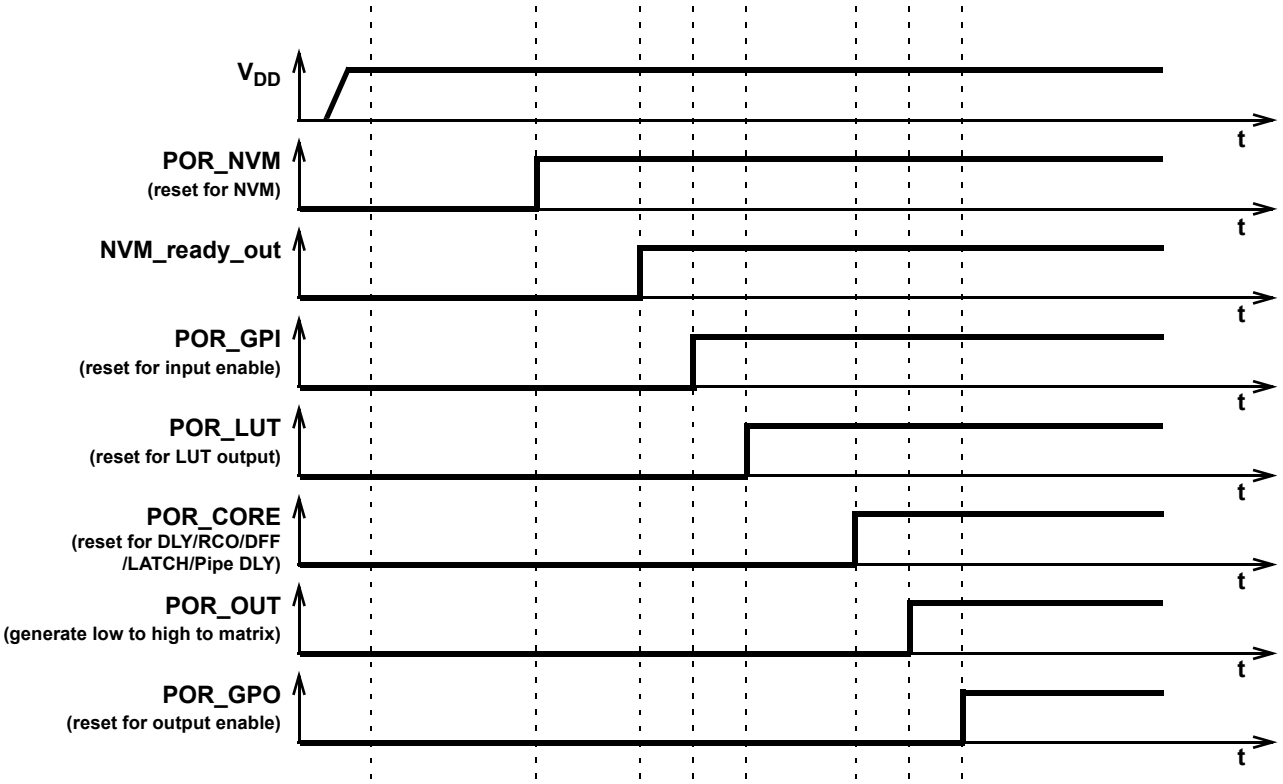


Figure 93. POR Sequence

As can be seen from Figure 93 after the V_{DD} has start ramping up and crosses the Power-On Threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix, which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSC, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46535-EV operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 94 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs, which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

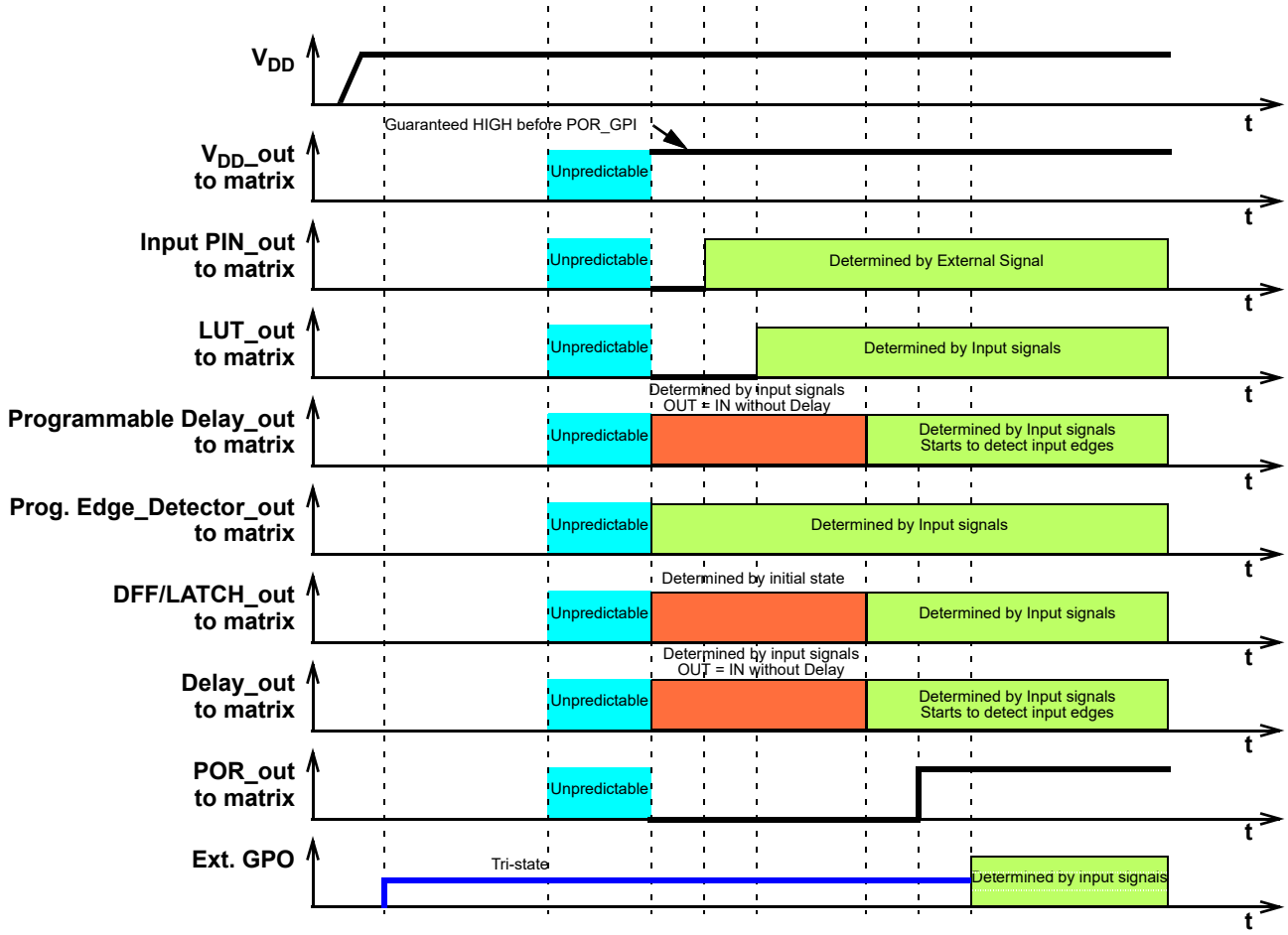


Figure 94. Internal Macrocell States during POR Sequence

14.3.1 Initialization

All internal macrocells by default have initial LOW level. Starting from indicated power-up time of 1.15 V to 1.6 V, macrocells in GPAK5 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. I^2C.
2. Input PINs, ACMP, Pull-up/down.
3. LUTs.
4. DFFs, Delays/Counters, Pipe Delay.
5. POR output to matrix.
6. Output PIN corresponds to the internal logic.

The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any PIN should not be higher than the V_{DD} level. There are ESD Diodes between PIN → V_{DD} and PIN → GND on each PIN. So, if the input signal applied to PIN is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input PIN, and V_{DD} will be pulled up, following the voltage on the input PIN. There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2 Power-Down

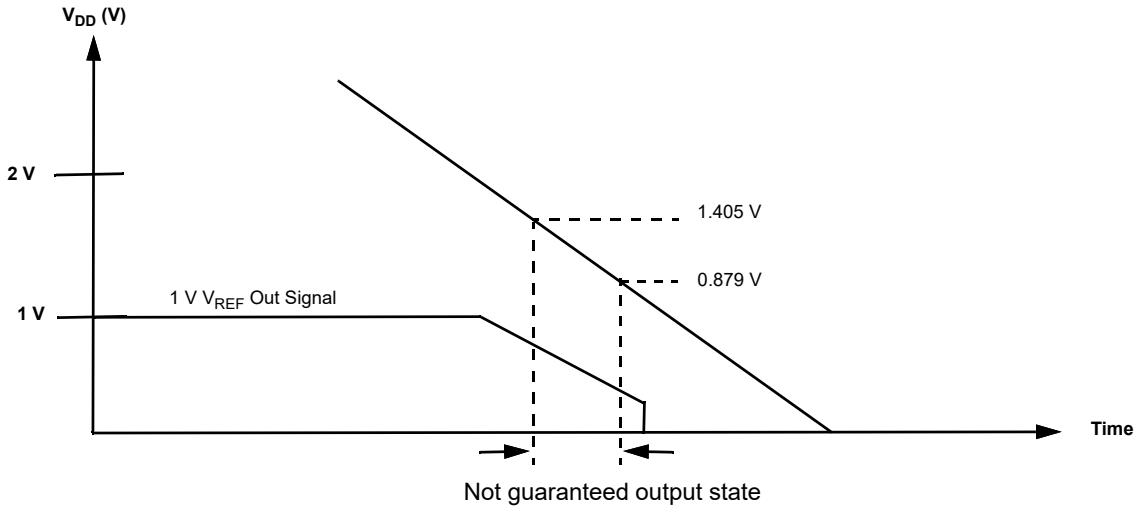


Figure 95. Power-Down

During power-down, macrocells in SLG46535-EV are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15. Asynchronous State Machine Macrocell

15.1 ASM Macrocell Overview

The Asynchronous State Machine (ASM) macrocell is designed to allow the user to create state machines with between 2 to 8 states. The user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in Figure 96.

This macrocell has a total of 25 inputs, as shown in Figure 97, which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state. Each of the 24 inputs is level sensitive and active high, meaning that a high level input will drive the user selected transition from one state to another. The fact that there are 24 inputs puts the upper bound of 24 possible state transitions total in the user defined state machine design. There is on nReset input, which will drive an immediate state transition to the user-defined Initial/Reset state when active, shown in red, in Figure 96. For more details refer to section 15.2 ASM Inputs.

There are a total of 8 outputs, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states. This information is held in the Connection Matrix Output RAM. For more details refer to section 15.3 ASM Outputs.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including IO delays, to ensure that signals are properly processed, and state transitions are deterministic.

The GPAK Designer development tools support user designs for the ASM macrocell at both the physical level and logic level. Figure 96 is a representation of the user design at the logical level, and Figure 97 shows the physical resources inside the macrocell. To best utilize this macrocell, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

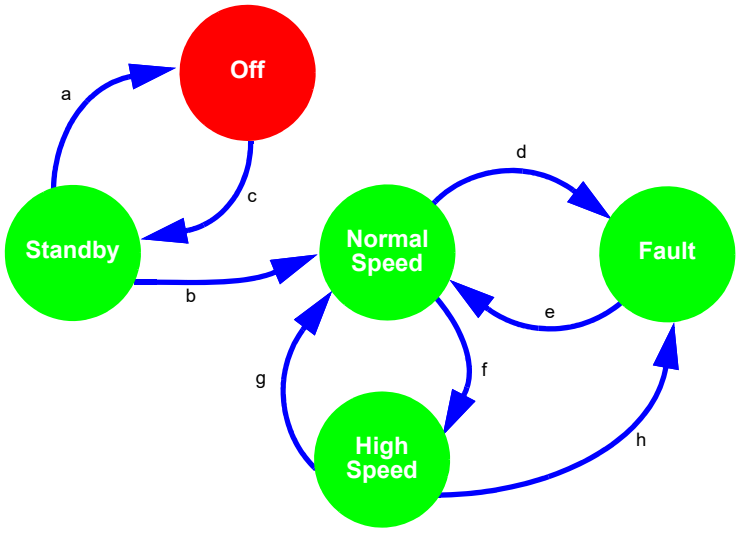


Figure 96. Asynchronous State Machine State Transitions

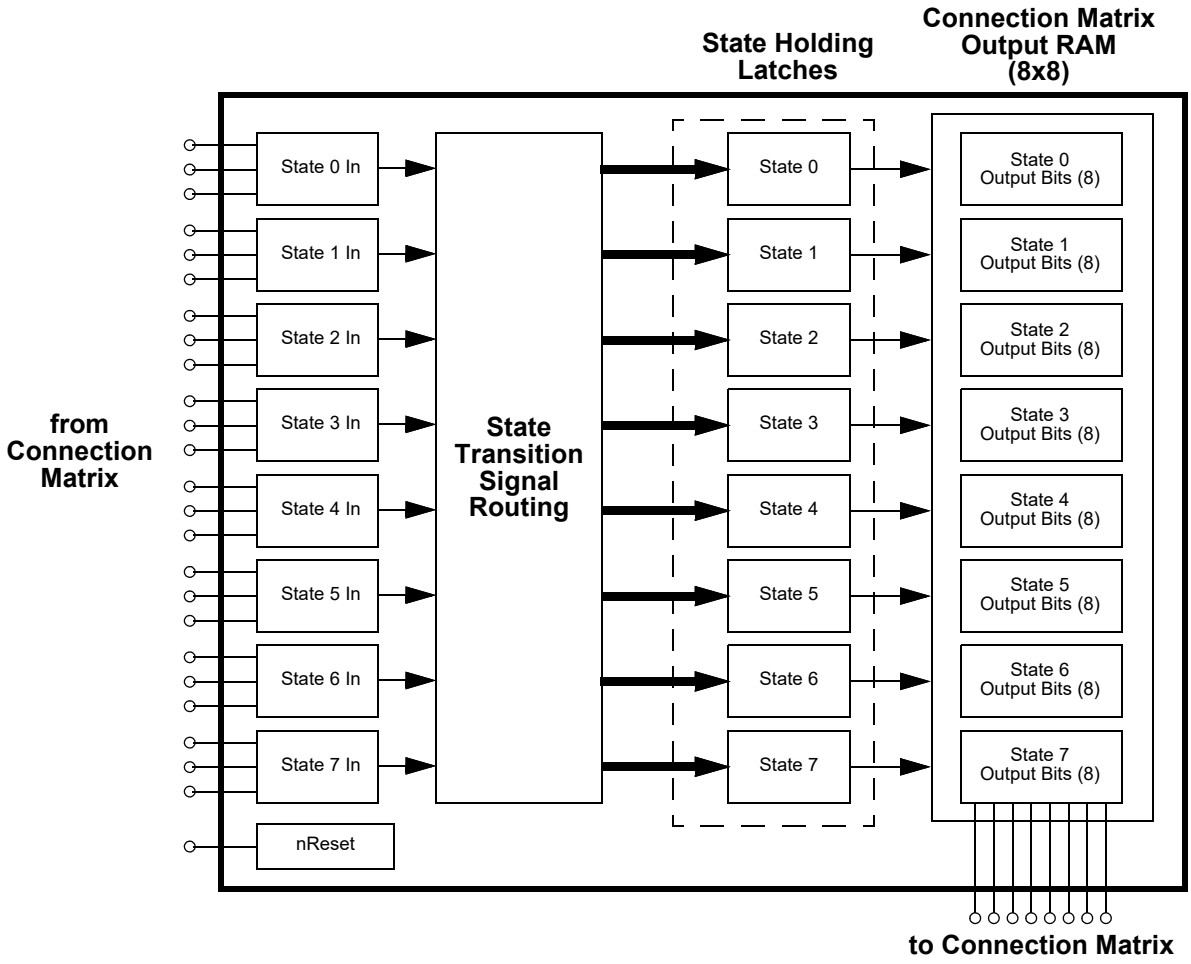


Figure 97. Asynchronous State Machine

15.2 ASM Inputs

The ASM macrocell has a total of 25 inputs, which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state.

There are a total of 24 inputs to the ASM macrocell for general state transitions, highlighted in red in Figure 98. Each of these inputs is level sensitive and active high. A high level input will trigger a state transition.

These inputs are grouped so that each set of 3 inputs can drive a state transition going into a particular state. As an example, there are three inputs that can drive a state transition to State 1. This sets an upper bound on the number of transitions that the user can select going into a particular state to be 3, shown in Figure 99.

There is no limitation on the number of transitions that can be supported coming out of a particular state, the user can select to have transitions going from a state to all other states, shown in Figure 100.

The ASM macrocell also has an nReset input highlighted in blue in Figure 98. This input is level sensitive and active low. An active signal on this input will drive an immediate state transition to the user-defined Initial/Reset state. The user can choose which state within the ASM Editor inside GPAK Designer is the initial state.

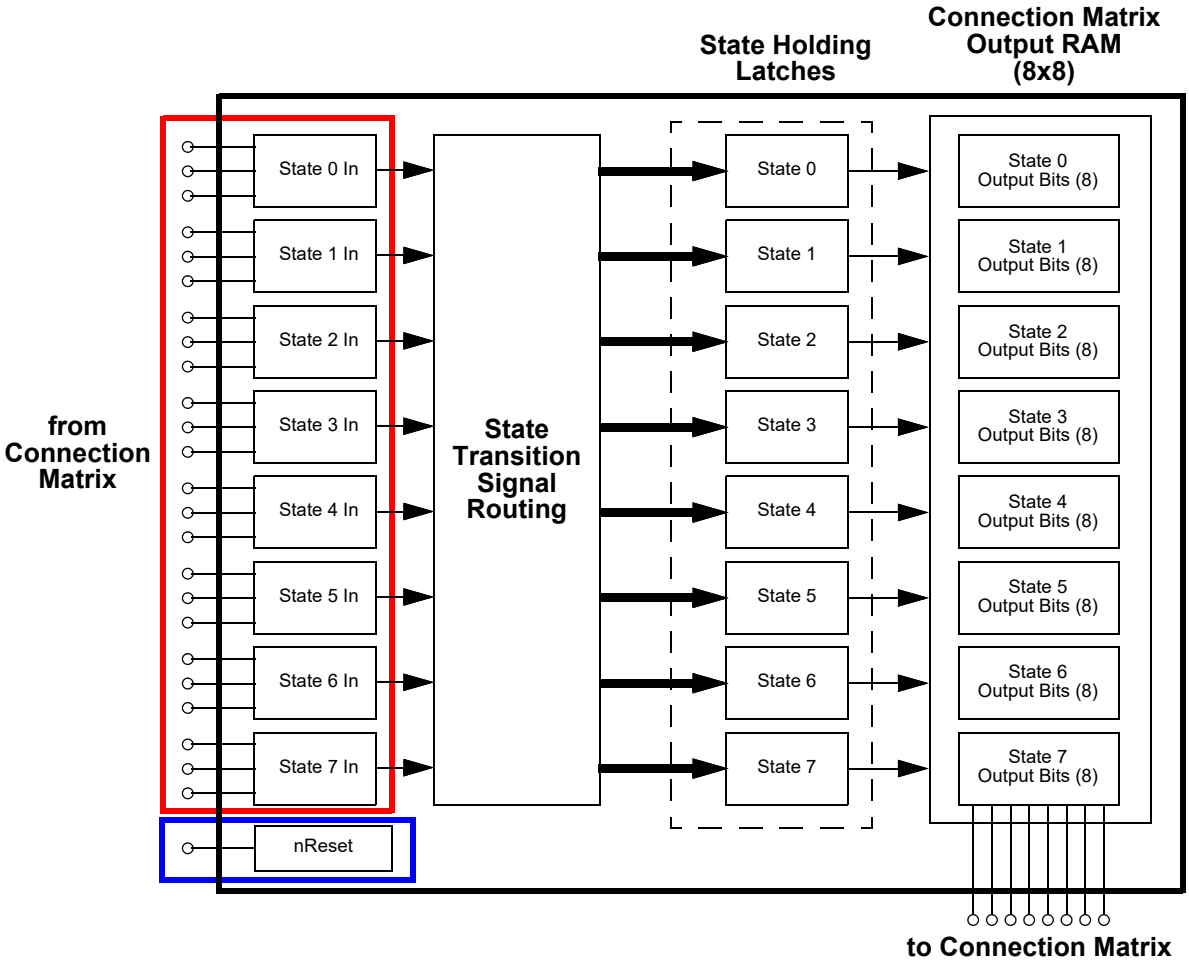


Figure 98. Asynchronous State Machine Inputs

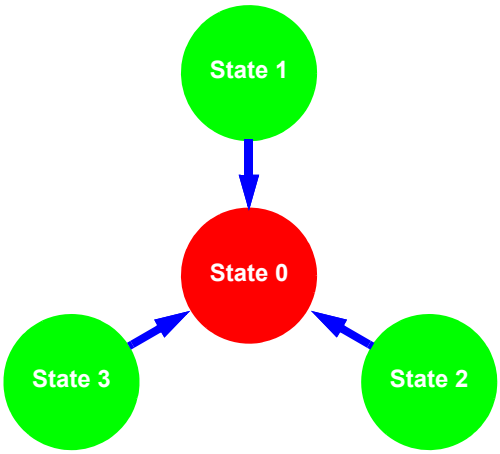


Figure 99. Maximum 3 State Transitions into Given State

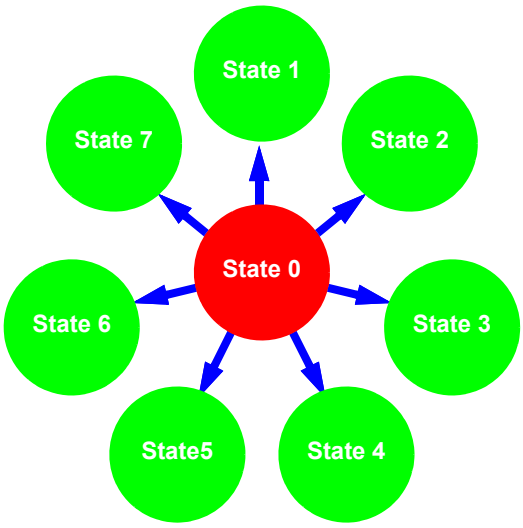


Figure 100. Maximum 7 State Transitions out of a Given State

15.3 ASM Outputs

There are a total of 8 outputs from the ASM macrocell, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states, this information is held in the Connection Matrix Output RAM, shown in Figure 101. The Connection Matrix Output RAM has a total of 64 bits, arranged as 8 bits per state. The values loaded in each of the 8 bits define the signal level on each of the 8 ASM macrocell outputs.

The ASM Editor inside the GPAK Designer software allows the user to make their selections for the value of each bit in the Connection Matrix Output RAM, which selects the level of the macrocell outputs based on the current state of the ASM macrocell, as shown in Figure 101.

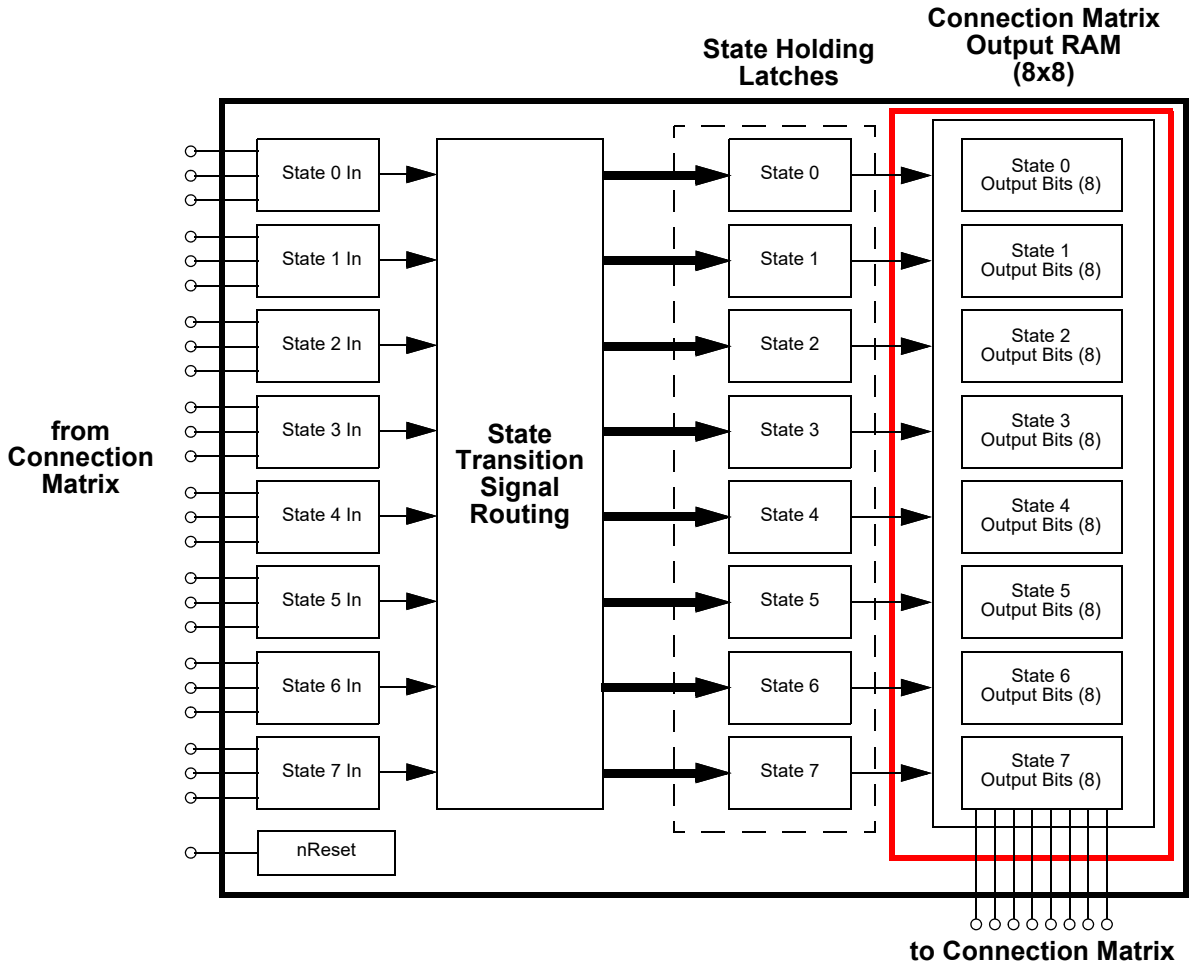


Figure 101. Connection Matrix Output RAM

Table 36. ASM Editor - Connection Matrix Output RAM

RAM								
State name	Connection Matrix Output RAM							
	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
State 0	0	0	0	0	0	0	0	1
State 1	0	0	0	0	0	0	1	0
State 2	0	0	0	0	0	1	0	0
State 3	0	0	0	0	1	0	0	0
State 4	0	0	0	1	0	0	0	0
State 5	0	0	1	0	0	0	0	0
State 6	0	1	0	0	0	0	0	0
State 7	1	0	0	0	0	0	0	0

There is a possibility to configure ASM (it's settings and transitions) via I2C. Registers (registers [197:0]) correspond for ASM inputs, registers (registers [1727:1664]) correspond for ASM outputs configuration. Using I2C commands (see section 16.4 I2C Serial Communications Commands) it is possible to read ASM settings and connections, as well as change them. Additionally, the user can change Connection Matrix Output RAM bit configuration (bytes 0xD0 to 0xD7).

Note: After Connection Matrix Output RAM was updated via I2C, ASM outputs to Connection Matrix can be changed only after ASM changes its state or after reset event. To change ASM outputs to Connection Matrix instantly after I2C write command, ASM must be in reset all the time.

15.4 Basic ASM Timing

The basic state transition timing from input on Matrix Connection output to output on Matrix Connection input is shown in Figure 102 and Figure 103. The time from a valid input signal to the time that there is a valid change of state and valid signals being available on the state outputs is State Machine Output Delay Time ($T_{st\_out\_delay}$). The minimum and maximum values of $T_{st\_out\_delay}$ define the differential timing between the shortest state transition (input on matrix output and output on matrix input) and the longest state transition (input on matrix output and output on matrix input).

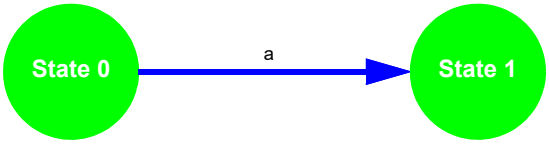


Figure 102. State Transition

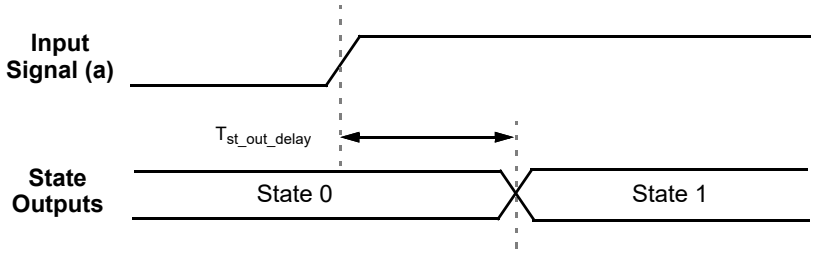


Figure 103. State Transition Timing

15.5 Asynchronous State Machines vs. Synchronous State Machines

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals.

2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.

3. This macrocell does not have traditional set-up and hold time specifications, which are related to incoming clock, as this macrocell has no clock source.

4. The macrocell only consumes power while in state transition.

15.6 ASM Power Considerations

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. Shown in Figure 102 and Figure 104, the current consumption of the macrocell will be a fraction of a µA between state transitions, and will rise only during state transitions. See section 3.4.4 Macrocells Current Consumption to find average current during state transitions.

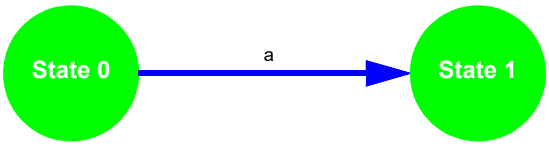


Figure 104. State Transition

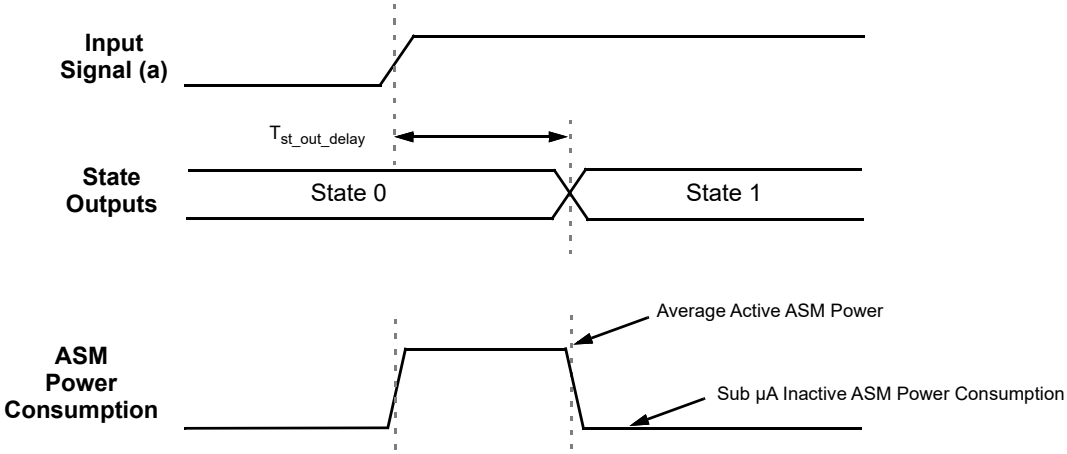


Figure 105. State Transition Timing and Power Consumption

15.7 ASM Logical vs. Physical Design

A successful design with the ASM macrocell must include both the logic level design, as well as the physical level design. The GPAK Designer development software support user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial/Reset state, and define the output values for the 8 outputs in the Output RAM Matrix. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as making connections for destinations for ASM output signals.

15.8 ASM Special Case Timing Considerations

15.8.1 State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine macrocell for a state transition is a pulse, there is a minimum pulse width on the input to the state machine macrocell (as measured at the matrix input to the macrocell), which is guaranteed to result in a state transition shown in Figure 106 and Figure 107. This pulse width is defined by the State Machine Input Pulse Acceptance Time (T_{st_pulse}). If a pulse width that is shorter than T_{st_pulse} is input to the state machine macrocell, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of T_{st_pulse}), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

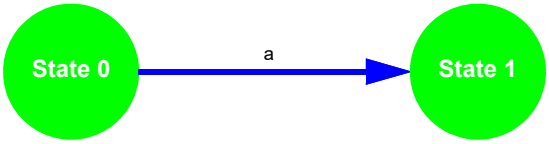


Figure 106. State Transition

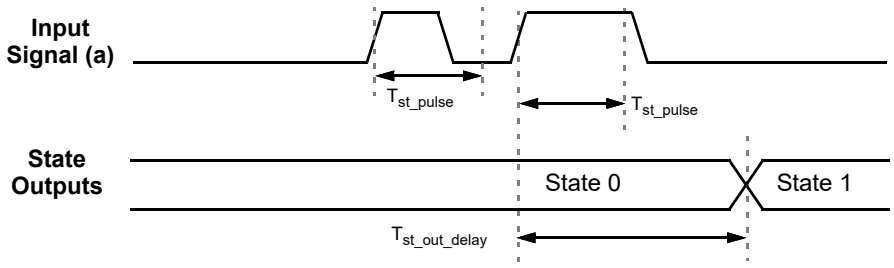


Figure 107. State Transition Pulse Input Timing

15.8.2 State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are “competing” (signals a and b in Figure 108), and the signal that arrives sooner should drive the state transition that will “win”, or drive the state transition. If one signal arrives T_{st_comp} before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in Figure 109. If the two signals arrive within T_{st_comp} of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in the paragraph above, as shown in Figure 110.

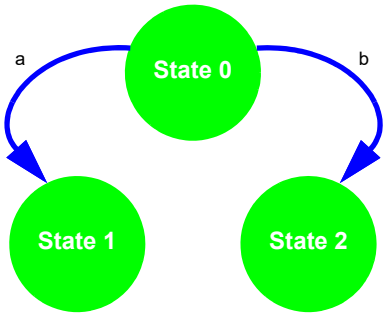


Figure 108. State Transition - Competing Inputs

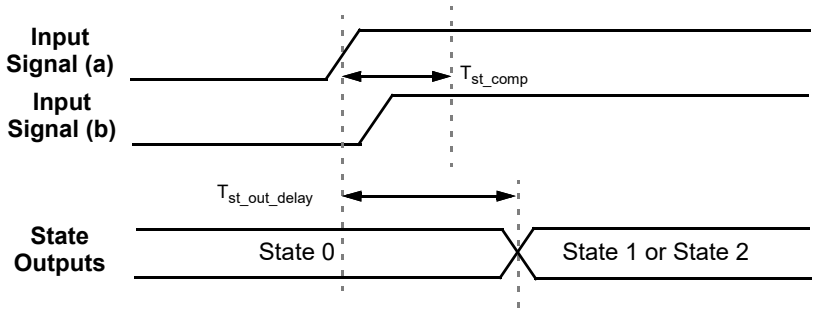


Figure 109. State Transition Timing - Competing Inputs Indeterminate

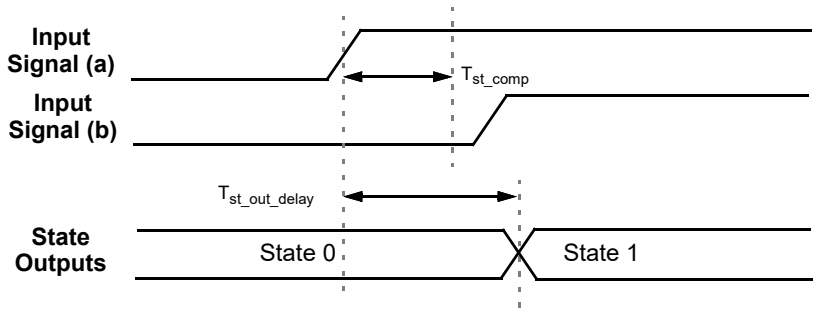


Figure 110. State Transition Timing - Competing Inputs Determinable

15.8.3 ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the macrocell will only stay in that particular state for $T_{st\_out\_delay}$ time before making the transition to the next state. An example of this sequential behavior is shown in Figure 111 and the associated timing is shown in Figure 112.

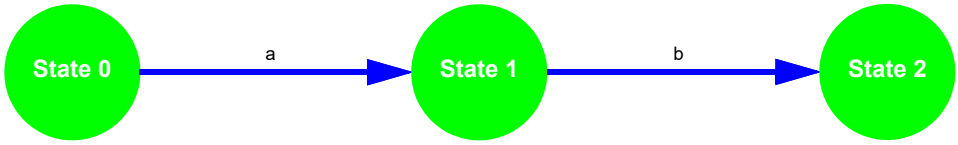


Figure 111. State Transition - Sequential

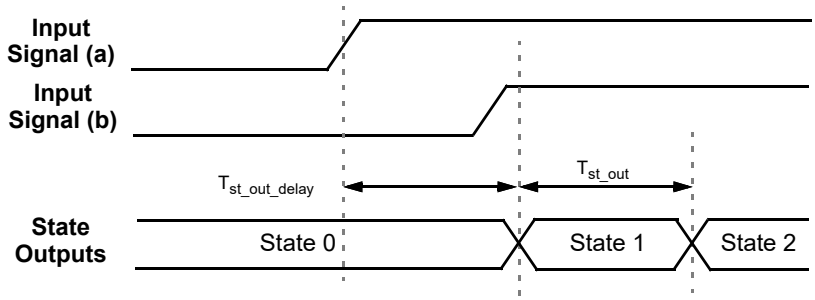


Figure 112. State Transition - Sequential Timing

15.8.4 State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by $T_{st\_out\_delay}$. The example shown in Figure 113 involves cycling between two states, but any number of two – eight states can be included in state transition closed cycling of this nature. Figure 114 shows the associated timing for closed cycling.

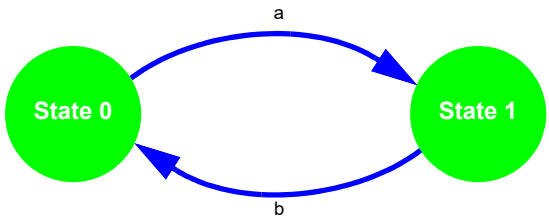


Figure 113. State Transition - Closed Cycling

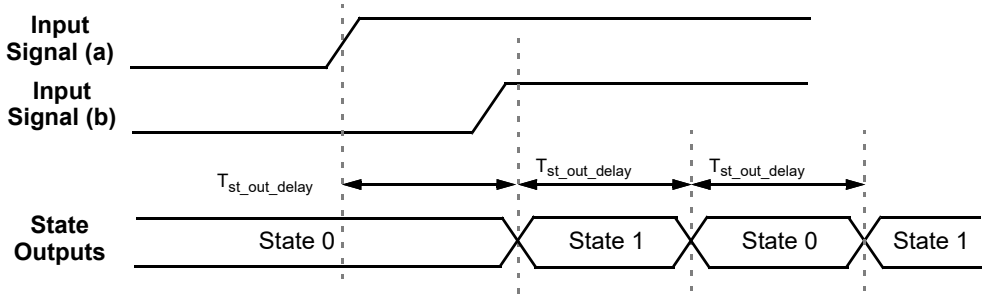


Figure 114. State Transition - Closed Cycling Timing

16. I²C Serial Communications Macrocell

16.1 I²C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Controller to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Controller is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Controller the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits register [1832], register [1870], and register [1871]. See section 16.5 I2C Serial Command Register Protection for more details on I²C read/write memory protection.

Note: GreenPAK I²C is fully compatible with standard I²C protocol.

16.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 115. After the Start bit, the first four bits are a control code, which can be set by the user in registers [1867:1864]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/$\overline{W}$ bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other target device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46535-EV are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46535-EV.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 115 shows this basic command structure.

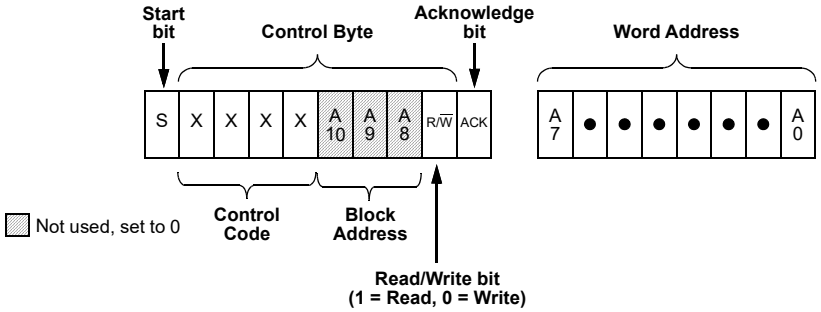


Figure 115. Basic Command Structure

16.3 I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 116. Timing specifications can be found in the section 3.4.2 I2C Pins Electrical Specifications.

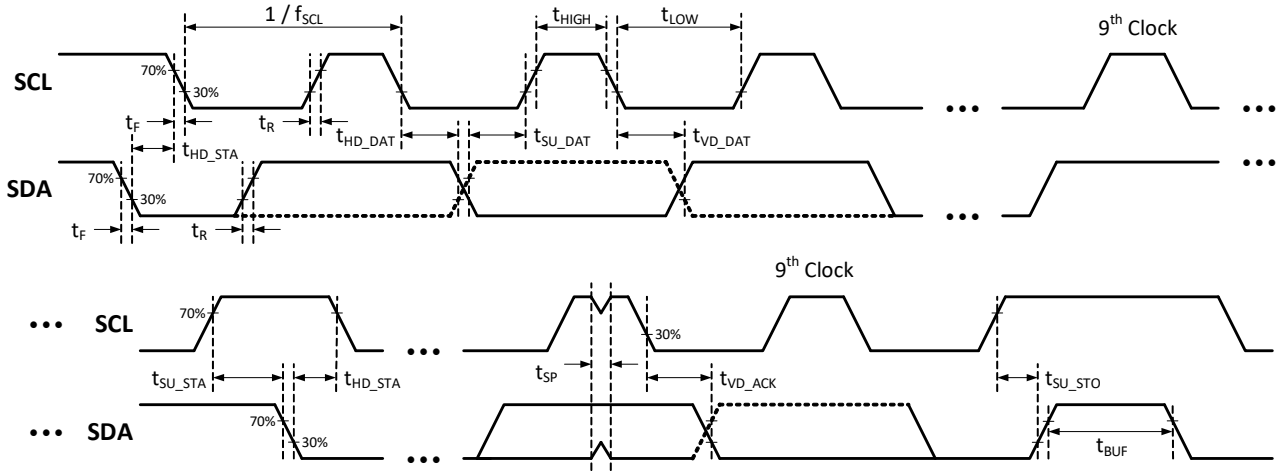


Figure 116. I²C General Timing Characteristics

16.4 I²C Serial Communications Commands

16.4.1 Byte Write Command

Following the Start condition from the Controller, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”) are placed onto the I²C bus by the Controller. After the SLG46535-EV sends an Acknowledge bit (ACK), the next byte transmitted by the Controller is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46535-EV, where the data byte is to be written. After the SLG46535-EV sends another Acknowledge bit, the Controller will transmit the data byte to be written into the addressed memory location. The SLG46535-EV again provides an Acknowledge bit and then the Controller generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46535-EV generates the Acknowledge bit.

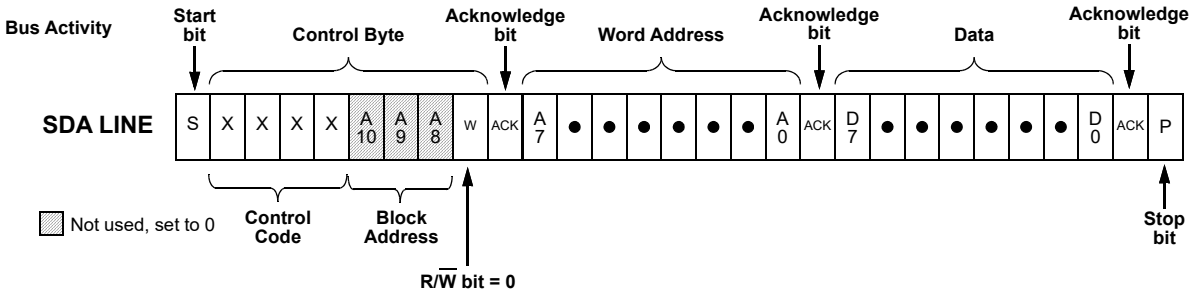


Figure 117. Byte Write Command, R/$\overline{W}$ = 0

16.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG46535-EV in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Controller continues to transmit data bytes to the SLG46535-EV. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46535-EV generates the Acknowledge bit.

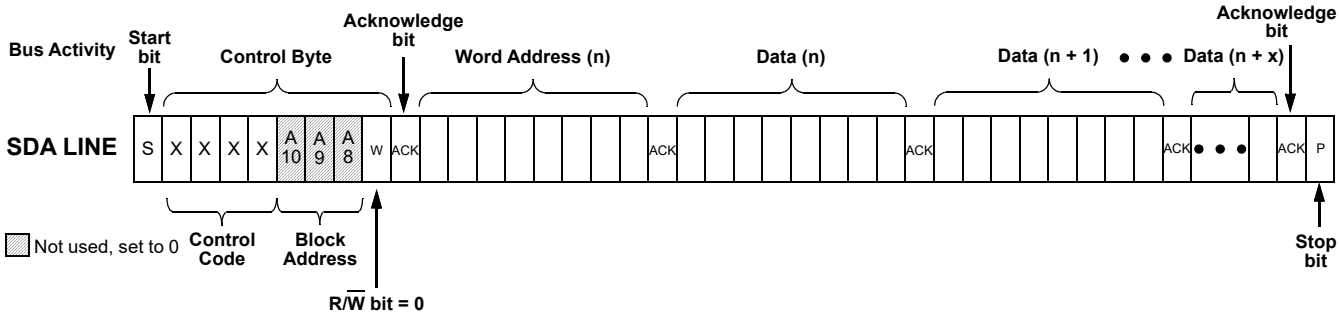


Figure 118. Sequential Write Command

16.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Write or Random Read command (which contains a write control byte) writes or reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Controller, with the R/$\overline{W}$ bit = “1”. The SLG46535-EV will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Controller will not issue an Acknowledge bit, and follow immediately with a Stop condition.

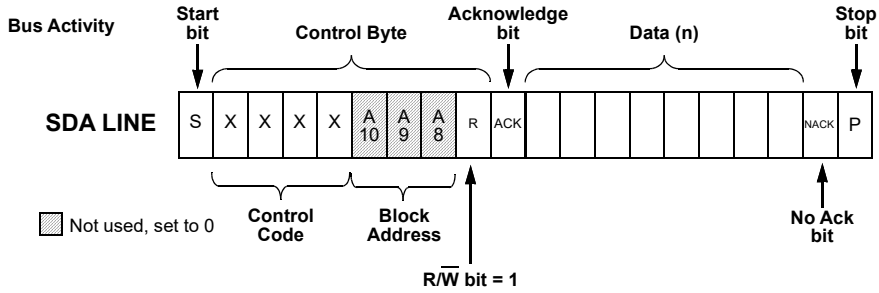


Figure 119. Current Address Read Command, R/W = 1

16.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Controller issues a second control byte with the R/W bit set to “1”, after which the SLG46535-EV issues an Acknowledge bit, followed by the requested eight data bits.

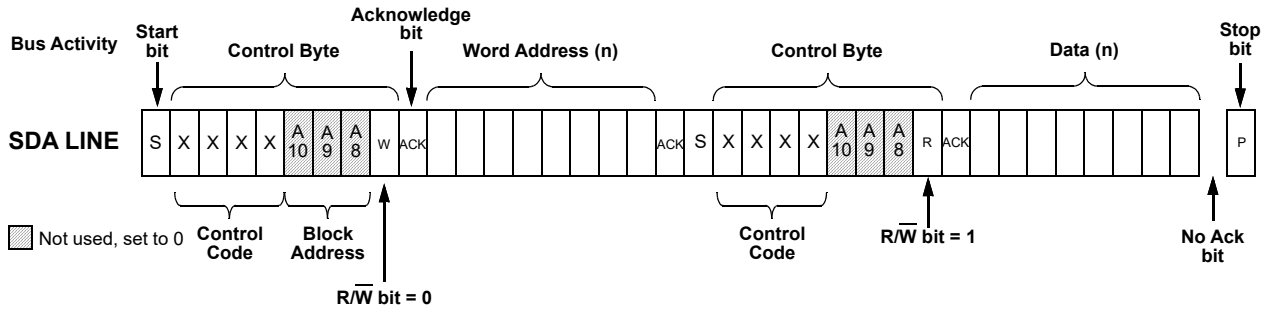


Figure 120. Random Read Command

16.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Current Address Read or Random Read command, except that once the SLG46535-EV transmits the first data byte, the Controller issues an Acknowledge bit as opposed to a Stop condition in a random read. The Controller can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

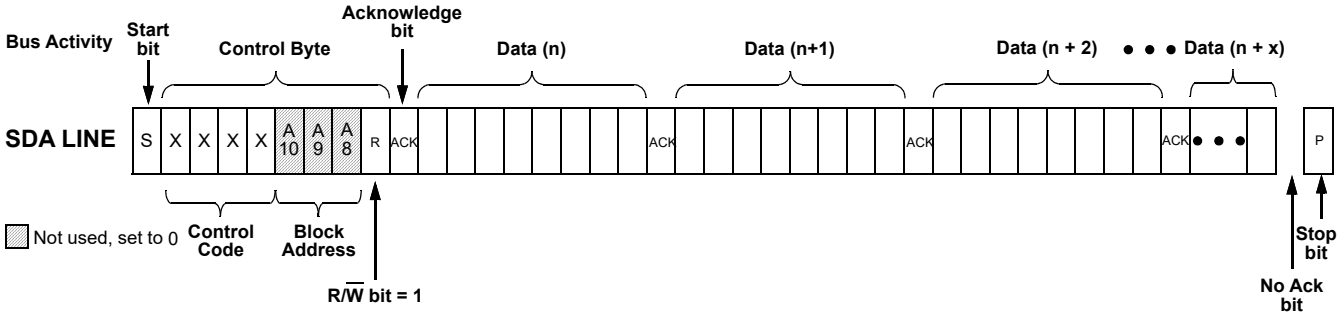


Figure 121. Sequential Read Command

16.4.6 I²C Serial Command Register Map

These register addresses are broken down into four Banks to give the user greater control on access to reading and writing information in each bank. Each of the four banks is 512 bits (64 bytes) in length. Writing information to register bits in these Banks will change the configuration of the device, resulting in either a change in the interconnection options provided by the Connection Matrix, or by changing the configuration of individual macrocells. During device use, all register bits can be read or written via I²C, unless protection bits are set to prevent this.

See section 17. Register Definitions for detailed information on all register bits.

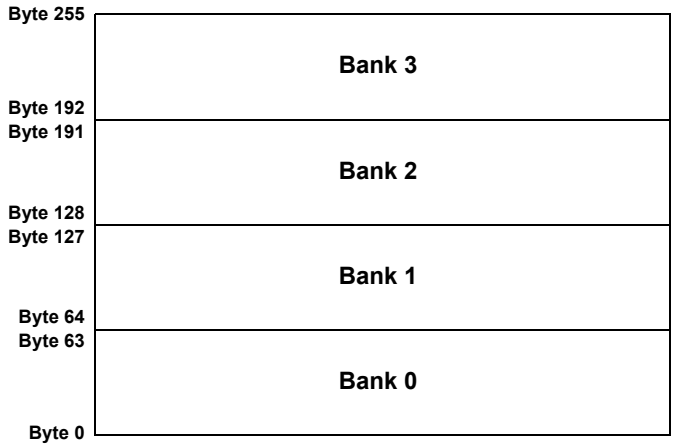


Figure 122. Register Bank Map

16.5 I²C Serial Command Register Protection

The memory space is divided into four banks, each of which has 512bits (64bytes). There are three bits that allow the user to define rules for reading and writing bits in each of these banks via I²C:

- Register [1832] I²C lock for read bits [1535:0] (Bank 0/1/2). If the system provides any read commands to the addresses in these three banks, the device will respond with 'FFH' in data field.
- Register [1871] I²C lock for write bits [1535:0] (Bank 0/1/2). If the system provides any write commands to the addresses in these three banks, the device will acknowledge these commands, but will not do internal writes to the register space.
- Register [1870] I²C lock for write all bits (Bank 0/1/2/3). If the system provides any write commands to the addresses in these four banks, the device will acknowledge these commands, but will not do internal writes to the register space.

Note 1: Register [1870] is higher priority than register [1871], and if register [1870] is set, than register [1871] does not have any effect.

Note 2: If the user sets Pins 8 and 9 function to a selection other than SDA and SCL, all access via I²C will be disabled.

If register [1870] is not set, register bits in Bank 3 are open to read and write commands via I²C with the following exceptions:

- register [1871] Bank 0/1/2 I²C-write protection bit is always protected from I²C write
- registers [1867:1864] I²C Control Code Bit [3:0] is always protected from I²C write.

Note: Any write commands that come to the device via I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See section 17. Register Definitions for detailed information on all registers.

16.5.1 Register Read/Write Protection

There are six read/write protect modes for the design sequence from being corrupted or copied. See Table 37 for details.

Table 37. Read/Write Protection Options

Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits [1535:0]	Locked for write bits [1535:0]	Locked for write all bits	Locked for read and write bits [1535:0]	Locked for read bits [1535:0] and write all bits
				register [1832] = 0, [1871] = 0, [1870] = 0	register [1832] = 1, [1871] = 0, [1870] = 0	register [1832] = 0, [1871] = 1, [1870] = 0	register [1832] =0, [1871] = x, [1870] = 1	register [1832] = 1, [1871] = 1, [1870] = 0	register [1832] = 1, [1871] = x, [1870] = 1
0	0-63	511-0	Connection Matrix Outputs Configuration	R/W	W	R	R	-	-
1	64-109	879-512		R/W	W	R	R	-	-
	110-127	880-1023	Reserved	-	-	-	-	-	-
2	128-186	1495-1024	Function Configuration for PINs, LUTs/DFFs, OSC, ASM, and some configuration for DLYs, ACMP	R/W	W	R	R	-	-
	187-191	1535-1496	Reserved	-	-	-	-	-	-
3	192-206	1655-1536	CNT/DLY counter data and some LUTs truth table, ACMP V_{REF}	R/W	R/W	R/W	R	R/W	R
	207	1662	I²C reset bit with reloading NVM into Data register	R/W	R/W	R/W	R	R/W	R
		1661-1659, 1663	Reserved	R	R	R	R	R	R
		1658-1656	OSC Power Control	R/W	R/W	R/W	R	R/W	R

Table 37. Read/Write Protection Options (Cont.)

Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits [1535:0]	Locked for write bits [1535:0]	Locked for write all bits	Locked for read and write bits [1535:0]	Locked for read bits [1535:0] and write all bits
				register [1832] = 0, [1871] = 0, [1870] = 0	register [1832] = 1, [1871] = 0, [1870] = 0	register [1832] = 0, [1871] = 1, [1870] = 0	register [1832] =0, [1871] = x, [1870] = 1	register [1832] = 1, [1871] = 1, [1870] = 0	register [1832] = 1, [1871] = x, [1870] = 1
3	208-223	1791-1664	ASM output RAM and User configurable RAM/OTP	R/W	R/W	R/W	R	R/W	R
	224-227	1823-1792	Reserved	-	-	-	-	-	-
	228	1831-1824	Reserved	R/W	R/W	R/W	R	R/W	R
	229	1839-1836	Product Family ID	R	R	R	R	R	R
		1835-1834	Reserved	-	-	-	-	-	-
		1833	Reserved	R	R	R	R	R	R
		1832	I^2C Lock for read bits [1535:0]	R	R	R	R	R	R
	230	1847-1840	Pattern ID	R/W	R/W	R/W	R	R/W	R
	231	1855-1848	Reserved	R	R	R	R	R	R
	232	1863-1856	Reserved	R	R	R	R	R	R
	233	1871	I^2C Lock for write bits [1535:0]	R	R	R	R	R	R
		1870	I^2C Lock for write all bits	R	R	R	R	R	R
		1869-1868	Reserved	-	-	-	-	-	-
		1867-1864	I^2C Control Code	R	R	R	R	R	R
	234-239	1919-1872	Counter Current Value	R	R	R	R	R	R
	240-243	1951-1920	Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R
	244	1959-1952	Connection Matrix Virtual Inputs	R/W	R/W	R/W	R	R/W	R
	245-247	1983-1960	Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R
	248-250	2007-1984	Reserved	R	R	R	R	R	R
3	251	2015-2008	Reserved	R/W	R/W	R/W	R	R/W	R
	252-253	2031-2016	Reserved	R	R	R	R	R	R
	254	2039-2032	Reserved	R/W	R/W	R/W	R	R/W	R
	255	2047-2040	Reserved	R/W	R/W	R/W	R	R/W	R

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

16.5.2 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power-up conditions, including configuration of all macrocells and all connections provided by the Connection Matrix. This is implemented by setting register [1662] I²C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1662] will be set to “0” automatically. Figure 123 illustrates the sequence of events for this reset function.

Note: I²C Serial Reset Command is not available during emulation.

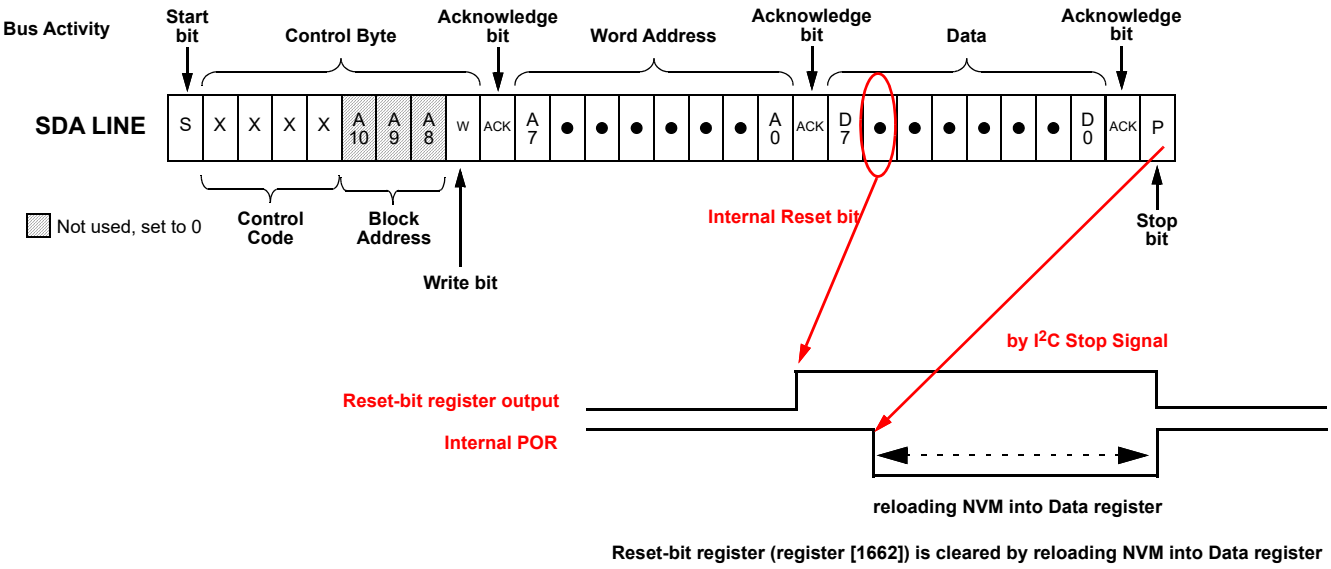


Figure 123. Reset Command Timing

16.6 I²C Additional Options

16.6.1 Reading Counter Data via I²C

The current count value in four counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0 and CNT1, and 8-bit counters CNT4 and CNT6.

16.6.2 User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I²C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User

Configurable RAM/OTP Byte 0) is located at I²C address 0xD8, and the highest order byte in this array is located at I²C address 0xDF.

Table 38. RAM Array Table

I²C Address (hex)	Highest Bit Address	Lowest Bit Address	Memory Byte
D8	1735	1728	User Configurable RAM/OTP Byte 0
D9	1743	1736	User Configurable RAM/OTP Byte 1
DA	1751	1744	User Configurable RAM/OTP Byte 2
DB	1759	1752	User Configurable RAM/OTP Byte 3
DC	1767	1760	User Configurable RAM/OTP Byte 4
DD	1775	1768	User Configurable RAM/OTP Byte 5
DE	1783	1776	User Configurable RAM/OTP Byte 6
DF	1791	1784	User Configurable RAM/OTP Byte 7

17. Register Definitions

17.1 Register Map

Table 39. Register Map

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Note: For register [0] to register [1495], I²C Read is valid (assuming register [1832] = 0), I²C Write is valid (assuming register [1871] = 0).					
Matrix 64-to-1 MUX's 6 Selection Bits					
00	5:0	Matrix OUT	ASM-state0-EN0	Valid	Valid
	7:6	Reserved		Valid	Valid
01	13:8	Matrix OUT	ASM-state0-EN1	Valid	Valid
	15:14	Reserved		Valid	Valid
02	21:16	Matrix OUT	ASM-state0-EN2	Valid	Valid
	23:22	Reserved		Valid	Valid
03	29:24	Matrix OUT	ASM-state1-EN0	Valid	Valid
	31:30	Reserved		Valid	Valid
04	37:32	Matrix OUT	ASM-state1-EN1	Valid	Valid
	39:38	Reserved		Valid	Valid
05	45:40	Matrix OUT	ASM-state1-EN2	Valid	Valid
	47:46	Reserved		Valid	Valid
06	53:48	Matrix OUT	ASM-state2-EN0	Valid	Valid
	55:54	Reserved		Valid	Valid
07	61:56	Matrix OUT	ASM-state2-EN1	Valid	Valid
	63:62	Reserved		Valid	Valid
08	69:64	Matrix OUT	ASM-state2-EN2	Valid	Valid
	71:70	Reserved		Valid	Valid
09	77:72	Matrix OUT	ASM-state3-EN0	Valid	Valid
	79:78	Reserved		Valid	Valid
0A	85:80	Matrix OUT	ASM-state3-EN1	Valid	Valid
	87:86	Reserved		Valid	Valid
0B	93:88	Matrix OUT	ASM-state3-EN2	Valid	Valid
	95:94	Reserved		Valid	Valid
0C	101:96	Matrix OUT	ASM-state4-EN0	Valid	Valid
	103:102	Reserved		Valid	Valid
0D	109:104	Matrix OUT	ASM-state4-EN1	Valid	Valid
	111:110	Reserved		Valid	Valid
0E	117:112	Matrix OUT	ASM-state4-EN2	Valid	Valid
	119:118	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
0F	125:120	Matrix OUT	ASM-state5-EN0	Valid	Valid
	127:126	Reserved		Valid	Valid
10	133:128	Matrix OUT	ASM-state5-EN1	Valid	Valid
	135:134	Reserved		Valid	Valid
11	141:136	Matrix OUT	ASM-state5-EN2	Valid	Valid
	143:142	Reserved		Valid	Valid
12	149:144	Matrix OUT	ASM-state6-EN0	Valid	Valid
	151:150	Reserved		Valid	Valid
13	157:152	Matrix OUT	ASM-state6-EN1	Valid	Valid
	159:158	Reserved		Valid	Valid
14	165:160	Matrix OUT	ASM-state6-EN2	Valid	Valid
	167:166	Reserved		Valid	Valid
15	173:168	Matrix OUT	ASM-state7-EN0	Valid	Valid
	175:174	Reserved		Valid	Valid
16	181:176	Matrix OUT	ASM-state7-EN1	Valid	Valid
	183:182	Reserved		Valid	Valid
17	189:184	Matrix OUT	ASM-state7-EN2	Valid	Valid
	191:190	Reserved		Valid	Valid
18	197:192	Matrix OUT	ASM-state-nRST	Valid	Valid
	199:198	Reserved		Valid	Valid
19	205:200	Reserved		Valid	Valid
	207:206	Reserved		Valid	Valid
1A	213:208	Reserved		Valid	Valid
	215:214	Reserved		Valid	Valid
1B	221:216	Matrix OUT	PIN3 Digital Output Source	Valid	Valid
	223:222	Reserved		Valid	Valid
1C	229:224	Reserved		Valid	Valid
	231:230	Reserved		Valid	Valid
1D	237:232	Reserved		Valid	Valid
	239:238	Reserved		Valid	Valid
1E	245:240	Matrix OUT	PIN4 Digital Output Source	Valid	Valid
	247:246	Reserved		Valid	Valid
1F	253:248	Matrix OUT	PIN5 Digital Output Source	Valid	Valid
	255:254	Reserved		Valid	Valid
20	261:256	Matrix OUT	PIN5 Output Enable	Valid	Valid
	263:262	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
21	269:264	Matrix OUT	PIN6 Digital Output Source (SCL with VI/Input and NMOS open-drain)	Valid	Valid
	271:270	Reserved		Valid	Valid
22	277:272	Matrix OUT	PIN7 Digital Output Source (SDA with VI/Input and NMOS open-drain)	Valid	Valid
	279:278	Reserved		Valid	Valid
23	285:280	Matrix OUT	PIN8 Digital Output Source	Valid	Valid
	287:286	Reserved		Valid	Valid
24	293:288	Matrix OUT	PIN8 Output Enable	Valid	Valid
	295:294	Reserved		Valid	Valid
25	301:296	Matrix OUT	PIN10 Digital Output Source	Valid	Valid
	303:302	Reserved		Valid	Valid
26	309:304	Reserved		Valid	Valid
	311:310	Reserved		Valid	Valid
27	317:312	Reserved		Valid	Valid
	319:318	Reserved		Valid	Valid
28	325:320	Matrix OUT	Inverter Input	Valid	Valid
	327:326	Reserved		Valid	Valid
29	333:328	Reserved		Valid	Valid
	335:334	Reserved		Valid	Valid
2A	341:336	Reserved		Valid	Valid
	343:342	Reserved		Valid	Valid
2B	349:344	Matrix OUT	PIN12 Digital Output Source	Valid	Valid
	351:350	Reserved		Valid	Valid
2C	357:352	Matrix OUT	PIN12 Output Enable	Valid	Valid
	359:358	Reserved		Valid	Valid
2D	365:360	Matrix OUT	PIN13 Digital Output Source	Valid	Valid
	367:366	Reserved		Valid	Valid
2E	373:368	Reserved		Valid	Valid
	375:374	Reserved		Valid	Valid
2F	381:376	Reserved		Valid	Valid
	383:382	Reserved		Valid	Valid
30	389:384	Reserved		Valid	Valid
	391:390	Reserved		Valid	Valid
31	397:392	Reserved		Valid	Valid
	399:398	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
32	405:400	Matrix OUT	PIN14 Digital Output Source	Valid	Valid
	407:406	Reserved		Valid	Valid
33	413:408	Matrix OUT	ACMP0 nPD (Power-Down)	Valid	Valid
	415:414	Reserved		Valid	Valid
34	421:416	Matrix OUT	ACMP1 nPD (Power-Down)	Valid	Valid
	423:422	Reserved		Valid	Valid
35	429:424	Matrix OUT	ACMP2 nPD (Power-Down)	Valid	Valid
	431:430	Reserved		Valid	Valid
36	437:432	Reserved		Valid	Valid
	439:438	Reserved		Valid	Valid
37	445:440	Matrix OUT	Input of Filter_0 with fixed time edge detector	Valid	Valid
	447:446	Reserved		Valid	Valid
38	453:448	Matrix OUT	Input of Filter_1 with fixed time edge detector	Valid	Valid
	455:454	Reserved		Valid	Valid
39	461:456	Matrix OUT	Input of Programmable Delay and Edge Detector	Valid	Valid
	463:462	Reserved		Valid	Valid
3A	469:464	Matrix OUT	OSC 25 kHz/2 MHz nPD (Power-Down)	Valid	Valid
	471:470	Reserved		Valid	Valid
3B	477:472	Matrix OUT	OSC 25 MHz nPD (Power-Down)	Valid	Valid
	479:478	Reserved		Valid	Valid
3C	485:480	Matrix OUT	IN0 of 2-bit LUT0 or Clock Input of DFF0	Valid	Valid
	487:486	Reserved		Valid	Valid
3D	493:488	Matrix OUT	IN1 of 2-bit LUT0 or Data Input of DFF0	Valid	Valid
	495:494	Reserved		Valid	Valid
3E	501:496	Matrix OUT	IN0 of 2-bit LUT1 or Clock Input of DFF1	Valid	Valid
	503:502	Reserved		Valid	Valid
3F	509:504	Matrix OUT	IN1 of 2-bit LUT1 or Data Input of DFF1	Valid	Valid
	511:510	Reserved		Valid	Valid
40	517:512	Matrix OUT	IN0 of 2-bit LUT2 or Clock Input of DFF2	Valid	Valid
	519:518	Reserved		Valid	Valid
41	525:520	Matrix OUT	IN1 of 2-bit LUT2 or Data Input of DFF2	Valid	Valid
	527:526	Reserved		Valid	Valid
42	533:528	Matrix OUT	IN0 of 2-bit LUT3 or Clock Input of PGen	Valid	Valid
	535:534	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
43	541:536	Matrix OUT	IN1 of 2-bit LUT3 or nRST of PGen	Valid	Valid
	543:542	Reserved		Valid	Valid
44	549:544	Matrix OUT	IN0 of 3-bit LUT0 or Clock Input of DFF3	Valid	Valid
	551:550	Reserved		Valid	Valid
45	557:552	Matrix OUT	IN1 of 3-bit LUT0 or Data Input of DFF3	Valid	Valid
	559:558	Reserved		Valid	Valid
46	565:560	Matrix OUT	IN2 of 3-bit LUT0 or nRST (nSET) of DFF3	Valid	Valid
	567:566	Reserved		Valid	Valid
47	573:568	Matrix OUT	IN0 of 3-bit LUT1 or Clock Input of DFF4	Valid	Valid
	575:574	Reserved		Valid	Valid
48	581:576	Matrix OUT	IN1 of 3-bit LUT1 or Data Input of DFF4	Valid	Valid
	583:582	Reserved		Valid	Valid
49	589:584	Matrix OUT	IN2 of 3-bit LUT1 or nRST (nSET) of DFF4	Valid	Valid
	591:590	Reserved		Valid	Valid
4A	597:592	Matrix OUT	IN0 of 3-bit LUT2 or Clock Input of DFF5	Valid	Valid
	599:598	Reserved		Valid	Valid
4B	605:600	Matrix OUT	IN1 of 3-bit LUT2 or Data Input of DFF5	Valid	Valid
	607:606	Reserved		Valid	Valid
4C	613:608	Matrix OUT	IN2 of 3-bit LUT2 or nRST (nSET) of DFF5	Valid	Valid
	615:614	Reserved		Valid	Valid
4D	621:616	Matrix OUT	IN0 of 3-bit LUT3 or Clock Input of DFF6	Valid	Valid
	623:622	Reserved		Valid	Valid
4E	629:624	Matrix OUT	IN1 of 3-bit LUT3 or Data Input of DFF6	Valid	Valid
	631:630	Reserved		Valid	Valid
4F	637:632	Matrix OUT	IN2 of 3-bit LUT3 or nRST (nSET) of DFF6	Valid	Valid
	639:638	Reserved		Valid	Valid
50	645:640	Matrix OUT	IN0 of 3-bit LUT4 or Clock Input of DFF7	Valid	Valid
	647:646	Reserved		Valid	Valid
51	653:648	Matrix OUT	IN1 of 3-bit LUT4 or Data Input of DFF7	Valid	Valid
	655:654	Reserved		Valid	Valid
52	661:656	Matrix OUT	IN2 of 3-bit LUT4 or nRST (nSET) of DFF7	Valid	Valid
	663:662	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
53	669:664	Matrix OUT	IN0 of 3-bit LUT5 or Delay2 Input (or Counter2 RST Input)	Valid	Valid
	671:670	Reserved		Valid	Valid
54	677:672	Matrix OUT	IN1 of 3-bit LUT5 or External Clock Input of Delay2 (or Counter2)	Valid	Valid
	679:678	Reserved		Valid	Valid
55	685:680	Matrix OUT	IN2 of 3-bit LUT5	Valid	Valid
	687:686	Reserved		Valid	Valid
56	693:688	Matrix OUT	IN0 of 3-bit LUT6 or Delay3 Input (or Counter3 RST Input)	Valid	Valid
	695:694	Reserved		Valid	Valid
57	701:696	Matrix OUT	IN1 of 3-bit LUT6 or External Clock Input of Delay3 (or Counter3)	Valid	Valid
	703:702	Reserved		Valid	Valid
58	709:704	Matrix OUT	IN2 of 3-bit LUT6	Valid	Valid
	711:710	Reserved		Valid	Valid
59	717:712	Matrix OUT	IN0 of 3-bit LUT7 or Delay4 Input (or Counter4 RST Input)	Valid	Valid
	719:718	Reserved		Valid	Valid
5A	725:720	Matrix OUT	IN1 of 3-bit LUT7 or External Clock Input of Delay4 (or Counter4)	Valid	Valid
	727:726	Reserved		Valid	Valid
5B	733:728	Matrix OUT	IN2 of 3-bit LUT7	Valid	Valid
	735:734	Reserved		Valid	Valid
5C	741:736	Matrix OUT	IN0 of 3-bit LUT8 or Delay5 Input (or Counter5 RST Input)	Valid	Valid
	743:742	Reserved		Valid	Valid
5D	749:744	Matrix OUT	IN1 of 3-bit LUT8 or External Clock Input of Delay5 (or Counter5)	Valid	Valid
	751:750	Reserved		Valid	Valid
5E	757:752	Matrix OUT	IN2 of 3-bit LUT8	Valid	Valid
	759:758	Reserved		Valid	Valid
5F	765:760	Matrix OUT	IN0 of 3-bit LUT9 or Delay6 Input (or Counter6 RST Input)	Valid	Valid
	767:766	Reserved		Valid	Valid
60	773:768	Matrix OUT	IN1 of 3-bit LUT9 or External Clock Input of Delay6 (or Counter6)	Valid	Valid
	775:774	Reserved		Valid	Valid
61	781:776	Matrix OUT	IN2 of 3-bit LUT9	Valid	Valid
	783:782	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
62	789:784	Matrix OUT	IN0 of 3-bit LUT10 or Input of Pipe Delay	Valid	Valid
	791:790	Reserved		Valid	Valid
63	797:792	Matrix OUT	IN1 of 3-bit LUT10 or nRST of Pipe Delay	Valid	Valid
	799:798	Reserved		Valid	Valid
64	805:800	Matrix OUT	IN2 of 3-bit LUT10 or Clock of Pipe Delay	Valid	Valid
	807:806	Reserved		Valid	Valid
65	813:808	Matrix OUT	IN0 of 4-bit LUT0 or Delay0 Input (or Counter0 RST/SET Input)	Valid	Valid
	815:814	Reserved		Valid	Valid
66	821:816	Matrix OUT	IN1 of 4-bit LUT0 or External Clock Input of Delay0 (or Counter0)	Valid	Valid
	823:822	Reserved		Valid	Valid
67	829:824	Matrix OUT	IN2 of 4-bit LUT0 or UP Input of FSM0	Valid	Valid
	831:830	Reserved		Valid	Valid
68	837:832	Matrix OUT	IN3 of 4-bit LUT0 or KEEP Input of FSM0	Valid	Valid
	839:838	Reserved		Valid	Valid
69	845:840	Matrix OUT	IN0 of 4-bit LUT1 or Delay1 Input (or Counter1 RST/SET Input)	Valid	Valid
	847:846	Reserved		Valid	Valid
6A	853:848	Matrix OUT	IN1 of 4-bit LUT1 or External Clock Input of Delay1 (or Counter1)	Valid	Valid
	855:854	Reserved		Valid	Valid
6B	861:856	Matrix OUT	IN2 of 4-bit LUT1 or UP Input of FSM1	Valid	Valid
	863:862	Reserved		Valid	Valid
6C	869:864	Matrix OUT	IN3 of 4-bit LUT1 or KEEP Input of FSM1	Valid	Valid
	871:870	Reserved		Valid	Valid
6D	877:872	Reserved		Valid	Valid
	879:878	Reserved		Valid	Valid
6E	887:880	Reserved		Invalid	Invalid
6F	895:888	Reserved		Invalid	Invalid
70	903:896	Reserved		Invalid	Invalid
71	911:904	Reserved		Invalid	Invalid
72	919:912	Reserved		Invalid	Invalid
73	927:920	Reserved		Invalid	Invalid
74	935:928	Reserved		Invalid	Invalid
75	943:936	Reserved		Invalid	Invalid
76	951:944	Reserved		Invalid	Invalid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
77	959:952	Reserved		Invalid	Invalid
78	967:960	Reserved		Invalid	Invalid
79	975:968	Reserved		Invalid	Invalid
7A	983:976	Reserved		Invalid	Invalid
7B	991:984	Reserved		Invalid	Invalid
7C	999:992	Reserved		Invalid	Invalid
7D	1007:1000	Reserved		Invalid	Invalid
7E	1015:1008	Reserved		Invalid	Invalid
7F	1023:1016	Reserved		Invalid	Invalid
PIN 2					
80	1024	Reserved		Valid	Valid
	1025	Reserved		Valid	Valid
	1027:1026	Reserved		Valid	Valid
	1029:1028	PIN2 Pull-Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1031:1030	PIN2 Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
Reserved					
81	1032	Reserved		Valid	Valid
	1033	Reserved		Valid	Valid
	1035:1034	Reserved		Valid	Valid
	1037:1036	Reserved		Valid	Valid
	1039:1038	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
PIN 3					
82	1040	Reserved		Valid	Valid
	1041	PIN3 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1042	PIN3 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1044:1043	PIN3 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1047:1045	PIN3 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved	Valid	Valid
Reserved					
83	1048	Reserved		Valid	Valid
	1049	Reserved		Valid	Valid
	1051:1050	Reserved		Valid	Valid
	1053:1052	Reserved		Valid	Valid
	1055:1054	Reserved		Valid	Valid
PIN 4					
84	1056	Reserved		Valid	Valid
	1057	PIN4 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1058	PIN4 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1060:1059	PIN4 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1063:1061	PIN4 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input and Open-Drain	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
PIN 5					
85	1064	Reserved		Valid	Valid
	1065	PIN5 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1067:1066	PIN5 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1069:1068	PIN5 Mode Control (sig_pin5_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1071:1070	PIN5 Mode Control (sig_pin5_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
PIN 6					
86	1072	Reserved		Valid	Valid
	1073	IO6 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1074	Select SCL and Virtual Input 0 or PIN6	0: SCL and Virtual Input 0 1: PIN6	Valid	Valid
	1076:1075	PIN6 Pull-Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1079:1077	PIN6 (or SCL) Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Reserved 101: Open-Drain NMOS 110: Reserved 111: Reserved	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
PIN 7					
87	1080	Reserved		Valid	Valid
	1081	PIN7 (or SDA) Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1082	Select SDA and Virtual Input 1 or PIN7	0: SDA and Virtual Input 1 1: PIN7	Valid	Valid
	1084:1083	PIN7 Pull-Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1087:1085	PIN7 (or SDA) Mode Control (input mode is selected by register at SDA, output mode is fixed as OD at SDA)	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Reserved 101: Open-Drain NMOS 110: Reserved 111: Reserved	Valid	Valid
PIN 8					
88	1088	PIN8 4x Drive (4x, NMOS Open-Drain) Selection	0: 4x Drive OFF 1: 4x Drive ON (if sig_pin8_oe = '1' and PIN8 Mode Control = '1X')	Valid	Valid
	1089	PIN8 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1091:1090	PIN8 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1093:1092	PIN8 Mode Control (sig_pin8_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1095:1094	PIN8 Mode Control (sig_pin8_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
PIN 10					
89	1096	PIN10 4x Drive (4x, NMOS Open-Drain) Selection	0: 4x Drive OFF (Default) 1: 4x Drive ON (if PIN10 Mode Control = '101')	Valid	Valid
	1097	PIN10 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1098	PIN10 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1100:1099	PIN10 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1103:1101	PIN10 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input and Open-Drain	Valid	Valid
Reserved					
8A	1104	Reserved		Valid	Valid
	1105	Reserved		Valid	Valid
	1107:1106	Reserved		Valid	Valid
	1109:1108	Reserved		Valid	Valid
	1111:1110	Reserved		Valid	Valid
Reserved					
8B	1112	Reserved		Valid	Valid
	1113	Reserved		Valid	Valid
	1115:1114	Reserved		Valid	Valid
	1117:1116	Reserved		Valid	Valid
	1119:1118	Reserved		Valid	Valid
Reserved					
8C	1120	Reserved		Valid	Valid
	1121	Reserved		Valid	Valid
	1122	Reserved		Valid	Valid
	1124:1123	Reserved		Valid	Valid
	1127:1125	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
PIN 12					
8D	1128	Reserved		Valid	Valid
	1129	PIN12 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1131:1130	PIN12 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1133:1132	PIN12 Mode Control (sig_pin12_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
	1135:1134	PIN12 Mode Control (sig_pin12_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
PIN 13					
8E	1136	Reserved		Valid	Valid
	1137	PIN13 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1138	PIN13 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1140:1139	PIN13 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1143:1141	PIN13 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved	Valid	Valid
Reserved					
8F	1144	Reserved		Valid	Valid
	1145	Reserved		Valid	Valid
	1147:1146	Reserved		Valid	Valid
	1149:1148	Reserved		Valid	Valid
	1151:1150	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Reserved					
90	1152	Reserved		Valid	Valid
	1153	Reserved		Valid	Valid
	1155:1154	Reserved		Valid	Valid
	1157:1156	Reserved		Valid	Valid
	1159:1158	Reserved		Valid	Valid
PIN 14					
91	1160	Reserved		Valid	Valid
	1161	PIN14 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1162	PIN14 Pull-Up/Down Resistor Selection	0: Pull-Down Resistor 1: Pull-Up Resistor	Valid	Valid
	1164:1163	PIN14 Pull-Up/Down Resistor Value Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M	Valid	Valid
	1167:1165	PIN14 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved	Valid	Valid
ACMP1					
92	1168	ACMP1 Positive Input Source Select	0: IO8 1: ACMP0 IN+ source	Valid	Valid
	1169	ACMP1 Analog Buffer Enable (Max. BW 1 MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
	1171:1170	ACMP1 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
ACMP0					
92	1172	ACMP0 Positive Input Source Select	0: IO4 1: V_{DD}	Valid	Valid
	1173	ACMP0 Analog Buffer Enable (Max. BW 1 MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
	1175:1174	ACMP0 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV (01: for both external and internal V_{REF}; 10 and 11: for only internal V_{REF}; External V_{REF} will not have 50 mV and 200 mV hysteresis)	Valid	Valid
Reserved					
93	1177:1176	Reserved		Valid	Valid
	1179:1178	Reserved		Valid	Valid
ACMP2					
93	1180	Reserved		Valid	Valid
	1182:1181	ACMP2 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV	Valid	Valid
ACMP1 100 µA Current Source Enable					
93	1183	ACMP1 100 µA Current Source Enable	0: Disable 1: Enable	Valid	Valid
3-bit LUTx Function Select					
94	1184	3-bit LUT3 or DFF6 with nRST/nSET Select	0: 3-bit LUT3 1: DFF6 with nRST/nSET	Valid	Valid
	1185	3-bit LUT2 or DFF5 with nRST/nSET Select	0: 3-bit LUT2 1: DFF5 with nRST/nSET	Valid	Valid
	1186	3-bit LUT1 or DFF4 with nRST/nSET Select	0: 3-bit LUT1 1: DFF4 with nRST/nSET	Valid	Valid
	1187	3-bit LUT0 or DFF3 with nRST/nSET Select (Two consecutive DFFs if register [1471] = 1 for SM)	0: 3-bit LUT0 1: DFF3 with nRST/nSET	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
2-bit LUTx Function Select					
94	1188	2-bit LUT3 or PGen Select	0: 2-bit LUT3 1: PGen	Valid	Valid
	1189	2-bit LUT2 or DFF2 Select	0: 2-bit LUT2 1: DFF2	Valid	Valid
	1190	2-bit LUT1 or DFF1 Select	0: 2-bit LUT1 1: DFF1	Valid	Valid
	1191	2-bit LUT0 or DFF0 Select	0: 2-bit LUT0 1: DFF0	Valid	Valid
4-bit LUTx Function Select					
95	1192	4-bit LUT1 or DLY/CNT1(16bits) Select	0: 4-bit LUT1 1: DLY/CNT1(16bits)	Valid	Valid
	1193	4-bit LUT0 or DLY/CNT0 (16bits) Select	0: 4-bit LUT0 1: DLY/CNT0(16bits)	Valid	Valid
3-bit LUTx Function Select					
95	1194	3-bit LUT9 or DLY/CNT6(8bits) Select	0: 3-bit LUT9 1: DLY/CNT6(8bits)	Valid	Valid
	1195	3-bit LUT8 or DLY/CNT5(8bits) Select	0: 3-bit LUT8 1: DLY/CNT5(8bits)	Valid	Valid
	1196	3-bit LUT7 or DLY/CNT4(8bits) Select	0: 3-bit LUT7 1: DLY/CNT4(8bits)	Valid	Valid
	1197	3-bit LUT6 or DLY/CNT3(8bits) Select	0: 3-bit LUT6 1: DLY/CNT3(8bits)	Valid	Valid
	1198	3-bit LUT5 or DLY/CNT2(8bits) Select	0: 3-bit LUT5 1: DLY/CNT2(8bits)	Valid	Valid
	1199	3-bit LUT4 or DFF7 with nRST/nSET Select	0: 3-bit LUT4 1: DFF7 with nRST/nSET	Valid	Valid
2-bit LUT1/DFF1					
96	1200	2-bit LUT1 [0]		Valid	Valid
	1201	2-bit LUT1 [1]/DFF1 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1202	2-bit LUT1 [2]/DFF1 Output Select	0: Q output 1: nQ output	Valid	Valid
	1203	2-bit LUT1 [3]/DFF1 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
2-bit LUT0/DFF0					
96	1204	2-bit LUT0 [0]		Valid	Valid
	1205	2-bit LUT0 [1]/DFF0 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1206	2-bit LUT0 [2]/DFF0 Output Select	0: Q output 1: nQ output	Valid	Valid
	1207	2-bit LUT0 [3]/DFF0 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
2-bit LUT3/PGen					
97	1211:1208	2-bit LUT3 [3:0] or PGen 4bit counter data [3:0]		Valid	Valid
2-bit LUT2/DFF2					
97	1212	2-bit LUT2 [0]		Valid	Valid
	1213	2-bit LUT2 [1]/DFF2 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1214	2-bit LUT2 [2]/DFF2 Output Select	0: Q output 1: nQ output	Valid	Valid
	1215	2-bit LUT2 [3]/DFF2 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
3-bit LUT0/DFF3					
98	1219:1216	3-bit LUT0 [3:0]		Valid	Valid
	1220	3-bit LUT0 [4]/DFF3 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1221	3-bit LUT0 [5]/DFF3 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1222	3-bit LUT0 [6]/DFF3 Output Select	0: Q output 1: nQ output	Valid	Valid
	1223	3-bit LUT0 [7]/DFF3 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
3-bit LUT1/DFF4					
99	1227:1224	3-bit LUT1 [3:0]		Valid	Valid
	1228	3-bit LUT1 [4]/DFF4 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1229	3-bit LUT1 [5]/DFF4 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1230	3-bit LUT1 [6]/DFF4 Output Select	0: Q output 1: nQ output	Valid	Valid
	1231	3-bit LUT1 [7]/DFF4 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
3-bit LUT2/DFF5					
9A	1235:1232	3-bit LUT2 [3:0]		Valid	Valid
	1236	3-bit LUT2 [4]/DFF5 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1237	3-bit LUT2 [5]/DFF5 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1238	3-bit LUT2 [6]/DFF5 Output Select	0: Q output 1: nQ output	Valid	Valid
	1239	3-bit LUT2 [7]/DFF5 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
3-bit LUT3/DFF6					
9B	1243:1240	3-bit LUT3 [3:0]		Valid	Valid
	1244	3-bit LUT3 [4]/DFF6 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1245	3-bit LUT3 [5]/DFF6 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1246	3-bit LUT3 [6]/DFF6 Output Select	0: Q output 1: nQ output	Valid	Valid
	1247	3-bit LUT3 [7]/DFF6 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
3-bit LUT4/DFF7					
9C	1251:1248	3-bit LUT4 [3:0]		Valid	Valid
	1252	3-bit LUT4 [4]/DFF7 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1253	3-bit LUT4 [5]/DFF7 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1254	3-bit LUT4 [6]/DFF7 Output Select	0: Q output 1: nQ output	Valid	Valid
	1255	3-bit LUT4 [7]/DFF7 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
3-bit LUT10/Pipe Delay					
9D	1259:1256	3-bit LUT10 [3:0]/Pipe Delay OUT0 Select		Valid	Valid
	1263:1260	3-bit LUT10 [7:4]/Pipe Delay OUT1 Select		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
9E	1265:1264	Select the Edge Mode of Programmable Delay and Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay	Valid	Valid
	1267:1266	Delay Value Select for Programmable Delay and Edge Detector (V_{DD} = 3.3 V, typical)	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns	Valid	Valid
	1269:1268	Reserved		Valid	Valid
	1270	3-bit LUT10 or Pipe Delay Select	0: 3-bit LUT10 1: Pipe Delay	Valid	Valid
	1271	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted	Valid	Valid
DLY/CNT2					
9F	1273:1272	DLY2 Mode Select or Asynchronous CNT2 Reset	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1276:1274	DLY/CNT2 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter1 Overflow	Valid	Valid
	1277	DLY/CNT2 Output Selection if DLY/CNT2 Mode Selection is "11"	0: Default Output 1: Edge Detector Output	Valid	Valid
	1279:1278	DLY/CNT2 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT3					
A0	1281:1280	DLY3 Mode Select or Asynchronous CNT3 Reset	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1284:1282	DLY/CNT3 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter2 Overflow	Valid	Valid
	1285	DLY/CNT3 Output Selection if DLY/CNT3 Mode Selection is "11"	0: Default Output 1: Edge Detector Output	Valid	Valid
	1287:1286	DLY/CNT3 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT4					
A1	1289:1288	DLY4 Mode Select or Asynchronous CNT4 Reset	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1292:1290	DLY/CNT4 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter3 Overflow	Valid	Valid
	1293	DLY/CNT4 Output Selection if DLY/CNT4 Mode Selection is "11"	0: Default Output 1: Edge Detector Output	Valid	Valid
	1295:1294	DLY/CNT4 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT5					
A2	1297:1296	DLY5 Mode Select or Asynchronous CNT5 Reset	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1300:1298	DLY/CNT5 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter4 Overflow	Valid	Valid
	1301	DLY/CNT5 Output Selection if DLY/CNT5 Mode Selection is "11"	0: Default Output 1: Edge Detector Output	Valid	Valid
	1303:1302	DLY/CNT5 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT6					
A3	1305:1304	DLY6 Mode Select or Asynchronous CNT6 Reset	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1308:1306	DLY/CNT6 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12, 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter5 Overflow	Valid	Valid
	1309	DLY/CNT6 Output Selection if DLY/CNT6 Mode Selection is "11"	0: Default Output 1: Edge Detector Output	Valid	Valid
	1311:1310	DLY/CNT6 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT0					
A4	1313:1312	DLY0 Mode Select or Asynchronous CNT0 Reset (16bits)	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset or Set	Valid	Valid
	1316:1314	DLY/CNT0 Clock Source Select (16bits)	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter6 Overflow	Valid	Valid
	1317	CNT0/FSM0's Q are Set to data or Reset to 0s Selection (16bits)	0: Reset to 0s 1: Set to data (Registers [1583:1576, 1591:1584])	Valid	Valid
	1319:1318	DLY/CNT0 Mode Selection (16bits)	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT1					
A5	1321:1320	DLY1 Mode Select or Asynchronous CNT1 Reset (16bits)	00: On both Falling and Rising Edges (for Delay and Counter Reset) 01: on Falling Edge only (for Delay and Counter Reset) 10: on Rising Edge only (for Delay and Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset or Set	Valid	Valid
	1324:1322	DLY/CNT1 Clock Source Select (16bits)	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter0 Overflow	Valid	Valid
	1325	CNT1/FSM1's Q are Set to data or Reset to 0s Selection (16bits)	0: Reset to 0s 1: Set to data (Registers [1599:1592, 1607:1600])	Valid	Valid
	1327:1326	DLY/CNT1 Mode Selection (16bits)	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNTx One-Shot/Freq. Detect Output Polarity					
A6	1328	DLY/CNT0 stop and restarting enable in CNT mode when new data is loaded	0: Disable 1: Enable	Valid	Valid
	1329	Select the Polarity of DLY/CNT6's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1330	Select the Polarity of DLY/CNT5's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1331	Select the Polarity of DLY/CNT4's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1332	Select the Polarity of DLY/CNT3's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1333	Select the Polarity of DLY/CNT2's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1334	Select the Polarity of DLY/CNT1's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1335	Select the Polarity of DLY/CNT0's One Shot/Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Oscillator					
A7	1337:1336	OSC Clock Pre-divider for 25 MHz	00: Div1 01: Div2 10: Div4 11: Div8	Valid	Valid
	1338	OSC Fast Start-Up Enable for 25 kHz/2 MHz	0: Disable 1: Enable	Valid	Valid
	1340:1339	OSC Clock Pre-divider for 25 kHz/2 MHz	00: Div1 01: Div2 10: Div4 11: Div8	Valid	Valid
	1341	Force 25 MHz Oscillator ON	0: Auto Power-On (If any CNT/DLY use 25 MHz source) 1: Force Power-On	Valid	Valid
	1342	Oscillator (25 kHz/2 MHz OSC) Select	0: 25 kHz OSC 1: 2 MHz OSC	Valid	Valid
	1343	Force 25 kHz/2 MHz Oscillator ON	0: Auto Power-On (if any CNT/DLY use 25k/2 MHz source) 1: Force Power-On	Valid	Valid
A8	1346:1344	Internal OSC 25 kHz/2 MHz Frequency Divider Control for matrix input [28]	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
	1349:1347	Internal OSC 25 kHz/2 MHz Frequency Divider Control for matrix input [27]	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
	1350	OSC Clock 25 kHz/2 MHz to matrix input [28] enable	0: Disable 1: Enable	Valid	Valid
	1351	OSC Clock 25 kHz/2 MHz to matrix input [27] enable	0: Disable 1: Enable	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A9	1354:1352	SM_reg_init [2:0] for SM state default setup bits		Valid	Valid
	1355	Reserved		Valid	Valid
	1356	OSC Clock 25 MHz to matrix input [29] enable	0: Disable 1: Enable	Valid	Valid
	1357	External Clock Source Select instead of 25 MHz	0: Internal Oscillator 1: External Clock from Pin13	Valid	Valid
	1358	External Clock Source Select instead of 25 kHz/2 MHz	0: Internal Oscillator 1: External Clock from Pin14	Valid	Valid
	1359	DLY/CNT1 stop and restarting enable in CNT mode when new data is loaded	0: Disable 1: Enable	Valid	Valid
ASM 8-to-1 MUX's 3 Selection Bits					
AA	1362:1360	ASM_state0_dec8x1_EN1		Valid	Valid
	1363	Reserved		Valid	Valid
	1366:1364	ASM_state0_dec8x1_EN0		Valid	Valid
	1367	Reserved		Valid	Valid
AB	1370:1368	ASM_state1_dec8x1_EN0		Valid	Valid
	1371	Reserved		Valid	Valid
	1374:1372	ASM_state0_dec8x1_EN2		Valid	Valid
	1375	Reserved		Valid	Valid
AC	1378:1376	ASM_state1_dec8x1_EN2		Valid	Valid
	1379	Reserved		Valid	Valid
	1382:1380	ASM_state1_dec8x1_EN1		Valid	Valid
	1383	Reserved		Valid	Valid
AD	1386:1384	ASM_state2_dec8x1_EN1		Valid	Valid
	1387	Reserved		Valid	Valid
	1390:1388	ASM_state2_dec8x1_EN0		Valid	Valid
	1391	Reserved		Valid	Valid
AE	1394:1392	ASM_state3_dec8x1_EN0		Valid	Valid
	1395	Reserved		Valid	Valid
	1398:1396	ASM_state2_dec8x1_EN2		Valid	Valid
	1399	Reserved		Valid	Valid
AF	1402:1400	ASM_state3_dec8x1_EN2		Valid	Valid
	1403	Reserved		Valid	Valid
	1406:1404	ASM_state3_dec8x1_EN1		Valid	Valid
	1407	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B0	1410:1408	ASM_state4_dec8x1_EN1		Valid	Valid
	1411	Reserved		Valid	Valid
	1414:1412	ASM_state4_dec8x1_EN0		Valid	Valid
	1415	Reserved		Valid	Valid
B1	1418:1416	ASM_state5_dec8x1_EN0		Valid	Valid
	1419	Reserved		Valid	Valid
	1422:1420	ASM_state4_dec8x1_EN2		Valid	Valid
	1423	Reserved		Valid	Valid
B2	1426:1424	ASM_state5_dec8x1_EN2		Valid	Valid
	1427	Reserved		Valid	Valid
	1430:1428	ASM_state5_dec8x1_EN1		Valid	Valid
	1431	Reserved		Valid	Valid
B3	1434:1432	ASM_state6_dec8x1_EN1		Valid	Valid
	1435	Reserved		Valid	Valid
	1438:1436	ASM_state6_dec8x1_EN0		Valid	Valid
	1439	Reserved		Valid	Valid
B4	1442:1440	ASM_state7_dec8x1_EN0		Valid	Valid
	1443	Reserved		Valid	Valid
	1446:1444	ASM_state6_dec8x1_EN2		Valid	Valid
	1447	Reserved		Valid	Valid
B5	1450:1448	ASM_state7_dec8x1_EN2		Valid	Valid
	1451	Reserved		Valid	Valid
	1454:1452	ASM_state7_dec8x1_EN1		Valid	Valid
	1455	Reserved		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Filter/Edge Detector					
B6	1457:1456	Select the edge mode of Edge Detector_1	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
	1458	Filter_1/Edge Detector_1 output Polarity Select	0: Filter_1 output 1: Filter_1 output inverted	Valid	Valid
	1459	Filter_1 or Edge Detector_1 Select (Typ. 30 ns at V_{DD} = 3.3 V)	0: Filter_1 1: Edge Detector_1	Valid	Valid
	1461:1460	Select the edge mode of Edge Detector_0	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
	1462	Filter_0/Edge Detector_0 output Polarity Select	0: Filter_0 output 1: Filter_0 output inverted	Valid	Valid
	1463	Filter_0 or Edge Detector_0 Select (Typ. 47 ns at V_{DD} = 3.3 V)	0: Filter_0 1: Edge Detector_0	Valid	Valid
V_{REF}/Bandgap					
B7	1464	Reserved		Valid	Valid
	1466:1465	Bandgap OK for ACMP Output Delay Time Select, the start Time is "nRST_core go to High"	00 or 10 with registers [1474:1472] = 100 (WideV_{DD} range,1.7 V~5.5 V): Auto-delay mode, 550 µs for V_{DD} < 2.7 V and 100 µs for 2.7 V < V_{DD} 00 or 10 with registers [1474:1472] = X10: Always 100 µs delay for 2.7 V < V_{DD} 00 or 10 with registers [1474:1472] = XX1: Always 550 µs delay for V_{DD} < 2.7 V, 01: Always 550 µs delay regardless of registers [1474:1472] and V_{DD}, 11: Always 100 µs delay with 2.7 V < V_{DD} regardless of registers [1474:1472]	Valid	Valid
	1467	Reserved		Valid	Valid
	1468	Reserved		Valid	Valid
	1469	Reserved		Valid	Valid
	1470	Reserved		Valid	Valid
	1471	Two consecutive DFFs enable for SM	0: Disable 1: Enable	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B8	1474:1472	Power divider (V_{DD}/3, V_{DD}/4) ON/OFF	0XX: Power divider off (if there is no use of V_{DD}/3, V_{DD}/4 at ACMP negative in) 100: Reserved X10: Reserved XX1: Reserved	Valid	Valid
	1475	V_{DD} Bypass Enable when device power is 1.8 V	0: Regulator Auto ON 1: Regulator OFF (V_{DD} Bypass)	Valid	Valid
	1476	Force Bandgap ON	0: Auto-Mode 1: Enable (if chip is Power-Down, the Bandgap will Power-Down even if it is Set to 1)	Valid	Valid
B8	1477	NVM Power-Down	0: None (Or Programming Enable) 1: Power-Down (Or Programming Disable)	Valid	Valid
	1478	Reserved		Valid	Valid
	1479	GPIO Quick Charge Enable	0: Disable 1: Enable	Valid	Valid
B9	1482:1480	Reserved		Valid	Valid
	1483	Reserved		Valid	Valid
	1486:1484	Reserved		Valid	Valid
	1487	Reserved		Valid	Valid
BA	1488	Reserved		Valid	Valid
	1489	Wake time Selection in Wake Sleep Mode	0: short wake time 1: normal wake time	Valid	Valid
	1490	ACMP0 Wake and Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1491	ACMP1 Wake and Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1492	ACMP2 Wake and Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1493	Reserved		Valid	Valid
	1494	Wake Sleep Output State When WS Oscillator is Power-Down if DLY/CNT0 Mode Selection is "11"	0: Low 1: High	Valid	Valid
	1495	Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11"	0: Default Mode 1: Wake Sleep Ratio Control Mode	Valid	Valid
BB	1503:1496	Reserved		Invalid	Invalid
BC	1511:1504	Reserved		Invalid	Invalid
BD	1519:1512	Reserved		Invalid	Invalid
BE	1527:1520	Reserved		Invalid	Invalid
BF	1535:1528	Reserved		Invalid	Invalid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
LUT/DLY/CNT Control Data					
C0	1543:1536	3-bit LUT5 [7:0] or DLY/CNT2 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C1	1551:1544	3-bit LUT6 [7:0] or DLY/CNT3 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C2	1559:1552	3-bit LUT7 [7:0] or DLY/CNT4 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C3	1567:1560	3-bit LUT8 [7:0] or DLY/CNT5 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C4	1575:1568	3-bit LUT9 [7:0] or DLY/CNT6 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C5	1583:1576	4-bit LUT0 [15:0] or DLY/CNT0 (16bits, [15:0] = [1591:1576]) Control Data	1 - 65535 (Delay Time = [Counter Control Data + 2]/Freq)	Valid	Valid
C6	1591:1584			Valid	Valid
C7	1599:1592	4-bit LUT1 [15:0] or DLY/CNT1 (16bits, [15:0] = [1607:1592]) Control Data	1 - 65535 (Delay Time = [Counter Control Data + 2]/Freq)	Valid	Valid
C8	1607:1600			Valid	Valid
C9	1615:1608	PGen pattern data [15:0] = [1623:1608]		Valid	Valid
CA	1623:1616			Valid	Valid
ACMP0					
CB	1628:1624	ACMP0-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: PIN10: EXT_V_{REF} 11011: PIN5: EXT_V_{REF} 11100: PIN10: EXT_$V_{REF}/2$ 11101: PIN5: EXT_$V_{REF}/2$	Valid	Valid
	1630:1629	ACMP0 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1631	ACMP0 Low Bandwidth (MAX: 1 MHz)Enable	0: OFF 1:ON	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I^2C Interface	
Byte	Register Bit			Read	Write
ACMP1					
CC	1636:1632	ACMP1-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: PIN10: EXT_V_{REF} 11011: Reserved 11100: PIN10: EXT_$V_{REF}/2$ 11101: Reserved	Valid	Valid
	1638:1637	ACMP1 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1639	ACMP1 Low Bandwidth (MAX: 1 MHz)Enable	0: OFF 1: ON	Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
ACMP2					
CD	1644:1640	ACMP2-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: PIN10: EXT_V_{REF} 11011: Reserved 11100: PIN10: EXT_$V_{REF}/2$ 11101: Reserved	Valid	Valid
	1646:1645	ACMP2 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1647	ACMP2 Low Bandwidth (MAX: 1 MHz)Enable	0: OFF 1: ON	Valid	Valid
Reserved					
CE	1652:1648	Reserved		Valid	Valid
	1654:1653	Reserved		Valid	Valid
	1655	Reserved		Valid	Valid
Miscellaneous					
CF	1656	Reserved		Valid	Valid
	1657	Switch from “Matrix OUT: OSC 25 MHz PD” to “Matrix OUT: OSC 25 MHz Force On”	0: OSC PD 1: OSC Force On (Matrix Output [59])	Valid	Valid
	1658	Switch from “Matrix OUT: OSC 25 kHz/2 MHz PD” to “Matrix OUT: OSC 25 kHz/2 MHz Force On”	0: OSC PD 1: OSC Force On (Matrix Output [58])	Valid	Valid
	1659	Reserved		Valid	Valid
	1660	Reserved		Valid	Valid
	1661	Reserved		Valid	Valid
	1662	I²C reset bit with reloading NVM into Data register	0: Keep existing condition 1: Reset execution	Valid	Valid
	1663	Reserved		Valid	Valid
D0	1671:1664	RAM 8 outputs for ASM-state0		Valid	Valid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
D1	1679:1672	RAM 8 outputs for ASM-state1		Valid	Valid
D2	1687:1680	RAM 8 outputs for ASM-state2		Valid	Valid
D3	1695:1688	RAM 8 outputs for ASM-state3		Valid	Valid
D4	1703:1696	RAM 8 outputs for ASM-state4		Valid	Valid
D5	1711:1704	RAM 8 outputs for ASM-state5		Valid	Valid
D6	1719:1712	RAM 8 outputs for ASM-state6		Valid	Valid
D7	1727:1720	RAM 8 outputs for ASM-state7		Valid	Valid
D8	1735:1728	User configurable RAM/OTP Byte 0		Valid	Valid
D9	1743:1736	User configurable RAM/OTP Byte 1		Valid	Valid
DA	1751:1744	User configurable RAM/OTP Byte 2		Valid	Valid
DB	1759:1752	User configurable RAM/OTP Byte 3		Valid	Valid
DC	1767:1760	User configurable RAM/OTP Byte 4		Valid	Valid
DD	1775:1768	User configurable RAM/OTP Byte 5		Valid	Valid
DE	1783:1776	User configurable RAM/OTP Byte 6		Valid	Valid
DF	1791:1784	User configurable RAM/OTP Byte 7		Valid	Valid
E0	1799:1792	Reserved		Invalid	Invalid
E1	1807:1800	Reserved		Invalid	Invalid
E2	1815:1808	Reserved		Invalid	Invalid
E3	1823:1816	Reserved		Invalid	Invalid
E4	1831:1824	Reserved		Valid	Valid
E5	1832	I²C lock for read bits [1535:0] (Bank 0/1/2)	0: Disable (Programmed data can be read), 1: Enable (Programmed data cannot be read)	Valid	Invalid
	1833	Reserved		Valid	Invalid
	1835:1834	Reserved		Valid	Invalid
	1839:1836	Reserved		Valid	Invalid
E6	1847:1840	16-bit Pattern ID Byte 0 (From NVM): ID[23:16]		Valid	Valid
E7	1855:1848	Reserved		Valid	Invalid
E8	1863:1856	Reserved		Valid	Invalid
E9	1867:1864	I²C Control Code Bit [3:0]	Value for target address	Valid	Invalid
	1868	Reserved		Valid	Invalid
	1869	Reserved		Valid	Invalid
	1870	I²C lock for write all bits (Bank 0/1/2/3)	0: writable 1: Non-writable	Valid	Valid
	1871	I²C lock for write bits [1535:0] (Bank 0/1/2)	0: writable 1: Non-writable	Valid	Invalid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
EA	1879:1872	CNT4 Counted Value		Valid	Invalid
EB	1887:1880	CNT0 (16bits) = [1895:1880] Counted Value		Valid	Invalid
EC	1895:1888			Valid	Invalid
ED	1903:1896	CNT6 Counted Value		Valid	Invalid
EE	1911:1904	CNT1 (16bits) = [1919:1904] Counted Value		Valid	Invalid
EF	1919:1912			Valid	Invalid
Matrix Input					
F0	1920	Matrix Input 0	GND	Valid	Invalid
	1921	Matrix Input 1	Pin2 Digital Input	Valid	Invalid
	1922	Matrix Input 2	GND	Valid	Invalid
	1923	Matrix Input 3	Pin3 Digital Input	Valid	Invalid
	1924	Matrix Input 4	GND	Valid	Invalid
	1925	Matrix Input 5	Pin4 Digital Input	Valid	Invalid
	1926	Matrix Input 6	Pin5 Digital Input	Valid	Invalid
	1927	Matrix Input 7	PIN8 Digital Input	Valid	Invalid
F1	1928	Matrix Input 8	2-bit LUT0/DFF0 Output	Valid	Invalid
	1929	Matrix Input 9	2-bit LUT1/DFF1 Output	Valid	Invalid
	1930	Matrix Input 10	2-bit LUT2/DFF2 Output	Valid	Invalid
	1931	Matrix Input 11	2-bit LUT3/PGen Output	Valid	Invalid
	1932	Matrix Input 12	3-bit LUT0/DFF3 Output	Valid	Invalid
	1933	Matrix Input 13	3-bit LUT1/DFF4 Output	Valid	Invalid
	1934	Matrix Input 14	3-bit LUT2/DFF5 Output	Valid	Invalid
	1935	Matrix Input 15	3-bit LUT3/DFF6 Output	Valid	Invalid
F2	1936	Matrix Input 16	3-bit LUT4/DFF7 Output	Valid	Invalid
	1937	Matrix Input 17	3-bit LUT5/CNT_DLY2(8bit) Output	Valid	Invalid
	1938	Matrix Input 18	3-bit LUT6/CNT_DLY3(8bit) Output	Valid	Invalid
	1939	Matrix Input 19	3-bit LUT7/CNT_DLY4(8bit) Output	Valid	Invalid
	1940	Matrix Input 20	3-bit LUT8/CNT_DLY5(8bit) Output	Valid	Invalid
	1941	Matrix Input 21	3-bit LUT9/CNT_DLY6(8bit) Output	Valid	Invalid
	1942	Matrix Input 22	4-bit LUT0/CNT_DLY0(16bit) Output	Valid	Invalid
	1943	Matrix Input 23	4-bit LUT1/CNT_DLY1(16bit) Output	Valid	Invalid

Table 39. Register Map (Cont.)

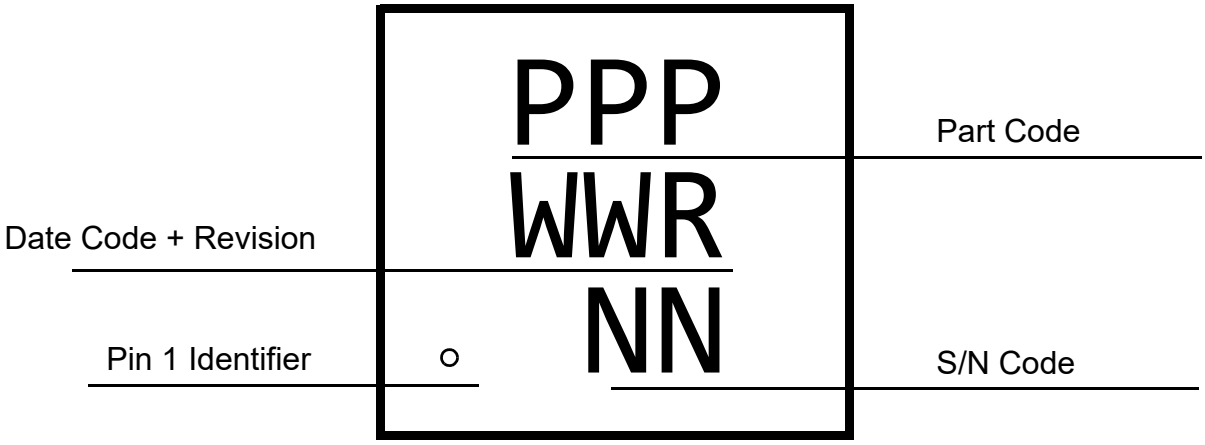
Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
F3	1944	Matrix Input 24	3-bit LUT10/Pipe Delay (1st stage) Output	Valid	Invalid
	1945	Matrix Input 25	Pipe Delay Output0	Valid	Invalid
	1946	Matrix Input 26	Pipe Delay Output1	Valid	Invalid
	1947	Matrix Input 27	Fixed "L" output because it is OSC clock.	Valid	Invalid
	1948	Matrix Input 28	Fixed "L" output because it is OSC clock.	Valid	Invalid
	1949	Matrix Input 29	Fixed "L" output because it is OSC clock.	Valid	Invalid
	1950	Matrix Input 30	Filter0/Edge Detect0 Output	Valid	Invalid
	1951	Matrix Input 31	Filter1/Edge Detect1 Output	Valid	Invalid
F4	1952	Matrix Input 32	Virtual Input [0]	Valid	Valid
	1953	Matrix Input 33	Virtual Input [1]	Valid	Valid
	1954	Matrix Input 34	Virtual Input [2]	Valid	Valid
	1955	Matrix Input 35	Virtual Input [3]	Valid	Valid
	1956	Matrix Input 36	Virtual Input [4]	Valid	Valid
	1957	Matrix Input 37	Virtual Input [5]	Valid	Valid
	1958	Matrix Input 38	Virtual Input [6]	Valid	Valid
	1959	Matrix Input 39	Virtual Input [7]	Valid	Valid
F5	1960	Matrix Input 40	RAM_0 Output for ASM-state	Valid	Invalid
	1961	Matrix Input 41	RAM_1 Output for ASM-state	Valid	Invalid
	1962	Matrix Input 42	RAM_2 Output for ASM-state	Valid	Invalid
	1963	Matrix Input 43	RAM_3 Output for ASM-state	Valid	Invalid
	1964	Matrix Input 44	RAM_4 Output for ASM-state	Valid	Invalid
	1965	Matrix Input 45	RAM_5 Output for ASM-state	Valid	Invalid
	1966	Matrix Input 46	RAM_6 Output for ASM-state	Valid	Invalid
	1967	Matrix Input 47	RAM_7 Output for ASM-state	Valid	Invalid
F6	1968	Matrix Input 48	Pin10 Digital Input	Valid	Invalid
	1969	Matrix Input 49	GND	Valid	Invalid
	1970	Matrix Input 50	Pin11 Digital Input	Valid	Invalid
	1971	Matrix Input 51	GND	Valid	Invalid
	1972	Matrix Input 52	Pin12 Digital Input	Valid	Invalid
	1973	Matrix Input 53	Pin13 Digital Input	Valid	Invalid
	1974	Matrix Input 54	GND	Valid	Invalid
	1975	Matrix Input 55	GND	Valid	Invalid

Table 39. Register Map (Cont.)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
F7	1976	Matrix Input 56	Pin14 Digital Input	Valid	Invalid
	1977	Matrix Input 57	ACMP_0 Output	Valid	Invalid
	1978	Matrix Input 58	ACMP_1 Output	Valid	Invalid
	1979	Matrix Input 59	ACMP_2 Output	Valid	Invalid
	1980	Matrix Input 60	ACMP_3 Output	Valid	Invalid
	1981	Matrix Input 61	Programmable Delay with Edge Detector Output	Valid	Invalid
	1982	Matrix Input 62	nRST_core	Valid	Invalid
	1983	Matrix Input 63	V_{DD}	Valid	Invalid
Reserved					
F8	1991:1984	Reserved		Valid	Invalid
F9	1999:1992	Reserved		Valid	Invalid
FA	2007:2000	Reserved		Valid	Invalid
FB	2015:2008	Reserved		Valid	Valid
FC	2023:2016	Reserved		Valid	Invalid
FD	2031:2024	Reserved		Valid	Invalid
FE	2039:2032	Reserved		Valid	Valid
FF	2047:2040	Reserved		Valid	Valid

18. Package Top Marking Definitions

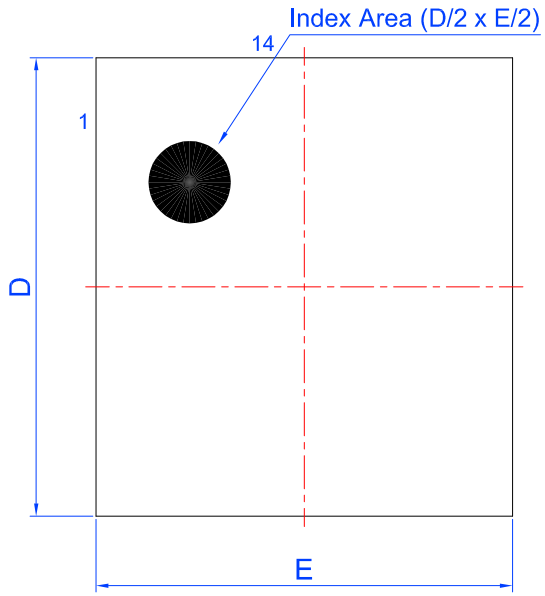
18.1 STQFN 14L 2.0 mm x 2.2 mm 0.4P COL Package



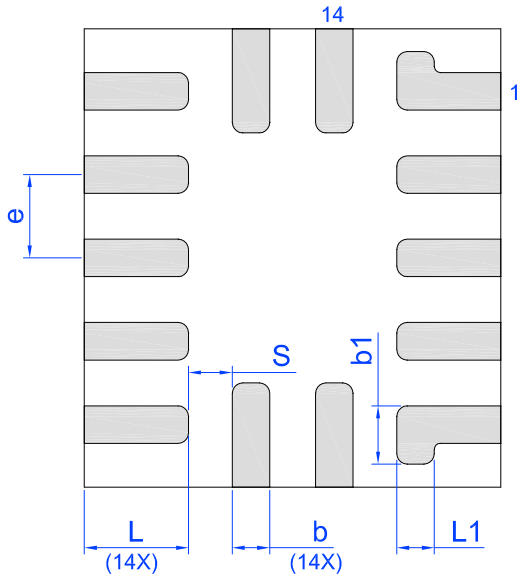
19. Package Information

19.1 Package Outlines for STQFN 14L 2.0 mm x 2.2 mm 0.4P COL Package

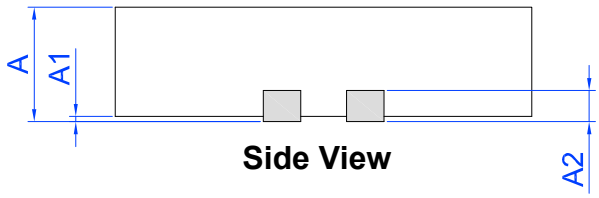
JEDEC MO-220, Variation WECE
IC Net Weight: 0.0068 g



Top View (package face down)



Bottom View



Side View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.15	2.20	2.25
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.45	0.50	0.55
b	0.13	0.18	0.23	S	0.21 TYP		
e	0.40 BSC			b1	0.28 TYP		
				L1	0.18 TYP		

19.2 STQFN Handling

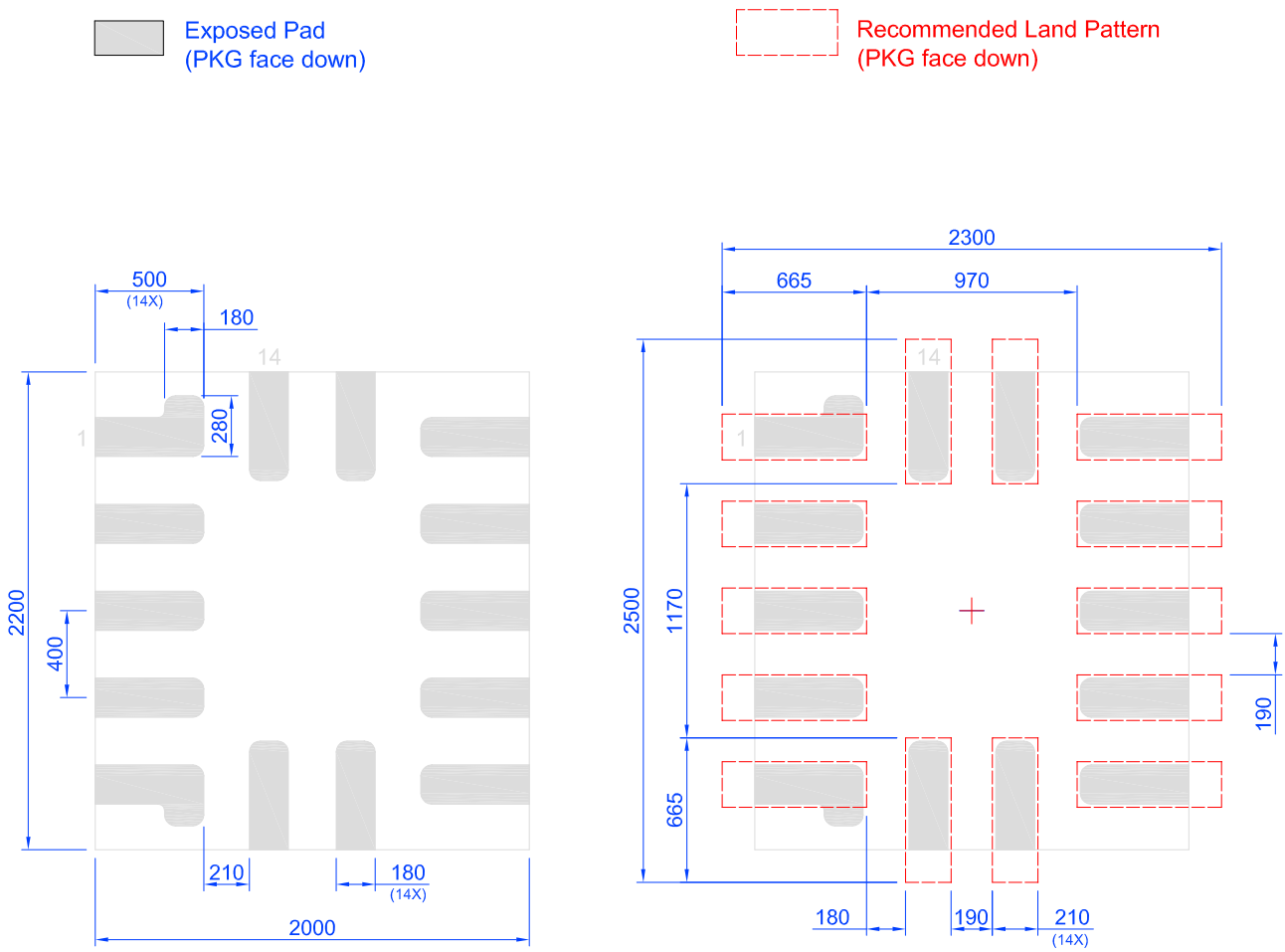
Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

19.3 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.42 mm^3 (nominal) for STQFN 14L Package. More information can be found at http://www.jedec.org.

20. Layout Guidelines

20.1 STQFN-14L 2.0 mm x 2.2 mm 0.4P COL Package



Unit:um

21. Ordering Information

Part Number	Type
SLG46535-EV	14-pin STQFN
SLG46535-EV	14-pin STQFN - Tape and Reel (3k units)

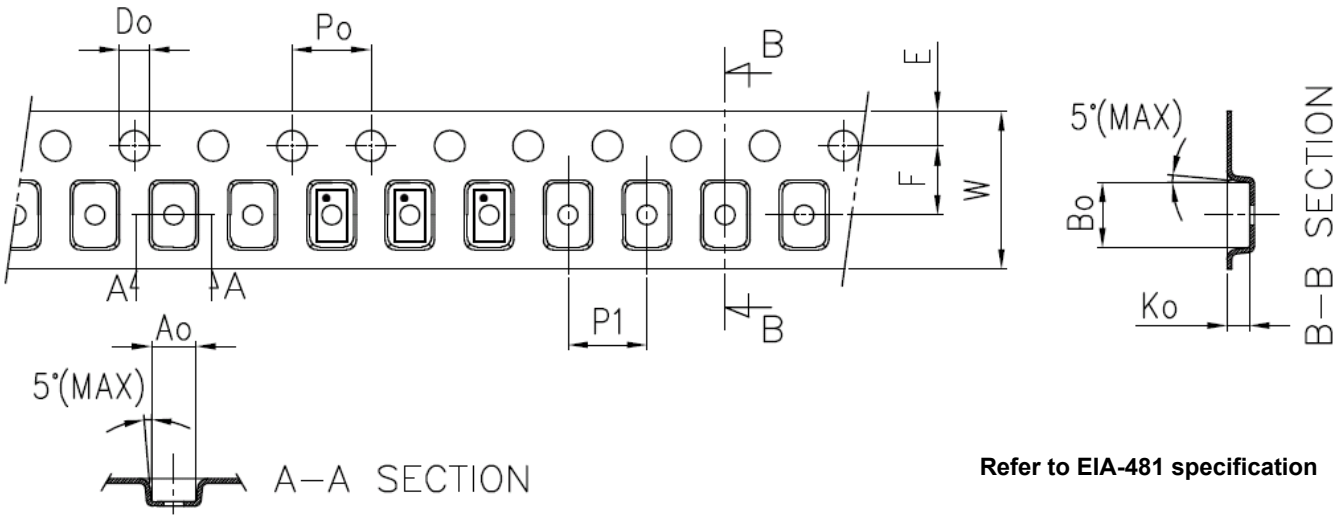
Note: Use SLG46535-EV to order. Shipments are automatically in Tape and Reel.

21.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer (min)		Leader (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 14L 2.0 mm x 2.2 mm 0.4P COL	14	2.0 x 2.2 x 0.55	3,000	3,000	178/60	100	400	100	400	8	4

21.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 2.0 mm x 2.2 mm 0.4P COL	2.2	2.35	0.8	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ASM	Asynchronous State Machine

B

BG	Bandgap

C

CLK	Clock
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic discharge

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LB	Low Bandwidth
LSB	Least Significant Bit
LUT	Look Up Table

M

MSB	Most Significant Bit
MUX	Multiplexer

N

nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output

V

V_{REF}	Voltage Reference

W

WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
1.01	Feb 14, 2025	Corrected cross-reference to figure 25 kHz/2 MHz OSC0 Block Diagram in subsections 25 kHz/2 MHz and 25 MHz Oscillators and Pin 20 or Pin 18 Source for 25 kHz/2 MHz Clock
1.00	Jan 30, 2025	Initial release

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