

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

### General Description

SLG51000 contains seven compact and customizable low dropout regulators and is designed for high performance camera modules and other small multi-rail applications.

Two integrated LDOs are optimized to meet the requirements of high-performance analog circuits. They provide very low output voltage noise characteristics of 13  $\mu\text{V}$  (rms) in addition to high PSRR of 81 dB at 1 MHz and tight output voltage accuracy of  $\pm 1\%$  over temperature.

Two LDOs can be configured to operate as load switches which are optimized to meet the requirements of low  $R_{\text{ON}}$ . By using efficient DC-DC switching regulators upstream in conjunction with SLG51000's linear regulators and load switches downstream, applications can leverage the best characteristics of each to simultaneously achieve low power, low noise, and low voltage dropout, respectively.

Built-in safety protection such as under-voltage lockout, over-temperature protection, and current limit ensures that the ICs are operating under nominal conditions. SLG51000 has an I<sup>2</sup>C-compatible interface for flexible power control. SLG51000 is available in a small 20-pin WLCSP package with a wide ambient operating temperature range of -40 °C to 85 °C.

### Key Features

- Input voltage range:
  - 2.8 V to 5.0 V (2 x HP LDO)
  - 1.7 V to 5.0 V (3 x HV LDO)
  - 0.8 V to 1.5 V (2 x LV LDO)
  - 0.5 V to 1.25 V (2 x load switch)
- Separate input supply and enable pins for flexible power configurations
- Output voltage range:
  - 2.4 V to 3.3 V (2 x HP LDO)
  - 1.2 V to 3.75 V (3 x HV LDO)
  - 0.5 V to 1.2 V (2 x LV LDO)
- Output current levels:
  - Up to 475 mA (2 x HP LDO)
  - Up to 500 mA (3 x HV LDO)
  - Up to 800 mA (2 x LV LDO)
  - Up to 800 mA (2 x load switch)
- High PSRR of 102 dB at 1 kHz and 81 dB at 1 MHz (2 x HP LDO)
- Ultra-low output voltage noise of 13  $\mu\text{V}$  (2 x HP LDO)
- Low dropout voltage (10 mV per 100 mA of load) for high current LDO supply rails (2 x LV LDO)
- Ultra-low  $R_{\text{ON}}$  load switches with low leakage and slew rate control for low  $V_{\text{IN}}$  supplies
- Tight output voltage accuracy of  $\pm 1\%$  over-temperature
- Low shutdown current of 300 nA
- Low quiescent current of 14  $\mu\text{A}$
- User configurable settings via I<sup>2</sup>C interface and OTP
  - Including output voltage, power sequencing, soft-start timing, and current limit threshold
- Soft start and soft shutdown
- Under-voltage lockout (UVLO)
- Thermal shutdown
- Configurable temperature alerts
- Wide -40 °C to +85 °C operating temperature
- 20-pin WLCSP: 1.675 mm x 2.075 mm x 0.465 mm, 0.4 mm pitch

### Applications

- High End Camera Module Applications
- Smartphones
- Digital Cameras
- Smart Devices with Imaging

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1 Block Diagram

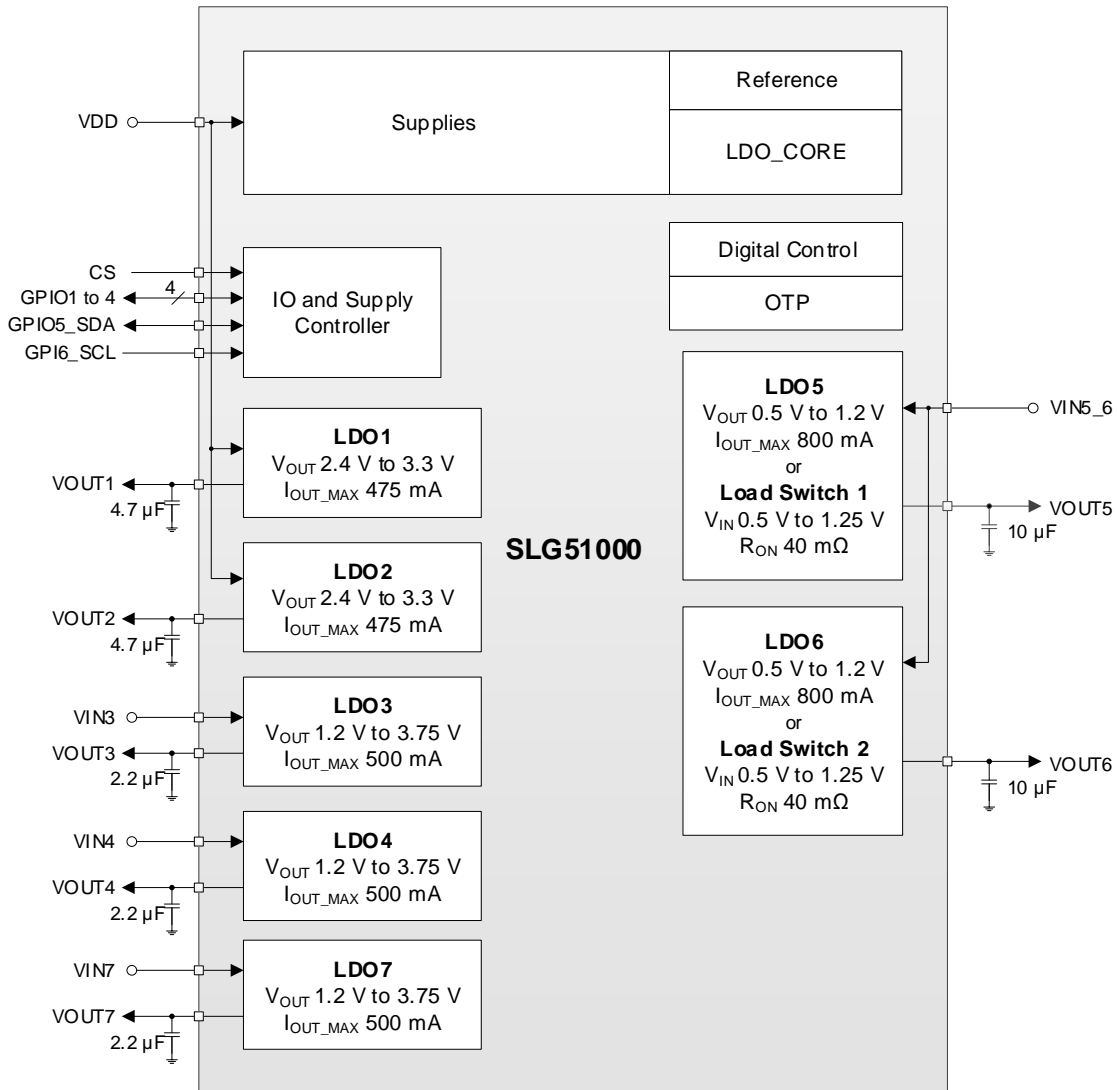


Figure 1: Block Diagram

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## 2 Characteristics

### 2.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 1: Absolute Maximum Ratings**

Parameter	Description	Conditions	Min	Max	Unit
T <sub>STG</sub>	Storage temperature	Non operational	-40	+150	°C
T <sub>J</sub>	Junction temperature		-25	+125	°C
T <sub>A</sub>	Ambient temperature		-40	+85	°C
V <sub>DD</sub>	Power supply voltage on VDD pin		-0.3	+6.0	V
	Power supply voltage on VIN3, VIN4, VIN7 pins		-0.3	+6.0	V
	Power supply voltage on VIN5_6 pin		-0.3	+1.8	V
V <sub>PIN_LV</sub>	Voltage on low-voltage pins	GPIO1 to GPIO5 and GPI6	-0.3	+1.98	V
V <sub>PIN_HV</sub>	Voltage on high-voltage pins	CS	-0.3	V <sub>DD</sub> + 0.3	V
ESD	ESD Protection (Human Body Model)		2000		V
	ESD Protection (Charged Device Model)		500		V

#### 2.1.1 Guidelines for Reliable Operation

- Low Voltage Pins: take care that the low voltage pins (GPIO1 to GPIO5, GPI6, and VIN5\_6) do not exceed their Abs. Max. ratings, even briefly. Transients both positive (above max) and negative (below min) can cause EOS (Electrical Overstress) damage.
- Power sequencing: CS should be held low before VDD is powered up. CS pin should also be pulled low before VDD falls out of operating range. VIN supplies for LDO\_HV and LDO\_LV channels (VIN3, VIN4, VIN7, VIN5\_6) can be safely biased even if VDD is not present. VIN supplies should be powered up before enabling their respective LDO channels. GPIO's configured as inputs are allowed to be forced high before VDD is powered up.

### 2.2 Recommended Operating Conditions

**Table 2: Recommended Operating Conditions**

Parameter	Description	Conditions	Min	Typ	Max	Unit
T <sub>A</sub>	Ambient temperature		-40		+85	°C
V <sub>DD</sub>	Power supply voltage on VDD pin		2.8		5.0	V
	Power supply voltage on VIN3, VIN4, VIN7 pins		1.7		5.0	V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
	Power supply voltage on VIN5_6 pin	LDO Mode	0.8		1.5	V
	Power supply voltage on VIN5_6 pin	Load Switch Mode	0.5		1.25	V
V <sub>PIN_LV</sub>	Voltage on low-voltage pins	GPIO1 to GPIO5 and GPI6	0		1.8	V
V <sub>PIN_HV</sub>	Voltage on high-voltage pins	CS	0		VDD	V

### 2.3 Thermal Characteristics

**Table 3: Package Ratings**

Parameter	Description	Conditions	Min	Typ	Max	Unit
R <sub>θ_JA</sub>	Package thermal resistance	Junction to ambient JEDEC standard PCB		55.3		K/W

### 2.4 Current Consumption

Note: Current consumption electrical characteristics apply over the full operating temperature range.

**Table 4: Current Consumption**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
I <sub>Q_SLEEP</sub>	Current consumption in SLEEP. I <sub>Q_SLEEP</sub> is the I <sub>Q</sub> in LOW IQ RESET State	V <sub>IN</sub> = 3.8 V All references disabled I <sup>2</sup> C interface disabled All rails disabled		0.15	0.65	μA
I <sub>Q_READY_DIS</sub>	Current consumption in READY State	V <sub>IN</sub> = 3.8 V All references enabled I <sup>2</sup> C interface enabled All rails disabled		14	24	μA
I <sub>Q_READY_EN</sub>	Current consumption in READY State	V <sub>IN</sub> = 3.8 V All references enabled I <sup>2</sup> C interface enabled All rails enabled, no load		785	1800	μA
I <sub>Q_OFF_25C</sub>	Quiescent current in OFF Mode	T <sub>A</sub> = 25 °C			1	μA
I <sub>Q_OFF</sub>	Quiescent current in OFF Mode	T <sub>A</sub> = -40 °C to 85 °C			7.6	μA

### 2.5 Chip Select Digital I/O Characteristics

Digital I/O electrical characteristics apply over the full operating temperature range, see Section 2.1.1.

**PMIC with High PSRR, Low Noise, Multi-Output LDOs  
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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
V <sub>IH</sub>	CS input high voltage		0.9		VDD	V
V <sub>IL</sub>	CS input low voltage		0		0.2	V
I <sub>LKG</sub>	CS input leakage current	CS < 2V			1	μA
t <sub>ON_READY</sub>	Turn-on time from CS HIGH to Ready State				10	ms

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### 2.6 1.2 V/1.8 V Digital I/O Characteristics

1.2 V/1.8 V digital I/O electrical characteristics apply over the full operating temperature range, see Section 2.1.1. The voltage thresholds for all I/Os are referenced to VDDIO, where VDDIO can be 1.2 V or 1.8 V. The supply configuration options depend on the I/O, see Section [Error! Reference source not found.](#)

**Table 6: 1.2 V/1.8 V Digital I/O Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
<b>GPIO1 to GPIO4</b>						
V <sub>THR_POS</sub>	Positive going threshold voltage		0.4*V <sub>DDIO</sub>		0.7*V <sub>DDIO</sub>	V
V <sub>THR_NEG</sub>	Negative going threshold voltage		0.3*V <sub>DDIO</sub>		0.6*V <sub>DDIO</sub>	V
V <sub>OL</sub>	Output low voltage	I <sub>OUT</sub> ≤ I <sub>OL</sub>	0		0.3	V
I <sub>OL</sub>	Output current	V <sub>OL</sub> = 0.3 V	2	13		mA
I <sub>LKG</sub>	Input leakage				500	nA
<b>SCL, SDA, GPIO5 and GPI6</b>						
V <sub>THR_POS</sub>	Positive going threshold voltage		0.4*V <sub>DDIO</sub>		0.7*V <sub>DDIO</sub>	V
V <sub>THR_NEG</sub>	Negative going threshold voltage		0.3*V <sub>DDIO</sub>		0.6*V <sub>DDIO</sub>	V
V <sub>HYS</sub>	Schmitt trigger hysteresis		0.1*V <sub>DDIO</sub>			V
V <sub>OL</sub>	Output low voltage SDA, GPIO5	I <sub>OUT</sub> ≤ I <sub>OL</sub>	0		0.3	V
I <sub>OL</sub>	Output current	V <sub>OL</sub> = 0.3 V	20			mA
I <sub>LKG</sub>	Input leakage				500	nA
C <sub>IN</sub>	Pin capacitance				10	pF



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### 2.7 LDO\_HP Characteristics

Table 7: LDO\_HP (LDO1 and 2) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input voltage		2.8		5	V
C <sub>OUT</sub>	Output capacitance	Effective capacitance after derating	2.2	4.7	10	μF
I <sub>OUT_MAX</sub>	Maximum output current	V <sub>IN</sub> = 3.3 V V <sub>OUT</sub> drops 50 mV	475			mA
<b>Programmable Conditions</b>						
V <sub>OUT</sub>	Selectable output voltage		2.4	2.85	3.3	V
V <sub>OUT_LSB</sub>	LSB of output voltage programming DAC (8-bit control)			5		mV
I <sub>OUT_STARTUP_LIM</sub>	Start-up current limit, programmable range <a href="#">Note 1</a>	At 90 % V <sub>OUT</sub>	11	140	240	mA
<b>Electrical Performance</b>						
<b>Static Parameters</b>						
V <sub>OUT_PP</sub>	Part to part output voltage accuracy <a href="#">Note 2</a>	I <sub>OUT</sub> = 1 mA T <sub>A</sub> = 25 °C	-5		5	mV
V <sub>OUT_TEMP</sub>	Temperature dependence of V <sub>OUT</sub> <a href="#">Note 2</a>	I <sub>OUT</sub> = 1 mA	-0.65		0.65	%
V <sub>OUT_STATIC_LINE</sub>	Static line regulation <a href="#">Note 2</a>	I <sub>OUT</sub> = 1 mA V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) to V <sub>IN</sub> (Max)	-2		2	mV
V <sub>OUT_STATIC_LD</sub>	Static load regulation <a href="#">Note 2</a>	1 mA < I <sub>OUT</sub> < 300 mA	-4		2	mV
V <sub>DROPOUT</sub>	Dropout voltage	@ V <sub>OUT</sub> = V <sub>OUT</sub> (V <sub>IN</sub> (Max)) - 10 mV I <sub>OUT</sub> = 300 mA			200	mV
<b>Dynamic Parameters</b>						
V <sub>OUT_TR_LINE</sub>	Line transient response	V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) + 100 mV to V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = 300 mA t <sub>r</sub> = t <sub>f</sub> = 1 μs			0.3	mV

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_TR\_LD\_1}$ mA	Load transient response	$V_{IN} = V_{OUT} + V_{DROPOUT} (Max)$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 1 \text{ mA to } 300 \text{ mA}$ $t_R = t_F = 1 \mu s$			20	mV
$t_{ON}$	Turn-on time	Time to 90 % of $V_{OUT}$ $I_{OUT} = 0 \text{ mA}$		0.15		ms
$t_{OFF}$	Turn-off time	Time to 10 % of $V_{OUT}$ $I_{OUT} = 0 \text{ mA}$			2	ms
<b>AC Parameters</b>						
$PSRR_{1kHz}$	Power supply rejection ratio	$f = 1 \text{ kHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 150 \text{ mA}$ <a href="#">Note 3</a>		102		dB
$PSRR_{100kHz}$	Power supply rejection ratio	$f = 100 \text{ kHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 150 \text{ mA}$ <a href="#">Note 3</a>		87		dB
$PSRR_{1MHz}$	Power supply rejection ratio	$f = 1 \text{ MHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} = 150 \text{ mA}$ <a href="#">Note 3</a>		81		dB
$V_{N\_100kHz}$	Output noise	$f = 10 \text{ Hz to } 100 \text{ kHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} > 30 \text{ mA}$		13		$\mu V$
$V_{N\_1MHz}$	Output noise	$f = 10 \text{ Hz to } 1 \text{ MHz}$ $V_{IN} = 3.2 \text{ V}$ $V_{OUT} = V_{OUT} (Typ)$ $I_{OUT} > 10 \text{ mA}$		21		$\mu V$
<b>Current Limit Accuracy</b>						
$I_{OUT\_FUNC\_LI}$ M	Functional current limit		500			mA
$I_{OUT\_STARTUP}$ $_{LIM\_ACC}$	Start-up current limit accuracy	$I_{OUT\_STARTUP\_LIM} > 11 \text{ mA}$	-50		50	%
$I_{OUT\_STARTUP}$ $_{LIM\_ACC\_11}$	Start-up current limit accuracy	$I_{OUT\_STARTUP\_LIM} = 11 \text{ mA}$	-75		75	%
<b>Quiescent Current Specifications</b>						
$I_{Q\_ON\_0mA}$	Quiescent current	$I_{OUT} = 0 \text{ mA}$			515	$\mu A$

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Parameter	Description	Conditions	Min	Typ	Max	Unit
I <sub>Q_ON_1mA</sub>	Quiescent current	I <sub>OUT</sub> = 1 mA			560	μA
I <sub>Q_ON_300mA</sub>	Quiescent current	I <sub>OUT</sub> = 300 mA			3.2	mA
R <sub>PD_OFF</sub>	Output pull down resistance	V <sub>OUT</sub> = 0.5 V LDO disabled			40	Ω

**Note 1** For programmable selections, refer to Section 4.4.1

**Note 2** The overall accuracy can be calculated by summing V<sub>OUT\_PP</sub> + V<sub>OUT\_TEMP</sub> + V<sub>OUT\_STATIC\_LD</sub> + V<sub>OUT\_STATIC\_LINE</sub>.

**Note 3** For V<sub>IN</sub> - V<sub>OUT</sub> < 350 mV, PSRR will be degraded.

### 2.8 LDO\_HV Characteristics

In the LDO\_HV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for V<sub>DD</sub> above 2.5 V and below 5 V, for V<sub>IN</sub> as defined in the table, and apply over the full operating temperature range, see Section 2.1.1.

**Table 8: LDO\_HV (LDO3, 4, and 7) Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input voltage		1.7 Note 1	3.8	5	V
C <sub>OUT</sub>	Output capacitance	Effective capacitance after derating	0.45	2.2	20	μF
I <sub>OUT_MAX</sub>	Maximum output current	V <sub>OUT</sub> drops 50 mV Note 2	500			mA
<b>Programmable Conditions</b>						
V <sub>OUT</sub>	Selectable output voltage		1.2	3.3	3.75	V
V <sub>OUT_LSB</sub>	LSB of output voltage programming DAC (8-bit control)			10		mV
I <sub>OUT_STARTUP_LIM</sub>	Start-up current limit, programmable in 12 mA steps Note 3	At 90 % V <sub>OUT</sub>	30	150	606	mA
I <sub>OUT_FUNC_LIM</sub>	Functional current limit, programmable in 12 mA steps Note 3		30	550	606	mA

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
<b>Static Parameters</b>						
$V_{OUT\_PP}$	Part to part output voltage accuracy <a href="#">Note 4</a>	$I_{OUT} = 1 \text{ mA}$ $T_A = 25 \text{ }^\circ\text{C}$	-10 <a href="#">Note 5</a>		10 <a href="#">Note 5</a>	mV
$V_{OUT\_TEMP}$	Temperature dependence of $V_{OUT}$ <a href="#">Note 4</a>	$I_{OUT} = 1 \text{ mA}$ <a href="#">Note 6</a>	-0.65		0.65	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation <a href="#">Note 4</a>	$I_{OUT} = 1 \text{ mA}$ $V_{IN} = V_{OUT} + V_{DROPOUT} (\text{Max})$ to $V_{IN} (\text{Max})$	-2		2	mV
$V_{OUT\_STATIC\_LD}$	Static load regulation <a href="#">Note 4</a>	$1 \text{ mA} < I_{OUT} < I_{OUT\_MAX}$	-6		2	mV
$V_{DROPOUT}$	Dropout voltage	@ $V_{OUT} = V_{OUT} (V_{IN} (\text{Max})) - 10 \text{ mV}$ $I_{OUT} = 250 \text{ mA}$ <a href="#">Note 7</a>			200 <a href="#">Note 8</a>	mV
$R_{ON}$	On resistance	@ $V_{IN} = V_{OUT} (V_{IN} (\text{Max})) - 50 \text{ mV}$ $I_{OUT} = I_{OUT\_MAX}$ <a href="#">Note 7</a>			800	m $\Omega$
<b>Dynamic Parameters</b>						
$V_{OUT\_TR\_LINE}$	Line transient response	$V_{IN} = V_{OUT} + V_{DROPOUT} (\text{Max}) + 0.6 \text{ V}$ to $V_{IN} = V_{OUT} + V_{DROPOUT} (\text{Max})$ $V_{OUT} = V_{OUT} (\text{Typ})$ $I_{OUT} = I_{OUT\_MAX}$ $t_R = t_F = 100 \text{ mV}/\mu\text{s}$		2	5 <a href="#">Note 9</a>	mV
$V_{OUT\_TR\_LD\_1 \text{ mA}}$	Load transient response	$V_{IN} = V_{OUT} + V_{DROPOUT} (\text{Max})$ $V_{OUT} = V_{OUT} (\text{Typ})$ $I_{OUT} = 1 \text{ mA}$ to $I_{OUT\_MAX}/2$ $t_R = t_F = 1 \mu\text{s}$		28	37	mV
$t_{ON}$	Turn-on time	Time to 90 % of $V_{OUT}$ $I_{OUT} = 0 \text{ mA}$		0.2		ms
$t_{OFF}$	Turn-off time	Time to 10 % of $V_{OUT}$ $I_{OUT} = 0 \text{ mA}$		0.2	10	ms
<b>AC Parameters</b>						
$PSRR_{1\text{kHz}}$	Power supply rejection ratio	$f = 1 \text{ kHz}$ $V_{IN} = V_{OUT} + 500 \text{ mV}$ $V_{OUT} = V_{OUT} (\text{Typ})$ $I_{OUT} = I_{OUT\_MAX}/2$		83		dB

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Parameter	Description	Conditions	Min	Typ	Max	Unit
PSRR <sub>100kHz</sub>	Power supply rejection ratio	f = 100 kHz V <sub>IN</sub> = V <sub>OUT</sub> + 500 mV V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = I <sub>OUT_MAX</sub> /2		56		dB
PSRR <sub>1MHz</sub>	Power supply rejection ratio	f = 1 MHz V <sub>IN</sub> = V <sub>OUT</sub> + 500 mV V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = I <sub>OUT_MAX</sub> /2		47		dB
V <sub>N</sub>	Output noise	f = 10 Hz to 100 kHz I <sub>OUT</sub> = I <sub>OUT_MAX</sub> /2		152		μV
<b>Current Limit Accuracy</b>						
I <sub>OV_SINK</sub>	Current sink at over-voltage	V <sub>OV</sub> = V <sub>OUT</sub> + 100 mV <a href="#">Note 10</a>	10	77		mA
<b>Quiescent Current Specifications</b>						
I <sub>Q_ON_0mA</sub>	Quiescent current	I <sub>OUT</sub> = 0 mA <a href="#">Note 11</a>		7	13	μA
I <sub>Q_ON_1mA</sub>	Quiescent current	I <sub>OUT</sub> = 1 mA <a href="#">Note 11</a>		30	38	μA
I <sub>Q_ON_IMAX</sub>	Quiescent current	I <sub>OUT</sub> = I <sub>OUT_MAX</sub> <a href="#">Note 11</a>		2.25	3.5	mA
R <sub>PD_OFF</sub>	Output pull down resistance	V <sub>OUT</sub> = 0.5 V LDO disabled		30	100	Ω

**Note 1** I<sub>OUT\_MAX</sub> below 2.1 V is limited to 200 mA. For V<sub>IN</sub> above 2.1 V, I<sub>OUT\_MAX</sub> of 500 mA is guaranteed.

**Note 2** Guaranteed for V<sub>IN</sub> > 2.1 V, between 1.7 V and 2.1 V the I<sub>OUT\_MAX</sub> guaranteed is 200 mA.

**Note 3** Accuracy ±30 %

**Note 4** The overall accuracy can be calculated by summing V<sub>OUT\_PP</sub> + V<sub>OUT\_TEMP</sub> + V<sub>OUT\_STATIC\_LD</sub> + V<sub>OUT\_STATIC\_LINE</sub>.

**Note 5** +10 mV / -10 mV accuracy applies to factory-trimmed V<sub>OUT</sub> values targeted between 1.23 V to 3.72 V. V<sub>OUT</sub> targets from 1.20 V to 1.22 V can be trimmed to +24 mV/ -10 mV accuracy. V<sub>OUT</sub> targets from 3.73 V to 3.75 V can be trimmed to +10 mV / -30 mV accuracy

**Note 6** Guaranteed for V<sub>IN</sub> ≥ 2.5 V.

**Note 7** Guaranteed for V<sub>IN</sub> > 1.8 V.

**Note 8** Dropout voltage is linear with the load current. If using a lower I<sub>OUT\_MAX</sub> than specified, the dropout can be calculated using 80 mV per 100 mA of load.

**Note 9** Guaranteed for V<sub>IN</sub> > 2.1 V. Otherwise, maximum line transient is 20 mV.

**Note 10** Guaranteed for V<sub>IN</sub> > 2.35 V.

**Note 11** Internal regulator current flowing to ground.

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

### 2.9 LDO\_LV Characteristics

In the LDO\_LV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 4.9 V, for  $V_{IN}$  as defined in the table, and apply over the full operating temperature range, see Section 2.1.1.

The characteristics for the LDOs in Load Switch Mode are given in Section 2.9.1.

**Table 9: LDO\_LV (LDO5 and 6) Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
$V_{IN}$	Input supply (pass device + part of controller)		0.8	1.25	1.5	V
$V_{DD\_CTRL}$	Supply for controller (VDD)		2.3	3.8	5	V
$C_{OUT}$	Output capacitance	Effective capacitance after derating	10 Note 1	20	80	$\mu$ F
$ESL_{COUT}$	Output capacitor series inductance	$f > 100$ kHz			1	nH
$I_{OUT\_MAX}$	Maximum output current	$V_{OUT}$ drops 50 mV	800			mA
<b>Programmable Conditions</b>						
$V_{OUT}$	Selectable output voltage		0.5 Note 2	1.175	1.2	V
$V_{OUT\_LSB}$	LSB of output voltage programming DAC (8-bit control)			5		mV
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable in 13 mA steps Note 3	At 90 % $V_{OUT}$	15	150	1211 Note 4	mA
$I_{OUT\_FUNC\_LIM}$	Functional current limit, programmable in 13 mA steps Note 3		15	1000	1211 Note 4	mA
<b>Electrical Performance</b>						
<b>Static Parameters</b>						
$V_{OUT\_PP}$	Part to part output voltage accuracy Note 5	$I_{OUT} = 1$ mA $T_A = 25$ °C	-5		5	mV
$V_{OUT\_TEMP}$	Temperature dependence of $V_{OUT}$ Note 5	$I_{OUT} = 1$ mA Note 6	-1.1		1.1	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 5	$I_{OUT} = 1$ mA $V_{IN} = V_{OUT} + V_{DROPOUT} (Max)$ to $V_{IN} (Max)$	-2		2	mV

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>OUT_STATIC_LD</sub>	Static load regulation <a href="#">Note 5</a>	1 mA < I <sub>OUT</sub> < I <sub>OUT_MAX</sub>	-8		2	mV
V <sub>DROPOUT</sub>	Dropout voltage	@ V <sub>OUT</sub> = V <sub>OUT</sub> (V <sub>IN</sub> (Max)) - 10 mV I <sub>OUT</sub> = I <sub>OUT_MAX</sub> <a href="#">Note 6</a>			80 <a href="#">Note 7</a>	mV
<b>Dynamic Parameters</b>						
V <sub>OUT_TR_LINE</sub>	Line transient response	V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) + 100 mV to V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = I <sub>OUT_MAX</sub> t <sub>R</sub> = t <sub>F</sub> = 100 mV/μs		2	5	mV
V <sub>OUT_TR_LD_1mA</sub>	Load transient response	V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = 1 mA to I <sub>OUT_MAX</sub> /2 t <sub>R</sub> = t <sub>F</sub> = 1 μs		21	29	mV
t <sub>ON</sub>	Turn-on time	Time to 90 % of V <sub>OUT</sub> I <sub>OUT</sub> = 0 mA C <sub>OUT</sub> = 20 μF		0.15		ms
t <sub>OFF</sub>	Turn-off time	Time to 10 % of V <sub>OUT</sub> I <sub>OUT</sub> = 0 mA C <sub>OUT</sub> = 20 μF		2	5 <a href="#">Note 8</a>	ms
<b>AC Parameters</b>						
PSRR <sub>1kHz</sub>	Power supply rejection ratio	f = 1 kHz V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) + 200 mV V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = I <sub>OUT_MAX</sub> /2		70		dB
PSRR <sub>100kHz</sub>	Power supply rejection ratio	f = 100 kHz V <sub>IN</sub> = V <sub>OUT</sub> + V <sub>DROPOUT</sub> (Max) + 200 mV V <sub>OUT</sub> = V <sub>OUT</sub> (Typ) I <sub>OUT</sub> = I <sub>OUT_MAX</sub> /2		50		dB
V <sub>N</sub>	Output noise	f = 10 Hz to 100 kHz I <sub>OUT</sub> = I <sub>OUT_MAX</sub> /2		100		μV
<b>Current Limit Accuracy</b>						
I <sub>OV_SINK</sub>	Current sink at over-voltage	V <sub>OV</sub> = V <sub>OUT</sub> + 100 mV	10			mA
<b>Quiescent Current Specifications</b>						
I <sub>Q_ON_0mA</sub>	Quiescent current, no load	I <sub>OUT</sub> = 0 mA <a href="#">Note 9</a>		8	15	μA

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

Parameter	Description	Conditions	Min	Typ	Max	Unit
I <sub>Q_ON_1mA</sub>	Quiescent current, low load	I <sub>OUT</sub> = 1 mA Note 9		10	16	μA
I <sub>Q_ON_IMAX</sub>	Quiescent current, I <sub>OUT_MAX</sub>	I <sub>OUT</sub> = I <sub>OUT_MAX</sub> Note 9		0.35	1.5	mA
R <sub>PD_OFF</sub>	Output pull down resistance	V <sub>OUT</sub> = 0.5 V LDO disabled		35	100	Ω

**Note 1** For currents less than 400 mA, a minimum of 1.2 μF (after derating) can be used.

**Note 2** Output is capable down to 0.4 V at reduced accuracy. Please contact Dialog Semiconductor for more information

**Note 3** Accuracy ±30 %

**Note 4** LDO5 and 6 share a supply pin and so their combined current limit must not exceed 1.5 A.

**Note 5** The overall accuracy can be calculated by summing V<sub>OUT\_PP</sub> + V<sub>OUT\_TEMP</sub> + V<sub>OUT\_STATIC\_LD</sub> + V<sub>OUT\_STATIC\_LINE</sub>.

**Note 6** Spec guaranteed for V<sub>DD\_CTRL</sub> ≥ 2.8 V.

**Note 7** Dropout voltage is linear with the load current. If using a lower I<sub>OUT\_MAX</sub> than specified, the dropout can be calculated using 10 mV per 100 mA of load.

**Note 8** Max t<sub>OFF</sub> of 20 ms achieved for C<sub>OUT</sub> = 80 μF.

**Note 9** Internal regulator current flowing to ground.

### 2.9.1 Load Switch Mode Characteristics

**Table 10: Load Switch Mode Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input voltage		0.5 Note 1 Note 2		1.25	V
I <sub>OUT_MAX</sub>	Maximum output current		800			mA
<b>Programmable Conditions</b>						
SR	Slew rate, programmable to (4, 6, 8, 10) mV/μs		4		10	mV/μs
I <sub>LIM</sub>	Current limit, programmable from 15 mA to 1.211 A in 13 mA steps Note 3		15		1211 Note 4	mA
<b>Electrical Performance</b>						
R <sub>ON</sub>	On resistance			40		mΩ
SR <sub>ACC</sub>	Slew rate accuracy		-35		35	%
I <sub>LIM_ACC</sub>	Current limit accuracy		-35		35	%



## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

Parameter	Description	Conditions	Min	Typ	Max	Unit
I <sub>Q_OFF</sub>	Quiescent current in off mode	T <sub>A</sub> = 25 °C			2	μA

**Note 1** Input is capable down to 0.4 V. Please contact Dialog Semiconductor for more information

**Note 2** Register bit SEL\_BYP\_VGATE must be set to 0 for V<sub>IN</sub> between 0.5 V and 0.8 V, and is recommended to be set to 1 for V<sub>IN</sub> between 0.8 V and 1.25 V.

**Note 3** Current limit is guaranteed for V<sub>IN</sub> > 0.7 V. Below 0.7 V, a functional current limit is not guaranteed.

**Note 4** Load switch 1 and 2 share a supply pin and so their combined current limit must not exceed 1.5 A.

### 2.10 VREF, IREF, Temperature Supervision Characteristics

Table 11: VREF, IREF, Temperature Supervision Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Programmable Conditions</b>						
V <sub>REF</sub>	Reference voltage	Internal VREF		1.2		V
T <sub>WARN</sub>	Warning temperature threshold, programmable to (90, 100, 110, 120) °C		90		120	°C
T <sub>WARN_HYS</sub>	Warning temperature hysteresis, programmable to (0, 14) °C			14		°C
<b>Electrical Performance</b>						
V <sub>REF_ACC</sub>	Reference voltage accuracy	Internal VREF	-1		1	%
T <sub>TOT</sub>	Thermal shutdown over-temperature		125	140	155	°C
T <sub>WARN_ACC</sub>	Warning temperature threshold accuracy		-5		5	°C

### 2.11 Internal Oscillator Characteristics

Table 12: Internal Oscillator Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
f <sub>CLK</sub>	Internal clock frequency		7.2	8	8.8	MHz

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

### 2.12 UVLO Characteristics

Table 13: UVLO Electrical Characteristics

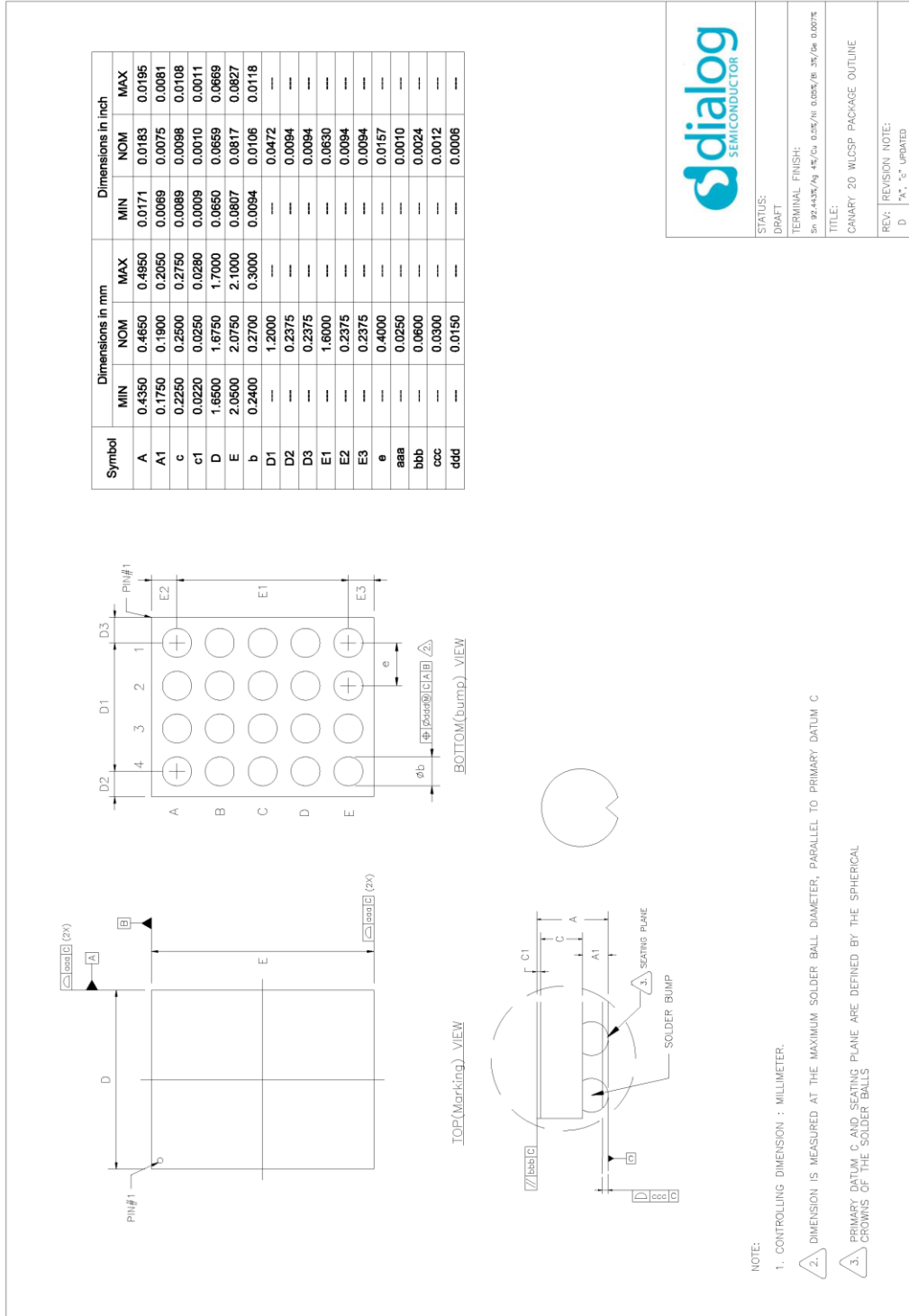
Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Programmable Conditions</b>						
V <sub>DD_UVLO_LWR</sub>	Under-voltage lower threshold (falling edge) <a href="#">Note 1</a>		2.215		2.658	V
V <sub>DD_UVLO_UPPER</sub>	Under-voltage upper threshold (rising edge)			V <sub>DD_UVLO_LWR</sub> + 3 %		V
<b>Electrical Performance</b>						
V <sub>DD_POR_UPPER</sub>	Deep discharge lockout upper threshold			2.1	2.2	V
V <sub>DD_POR_LWR</sub>	Deep discharge lockout lower threshold			1.9		V
V <sub>DD_UVLO_STAT_ACC</sub>	Under-voltage lower threshold static accuracy with flip gate bandgap reference		-1.5		1.5	%

**Note 1** This voltage is programmed from OTP in 24.6 mV steps.

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

### 3 Package Information

#### 3.1 Package Outlines



STATUS:  
DRAFT

TERMINAL FINISH:  
Sn, 92.443%/Ag, 45%/Cu, 0.05%/Ni, 0.005%/Bi, 35%/Ge, 0.007%

TITLE:  
CANARY 20 WLCSP PACKAGE OUTLINE

REV: REVISION NOTE:  
D "A", "c" UPDATED

Figure 2: Package Outline Drawing

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

3.2 PCB Landing Pattern

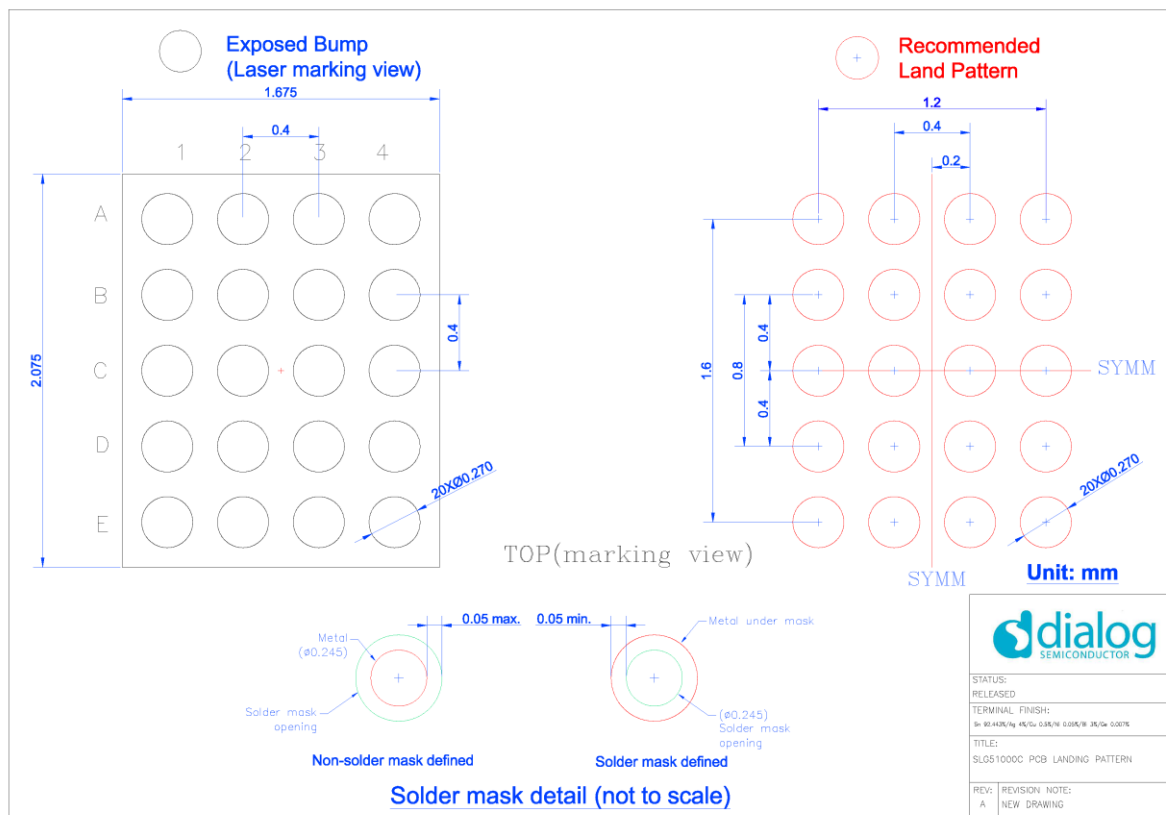


Figure 3: PCB Landing Pattern

3.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 14

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

MSL rating does not apply to this device as it is not plastic encapsulated.

Table 14: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

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**PMIC with High PSRR, Low Noise, Multi-Output LDOs  
and Integrated Load Switches****3.4 WLCSP Handling**

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

**3.5 Soldering Information**

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

## PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

### 4 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's [customer support portal](#) or your local sales representative.

**Table 15: Ordering Information**

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
SLG51000CTR	WLCSP-20	1.675 x 2.075	T & R	

### 5 Layout Recommendation

**To ensure stability and best performance:**

1. Place input and output decoupling capacitors as close to their respective device pins as possible, on same side as the device, and connected via wide tracks and paralleled vias to reduce inductance.
2. Separate VIN, VDD and VOUT grounds by star connecting these grounds to the main GND as close to the GND ball as possible. Avoid sharing of GND return paths of decoupling caps to chip. Avoid GND loops between input supplies (VIN, VDD) and VOUT. See [Figure 4](#).
3. Use wide tracks where possible for high current carrying paths such as VIN and VOUT.
4. Do not allow VIN and VOUT routes to run alongside each other too closely for too long a length. This may cause crosstalk or coupling effects.
5. Place VIN and VOUT grounds directly above the VDD plane for high PSRR LDOs.

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

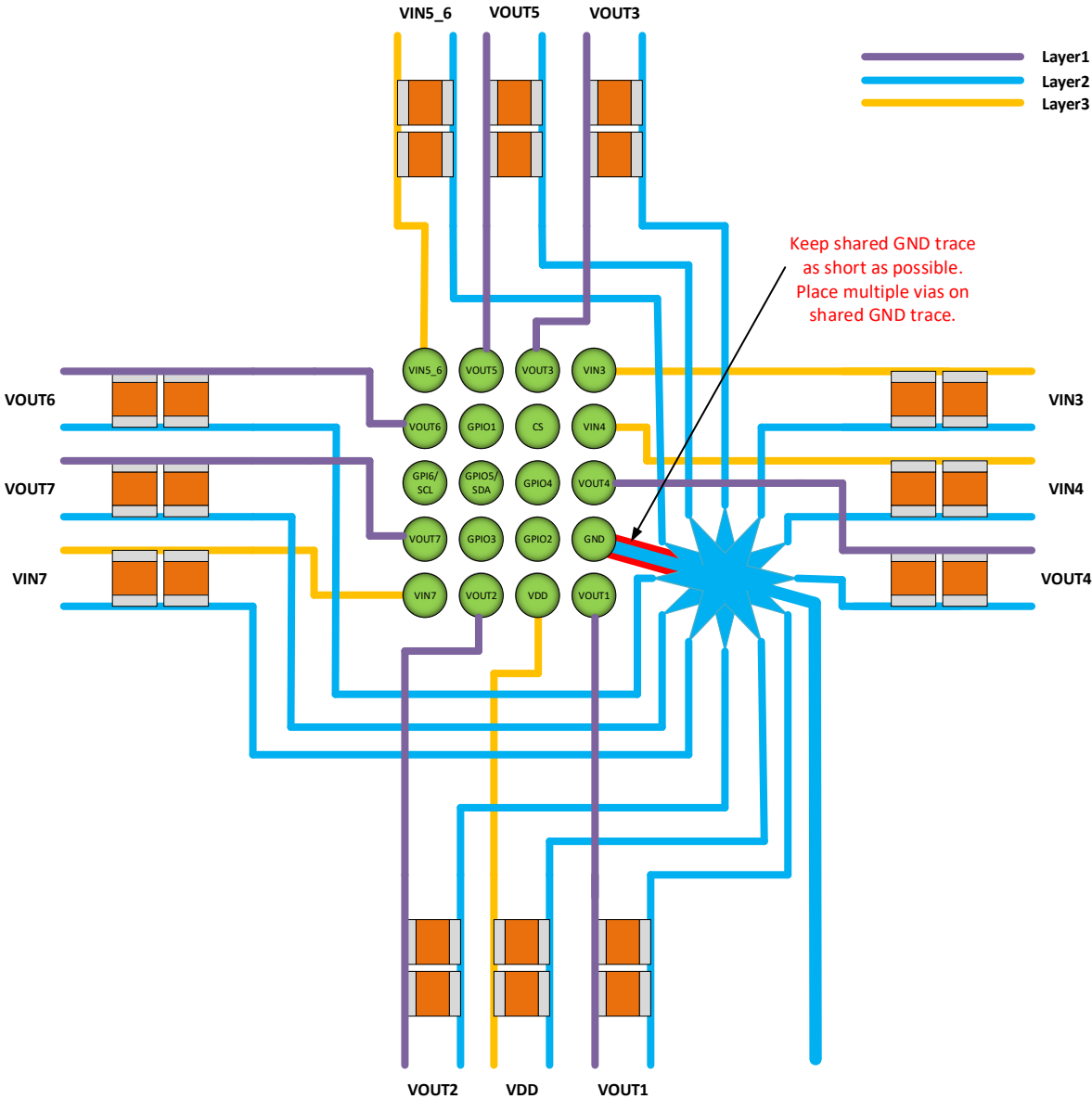
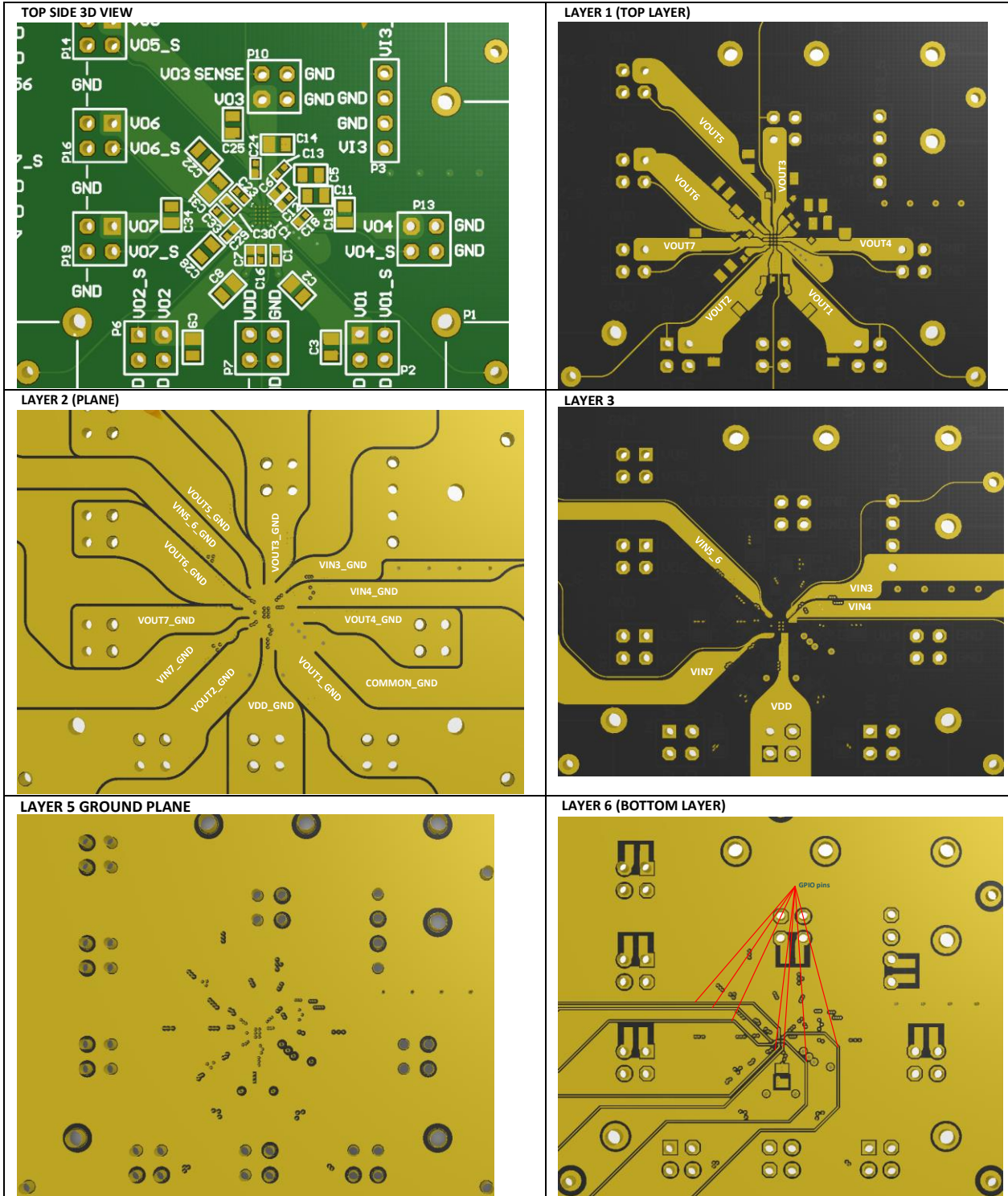


Figure 4: Star point for LDO Ground connection

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

Table 16: PCB layers recommendation view





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**PMIC with High PSRR, Low Noise, Multi-Output LDOs  
and Integrated Load Switches****Status Definitions**

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via website
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.