

Dual Rail High Voltage Gate Driver

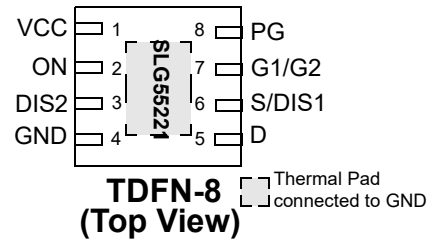
Features

- 5 V Power supply
- Drain Voltage Range 1.0 V to 20 V
- Internal Gate Voltage Charge Pump
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- TDFN-8 Package

Applications

- Power Supply Sequencing with ramp/delay/discharge control
- Power Rail “Soft” Switch
- Hot Plugging Applications
- Low Transient Load Switching
- Replace high cost P-channel MOSFETs with lower cost N-channel MOSFETs

Pin Configuration



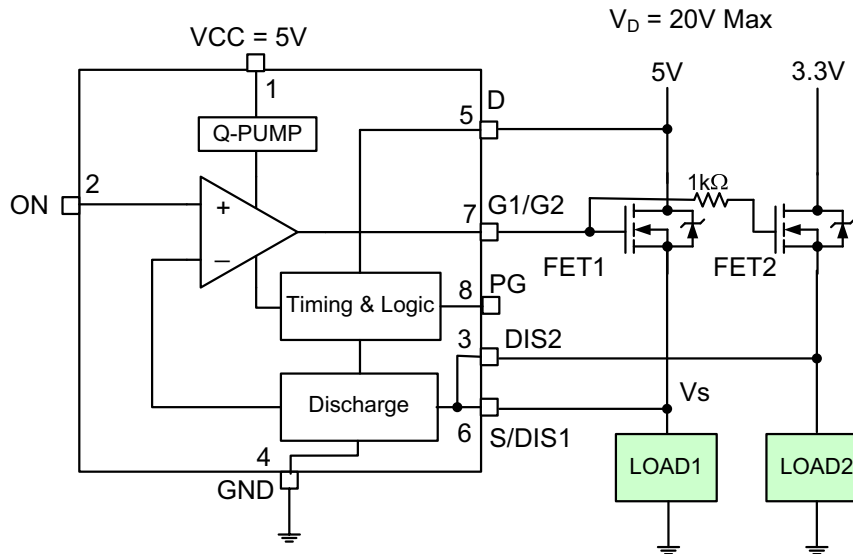
Environmental

- Pb-Free / RoHS compliant
- Halogen Free

Target Application Products

- Notebook & Netbook Battery Packs
- Notebook & Netbook Sleep Mode Circuits
- Server Load Switches
- Gaming Sleep Mode Power Switches
- Communications Power Switches

Block Diagram



The highest  $V_D$  being switched must be at FET1 and pin 5 of the SLG55221 and SLG55220

**SLG55221**  
 $V_G$  is pumped to  $V_D + 8V$

**SLG55220**  
 $V_G$  is pumped to  $V_D + 4V$  min

## Dual Rail High Voltage Gate Driver

### Pin Description

Pin #	Pin Name	Type	Pin Description
VCC	1	Power	Supply Voltage
2	ON	Input	CMOS Logic Level. See SLG55251 for Control Input ON# instead of ON.
3	DIS2	Output	Discharge Connection for Load2
4	GND	GND	Ground
5	D	Input	FET Drain Connection (Connect to FET with highest $V_D$ voltage)
6	S/DIS1	Input/Output	Source Connection, Discharge Connection for Load1
7	G1/G2	Output	FET Gate Drive for FET1, FET2
8	PG	Output	CMOS Power Good Signal
Exposed Bottom Pad	GND	GND	Ground

### Overview

The SLG55221/220 N-Channel FET Gate Drivers are used for controlling and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the SLG55221/220 also integrates circuits to discharge opened switched voltage rails. The gate driver is available in a variety of configurations supporting a range of turn-on slew rates from 0.80V/ms up to 2V/ms which, depending on load supplying source voltages in the range of 1.0V to 20V results in ramp times from 200 $\mu$ s to over 20ms (see Application Section). Additionally, an internal discharge circuit provides a controlled path to remove charge from open power rails. The SLG55221/220 gate drive is packaged in an 8 pin DFN package. A power good (PG) signal is asserted when FET1 is fully ON.

When used with external N-Channel FETs, the SLG55221 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0V to 20V.

A 'Low Drive' version of the device, is available to support applications where FET  $V_{gs}$  cannot exceed 8V.

### Ordering Information

Part Number	Ramp Slew Rate (Volts/ms)	Delay Time (ms)	Discharge Resistor (ohms)	Package Type
SLG55220 -120010V	1.30	0.50	200	TDFN-8
SLG55221-120010V	1.30	0.50	200	TDFN-8
SLG55220 -120010VTR	1.30	0.50	200	TDFN-8 - Tape and Reel (3k units)
SLG55221-120010VTR	1.30	0.50	200	TDFN-8 - Tape and Reel (3k units)

## Dual Rail High Voltage Gate Driver

## Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
$V_D$ or $V_S$ to GND	-0.3	40.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Operating temperature range	-55	125	°C
Junction temperature	--	150	°C
ESD Human Body Model	--	2000	V
ESD Machine Model	--	200	V

## Electrical Characteristics

 $T_A = -10\text{ °C to }75\text{ °C}$ 

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage		4.75	5.0	5.25	V
$T_{VCC\_RAMP}$	$V_{CC}$ Ramp-up Rate	See Note 1	0.25	--	--	V/ms
$I_q$	Quiescent Current	$V_G$ not ramping FET = ON	--	--	80	$\mu$ A
		$V_G$ not ramping FET = OFF	--	0.1	1	$\mu$ A
		$V_G$ ramping FET = OFF to ON	--	600	1500	$\mu$ A
$V_D$	FET Drain Voltage	SLG55220	0.95	--	5.25	V
		SLG55221	1.0	--	20	V
$V_{GS}$	Gate-Source Voltage	SLG55220	4.0	4.7	6.0	V
		SLG55221	8.0	--	13	V
$C_G$	FET Gate Capacitance		500	--	18000	pF
$T_{DELAY}$	Ramp Delay Range		0.25	0.5	0.75	ms
$T_{SLEW}$	FET Turn on Slew Rate		0.91	1.30	1.69	V/ms
$I_{DISCHARGE}$	Internal Discharge Resistor	Nominal discharge time of ~100ms 10mA max rate	140	200	260	$\Omega$
$V_{IH}$	HIGH-level input voltage	ON (200mV Hysteresis)	2.4	--	5.5	V
$V_{IL}$	LOW-level Input voltage	ON (200mV Hysteresis)	--	--	0.4	V
$V_{OH}$	HIGH-level output voltage	PG	4.0	--	--	V
$V_{OL}$	LOW-level output voltage	PG	--	--	0.7	V
$I_{OL\_LOGIC}$	Logic LOW level output	PG Sink Current	1	2	3	mA
$I_{G\_OL}$	Gate Drive Sink Current		400	--	--	$\mu$ A
$I_{G\_OH}$	Gate Drive Source Current		32	--	--	$\mu$ A
$I_{D\_IH}$	Drain Pin Current	$V_D = 20V$ in Standby	--	--	<1.0	$\mu$ A
$I_{S\_IH}$	Source Pin Current Quiescent	$V_S = 20V$	--	--	<1.0	$\mu$ A

Notes:

- If  $T_{VCC\_RAMP} > 5V/ms$  and ON is asserted, Gate charging will begin after 1ms.

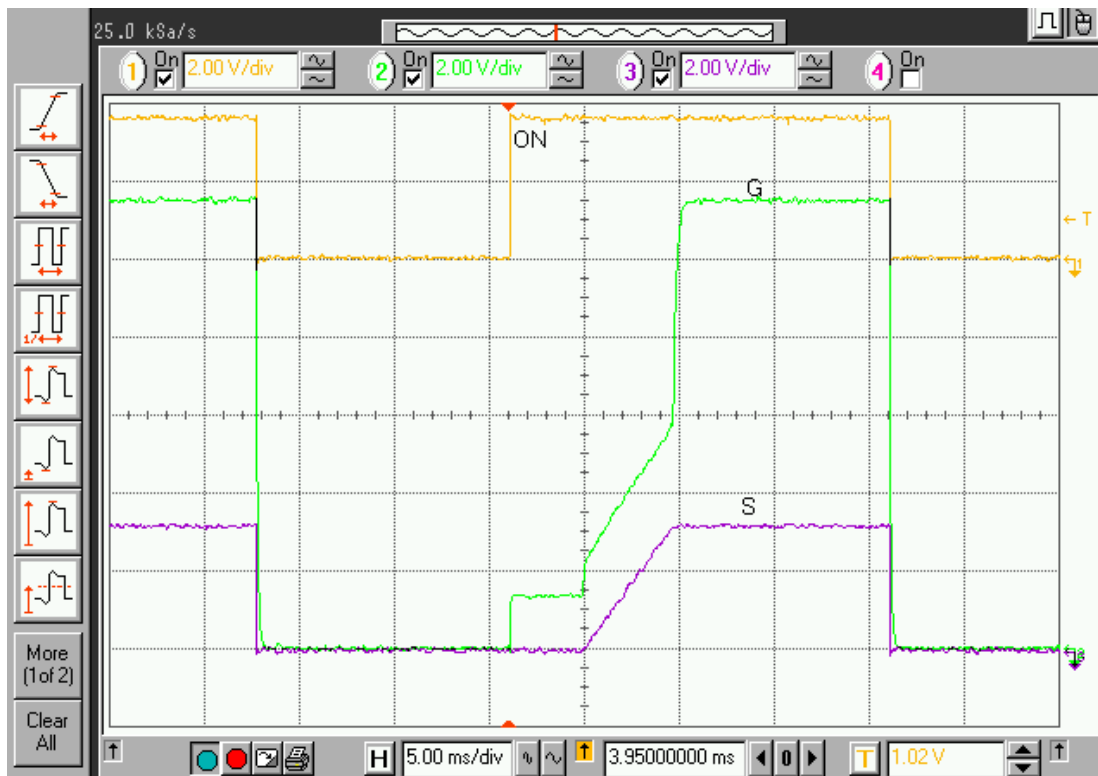
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Application Example

In a typical application, de-asserting ON (low) or turns off the external power N-FET. When the FET is turned off, the voltage at the load is discharged through a resistor (400 Ohms to 1000 Ohms or Open) internal to the SLG55221/220 with the discharge current limited to a maximum of 10mA. When ON is asserted (high), gate voltage is not applied to the gate of the external power N-FET until after DLY\_t then the gate source (Vgs) voltage is ramped up to 11.5V above the source voltage  $V_S$  at a slew rate determined by the internal slew rate control element internal to the SLG55221/220. Monotonic rise of  $V_S$  is maintained even as  $I_D$  increases dramatically after the load device turn on threshold voltage is reached. After the source voltage has ramped up to its maximum steady state value, PG (Power Good) is asserted. PG may be used as the ON control of a second SLG55221/220 thereby providing power on sequence control of a number of switched power rails.

The devices will not operate if  $V_{CC}$  is below 3.5V and will not operate until  $V_D$  reaches 0.8V.

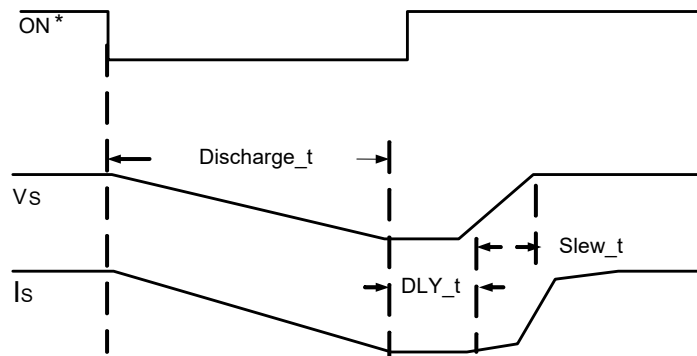
The waveforms shown illustrate the monotonic rise of the source voltage of a FET as gate voltage is controlled to accommodate for variations in load current as the voltage is applied.



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Delay Time and Slew Rates

The two components of controlling the application of FET source voltage to the load are a fixed time delay before beginning turn on of the FET (DLY\_t below) and the Slew Time of the source voltage (Slew\_t below). The Delay Time before gate voltage to the FET is applied is 250 μs independent of FET drain voltage, source voltage or SLG55221/220 supply voltage.



Having control over the Slew Rate of the FET's source voltage as the FET is turning on is important in controlling dv/dt caused transients. A power FET, for example, switching a 5 V rail which has a total of 500 μF of decoupling, fully on in 10 μs will generate a 250 A current surge which is very undesirable. If the FET turn on time can be stretched to 1 ms, the current surge to charge the decoupling capacitors is reduced to 2.5 A. The SLG55221/220 controls slew rate of a FET's source voltage as it is turned on. A range of slew rates are available as device order options. Obviously the time to fully slew the source voltage to fully on is a function of the drain supply voltage. The table and graph below shows source voltage ramp times for various slew rates supported by the SLG55221/220 for a range of specific source voltages.

Slew Rates (V/ms)	Ramp Times (ms) vs. Source Voltages (V)				
	1.1 V	1.5 V	1.8 V	3.3 V	5.0 V
1.30	0.83	1.13	1.35	2.48	3.75

\* The minimum time that ON can be de-asserted between switching cycles is 100 ms.

**Package Top Marking System Definition**  
For devices manufactured after 2021

<b>PPP</b>	Part Code
<b>NNN</b>	Serial Number
○ <b>R</b>	Pin 1 Identifier + Revision Code

PPP - Part Code Field: Identifies the specific device Configuration

NNN - Serial Number Field: Serial number

R - Revision Code Field: Device Revision

**For devices manufactured before 2021**

<b>XXA</b>	Part ID + Assembly Code
<b>DDL</b>	Date Code + Lot
○ <b>R</b>	Pin 1 Identifier + Revision Code

XX - Part ID Field: Identifies the specific device Configuration

A - Assembly Code Field: Assembly Location of the device

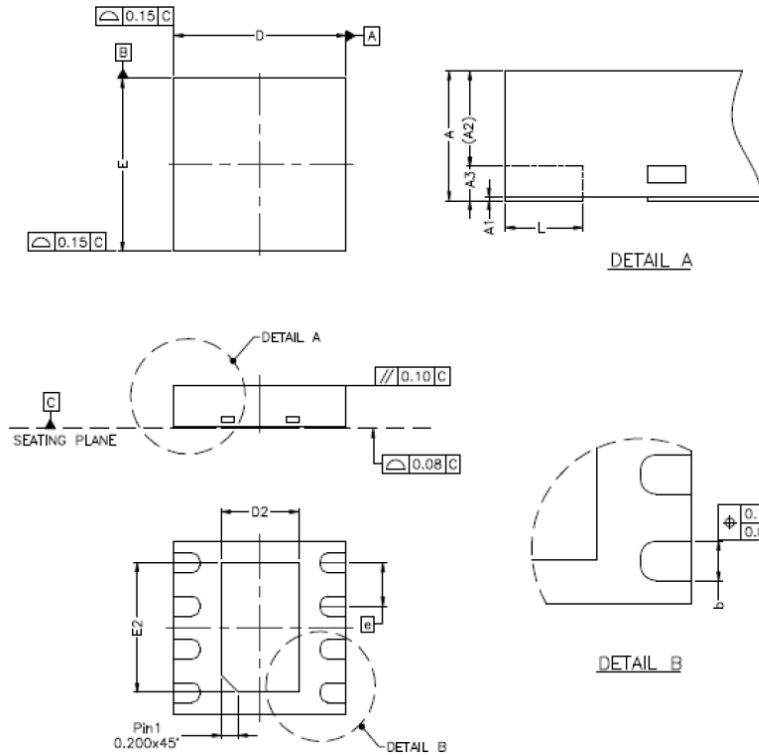
DD - Date Code Field: Coded Date of Manufacture

L - Lot Code: Designates Lot #

R - Revision Code: Device Revision

Package Drawing and Dimensions

8 Lead TDFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	—	0.20	—	—	8	—
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1	—			—		
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1	—			—		
E2	1.50	1.65	1.70	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

NOTE :

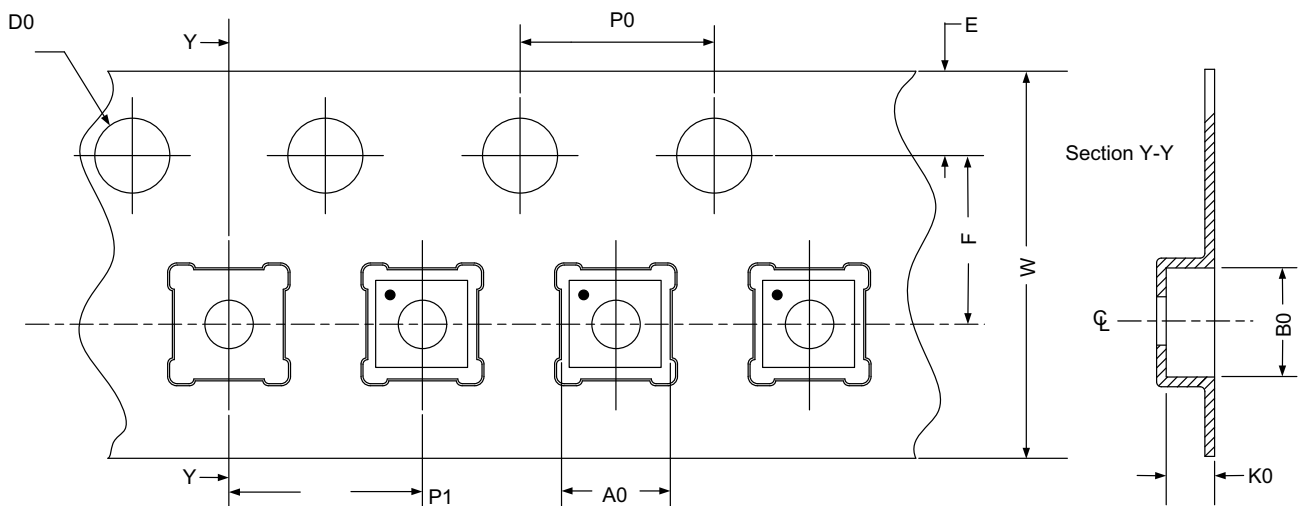
1. REFER TO JEDEC STD: MO-229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).



**Revision History**

Date	Version	Change
6/8/2023	1.03	Updated Part Marking Definition
2/9/2022	1.02	Updated Company name and logo Fixed typos
7/10/2018	1.01	Updated style and formatting

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