SLG59H1132V

22 V, 13 mΩ, 6 A Load Switch with V_{IN} Lockout Select and MOSFET Analog Current Monitor Output

The SLG59H1132V is a high-performance, self-powered 13 mΩ NMOS load switch designed for all 4.5 V to 22 V power rails up to 6 A. Using a proprietary MOSFET design, the SLG59H1132V achieves a stable 13 mΩ RDS_{ON} across a wide input voltage range. In combining novel FET design and copper pillar interconnects, the SLG59H1132V package also exhibits a low thermal resistance for high current operation.

Designed to operate over a -40 °C to +85 °C range, the SLG59H1132V is available in a low thermal resistance, RoHS-compliant, 1.6 mm x 3.0 mm STQFN package.

Features

- Wide Operating Input Voltage Range: 4.5 V to 22 V
- Maximum Continuous Current: 6 A
- Integrated Low RDS_{ON} nFET switch: 13 mΩ
- Pin-selectable V_{IN} Overvoltage Lockout
- Two stage Automatic nFET SOA Protection:
  - 25 W SOA Threshold Without Blanking Time
  - 12.5 W SOA Threshold With 18 ms Blanking Time
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
  - Resistor-adjustable Active Current Limit
  - Internal Short-circuit Current limit
- Open Drain $\overline{FAULT}$ Signaling
- Open Drain Power Good Signaling
- MOSFET Analog Current Monitor Output: 10 µA/A
- ON-OFF Control: Active HIGH
- Operating Temperature Range: -40°C to 85°C
- Fast 4 kΩ Output Discharge
  - Pb-Free / Halogen-Free / RoHS Compliant Packaging

Applications

- Power-Rail Switching
- Multifunction Printers
- Telecommunications Equipment
- High-performance Computing
  - 5 V, 9 V, 12 V, and 20 V Point-of-Load Power Distribution

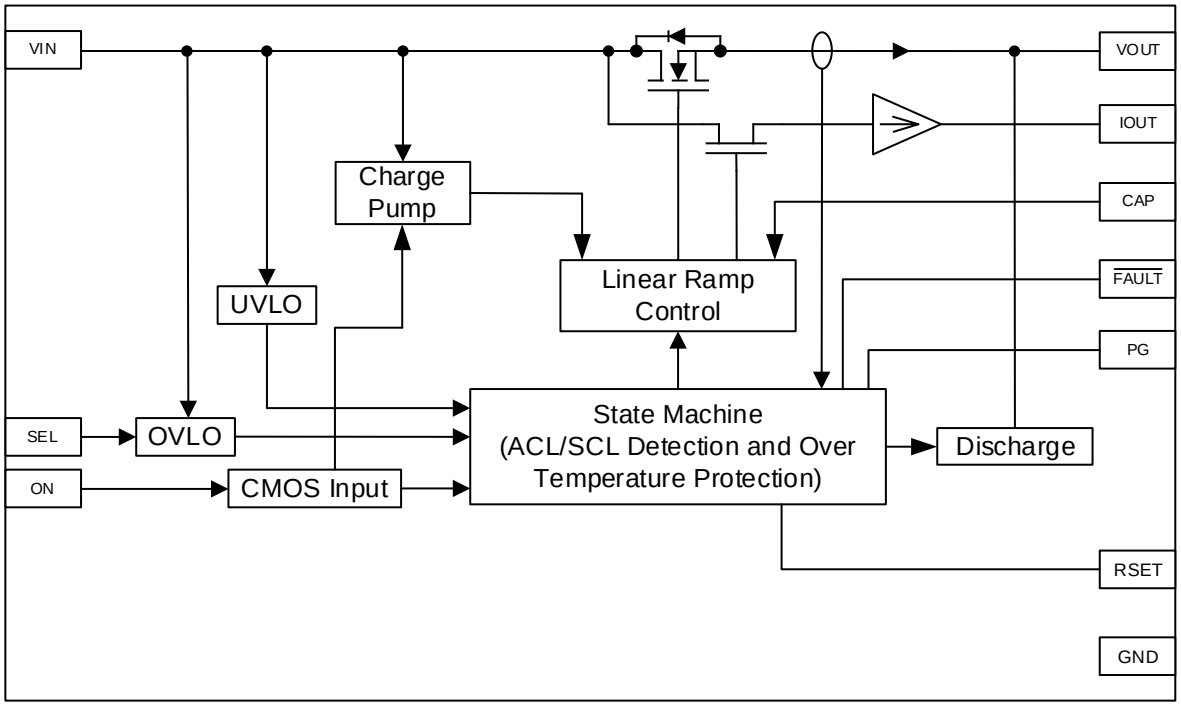

Figure 1. Block Diagram

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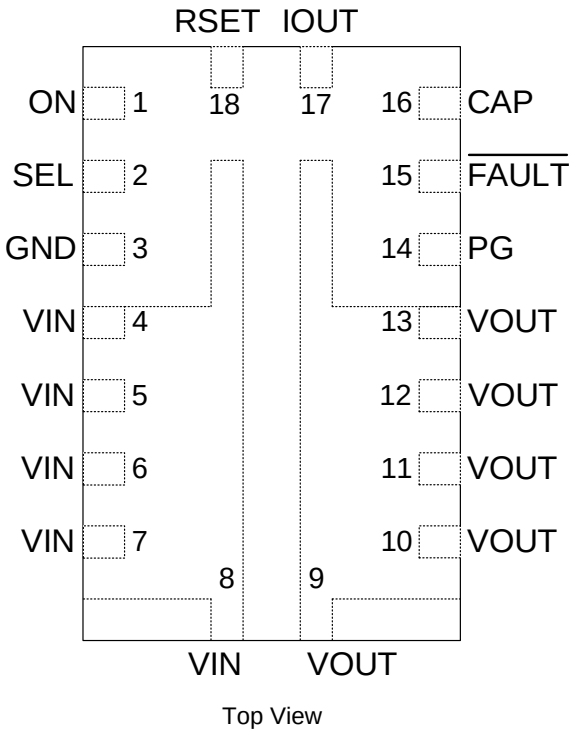
1. Pin Assignments



Top View

Figure 2. Pin Assignment - STQFN-18

1.1 Pin Descriptions

Table 1. Pin Assignment & Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1132V. ON is an asserted High, level-sensitive CMOS input with V_{IL_ON} < 0.3 V and V_{IH_ON} > 0.9 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
2	SEL	Input	As level-sensitive, CMOS input with V_{IL_SEL} < 0.3 V and V_{IH_SEL} > 1.65 V, SEL selects one of two V_{IN} overvoltage lockout thresholds. Please see the Application Information section for additional information and the Electrical Characteristics table for the V_{IN} overvoltage thresholds. A logic low on SEL pin is achieved by connecting it to GND while logic high is achieved by connecting a 10 kΩ external resistor from the SEL pin to the system's local logic supply that is not higher than V_{IN} voltage. The SEL pin input circuit has an internal 220 kΩ pull-down resistor when ON is Low.
3	GND	Power	Pin 3 is the main ground connection for the SLG59H1132V's internal charge pump, its gate driver and current limit circuits as well as its internal state machine. Therefore, use a short, solid connection from Pin 3 to the system's analog or power plane.
4-8	VIN	Power	VIN supplies the power for the operation of the SLG59H1132V, its internal control circuitry, and the drain terminal of the nFET load switch. With 5 pins fused together at VIN, connect a 47 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at a voltage higher than maximum input voltage ever present.
9-13	VOUT	Power	Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 10 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at a voltage higher than maximum output voltage ever present.

Pin #	Pin Name	Type	Pin Description
14	PG	Output	An open-drain output, PG is asserted within TPG_{HIGH} when V_{OUT} is higher than SLG59H1132V's $PG_{TRIGGER}$ threshold. PG output becomes de-asserted within TPG_{LOW} when ON is toggled from High-to-Low. PG is not defined for V_{IN} < 4 V. Connect a 10 kΩ or higher external resistor from the PG pin to local system logic supply that is not higher than V_{IN} voltage.
15	$\overline{FAULT}$	Output	An open drain output, $\overline{FAULT}$ is asserted within $T\overline{FAULT}_{LOW}$ when a V_{IN} overvoltage, SOA protection, a current limit, or an over-temperature condition is detected. $\overline{FAULT}$ is de-asserted within $T\overline{FAULT}_{HIGH}$ when the fault condition is removed. Connect a 10 kΩ or higher external resistor from the $\overline{FAULT}$ pin to local system logic supply that is not higher than V_{IN} voltage. $\overline{FAULT}$ is not defined for V_{IN} < 4 V.
16	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount C_{SLEW} capacitor connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn on time of the SLG59H1132V. For best performance, the range for C_{SLEW} values are 10 nF ≤ C_{SLEW} ≤ 20 nF – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher.
17	IOUT	Output	IOUT is the SLG59H1132V's power MOSFET load current monitor output. As an analog current output, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The I_{OUT} transfer characteristic is typically 10 µA/A with a voltage compliance range of 0.5 V ≤ V_{IOUT} ≤ 4 V. Optimal I_{OUT} linearity is exhibited for 0.5 A ≤ I_{DS} ≤ 6 A. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor.
18	RSET	Input	A 1%-tolerance, metal-film resistor between 14 kΩ and 91 kΩ sets the SLG59H1132V's active current limit. A 91 kΩ resistor sets the SLG59H1132V's active current limit to 1 A and a 14 kΩ resistor sets the active current limit to 7 A.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter		Min	Max	Unit
Load Switch Input Voltage (V_{IN}) to GND	Continuous	-0.3	30	V
	Maximum pulsed V_{IN}, pulse width < 0.1 s	-	32	
Load Switch Output Voltage (V_{OUT}) to GND		-0.3	V_{IN}	V
ON, PG, CAP, SEL, RSET, IOUT and $\overline{FAULT}$ Pin Voltages to GND		-0.3	7	V
Continuous Current from VIN to VOUT (T_J < 150 °C)		-	8.2	A
Peak Current from VIN to VOUT (Maximum pulsed switch current for no more than 1 ms pulse width with 1% duty cycle)		-	9	A

2.2 ESD Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	-	V
ESD Protection (Charged Device Model)	500	-	V

2.3 Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
V_{IN} Operating Input Voltage		4.5	22	V
Maximum Operating Current from VIN to VOUT		-	6	A
Operating Ambient Temperature Range		-40	+85	°C

2.4 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]
STQFN-18 Package	40
[1] Determined with the device mounted onto a 1 in^2, 1 oz. copper pad of FR-4 material.	

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C

2.5 Electrical Characteristics

4.5 V ≤ V_{IN} ≤ 22 V; C_{IN} = 47 µF, T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25 °C

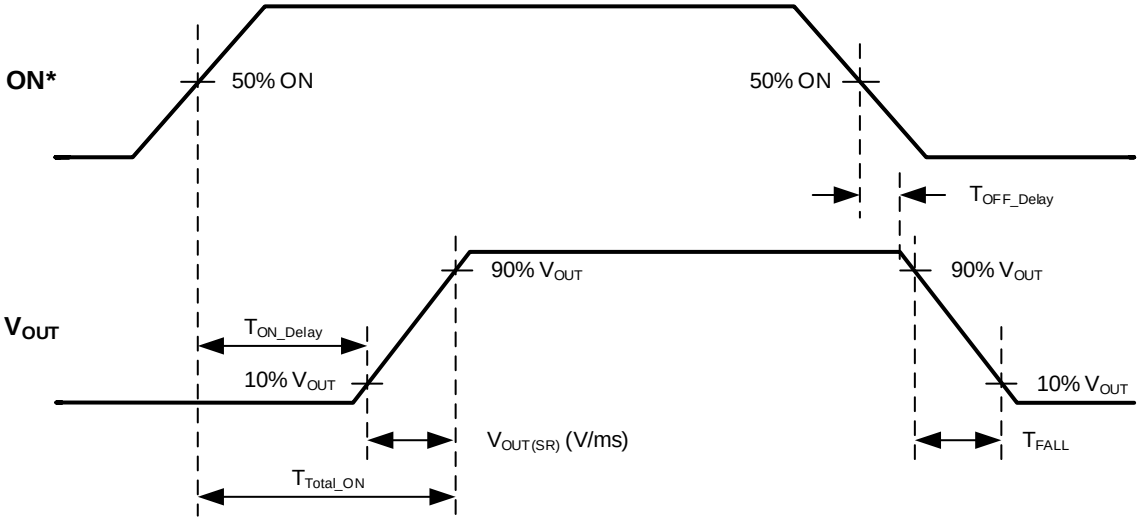
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Supply Current	I_Q	ON = High; No Load	-	0.50	0.61	mA
OFF Mode Supply Current	I_{SHDN}	ON = Low; No Load	-	0.5	3	µA
V_{IN} Undervoltage Lockout Threshold	V_{IN_UVLO}	V_{IN} Fall ↓, R_{LOAD} = 1 kΩ, no C_{LOAD}	1.9	-	3.8	V
V_{IN} Undervoltage Lockout Hysteresis	$V_{IN\_UVLO\_HYS}$	V_{IN} Rise ↑, R_{LOAD} = 1 kΩ, no C_{LOAD}	-	300	-	mV
V_{IN} Overvoltage Lockout Threshold	V_{IN_OVLO}	V_{IN} Rise ↑; SEL = Low	13.2	14.4	15.2	V
		V_{IN} Rise ↑; SEL = High	22.2	24	25.2	V
Power MOSFET Static ON Resistance	RDS_{ON}	T_A = 25 °C; I_{DS} = 0.1 A	-	13	14	mΩ
		T_A = 85 °C; I_{DS} = 0.1 A	-	16.8	18	
Active Current Limit	I_{ACL}	V_{OUT} > 0.5 V; R_{SET} = 30.1 kΩ	2.64	3.3	3.96	A
Short-circuit Current Limit	I_{SCL}	V_{OUT} < 0.5 V; R_{LOAD} = 0.25 Ω	-	1	-	A
VOUT Discharge Resistance	$R_{DISCHRG}$	V_{OUT} = 0.4 V Input Bias; ON = Low	3.5	4.4	5.3	kΩ
VOUT Load Capacitance	C_{LOAD}	C_{LOAD} connected from VOUT to GND	-	10	-	µF
MOSFET Analog Current Monitor Output	I_{OUT}	I_{DS} = 1 A	8.5	10	11.5	µA
		I_{DS} = 3 A	27	30	33	µA
I_{OUT} Response Time to Change Current in Main MOSFET	T_{IOUT}	0% I_{OUT} to 90% I_{OUT} R_{IOUT} = 64.9 kΩ, C_{IOUT} = 180 pF; Load step from 0 A to 1 A;	-	70	-	µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn ON Delay Time	T_{ON_Delay}	50% ON to 10% V_{OUT}; V_{IN} = 4.5 V, C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	-	0.40	0.54	ms
		50% ON to 10% V_{OUT}; V_{IN} = 22 V, C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	-	0.9	1.2	ms
Total Turn ON Time	T_{Total_ON}	50% ON to 90% V_{OUT}	Set by External C_{SLEW}[2]			
		50% ON to 90% V_{OUT}; V_{IN} = 4.5 V, C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	-	1.6	2.1	ms
		50% ON to 90% V_{OUT}; V_{IN} = 22 V, C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	-	6.5	8	ms
V_{OUT} Slew Rate	$V_{OUT(SR)}$	10% V_{OUT} to 90% V_{OUT}	Set by External C_{SLEW}[2]			
		10% V_{OUT} to 90% V_{OUT}; V_{IN} = 4.5 V to 22 V, C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF	2.4	3.2	4.0	V/ms
Turn OFF Delay Time	T_{OFF_Delay}	50% ON to V_{OUT} Fall Start; V_{IN} = 4.5 V to 22 V, R_{LOAD} = 100 Ω, No C_{LOAD}	-	18	-	µs
V_{OUT} Fall Time	T_{FALL}	90% V_{OUT} to 10% V_{OUT}; ON = Hight-to-Low, V_{IN} = 4.5 V to 22 V, R_{LOAD} = 100 Ω, No C_{LOAD}	8	13	20	µs
$\overline{FAULT}$ Assertion Time	$T\overline{FAULT}_{LOW}$	Abnormal Step Load Current event to $\overline{FAULT}$ go Low; I_{ACL} = 1 A, V_{IN} = 22 V, R_{SET} = 91 kΩ, switch in R_{LOAD} = 14 Ω	-	80	-	µs
$\overline{FAULT}$ De-assertion Time	$T\overline{FAULT}_{HIGH}$	Delay to $\overline{FAULT}$ go High after fault condition is removed; I_{ACL} = 1 A, V_{IN} = 22 V, R_{SET} = 91 kΩ, switch out R_{LOAD} = 14 Ω	-	180	-	µs
Active Current Limit Response Time	T_{ACL}	From Load Current Step Event I_{DS} > I_{ACL} to current is regulated to I_{ACL} threshold; V_{IN} = 12 V; R_{SET} = 91 kΩ, C_{LOAD} = 10 µF; switch in R_{LOAD} = 10 Ω	-	880	-	µs
PG Pin Output Low Voltage	V_{OL_PG}	PG Pin Sink Current I_{PG_SINK} = 5 mA	-	-	0.4	V
PG Pin Leakage Current	$I_{PG\_Leakage}$	V_{IN} = 4.5 V, 9 V, 12 V, 22 V; Switch is in On state,	-	-	1	µA
Power Good Threshold Voltage Level	$PG_{TRIGGER}$[3]	V_{OUT} % of V_{IN}	85	90	95	%
PG Assertion Time	TPG_{HIGH}	Delay to PG go High after $PG_{TRIGGER}$ threshold is crossed.	1	1.25	1.5	ms
PG De-assertion Time	TPG_{LOW}	Delay to PG go Low after ON is toggled from High-to-Low.	-	7	-	µs
$\overline{FAULT}$ Pin Output Low Voltage	$V_{OL\_\overline{FAULT}}$	$\overline{FAULT}$ Pin Sink Current $I_{\overline{FAULT}\_SINK}$ = 5 mA, V_{IN} = 4.5 V, 9 V, 12 V, 22 V.	-	-	0.4	V
$\overline{FAULT}$ Pin Leakage Current	$I_{\overline{FAULT}\_Leakage}$	V_{IN} = 4.5 V, 9 V, 12 V, 22 V; Switch is in On state,	-	-	1	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ON Pin Input High Voltage	V_{IH_ON}		0.9	-	5	V
ON Pin Input Low Voltage	V_{IL_ON}		-	-	0.3	V
ON Pin Leakage Current	$I_{ON\_Leakage}$	1 V ≤ V_{ON} ≤ 5 V or ON = GND	-	-	1	µA
SEL Pin Input High Voltage	V_{IH_SEL}		1.65	-	4.5	V
SEL Pin Input Low Voltage	V_{IL_SEL}		-	-	0.3	V
SEL Pin Leakage Current	$I_{SEL\_Leakage}$	0.3 V ≤ V_{SEL} ≤ 4.5 V or SEL = GND, ON = High	-	-	1	µA
Thermal shutdown turn on temperature threshold	$THERM_{ON}$		-	150	-	°C
Thermal shutdown turn off temperature threshold	$THERM_{OFF}$		-	125	-	°C

[2] Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information.
[3] Guaranteed by Design

3. Typical Performance Graphs and Operation Waveforms



*Rise and Fall Times of the ON Signal are 100 ns

Figure 3. Turn ON and Turn OFF Timing Parameter Details

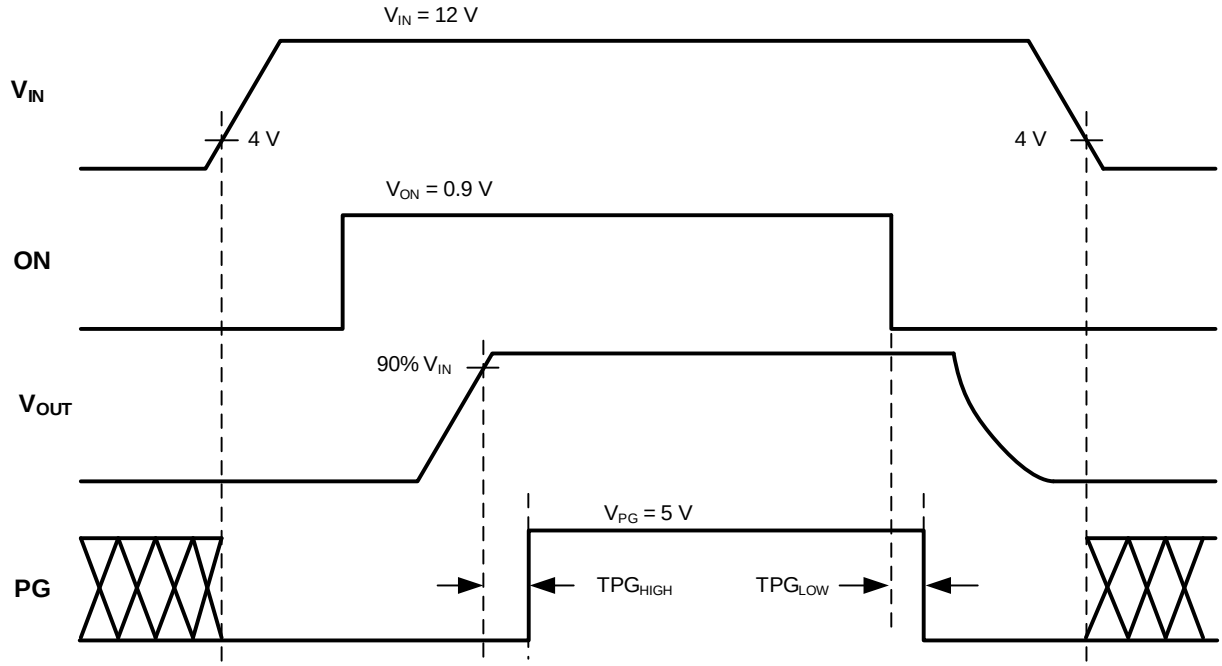


Figure 4. PG Timing Parameter Details

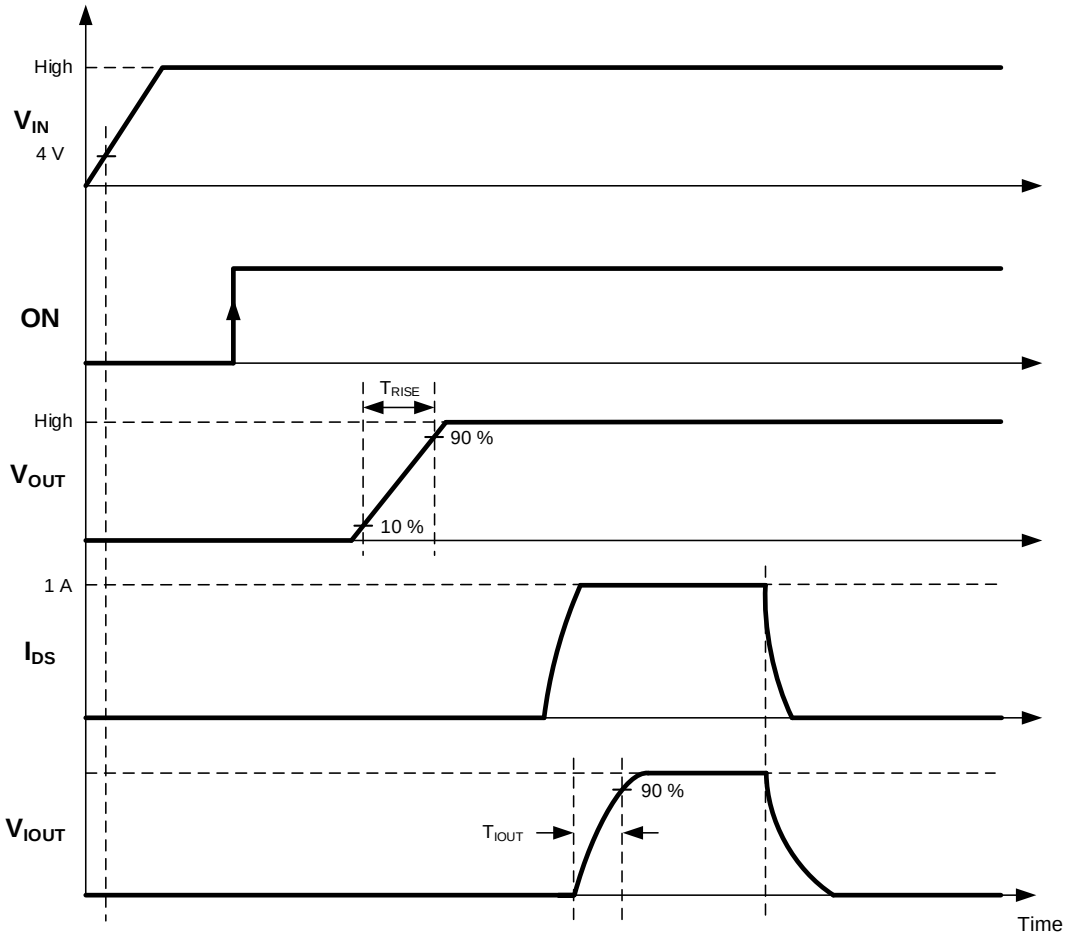


Figure 5. Analog Current Monitor Output Timing Parameter Details

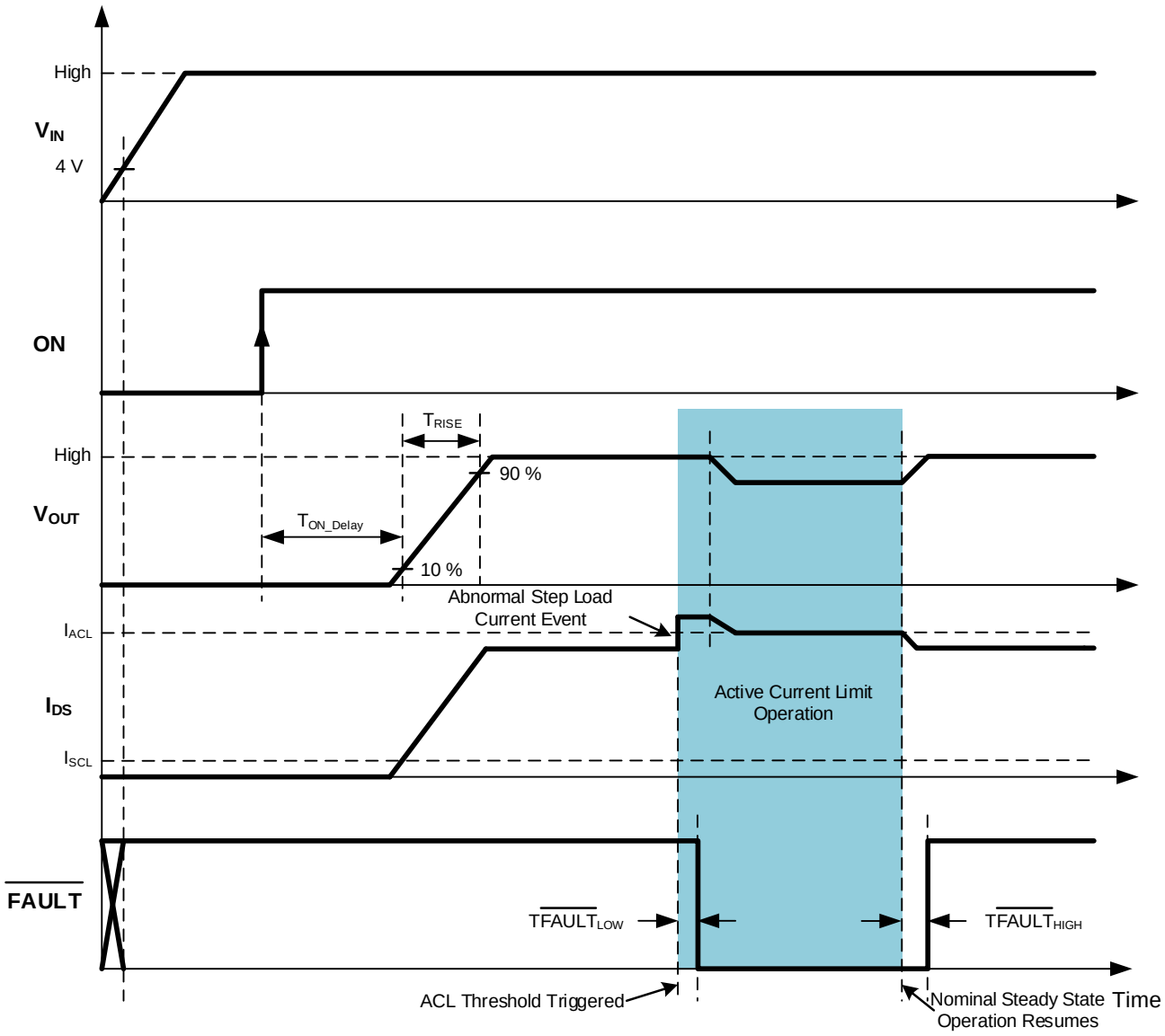


Figure 6. Basic Operation Including Active Current Limit Protection Timing Parameter Details

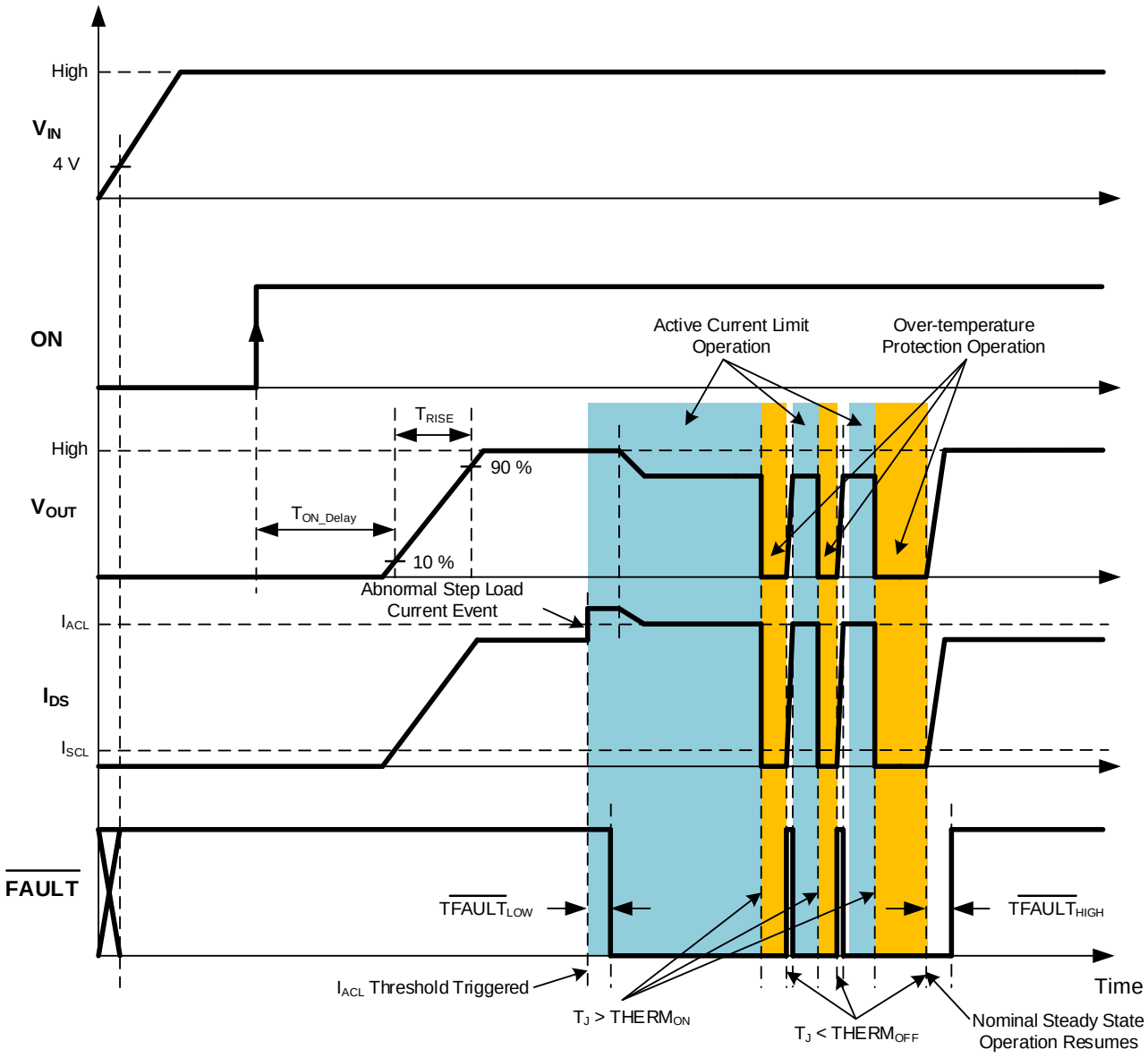


Figure 7. Active Current Limit & Thermal Protection Timing Parameter Details

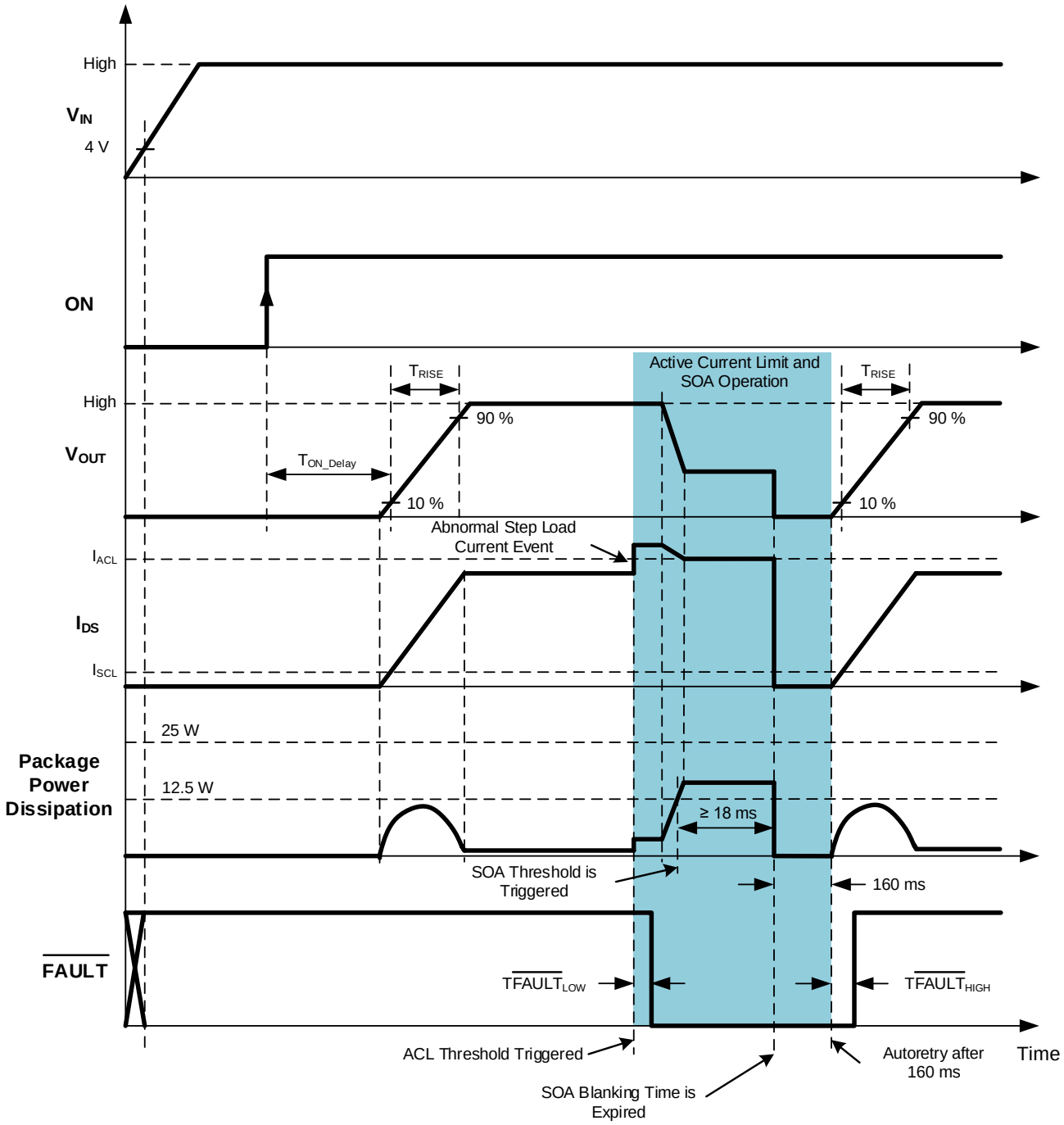


Figure 8. Active Current Limit & 12.5 W SOA Timing Parameter Details

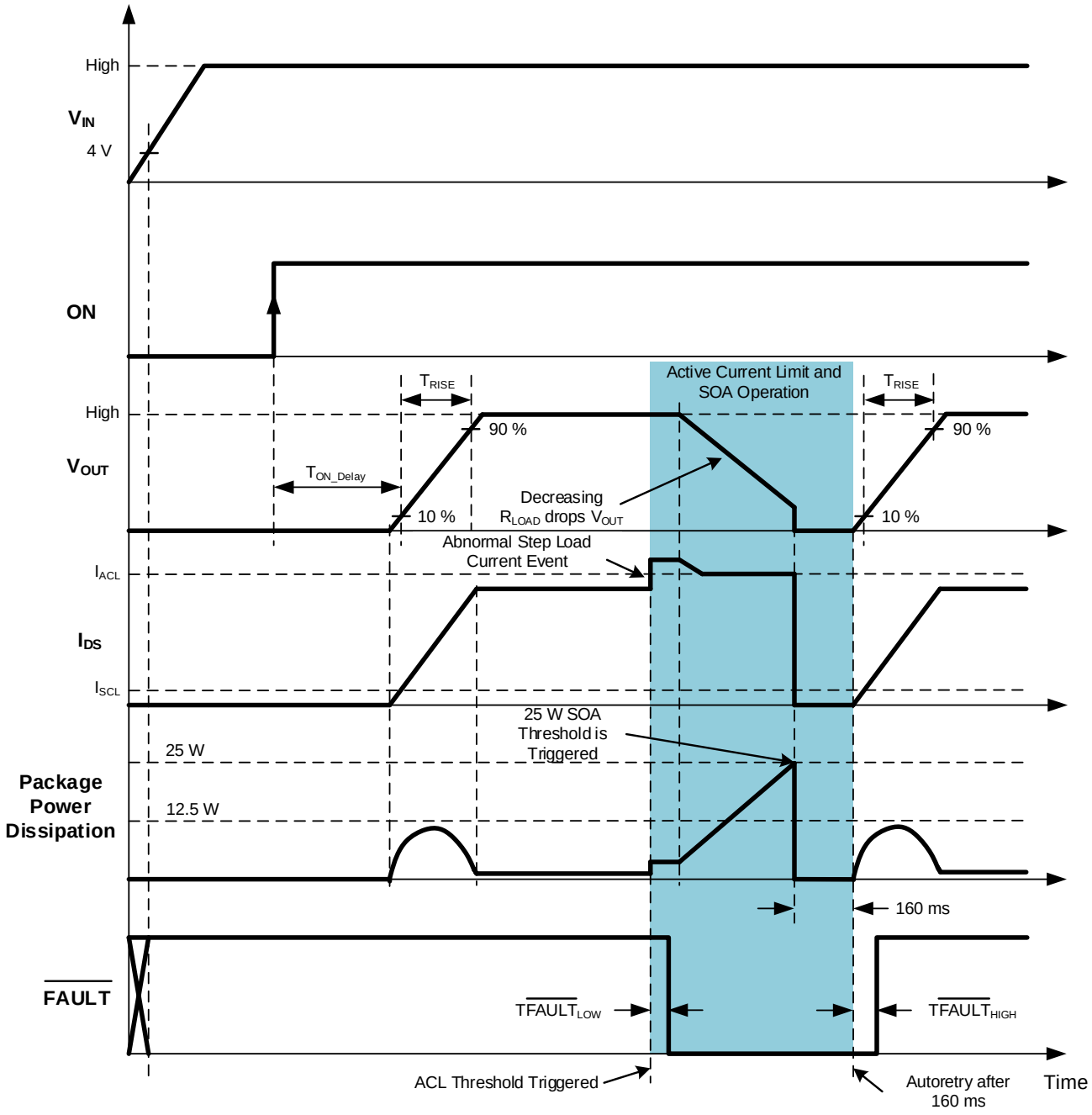


Figure 9. Active Current Limit & 25 W SOA Timing Parameter Details

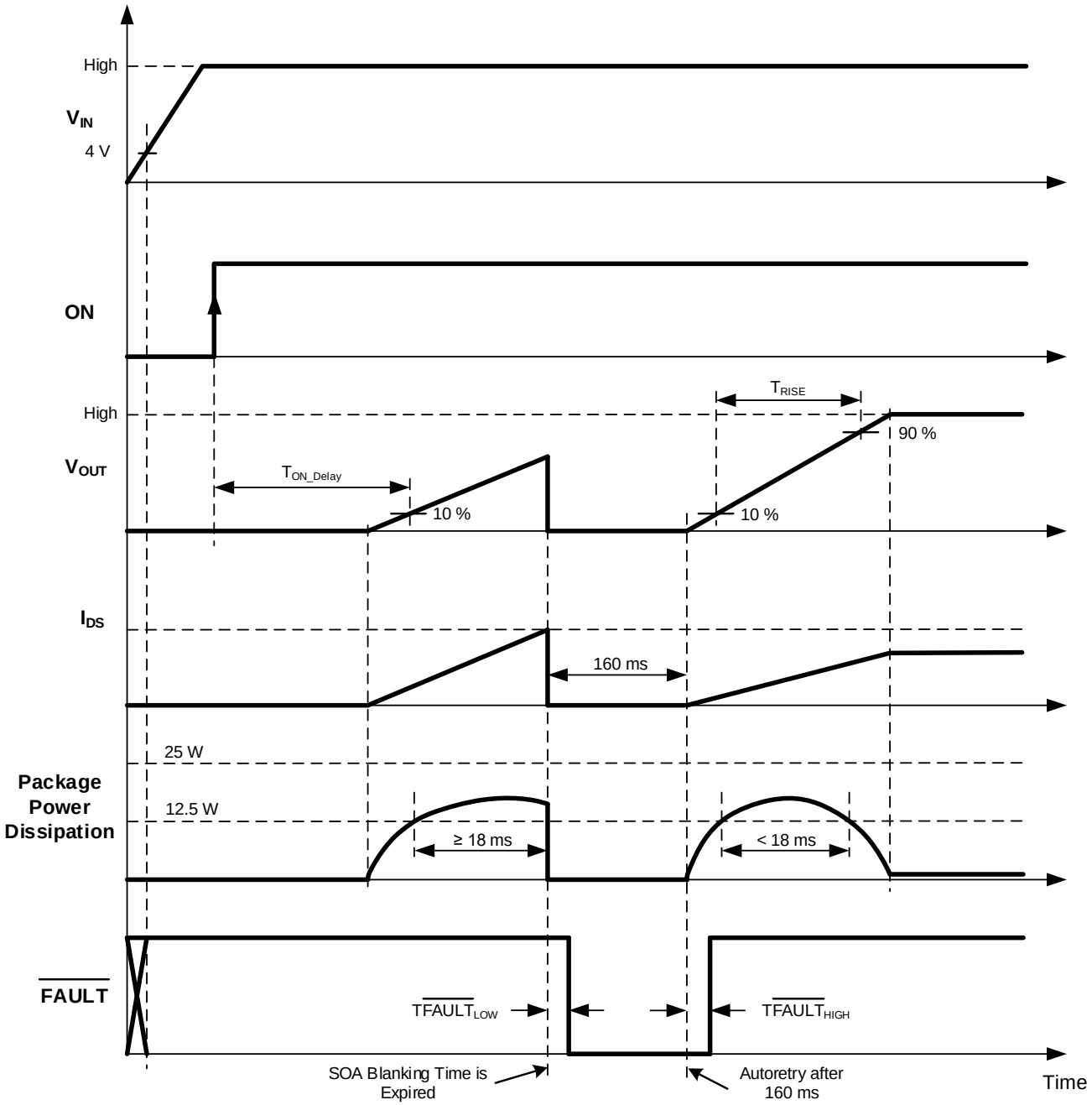


Figure 10. 12.5 W SOA Operation During Power up at Heavy Load Timing Parameter Details

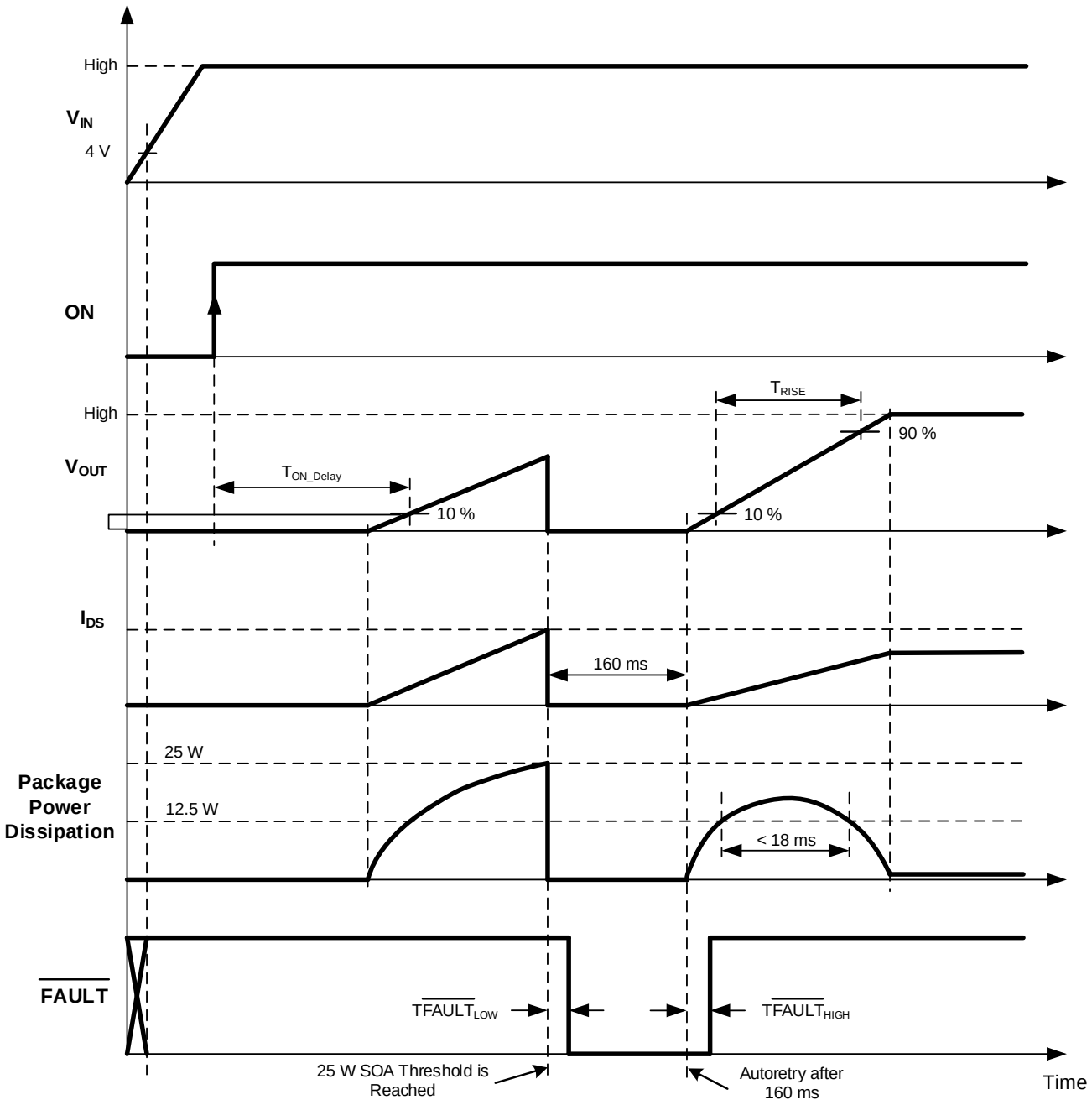


Figure 11. 25 W SOA Operation During Power up at Heavy Load Timing Parameter Details

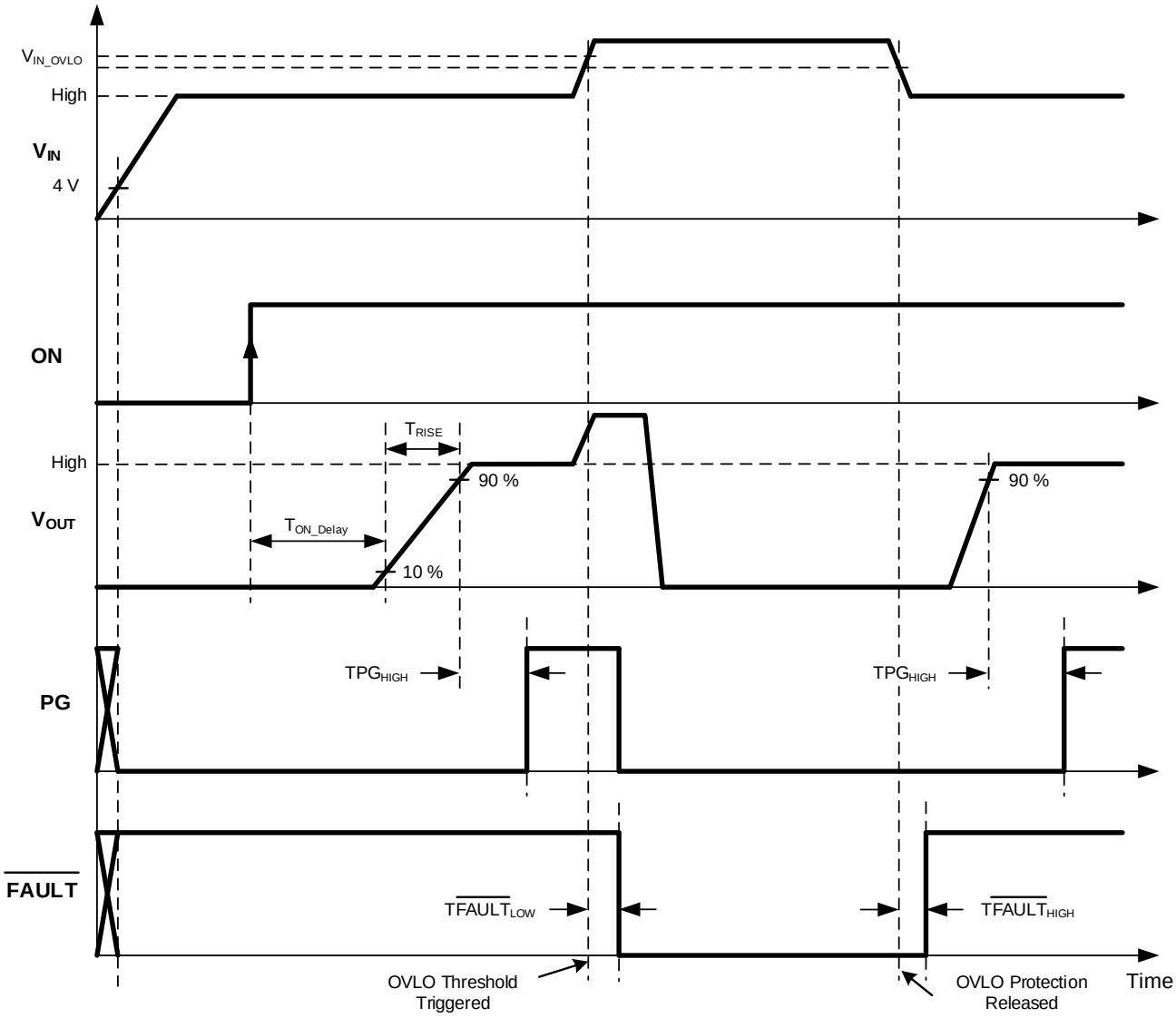


Figure 12. OVLO Timing Parameter Details

3.1 Typical Performance Graphs

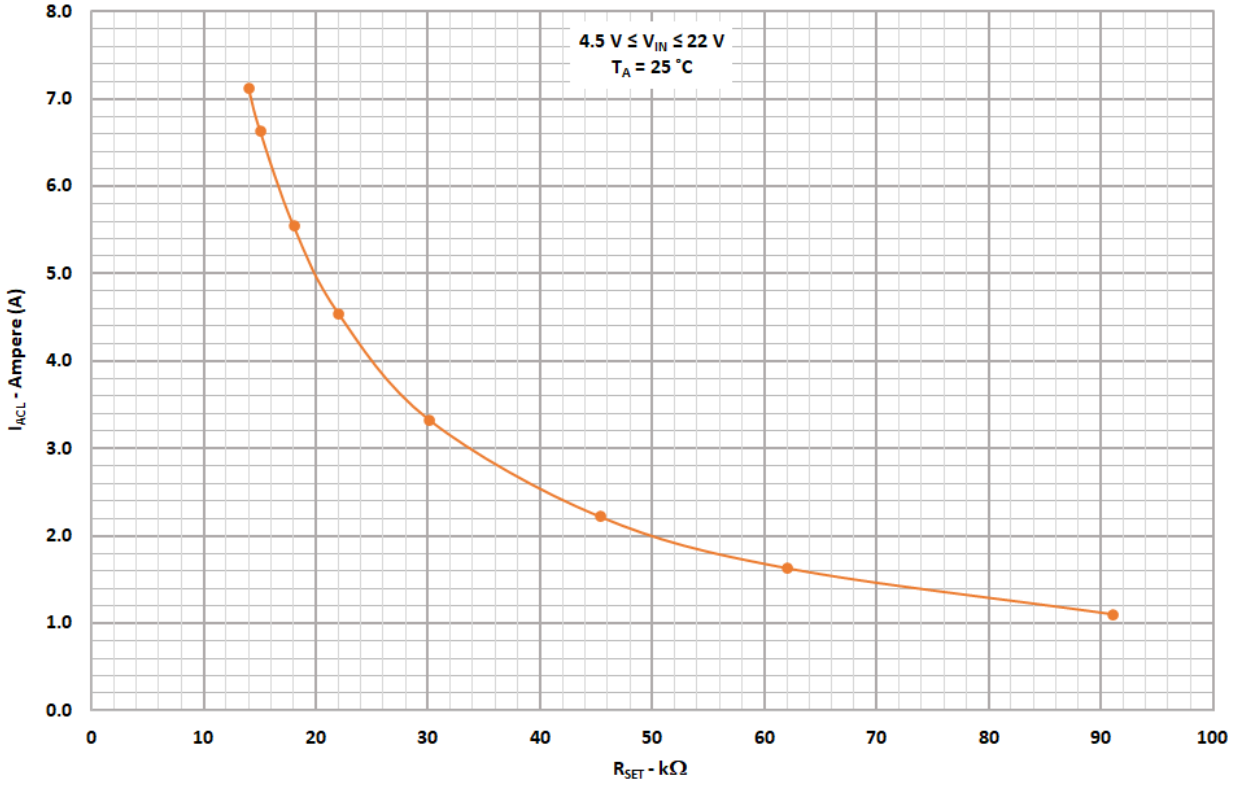


Figure 13. I_{ACL} vs. R_{SET} and V_{IN}

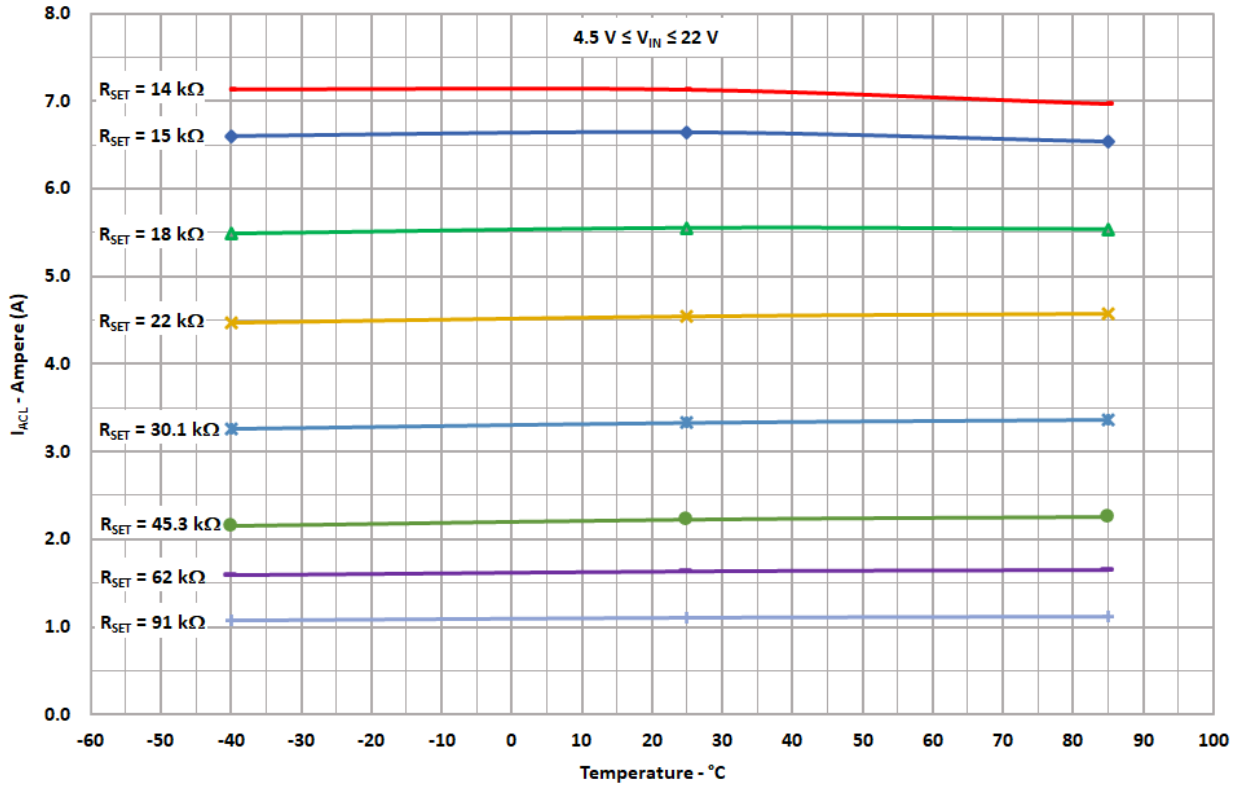


Figure 14. I_{ACL} vs. Temperature, V_{IN}, and R_{SET}

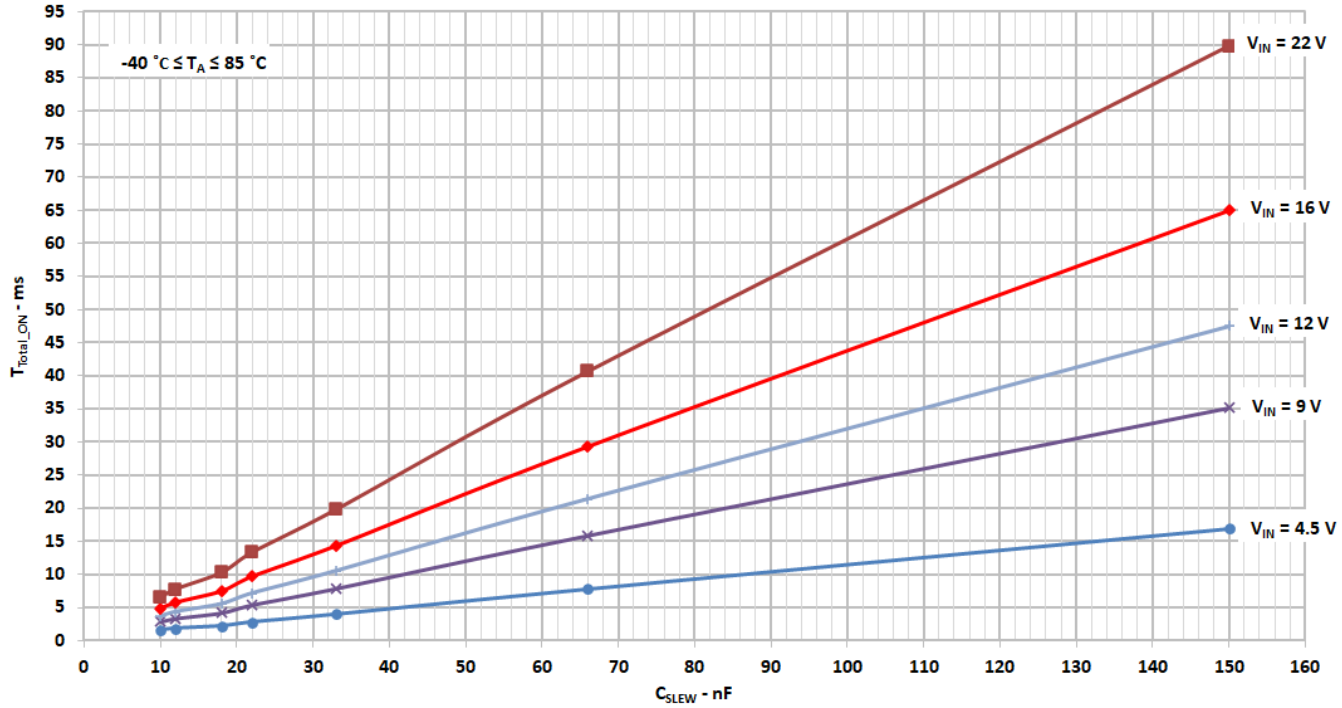


Figure 15. T_{Total_ON} vs. C_{SLEW}, V_{IN}, and Temperature

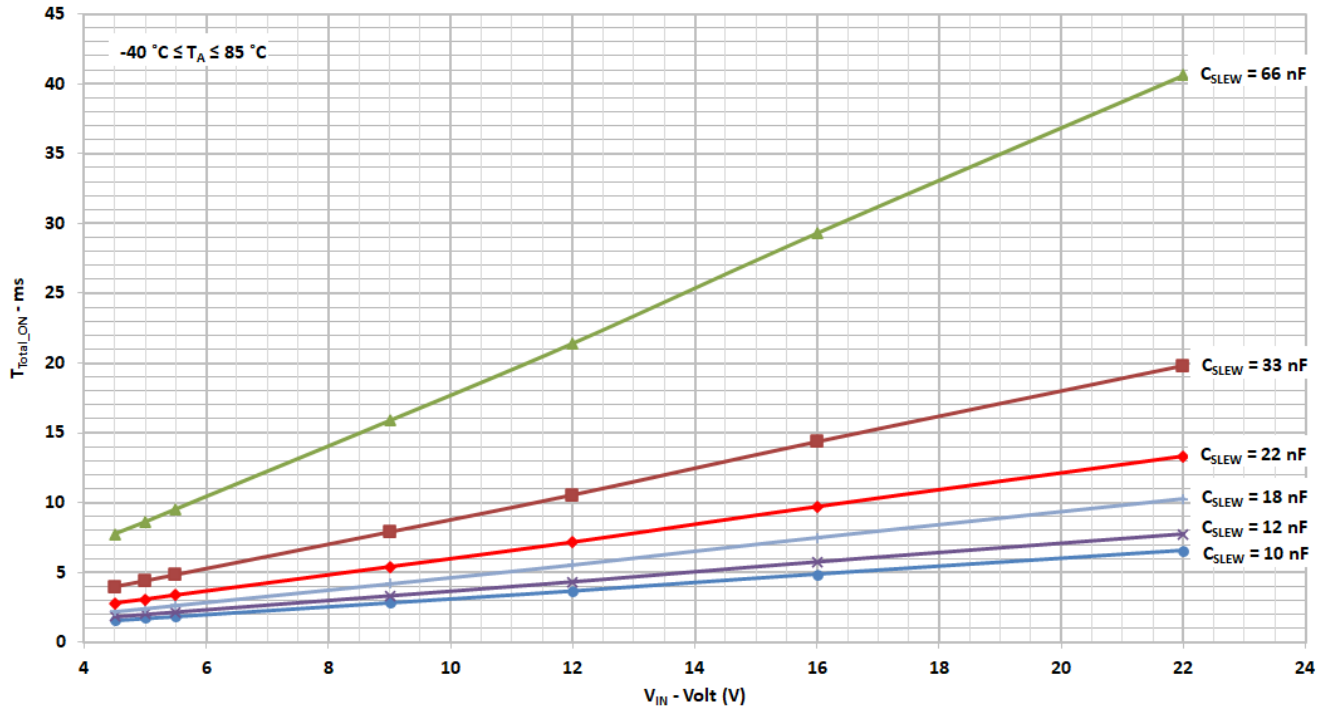


Figure 16. T_{Total_ON} vs. V_{IN}, C_{SLEW}, and Temperature

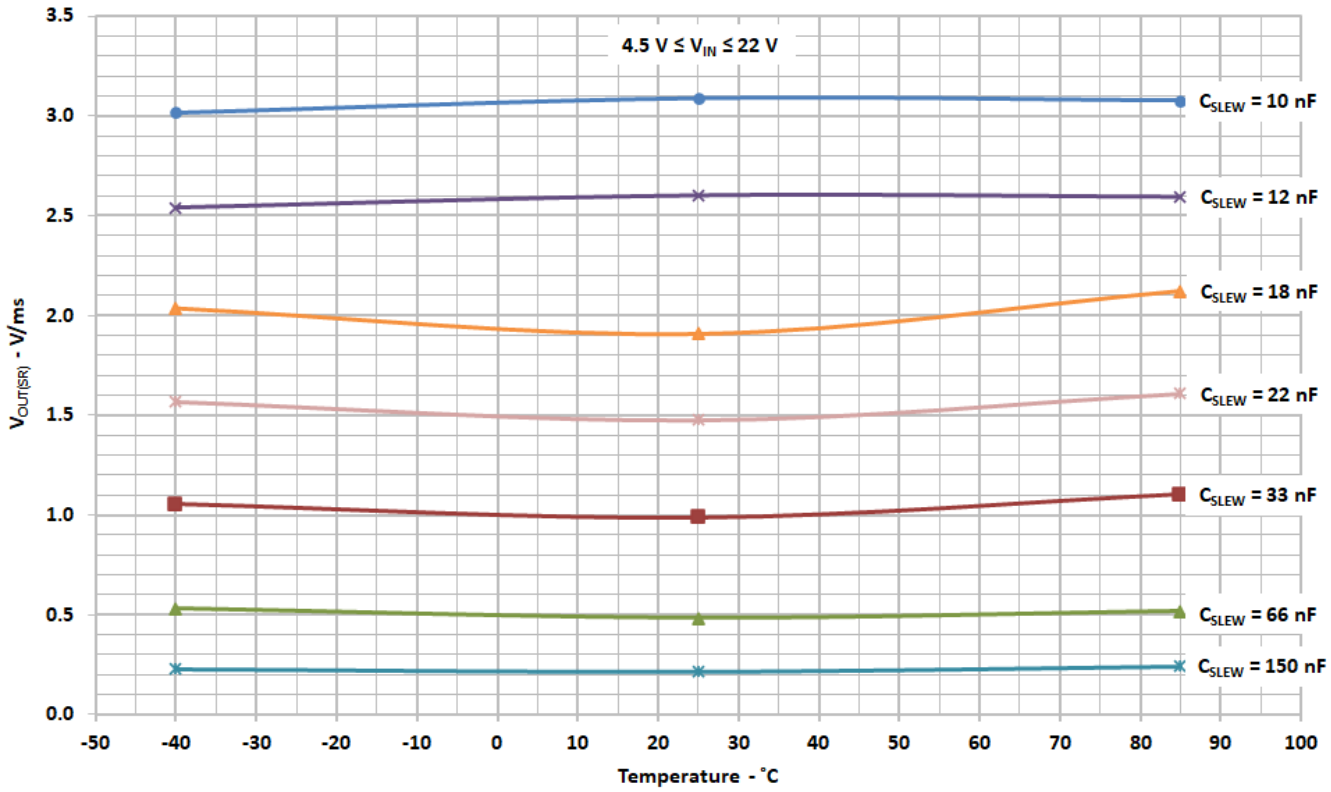


Figure 17. V_{OUT} Slew Rate vs. Temperature, V_{IN}, and C_{SLEW}

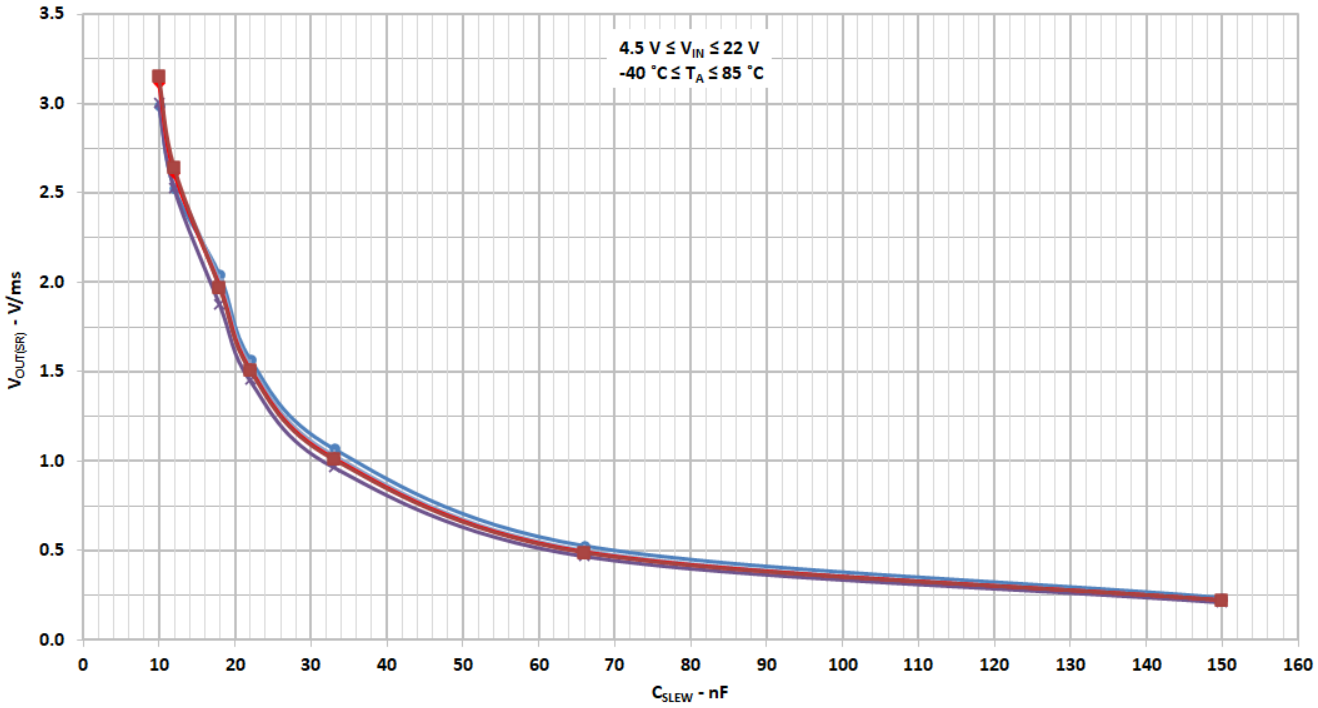


Figure 18. V_{OUT} Slew Rate vs. C_{SLEW}, V_{IN}, and Temperature

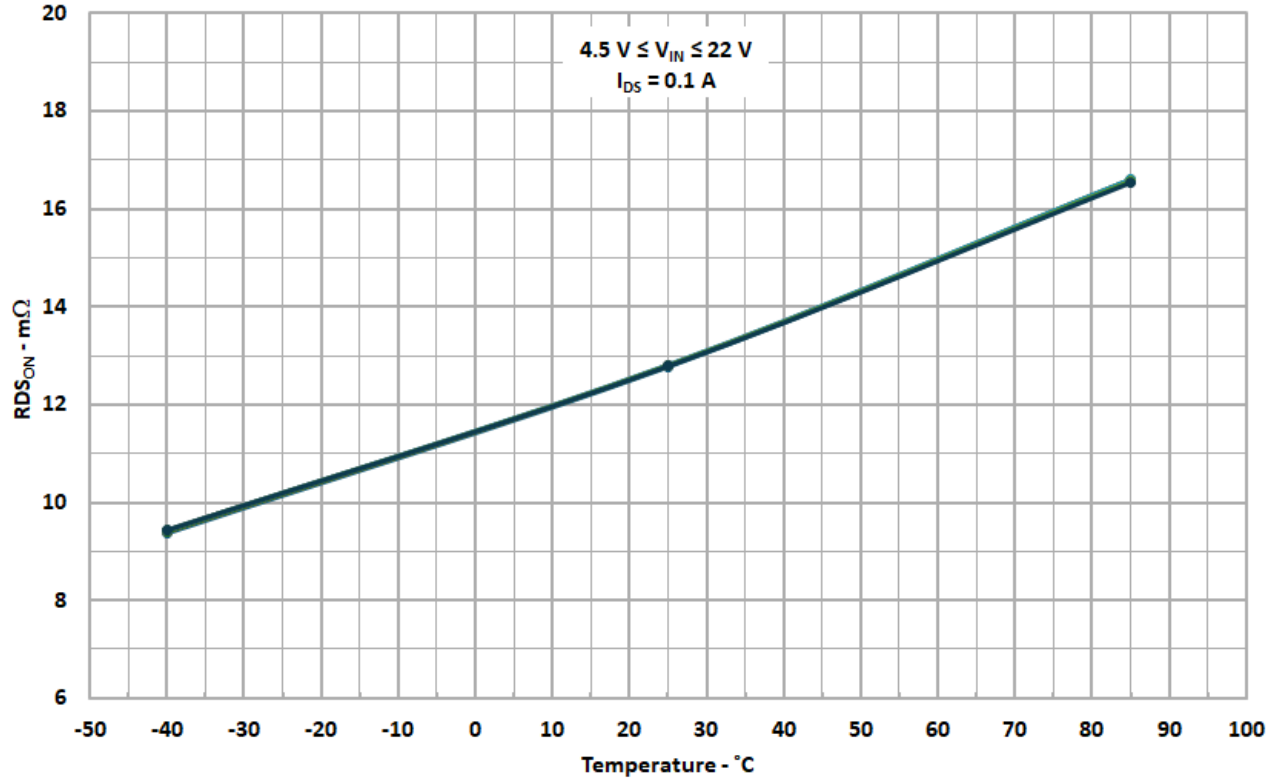


Figure 19. RDS_{ON} vs. Temperature and V_{IN}

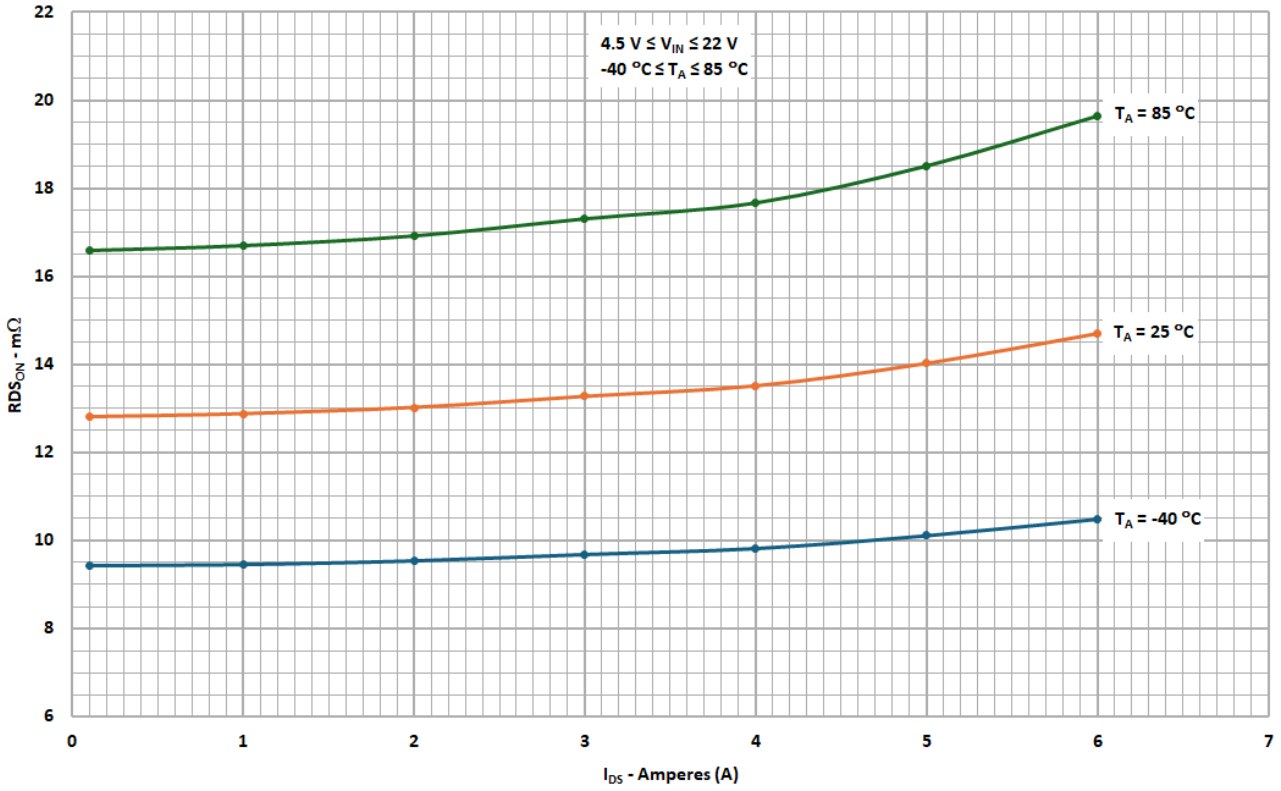


Figure 20. RDS_{ON} vs. I_{DS}, Temperature, and V_{IN}

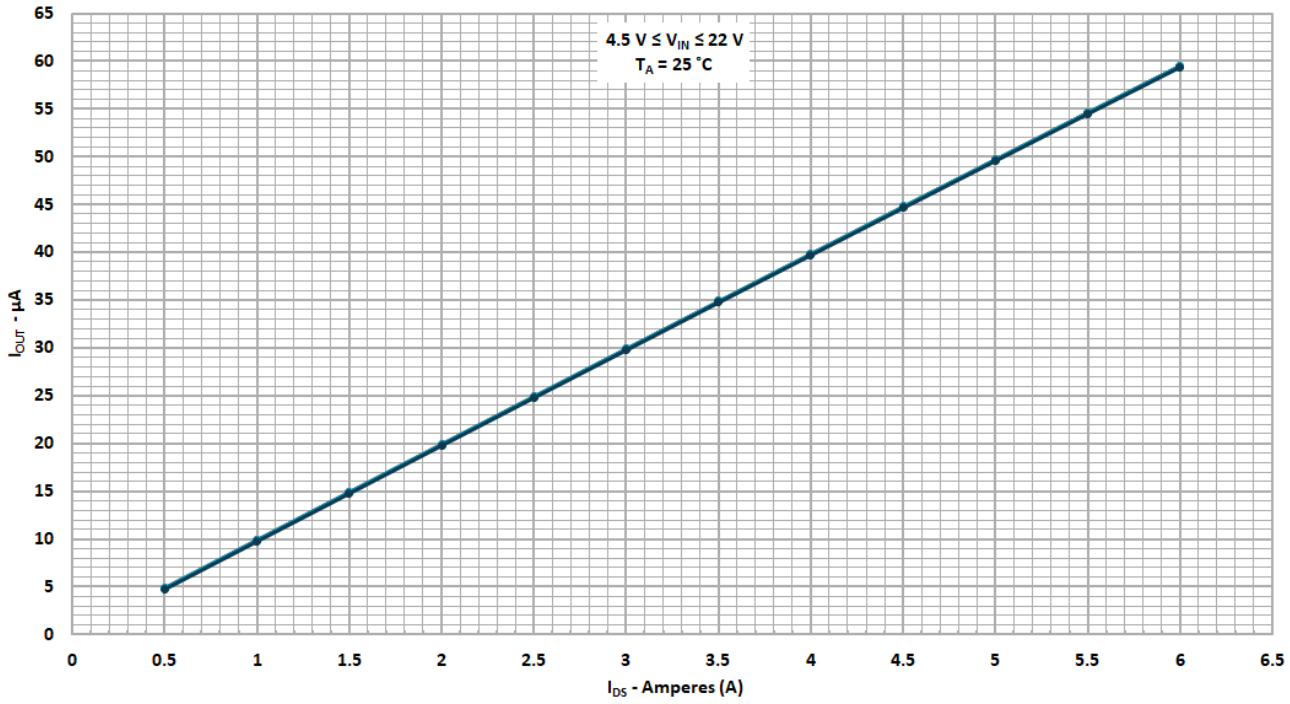


Figure 21. I_{OUT} vs. I_{DS} and V_{IN}

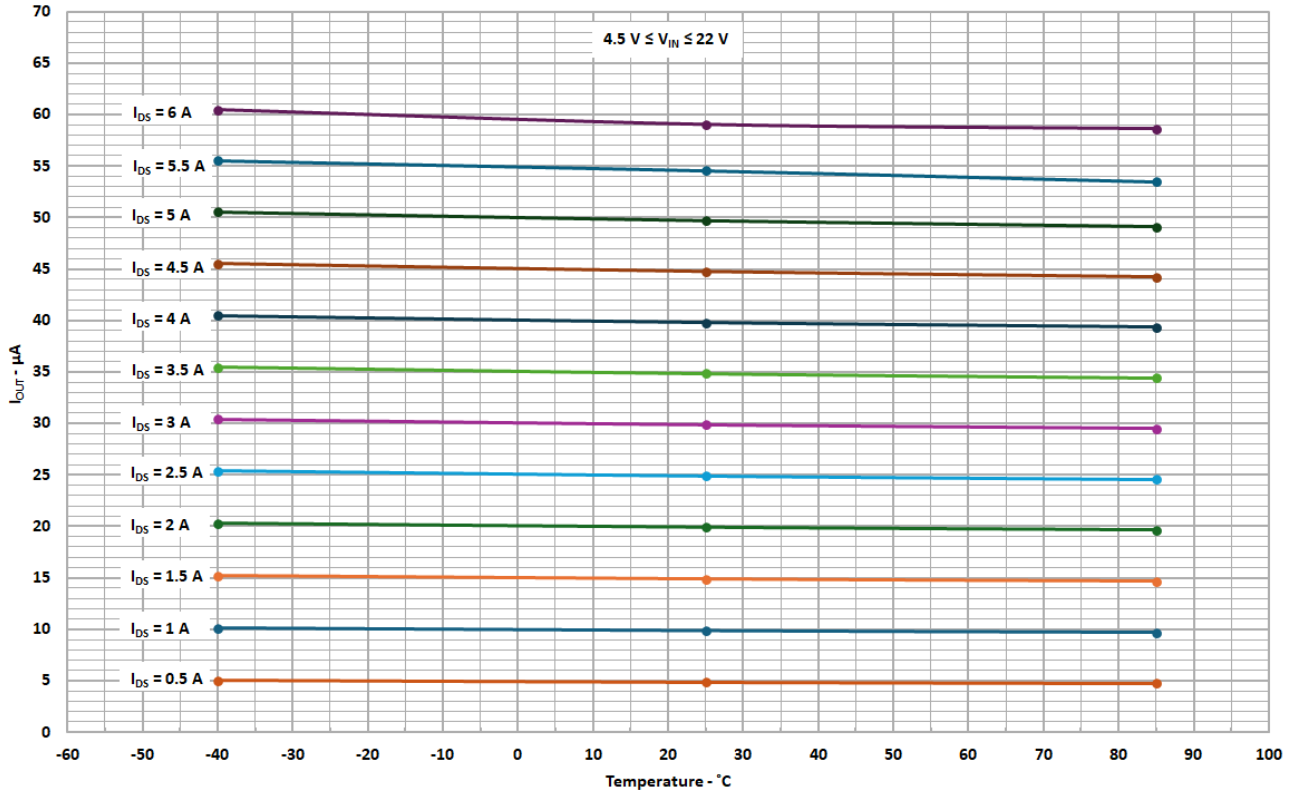
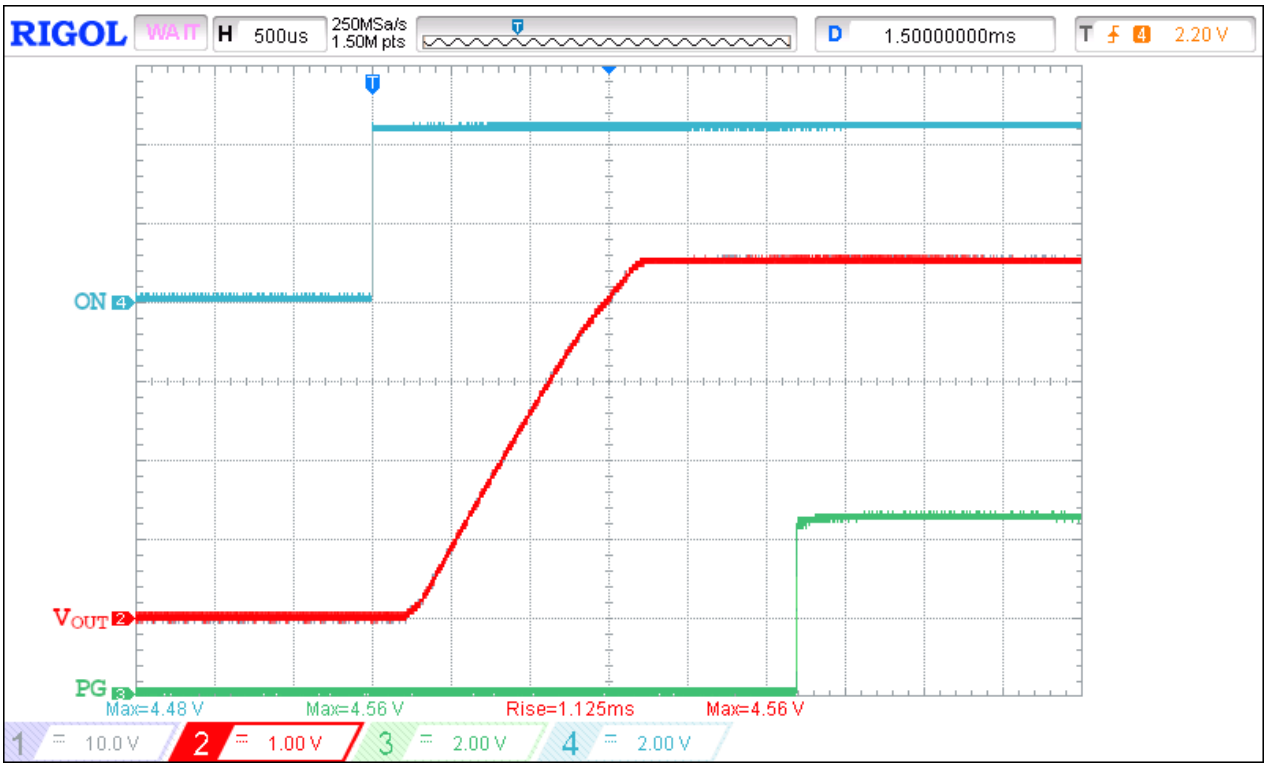


Figure 22. I_{OUT} vs. Temperature, I_{DS}, and V_{IN}

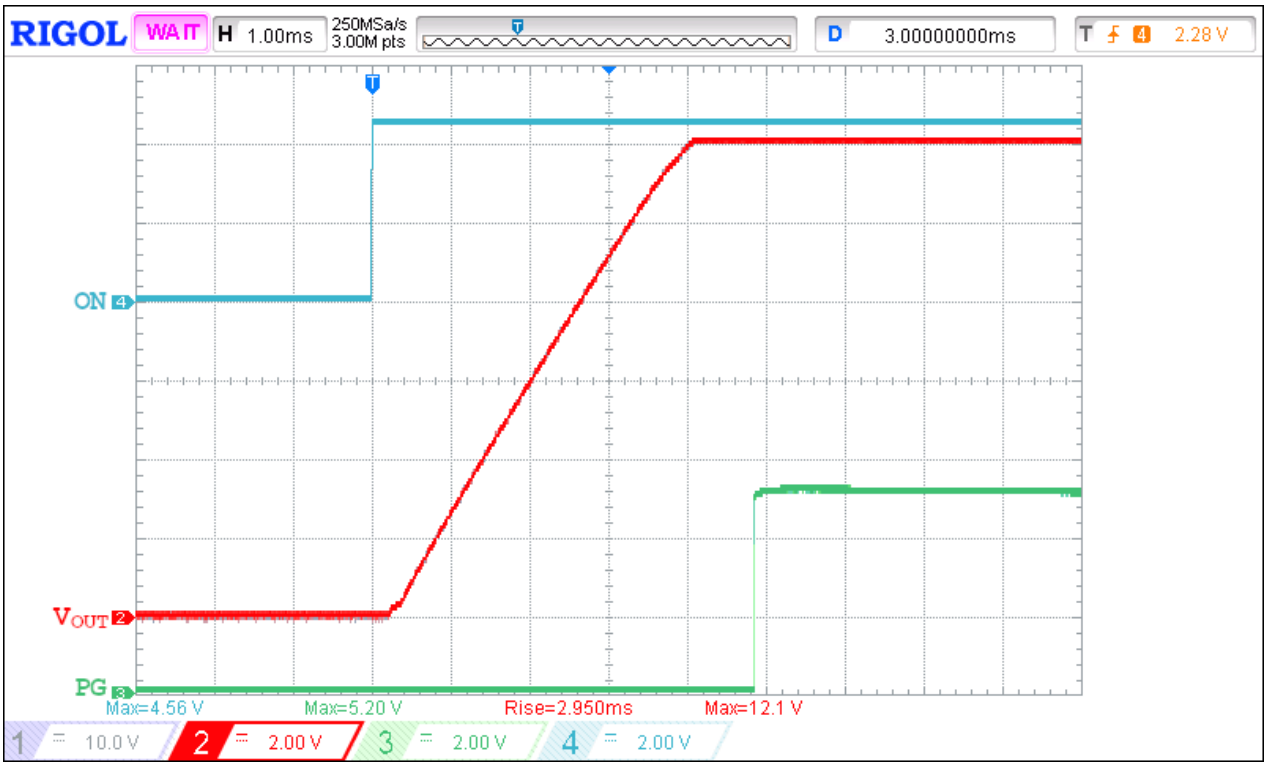
3.2 Typical Operation Waveforms

3.2.1. Typical Turn ON and Power Good Operation Waveforms



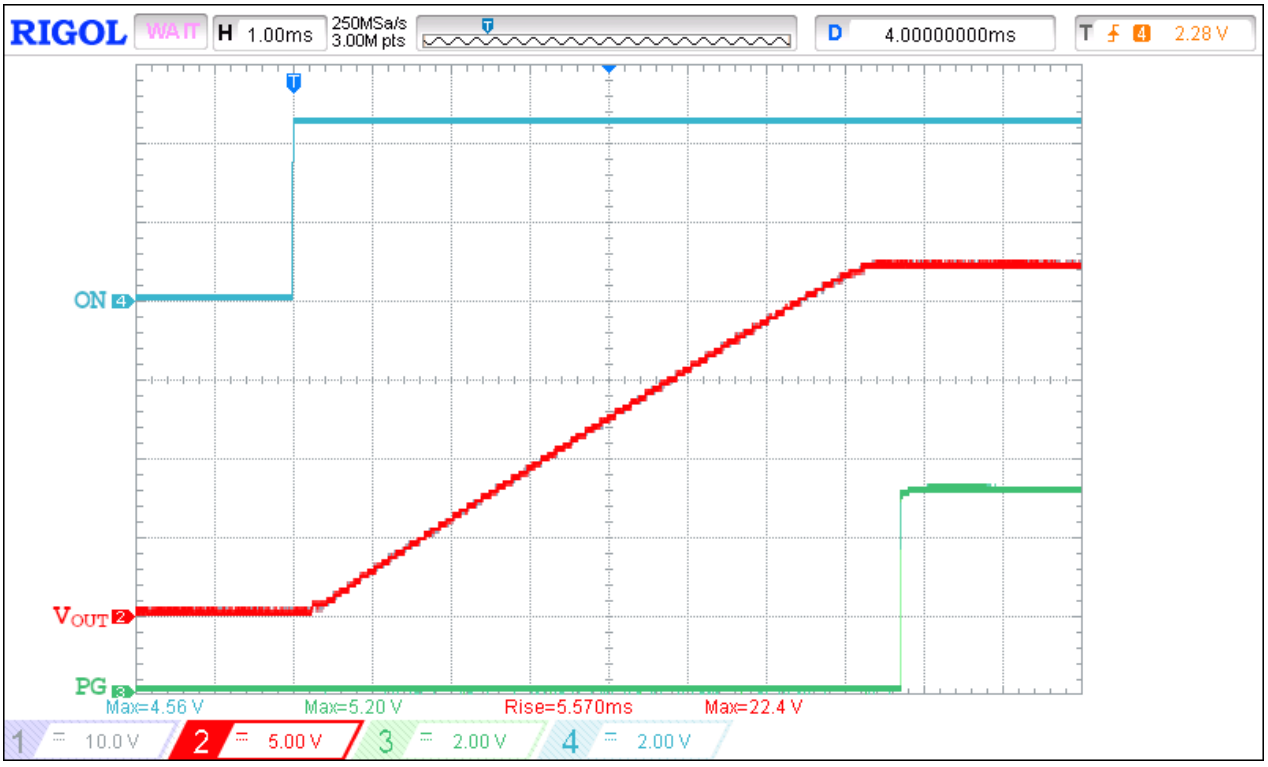
Conditions: C_{SLEW} = 10 nF, C_{LOAD} = 10 µF, R_{LOAD} = 100 Ω.

Figure 23. Turn ON and Power Good Operation Waveform for V_{IN} = 4.5 V



Conditions: C_{SLEW} = 10 nF, C_{LOAD} = 10 µF, R_{LOAD} = 100 Ω.

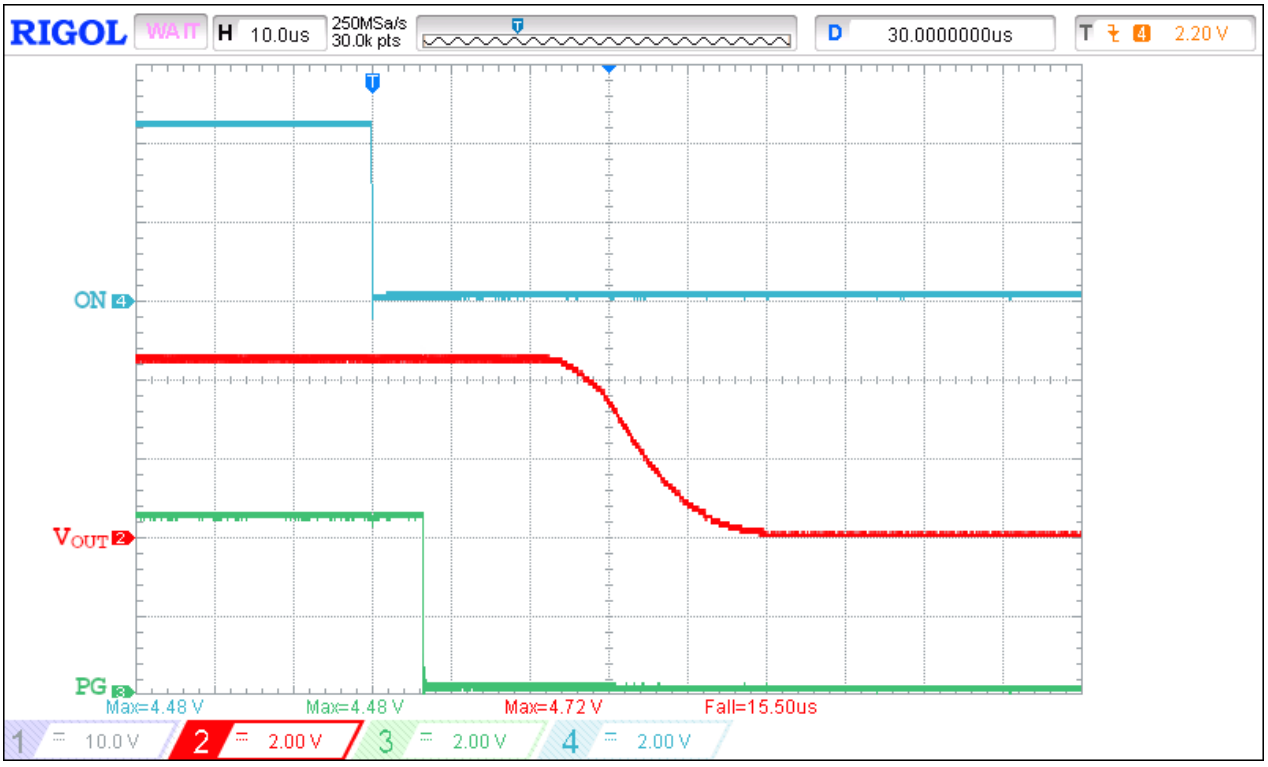
Figure 24. Turn ON and Power Good Operation Waveform for V_{IN} = 12 V



Conditions: C_{SLEW} = 10 nF, C_{LOAD} = 10 µF, R_{LOAD} = 100 Ω.

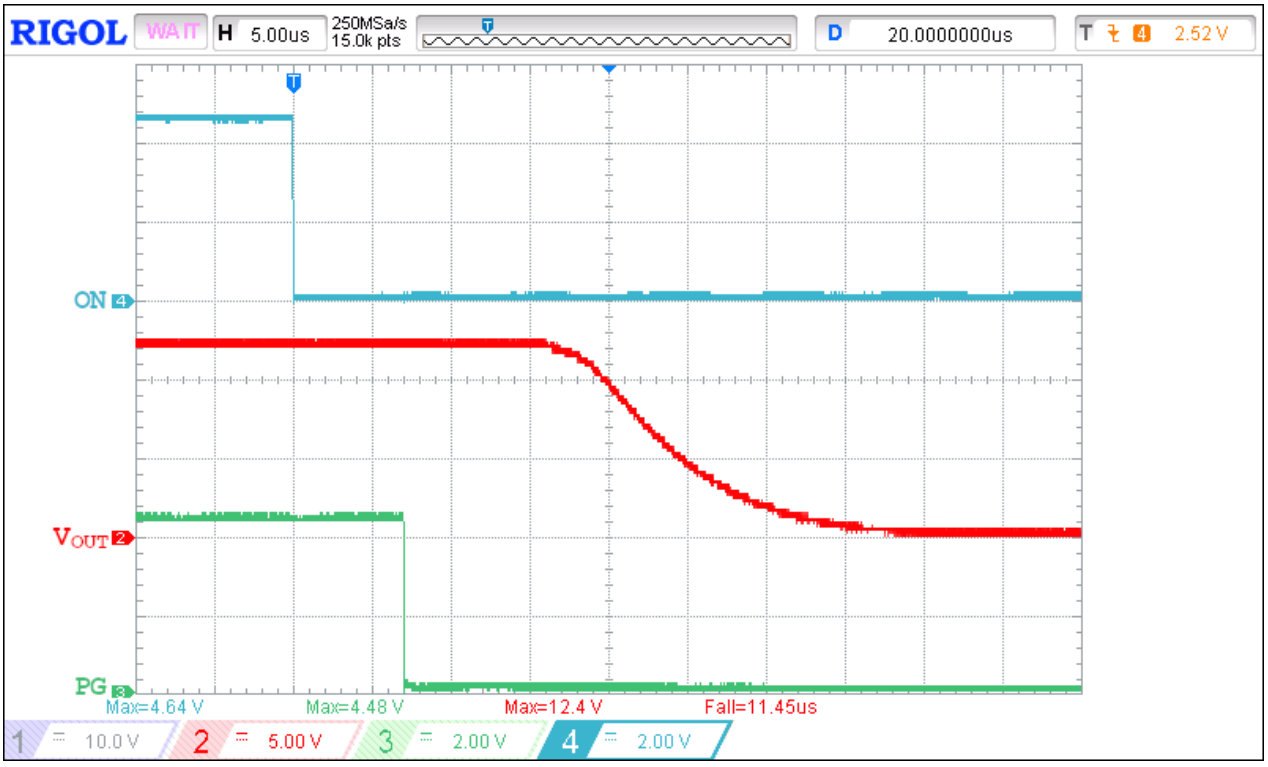
Figure 25. Turn ON and Power Good Operation Waveform for V_{IN} = 22 V

3.2.2. Typical Turn OFF Operation Waveforms



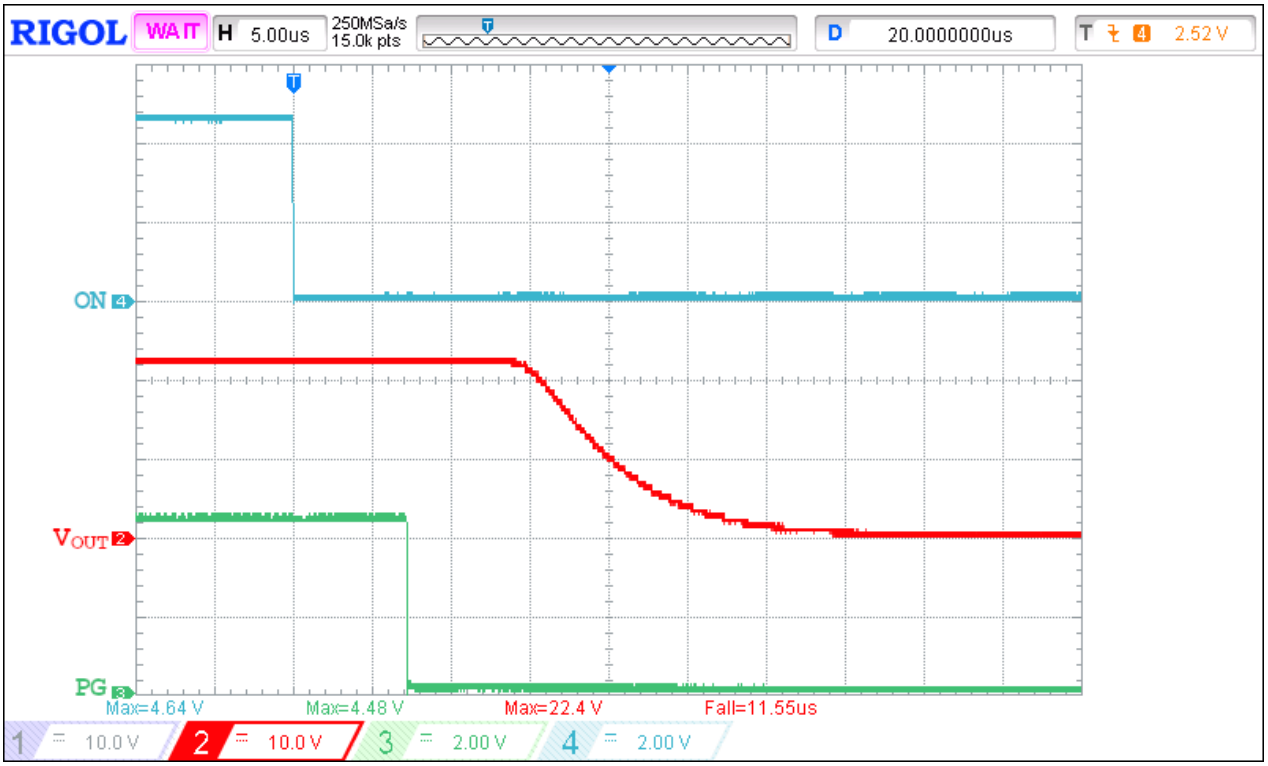
Conditions: C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, No C_{LOAD}.

Figure 26. Turn OFF Operation Waveform for V_{IN} = 4.5 V



Conditions: C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, No C_{LOAD}.

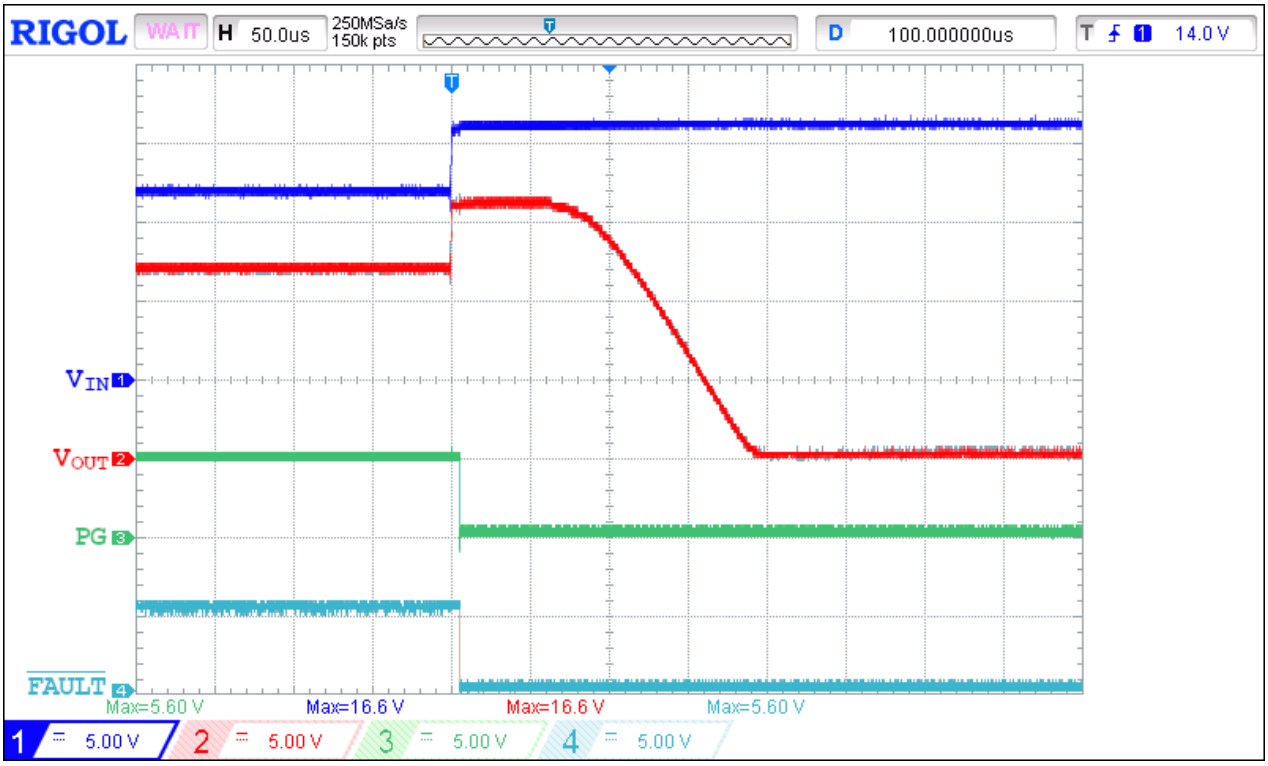
Figure 27. Turn OFF Operation Waveform for V_{IN} = 12 V



Conditions: C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, No C_{LOAD}.

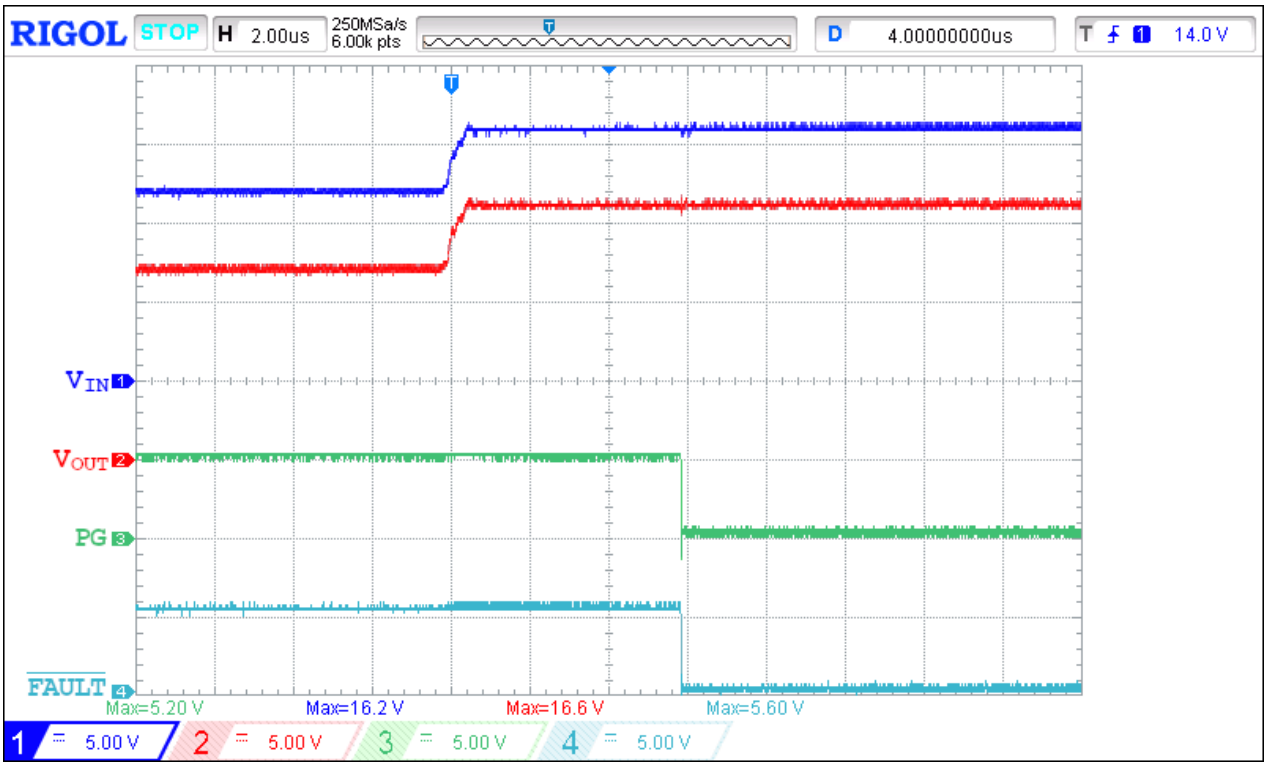
Figure 28. Turn OFF Operation Waveform for V_{IN} = 22 V

3.2.3. Typical Overvoltage Protection Operation Waveforms



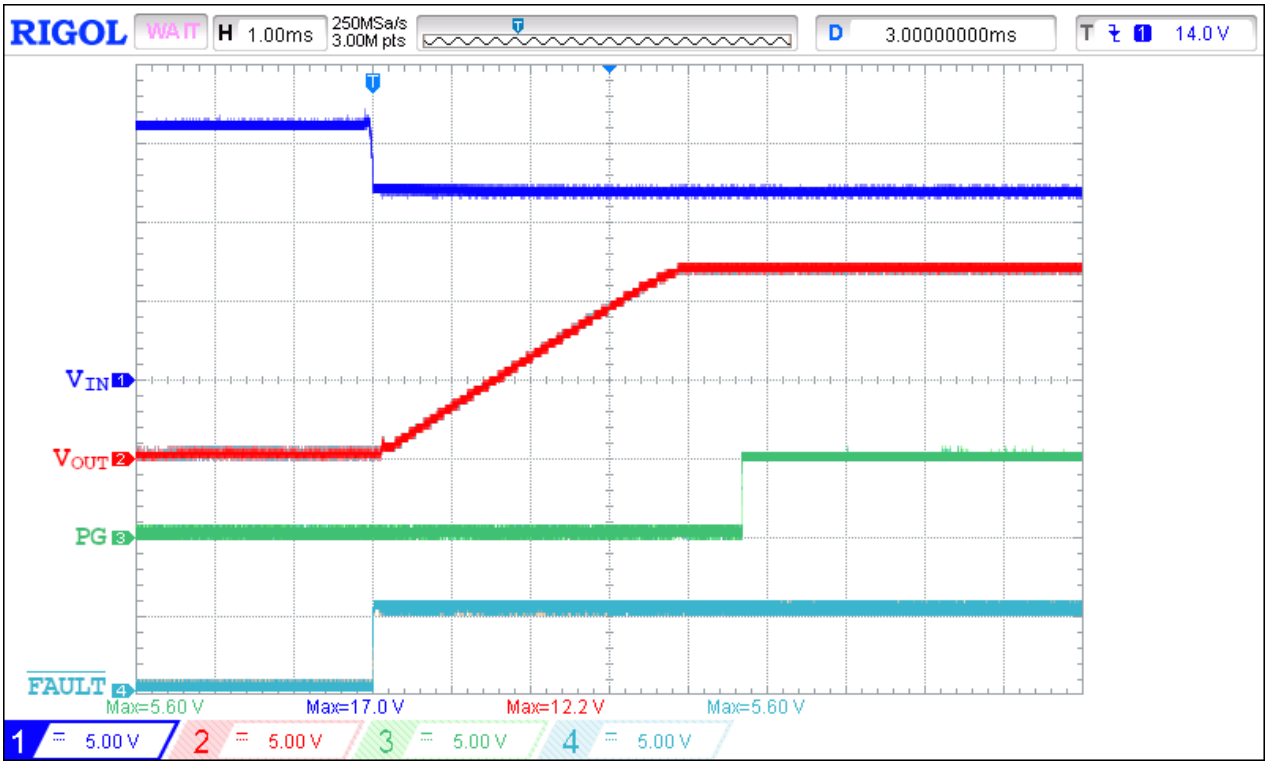
Conditions: SEL = Low, C_{SLEW} = 10 nF, No C_{LOAD}, R_{LOAD} = 1 kΩ.

Figure 29. OVLO Operation Waveform for V_{IN} = 12 V → 16 V



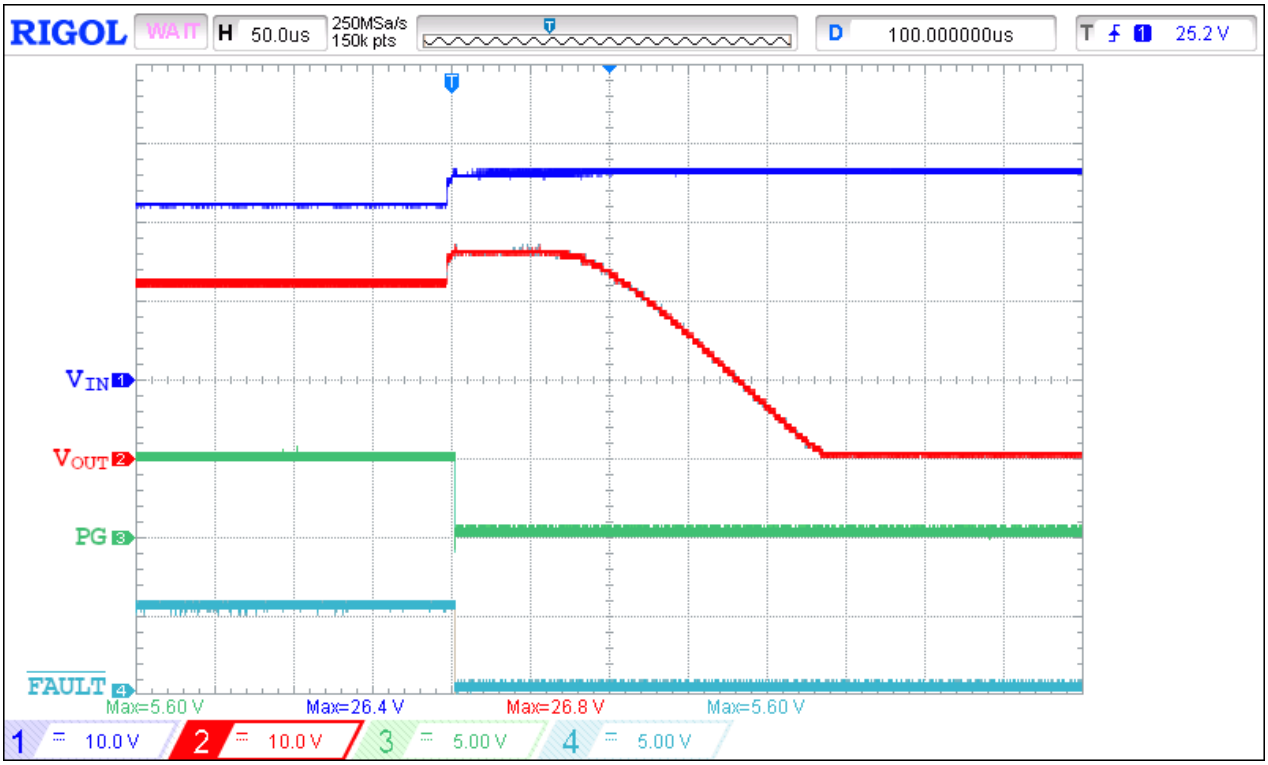
Conditions: SEL = Low, C_{SLEW} = 10 nF, No C_{LOAD}, R_{LOAD} = 1 kΩ.

Figure 30. OVLO Operation Waveform for V_{IN} = 12 V → 16 V (Extended View)



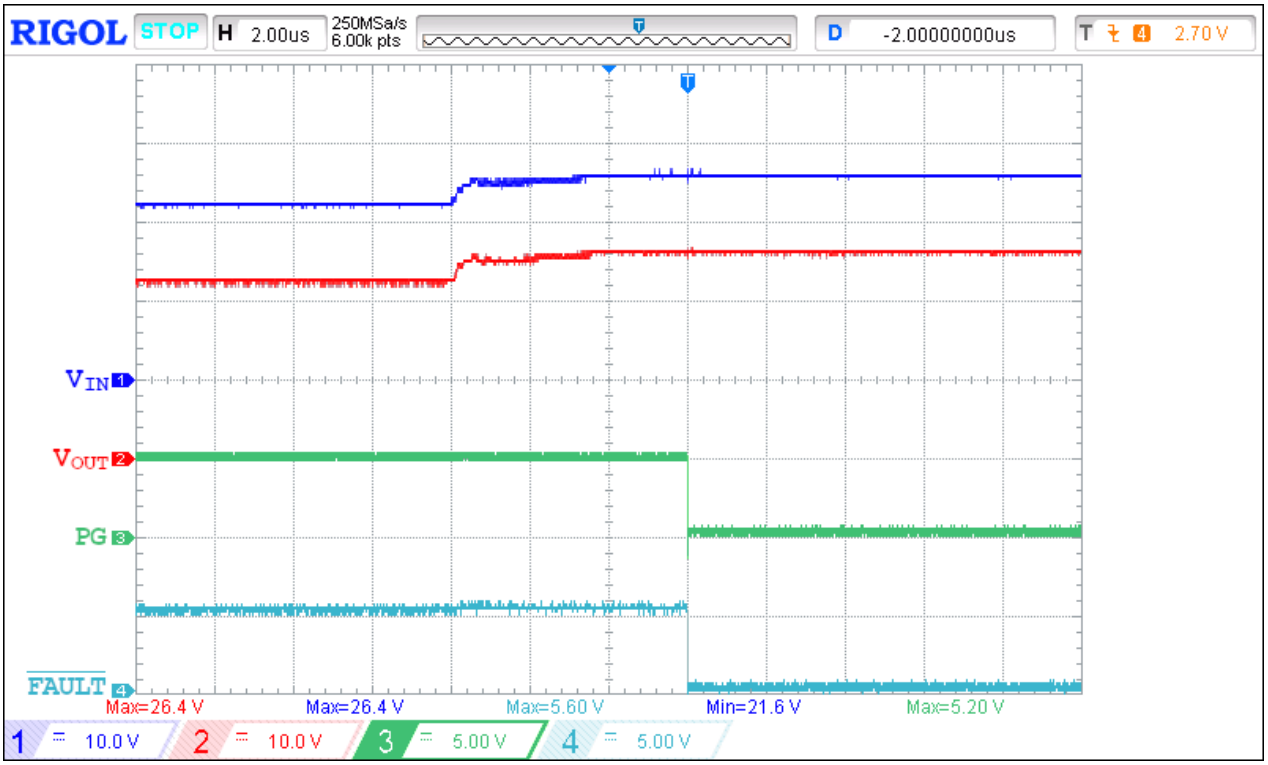
Conditions: SEL = Low, C_{SLEW} = 10 nF, No C_{LOAD}, R_{LOAD} = 1 kΩ.

Figure 31. OVLO Operation Waveform for V_{IN} = 16 V → 12 V



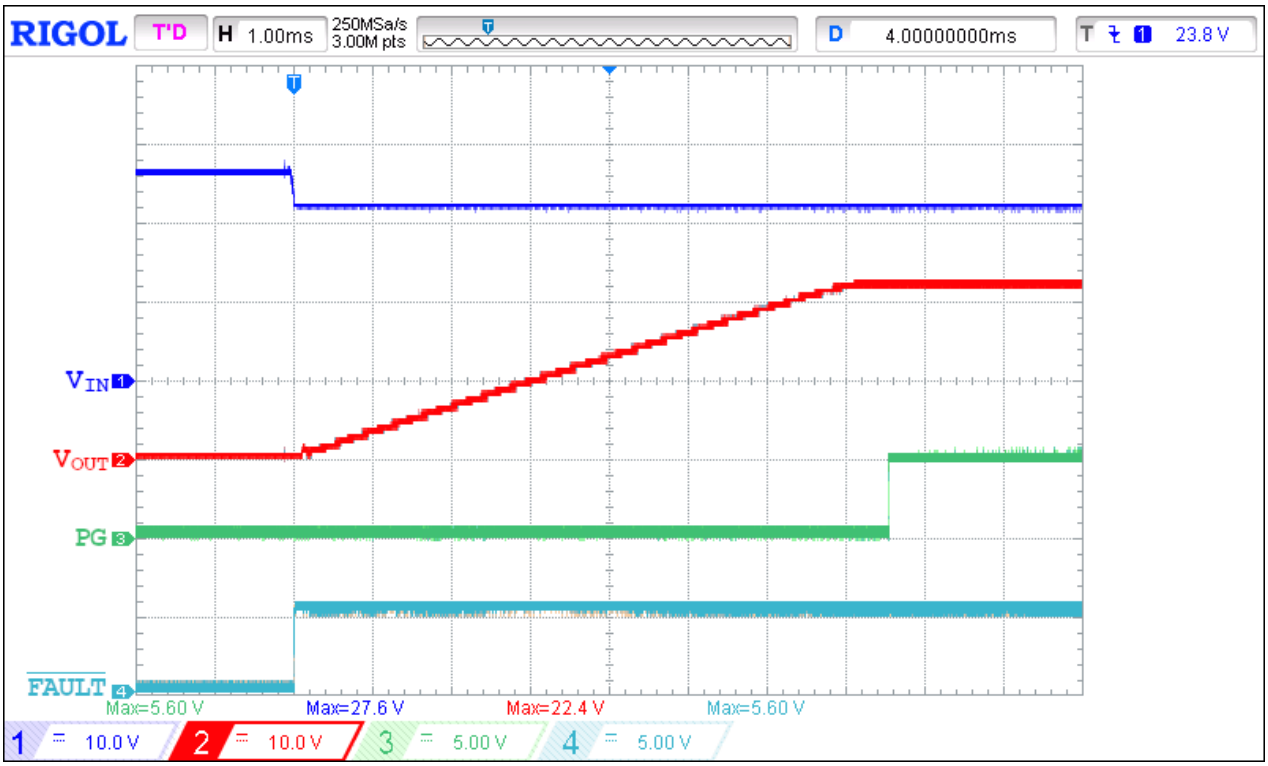
Conditions: SEL = High, C_{SLEW} = 10 nF, No C_{LOAD}, R_{LOAD} = 1 kΩ.

Figure 32. OVLO Operation Waveform for V_{IN} = 22 V → 26 V



Conditions: SEL = High, C_{SLEW} = 10 nF, No C_{LOAD}, R_{LOAD} = 1 kΩ.

Figure 33. OVLO Operation Waveform for V_{IN} = 22 V → 26 V (Extended View)



Conditions: SEL = High, C_{SLEW} = 10 nF, No C_{LOAD}, R_{LOAD} = 1 kΩ.

Figure 34. OVLO Operation Waveform for V_{IN} = 26 V → 22 V

3.2.4. Typical Active Current Limit Operation Waveforms

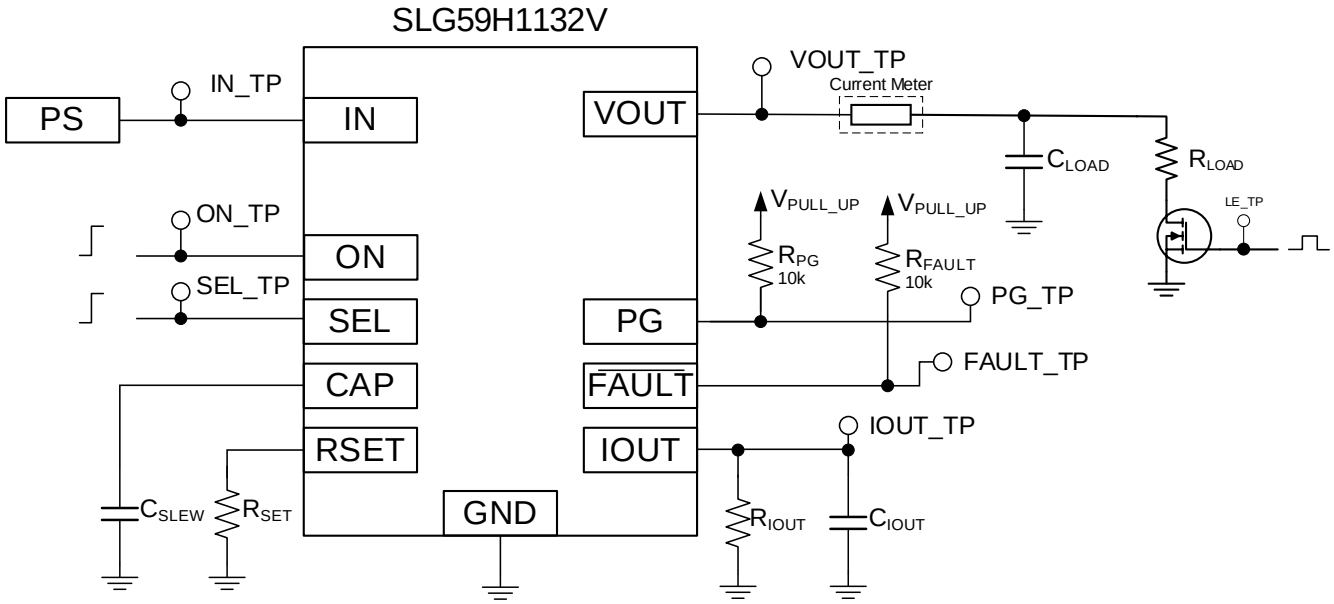
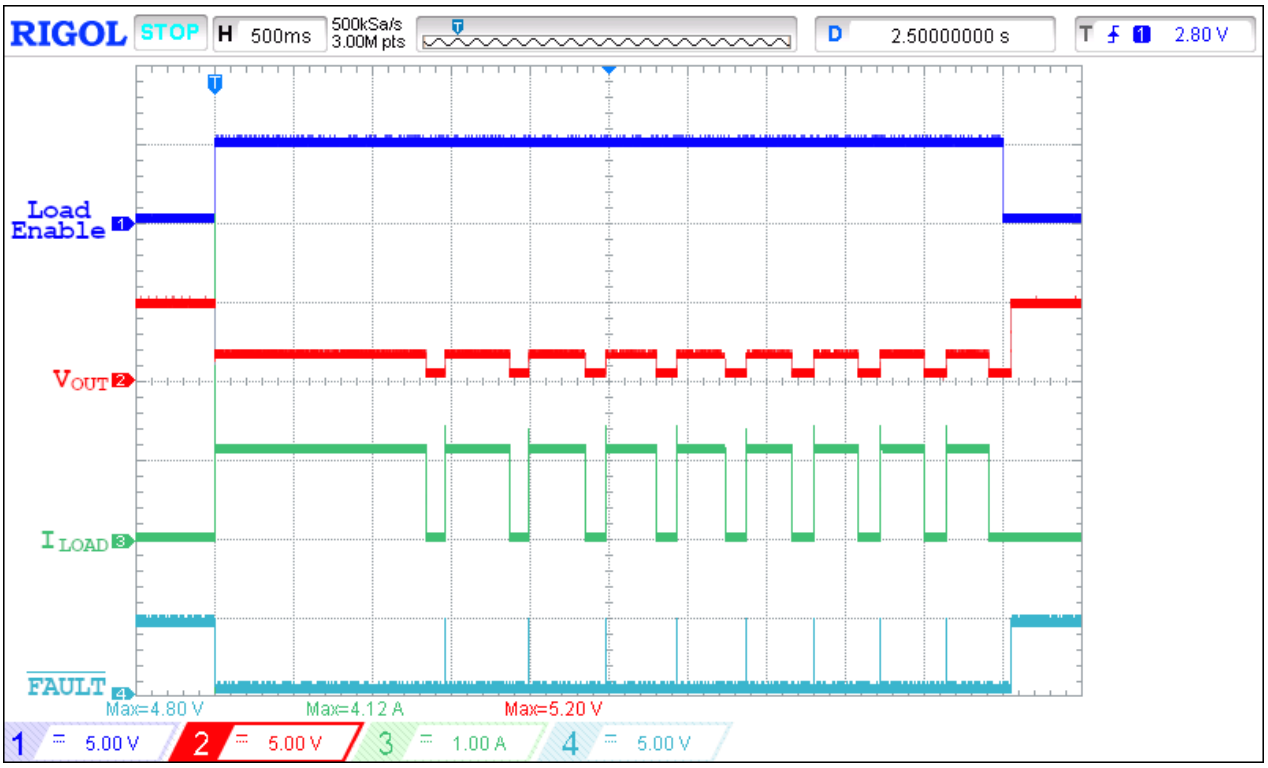
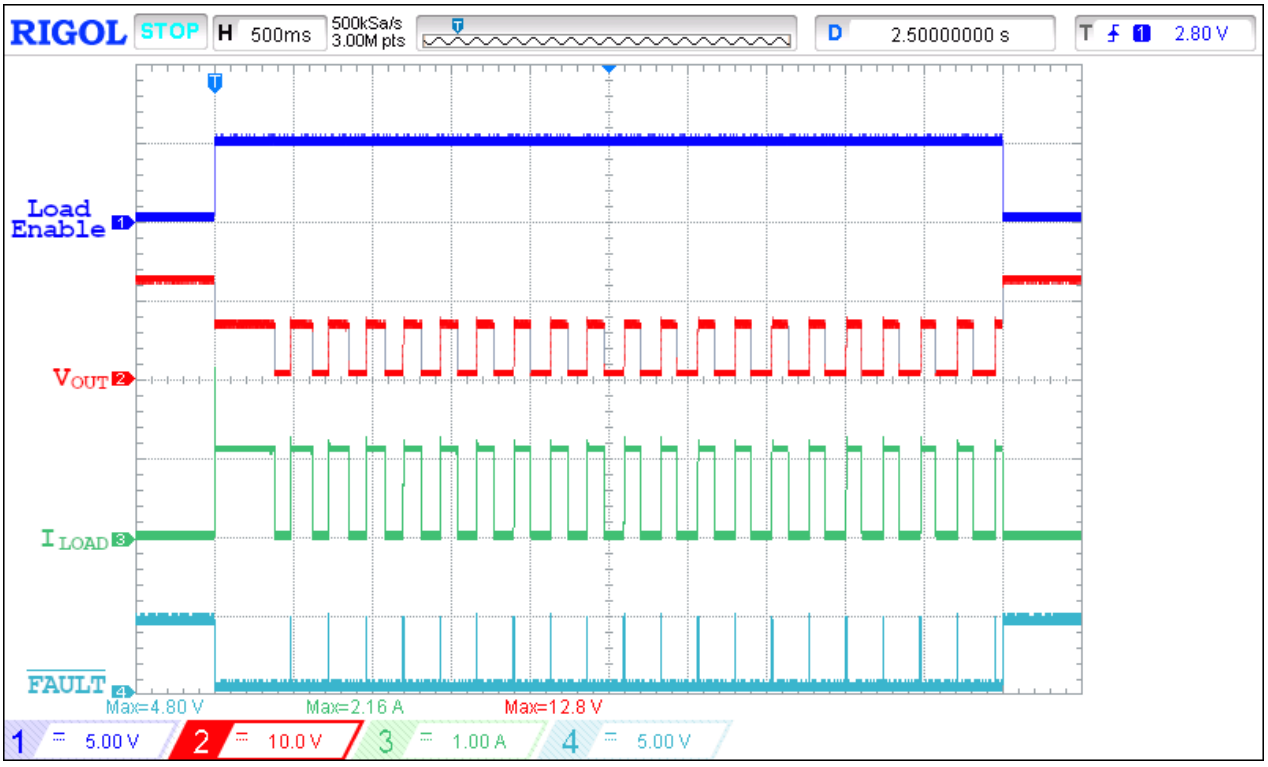


Figure 35. Application Diagram for Testing Active Current Limit and I_{OUT} Response Time



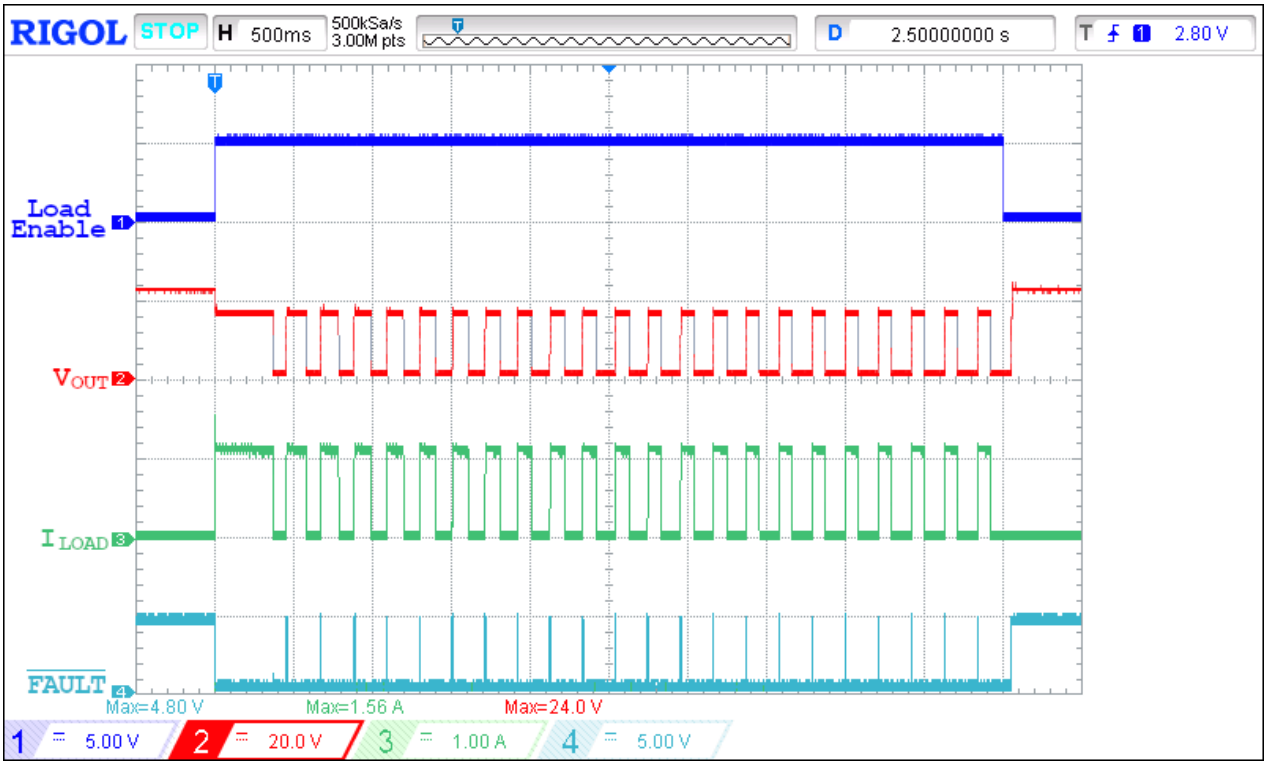
Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

Figure 36. Active Current Limit Operation Waveform for V_{IN} = 4.5 V



Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

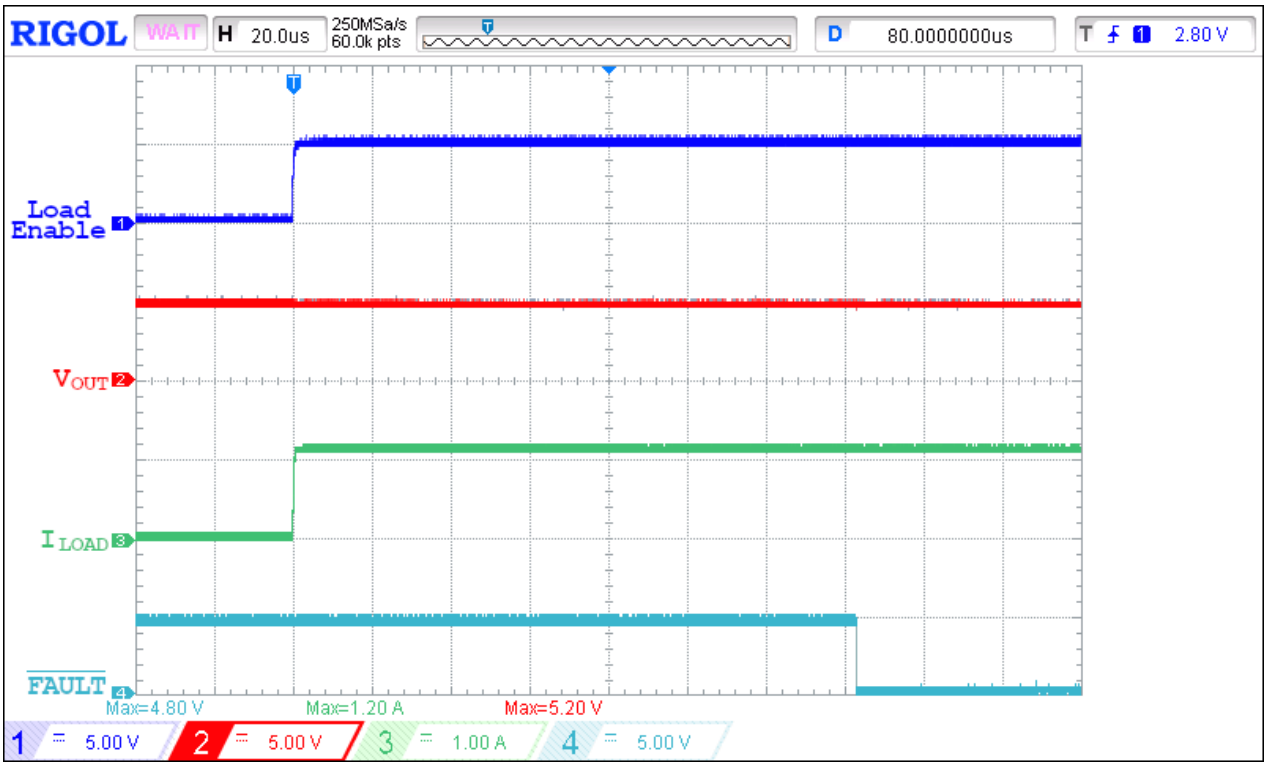
Figure 37. Active Current Limit Operation Waveform for V_{IN} = 12 V



Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

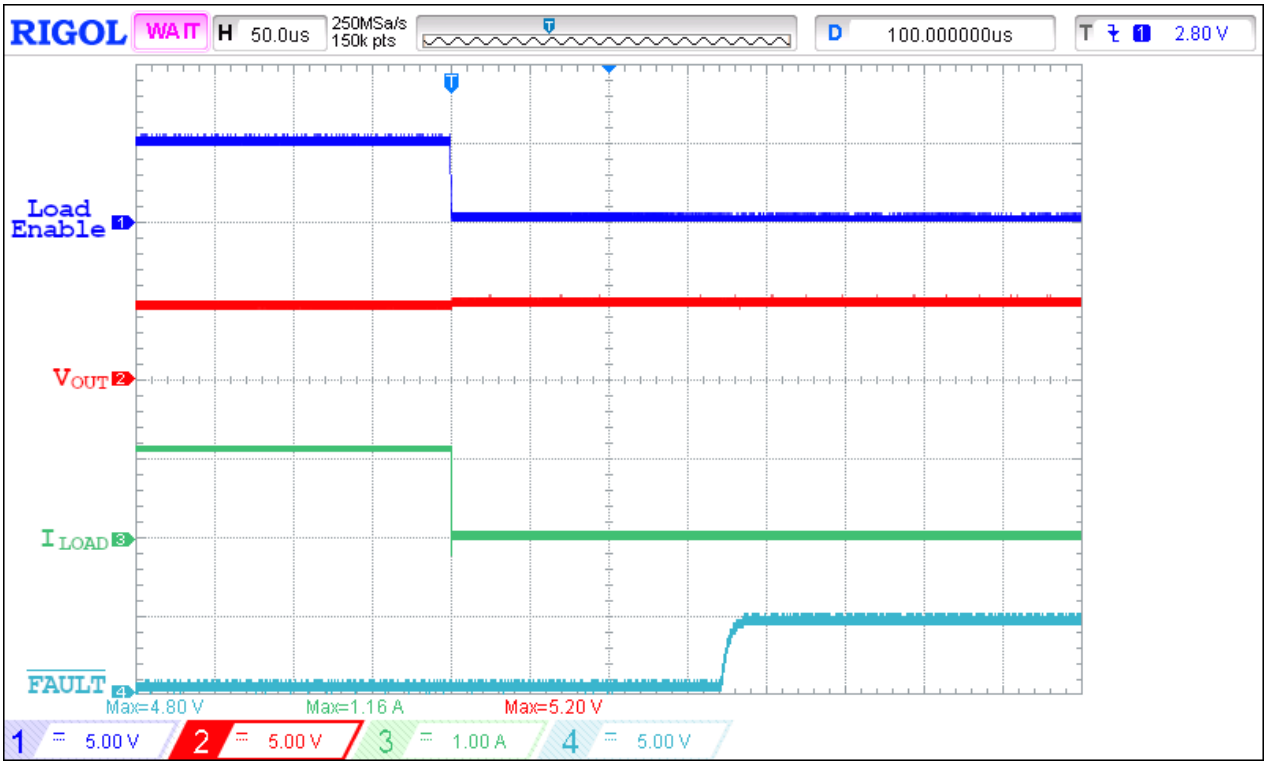
Figure 38. Active Current Limit Operation Waveform for V_{IN} = 22 V

3.2.5. Typical $\overline{\text{FAULT}}$ Operation Waveforms



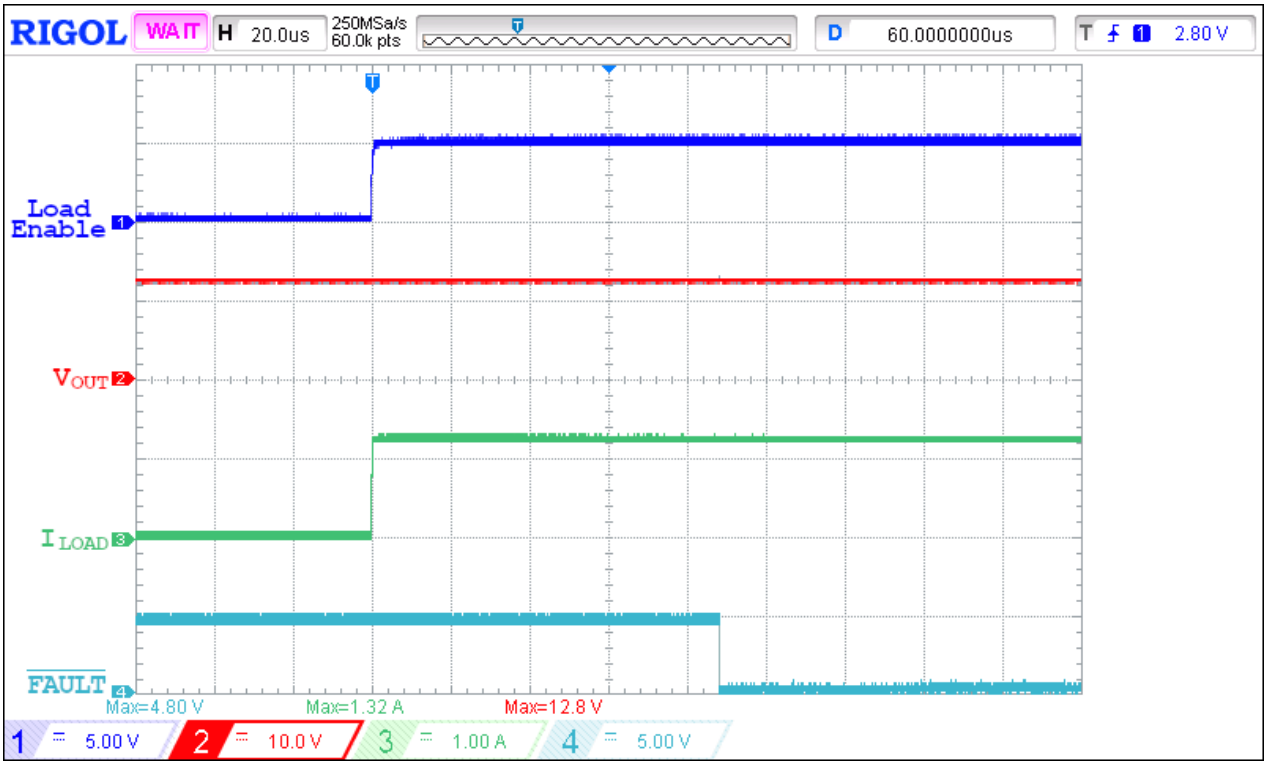
Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

Figure 39. $\overline{\text{FAULT}}$ Assertion Operation Waveform for V_{IN} = 4.5 V, Switch In 3.9 Ω Load



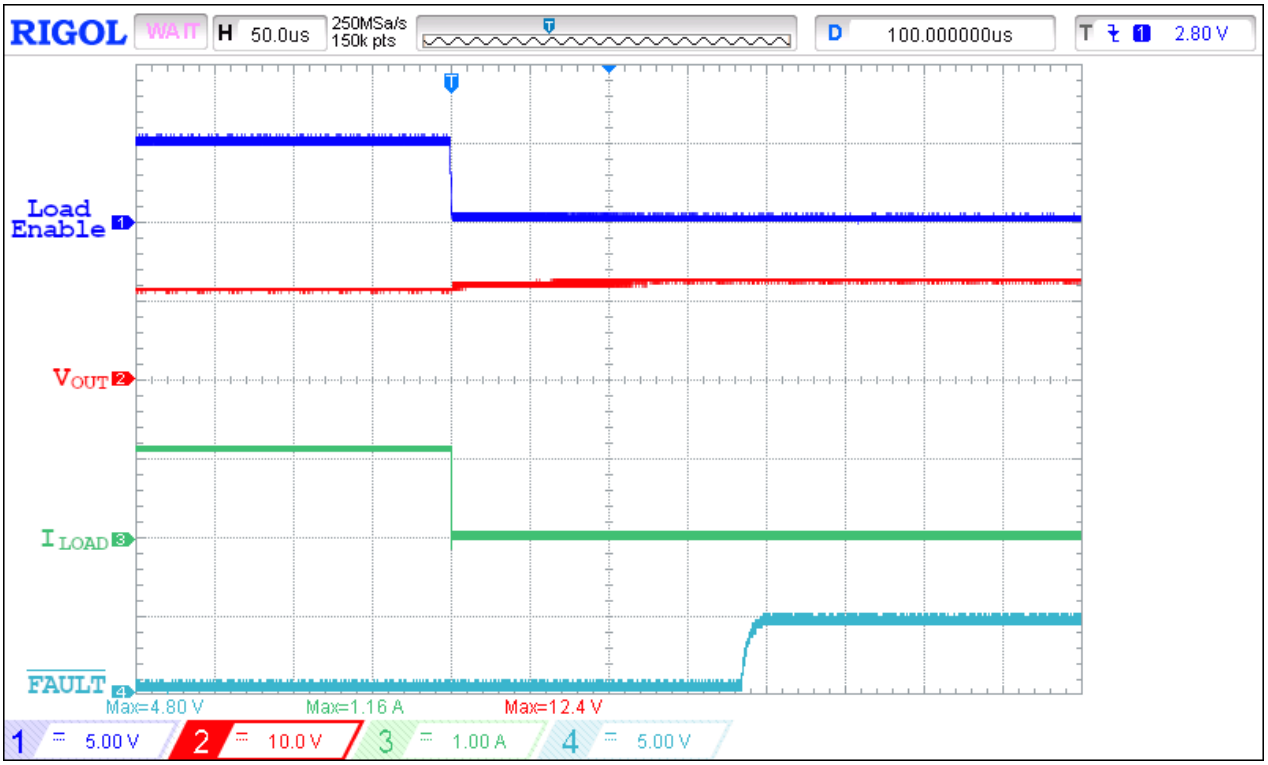
Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

Figure 40. $\overline{\text{FAULT}}$ De-Assertion Operation Waveform for V_{IN} = 4.5 V, Switch Out 3.9 Ω Load



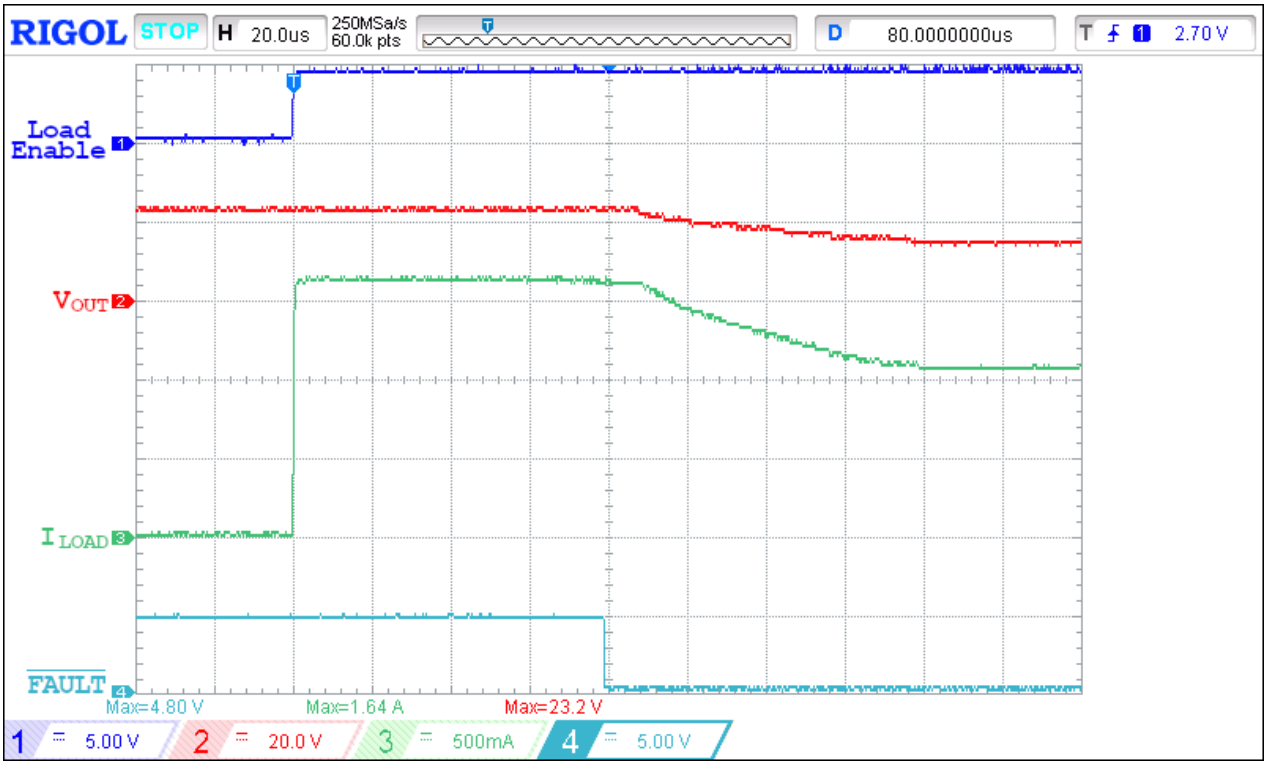
Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

Figure 41. $\overline{\text{FAULT}}$ Assertion Operation Waveform for V_{IN} = 12 V, Switch In 10 Ω Load



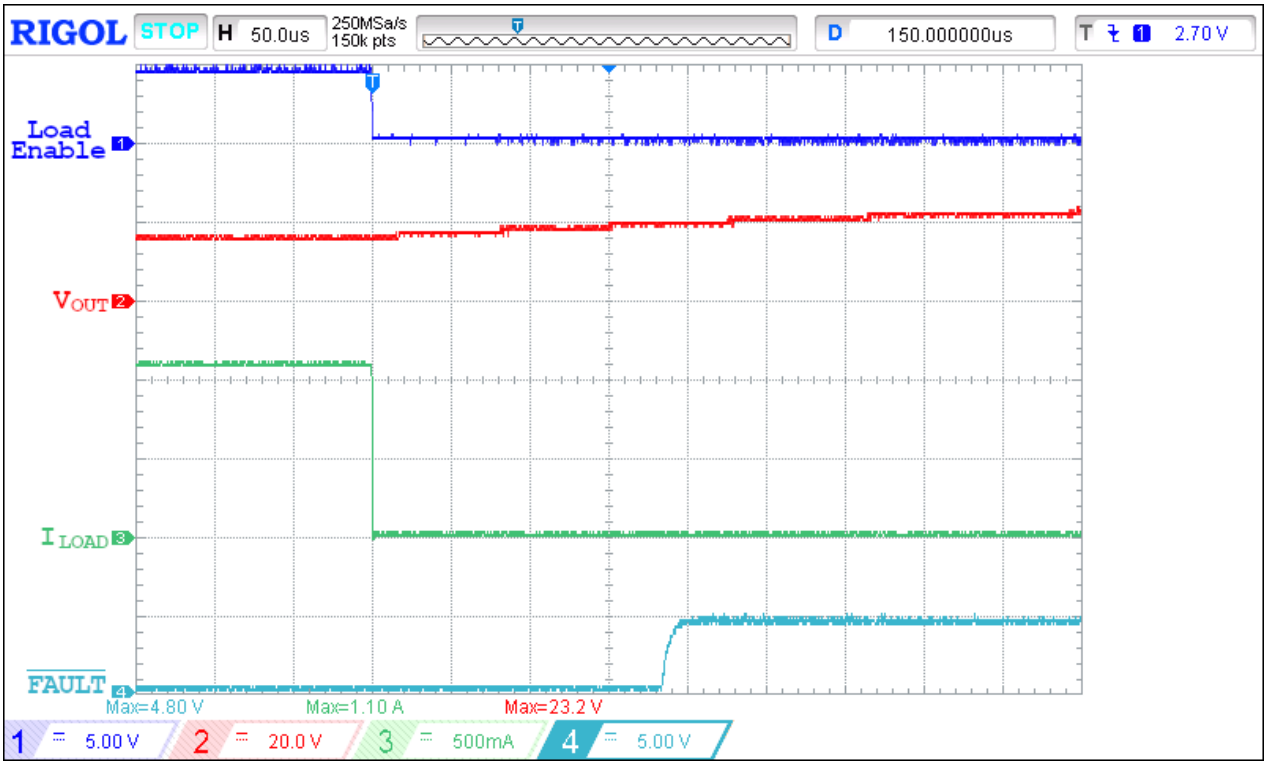
Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

Figure 42. $\overline{\text{FAULT}}$ De-Assertion Operation Waveform for V_{IN} = 12 V, Switch Out 10 Ω Load



Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

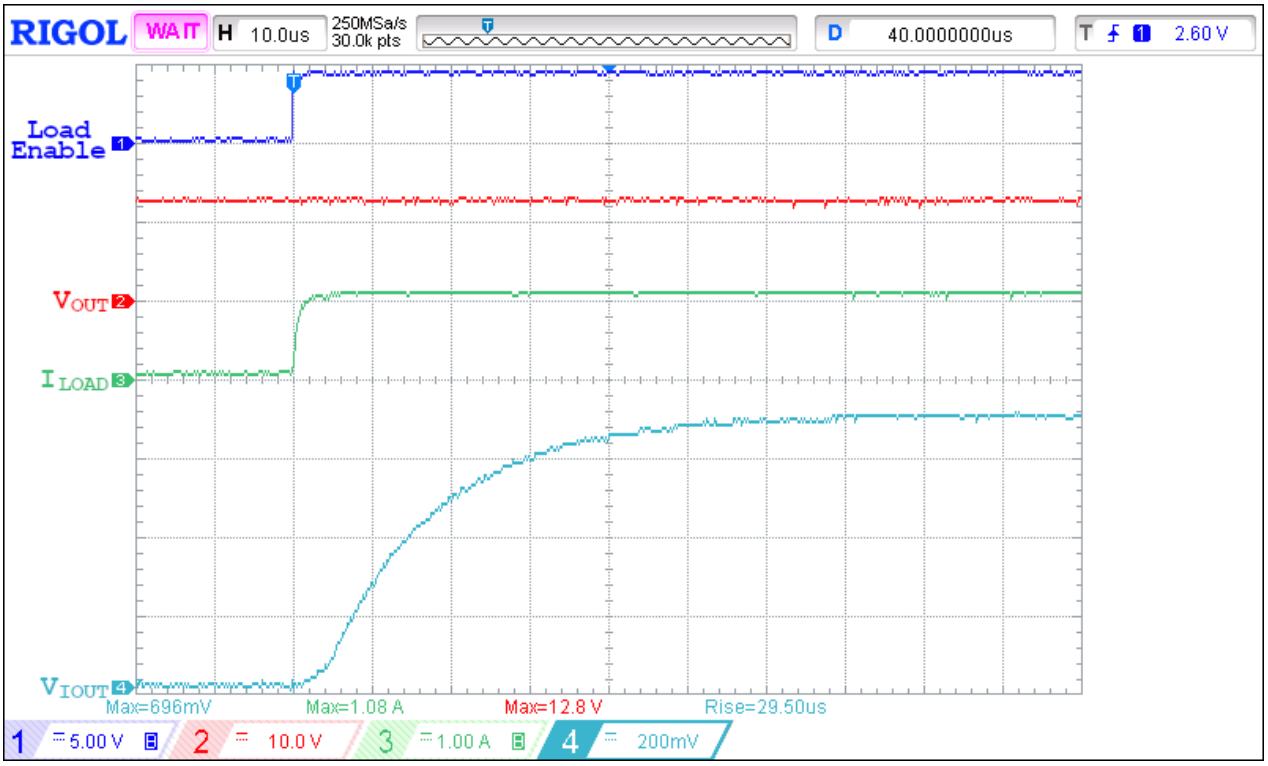
Figure 43. $\overline{\text{FAULT}}$ Assertion Operation Waveform for V_{IN} = 22 V, Switch In 14 Ω Load



Conditions: C_{LOAD} = 10 µF, I_{ACL} = 1 A, R_{SET} = 91 kΩ.

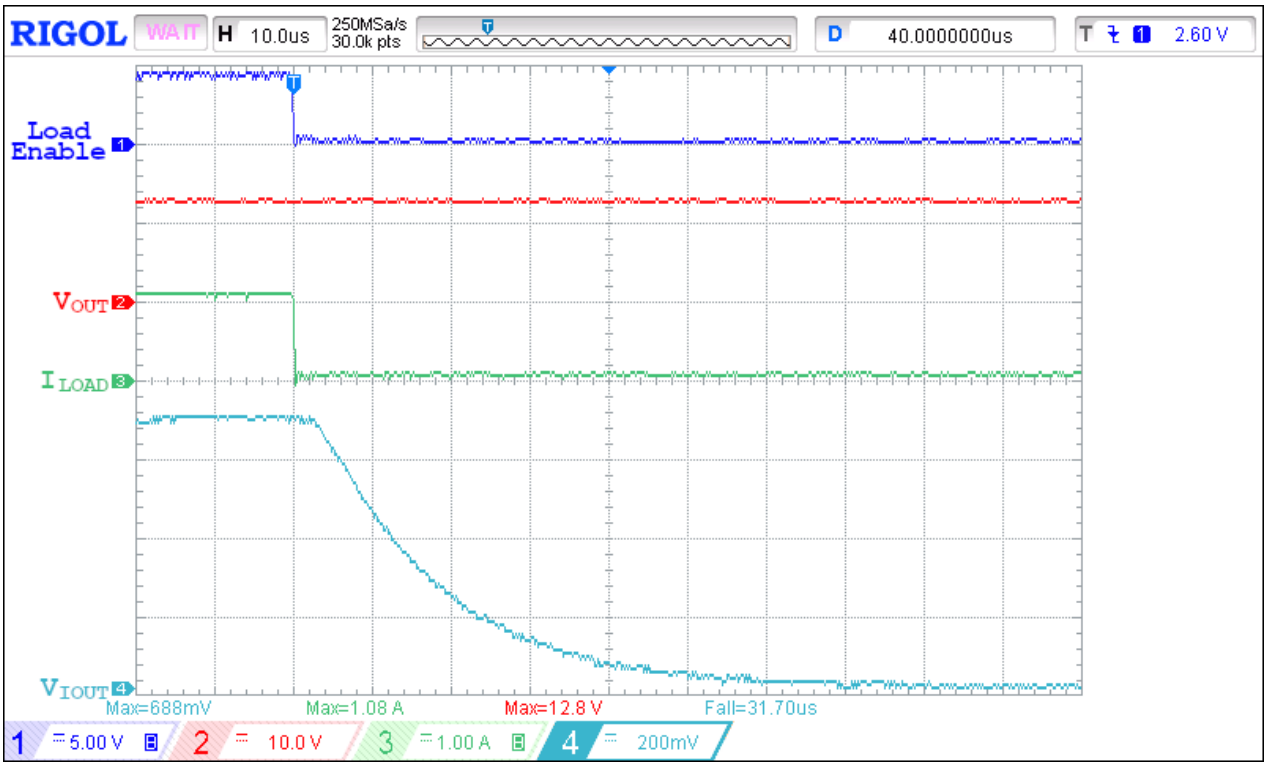
Figure 44. $\overline{\text{FAULT}}$ De-Assertion Operation Waveform for V_{IN} = 22 V, Switch Out 14 Ω Load

3.2.6. Typical I_{OUT} Operation Waveforms



Conditions: C_{LOAD} = 10 µF, R_{LOAD} = 12 Ω, C_{IOUT} = 0.18 nF, R_{IOUT} = 64.9 kΩ.

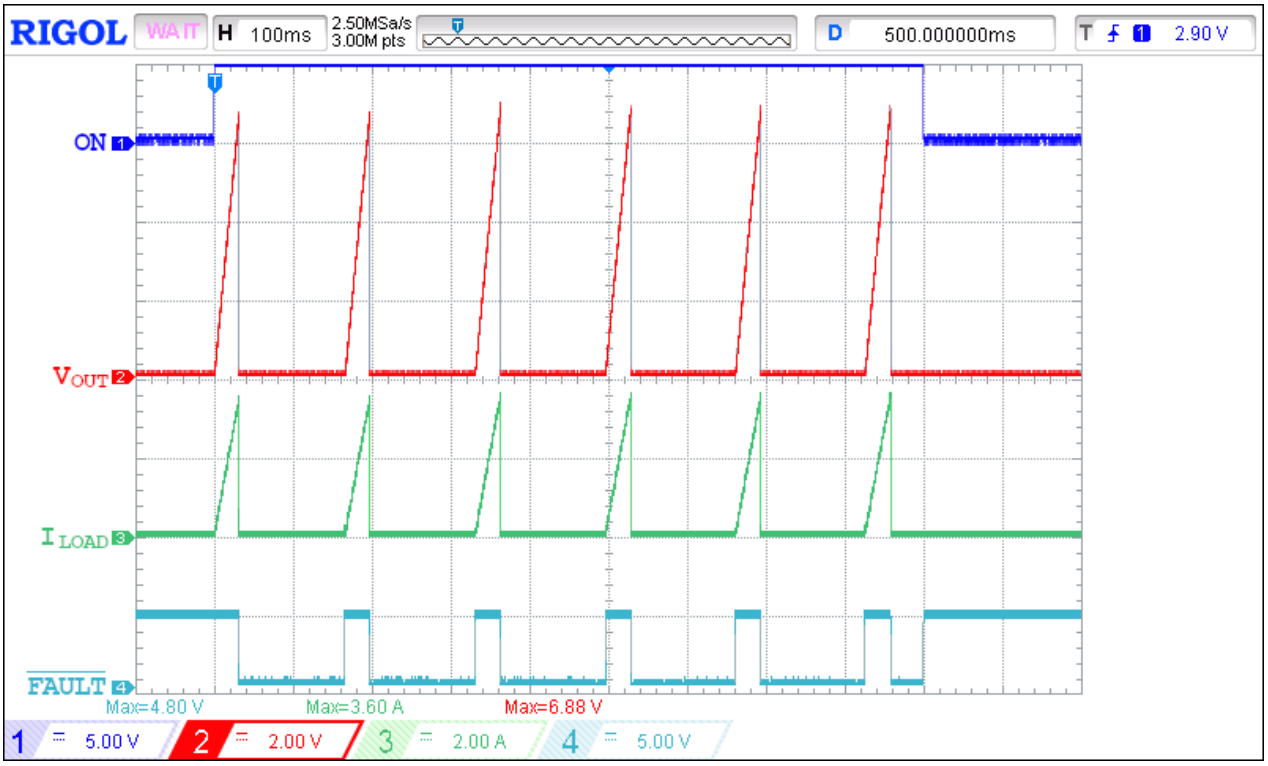
Figure 45. I_{OUT} Response Time Operation Waveform for V_{IN} = 12 V, Load Step from 0 A to 1 A



Conditions: C_{LOAD} = 10 µF, R_{LOAD} = 12 Ω, C_{IOUT} = 0.18 nF, R_{IOUT} = 64.9 kΩ.

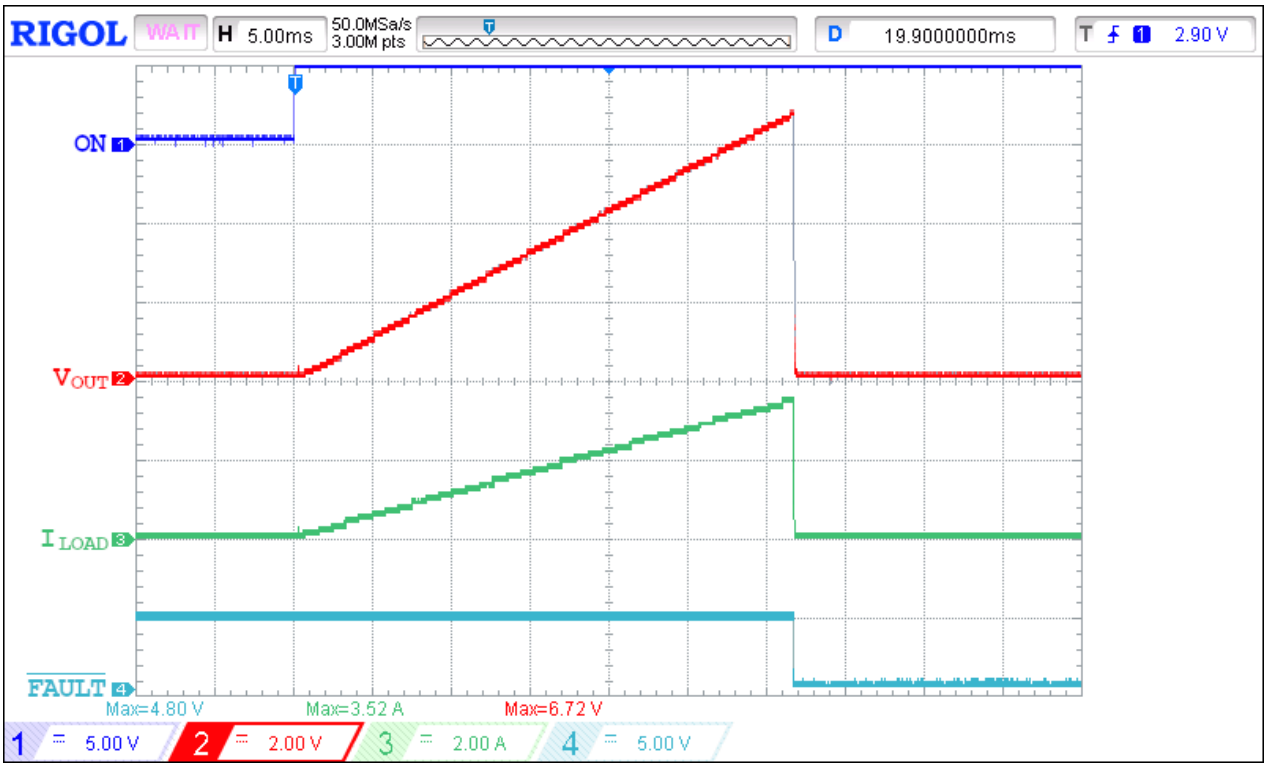
Figure 46. I_{OUT} Response Time Operation Waveform for V_{IN} = 12 V, Load Step from 1 A to 0 A

3.2.7. Typical SOA Operation Waveforms



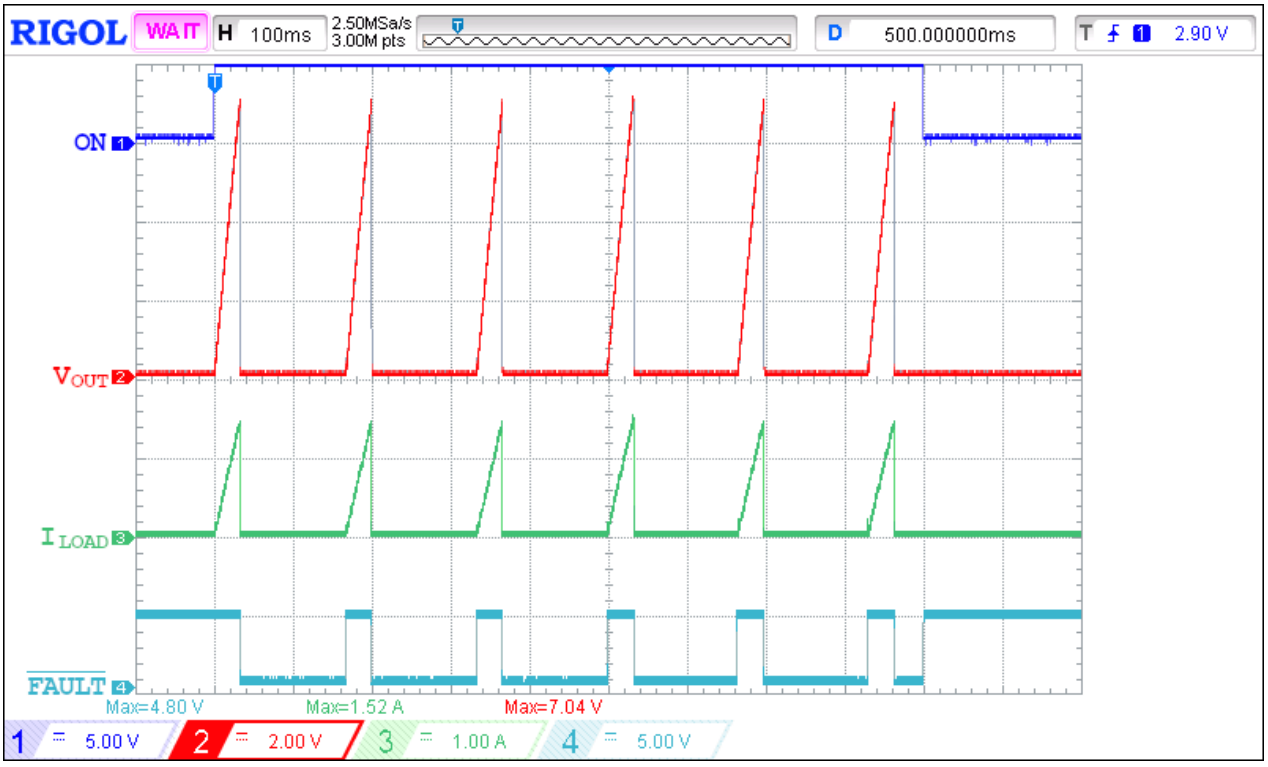
Conditions: C_{SLEW} = 150 nF, C_{LOAD} = 10 µF, R_{LOAD} = 1.9 Ω.

Figure 47. 12.5 W SOA Protection Operation Waveform with 18 ms Blanking Time for V_{IN} = 12 V



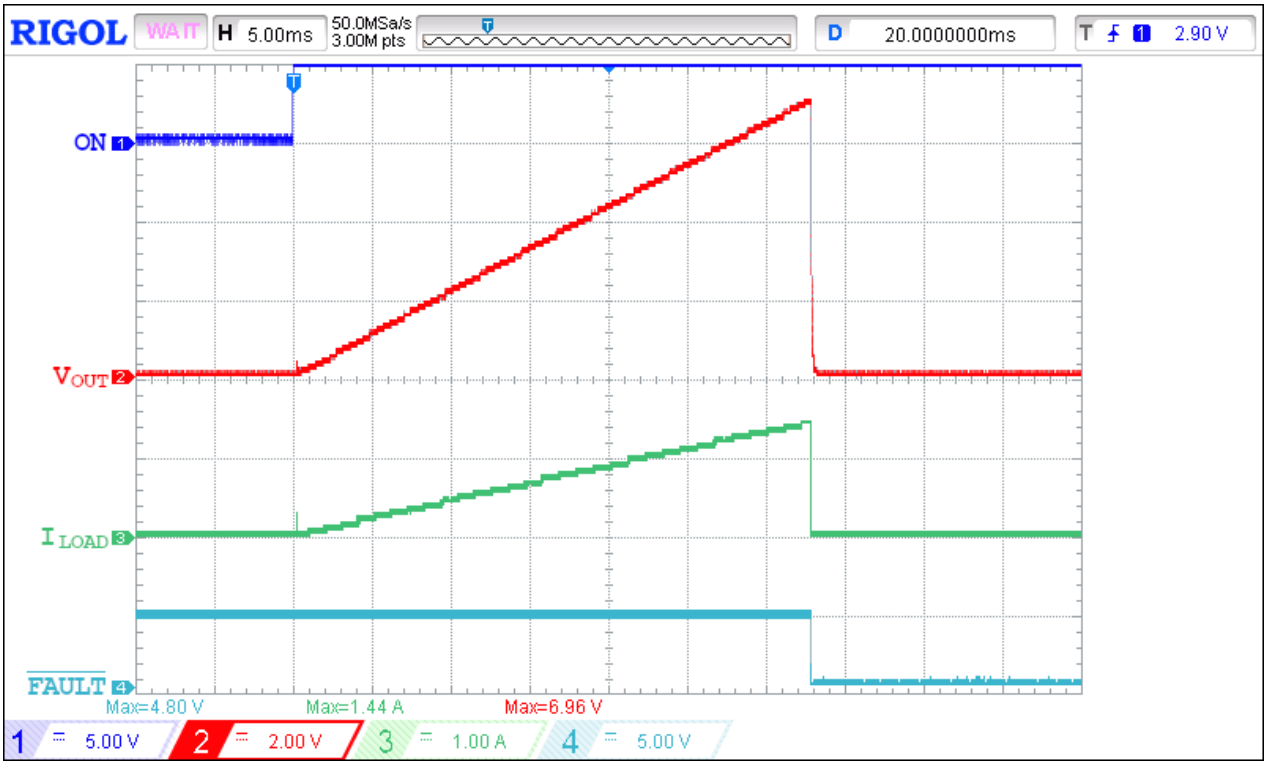
Conditions: C_{SLEW} = 150 nF, C_{LOAD} = 10 µF, R_{LOAD} = 1.9 Ω.

Figure 48. 12.5 W SOA Protection Operation Waveform with 18 ms Blanking Time for V_{IN} = 12 V (Extended View)



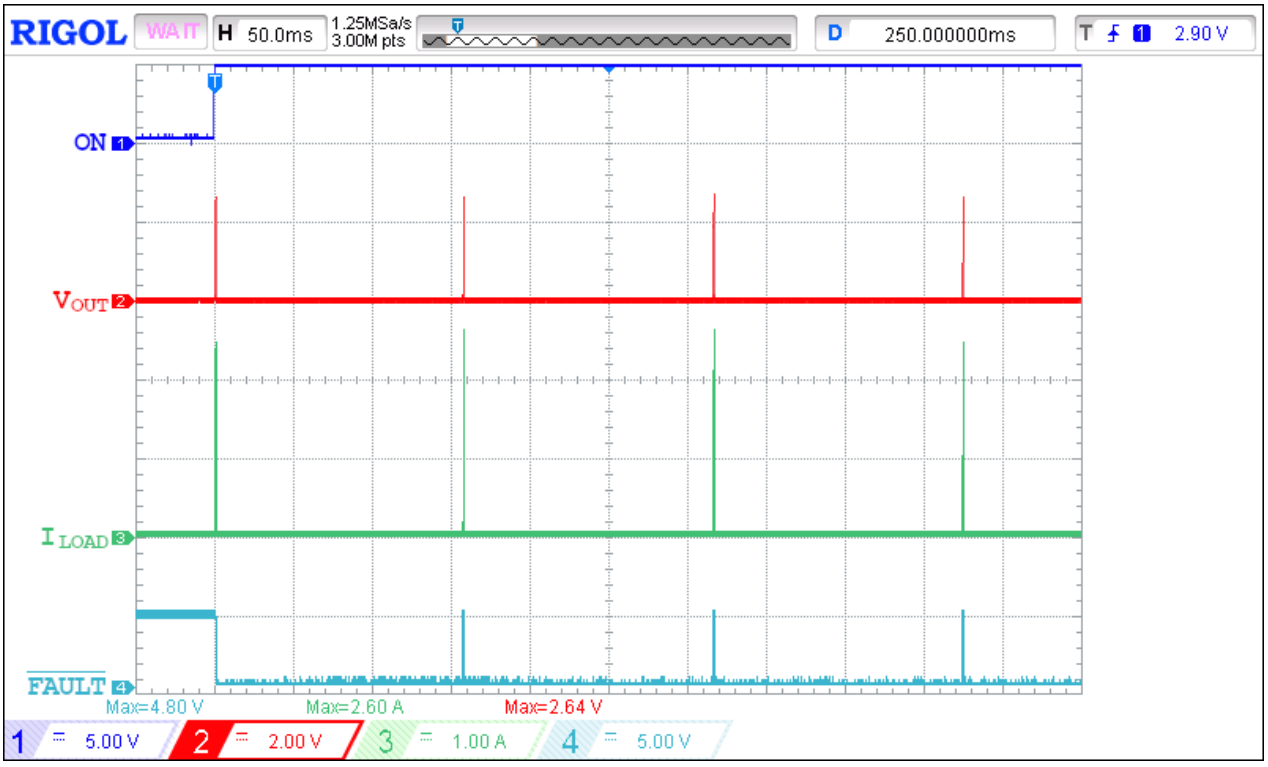
Conditions: C_{SLEW} = 150 nF, C_{LOAD} = 10 µF, R_{LOAD} = 5 Ω.

Figure 49. 12.5 W SOA Protection Operation Waveform with 18 ms Blanking Time for V_{IN} = 22 V



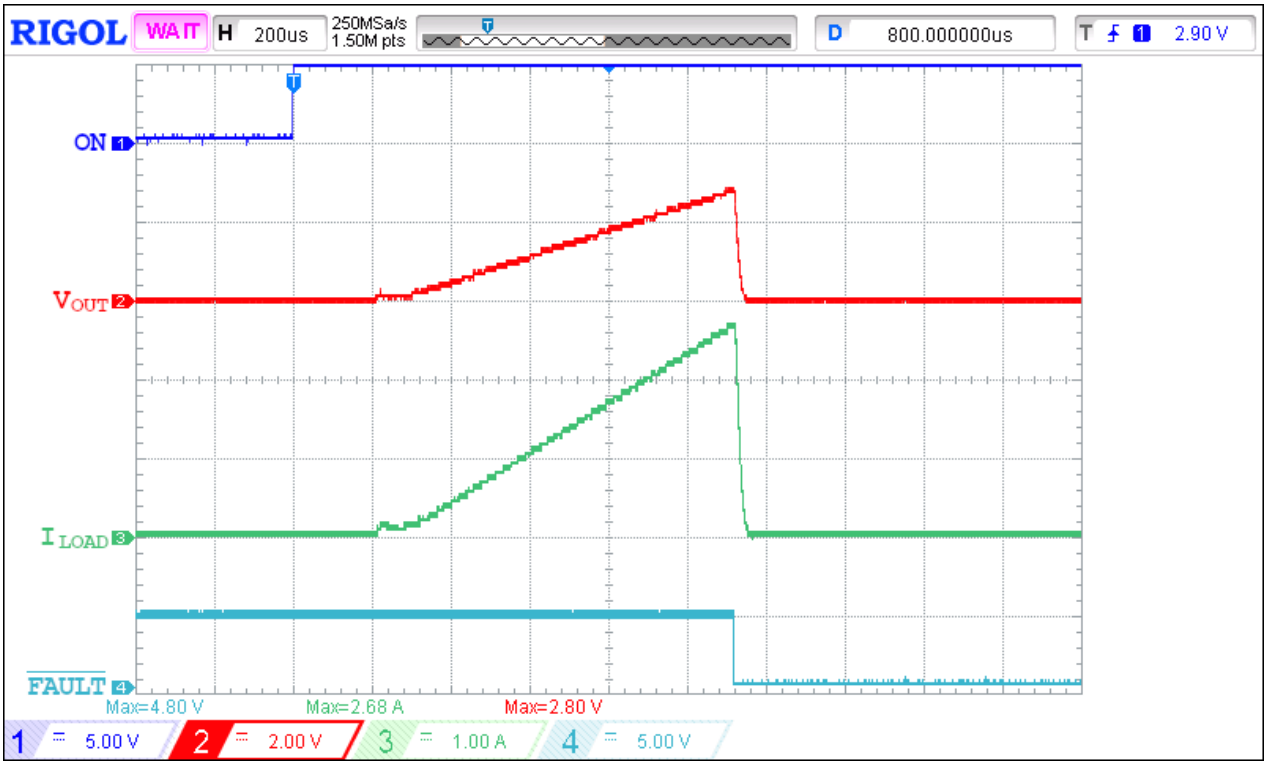
Conditions: C_{SLEW} = 150 nF, C_{LOAD} = 10 µF, R_{LOAD} = 5 Ω.

Figure 50. 12.5 W SOA Protection Operation Waveform with 18 ms Blanking Time for V_{IN} = 22 V (Extended View)



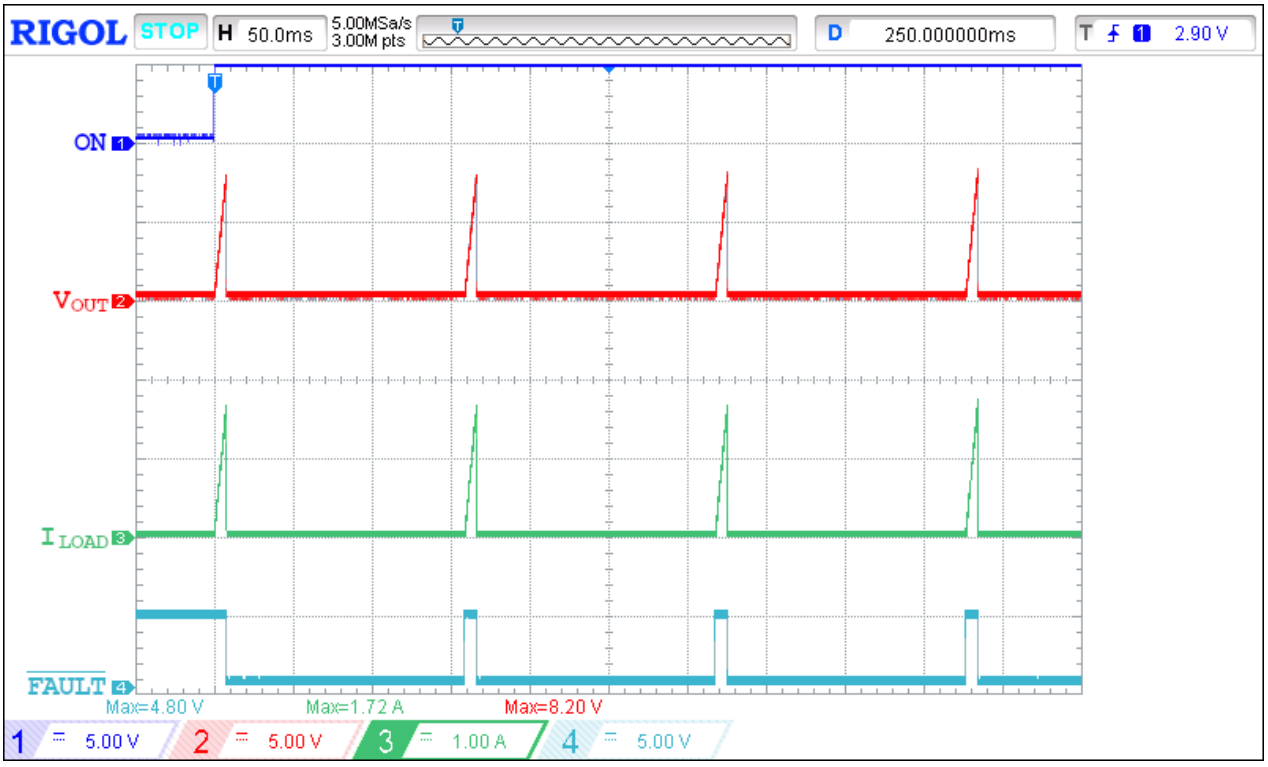
Conditions: C_{SLEW} = 10 nF, C_{LOAD} = 10 µF, R_{LOAD} = 1 Ω.

Figure 51. 25 W SOA Protection Operation Waveform for V_{IN} = 12 V



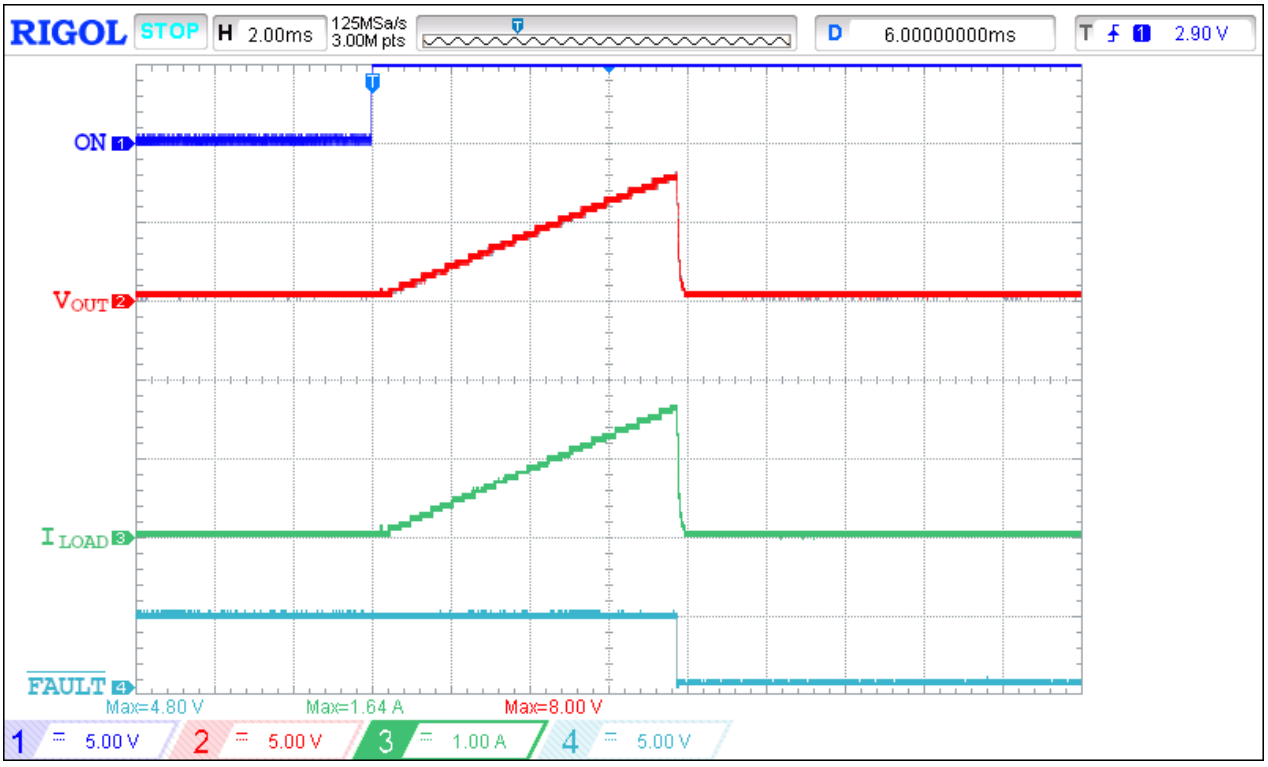
Conditions: C_{SLEW} = 10 nF, C_{LOAD} = 10 µF, R_{LOAD} = 1 Ω.

Figure 52. 25 W SOA Protection Operation Waveform for V_{IN} = 12 V (Extended View)



Conditions: C_{SLEW} = 33 nF, C_{LOAD} = 10 µF, R_{LOAD} = 4.7 Ω.

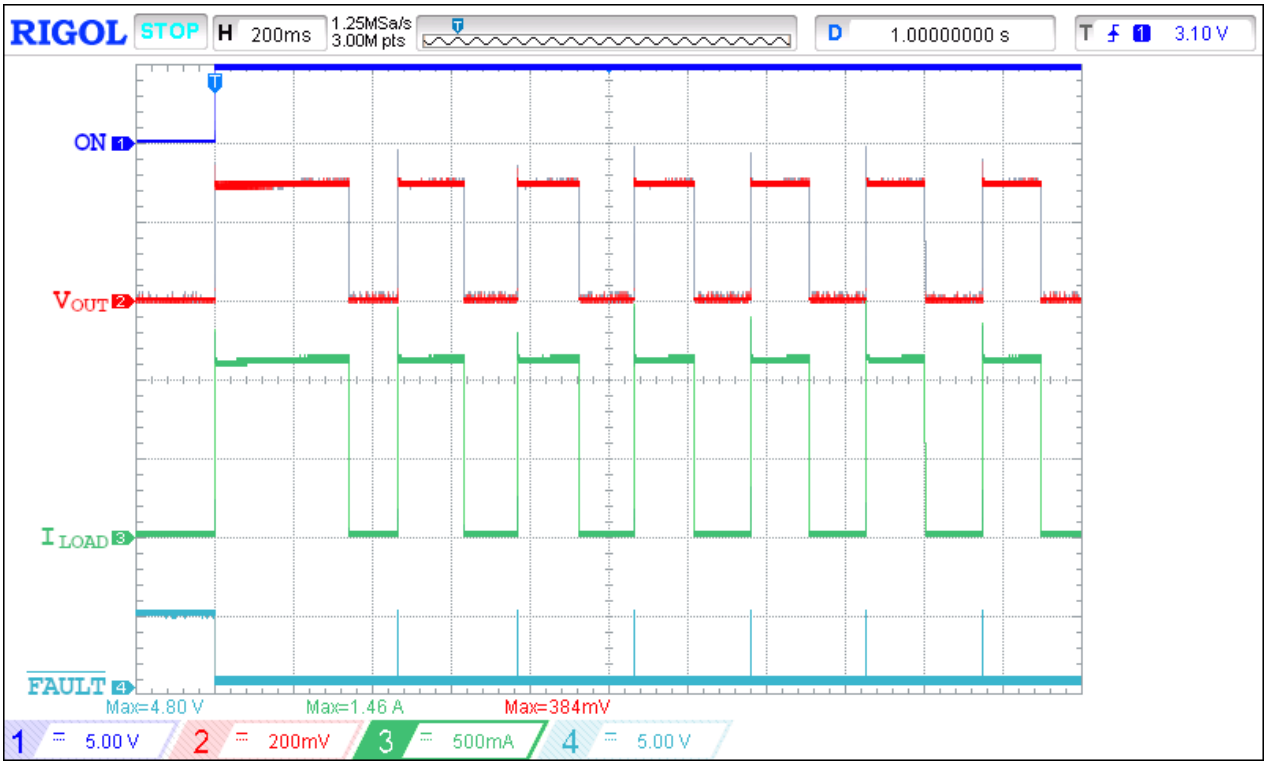
Figure 53. 25 W SOA Protection Operation Waveform for V_{IN} = 22 V



Conditions: C_{SLEW} = 33 nF, C_{LOAD} = 10 µF, R_{LOAD} = 4.7 Ω.

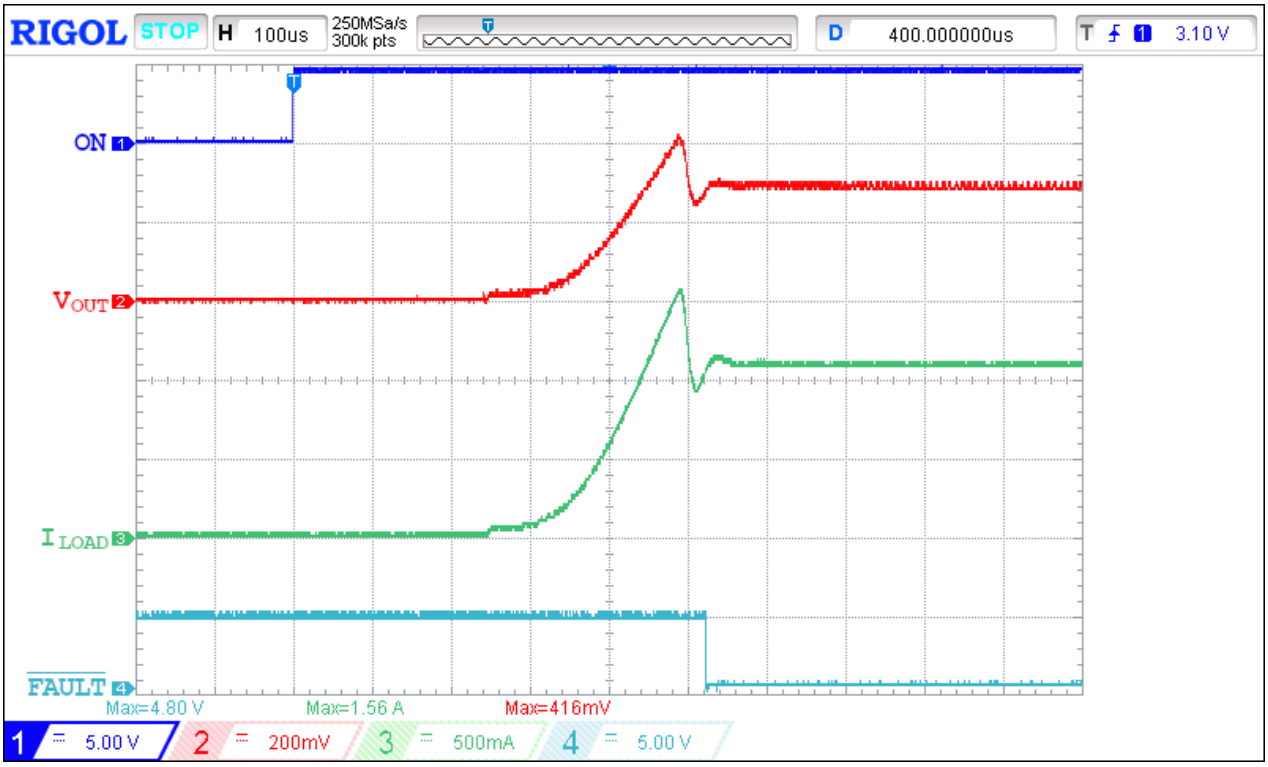
Figure 54. 25 W SOA Protection Operation Waveform for V_{IN} = 22 V (Extended View)

3.2.8. Typical Short Circuit Current Limiting Operation Waveforms



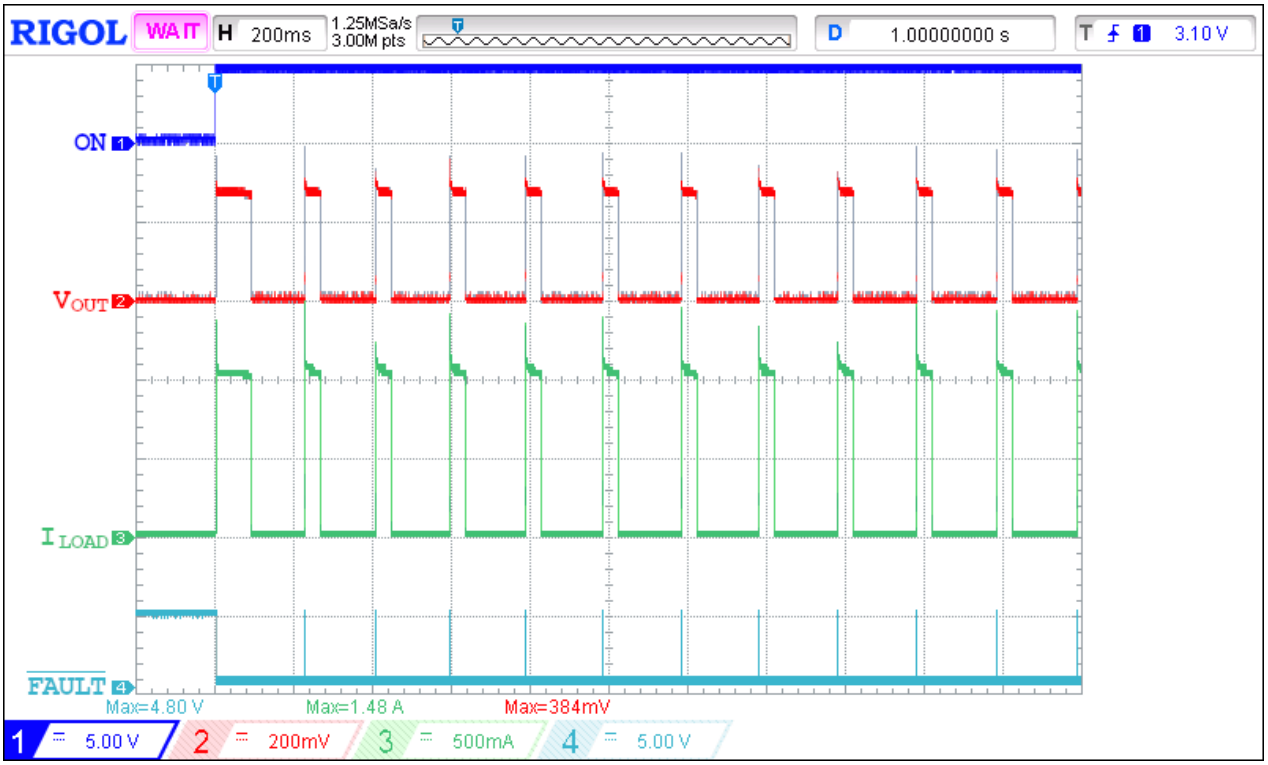
Conditions: SEL = High, C_{SLEW} = 10 nF, R_{SET} = 13.3 kΩ, C_{LOAD} = 10 µF, R_{SHORT} = 0.25 Ω.

Figure 55. Short Circuit Current Limiting Operation Waveform for V_{IN} = 4.5 V, ON = Low → High



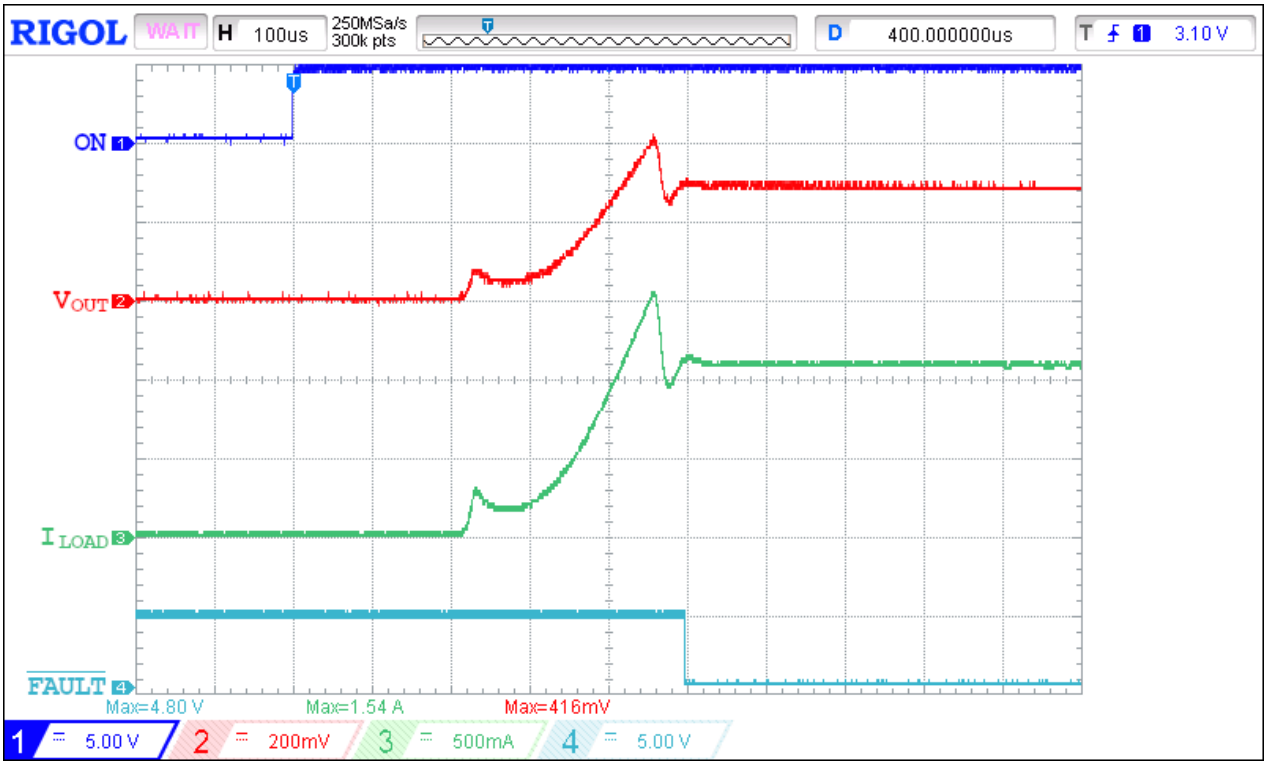
Conditions: SEL = High, C_{SLEW} = 10 nF, R_{SET} = 13.3 kΩ, C_{LOAD} = 10 µF, R_{SHORT} = 0.25 Ω.

Figure 56. Short Circuit Current Limiting Operation Waveform for V_{IN} = 4.5 V, ON = Low → High (Extended View)



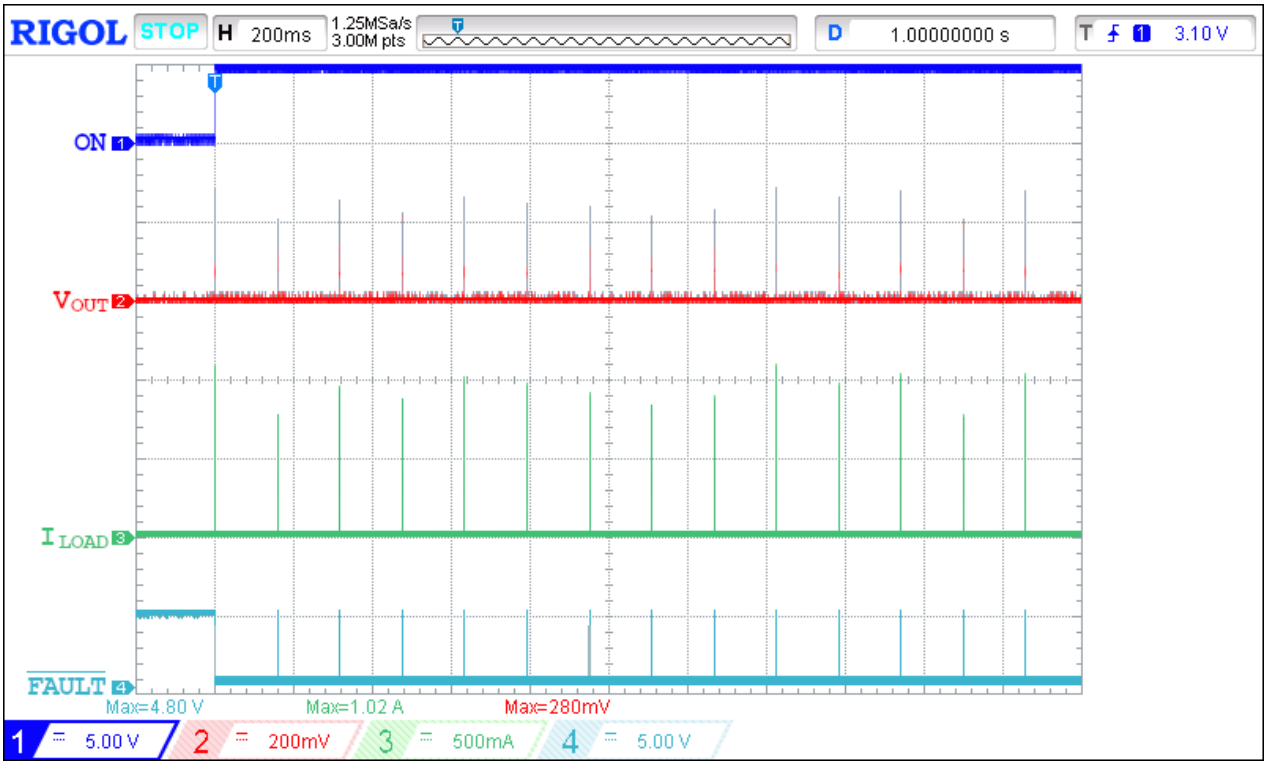
Conditions: SEL = High, C_{SLEW} = 10 nF, R_{SET} = 13.3 kΩ, C_{LOAD} = 10 µF, R_{SHORT} = 0.25 Ω.

Figure 57. Short Circuit Current Limiting Operation Waveform for V_{IN} = 12 V, ON = Low → High



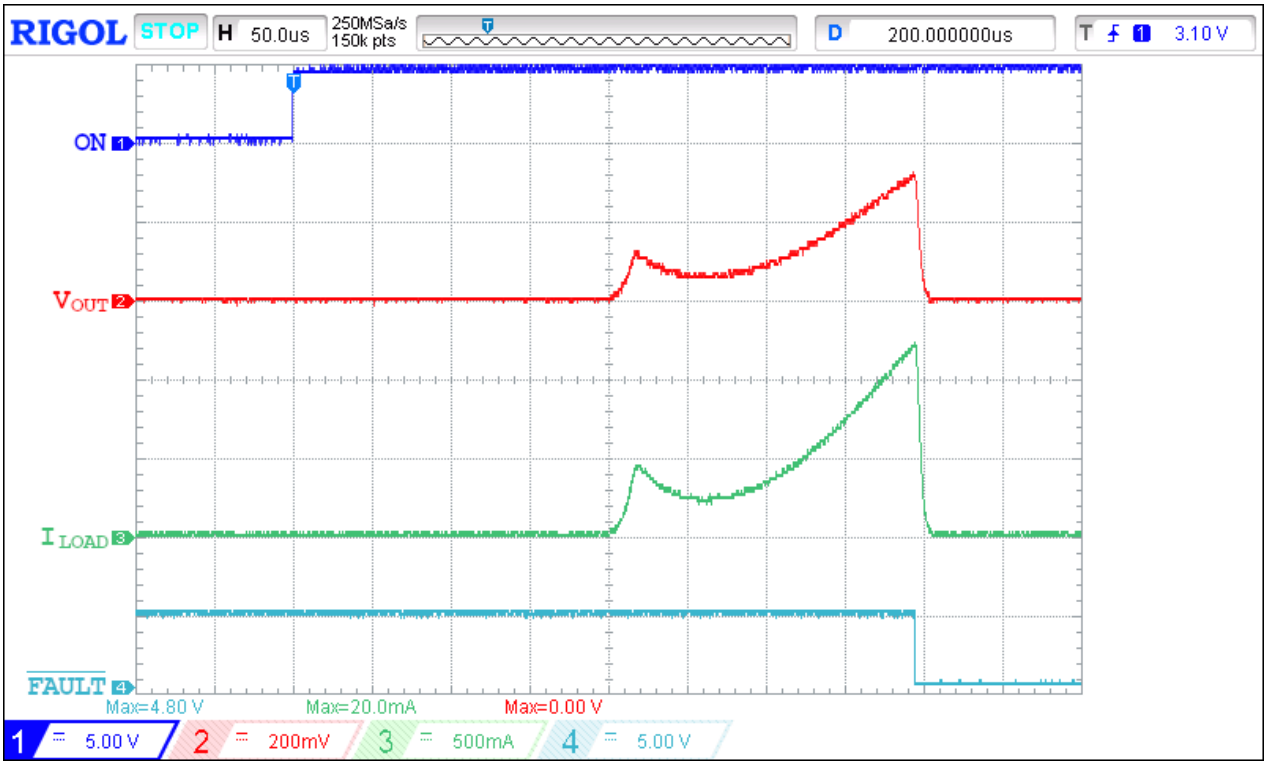
Conditions: SEL = High, C_{SLEW} = 10 nF, R_{SET} = 13.3 kΩ, C_{LOAD} = 10 µF, R_{SHORT} = 0.25 Ω.

Figure 58. Short Circuit Current Limiting Operation Waveform for V_{IN} = 12 V, ON = Low → High (Extended View)



Conditions: SEL = High, ON = Low → High, C_{SLEW} = 10 nF, R_{SET} = 13.3 kΩ, C_{LOAD} = 10 µF, R_{SHORT} = 0.25 Ω.

Figure 59. SOA is Activated at Short Circuit Condition Operation Waveform for V_{IN} = 22 V



Conditions: SEL = High, ON = Low → High, C_{SLEW} = 10 nF, R_{SET} = 13.3 kΩ, C_{LOAD} = 10 µF, R_{SHORT} = 0.25 Ω.

Figure 60. SOA is Activated at Short Circuit Condition Operation Waveform for V_{IN} = 22 V (Extended View)

4. Application Information

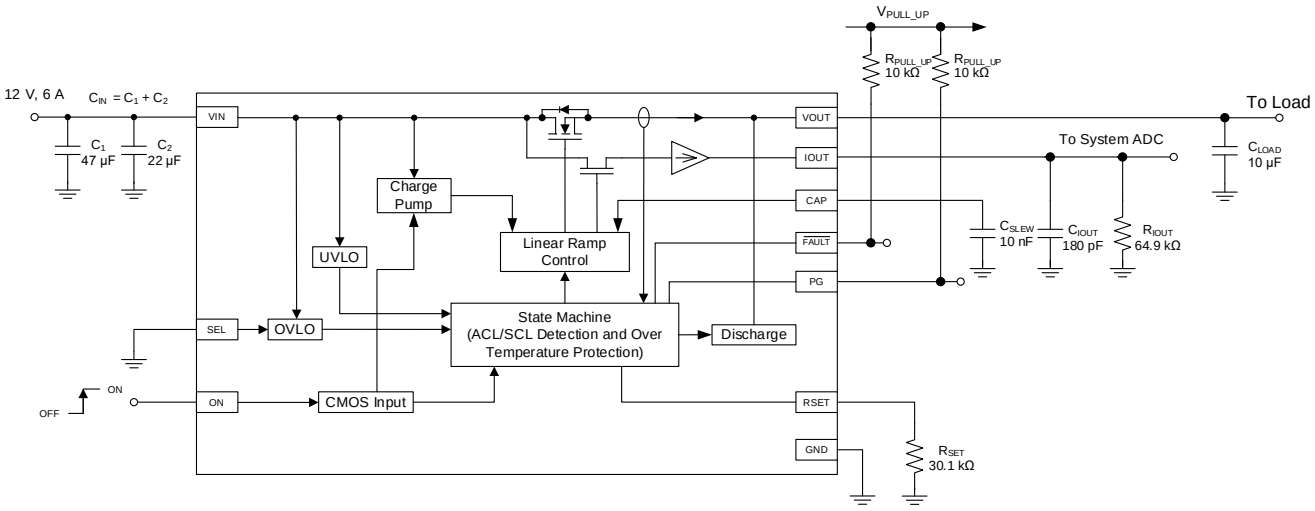


Figure 61. Typical Connection Diagram

4.1 SLG59H1132V Active Current Limiting Operation

After power up the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold. During active current limit operation, V_{OUT} is also reduced by I_{ACL} x $RDS_{ON(ACL)}$. This observed behavior is illustrated in the timing diagrams from Page 14 to Page 17.

However, if the overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET will completely shutdown, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

When a current limit event is detected, the $\overline{FAULT}$ signal becomes asserted in approximately $T\overline{FAULT}_{LOW}$ and the SLG59H1132V operates in constant current mode with the output current set by R_{SET} (see Setting Current Limit Threshold vs. RSET table). The SLG59H1132V continues to operate in constant current mode indefinitely until the current limit event has elapsed.

4.2 SLG59H1132V Short Circuit Current Limiting Operation

When V_{OUT} < 0.5 V (which is the case of the short circuit with the equivalent load resistance R_{LOAD} ≥ 250 mΩ), the load switch's internal Short Circuit Current Limit (SCL) monitor limits the MOSFET current to approximately 1 A (the I_{SCL} threshold). The SLG59H1132V's short circuit current limit (SCL) protection scheme is disabled automatically once V_{OUT} rises above 0.5 V.

While keeping the output current at I_{SCL} threshold for a long period of time a die temperature can exceed the listed $THERM_{ON}$ specification and the FET will completely shutdown, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output short circuit current limit condition persists.

If a short-circuit or a very large load current transient occurs after the ON pin is toggled Low-to-High transition, the SLG59H1132V's internal SCL circuit will be triggered if V_{OUT} falls by 0.5 V.

4.3 SLG59H1132V $\overline{FAULT}$ Operation

As previously stated in the Pin Description section, the open-drain $\overline{FAULT}$ output is asserted when an V_{IN} overvoltage, SOA protection, a current limit, or an over-temperature condition is detected. This output becomes

asserted in $\overline{TFAULT}_{LOW}$ upon the detection of a fault condition. If the ON pin is toggled Low-to-High while the $\overline{FAULT}$ output is low, the $\overline{FAULT}$ output is de-asserted without delay. $\overline{FAULT}$ state is not defined for V_{IN} < 4 V.

4.4 SLG59H1132V PG Operation

As previously stated in the Pin Description section the open-drain PG output is asserted within TPG_{HIGH} when V_{OUT} is higher than the SLG59H1132V's $PG_{TRIGGER}$ threshold. PG output becomes de-asserted within TPG_{LOW} when ON is toggled from High-to-Low. PG state is not defined for V_{IN} < 4 V.

4.5 SLG59H1132V Analog Current Monitor Operation

As an analog current output, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The I_{OUT} transfer characteristic is typically 10 µA/A with a voltage compliance range of 0.5 V ≤ V_{IOUT} ≤ 4 V. Optimal I_{OUT} linearity is exhibited for 0.5 A ≤ I_{DS} ≤ 6 A. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor. Depends on the applications full operating current range a resistor value from IOUT pin to GND can be changed to adjust voltage scale that is more convenient for external ADC.

4.6 Setting the SLG59H1132V Output Current Limit with R_{SET}

The current limit operation of the SLG59H1132V begins by choosing the appropriate ±1%-tolerance R_{SET} value for the application. The recommended range for R_{SET} is:

$$91\ k\Omega \geq R_{SET} \geq 14\ k\Omega$$

which corresponds to an output constant current limit in the following range:

$$1\ A \leq I_{ACL} \leq 7\ A$$

Table 2. Setting Current Limit Threshold vs. R_{SET}

R_{SET}	Active Current Limit	Active Current Limit Accuracy[4]
91 kΩ	1 A	± 29%
51 kΩ	2 A	± 23%
33 kΩ	3 A	± 20%
24.9 kΩ	4 A	± 18%
20 kΩ	5 A	± 16%
16.9 kΩ	6 A	± 15%
14 kΩ	7 A	± 13%

[4] Over voltage and over temperature range.

4.7 High Voltage GreenFET Safe Operating Area Explained

Renesas' High Voltage GreenFET load switches incorporate a number of internal protections features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operating Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if during start-up package power dissipation exceeds an internal 12.5 W threshold longer than 18 ms blanking time or 25 W threshold without blanking time. High Voltage GreenFET devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One possible way to have an overpower condition trigger SOA protection is when High Voltage GreenFET products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Condition" guidance in the Applications section of the datasheet.

During an overcurrent condition, High Voltage GreenFET devices will try to limit the output current to the level set by the external R_{SET} resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's RDS_{ON} increased as well. Since the FET's RDS_{ON} is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 12.5 W for longer than 18 ms blanking time or 25 W threshold without blanking time, internal SOA protection will be triggered and the FET will open circuit (switch off).

Every time SOA protection is triggered, all High Voltage GreenFET devices will automatically attempt to resume nominal operation after 160 ms. The automatic retry attempt allows to start-up again with SOA at 12.5 W for longer than 18 ms blanking time or 25 W without blanking time.

4.8 Safe Start-up Condition

SLG59H1132V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the VOUT pin with a capacitor and a resistor may result in non-monotonic V_{OUT} ramping. In general, under light loading on VOUT, V_{OUT} ramping can be controlled with C_{SLEW} value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4.9\ \mu A \times \frac{20}{3}$$

where:
T_{RISE} = Total rise time from 10% V_{OUT} to 90% V_{OUT} (ms)
V_{IN} = Input Voltage (V)
C_{SLEW} = Capacitor value on CAP pin (nF)

When there is capacitor and resistor loading on VOUT during start up, the following tables will ensure V_{OUT} ramping is monotonic without triggering internal protection:

Table 3. Safe Start-up Loading for V_{IN} = 12 V (Monotonic Ramp)

Slew Rate, V/ms	C_{SLEW}[5], nF	C_{LOAD}, µF	R_{LOAD}, Ω
0.2	150	3300	6.2
0.5	66	300	2
1	33	500	2
2	18	250	2
3	10	160	2
4	8.2	120	2
5	6.8	100	2

Table 4. Safe Start-up Loading for V_{IN} = 22 V (Monotonic Ramp)

Slew Rate, V/ms	C_{SLEW}[5], nF	C_{LOAD}, µF	R_{LOAD}, Ω
0.5	66	500	12
1	33	250	8
1.5	22	160	8
2	18	120	8
2.5	13	100	8

[5] Select the closest-value tolerance capacitor.

4.9 Setting the SLG59H1132V's Input Overvoltage Lockout Threshold

As shown in the table below, SEL selects the V_{IN} overvoltage threshold at which the SLG59H1132V's internal state machine will turn OFF (open circuit) the power MOSFET if V_{IN} exceeds the selected threshold.

Table 5. Setting Typical Overvoltage Lockout Threshold

SEL	V_{IN_OVLO}
Low	14.4 V
High	24 V

With an activated SLG59H1132V (ON = High) and at any time V_{IN} crosses the programmed V_{IN} overvoltage threshold (V_{IN_OVLO}), the state machine opens the load switch and asserts the $\overline{FAULT}$ pin within $TFAULT_{LOW}$.

In applications with a deactivated or inactive SLG59H1132V ($V_{IN} > V_{IN\_UVLO} + V_{IN\_UVLO\_HYS}$ and ON = Low) and if the applied V_{IN} is higher than the programmed V_{IN_OVLO} threshold, the SLG59H1132V's state machine will keep the load switch open circuited if the ON pin is toggled Low-to-High. In these cases, the $\overline{FAULT}$ pin will also be asserted within $TFAULT_{LOW}$ and will remain asserted until V_{IN} resumes nominal, steady-state operation.

4.10 Power Dissipation Considerations

The junction temperature of the SLG59H1132V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON} generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59H1132V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:
PD_{TOTAL} = Total package power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:
T_J = Die junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on PCB layout
T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59H1132V's power dissipation can also be calculated by taking into account the voltage drop across the switch (V_{IN} - V_{OUT}) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ , or}$$
$$PD_{TOTAL} = (V_{IN} - (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:
PD_{TOTAL} = Total package power dissipation, in Watts (W)
V_{IN} = Switch input Voltage, in Volts (V)
R_{LOAD} = Output Load Resistance, in Ohms (Ω)
I_{DS} = Switch output current, in Amps (A)
V_{OUT} = Switch output voltage, or R_{LOAD} x I_{DS}

In current limit mode, the SLG59H1132V's power dissipation can be calculated by taking into account the voltage drop across the load switch (V_{IN} - V_{OUT}) and the magnitude of the output current in current limit mode (I_{ACL}):

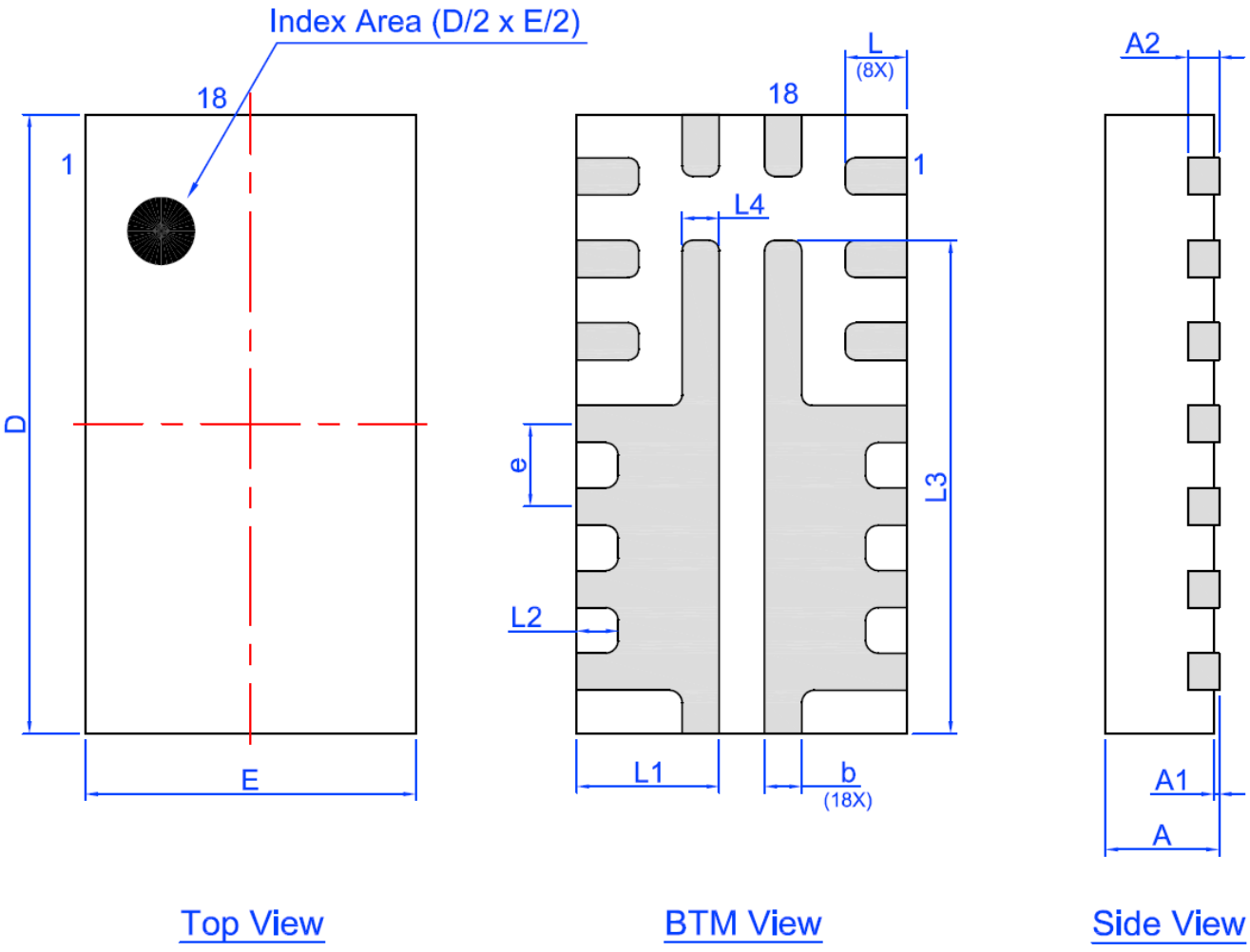
$$PD = (V_{IN} - V_{OUT}) \times I_{ACL}, \text{ or}$$
$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:
PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
V_{OUT} = R_{LOAD} x I_{ACL}

5. Package Information

5.1 Package Outline Drawings

5.1.1. STQFN-18 (1.6mm x 3.0mm x 0.55mm, 0.4mm Pitch) Fused Lead, JEDEC MO-220, Variation WCEE

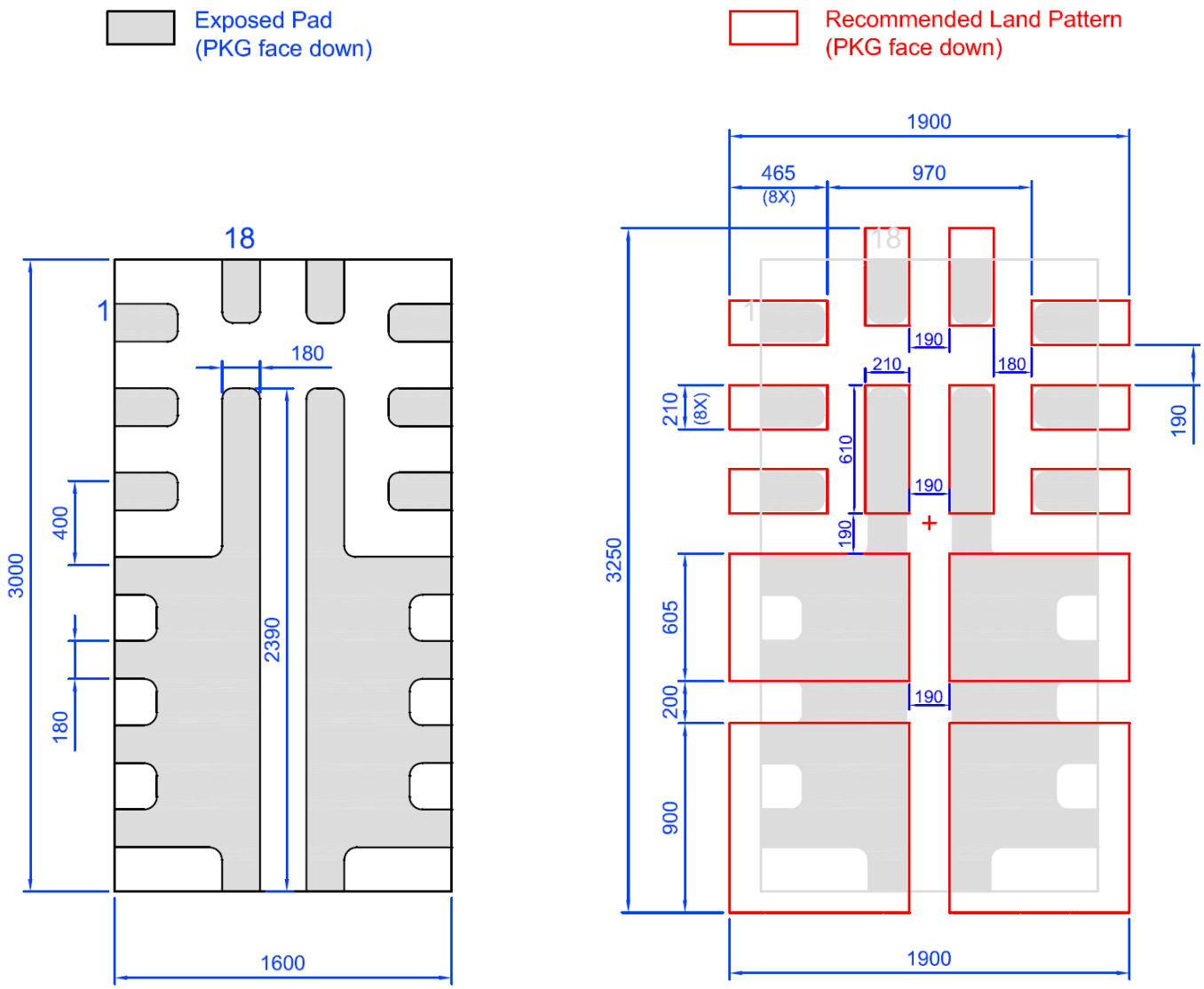


Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
L3	2.34	2.39	2.44	L4	0.13	0.18	0.23

Figure 62. STQFN-18 Package Outline Drawing

5.1.2. STQFN-18 Recommended PCB Landing Pattern



Note 1 All dimensions shown in micrometers (µm).

5.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 6.
For detailed information on MSL levels refer to the IPC / JEDEC standard J-STD-020, which can be downloaded from *http://www.jedec.org.*
The STQFN-18 package is qualified for MSL 1.

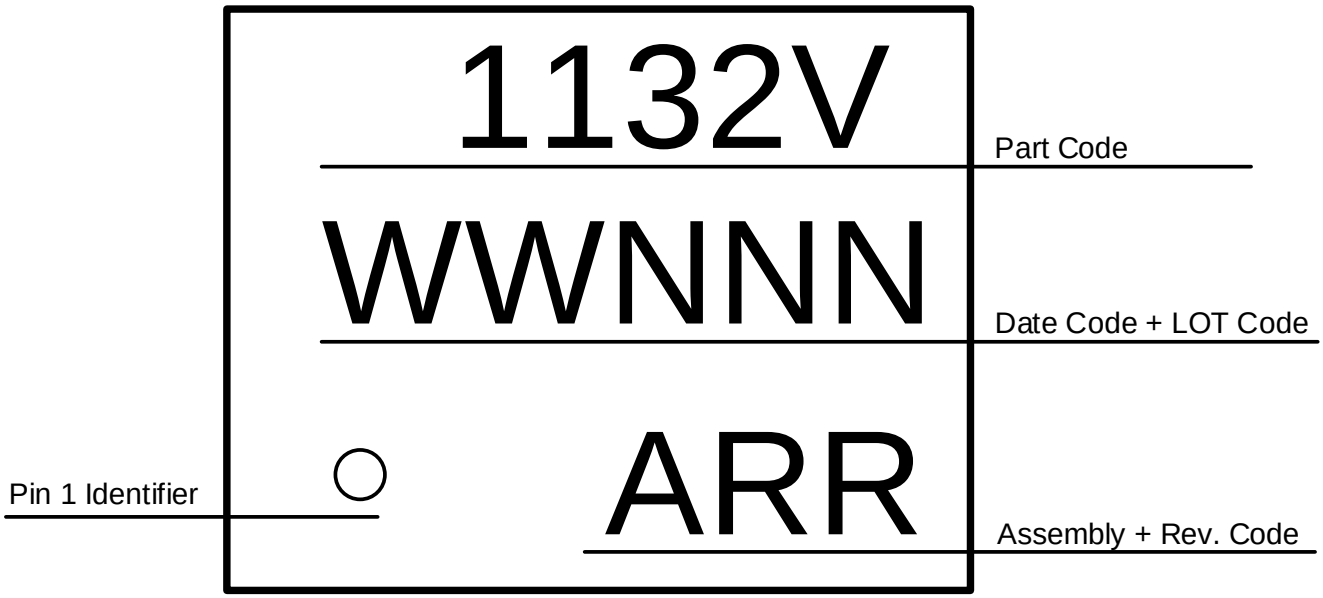
Table 6. MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 Hours	30°C / 60% RH
MSL 3	168 Hours	30°C / 60% RH
MSL 2A	4 Weeks	30°C / 60% RH
MSL 2	1 Year	30°C / 60% RH
MSL 1	Unlimited	30°C / 85% RH

5.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from *http://www.jedec.org*.

6. Marking Diagram



1132V - Part ID Field
WW - Date Code Field[2]
NNN - Lot Traceability Code Field[2]
A - Assembly Site Code Field[3]
RR - Part Revision Code Field[3]

Note 2 Each character in code field can be alphanumeric A-Z and 0-9

Note 3 Character in code field can be alphabetic A-Z

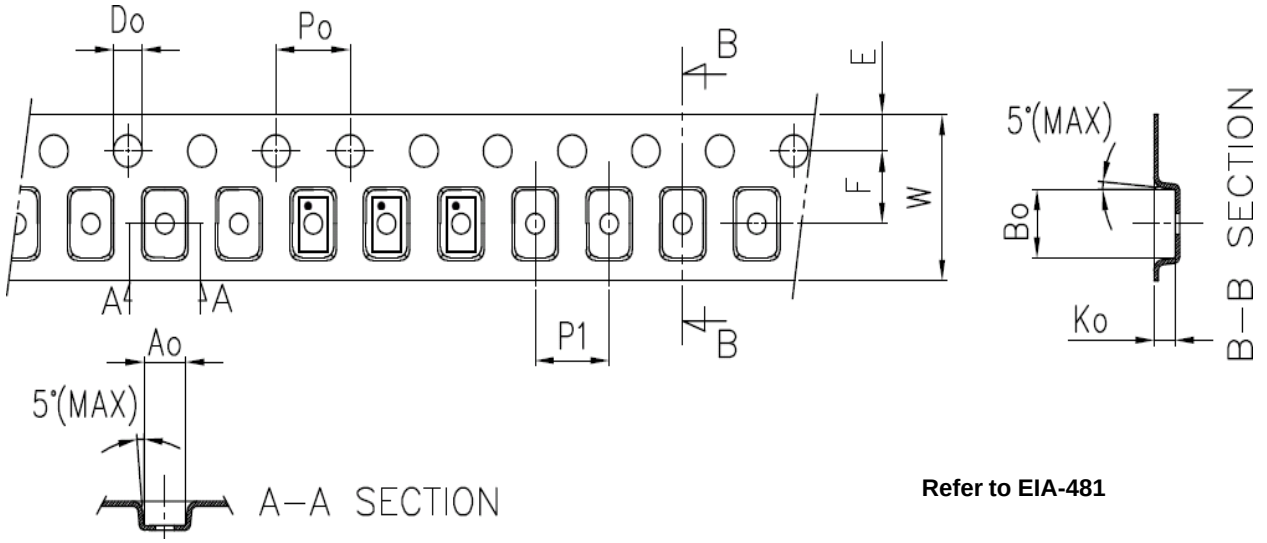
7. Packing Specifications

7.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L 1.6x3mm 0.4P FC Green	18	1.6 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

7.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L 1.6 x 3 mm 0.4P FC Green	1.78	3.18	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481

8. PCB Layout Guidelines

1) Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere;
2) To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59H1132V's VIN and VOUT pins;
3) The GND pin should be connected to system analog or power ground plane.
4) 2 oz. copper is recommended for high current operation.

8.1 SLG59H1132V Evaluation Board

A High Voltage GreenFET Evaluation Board for SLG59H1132V is designed according to the statements above and is illustrated on Figure 63. Please note that evaluation board have Sense pads. They cannot carry high currents and are dedicated only for RDS_{ON} evaluation.

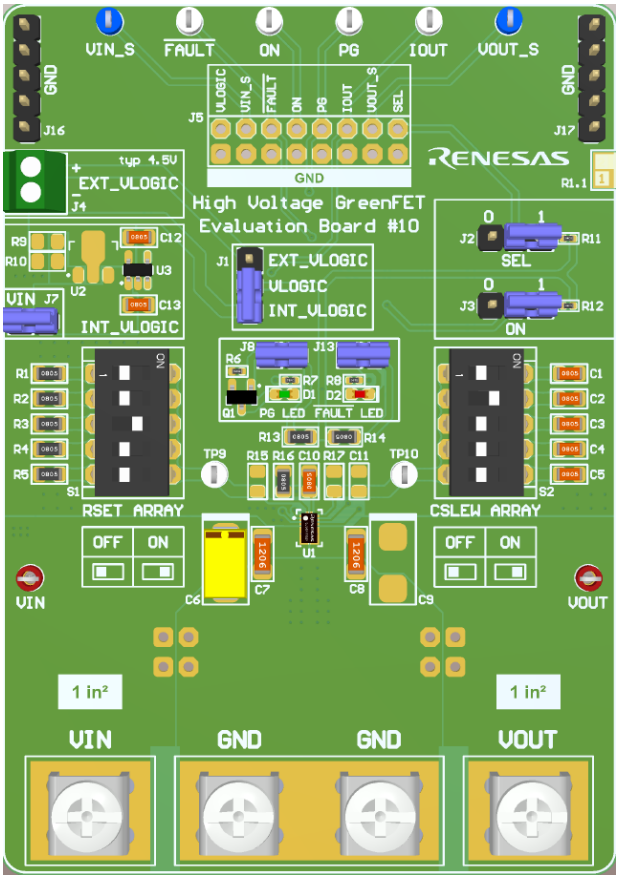


Figure 63. SLG59H1132V Evaluation Board

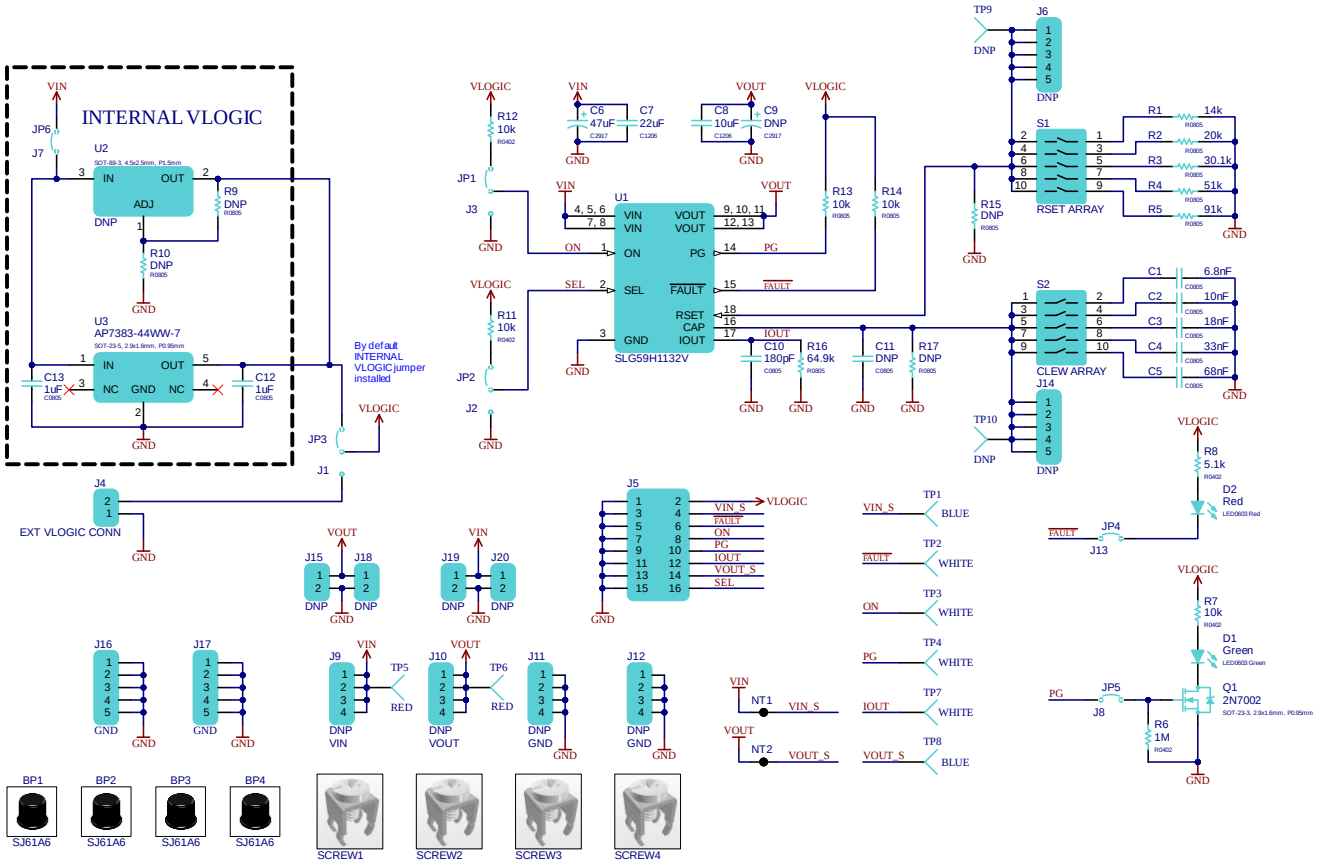


Figure 64. SLG59H1132V Evaluation Board Connection Circuit

8.2 EVB Configuration

1) Based on V_{IN} voltage, set SEL pin to logic Low or logic High to configure V_{IN_OVLO} threshold;
2) Connect oscilloscope probes to VIN, VOUT, ON, SEL etc.;
3) Turn on Power Supply and set desired V_{IN} from 4.5 V…22 V range;
4) Toggle the ON signal High or Low to observe SLG59H1132V operation;
5) A more detailed EVB user guide can be found on the website.

9. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
SLG59H1132V	STQFN-18L, 1.6 mm x 3.0 mm	Tape and Reel	-40°C to +85°C

10. Revision History

Revision	Date	Description
1.01	Dec 09, 2024	Updated Document Number
1.00	Sep 12, 2024	Production release

RoHS Compliance

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