Ultra-small 28.5 mΩ, 1.0 A Load Switch with Discharge

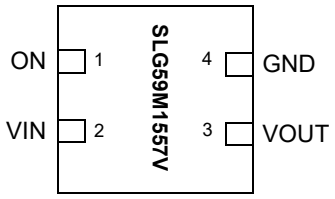
General Description

The SLG59M1557V is designed for load switching applications with ultra low quiescent current. The part comes with one 28.5 mΩ 1.0 A rated P-channel MOSFET controlled by a single ON control pin. The product is packaged in an ultra-small 1.0 x 1.0 mm package.

Features

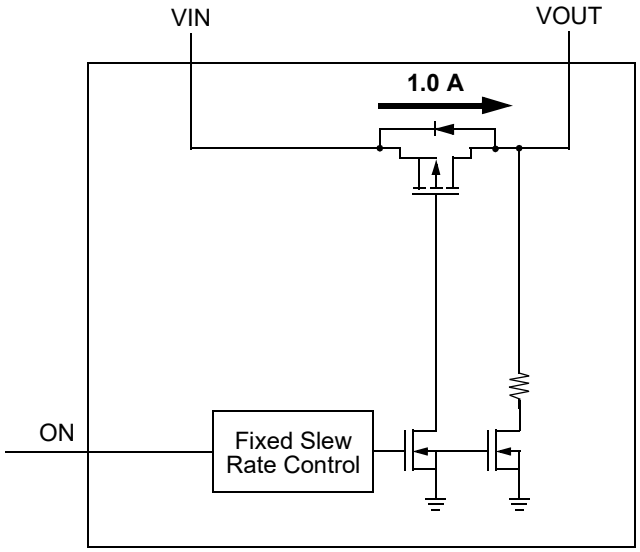
- One 1.0 A MOSFET
- Ultra Low Quiescent Current
- Low RDSON
  - 28.5 mΩ @ 5.0 V
  - 36.4 mΩ @ 3.3 V
  - 44.3 mΩ @ 2.5 V
  - 60.8 mΩ @ 1.8 V
  - 77.6 mΩ @ 1.5 V
- V_{IN} = 1.5 V to 5.5 V
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 4L, 1.0 x 1.0 x 0.55 mm

Pin Configuration



4-pin STDFN
(Top View)

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	Turns on MOSFET.
2	VIN	MOSFET	Power MOSFET input
3	VOUT	MOSFET	Power MOSFET output
4	GND	GND	Ground

Ordering Information

Part Number	Type	Production Flow
SLG59M1557V	STDFN 4L	Industrial, -40 °C to 85 °C
SLG59M1557VTR	STDFN 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply		--	--	6	V
T_S	Storage Temperature		-65	--	140	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W_{DIS}	Package Power Dissipation		--	--	0.5	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

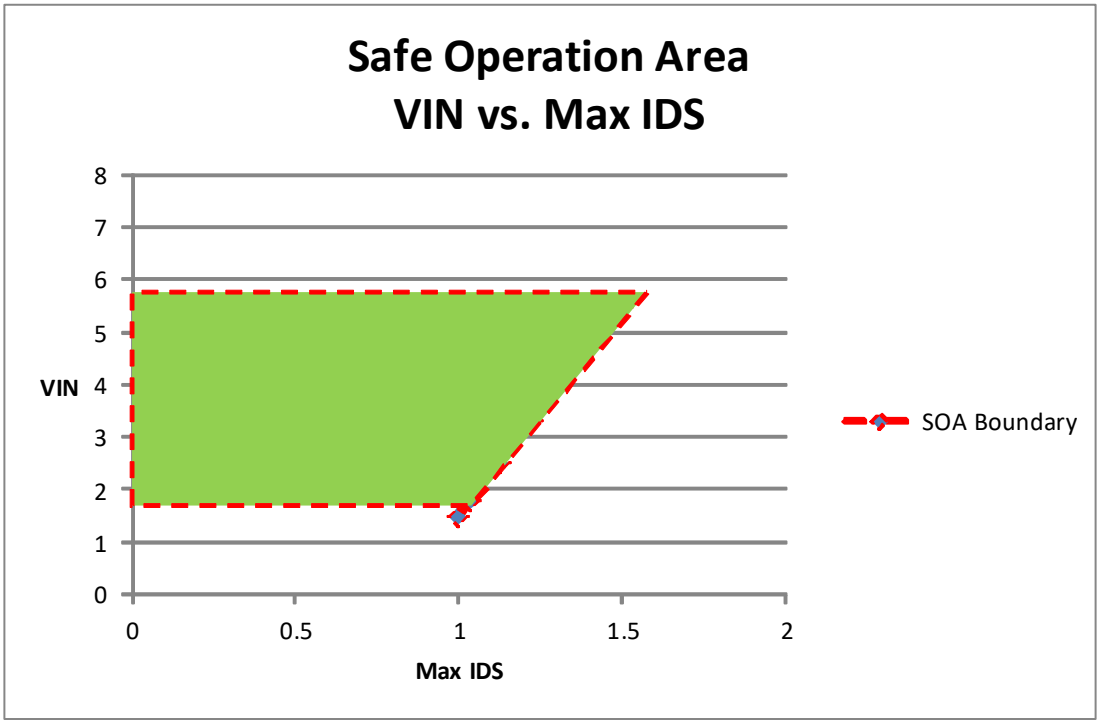
T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply Voltage	-40 °C to 85 °C	1.5	--	5.5	V
I_{DD}	Power Supply Current (PIN 2)	when OFF, V_{IN} = 5.5 V, No load	--	0.02	1	µA
		when ON = V_{IN}, No load	--	0.05	0.5	µA
I_{ON_LKG}	ON Pin Input Leakage		--	--	0.1	µA
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 25°C	@ 5.5 V, 100 mA	--	28.5	32.0	mΩ
		@ 3.3 V, 100 mA	--	36.4	40.0	mΩ
		@ 2.5 V, 100 mA	--	44.3	49.0	mΩ
		@ 1.8 V, 100 mA	--	60.8	65.0	mΩ
		@ 1.5 V, 100 mA	--	77.6	82.0	mΩ
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 85°C	@ 5.5 V, 100 mA	--	34.0	36.0	mΩ
		@ 3.3 V, 100 mA	--	43.8	46.0	mΩ
		@ 2.5 V, 100 mA	--	53.3	56.0	mΩ
		@ 1.8 V, 100 mA	--	72.2	76.0	mΩ
		@ 1.5 V, 100 mA	--	90.7	94.0	mΩ
IDS	Operating Current	V_{IN} = 1.5 V to 5.5 V	--	--	1.0	A
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	10	15	27	µs
		50% ON to Ramp Begin V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	17	31	40	µs
		50% ON to Ramp Begin V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	44	69	96	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% VOUT V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	114	122	134	µs
		50% ON to 90% VOUT V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10Ω	146	156	176	µs
		50% ON to 90% VOUT V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	292	332	399	µs

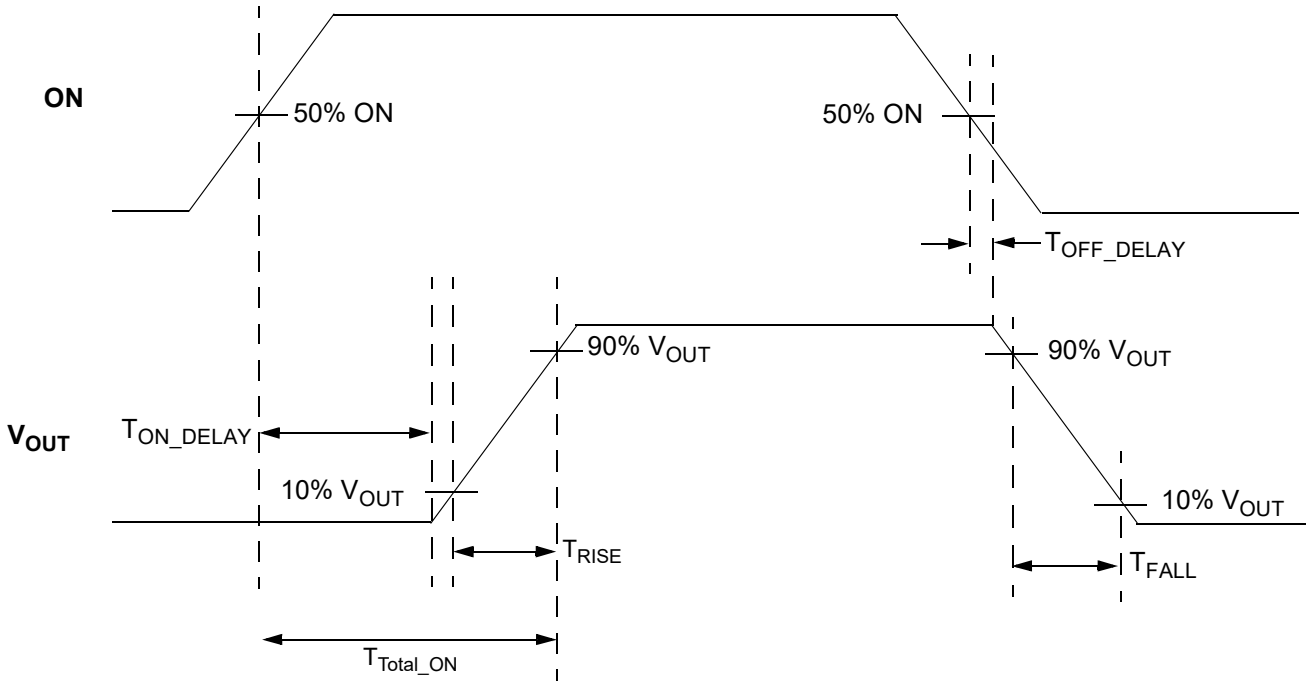
T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{RISE}	Rise Time	10% VOUT to 90% VOUT V_{IN} = 5.0 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	92	97	107	µs
		10% VOUT to 90% VOUT V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	116	120	131	µs
		10% VOUT to 90% VOUT V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	228	253	296	µs
R_{DIS}	Discharge Resistance	V_{IN} = 1.5 V to 5.5 V, V_{OUT} = 0.4 V Input Bias	65	80	400	Ω
ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
T_{Delay_OFF}	OFF Delay Time	50% ON to V_{OUT} Fall, V_{IN} = 5 V, R_L =10 Ω, no C_L	6.2	6.5	7.0	µs

VIN vs. Max IDS, Safe Operation Area



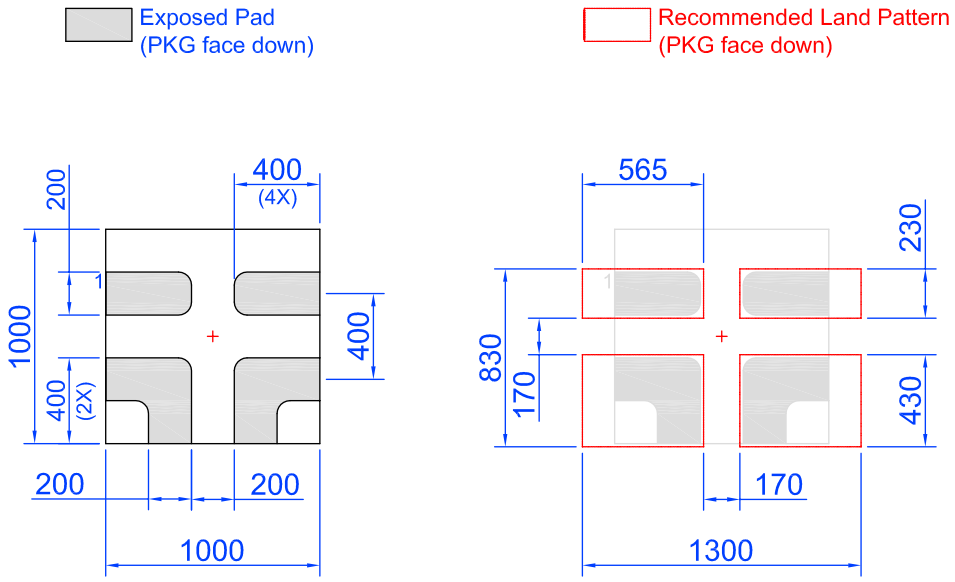
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



SLG59M1557V Power-Up/Power-Down Sequence Considerations

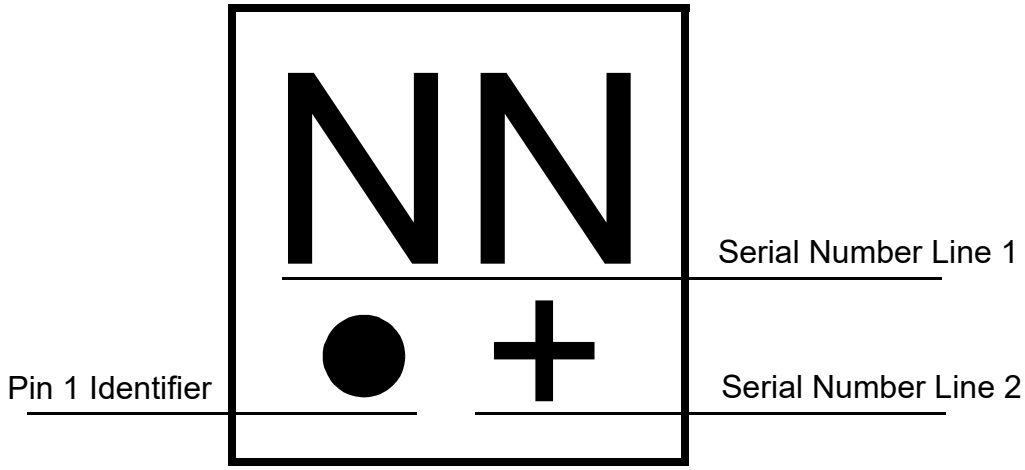
A nominal power-up sequence is to apply VIN and toggle the ON pin LOW-to-HIGH after VIN is at least 90% of its final value. A nominal power-down sequence is the power-up sequence in reverse order. If VIN ramp is too fast, a voltage glitch may appear on the output pin at VOUT. To prevent glitches at the output, it is recommended to connect at least 0.1uF capacitor from the VOUT pin to GND and to keep the VIN ramp time less than 2 ms.

SLG59M1557V Layout Suggestion



Note: All dimensions shown in micrometers (µm)

Package Top Marking System Definition

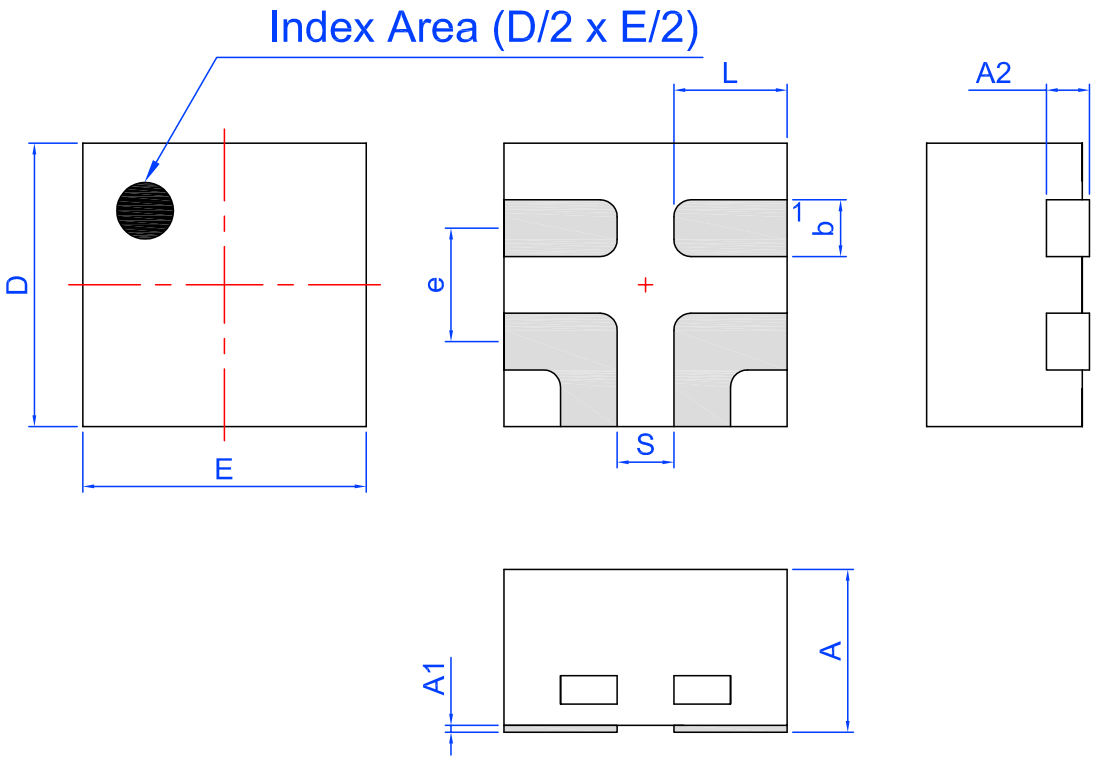


NN - Part Serial Number Field Line 1
where each “N” character can be A-Z and 0-9

+ - Part Serial Number Field Line 2
where “+” character can be +, -, =, or blank

Package Drawing and Dimensions

4 Lead STDFN Package 1.0 x 1.0 mm



Unit: mm

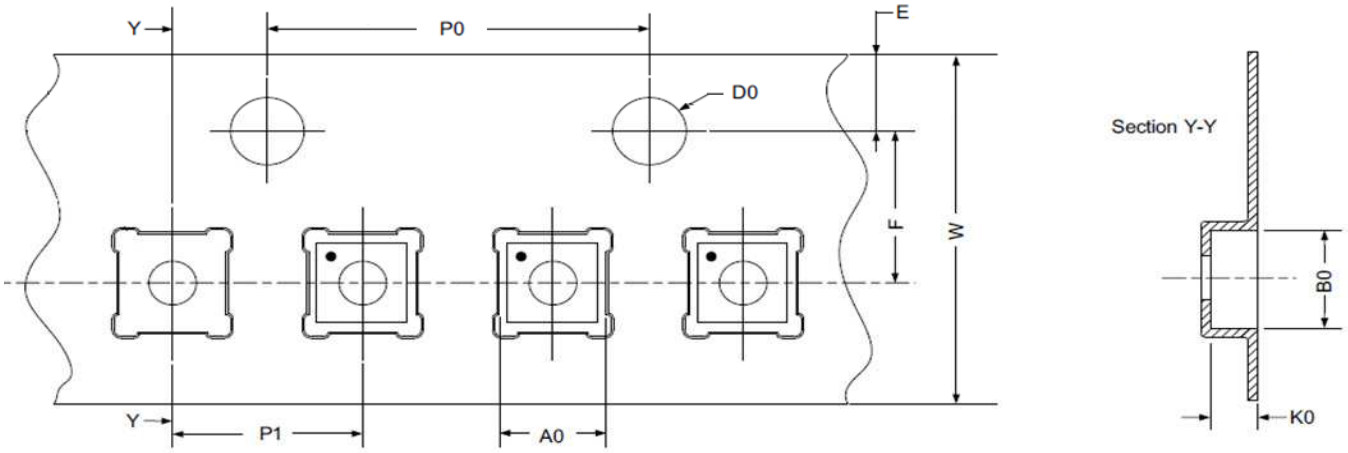
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	0.95	1.00	1.05
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.15	0.20	0.25	S	0.2 REF		
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 4L 1x1mm 0.4P FC Green	4	1.0 x 1.0 x 0.55	8000	8000	178 / 60	200	400	200	400	8	2

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 4L 1x1mm 0.4P FC Green	1.16	1.16	0.63	4	2	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.55 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/4/2022	1.04	Updated Company name and logo Fixed typos
11/14/2017	1.03	Updated Package Marking Definition
6/22/2016	1.02	Added section on Power Up/Down Sequence Considerations Removed IDS_lkg parameter (same as IDD when OFF) Updated Recommended Layout suggestion
9/11/2015	1.01	Updated IDD and Tdelay_ON

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