An Ultra-small 1.0 mm^2, 28.5 mΩ, 1.0 A, Load Switch

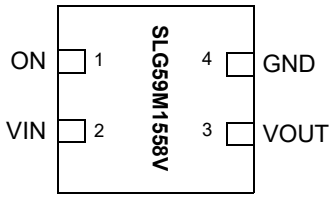
General Description

The SLG59M1558V is designed for load switching applications with ultra low quiescent current. The part comes with one 28.5 mΩ, 1.0 A rated P-channel MOSFET controlled by a single ON control pin. The product is packaged in an ultra-small 1.0 mm x 1.0 mm package.

Features

- One 1.0 A MOSFET
- Ultra Low Quiescent Current
- Low RDS_{ON}
  - 28.5 mΩ at V_{IN} = 5.0 V
  - 36.4 mΩ at V_{IN} = 3.3 V
  - 44.3 mΩ at V_{IN} = 2.5 V
  - 60.8 mΩ at V_{IN} = 1.8 V
  - 77.6 mΩ at V_{IN} = 1.5 V
- V_{IN} = 1.5 V to 5.5 V
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 4L, 1.0 x 1.0 x 0.55 mm

Pin Configuration

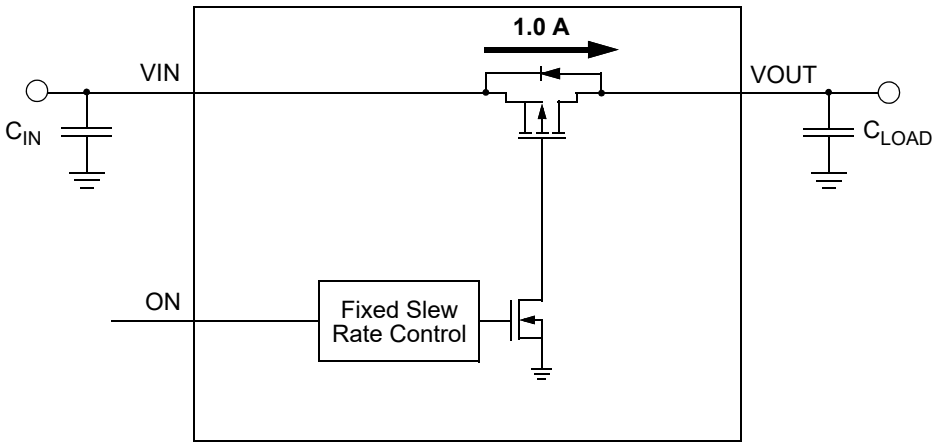


4-pin STDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1558V. ON is an asserted HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 0.85 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
2	VIN	MOSFET	Input terminal connection of the power MOSFET. Connect a 10 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 10 V or higher.
3	VOUT	MOSFET	Output terminal connection of the power MOSFET. Capacitors used at VOUT should be rated at 10 V or higher.
4	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1558V	STDFN 4L	Industrial, -40 °C to 85 °C
SLG59M1558VTR	STDFN 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Load Switch Input Voltage		--	--	6	V
T_S	Storage Temperature		-65	--	140	°C
T_J	Junction Temperature		-40	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
MSL	Moisture Sensitivity Level			1		
θ_{JA}	Thermal Resistance	1.0 x 1.0 mm, 4L STDFN; Determined using 1 in^2, 2 oz. copper pads under each VIN and VOUT terminals and FR4 pcb material	--	122	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.5	W
MOSFET IDS_{PEAK}	Peak Current from VIN to VOUT	For no more than 1 ms with 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C unless otherwise noted. Typical values are at T_A = 25 °C

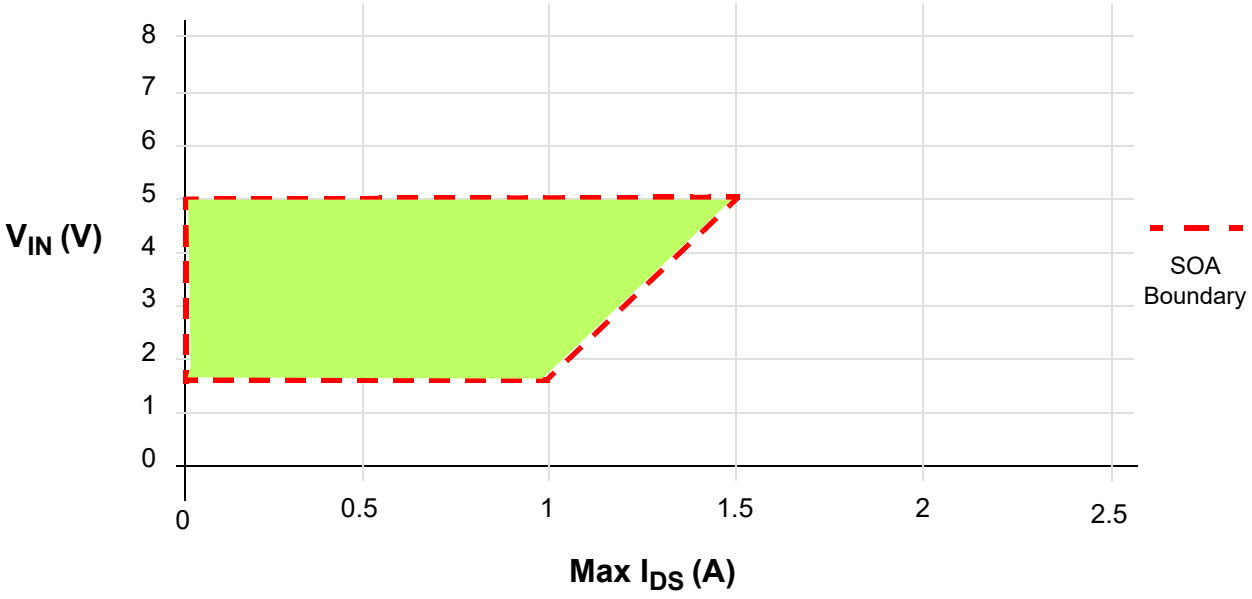
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Load Switch Input Voltage	-40 °C to 85 °C	1.5	--	5.5	V
I_{IN}	Load Switch Input Current (PIN 2)	when OFF, V_{IN} = 5.5 V, No load	--	0.02	1	µA
		when ON, ON = V_{IN}, No load	--	0.05	0.5	µA
I_{FET_OFF}	MOSFET OFF Leakage Current	ON = LOW; V_{IN} = 5.5 V	--	0.05	1	µA
I_{ON_LKG}	ON Pin Input Leakage		--	--	0.1	µA
RDS_{ON}	ON Resistance, T_A = 25 °C	V_{IN} = 5.5 V, I_{DS} = 100 mA	--	28.5	32.0	mΩ
		V_{IN} = 3.3 V, I_{DS} = 100 mA	--	36.4	40.0	mΩ
		V_{IN} = 2.5 V, I_{DS} = 100 mA	--	44.3	49.0	mΩ
		V_{IN} = 1.8 V, I_{DS} = 100 mA	--	60.8	65.0	mΩ
		V_{IN} = 1.5 V, I_{DS} = 100 mA	--	77.6	82.0	mΩ
RDS_{ON}	ON Resistance, T_A = 85 °C	V_{IN} = 5.5 V, I_{DS} = 100 mA	--	34.0	36.0	mΩ
		V_{IN} = 3.3 V, I_{DS} = 100 mA	--	43.8	46.0	mΩ
		V_{IN} = 2.5 V, I_{DS} = 100 mA	--	53.3	56.0	mΩ
		V_{IN} = 1.8 V, I_{DS} = 100 mA	--	72.2	76.0	mΩ
		V_{IN} = 1.5 V, I_{DS} = 100 mA	--	90.7	94.0	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	1.0	A

Electrical Characteristics (continued)

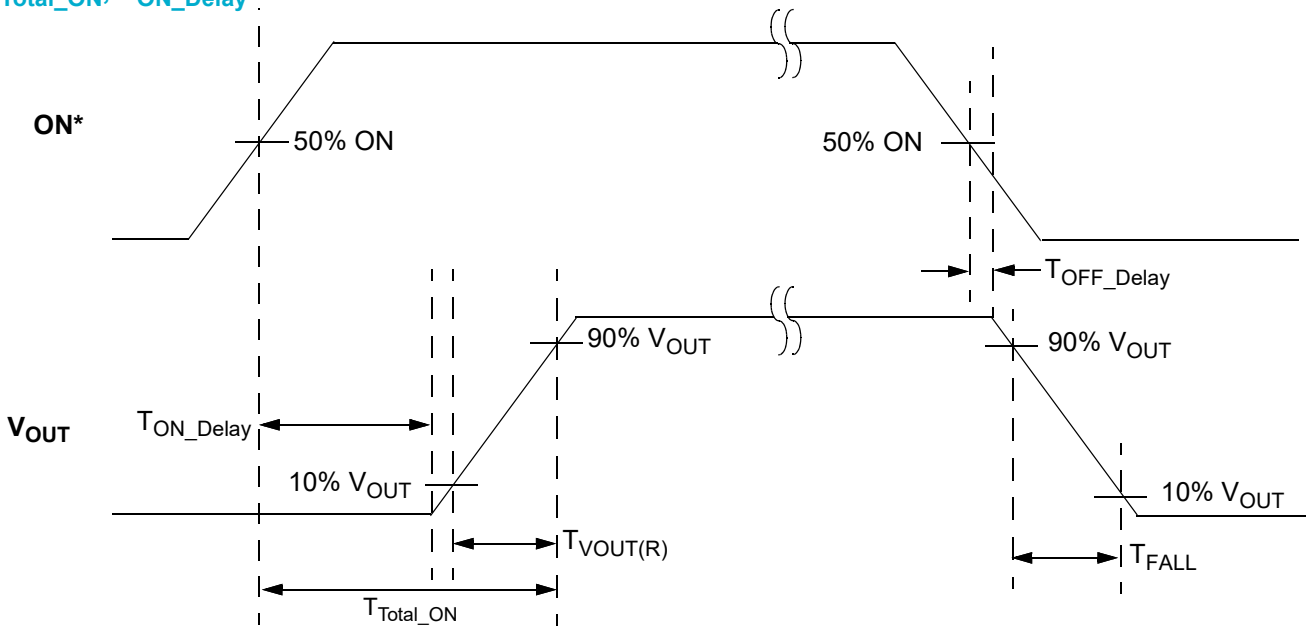
T_A = -40 °C to 85 °C unless otherwise noted. Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{ON_Delay}	ON Delay Time	50% ON to V_{OUT} Ramp Start; V_{IN} = 5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	10	15	27	µs
		50% ON to V_{OUT} Ramp Start; V_{IN} = 3.3 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	17	31	40	µs
		50% ON to V_{OUT} Ramp Start; V_{IN} = 1.5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	44	69	96	µs
T_{Total_ON}	Total Turn ON Time	50% ON to 90% V_{OUT}; V_{IN} = 5.0 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	114	122	134	µs
		50% ON to 90% V_{OUT}; V_{IN} = 3.3 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	146	156	176	µs
		50% ON to 90% V_{OUT}; V_{IN} = 1.5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	292	332	399	µs
$T_{VOUT(R)}$	V_{OUT} Rise Time	10% V_{OUT} to 90% V_{OUT}; V_{IN} = 5.0 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	92	97	107	µs
		10% V_{OUT} to 90% V_{OUT}; V_{IN} = 3.3 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	116	120	131	µs
		10% V_{OUT} to 90% V_{OUT}; V_{IN} = 1.5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω	228	253	296	µs
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{IN}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start, V_{IN} = 5 V, R_{LOAD} = 10 Ω, no C_{LOAD}	6.2	6.5	7.0	µs

V_{IN} vs. Max I_{DS}, Safe Operation Area



T_{Total_ON}, T_{ON_Delay} and Rise Time Measurement



*Rise and Fall Times of the ON Signal are 100 ns

SLG59M1558V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{IN} and toggle the ON pin LOW-to-HIGH after V_{IN} is at least 90% of its final value. A nominal power-down sequence is the power-up sequence in reverse order. If V_{IN} ramp is too fast, a voltage glitch may appear on the output pin at VOUT. To prevent glitches at the output, it is recommended to connect at least 0.1uF capacitor from the VOUT pin to GND and to keep the V_{IN} ramp time higher than 2 ms.

Power Dissipation Considerations

The junction temperature of the SLG59M1558V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON} generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1558V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON}= Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59M1558V's power dissipation can also be calculated by taking into account the voltage drop across the load switch (V_{IN} - V_{OUT}) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} – (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

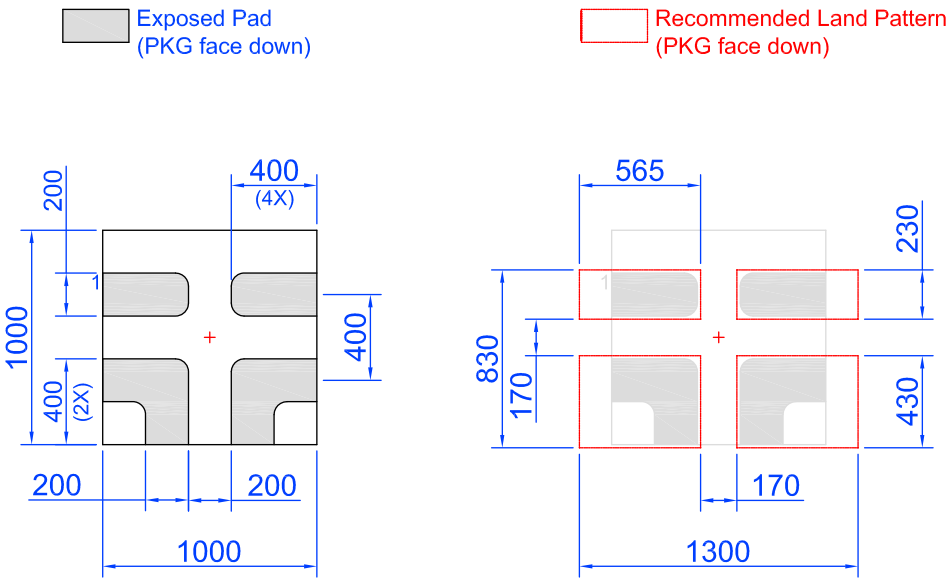
V_{IN} = Switch input Voltage, in Volts (V)

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

I_{DS} = Switch output current, in Amps (A)

V_{OUT} = Switch output voltage, or $R_{LOAD} \times I_{DS}$

SLG59M1558V Layout Suggestion



Note: All dimensions shown in micrometers (µm)

Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1 illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1558V's VIN and VOUT pins;

3. The GND pin should be connected to system analog or power ground plane.

4. 2 oz. copper is recommended for high current operation.

SLG59M1558V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1558V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1558V here

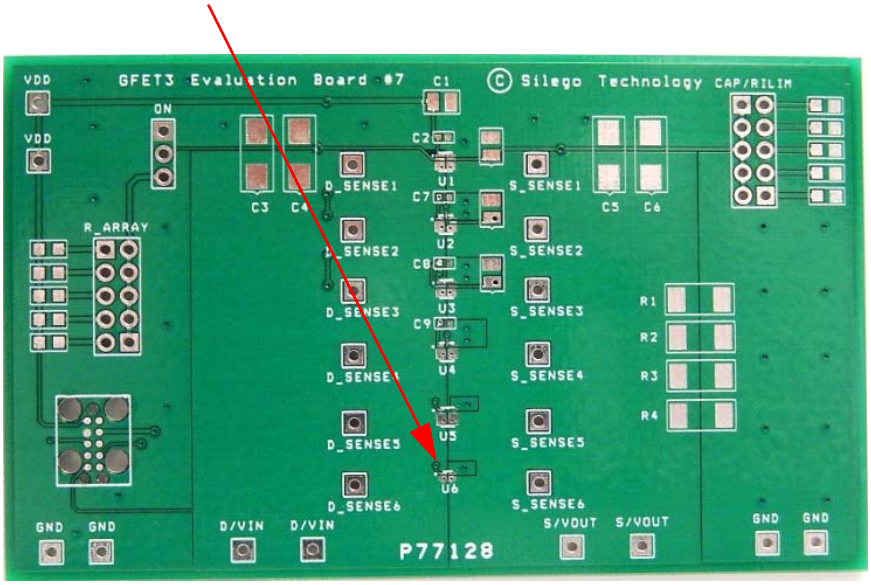


Figure 1. SLG59M1558V Evaluation Board

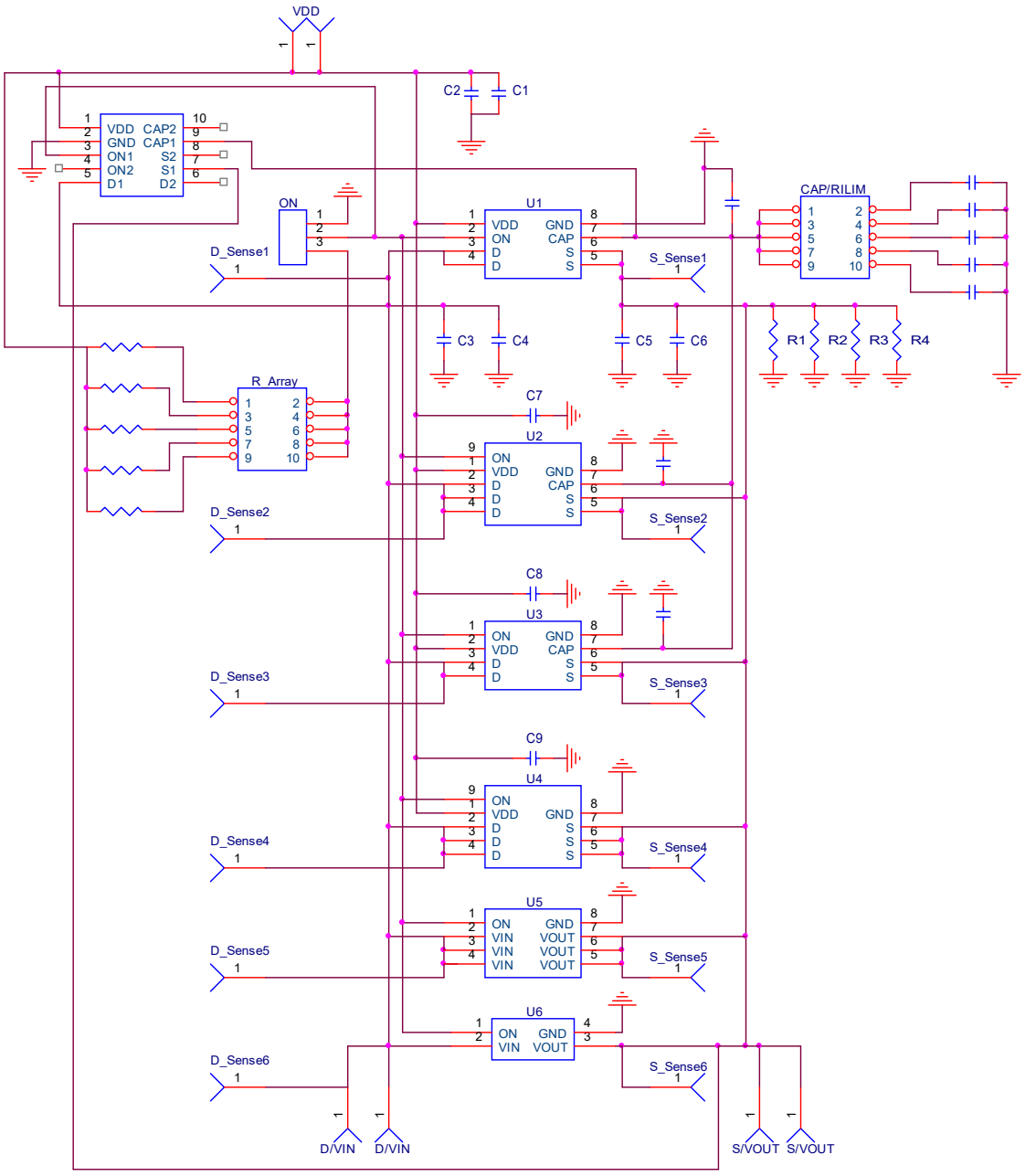


Figure 2. SLG59M1558V Evaluation Board Connection Circuit

Basic Test Setup and Connections

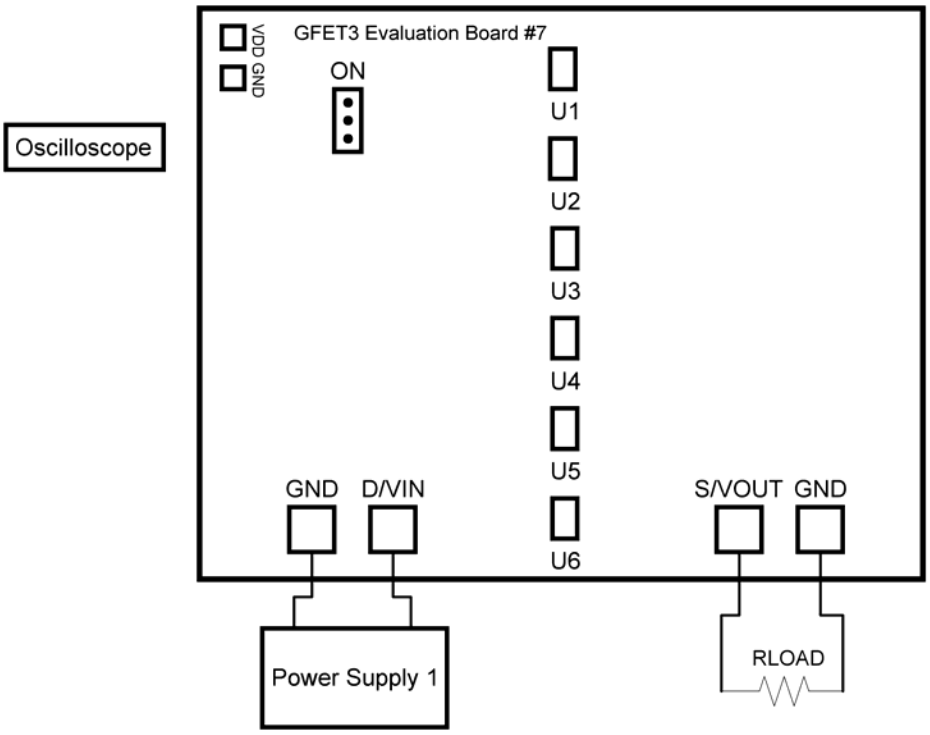


Figure 3. SLG59M1558V Evaluation Board Connection Circuit

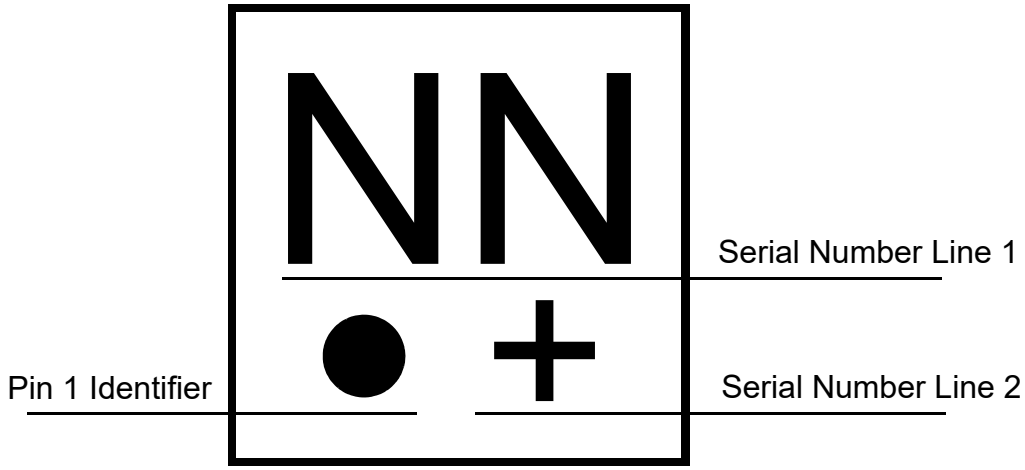
EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2. Turn on Power Supply 1 and set desired V_{IN} from 1.5 V…5.5 V range;

3. Toggle the ON signal High or Low to observe SLG59M1558V operation.

Package Top Marking System Definition

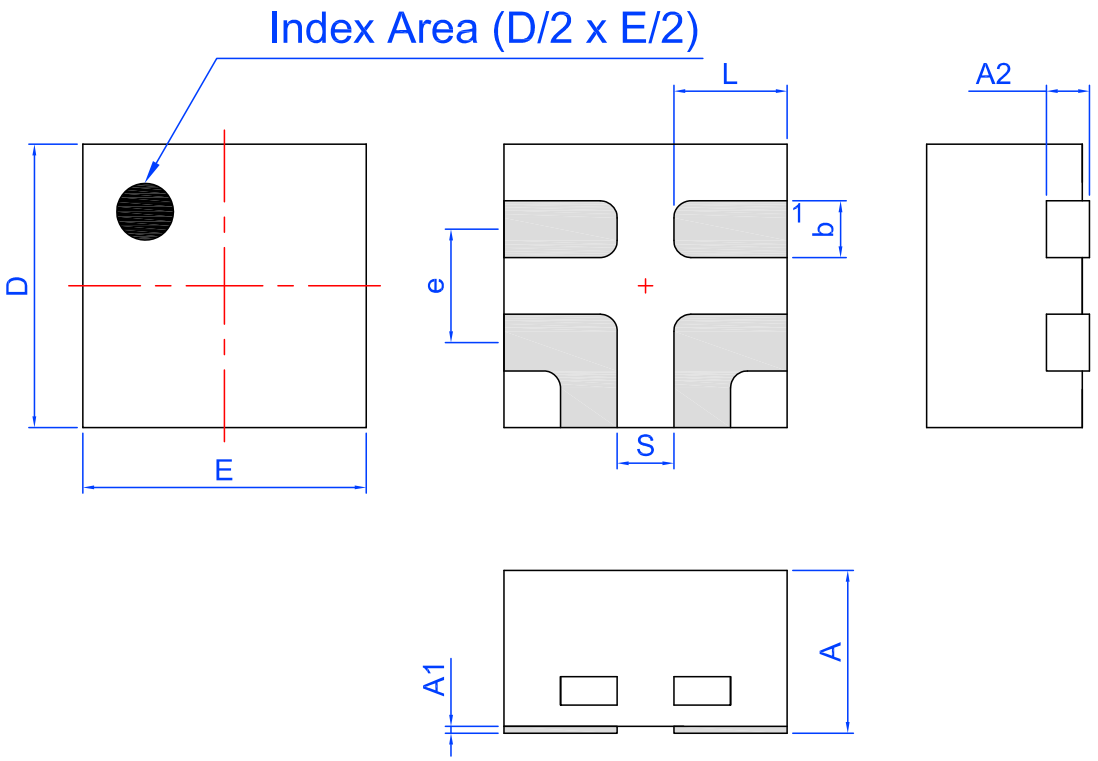


NN - Part Serial Number Field Line 1
where each “N” character can be A-Z and 0-9

+ - Part Serial Number Field Line 2
where “+” character can be +, -, =, or blank

Package Drawing and Dimensions

4 Lead STDFN Package 1.0 x 1.0 mm



Unit: mm

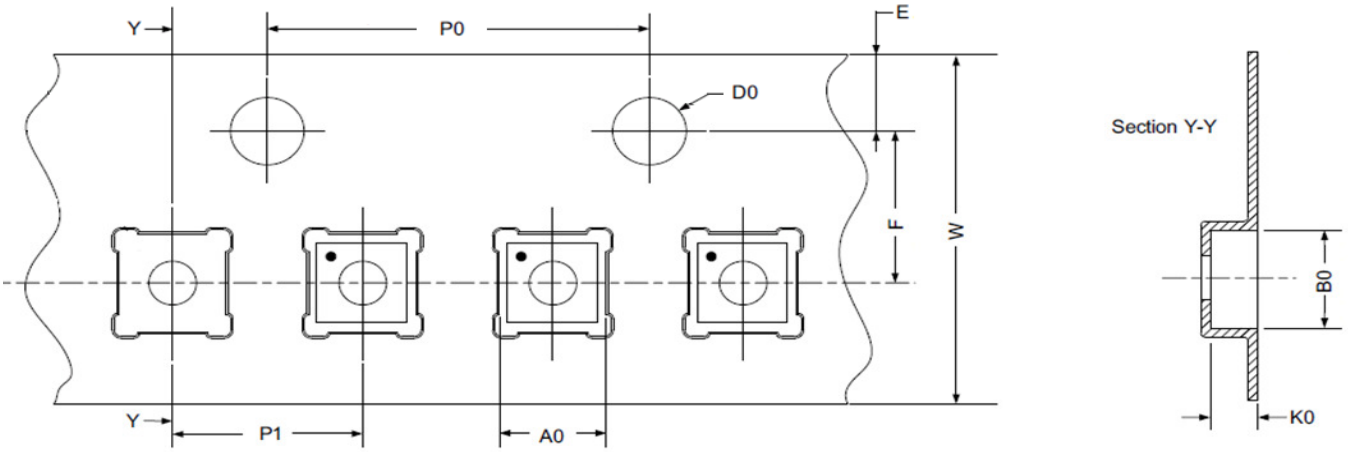
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	0.95	1.00	1.05
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.15	0.20	0.25	S	0.2 REF		
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 4L Green	4	1.0 x 1.0 x 0.55	8000	8000	178 / 60	200	400	200	400	8	2

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 4L Green	1.16	1.16	0.63	4	2	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.55 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
8/7/2023	1.08	Fixed typo in Title
2/2/2022	1.07	Updated Company name and logo Fixed typos
10/27/2020	1.06	Added MSL to Abs Max Table
6/10/2020	1.05	Updated Style and formatting Added Power Dissipation Considerations Added Layout Guidelines Fixed typos
11/14/2017	1.04	Updated Package Marking Definition
11/30/2016	1.03	Fixed Parameter name from VDD to VIN in Abs. Max Table
6/22/2016	1.02	Added section on Power Up/Down Sequence Considerations Removed IDS_lkg parameter (same as IDD when OFF) Updated Recommended Layout suggestion
9/11/2015	1.01	Updated IDD and Tdelay_ON

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