

SLG59M1655V

An Ultra-small, 7.8 mΩ, 9 A, Single-channel Load Switch with Reverse-current Blocking

General Description

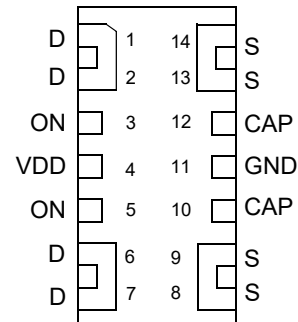
The SLG59M1655V is a high-performance 7.8 mΩ nFET load switch designed for all 0.85 V to 5.5V power rail applications up to 9 A. Incorporating reverse-current blocking, the SLG59M1655V is uniquely suited for those power rail applications where output-to-input voltage backfeed conditions are to be avoided. Using a proprietary MOSFET design, the SLG59M1655V achieves its stable 7.8 mΩ $R_{DS(ON)}$ across a wide input/supply voltage range. Using Renesas's proprietary CuFET technology, the SLG59M1655V package also exhibits low thermal resistance for high-current operation.

Fully specified over the -40 °C to 85 °C temperature range, the SLG59M1655V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.0 mm x 3.0 mm STDFN package.

Features

- High-performance MOSFET Switch Design
 - Low Typical $R_{DS(ON)}$: 7.8 mΩ
- Steady-state Operating Current: Up to 9 A
- FET Bulk-switch Reverse-current Blocking
- Supply Voltage: $2.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
- Wide Input Voltage Range: $0.85\text{ V} \leq V_D \leq V_{DD}$
- Capacitor-adjustable Start-up and Inrush Current Control
- Internal MOSFET Gate Driver
- Thermal Shutdown Protection
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA} , 14-pin 1.0 mm x 3.0 mm STDFN Packaging
- Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

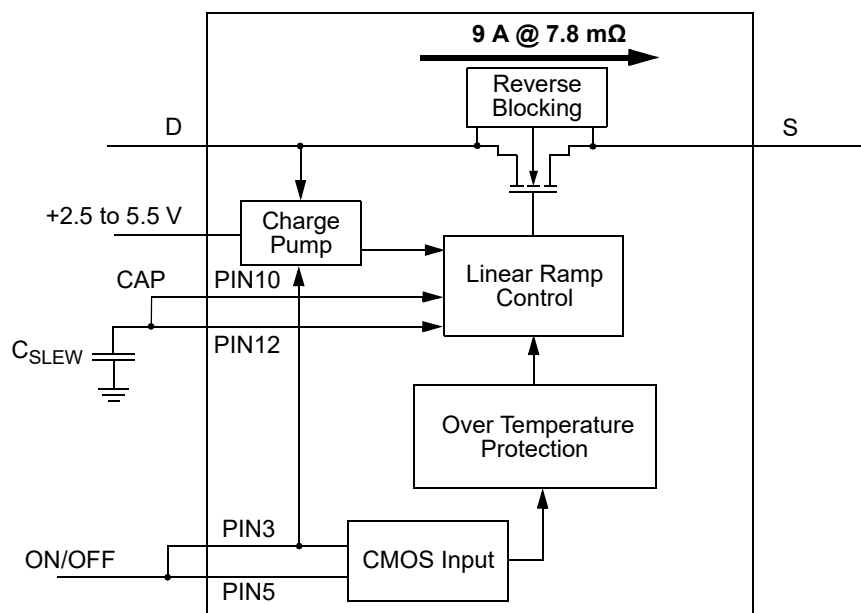


14-pin STDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



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Pin Description

| Pin # | Pin Name | Type | Pin Description |
|--------------|----------|--------|---|
| 1, 2, 6, 7 | D | MOSFET | Drain terminal connections of the n-channel MOSFET. Connect a low-ESR 10-μF (or larger) capacitor from the D pins (Pins 1, 2, 6, and 7) to ground. Capacitors used at V_D should be rated at 10 V or higher. |
| 3, 5 | ON | Input | A low-to-high transition on these pins initiates the operation of the SLG59M1655V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $ON_V_{IL} < 0.3$ V and $ON_V_{IH} > 0.85$ V. While there is an internal pull-down circuit to GND (~4 MΩ), connect these pins directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller. |
| 4 | VDD | VDD | VDD supplies the power for the operation of the load switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 μF (or larger) capacitor. |
| 8, 9, 13, 14 | S | MOSFET | Source terminal connections of the n-channel MOSFET. Connect a low-ESR 10-μF (up to C_{LOAD}) capacitor from the S pins (Pins 8, 9, 13, and 14) to ground. Capacitors used at V_S should be rated at 10 V or higher. |
| 10, 12 | CAP | Input | A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from the CAP pins (Pins 10 & 12) to GND sets the V_S slew rate and overall turn-on time of the SLG59M1655V. For additional information, please consult the C_{SLEW} typical performance characteristics on Page 5. Capacitors used at C_{SLEW} should be rated at 10 V or higher. |
| 11 | GND | GND | Ground connection. Connect this pin to the system's analog or power ground plane. |

Ordering Information

| Part Number | Type | Production Flow |
|---------------|---------------------------|-----------------------------|
| SLG59M1655V | STDFN 14L | Industrial, -40 °C to 85 °C |
| SLG59M1655VTR | STDFN 14L (Tape and Reel) | Industrial, -40 °C to 85 °C |

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Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|---|--|------|------|------|------|
| V _{DD} | Power Supply | | -- | -- | 6 | V |
| T _S | Storage Temperature | | -65 | -- | 150 | °C |
| ESD _{HBM} | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| ESD _{CDM} | ESD Protection | Charged Device Model | 1000 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | 1 | | | |
| θ _{JA} | Package Thermal Resistance, Junction-to-Ambient | 1mm x 3mm 14L STDFN; Determined using 1 in ² , 1.2 oz. copper pads under VIN and VOUT on FR4 pcb material | -- | 71 | -- | °C/W |
| W _{DIS} | Package Power Dissipation | | -- | -- | 1.2 | W |
| MOSFET I _{DS} CONT | Max Continuous Switch Current | | | | 9 | A |
| MOSFET I _{DS} PK | Peak Current from Drain to Source | For no more than 10 continuous seconds out of every 100 seconds | -- | -- | 12 | A |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C, unless otherwise noted.

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------------------|--|--|--|------|-----------------|------|
| V _{DD} | Power Supply Voltage | | 2.5 | -- | 5.5 | V |
| I _{DD} | Power Supply Current, when OFF | | -- | 0.1 | 1 | μA |
| | Power Supply Current, when ON | | -- | 50 | 100 | μA |
| RDS _{ON} | ON Resistance | T _A 25°C, I _{DS} = 0.1 A | -- | 7.8 | 10.5 | mΩ |
| | | T _A 70°C, I _{DS} = 0.1 A | -- | 9.0 | 12.1 | mΩ |
| | | T _A 85°C, I _{DS} = 0.1 A | | 8.4 | 12.7 | mΩ |
| MOSFET I _{DS} | Current from Drain to Source | Continuous | -- | -- | 9 | A |
| I _{DS} LKG | I _{DS} Leakage (Reverse Blocking enabled) | V _S = 1.0 V to 5.0 V, V _{DD} = V _D = 0 V, ON = LOW | -- | 0.5 | 5.0 | μA |
| V _D | Drain Voltage | | 0.85 | -- | V _{DD} | V |
| T _{ON} Delay | ON Delay Time | 50% ON to V _S Ramp Start, R _{LOAD} = 20 Ω, C _{LOAD} = 10 μF, | -- | 270 | 500 | μs |
| T _{Total} ON | Total Turn On Time | 50% ON to 90% V _S | Set by External C _{SLEW} ¹ | | | ms |
| | | Example: C _{SLEW} = 4 nF, V _{DD} = V _D = 5 V, R _{LOAD} = 20 Ω, C _{LOAD} = 10 μF | -- | 1.1 | -- | ms |
| V _S (SR) | V _S Slew Rate | 10% V _S to 90% V _S | Set by External C _{SLEW} ¹ | | | V/ms |
| | | Example: C _{SLEW} = 4 nF, V _{DD} = V _D = 5 V, R _{LOAD} = 20 Ω, C _{LOAD} = 10 μF | -- | 6.0 | -- | V/ms |

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Electrical Characteristics (continued)

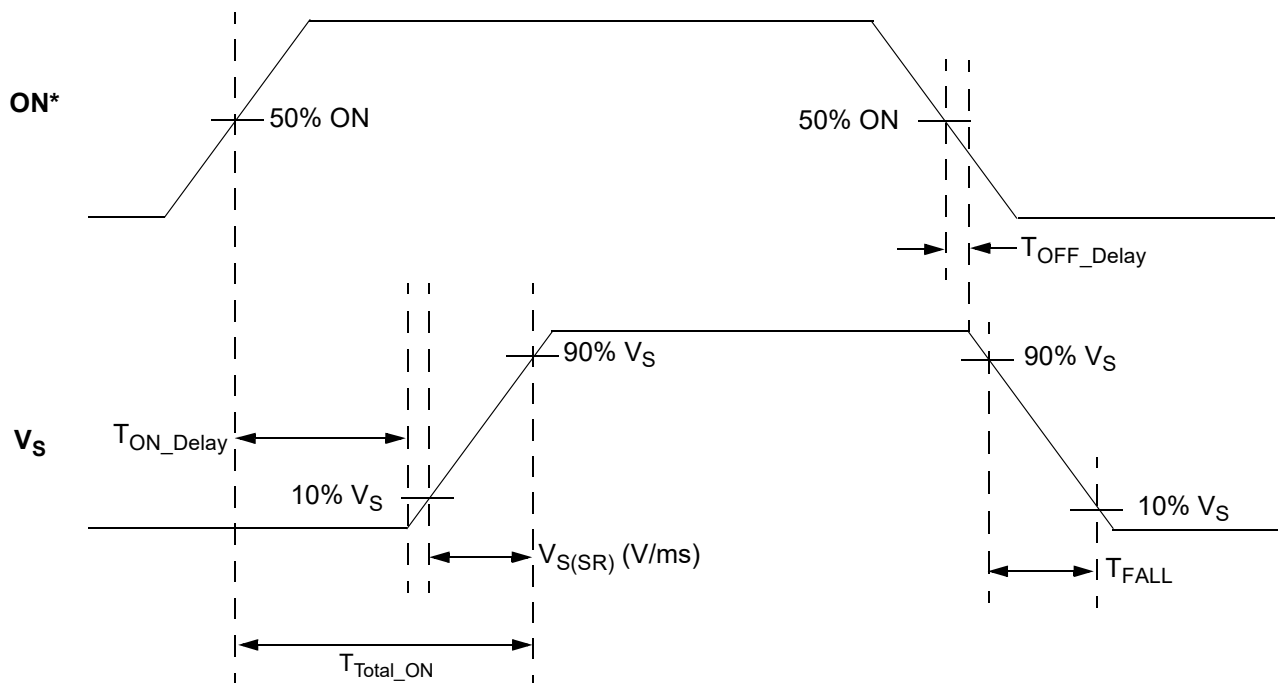
$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise noted.

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------------|---|------|------|----------|--------------------|
| T_{OFF_Delay} | OFF Delay Time | 50% ON to V_S Fall Start, $V_{DD} = V_D = 5\text{ V}$, $R_{LOAD} = 20\ \Omega$, no C_{LOAD} | -- | 1.7 | 3 | μs |
| ON_V_{IH} | High Input Voltage on ON pin | | 0.85 | -- | V_{DD} | V |
| ON_V_{IL} | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| C_{LOAD} | Output Load Capacitance | C_{LOAD} connected from S to GND | -- | -- | 1000 | μF |
| $THERM_{ON}$ | Thermal shutoff turn-on temperature | | -- | 125 | -- | $^{\circ}\text{C}$ |
| $THERM_{OFF}$ | Thermal shutoff turn-off temperature | | -- | 100 | -- | $^{\circ}\text{C}$ |
| $THERM_{TIME}$ | Thermal shutoff time | | -- | -- | 1 | ms |

Notes:

1. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information when available.

T_{ON_Delay} , $V_{S(SR)}$, and T_{Total_ON} Timing Details



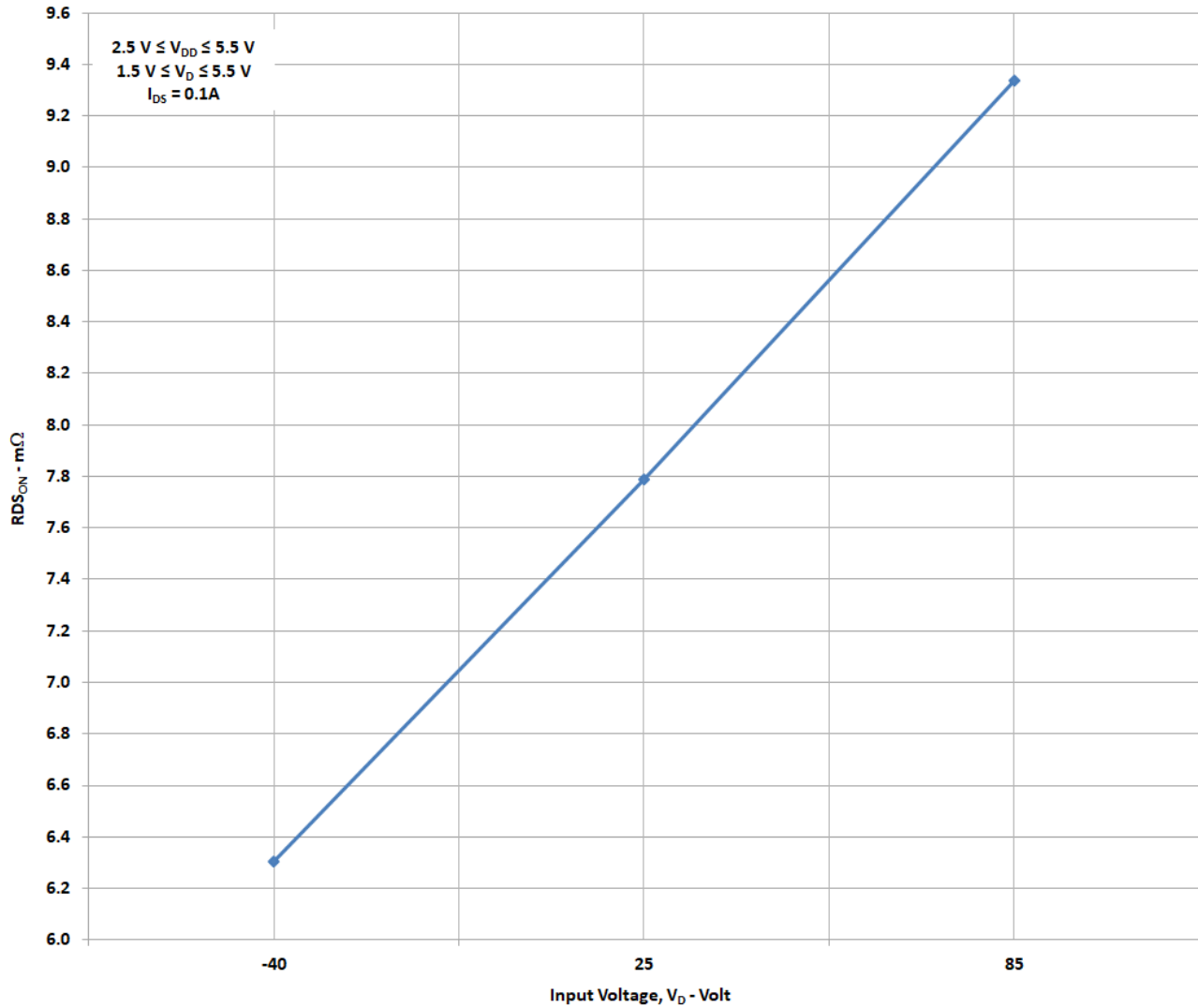
Note: *Rise and Fall Times of the ON Signal are 100 ns

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Typical Performance Characteristics

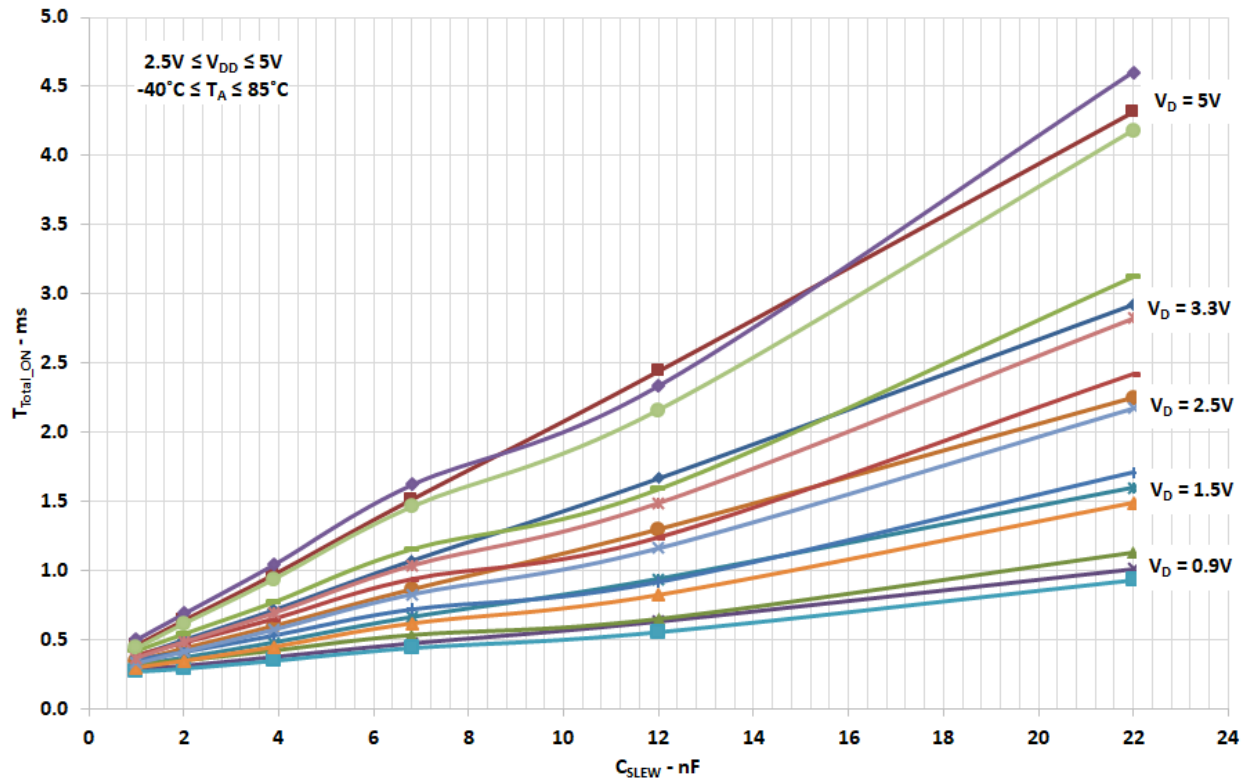
RDS_{ON} vs. Temperature, V_{DD}, and V_D



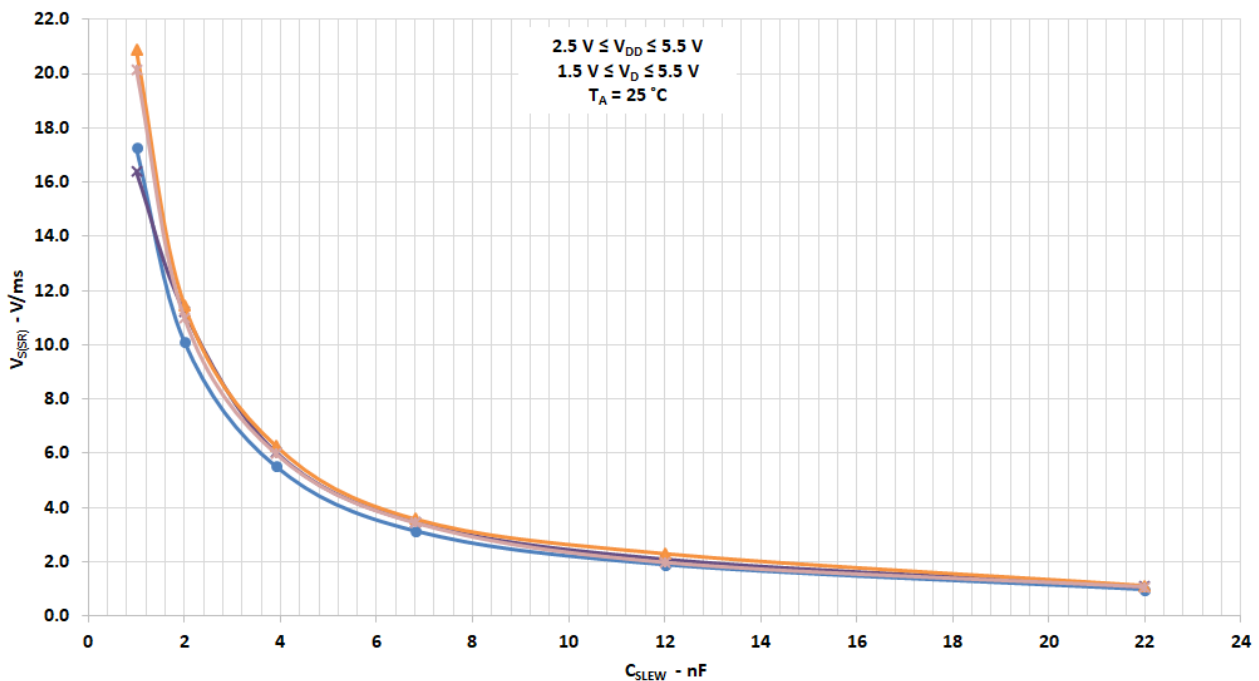
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T_{Total_ON} vs. C_{SLEW}, V_{DD}, V_D, and Temperature



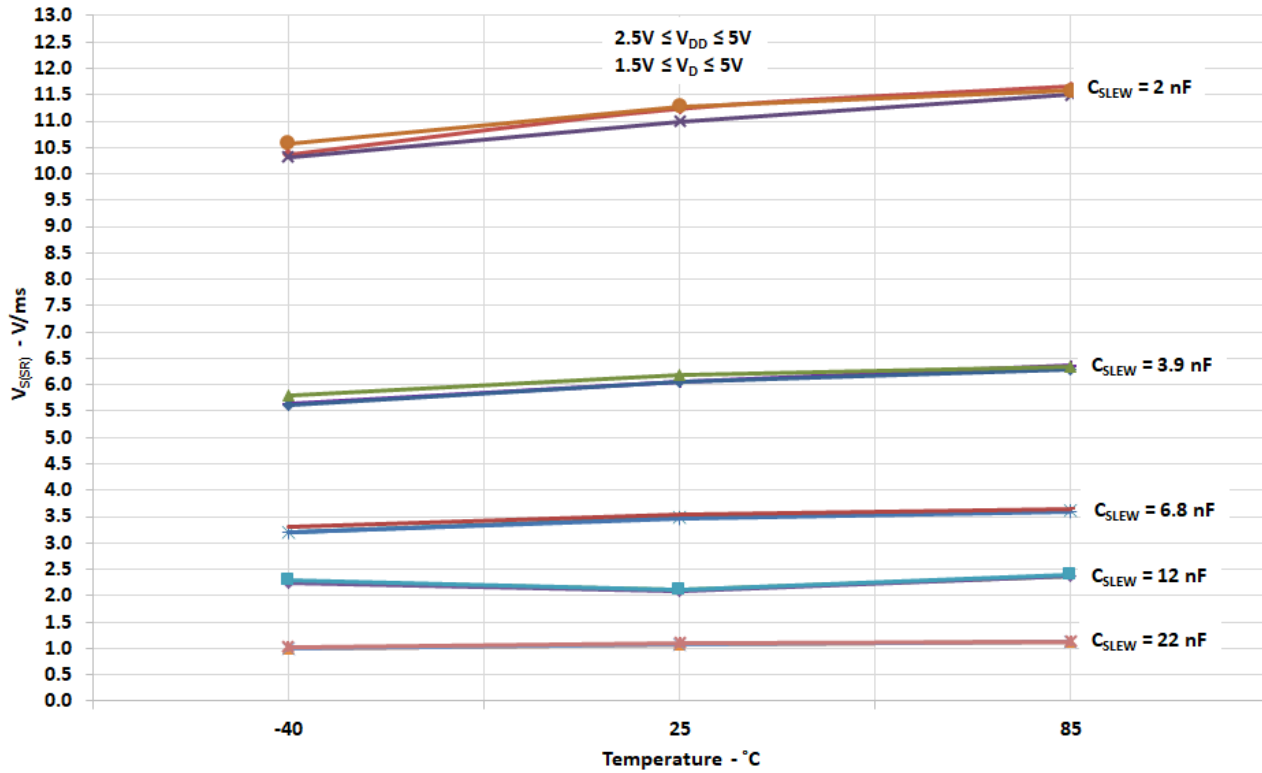
V_{S(SR)} vs. C_{SLEW}, V_{DD}, and V_D



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$V_{S(SR)}$ vs. Temperature, V_{DD} , V_D , and C_{SLEW}



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SLG59M1655V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 μF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the load switch timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

Power Dissipation

The junction temperature of the SLG59M1655V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1655V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \Theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)

Θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)

T_A = Ambient temperature, in Celsius degrees (°C)

For more information on GreenFET load switch features, please visit our website and see App Note “AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics”.

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Layout Guidelines:

1. The VDD pin needs a 0.1 μF and 10 μF external capacitors to smooth pulses from the power supply. Locate these capacitors as close as possible to the SLG59M1655V's PIN4.
2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1655V's D and S pins;
4. The GND pin should be connected to system analog or power ground plane.

SLG59M1655V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1655V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1655V here

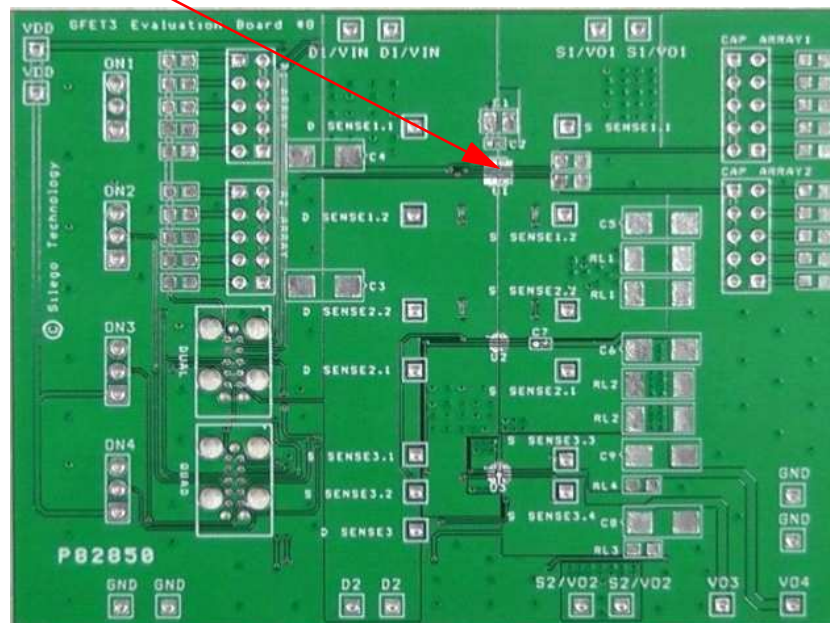


Figure 1. SLG59M1655V Evaluation Board.

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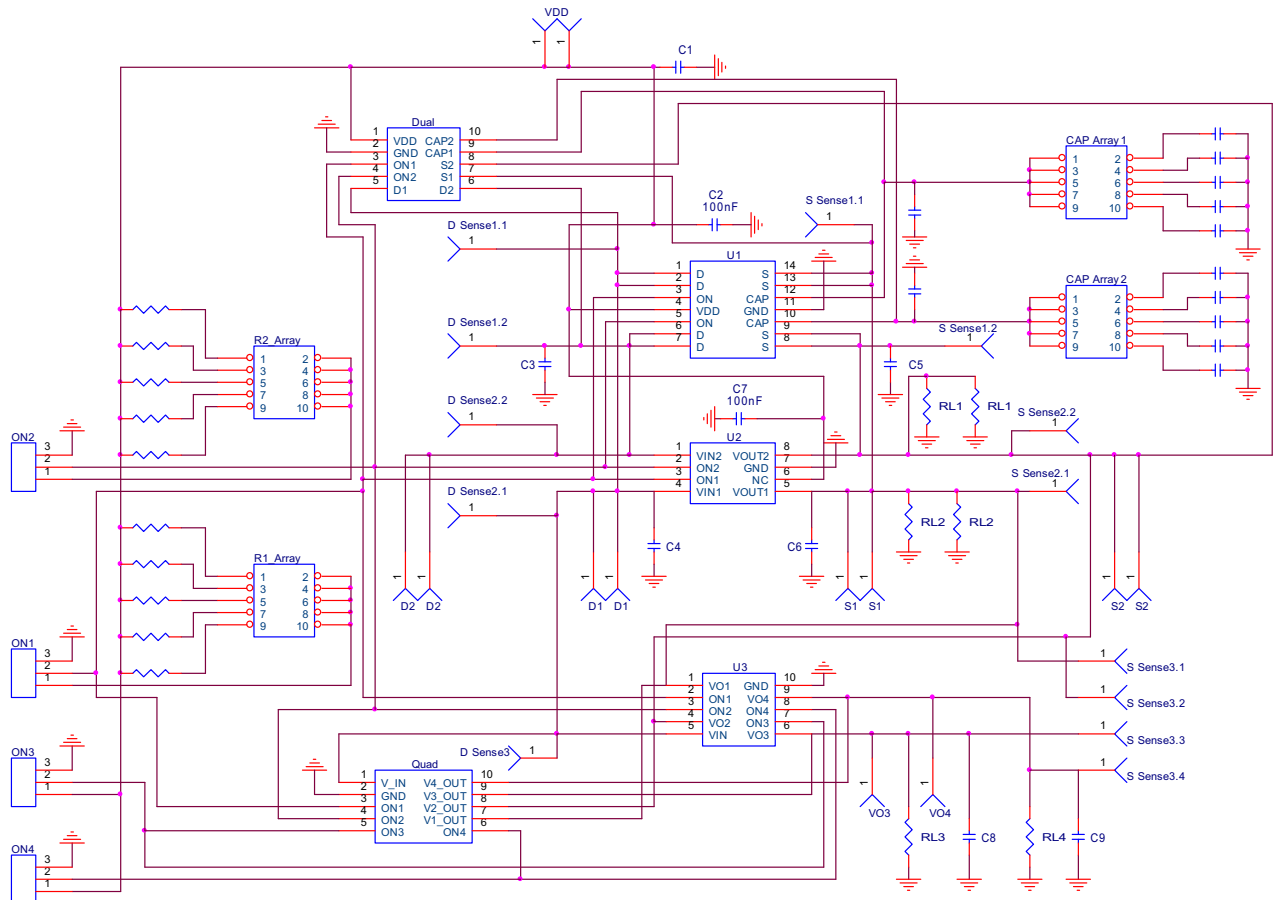


Figure 2. SLG59M1655V Evaluation Board Connection Circuit.

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Basic Test Setup and Connections

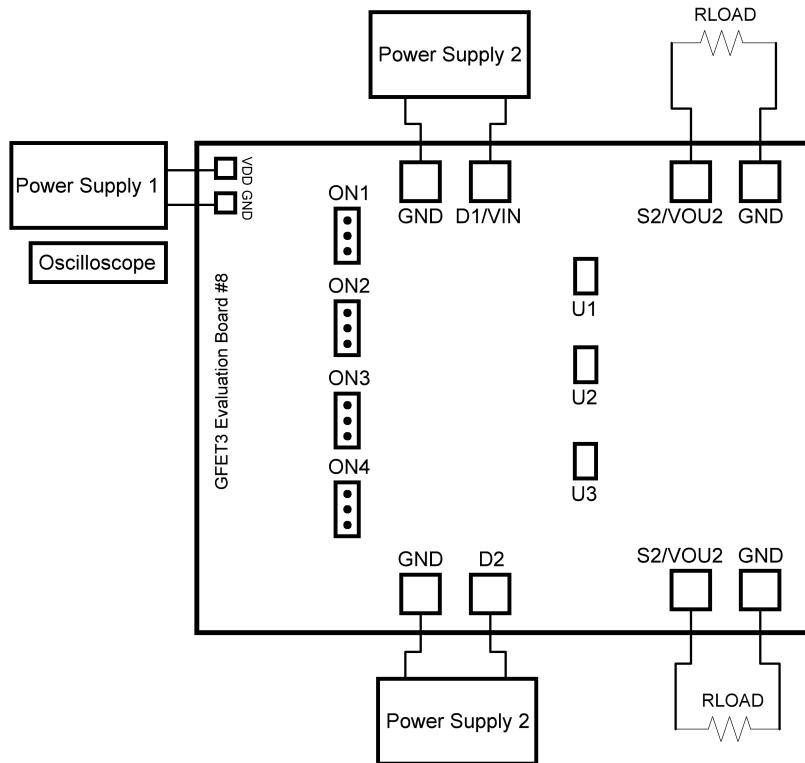


Figure 3. Typical connections for GFET3 Evaluation.

EV B Configuration

1. Connect oscilloscope probes to D1/VIN, D2, S1/VO1, S1/VO2, ON1, ON2 etc.;
2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V...5.5 V range;
3. Turn on Power Supply 2 and set desired V_D from 0.85 V...5.5 V range;
4. Toggle the ON signal High or Low to observe SLG59M1655V operation.

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Package Top Marking System Definition



PP - Part ID Field
 DD- Date Code Field¹
 L - Lot Traceability Code Field¹

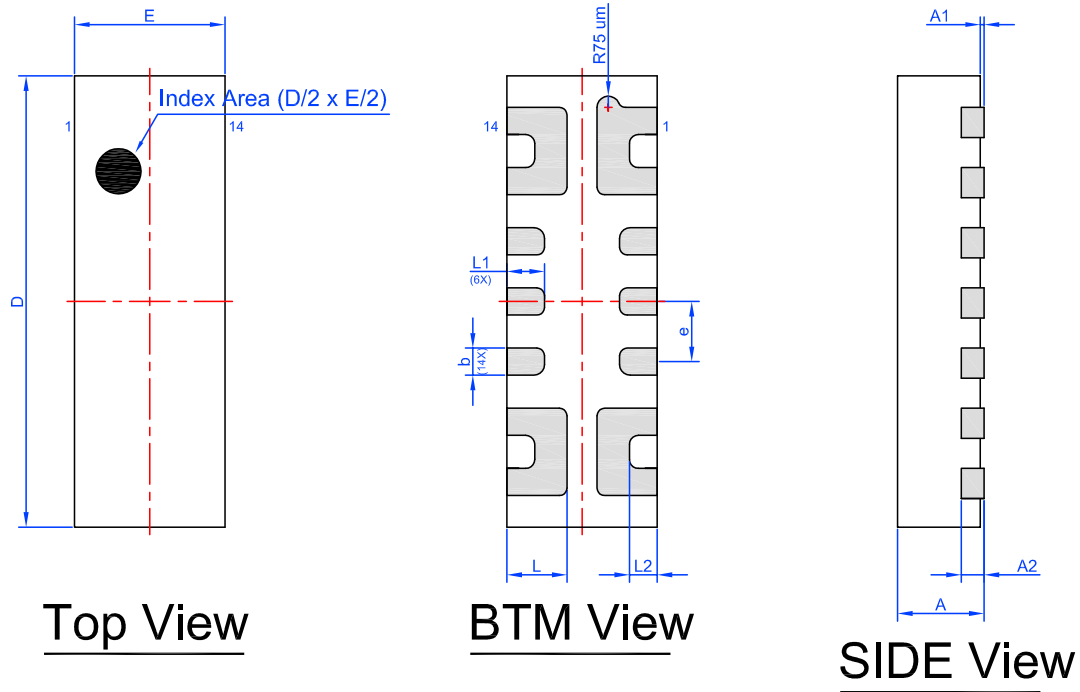
Note 1: Each character in code field can be alphanumeric A-Z and 0-9

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Package Drawing and Dimensions

14 Lead STDFN Package 1 mm x 3 mm (Fused Lead)



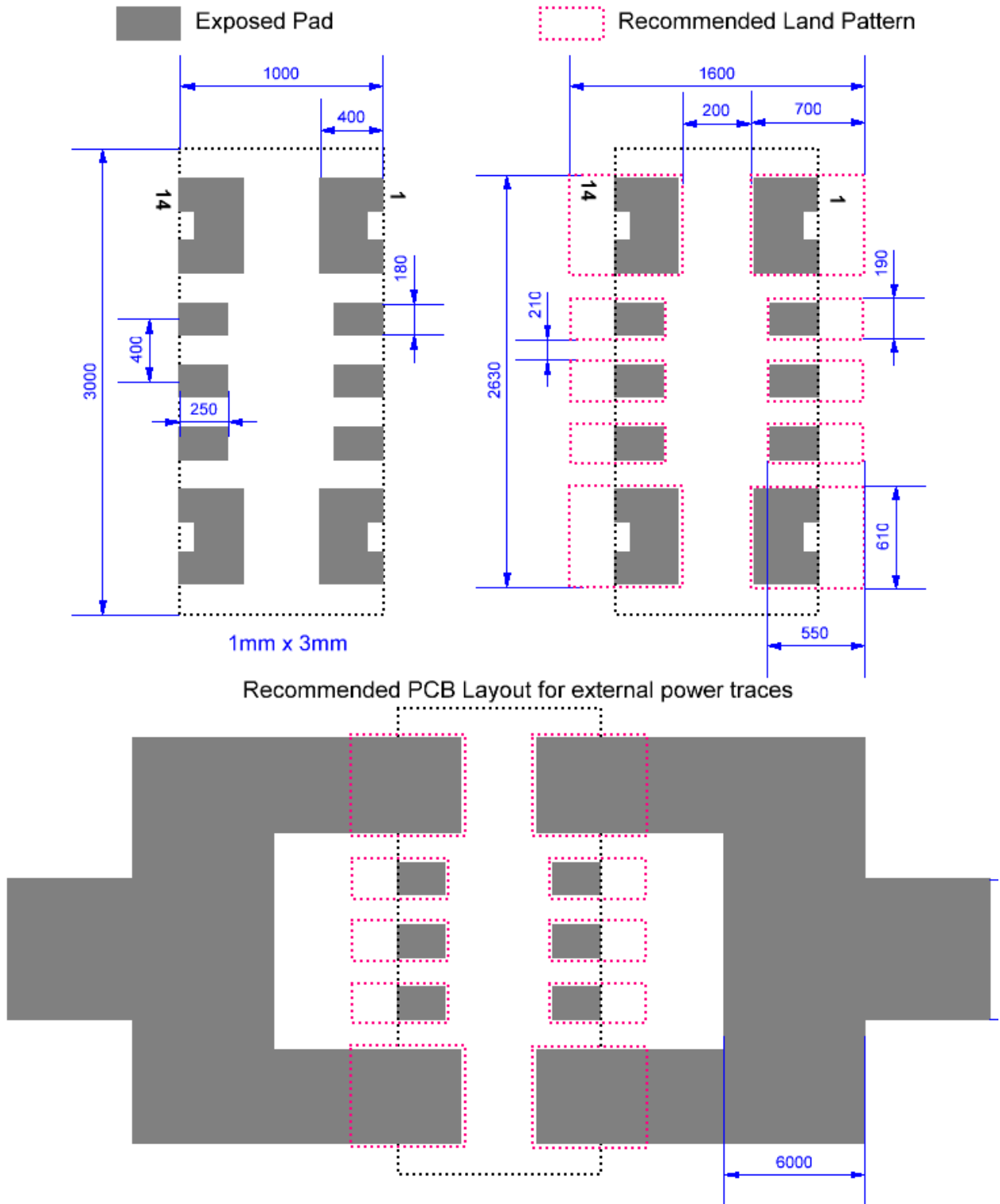
Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|-------|--------|------|------|------|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.050 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.20 | 0.25 | 0.30 |
| e | 0.40 BSC | | | L2 | 0.06 | 0.11 | 0.16 |

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Recommended Land Pattern and PCB Layout



Note: All dimensions are in micrometers (μm)

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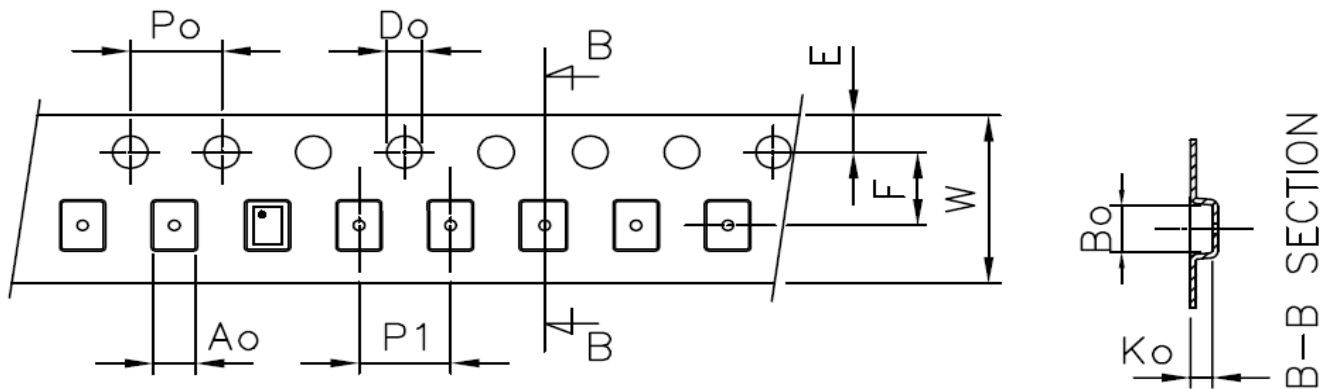
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Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|-------------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STDFN 14L 1x3mm 0.4P FC | 14 | 1x3x0.55mm | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|-------------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 14L 1x3mm 0.4P FC | 1.15 | 3.15 | 0.7 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.65 mm³ (nominal). More information can be found at www.jedec.org.

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Revision History

| Date | Version | Change |
|------------|---------|--|
| 2/3/2022 | 1.04 | Updated Company name and logo Fixed typos |
| 10/12/2018 | 1.03 | Clarified Pin Names Updated style and formatting Added Layout Guidelines |
| 1/20/2016 | 1.02 | Updated IDD values |
| 1/14/2016 | 1.01 | Updated Title, General Description, and Features Updated Pin Descriptions Updated text for clarity |
| 10/7/2015 | 1.00 | Production Release |
| 10/6/2015 | 0.50 | Preliminary Release |
| 10/6/2015 | 0.10 | Advanced Release |

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