# SLG7MD47673

High Voltage High Current H/Half-Bridge Driver

The SLG7MD47673 offers a compact and efficient integrated H/Half-Bridge driver for wide voltage applications up to 26.4 V and 3 A (MAX) output. This device is optimized for various applications where power and size are a critical factor.

The NMOS FETs are integrated in the HV OUT CTRL macro cell allowing for many settings to be configured in detail. Integrating driver FETs and FET control circuitry into a single component, the SLG7MD47673 reduces the component count in motor driver systems, simplifying the design. The device features an EN input interface on IN, providing precise control of motor start functionality. The device also features a low-power sleep mode that can be activated using the INH pin, reducing power consumption when the device is not in use.

Additionally, the device includes important protection features such as undervoltage lockout, overcurrent protection, and thermal shutdown, ensuring reliable and safe operation in various environments.

**This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations visit the GreenPAK website.**

**Click here to download the GreenPAK file for the SLG7MD47673 design.**

**Email GreenPAKSupport@renesas.com for more information and GreenPAK design support.**

## Features

- Two high voltage high current drive GPOs
- Current up to 1.5 A RMS per GPO/H-Bridge
- Low power consumption
- Pb-free/RoHS compliant
- Halogen-free
- STQFN-20 package

## Applications

- Brushed DC motor
- Solenoid
- Washers
- Dryers
- Dishwashers
- Smart meters
- Robotics
- Infusion pumps
- Blood pressure monitor
- Beauty and grooming
- Motor control

## Output Summary

- High Voltage High Current GPO

# Contents

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# 1. Block Diagram

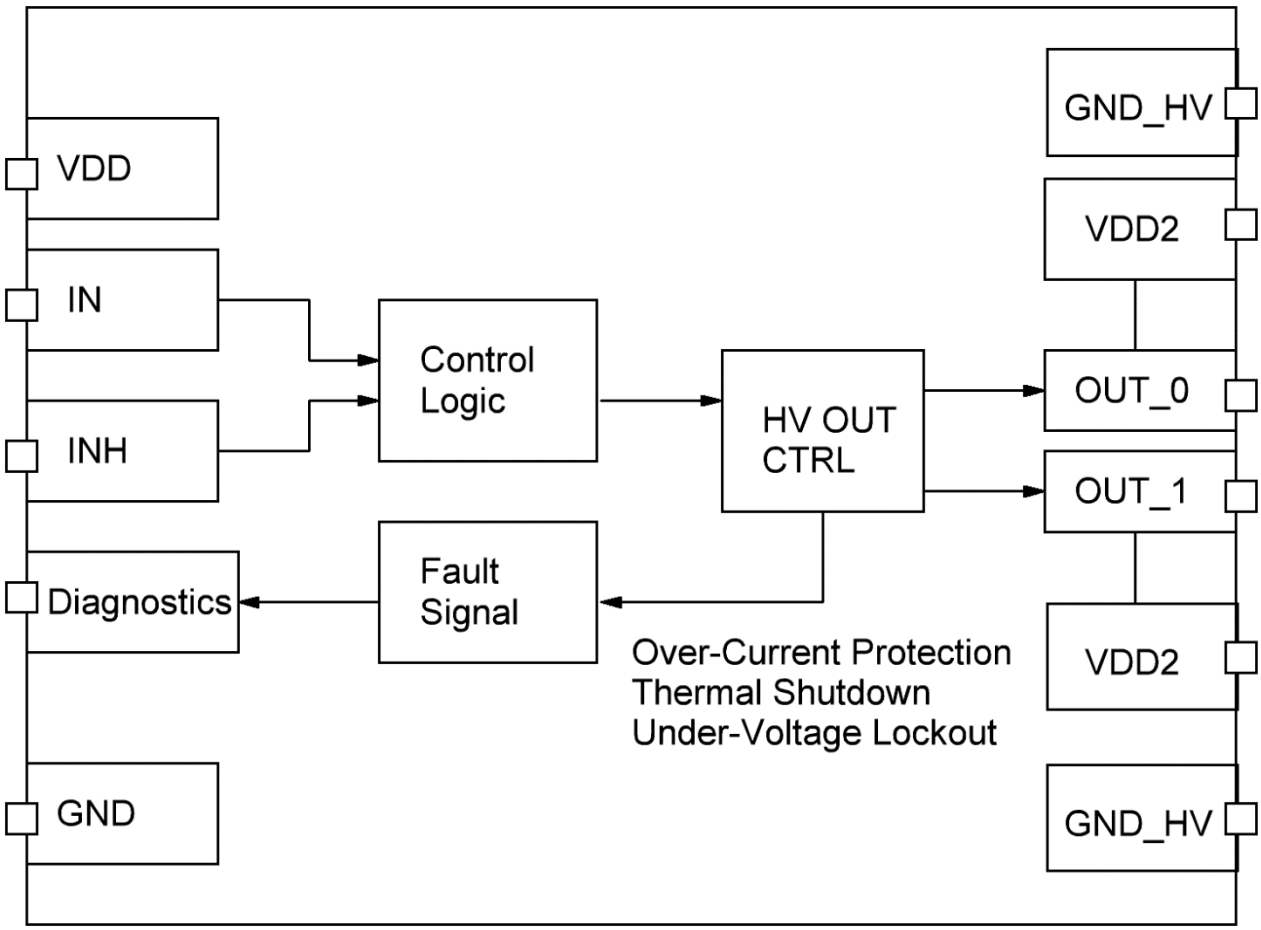



**Figure 1. Block Diagram**

# 2. Pin Information

## 2.1 Pin Assignments

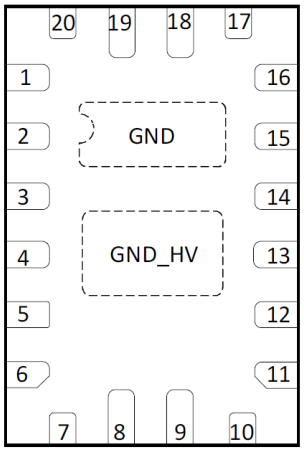



**Figure 2. Pin Assignments**

## 2.2 Pin Descriptions

| Pin # | Pin Name | Type | Description | Internal Resistor |
|---|---|---|---|---|
| 1 | $V_{DD}$ | PWR | Supply Voltage | -- |
| 2 | IN | Digital Input | Digital Input without Schmitt Trigger | Floating |
| 3 | INH | Digital Input | Digital Input without Schmitt Trigger | Floating |
| 4 | GND_HV | GND | Ground | -- |
| 5 | SENSE | Analog Input/Output | Analog Input/Output | Floating |
| 6 | $V_{DD2}$ | PWR | Supply Voltage | -- |
| 7 | OUT0 | High Drive Output | High Drive Push-Pull | Floating |
| 8 | OUT0 | High Drive Output | High Drive Push-Pull | Floating |
| 9 | OUT1 | High Drive Output | High Drive Push-Pull | Floating |
| 10 | OUT1 | High Drive Output | High Drive Push-Pull | Floating |
| 11 | $V_{DD2}$ | PWR | Supply Voltage | -- |
| 12 | SENSE | Analog Input/Output | Analog Input/Output | Floating |
| 13 | GND_HV | GND | Ground | -- |
| 14 | NC | -- | Keep Floating or Connect to GND | -- |
| 15 | NC | -- | Keep Floating or Connect to GND | -- |
| 16 | NC | -- | Keep Floating or Connect to GND | -- |

| Pin # | Pin Name | Type | Description | Internal Resistor |
|---|---|---|---|---|
| 17 | NC | -- | Keep Floating or Connect to GND | -- |
| 18 | GND | GND | Ground | -- |
| 19 | NC | -- | Keep Floating or Connect to GND | -- |
| 20 | Diagnostics | Digital Output | Open-Drain NMOS 1x | Floating |

# 3. Specifications

## 3.1 Absolute Maximum Ratings

| Parameter | | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage on $V_{DD}$ relative to GND | | | | -0.3 | 7.0 | V |
| Supply Voltage on $V_{DD2}$ relative to GND | | | | -0.3 | 28 | V |
| DC Input Voltage | | | | GND - 0.5 | $V_{DD}$ + 0.5 | V |
| Maximum $V_{DD}$ Average or DC Current | | (Through $V_{DD}$ or GND Pin) for $V_{DD}$ Group | | -- | 120 | mA |
| Maximum $V_{DD2}$ Average or DC Current | | Through $V_{DD2}$ or SENSE Pin | | -- | 2000 | mA |
| Maximum Average or DC Current ($V_{DD}$ Power Supply) | OD 1x | Through $V_{DD}$ Group Pins | $T_J$ = -40 °C to 85 °C | -- | 11 | mA |
| | | | $T_J$ = -40 °C to 150 °C | -- | 3.8 | mA |
| Maximum Average or DC Current ($V_{DD2}$ Power Supply) | Push-Pull/ Half Bridge | Through $V_{DD2}$ High Current Group Pins | | -- | 1500 | mA |
| Current at Input Pin | | Through $V_{DD}$ Group Pin | | -0.1 | 1.0 | mA |
| Input Leakage Current (Absolute Value) | | | | -- | 1000 | nA |
| Storage Temperature Range | | | | -65 | 150 | °C |
| Junction Temperature | | | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | | | 4000 | -- | V |
| ESD Protection (Charged Device Model) | | | | 1300 | -- | V |
| Moisture Sensitivity Level | | | | 1 | | |

## 3.2 Thermal Information

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\Theta_{JA}$ | 4L JEDEC PCB | -- | -- | 65 | °C/W |
| | | 4L JEDEC PCB with a thermal vias that connect thermal pad through all layers of the PCB | -- | -- | 56 | °C/W |
| Junction-to-case (top) Thermal Resistance | $\Theta_{JC(top)}$ | | -- | 38.40 | -- | °C/W |
| Junction-to-board Thermal Resistance | $\Theta_{JB}$ | | -- | 34.88 | -- | °C/W |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Junction-to-case (top) Characterization Parameter | $\Psi_{JC(top)}$ | | -- | 13.46 | -- | °C/W |
| Junction-to-board Characterization Parameter | $\Psi_{JB}$ | | -- | 27.24 | -- | °C/W |

## 3.3 Electrical Specifications

| Parameter | Symbol | Condition/Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.3 | 3.3 | 5.5 | V |
| Supply Voltage | $V_{DD2}$ | | 4.5 | 24 | 26.4 | V |
| Operating Temperature | $T_A$ | | -40 | 25 | 85 | °C |
| Capacitor Value at $V_{DD}$ | $C_{VDD}$ | | -- | 0.1 | -- | µF |
| Input Capacitance | $C_{IN}$ | | -- | 2.5 | -- | pF |
| Quiescent Current $V_{DD}$ Side | $I_{Q\_VDD}$ | Static inputs and floating outputs | -- | 1 | -- | µA |
| iHIGH-Level Input Voltage [3] | $V_{IH}$ | Logic Input [1] | 0.7 x $V_{DD}$ | -- | $V_{DD}$ + 0.3 | V |
| LOW-Level Input Voltage [3] | $V_{IL}$ | Logic Input [1] | GND - 0.3 | -- | 0.3 x $V_{DD}$ | V |
| LOW-Level Output Voltage for $V_{DD}$ Group, $T_J$ = -40 °C to 85 °C | $V_{OL}$ | Open-drain NMOS 1x, $I_{OL}$ = 1 mA, at $V_{DD}$ = 2.5 V | -- | -- | 0.030 | V |
| | | Open-drain NMOS 1x, $I_{OL}$ = 3mA, at $V_{DD}$ = 3.3 V | -- | -- | 0.068 | V |
| | | Open-drain NMOS 1x, $I_{OL}$ = 5 mA, at $V_{DD}$ = 5.0 V | -- | -- | 0.083 | V |
| LOW-Level Output Voltage for $V_{DD}$ Group, $T_J$ = -40 °C to 150 °C | | Open-drain NMOS 1x, $I_{OL}$ = 1 mA, at $V_{DD}$ = 2.5 V | -- | -- | 0.035 | V |
| | | Open-drain NMOS 1x, $I_{OL}$ = 3 mA, at $V_{DD}$ = 3.3 V | -- | -- | 0.082 | V |
| | | Open-drain NMOS 1x, $I_{OL}$ = 5 mA, at $V_{DD}$ = 5.0 V | -- | -- | 0.100 | V |
| HIGH-Level Output Voltage for $V_{DD2}$ High Current Group | $V_{OH2}$ | Push-Pull, $V_{DD2}$ = 5 ± 10 %, $I_{OH2}$ = 10 mA | 4.5 | -- | -- | V |
| | | Push-Pull, $V_{DD2}$ = 9 V ± 10 %, $I_{OH2}$ = 10 mA | 8.1 | -- | -- | V |
| | | Push-Pull, $V_{DD2}$ = 12 V ± 10 %, $I_{OH2}$ = 10 mA | 10.8 | -- | -- | V |
| | | Push-Pull, $V_{DD2}$ = 18 V ± 10 %, $I_{OH2}$ = 10 mA | 16.2 | -- | -- | V |
| | | Push-Pull, $V_{DD2}$ = 24 V ± 10 %, $I_{OH2}$ = 10 mA | 21.6 | -- | -- | V |

| Parameter | Symbol | Condition/Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LOW-Level Output Voltage for $V_{DD2}$ High Current Group | $V_{OL2}$ | Push-Pull, $V_{DD2}$ = 5 ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| | | Push-Pull, $V_{DD2}$ = 9 V ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| | | Push-Pull, $V_{DD2}$ = 12 V ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| | | Push-Pull, $V_{DD2}$ = 18 V ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| | | Push-Pull, $V_{DD2}$ = 24 V ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| LOW-Level Output Pulse Current [2] Voltage for $V_{DD}$ Group, $T_J$ = -40 °C to 85 °C | $I_{OL}$ | Open-drain NMOS 1x, $V_{OL}$ = 0.15 V, at $V_{DD}$ = 2.5 V | 4.7 | -- | -- | mA |
| | | Open-drain NMOS 1x, $V_{OL}$ = 0.4 V, at $V_{DD}$ = 3.3 V | 15.2 | -- | -- | mA |
| | | Open-drain NMOS 1x, $V_{OL}$ = 0.4 V, at $V_{DD}$ = 5.0 V | 21.8 | -- | -- | mA |
| LOW-Level Output Pulse Current [2] Voltage for $V_{DD}$ Group, $T_J$ = -40 °C to 150 °C | | Open-drain NMOS 1x, $V_{OL}$ = 0.15 V, at $V_{DD}$ = 2.5 V | 4.0 | -- | -- | mA |
| | | Open-drain NMOS 1x, $V_{OL}$ = 0.4 V, at $V_{DD}$ = 3.3 V | 12.8 | -- | -- | mA |
| | | Open-drain NMOS 1x, $V_{OL}$ = 0.4 V, at $V_{DD}$ = 5.0 V | 18.3 | -- | -- | mA |
| Delay Time | $T_{DLYED1}$ | At temperature 25 °C | 3.84 | 4.02 | 4.27 | µs |
| | | At temperature -40 °C to 85 °C[4] | 3.76 | 4.02 | 4.34 | µs |
| Startup Time | $T_{SU}$ | From $V_{DD}$ rising past $PON_{THR}$ | -- | 0.91 | 1.20 | ms |
| Power-On Threshold | $PON_{THR}$ | $V_{DD}$ level required to start up the chip | 1.80 | 1.98 | 2.20 | V |
| Power-Off Threshold | $POFF_{THR}$ | $V_{DD}$ level required to switch off the chip | 1.30 | 1.55 | 1.80 | V |

**[1]** No hysteresis.
**[2]** DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
**[3]** ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect $V_{IH}$ and $V_{IL}$.
**[4]** Guaranteed by Design.

## 3.4 HV Output Electrical Specifications (Full Bridge or Half Bridge Modes)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rise Time HV OUT in Motor Driver Mode | $t_R$ | $V_{DD2}$ = 5 V, 16 Ω to GND, 10 % to 90 % $V_{DD2}$, $T_J$ = -40 °C to 150 °C | 56 | 107 | 168 | ns |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fall Time HV OUT in Motor Driver Mode | $t_F$ | $V_{DD2}$ = 5 V, 16 Ω to GND, 90 % to 10 % $V_{DD2}$, $T_J$ = -40 °C to 150 °C | 57 | 129 | 216 | ns |
| Dead Band Time of OUT0/OUT1 in Motor Driver Mode | $T_{DEAD}$ | $V_{DD2}$ = 4.5 V, $T_J$ = -40 °C to 150 °C | -- | 91 | -- | ns |
| | | $V_{DD2}$ = 12 V, $T_J$ = -40 °C to 150 °C | -- | 85 | -- | ns |
| | | $V_{DD2}$ = 26.4 V, $T_J$ = -40 °C to 150 °C | -- | 121 | -- | ns |
| Dead Band Time, Generated by PWM Block | PWM_$t_{DEAD}$ | Configured in PWM block | 0; 1·$T_{clk}$ | 2·$T_{clk}$ | 3·$T_{clk}$ | CLK time |
| HS FET on Resistance (SENSE, GND_HV, and GND Pins are Connected Together) | $R_{DS(ON)}$ | $V_{DD2}$ = 4.5 V to 5.5 V, $I_O$ = 500 mA, $T_J$ = 25 °C | -- | 240 | -- | mΩ |
| | | $V_{DD2}$ = 4.5 V to 5.5 V, $I_O$ = 500 mA, $T_J$ = 150 °C | -- | 276 | 336 | mΩ |
| | | $V_{DD2}$ = 5.5 V to 26.4 V, $I_O$ =500 mA, $T_J$ = 25 °C | -- | 239 | -- | mΩ |
| | | $V_{DD2}$ = 5.5 V to 26.4 V, $I_O$ =500 mA, $T_J$ = 150 °C | -- | 276 | 336 | mΩ |
| LS FET on Resistance (SENSE, GND_HV, and GND Pins are Connected Together, $R_{DS(ON)}$ with Sense Pin = GND, if Sense Pin $V_{DD}$ = 0.5 V, Additional 100 mΩ at Worst Case) | $R_{DS(ON)}$ | $V_{DD2}$ = 4.5 V to 5.5 V, $I_O$ = 500 mA, $T_J$ = 25 °C | -- | 239 | -- | mΩ |
| | | $V_{DD2}$ = 4.5 V to 5.5 V, $I_O$ = 500 mA, $T_J$ = 150 °C | -- | 274 | 338 | mΩ |
| | | $V_{DD2}$ = 5.5 V to 26.4 V, $I_O$ =500 mA, $T_J$ = 25 °C | -- | 235 | -- | mΩ |
| | | $V_{DD2}$ = 5.5 V to 26.4 V, $I_O$ =500 mA, $T_J$ = 150 °C | -- | 270 | 327 | mΩ |
| Off-state Leakage Current | $I_{OFF}$ | OUT0, OUT1 [1], $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 85 °C, PWM is off, including the charge pump OSC | 0 | -- | 9.3 | µA |
| | | GPO0_HD, GPO1_HD [1], $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C, PWM is off, including the charge pump OSC | 0 | -- | 10.2 | µA |
| Single HV Driver Current Consumption (Including Support Circuits), without Output Load | $I_{DD2}$ | $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C Static (PWM is off), including the charge pump OSC | -- | -- | 115.9 | µA |
| | | $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C Switching (PWM = 250 kHz) | -- | 0.7 | 1.4 | mA |
| Wake-up Time | $t_{WAKE}$ | HV SLEEP OUT high to output transition, BG is always on, another pins SLEEP - disable | -- | 80 | 130 | µs |

**[1]** There is a resistive voltage divider in front of Diff Amplifier that is connected to OUT0 and OUT1.

## 3.5 Protection Circuits

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Overcurrent Protection Threshold | $I_{OCP}$ | Per any HS or LS FET | -- | 3.0 | -- | A |
| OCP Deglitch Time | $t_{OCP1}$ | $V_{DD}$ = 5 V, $V_{DD2}$ = 5 V, T = 25 °C, Deglitch = Enable, High Side | -- | 2.50 | -- | µs |
| | | $V_{DD}$ = 5 V, $V_{DD2}$ = 5 V, T = 25 °C, Deglitch = Enable, Low Side | -- | 1.23 | -- | µs |
| OCP Retry Time | $t_{OCP2}$ | Delay = 492 µs | -- | 491 | -- | µs |
| Recover from Undervoltage Lockout | $V_{UVLO}$ | At rising edge of $V_{DD2}$ | -- | 2.78 | 2.9 | V |
| Undervoltage Lockout | | At falling edge of $V_{DD2}$ | -- | 2.66 | 2.8 | V |
| Thermal Shutdown Temperature | $T_{TSD}$ | Junction temperature $T_J$ | 135.0 | 147.4 | 159.2 | °C |
| Thermal Shutdown Hysteresis | $T_{HYST}$ | | -- | 16.2 | -- | °C |

# 4. Typical Application Circuit

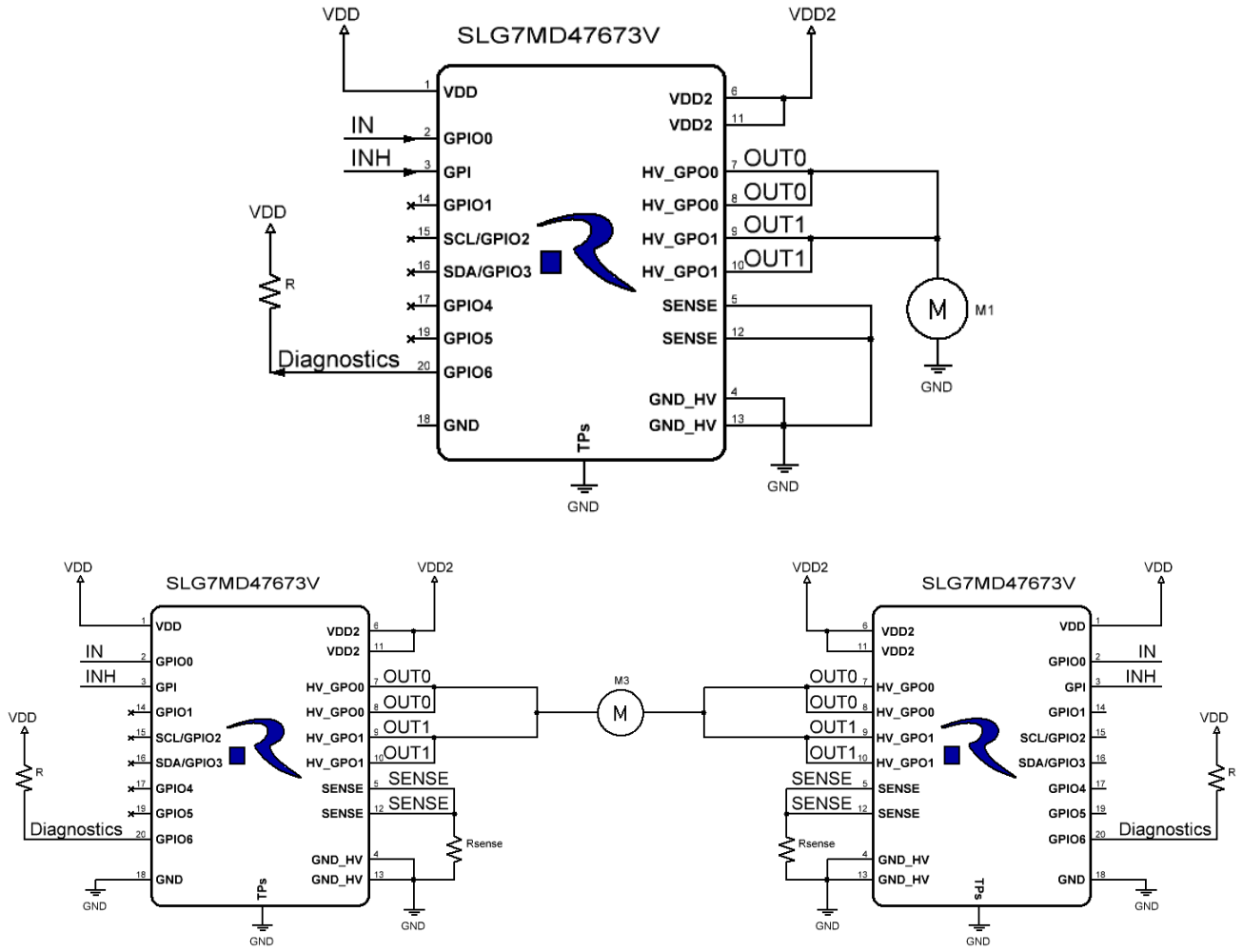
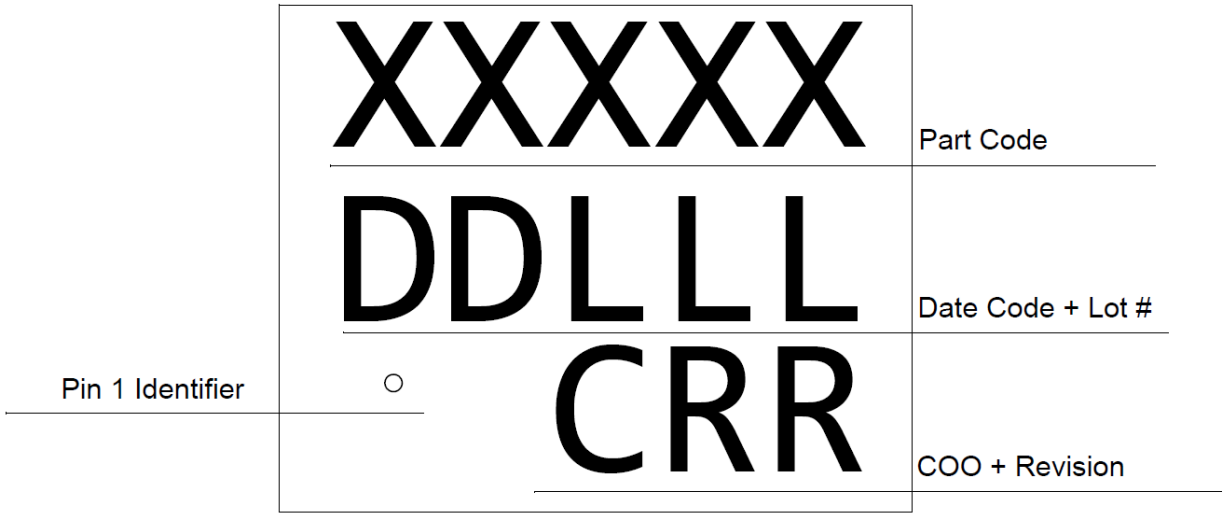



**Figure 3. Typical Application Circuit**

# 5. Package Top Marking Definitions




XXXXX - Part ID Field identifies the specific device configuration

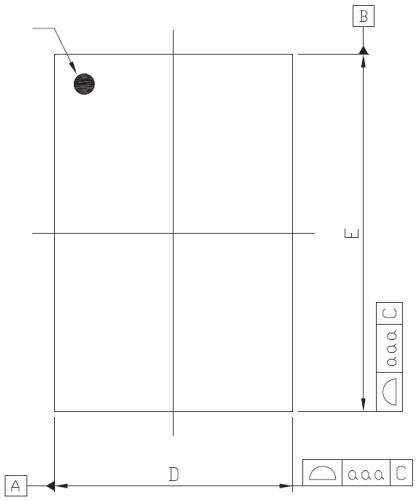
| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|---|---|---|---|---|---|---|
| 1.00 | 001 | U | 0xFEF77904 | | | 6/26/2024 |

Lock coverage for this part is indicated by √, from one of the following options:

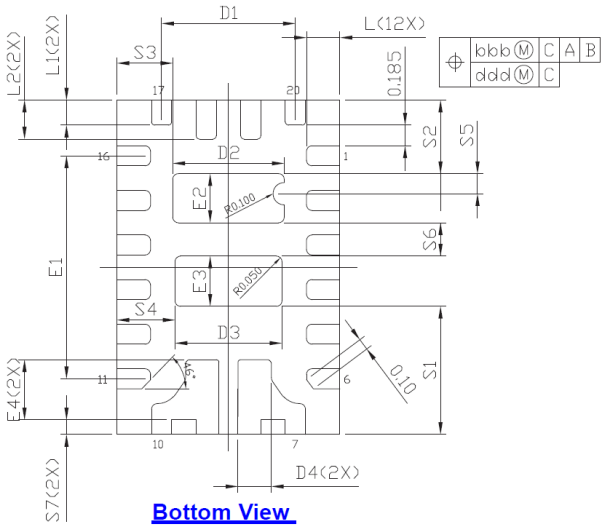
| | |
|---|---|
| √ | Unlocked |
| | Partly lock read (mode 1) |
| | Partly lock read2 (mode 2) |
| | Partly lock read2/write (mode 3) |
| | All lock read (mode 4) |
| | All lock write (mode 5) |
| | All lock read/write (mode 6) |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

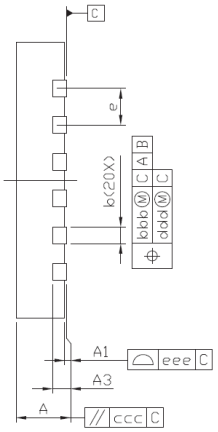
# 6. Package Outlines




Top View




Bottom View




Side View

Notes:

1. All dimensions are in millimeters.

2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.

3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminal.

Controlling dimension: mm

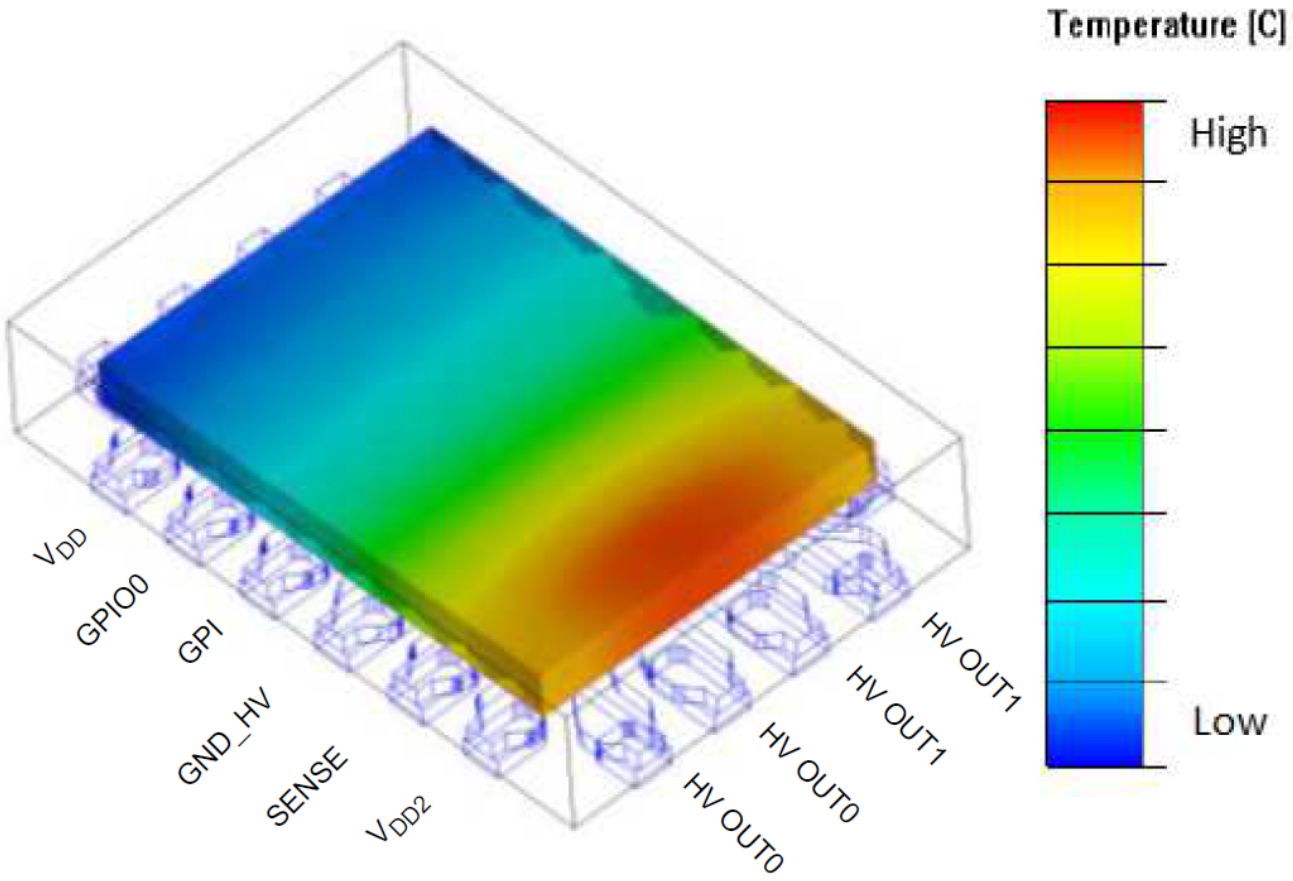
| Symbol | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | Min | Nom. | Max | Min | Nom. | Max |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.000 | 0.020 | 0.050 | 0.000 | 0.001 | 0.002 |
| A3 | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 1.95 | 2.00 | 2.05 | 0.077 | 0.079 | 0.081 |
| E | 2.95 | 3.00 | 3.05 | 0.116 | 0.118 | 0.120 |
| D1 | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| E1 | 1.95 | 2.00 | 2.05 | 0.077 | 0.079 | 0.081 |
| D2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| E2 | 0.39 | 0.44 | 0.49 | 0.015 | 0.017 | 0.019 |
| D3 | 0.91 | 0.96 | 1.01 | 0.036 | 0.038 | 0.040 |
| E3 | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| D4 | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| E4 | 0.49 | 0.54 | 0.59 | 0.019 | 0.021 | 0.023 |
| S1 | 1.10 | 1.15 | 1.20 | 0.043 | 0.045 | 0.047 |
| S2 | 0.61 | 0.66 | 0.71 | 0.024 | 0.026 | 0.028 |
| S3 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| S4 | 0.47 | 0.52 | 0.57 | 0.018 | 0.020 | 0.022 |
| S5 | 0.180 REF | | | 0.007 REF | | |
| S6 | 0.300 REF | | | 0.012 REF | | |
| S7 | 0.131 REF | | | 0.005 REF | | |

“A1” max lead coplanarity 0.05 mm
Standard tolerance: ±0.05

| Symbol | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | Min | Nom. | Max | Min | Nom. | Max |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.250 | 0.300 | 0.350 | 0.010 | 0.012 | 0.014 |
| L1 | 0.175 | 0.225 | 0.275 | 0.007 | 0.009 | 0.011 |
| L2 | 0.300 | 0.350 | 0.400 | 0.012 | 0.014 | 0.016 |
| b | 0.130 | 0.180 | 0.230 | 0.005 | 0.007 | 0.009 |
| aaa | 0.07 | | | 0.003 | | |
| bbb | 0.07 | | | 0.003 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.05 | | | 0.002 | | |
| eee | 0.08 | | | 0.003 | | |

# 7. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to 85 °C. To guarantee reliable operation, the junction temperature of the SLG7MD47673 must not exceed 150 °C.



# 8. Layout Consideration

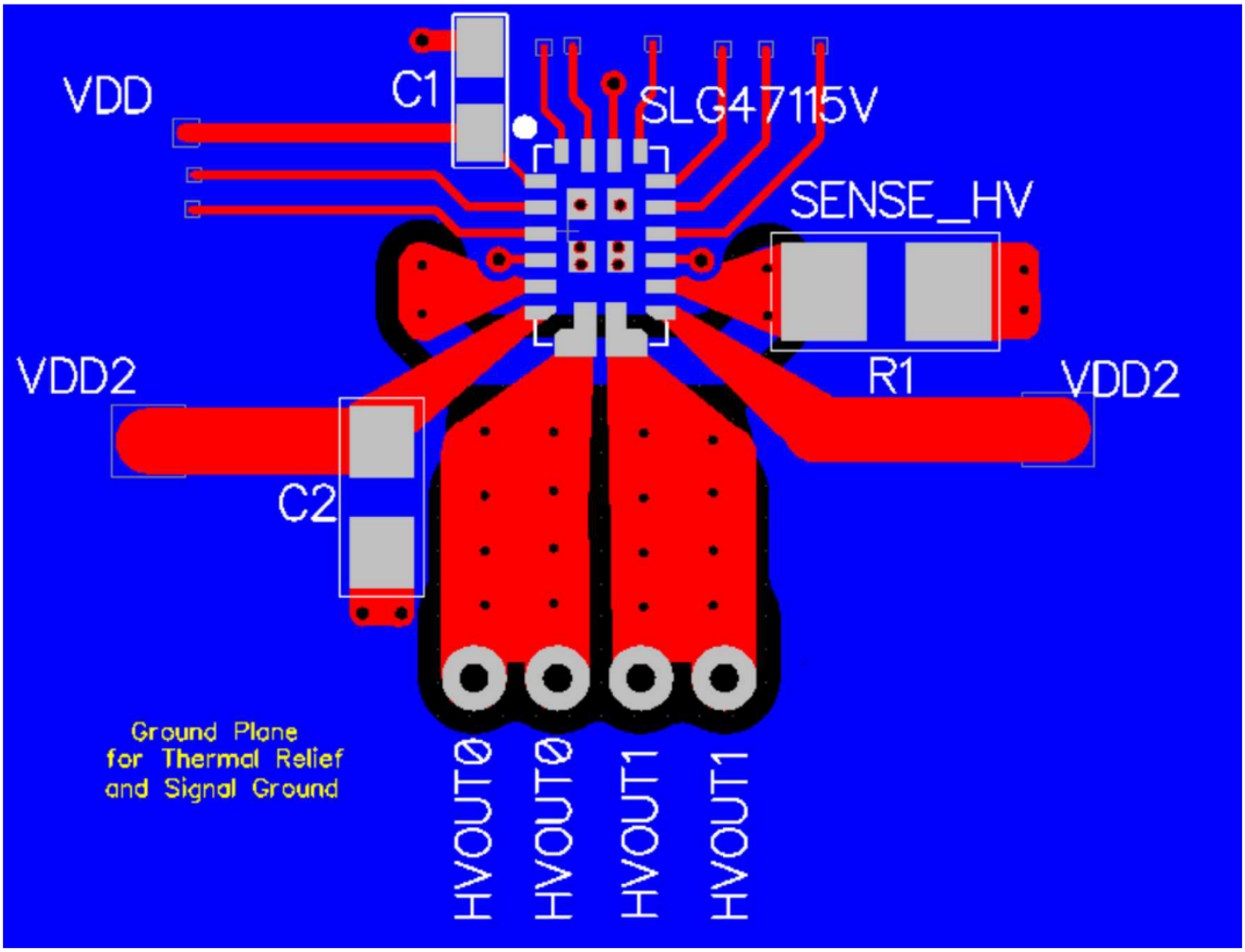
PCB should have enough ground plane to dissipate heat. SLG7MD47673 has two additional pads, which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.

The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters.

It is highly recommended to place low-ESR capacitor between $V_{DD2}$ and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it is highly recommended to place 0.1 µF ceramic capacitor between $V_{DD}$ and GND.

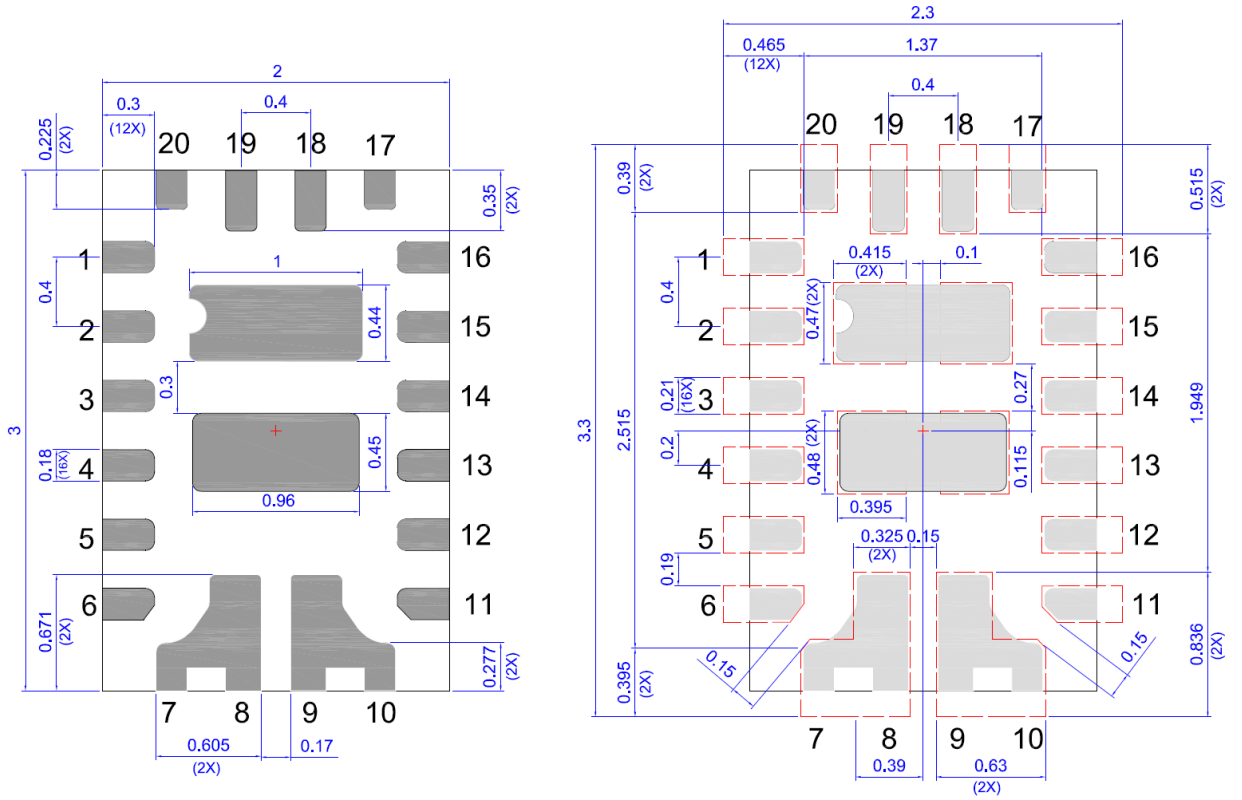
## 8.1 PCB Layout Example



# 9. Layout Guidelines

Expose Pad
(Package face down)

Recommended Landing Pattern
(Package face down)




## 9.1 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020. More information can be found at www.jedec.org.

# 10. Ordering Information

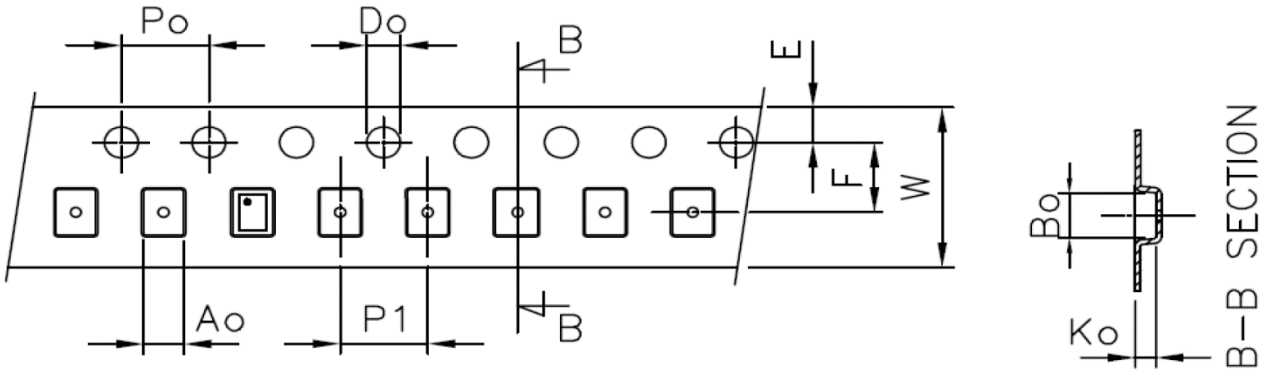
| Part Number | Temperature Range |
|---|---|
| SLG7MD47673V | 20-pin STQFN - Tape and Reel (3k units) |

## 10.1 Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green | 20 | 2.0x3.0x0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

## 10.2 Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



# 11. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Jun 26, 2024 | Initial release |